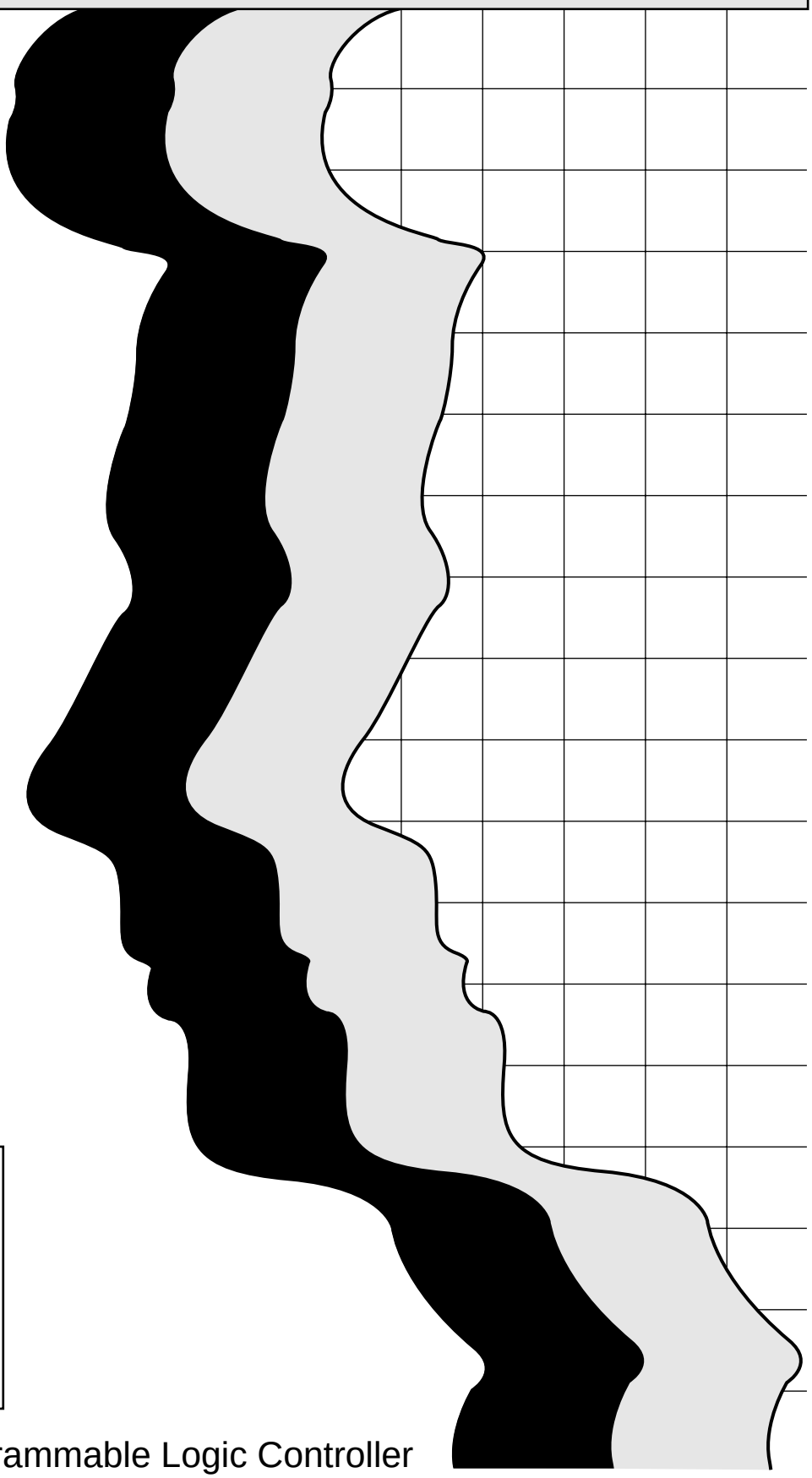
MITSUBISHI

# High Speed Counter Module Type AD62C

# User's Manual



MELSEC

Mitsubishi Programmable Logic Controller

# • SAFETY PRECAUTIONS •

(Always read before starting use.)

Before using this product, please read this manual introduced in this manual carefully and pay full attention to safety to handle the product correctly.
The instructions given in this manual are concerned with this product. For the safety instructions of the programmable controller system, please read the user's manual for the CPU module to use.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

| | |
|---|---|
| ⚠ DANGER | Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury. |
| ⚠ CAUTION | Indicates that incorrect handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage. |

Note that the ⚠CAUTION level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please store this manual in a safe place and make it accessible when required. Always forward it to the end user.

## [DESIGN PRECAUTIONS]

### ⚠ DANGER

- Do not write data into the "system area" of the buffer memory of intelligent function modules. Writing data into the "system area" may cause a PLC system malfunction.
- Depending on the malfunction of the external output transistor, there may be cases where the output is ON or OFF status. Install external monitoring circuitry for output signals that may lead to major accidents.

### ⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 150 mm(5.9 inch) or more from each other.
  Not doing so could result in noise that may cause malfunction.

## [INSTALLATION PRECAUTIONS]

**⚠ CAUTION**

- Securely fix the module with a DIN rail or mounting screws, and securely tighten the mounting screws in the specified torque range.
- Switch all phases of the external power supply off when mounting or removing the module. Not ding so may cause electric shock or damage to the module.
- Do not directly touch the conductive area or electronic components of the module. Doing so may cause malfunction or failure in the module.

## [WIRING PRECAUTIONS]

**⚠ CAUTION**

- Perform correct pressure-displacement, crimp-contact or soldering for connector wire connections using the tools specified by the manufactures.
  Attach connectors to the module securely.
- Be careful not to let foreign matters such as sawdust or wire chips get inside the module. They may cause fires, failure or malfunction.
- The top surface of the module is covered with protective film to prevent foreign objects such as cable offcuts from entering the module when wiring.
  Do not remove this film until the wiring is complete.
  Before operating the system, be sure to remove the film to provide adequate heat ventilation.
- Be sure to fix communication cables or power supply cables leading from the module by placing them in the duct or clamping them.
  Cables not placed in the duct or without clamping may hang or shift, allowing them to be accidentally pulled, which may cause a module malfunction and cable damage.
- When removing the communication cable from the module, do not pull the cable. When removing the cable with a connector, hold the connector on the side that is connected to the modules.
  Pulling the cable that is still connected to the module may cause malfunction or damage to the module or cable.

## [WIRING PRECAUTIONS]

### ⚠ CAUTION

- Always ground the shielded cable on the encoder side (relay box).
  Otherwise, malfunction may occur.
- When wiring, be sure to verify the rated voltage of the product as well as the terminal layout. Fire or failure may result if incorrect voltage is input or incorrect wiring is performed.
- Connecting terminals with incorrect voltage may result in malfunction or mechanical failure.

## [STARTUP/MAINTENANCE PRECAUTIONS]

### ⚠ CAUTION

- Do not disassemble or modify the module.
  Doing so could cause failure, malfunction, injury or fire.
- Switch all phases of the external power supply off when mounting or removing the module.
  Not doing so may cause failure or malfunction of the module.
- Do not touch the connector while the power is on.
  Doing so may cause malfunction.
- Switch all phases of the external power supply off when cleaning or retightening the terminal screws and module installation screws.
  Not doing so may cause failure or malfunction of the module.
  If the screws are loose, it may cause the module to fallout, short circuits, or malfunction.
  If the screws are tightened too much, it may cause damages to the screws and/or the module, resulting in the module falling out, short circuits or malfunction.
- Always make sure to touch the grounded metal to discharge the electricity charged in the body, etc., before touching the module.
  Failure to do so may cause a failure or malfunctions of the module.

## [DISPOSAL PRECAUTIONS]

### ⚠ CAUTION

- When disposing of the product, handle it as industrial waste.

## REVISIONS

*The manual number is given on the bottom left of the back cover.

| Print Date | *Manual Number | Revision |
|---|---|---|
| Dec.,1992 | IB (NA) 66400-A | First edition |
| Oct ., 2004 | IB (NA) 66400-B | Partial Correction<br>Chapter 1,Section 3.5.4, 3.5.5, Chapter 6, Section 6.1.1, 6.1.2, Section 6.1.3, 6.2.1, 6.2.2, 6.2.3, 6.3.1, 6.3.2, 6.4.2, 6.5, 6.5.1, Section 6.5.2, 6.5.3, 6.5.4, 6.5.5, 6.5.6, 6.5.7, 7.1.1, 7.1.2, Section 7.2, 7.2.1, 7.2.2, 7.3.1, 7.3.2, 7.3.3, 7.4, 7.4.1, 7.4.2, Section 7.5.2, 7.6, 7.6.1, 7.6.2, 7.6.3, 7.6.4, 7.6.5, 7.6.6, 7.6.7, Section 8.2, 8.5.2, 9.1<br><br>Addition<br>SAFETY PRECAUTIONS, WARRANTY |
| | | |

Japanese Manual Version IB-68348-B

# INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

## CONTENTS

# 1. GENERAL DESCRIPTION

This manual describes the specifications, handling, and programming of the AD62C high-speed counter (hereafter called the AD62C).

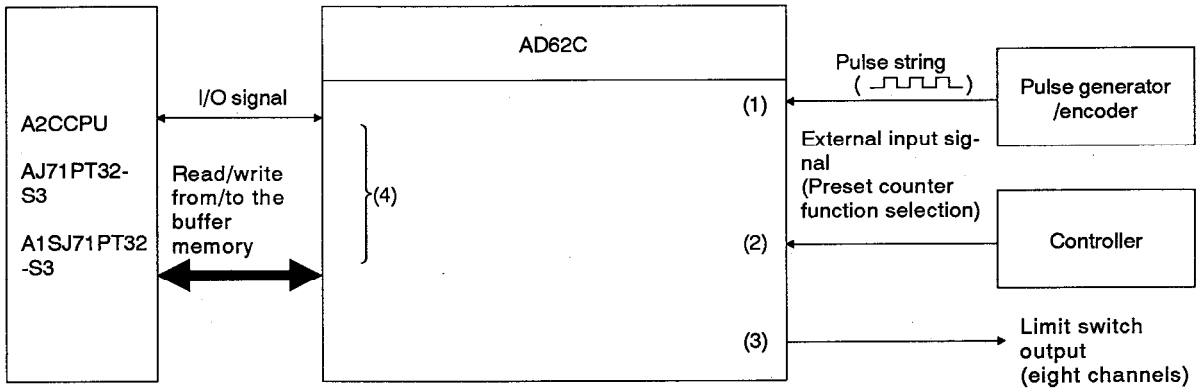
This unit is used in the following three combinations:

- Combined with an A2CCPU
- Combined with an AnSH/A2US(H)/Q2AS(H)/AnA/AnU/QnA CPU (using dedicated instructions) and an A1S/AJ71PT32-S3
- Combined with an ACPU and an AJ71PT32-S3 (A1S/A2SCPU and A1SJ71PT32-S3)

The AD62C counts 1-phase and 2-phase pulse inputs in the following ways:

- 1-phase pulse input : Counts the pulse at the leading edge;
- 2-phase pulse input multiplied by one : Counts the pulse at the leading edge of phase A;
- 2-phase pulse input multiplied by two : Counts the pulse at the leading edge/fall of phase A;
- 2-phase pulse input multiplied by four : Counts the pulse at the leading edge/fall of phases A and B.

The following diagram shows how the AD62C operates in combination.



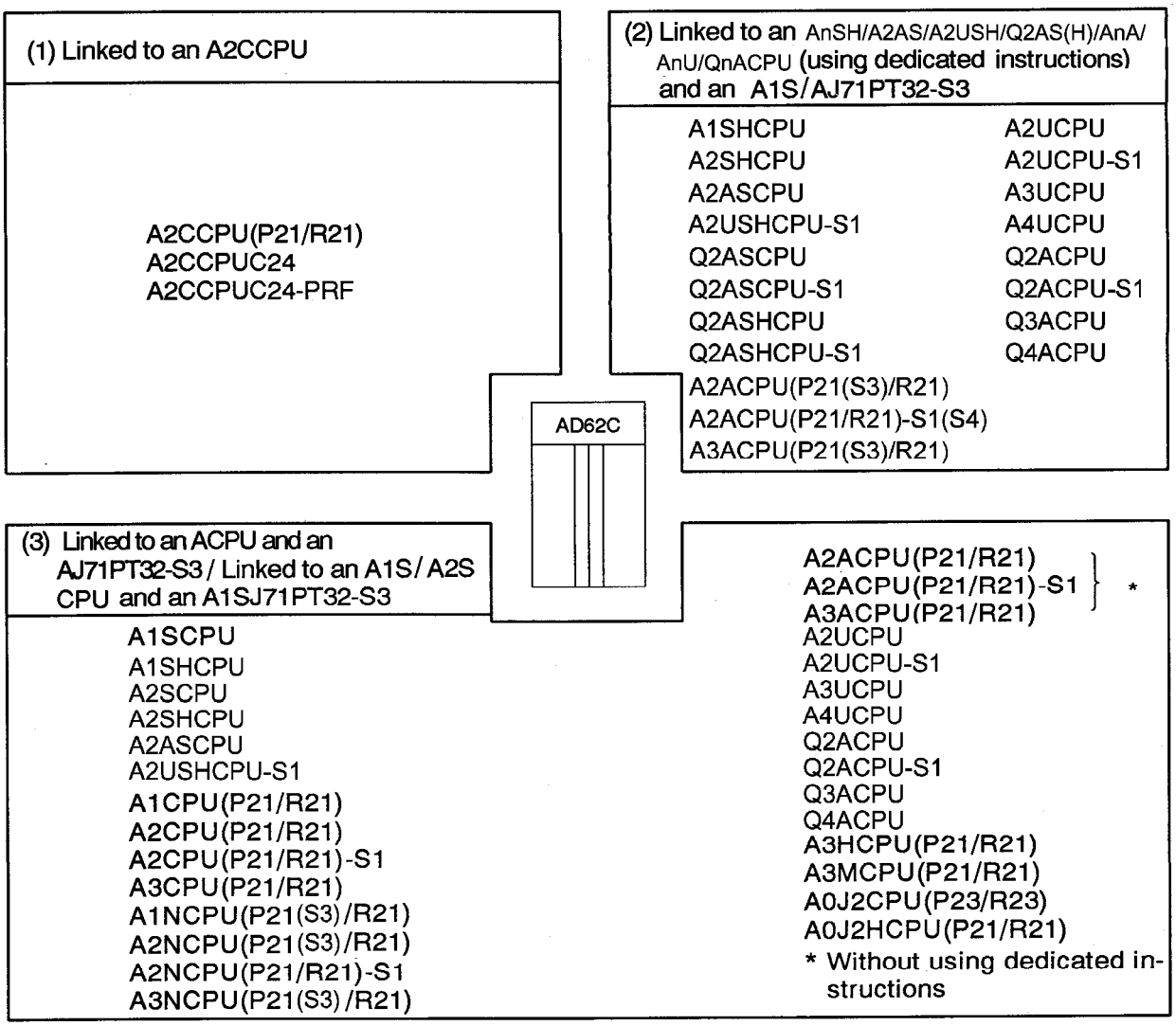

(1) Counts pulses input to the AD62C.

(2) External input signal allows preset/counter selection.

(3) Allows comparison with the counter's present value and outputs the signal using the limit switch.

(4) Allows confirmation of the AD62C I/O signals and the buffer memory using a sequence program. Start/stop or preset counter operations may also be performed.

The following chart shows CPU modules which can be used with the AD62C. They are classified by linkage.




Refer to the following manuals when using the AD62C.

| Manual Title | |
|---|---|
| type ACPU/QCPU-A (A mode) (Fundamentals) Programming Manual | IB-66249 |
| type ACPU/QCPU-A (A mode) (Common Instructions) Programming Manual | IB-66250 |
| type AnSHCPU/AnACPU/AnUCPU/QCPU-A (A Mode) (Dedicated Instructions) Programming Manual | IB-66251 |
| User's Manual for each CPU module | - |
| MELSECNET/MINI-S3 master module type AJ71PT32-S3, AJ71T32-S3, A1SJ71PT32-S3, A1SJ71T32-S3 User's Manual | IB-66565 |
| SW0GP-MINIPE Operating Manual | IB-66226 |

## 1.1 Features

(1) Pulses can be counted within a wide range, from –2147483648 to 2147483647

The count value is stored as a signed 32-bit data in binary code.

(2) Count multiplication may be done (see Section 4).

When a 2-phase pulse is input, the count can be multiplied by either one, two, or four.

(3) The maximum counting speed can be selected between 50 and 10K pulse/s (see Sections 2.2 and 8.4.2).

When the maximum counting speed is set to 50K pulse/s, a pulse at a maximum of 50K pulse/s can be counted in both the 1-phase and 2-phase inputs. When the maximum counting speed is set to 10K pulse/s, a pulse at a maximum of 10K pulse/s in the 1-phase input or at a maximum of 7K pulse/s in the 2-phase input can be counted.

(4) The ring counter function can be used (see Section 3.3).

By setting the ring counter switch, the coincidence signal is output when the counter value reaches the set value. Since the preset value is automatically and simultaneously preset, counting can be repeated.

(5) The limit switch output can be used (see Section 3.4).

By setting the output status of a certain channel, an ON/OFF signal may be output instead of the present value of the counter.

(a) A single module outputs to eight channels.

(b) Four dogs can be used for each channel.

(6) One out of the four counter functions can be selected (see Section 3.5)

Whichever function is desired from the following functions may be used:

(a) Latch counter function

(b) Sampling counter function

(c) Periodic-pulse counter function

(d) Count disable function

(7) A function can be selected between the preset and the counter using the external input (see Sections 3.2.2 and 3.5).

By applying voltage to the PRESET (preset) /F.START (function start) external terminal, either the preset or the counter function can be used.

(8) The AD62C can be installed on a DIN rail (see Section 8.5).

The AD62C can be installed on a DIN rail by using a dedicated adapter.

(9) Max. of 14 AD62Cs can be connected.

Max. of 14 AD62Cs can be set by using twisted pair cable at intervals of 100 meters or less.

# 2. SPECIFICATIONS

## 2.1 General Specifications

Table 2.1 gives the general specifications of the AD62C.

**Table 2.1 General Specifications**

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55 °C</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">–20 to 75 °C</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90% RH, non-condensing</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to ** JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55 Hz</td><td>—</td><td>0.075 mm (0.003 in)</td><td rowspan="2">10 times *(1 octave/ minute)</td></tr>
<tr><td>55 to 150 Hz</td><td>9.8 m/s$^2$ (1 g)</td><td>—</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to **JIS C 0912 (98m/s$^2$ (10 g) x 3 times in 3 directions)</td></tr>
<tr><td>Noise durability</td><td colspan="5">By noise simulator 1500 Vpp noise voltage, 1 μs width and 25 to 60 Hz noise frequency.</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">1500 VAC for 1 minute across AC external terminals and ground<br>500 VAC for 1 minute across DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5 MΩ or larger by 500 VDC insulation resistance tester across AC external terminals and ground</td></tr>
<tr><td>Grounding</td><td colspan="5">Class 3 grounding; grounding is not required when it is no possible.</td></tr>
<tr><td>Operating ambient</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

**REMARK**

One octave marked * indicates a change from the initial frequency to double or half frequency.

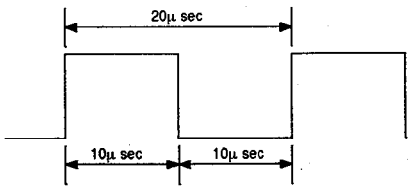
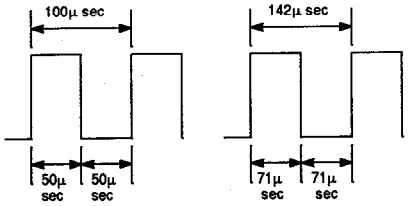
For example, any of the changes from 10 to 20 Hz, from 20 to 40 Hz, from 40 to 20 Hz, and 20 to 10 Hz are referred to as one octave.

Note: ** JIS : Japanese Industrial Standard

## 2.2 Performance Specifications

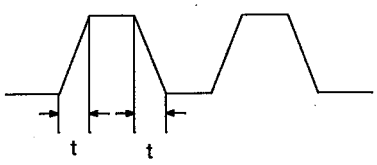
Table 2.2 gives the performance specifications of the AD62C.

**Table 2.2 Performance Specifications**

| Item | | Specifications | | |
|---|---|---|---|---|
| Counting speed switching | | 50K pulse/s | | 10K pulse/s |
| Number of I/O occupied points | | 4 stations (32 points) | | |
| Number of channels | | One | | |
| Count input signal | Phase | 1-phase and 2-phase inputs | | |
| | Signal levels (øA and øB) | 5 VDC<br>12 VDC<br>24 VDC ) 2 to 5 mA | | |
| Counter | Maximum counting speed* | 1-phase input | 50K pulse/s | 10K pulse/s |
| | | 2-phase input | 50K pulse/s | 7K pulse/s |
| | Counting range | 32-bit signed binary<br>–2147483648 to 2147483647 | | |
| | Type | Equipped with UP/DOWN preset counter and ring counter functions | | |
| | Minimum pulse width that can be counted(Adjust so that the leading edge/fall time of the input is 5μ sec or less. Duty ratio: 50 %) |  (1-phase and 2-phase inputs) | |  (1-phase input) (2-phase input) |
| Limit switch output | Comparison range | 32-bit signed binary | | |
| | Comparison result | N/O contact operation: dog ON address ≤ count value ≤ dog OFF address<br>N/C contact operation: dog OFF address ≤ count value ≤ dog ON address | | |
| External input | Preset | 12/24 VDC 3/6mA<br>5 VDC 5 mA | | |
| | Function start | | | |
| External output | Comparison output | Transistor (open collector) output<br>12/24 VDC 0.1 A/point 0.8 A/common | | |
| Power consumption | | 24 VDC 0.15 A | | |
| Weight (kg) (lb) | | 0.86 (1.91) | | |

* The counting speed is influenced by the pulse leading edge/fall time. The following counting speeds are possible. If a pulse is counted with a leading edge/fall time that is too long, a counter error may be caused.

| Leading Edge/fall Time | Counting Speed Switching | | | |
|---|---|---|---|---|
| | 50K | | 10K | |
| | 1-phase Input | 2-phase Input | 1-phase Input | 2-phase Input |
| t=5μ sec or less | 50K pulse/s | 50K pulse/s | 10K pulse/s | 7K pulse/s |
| t=50μ sec or less | 5K pulse/s | 5K pulse/s | 1K pulse/s | 700 pulse/s |
| t=500 μ sec | — | — | 500 pulse/s | 250 pulse/s |



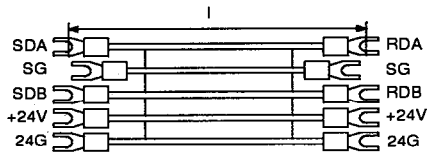
## 2.3 Cable Specifications

The following cables can be used with an AD62C.

(1) 5-core flat cable cut wires

These cables, used when an AD62C is installed adjacently to an A2CCPU or A2CCPU I/O unit, can transmit data while supplying 24 VDC. Cable specifications are given below.

**Table 2.3 5-Core Flat Cable Specifications**

| Model | A2C-C005 | A2C-C007 |
|---|---|---|
| Module intervals | 0 to 34 mm | 0 to 54 mm |
| Allowable current | 2 A | 2 A |
| Conductor resistance | 0.2 Ω | 0.2 Ω |
| Insulation resistance (20°C) | 15 MΩkm or larger | 15 MΩkm or larger |
| Dielectric withstand voltage V-min | 200 VAC | 200 VAC |
| Cable length l | 95 mm | 115 mm |
| Configuration |  | |



(2) Twisted pair cable

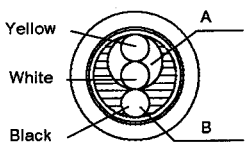
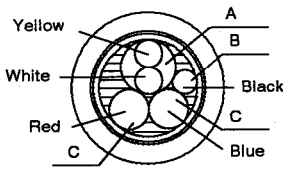
**Table 2.4 Twisted Pair Cable Specifications**

| Items | Specifications |
|---|---|
| Cable type | Shielded twisted pair cable |
| Logarithm | 2P or larger |
| Conductor resistance (20°C) | 88.0 Ω/km or less |
| Electrostatic capacity (1 kHz) | Average 60 nF/km or less |
| Characteristic impedance (100 kHz) | 110 ± 10 Ω |

(3) Shielded PVC cables

There are 2 types of cables - a 3-core cable for data send signals and a 5-core cable for data send signals and for supplying 24 VDC. Cable specifications are given below.

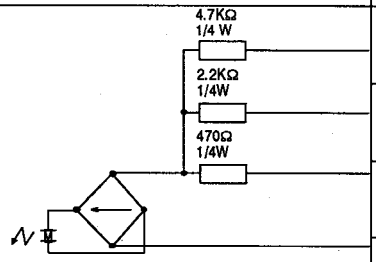
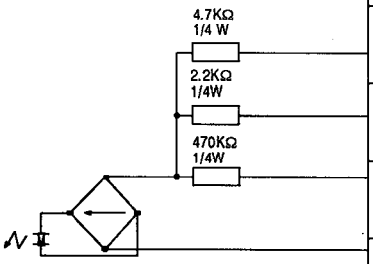
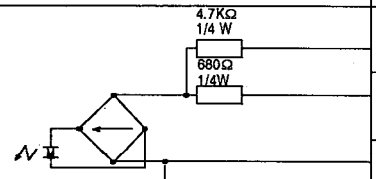
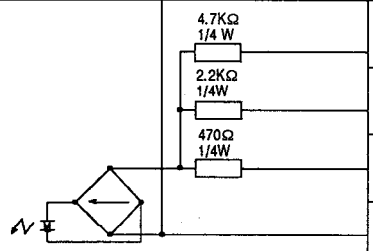
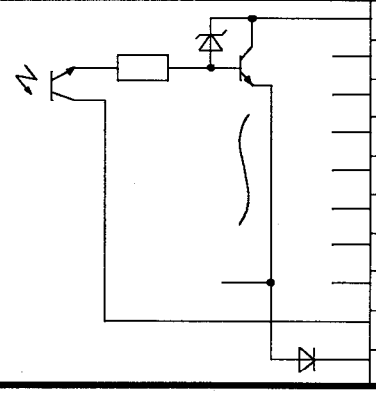
**Table 2.5 Shielded PVC Cable Specifications**

| Model | MI x 3 CHRV-SV-SB | MI x 5CHRV-SV-SB |
|---|---|---|
| Cable type | Shielded twisted-wire-pair cable | |
| Number of cores | Three-core composite | Five-core-composite |
| Application | A: SDA, SDB/B: SG/C: 24 VDC | |
| Module intervals | 100 m (3937 in.) maximum | |
| Conductor resistance (20°C) | A, B: 38 Ω/km or less<br>C: 10 Ω/km or less | |
| Insulation resistance (20°C) | 10 M Ωkm or larger | |
| Dielectric withstand voltage V-min | 200 VAC | |
| Cross sections |  |  |

## 2.4 External Devices Interfaces

Table 2.6 lists the external device interfaces.

**Table 2.6 External Device Interfaces**

| Input/ Output | Internal Circuits | Terminal | Signal Names | Operating Status | Input Voltage (Guaranteed Value) | Operating Current |
|---|---|---|---|---|---|---|
| Input |  | 24V | Phase A pulse input 24V | ON | 21.6 to 26.4 V | 2 to 5 mA |
| | | | | OFF | 5 V or lower | 0.1 mA or lower |
| | | 12V | Phase A pulse input 12V | ON | 10.8 to 13.2 V | 2 to 5 mA |
| | | | | OFF | 4V or lower | 0.1 mA or lower |
| | | 5V | Phase A pulse input 5V | ON | 4.5 to 5.5V | 2 to 5mA |
| | | | | OFF | 2V or lower | 0.1mA or lower |
| | | COM | COM | | | |
| |  | 24V | Phase B pulse input 24V | ON | 21.6 to 26.4 V | 2 to 5 mA |
| | | | | OFF | 5 V or lower | 0.1mA |
| | | 12V | Phase B pulse input 12 V | ON | 10.8 to 13.2 V | 2 to 5 mA |
| | | | | OFF | 4V or lower | 0.1mA or lower |
| | | 5V | Phase B pulse input 5 V | ON | 4.5 to 5.5 V | 2 to 5 mA |
| | | | | OFF | 2 V or lower | 0.1 mA or lower |
| | | COM | COM | | | |
| Input |  | 12/24V | Preset input 12 V/24 V | ON | 10.2 to 26.4 V | 2 to 6 mA |
| | | | | OFF | 2 V or lower | 0.1mA or lower |
| | | 5V | Preset input 5V | ON | 4.5 to 5.5 V | 3.5 to 5.5 mA |
| | | | | OFF | 1.5V or lower | 0.1mA or lower |
| | | COM | COM | Response time | OFF → ON 1 msec or less | ON → OFF 3.5 msec or less |
| Input |  | 24V | Function start input 24 V | ON | 21.6 to 26.4 V | 2 to 5 mA |
| | | | | OFF | 5 V or lower | 0.1 mA or lower |
| | | 12V | Function start input 12V | ON | 10.8 to 13.2 V | 2 to 5 mA |
| | | | | OFF | 4 V or lower | 0.1 mA or lower |
| | | 5V | Function start input 5V | ON | 4.5 to 5.5 V | 2 to 5 mA |
| | | | | OFF | 2 V or lower | 0.1 mA or lower |
| | | COM | COM | Response time | OFF → ON 1 msec or less | ON → OFF 1 msec or less |
| Output |  | 1 | OUT 1 | Operating voltage: 10.2 to 30 V<br>Rated current: 0.5 A<br>Rated voltage: 0.1 A/point 0.8 A/common<br>Maximum rush current: 0.6 A 10 msec<br>Maximum voltage drop at ON: 0.7 V(TYP) 1.3 V(MAX)<br>Response time OFF → ON: 1 msec (MAX) 0.3 msec (MIN)<br>ON → OFF 1 msec (MAX) 0.3 msec (MIN) | | |
| | | 2 | OUT 2 | | | |
| | | 3 | OUT 3 | | | |
| | | 4 | OUT 4 | | | |
| | | 5 | OUT 5 | | | |
| | | 6 | OUT 6 | | | |
| | | 7 | OUT 7 | | | |
| | | 8 | OUT 8 | | | |
| | | 12/24V | 12/24V | Input voltage: 10.2 to 30 V<br>Current consumption: 8 mA (TYP 24 VDC) | | |
| | | COM | 0V | | | |

## 2.5 Applicable Encoders

The encoders applicable to the AD62C are shown below:

(1) Open-collector type

(2) CMOS output type

(Make sure that the output voltage of the encoder complies with the AD62C specifications.)

**POINT**

The following types of encoders cannot be used with the AD62C:

- TTL output type
- Line drive output type

# 3. FUNCTIONS

## 3.1 Functions List

Table 3.1 gives the functions of the AD62C.

**Table 3.1 Function Specifications**

| Function | | Description | Reference Section |
|---|---|---|---|
| Preset | | • Changes the present value of the counter.<br>• The preset operation can be done either by a sequence program or by an external preset input. | 3.2 |
| Ring counter | | • Counting alternates between the preset value and the ring counter value. | 3.3 |
| Limit switch output | | • Outputs an ON/OFF signal in a specified output status, comparing it with the present value of the limit switch output command counter. | 3.4 |
| Counter function selection | Latch counter | • Stores the present value of the counter when the signal of the counter function selection start command is input. | 3.5.3 |
| | Sampling counter function | • After inputting the signal of the counter function selection start command, the input pulse is counted during a specified period and stored in the buffer memory. | 3.5.4 |
| | Periodic pulse counter | • While inputting the signal of the counter function selection start command, the input pulses are stored in the buffer memory at specified intervals. | 3.5.5 |
| | Count disable | • Stops counting pulses while the count enable command is ON. | 3.5.6 |

* Counter function selection means that only one out of the four functions can be used.

## 3.2 Preset Function

The preset function is used for converting the counter's present value to a different value.

This changed value is called the preset value.

The preset function can be used when a pulse count is started from the set value.

The preset function consists of two modes: preset by the sequence program and preset from the external input (applying the voltage to the external terminal).

Preset function application example:

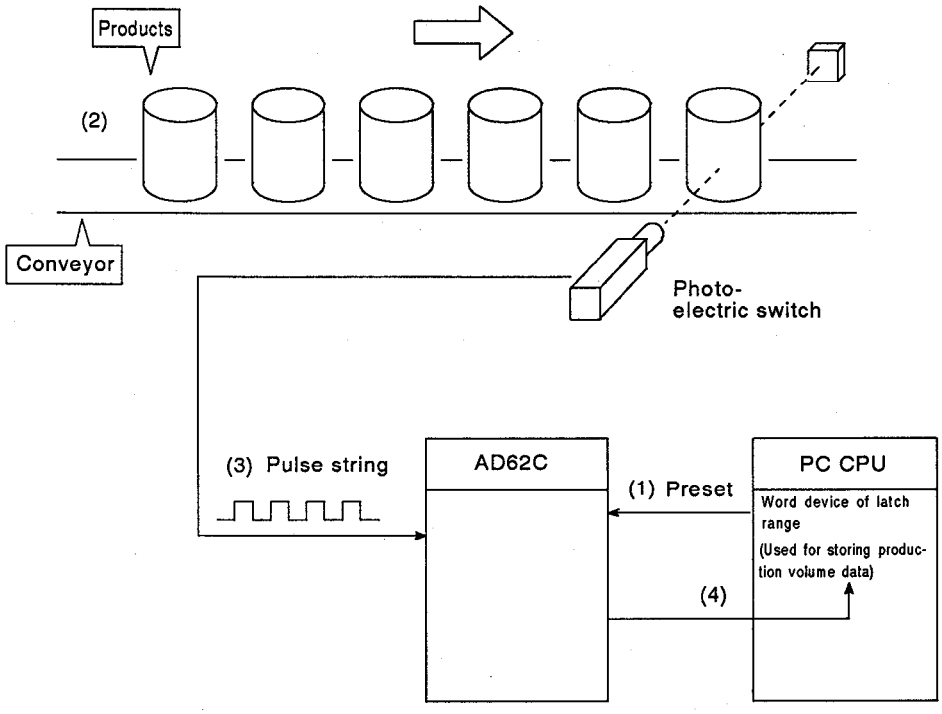
By using the preset function, the production count can be continued from the previous day.

(1) The production volume of the previous day is "preset" from the PC CPU to the AD62C.

(2) Products are carried by a conveyor.

(3) The production volume is counted by inputting the pulse from the photo-electric switch.

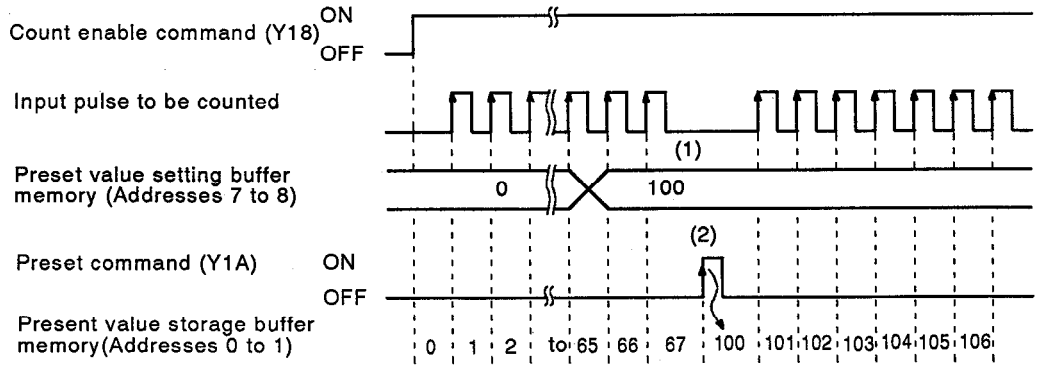
(4) At the end of the daily production, the counter value in the buffer memory is stored to a word device (D, W, etc.) in the PC CPU latch range.



### 3.2.1 Preset using the sequence program

The following describes the preset function executed by the sequence program.

Turn ON the preset command (Y1A) in the sequence program to execute the preset.



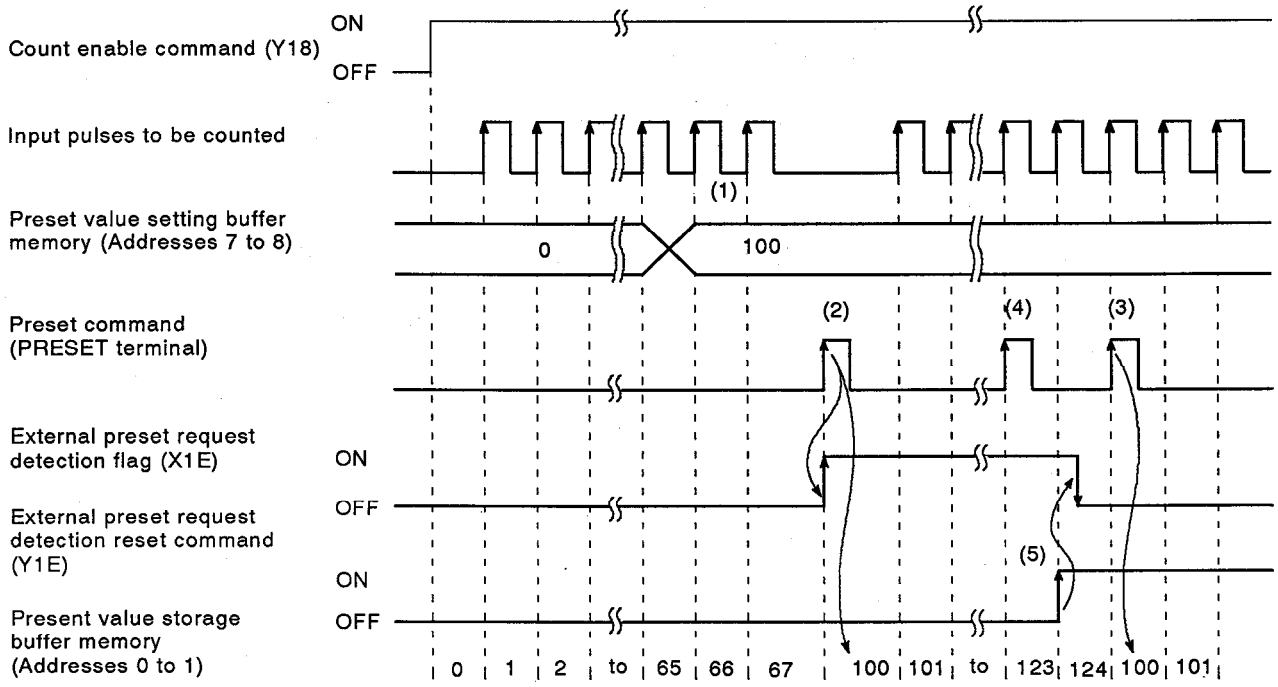

1) Writes a given value to the preset value setting buffer memory (addresses 7 to 8) in 32-bit binary code.
2) Turing ON the preset command (Y1A) sets the preset value in the buffer memory to the present value buffer memory.

   The preset function can be used whether the count enable command (Y18) is ON or OFF.

### 3.2.2 Preset by external input

The following describes the preset by the external input.

Execute the preset by applying the voltage to the external input PRESET terminal.




1) Writes a given value to the preset value of the setting buffer memory (addresses 7 to 8) in 32-bit binary code.
2) Executing the preset command (applying the voltage to the PRESET terminal) sets the preset value in the buffer memory to the present value buffer memory.
3) Even when the external preset command detection reset command (Y1E) is ON, the preset can be executed with the preset command (applying the voltage to the PRESET terminal).

   The preset function can be used whether the count enable command (Y18) is ON or OFF.

**POINT**

When the external preset request detection flag (X1E) is ON (see (4) in the above-indicated diagram), even if the voltage is applied to the PRESET terminal, the preset function cannot be executed.

In this case, by turning ON the external preset command detection reset command (Y1E) and turning OFF the external preset request detection flag (X1E), the preset function can be executed.

### 3.3 Ring Counter Function

This section describes the ring counter function.

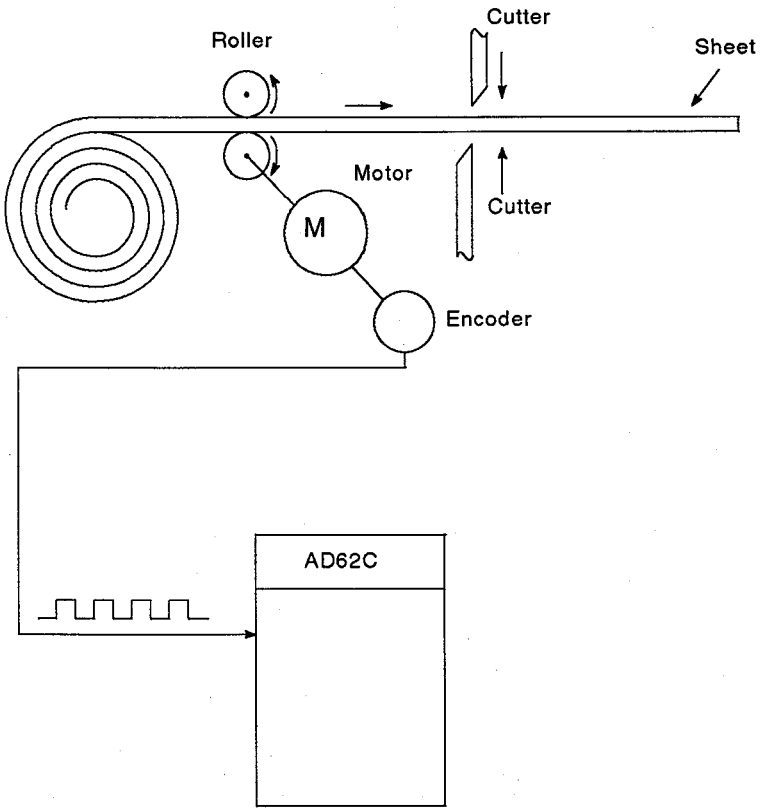
The ring counter function automatically sets the present value to the value that has been preset and executes counting operations.

The ring counter function can be used when executing controlled cycles such as incremental feed.

Ring counter function application example:

Using a system to cut a sheet to a specified size, adjust its rollers by setting the ring counter value, and cut the sheet to the specified size.

1) Set the preset and ring counter values to execute the ring counter function.
2) Turn on the motor to operate the rollers.
3) Operate the rollers so that the sheet can be cut to the specified size.
4) Cut the sheet.
5) Repeat steps 2 to 4.



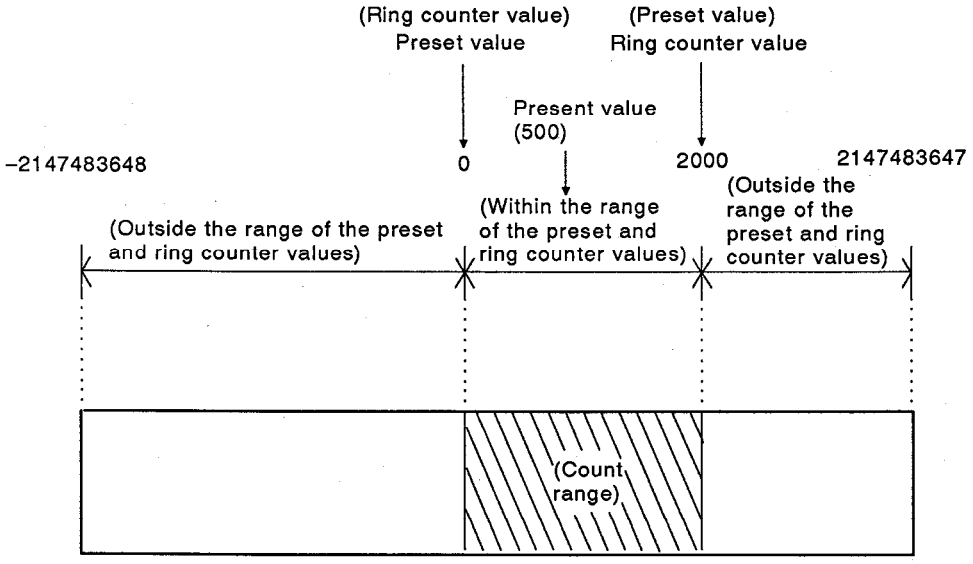
(1) The ring counter function is executed when both the count enable command (Y18) and the ring counter commands (Y1B) are ON.

(2) Ring counter operation

When the counter value is between the preset value and the ring counter value, the ring counter functions within the range between the preset value and the ring counter value.

When the ring counter function is executed, if the counter present value reaches the ring counter value, the present value will be automatically set to the preset value.

Also, if the present value of the counter reaches the preset value, the preset value will remain the same.




(a) When the preset value of the storage buffer memory (addresses 7 to 8) is set to 0, the ring counter value of the storage buffer memory (addresses 9 to 10) to 2000, and the present value of the storage buffer memory (addresses 0 to 1) to 500 respectively, the ring counter is executed as shown below:

1) Increment count:

If the ring counter value reaches the ring counter set value (2000), the present value storage buffer memory (addresses 0 to 1) will be set to the preset value (0).

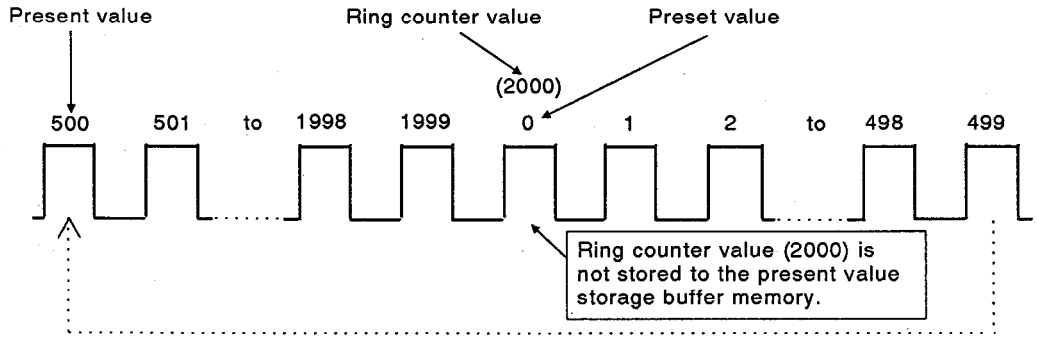
The ring counter value (2000) is stored to the present value storage buffer memory.

2) Decrement count:

If the ring counter value reaches the preset value (0), the preset value will remain.

When the next count is made, the preset value (ring counter value - 1) is stored to the present value of the storage buffer memory.

The ring counter value (2000) is not stored to the present value of the storage buffer memory.




(b) When the preset value of the storage buffer memory (addresses 7 to 8) is set to 2000, the ring counter value of the storage buffer memory (addresses 9 to 10) to 0, and the present value of the storage buffer memory (addresses 0 to 1) to 500 respectively, the ring counter is executed as shown below:

1) Increment count:

If the ring counter value reaches the preset value (2000), the preset value will remain.

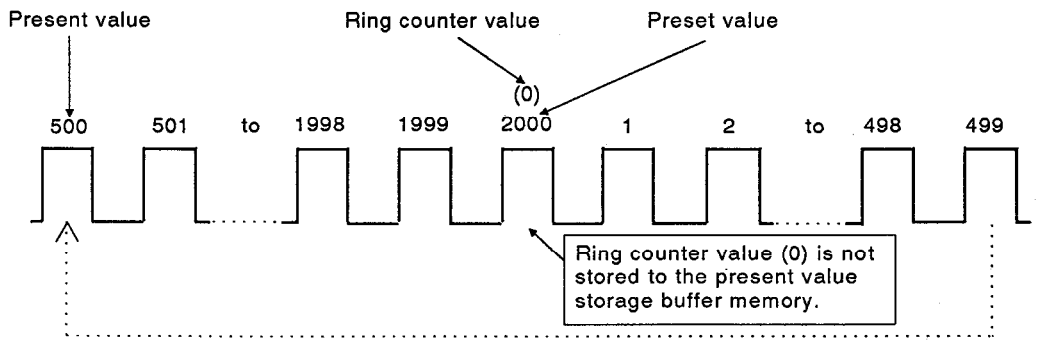
When the next count is made, the preset value (ring counter value + 1) is stored to the present value of the storage buffer memory.

The ring counter value (0) is not stored to the present value of the storage buffer memory.

2) Decrement count:

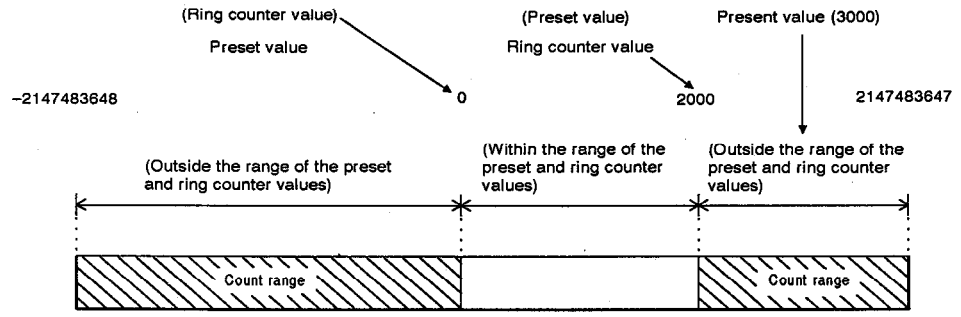
If the ring counter value reaches the preset value (0), the preset value (2000) is stored to the present value of the storage buffer memory.

The ring counter value (0) is not stored to the present value of the storage buffer memory.

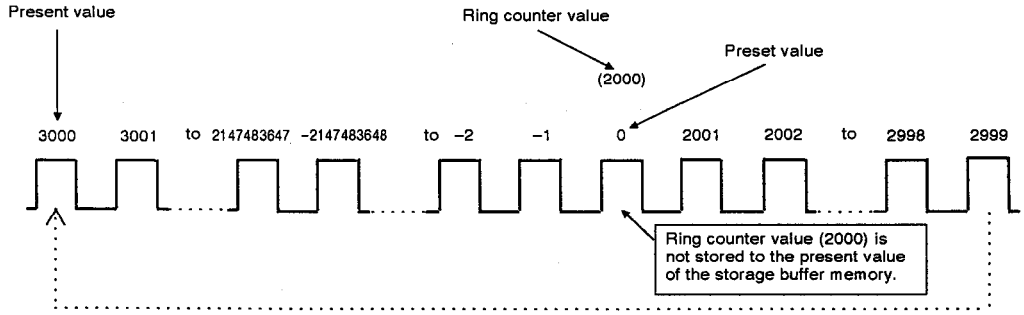


**REMARK**

If the ring counter starts when the present value is outside the range of the preset and ring counter values (except when the present value is equal to the preset and ring counter values), the count cannot be made within the range of the preset and ring counter values.




When the preset value storage buffer memory (addresses 7 to 8) is set to 0, the ring counter value storage buffer memory (addresses 9 to 10) to 2000, and the present value storage buffer memory (addresses 0 to 1) to 3000 respectively, the ring counter is executed as shown below:




**POINT**

When the present value of the counter is outside the range of the preset and ring counter values, the present value of the counter can be changed to the preset value by using the preset command (Y1A).

**POINTS**

(1) When the ring counter function is executed, do not write the preset value or ring counter value.

If the write is executed, an error will occur and the error code (114) will be stored as a data error of the storage buffer memory (address 12).

(2) When the ring counter function is executed, make sure that the difference between the preset and the ring counter values is larger than the number of input pulses per msec.

| (Preset value) — (Ring counter value) | ≥ Number of pulses/msec

Example: When the pulse input speed is more than 50K pulse/s:

When the pulse is input at a speed of 50K pulse/s, make sure that the difference between the preset and the ring counter values is larger than 50 (pulses/msec).

## 3.4 Limit Switch Output Function

This section describes the limit switch output function.

The limit switch output function is used in the following cases:

When the counter present value is consistent with a specified limit output status (ON/OFF address) of a certain channel, the ON/OFF signal is output.

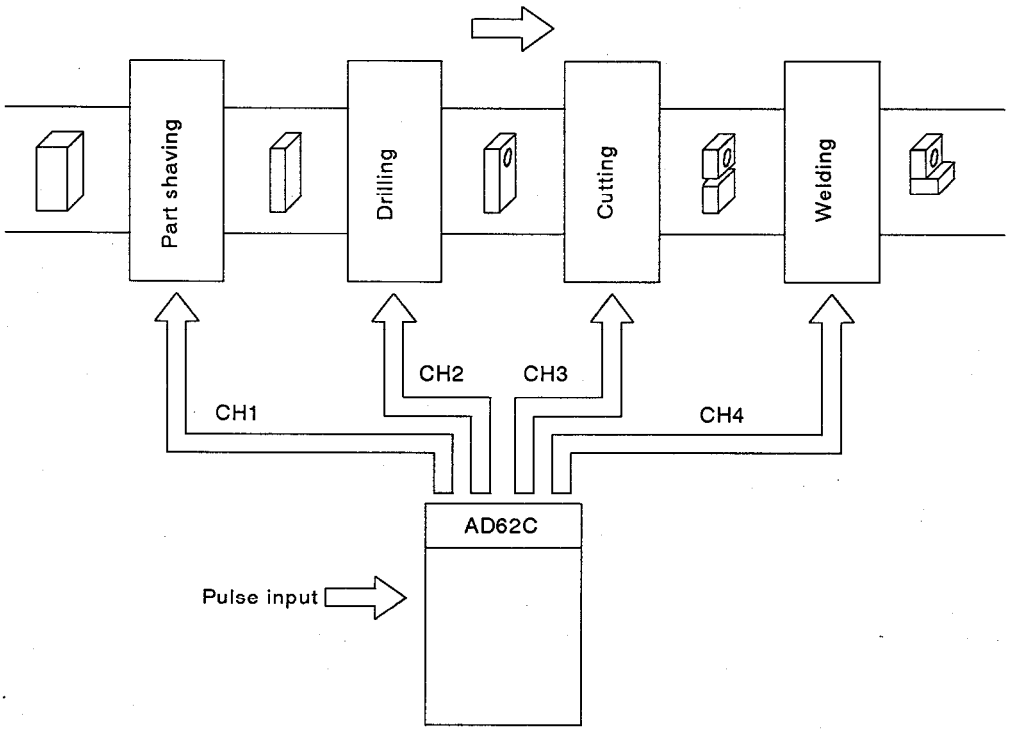
When the limit switch output enable signal is not set, turning ON the limit switch output enable command (Y1D) does not activate the limit switch output function.

Instead of the conventional limit switch, the limit switch output can be also applied to a series of the operations on the processing line.

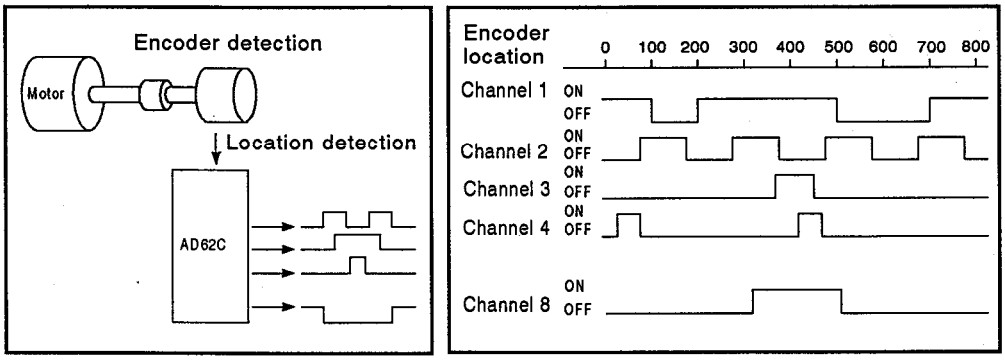
**[ Limit switch output function application example ]**

By using a processing line system, products are made through the processing operations corresponding to each channel.

1) Carries material with the belt conveyor.
2) The location of material is known through the counter present value since the pulses are input to the AD62C.
3) The material is processed according to the limit switch output (CH1 to CH4).

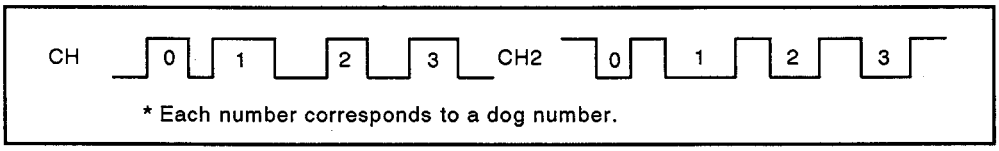


(1) In limit switch output, up to 8 channels can be used.

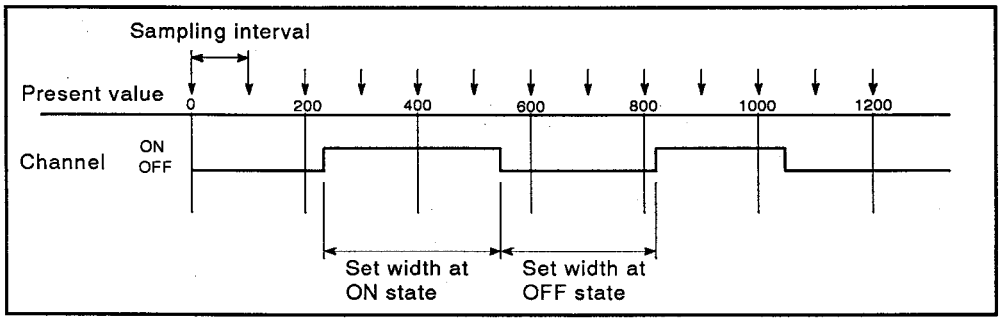



(2) There are four dogs per channel.

In this manual, the dog refers to the concave of convex parts as shown below:




(3) The speed of the pulse input will determine the minimum setting width at ON/OFF states.




In the AD62C, the location data is sampled at an interval of 1.0 msec. The limit switch signal is compared with the set ON/OFF data and is then output.

Therefore, if the pulse input speed exceeds the allowable speed, the location cannot be detected in units of minimum length and the ON/OFF signal cannot be executed according to the specification.

In this case, enlarge the set width of the ON or OFF signal.

Find the allowable speed using the following formula:

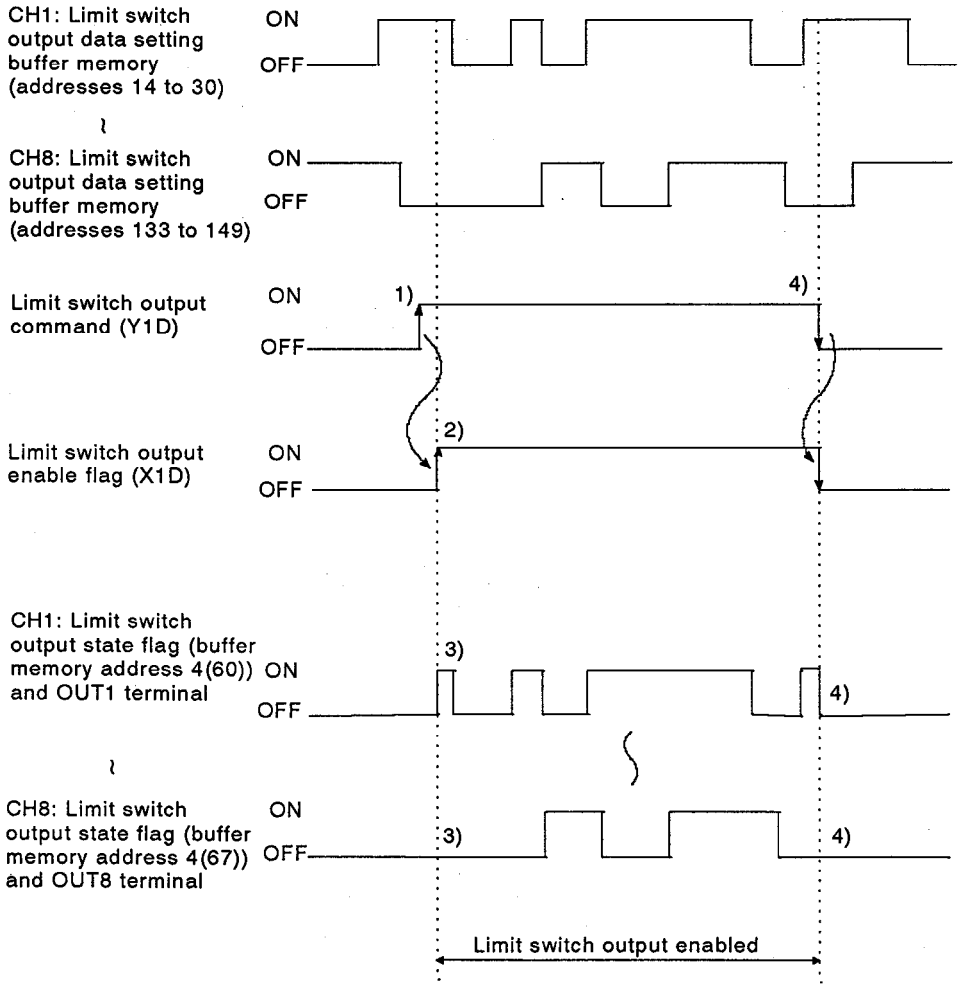
(a) Set width at ON state:

$$\frac{\text{Pulse input speed [pulse/s]}}{1000} \times \text{(Multiplication number)} \leqq \text{(Count present value at OFF)} - \text{(Count present value at ON)}$$

(b) Set width to the OFF state:

$$\frac{\text{Pulse input speed [pulse/s]}}{1000} \times \text{(Multiplication number)} \leqq \text{(Count present value at ON)} - \text{(Count present value at OFF)}$$

(4) The timing of each signal when the limit switch output function is executed:




1) Turning ON the limit switch output command (Y1D) verifies whether or not the set limit switch output data contains an error.

   When no error is detected, the limit switch output enable flag (X1D) will be set.

2) Setting the limit switch output enable flag (X1D) executes the limit switch output function.

3) The present value of the counter is compared with the set limit switch output data. The data is then output to the limit switch output state flags (Address 4 (60 to 67)) and the OUT terminals (OUTs 1 to 8).

4) Turing OFF the limit switch output command (Y1D) resets the limit switch output enable flag (X1D), the limit switch output state flags (Address 4 (60 to 67)), and the OUT terminals (OUTs 1 to 8).

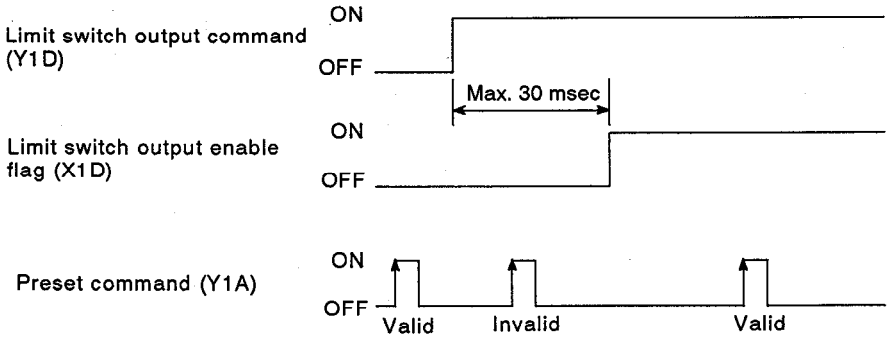
**POINTS**

(1) The limit switch output is executed whether the count enable command (Y18) is ON or OFF.

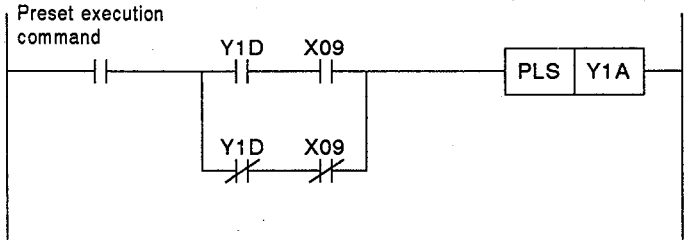
(2) In the limit switch output, the preset, latch counter, and sampling counter execution commands are ignored until the limit switch output command (Y1D) is turned ON to set the limit switch enable flag (X1D).

However, the execution of the external input is valid.

For example: When the preset function is executed:




Refer to a program as show below:



(5) Limit switch output data (CH1 to CH8) setting buffer memory (addresses 14 to 149)

This is an area in which ON/OFF data for each channel in the limit switch output function is stored.

(a) The data set consists of the number of multiple-dogs and ON/OFF position data of each dog for each channel.

(b) The data set for the multiple-dogs and ON/OFF position data is written in binary code.

If the number of the multiple-dogs is set beyond the detection range or some dogs overlap, an error occurs.

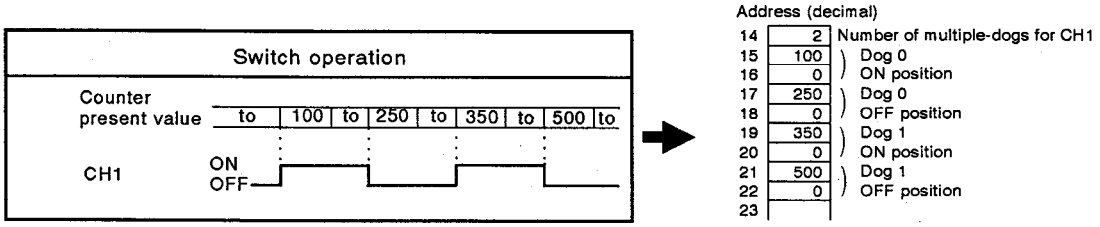
The dog position write operation is divided into two modes: the dog position write in the ON range and the dog position write in the OFF range.

The AD62C automatically verifies if the dog data write is done in ON or OFF range by checking the contents of dog 0.

1) ON range (limit switch NO contact operation) dog position write

In this case, the ON position data is written along with a value less than the OFF position data.

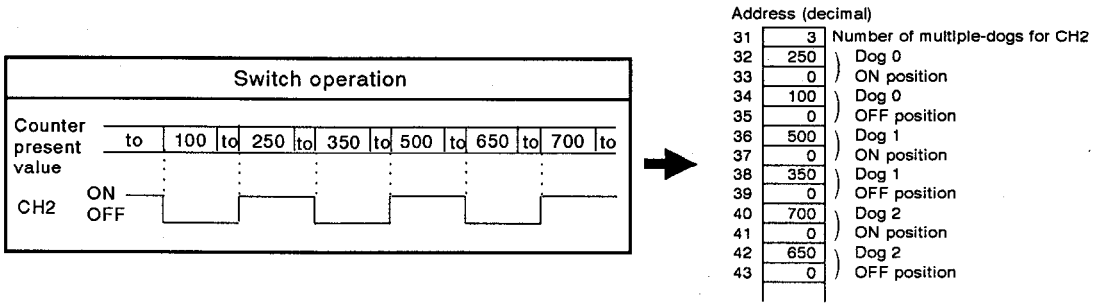
If the dogs are not written in ascending order, an error occurs.




2) OFF range (limit switch NC contact operation) dog position write

In this case, the ON position data is written along with a value larger than the OFF position data.

If the dogs are not written in ascending order, an error occurs.



3) The number of multiple dogs can be set in the following range: 0 to 4 (The lower 4 bits of the data set are valid.)

However, if this number is set to 0, the corresponding dog ON/OFF position data becomes invalid.

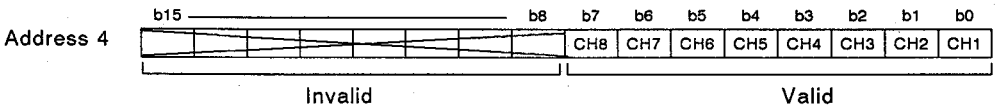
Also, if a value larger than 4 is set, an error occurs which disables the limit switch output function.

(c) The following occurs when there is a multi-dog setting error:

1) The limit switch output READY flag (X1D) : OFF

2) The limit switch output states
(address 4 (b0 to b7), and OUT 1 to OUT 8) : All channels are OFF

(6) CH 1 to CH 8 limit switch output state flags (buffer memory address 4)




(a) The output state of address 4 is represented by a bit string.

(b) The output states of each channel (CH 1 to CH 8) are stored to the corresponding bits as shown above.

**POINTS**

(1) When limit switch output data is set or changed, make sure that the following conditions have been satisfied:

(a) The limit switch output enable command (Y1D) is OFF.

(b) The limit switch output READY flag (X1D) is OFF.

(2) If the multi-dog data setting contains an error (error codes: 210 to 283 and 301 to 308), switching the limit switch output enable command (Y1D) ON sets the limit switch output READY flag (X1D).
In this case, reset the error, and switch the limit switch output enable command (Y1D) ON again.

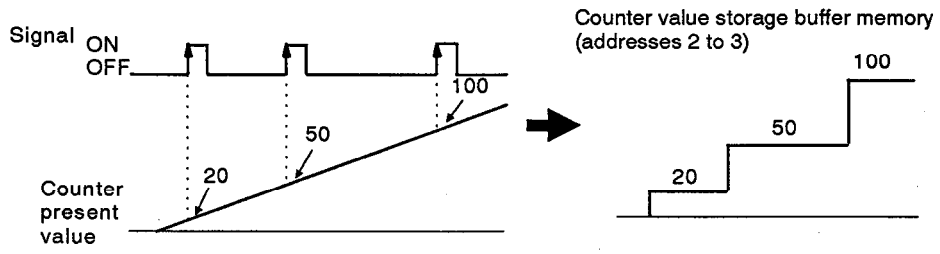
## 3.5 Selecting a Counter Function

This section describes the counter function.

Select one of the four counter functions and execute it.

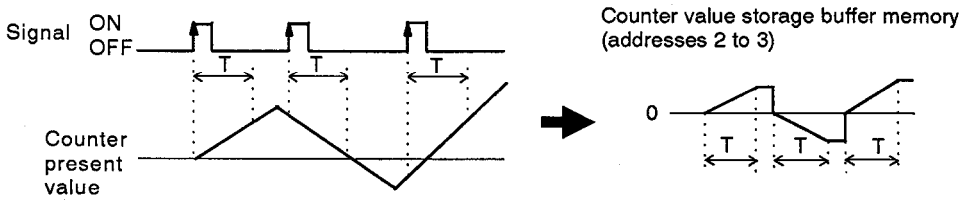
1) Latch counter function: see Section 3.5.3.

Latches the present value of the counter when the signal is input.



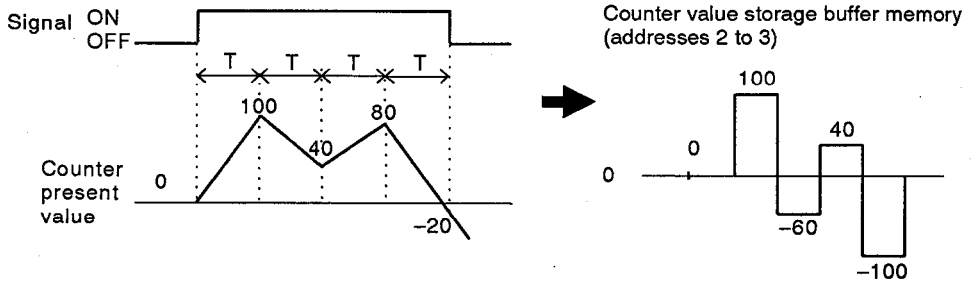

2) Sampling the counter function: see Section 3.5.4.

Counts the input pulse times that are specified by the signal.



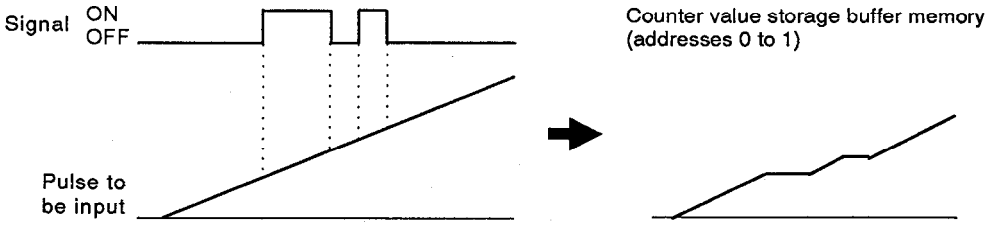

3) Periodic pulse counter function: see Section 3.5.5.

Stores the number of input pulses at specified intervals while a signal input is done.




4) Count disable function: see Section 3.5.6.

Inputs the signals when the count enable command is ON, stopping the pulse count.



(1) Counter function selection

Select a counter function by writing a value to the counter setting buffer memory (address 6) as shown in the following table:

However, when the counter function is changed, make sure that the counter start command (Y1C, F.START terminal) is OFF.

| Counter Function Selection | Setting Value |
|---|---|
| None | 0 |
| Latch counter function | 1 |
| Sampling counter function | 2 |
| Periodic pulse counter function | 3 |
| Count disable function | 4 |

(2) Executing counter function selection

Counter function selection can be executed by using either the counter start command (Y1C) or the F.START terminal (external input).

If both signals are input, priority is given to the first signal input.

(3) Precautions concerning the sampling counter function and the periodic pulse counter function time settings

The sampling counter function and periodic pulse counter function time settings must be within the range of 1 to 65535.

The unit of time is 10 (msec).

Example) If 420 is set to the sampling/periodic time setting buffer memory.
420 x 10 = 4200 (msec)

**IMPORTANT**

(1) Do not execute counter function selection using F.START (external input) immediately after a counter function selection setting value has been written to the buffer memory (address 6).

(2) Use the following operations to execute counter function selection using F.START (external input).

* When linking with an A2CCPU : Apply voltage to the F.START terminal after the device number (which switches ON when the instruction has been executed) of the PRC instruction that is added to the T instruction switches ON.

* When linking with an AJ71PT32-S3 (A1SJ71PT32-S3) : Apply voltage to the F.START terminal after the send-completed signal (X(n+[ ])) of the AJ71PT32-S3 (A1SJ71PT32-S3) switches ON.

### 3.5.1 Reading the counter value when executing the counter function selection

Read the counter value when the counter function is selected.

The following explains the counter contents stored in the AD62C counter value storage buffer memory (addresses 2 to 3) and how to read the counter value:

(1) In the counter storage buffer memory, the value of the latch counter, sampling counter, or periodic pulse counter is stored.

(2) The counter value (2147483648 to –2147483647) is stored in a signed 32-bit binary code.

When the counter value is negative, this value is stored as a complementary number of two.

(3) When an incremental count is made, if the counter value exceeds 2147483647, it will jump to –2147483648.

When a decremental count is made, if the counter value exceeds –2147483648, it will jump to 2147483647.

**POINT**

The programming for reading the counter value when the counter function is selected differs according to which link method is used.

Therefore, refer to the programming example for the corresponding link method.

### 3.5.2 Count errors

When the counter function selection is executed by the external input (applying the voltage to the F.START terminal) or by the sequence program (turning ON the counter function selection start command), there is an error in counting.

(1) The error range when the counter function is executed by the external input is shown below:

**Max. count error:**

1 [msec] x pulse input speed [pulse/s] x multiplication number [count]

**Min. count error:**

0.1 [msec] x pulse input speed [pulse/s] x multiplication number [count]

(2) When the counter function is executed by the sequence program, there is an additional error for one scan of the PC CPU besides the error as shown in (1).

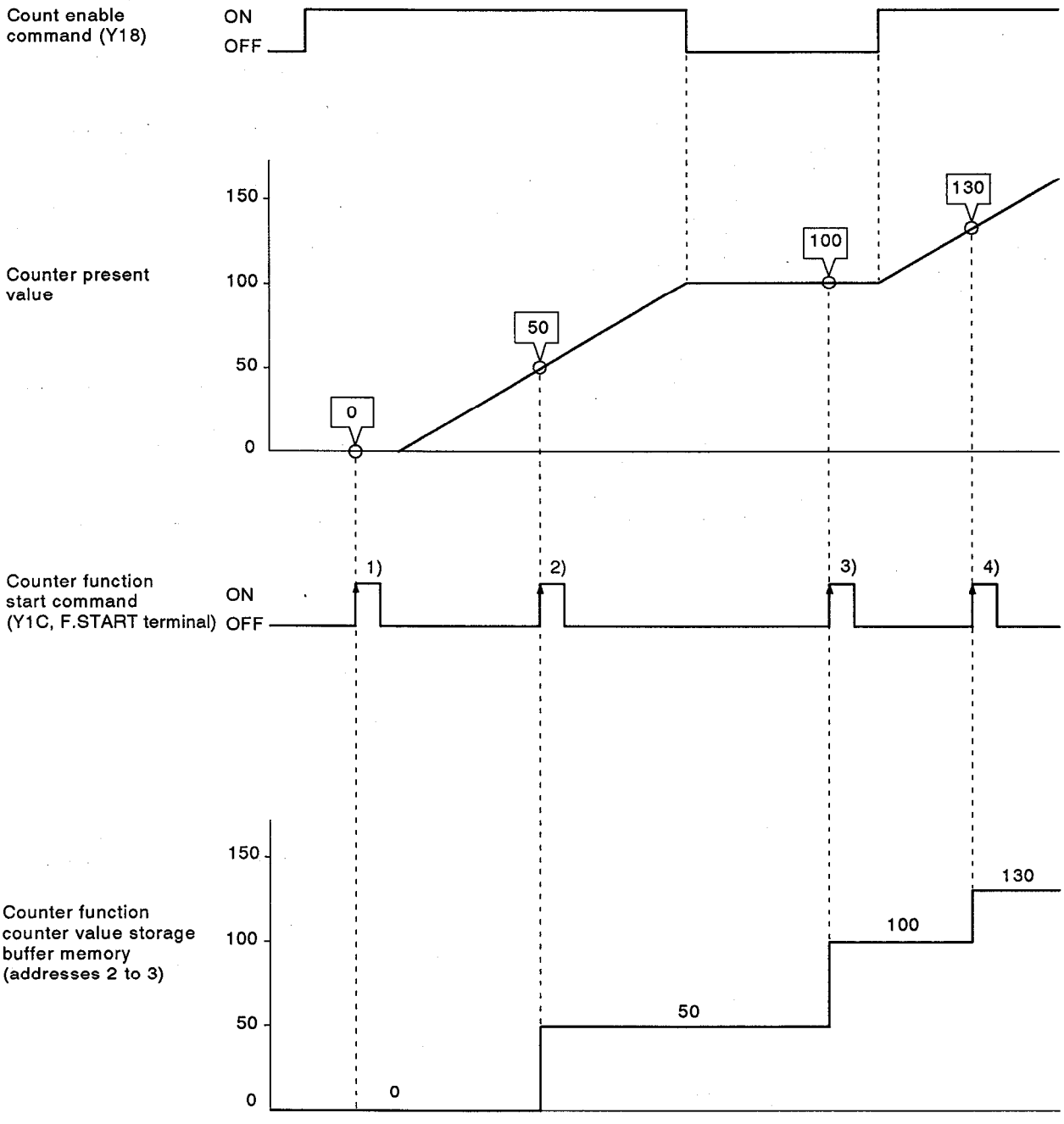
**POINT**

Mitsubishi recommends that the counter function selection should be executed by external input.

### 3.5.3 Latch counter function

Latch the present value of the counter when a signal input is done.

The relationships between the counter present value and the counter start command and between the present value and the counter buffer memory are shown below:

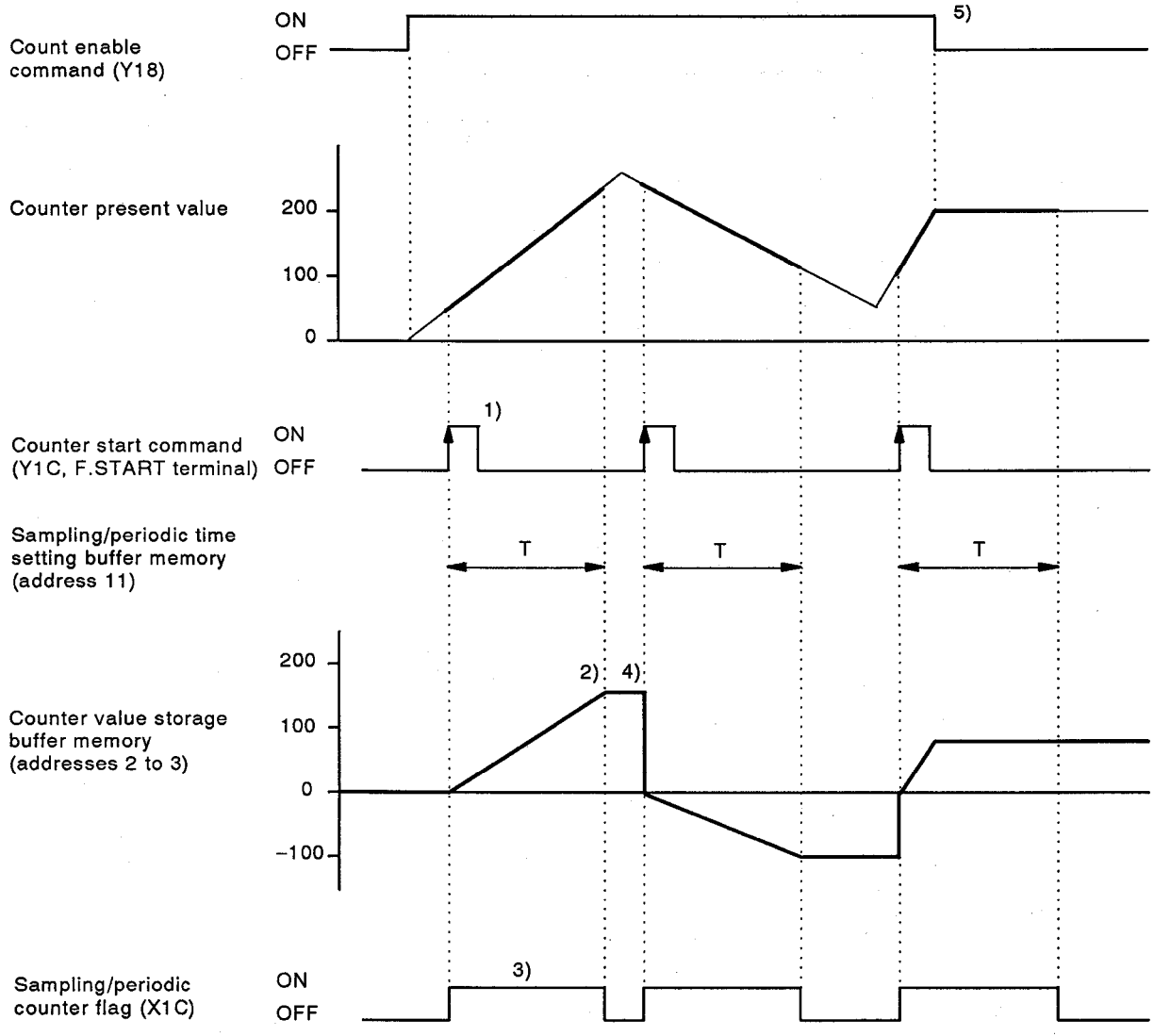



At the leading edge of the counter function start command (Y1C, F.START terminal)(corresponding to 1) to 4) in the above diagram), the counter present value is stored to the counter value buffer memory (addresses 2 to 3).

The latch counter function works whether the count enable command (Y18) is ON or OFF.

### 3.5.4 Sampling counter function

Count the pulses when a sampling time is specified.
Sampling time can be set in 10ms unit, and its accuracy is less than 1 count.
The relationship between each signal and the buffer memory is shown below:




1) Starts counting input pulses from 0 at the leading edge of the counter function command (Y1C, F.START terminal).

2) Stops counting after the specified sampling time.

3) Keeps the sampling/periodic counter flag (X1C) set while executing the sampling counter function.

4) Retains the value in the buffer memory after completing the sampling counter function.

5) The sampling counter function works whether the count enable command (Y18) is ON or OFF.

### 3.5.5 Periodic pulse counter function

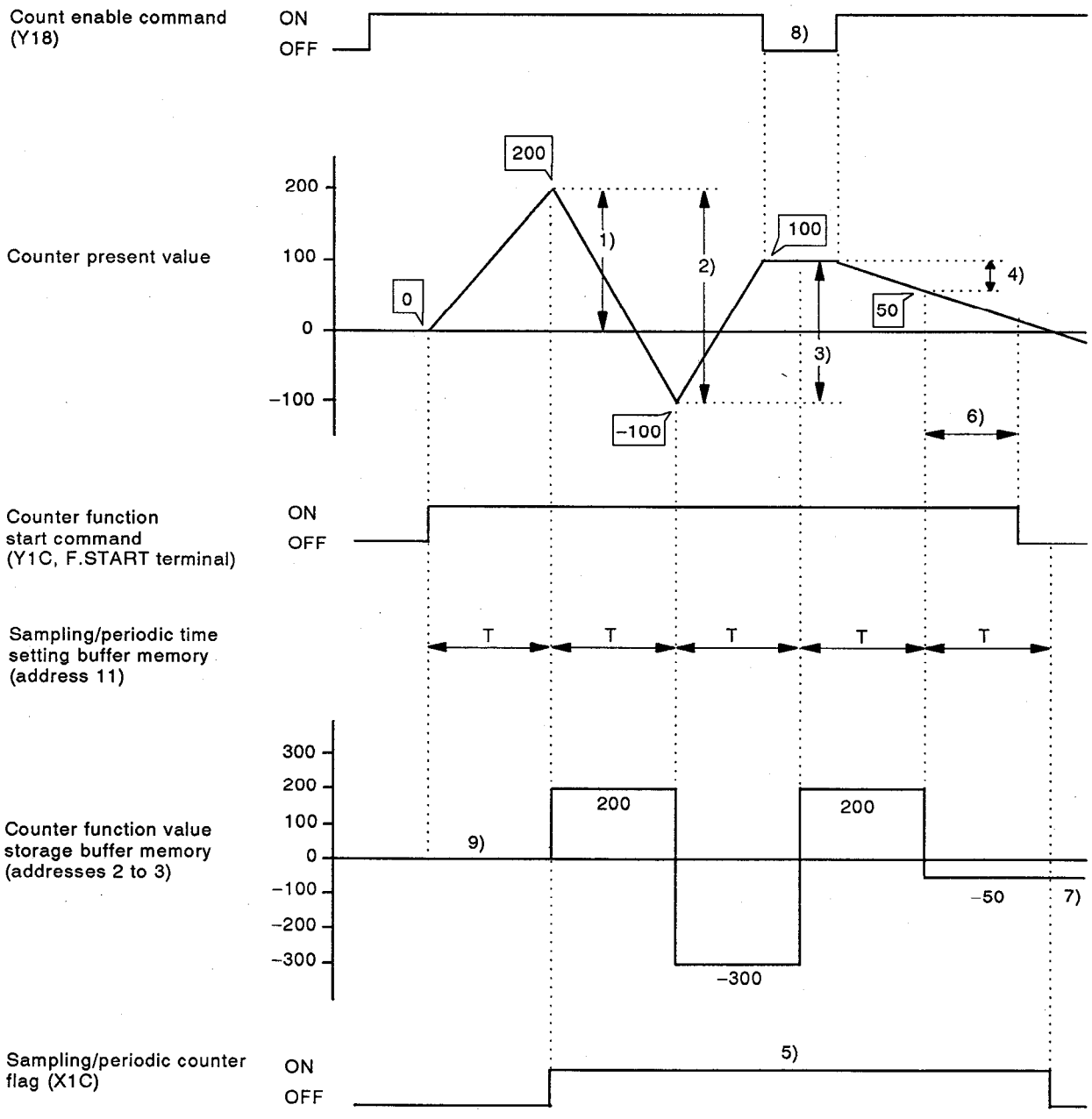
Count pulses that are input at specified intervals, and store the counter value to the counter value storage buffer memory.

Periodic time can be set in 10ms unit, and its accuracy is less than 1 count.

Find the value stored in the counter storage buffer memory using the following formula:

| Stored value = (Counter present value after the periodic time) - (Counter present value at the start) |
|---|

The relationship between the each signal and the buffer memory is shown below:



1) Stores the counter present value (200 – 0 = 200) to the counter function value storage buffer memory, after the periodic time (set in address 11).

   9) is set to the "0" state.

2) Stores the counter present value of –300 to the counter function value storage buffer memory.

3) Stores the counter present value of 200 to the counter function value storage buffer memory.

4) Stores the counter present value of –50 to the counter function value storage buffer memory.

5) Keeps the sampling/periodic counter flag (X1C) set while executing the periodic pulse counter.

6) Ignores the counter value of the periodic pulse, since the counter function start command (Y1C) is turned OFF.

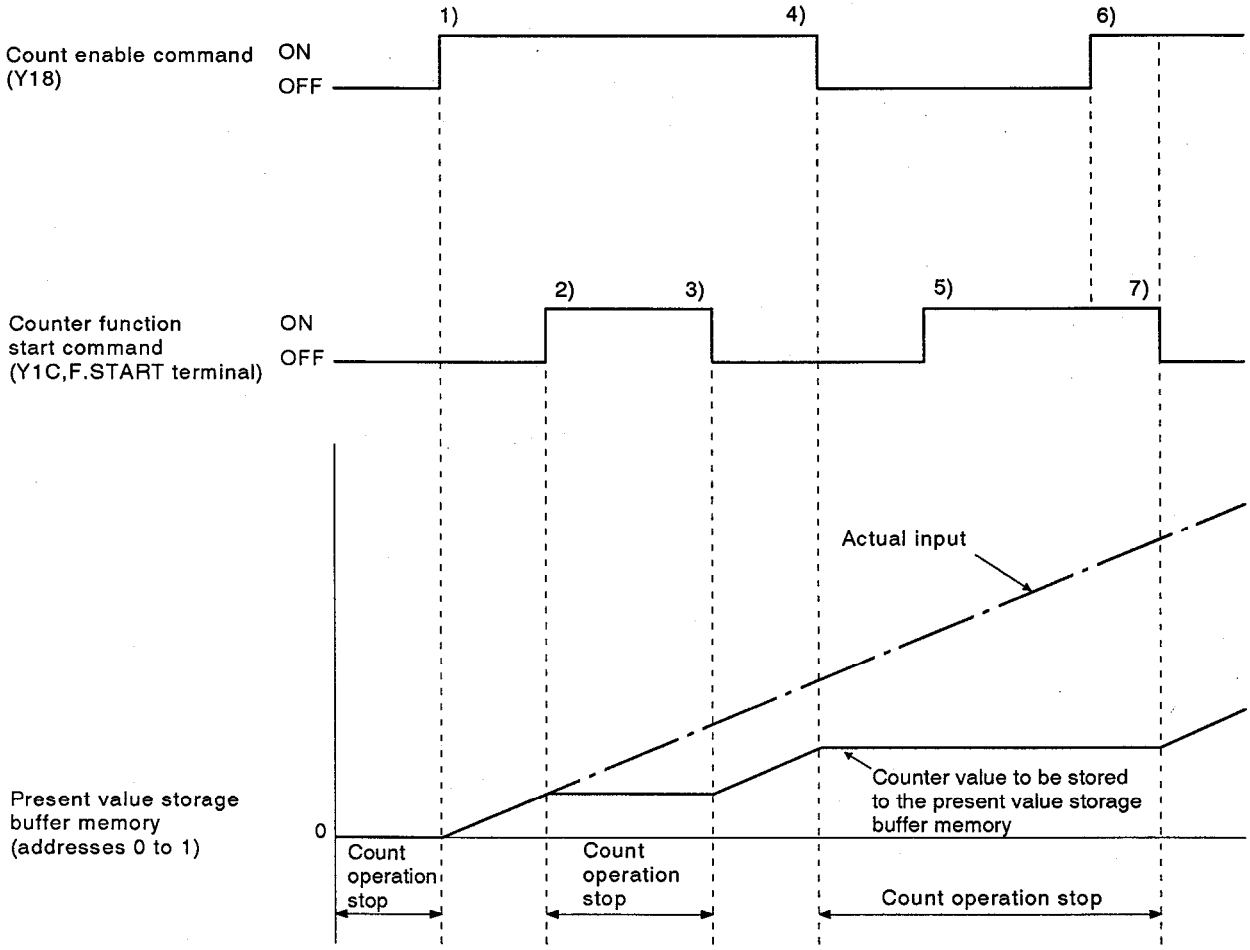
7) Retains the value of –50 [item 4)] after the periodic pulse counter is executed.

8) The periodic pulse counter function works whether the count enable command (Y18) is ON or OFF.

### 3.5.6 Count disable function

Stop the count operation while the count enable command is ON.

The relationships between the count enable command and the counter start command and between them and the counter present value are shown below:




1) Starts counting pulses when the count enable command (Y18) is turned ON.

2) Stops counting when the counter function start command (Y1C, F.START terminal) is turned ON.

3) Resumes the counting when the counter function start command (Y1C, F.START terminal) is turned OFF.

4) Stops the counting when the count enable command (Y18) is turned OFF.

5) Stops counting independently of the counter function start command (Y1C, F.START terminal), since the count enable command (Y18) is OFF.

6) Continues to stop counting even when the count enable command (Y18) is turned ON, since the counter function start command (Y1C, F.START terminal) is OFF.

7) Resumes the counting when the counter function start command (Y1C, F.START terminal).

# 4. PULSE INPUT AND COUNTER PROCESSING METHOD

This section describes the pulse input and counter processing method.

(1) Either 1-phase or 2-phase pulse input may be executed.

(a) 1-Phase pulse input

When 1-phase pulse input is executed, the following counts can be made:

1) Counts the phase A pulse inputs incrementally and counts the pulses by the decremental count command.

2) Counts the phase A pulse inputs incrementally and counts the phase B pulse inputs decrementally.

(b) 2-Phase pulse input

1) Multiplied by one: Counts phase A pulses at the leading edge.

2) Multiplied by two: Counts phase A pulses both at the leading edge and at the fall.

3) Multiplied by four: Counts phase A/B pulses both at the leading edge and at the fall.

(2) When 1-phase pulse input is done, the pulses are counted at the leading edge.

(3) When the pulse input mode is changed, the count is made from "0".

## 4.1 Counting at 1-Phase Input

This section explains the counter processing method for 1-phase input.

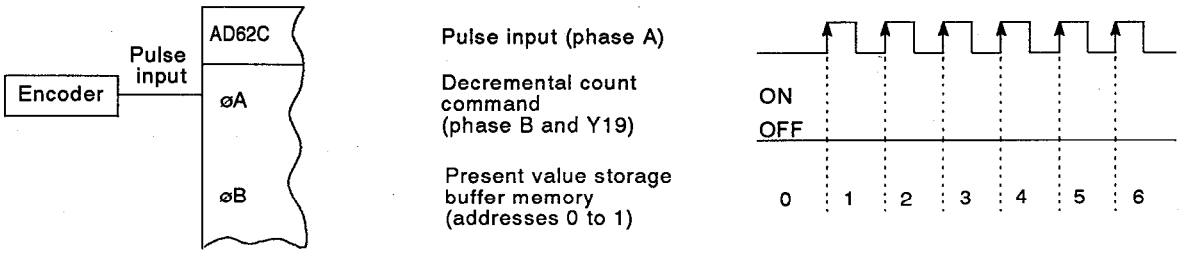
### 4.1.1 Counting using the phase A pulse input and decremental count command

The following counts can be made using the incremental phase A pulse input and decremental count command:

- Incrementally counts pulses input to phase A.
- Decrementally counts pulses when the decremental count command (voltage applied to phase B or Y19 turned ON by the PC CPU) is input at the leading edge of a pulse input to phase A.

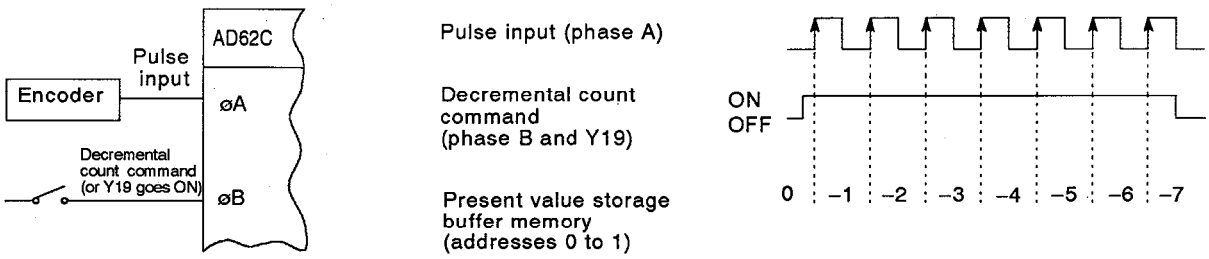
(1) Incremental count

When an incremental count is executed, the operation timing of the pulse inputs, decremental count command, and the present value of the storage buffer memory are shown below:




(2) Decremental count

When a decremental count is executed, the operation timing of pulse inputs, decremental count command, and the present value of the storage buffer memory are shown below:




**POINT**

When the decremental count command is executed, apply voltage to phase B or turn ON Y19.

(3) Counter processing mode setting

To use the above-mentioned mode (counting using the phase A pulse input and decremental count command), set the AD62C pulse input mode setting buffer memory (address 4) to "0" using the sequence program.

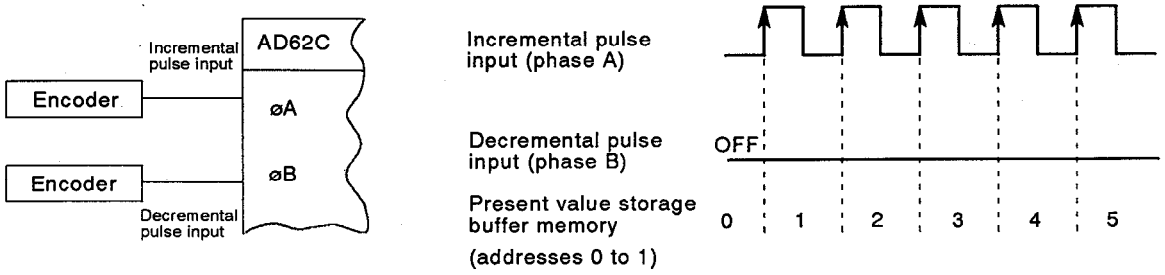
### 4.1.2 Counting using the incremental phase A pulse input and the decremental phase B pulse input

The following counts can be made using the incremental phase A pulse input and the decremental count command:

- Incrementally counts the pulses that are input to phase A at the leading edge.
- Decrementally counts the pulses that are input to phase A at the leading edge.
- Subtracts the number of incremental pulses from the number of decremental pulses when the pulses are input to both phases A and B.

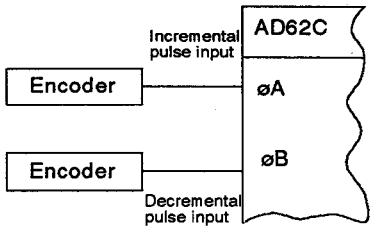
(1) Incremental count

When an incremental count is made, the operation timings of the incremental and decremental pulse inputs, and the present value of the storage buffer memory are shown below:



(2) Decremental count

When a decremental count is made, the operation timings of the incremental and decremental pulse inputs, and the present value of the storage buffer memory are shown below:

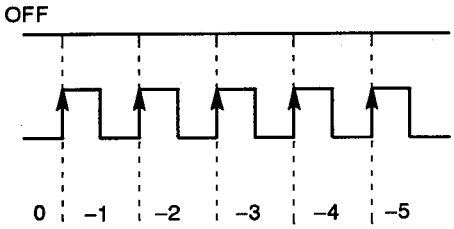



Incremental pulse input (phase A)

Decremental pulse input (phase B)

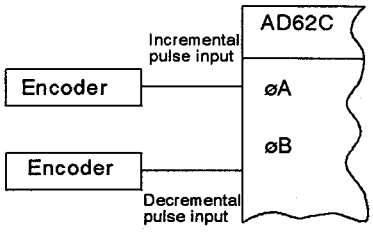
Present value storage buffer memory

(addresses 0 to 1)




(3) Incremental/decremental count

When an incremental/decremental count is made, the operation timings of the incremental and decremental pulse inputs, and the present value of the storage buffer memory are shown below:

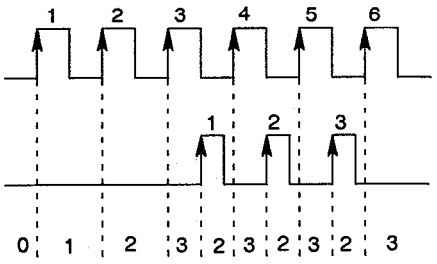



Incremental pulse input (phase A)

Decremental pulse input (phase B)

Present value storage buffer memory

(addresses 0 to 1)




(4) Counter processing mode setting

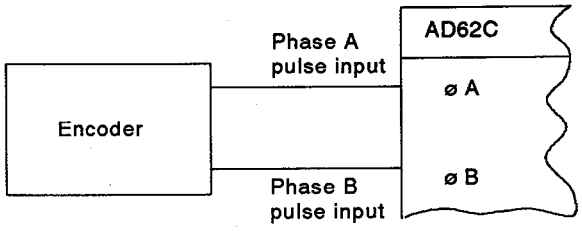
To use the above-mentioned mode (counting using the incremental phase A pulse input and decremental phase B pulse input), set the AD62C pulse input mode setting buffer memory (address 4) to "0" using the sequence program.

## 4.2 Counting at 2-Phase Pulse Input

When the 2-phase pulse input is done, the counting mode can be selected from multiplication by one, two, and four.

- Multiplied by one: Incrementally and decrementally counts phase A pulses at the leading edge.
- Multiplied by two: Incrementally and decrementally counts phase A pulses both at the leading edge and at the fall.
- Multiplied by four: Incrementally and decrementally counts phase A/B pulses both at the leading edge and at the fall.

(1) The relationship between the phase A pulse input and the phase B pulse input is given below:




(2) Counter processing mode setting

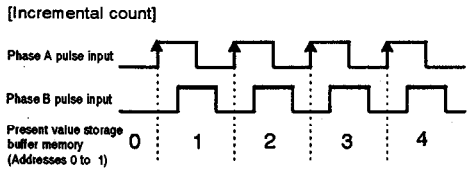
To use the above-mentioned mode (counting using the incremental phase A pulse input and decremental phase B pulse input), set the AD62C pulse input mode setting buffer memory (address 5) to any number from 2 to 4 using the sequence program.

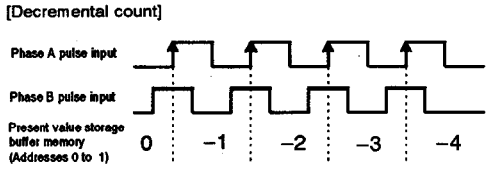
| Counting Mode | Setting Value |
|---|---|
| Multiplied by one | 2 |
| Multiplied by two | 3 |
| Multiplied by three | 4 |

### 4.2.1 Counting using 2-phase pulse input multiplied by one

Count is made at leading edge of phase A pulse.

The phase difference between phase A and phase B pulses determines whether the count is made incrementally or decrementally.



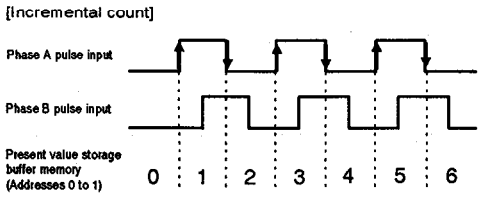

| | Timings to Make an Incremental Count |
|---|---|
| Phase A | Leading edge |
| Phase B | OFF |

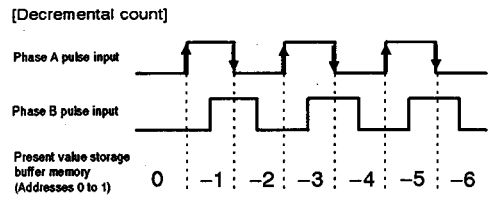
| | Timings to Make a Decremental Count |
|---|---|
| Phase A | Leading edge |
| Phase B | ON |

### 4.2.2 Counting using 2-phase pulse input multiplied by two

Count is made both at the leading edge and at the fall of the phase A pulse.

The phase difference between phase A and phase B pulses determines whether the count is made incrementally or decrementally.



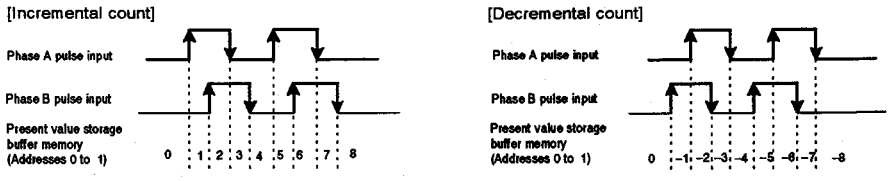

| | Timings to Make an Incremental Count | |
|---|---|---|
| Phase A | Leading edge | Fall |
| Phase B | OFF | ON |

| | Timings to Make a Decremental Count | |
|---|---|---|
| Phase A | Leading edge | Fall |
| Phase B | ON | OFF |

### 4.2.3 Counting using 2-phase pulse input multiplied by four

Count is made both at the leading edge and at the fall of the phase A/B pulse.

The phase difference between phase A and phase B pulses determines whether the count is made incrementally or decrementally.




| | Timings to Make an Incremental Count | | | |
|---|---|---|---|---|
| Phase A | Leading edge | Fall | ON | OFF |
| Phase B | OFF | ON | Leading edge | Fall |

| | Timings to Make a Decremental Count | | | |
|---|---|---|---|---|
| Phase A | Leading edge | Fall | OFF | ON |
| Phase B | ON | OFF | Leading edge | Fall |

### 4.3 Reading the Present Value

The following describes the contents of the present value stored in the addresses 0 to 1 of the AD62C buffer memory and how to read the present value.

(1) In this buffer area, the count values are stored when a pulse input, preset, ring counter function, or count disable (counter function selection) is executed.

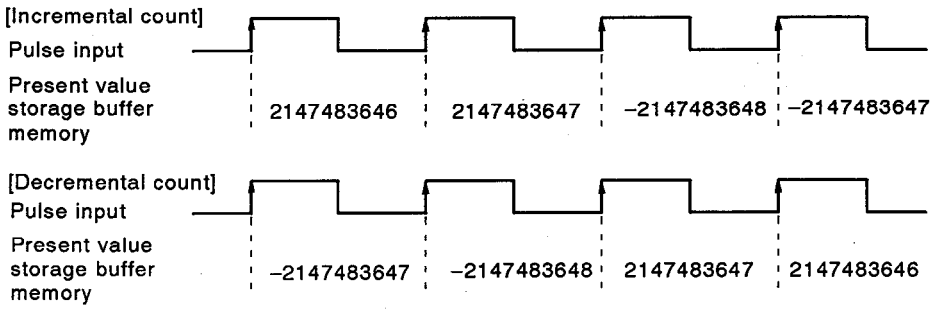
However, the counter values are stored in the counter function selection count value of the storage buffer memory (addresses 2 to 3) when a latch counter, a sampling counter, or a periodic pulse counter function is executed.

(2) The present value of –2147483648 to 2147483647 is stored in signed 32-bit binary code to the buffer memory.

When the present value is negative, that data is stored as a complementary number of two to the present value of the storage buffer memory.

(3) When an incremental count is made, if the value exceeds 2147483647, it will jump to –2147483648.

When a decremental count is made, if the value exceeds –2147483648, it will jump to 2147483647.




**POINT**

The programming for reading the present value differs according to which link method is used.

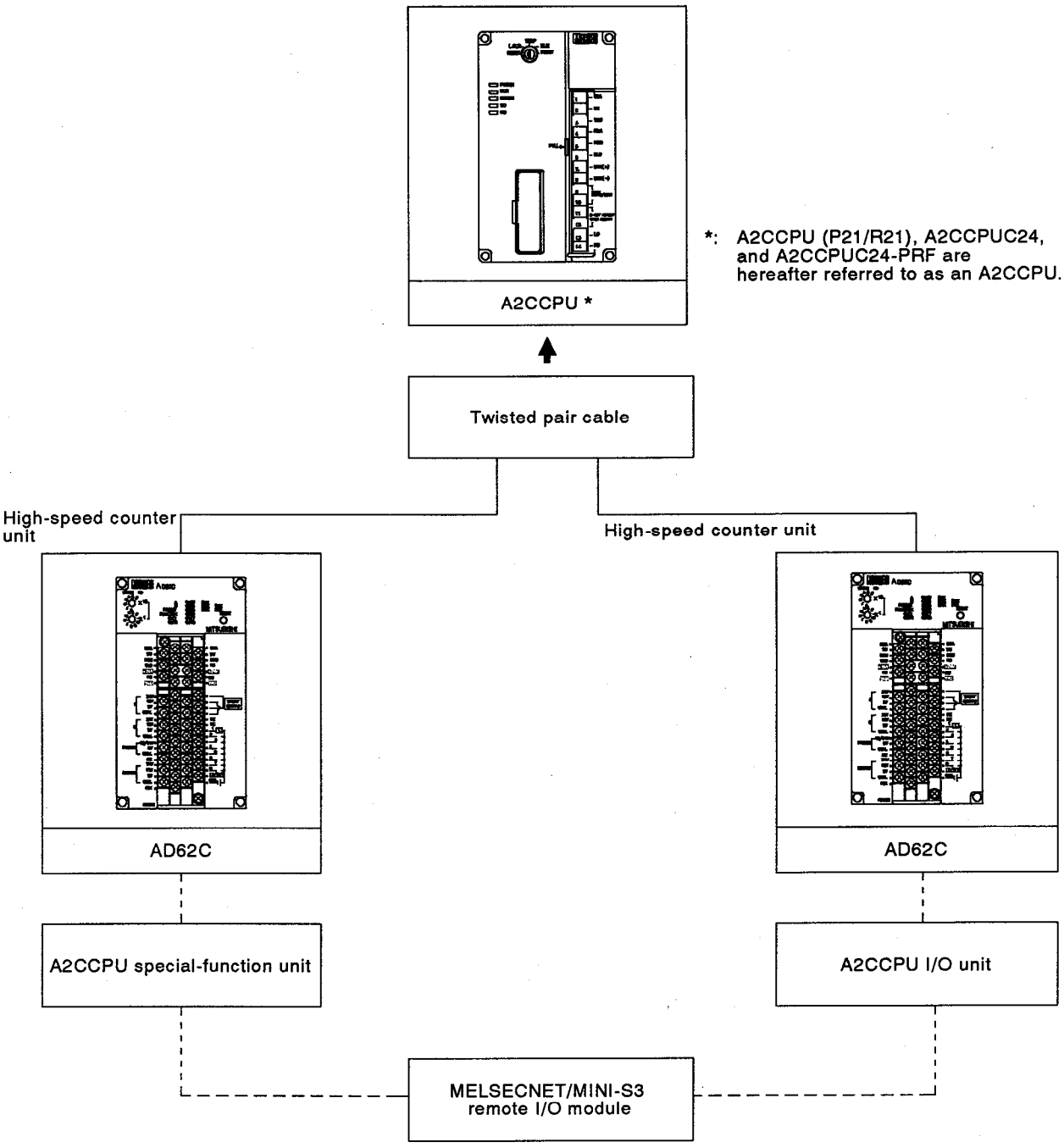
Therefore, refer to the programming example for the corresponding link method.

# 5. LINKING TO THE A2CCPU

## 5.1 System Configuration

### 5.1.1 Overall configuration

(1) The overall configuration of the AD62C using an A2CCPU is shown below.



### 5.1.2 Precautions when constructing the system

(1) All AD62Cs are linked using twisted pair cables.

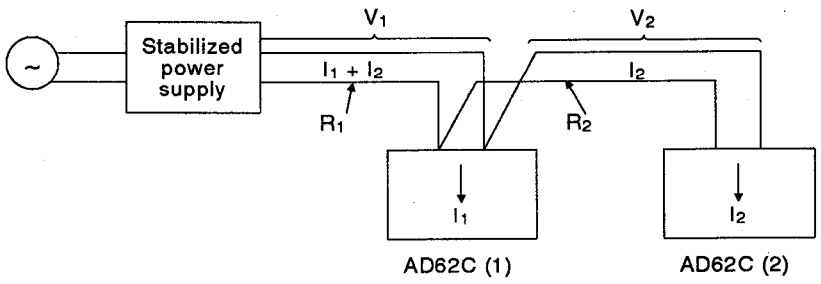
(2) Since each AD62C occupies 4 stations and a total of 32 I/O points, be careful when setting station numbers and allocating I/O addresses.

(3) The AD62C requires a 24 VDC power supply.

When supplying power from one power supply to multiple AD62Cs or to the link I/O modules, select proper cables and wiring route taking voltage drops into consideration.

**REMARK**

Calculating the AD62C's receiving port voltage



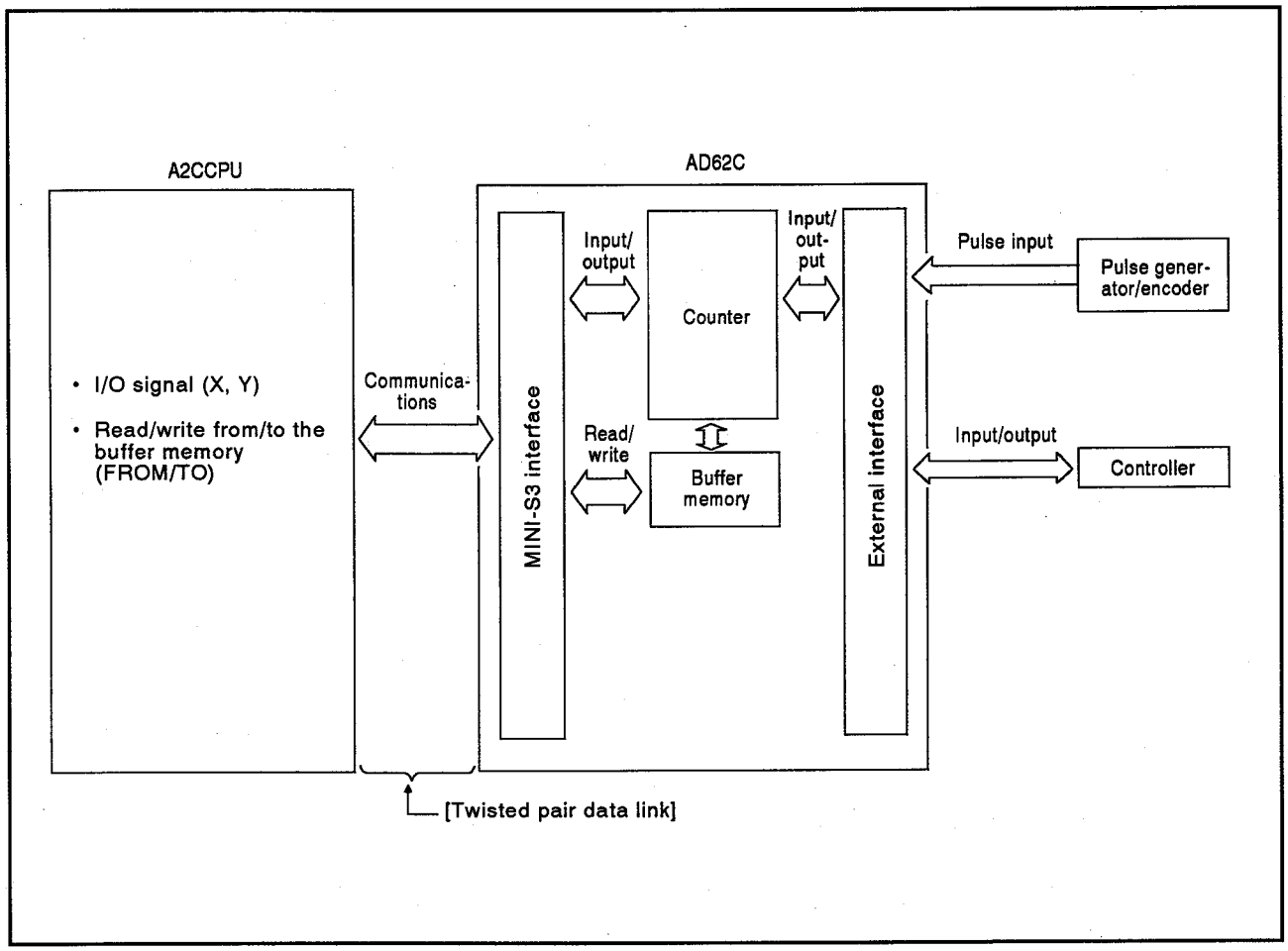

$V_1$ : Voltage drop between stabilized power supply and AD62C (1)
$V_2$ : Voltage drop between AD62C (1) and AD62C (2)
$R_1$ : Resistance between stabilized power supply and AD62C (1)
$R_2$ : Resistance between AD62C (1) and AD62C (2)
$I_1$ : AD62C (1) current consumption
$I_2$ : AD62C (2) current consumption

- Calculating voltage drops $V_1 = R_1 \times (I_1 + I_2)$
  $V_2 + R_2 \times I_2$
- AD62C's receiving port voltage
  (AD62C (1) receiving port voltage) = (stabilized power supply) – $V_1$
  (AD62C (2) receiving port voltage) = (stabilized power supply) – ($V_1$ + $V_2$)
- Connection is possible if the AD62C receiving port voltage is within the range 15.6 V through 31.2 V.

## 5.2 Data Communication Processing

### 5.2.1 Communication method

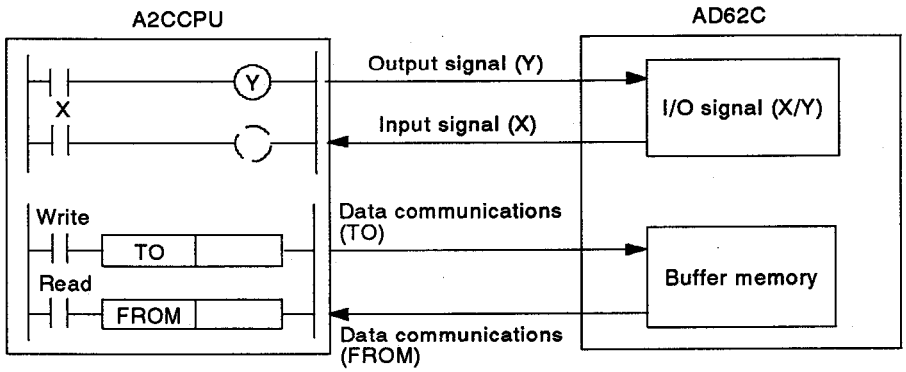
(1) The following diagram shows how communications is done between an AD62C and an A2CCPU.




(a) Communications of I/O signals and counter data with the A2CCPU is done via the MINI-S3 interface.

Data such as preset values, set values, and present values is stored to the AD62C buffer memory.

(2) I/O signal processing and buffer memory data processing are shown below.




(a) I/O signal processing

Output (Y): The A2CCPU outputs output signal (Y) to the AD62C at the end processing by turning it ON/OFF using the sequence program.

Input (X): The A2CCPU reads the ON/OFF status of input signal (X) from the AD62C using the sequence program's end processing and executes program operations.

(b) Buffer memory data processing

Write: The A2CCPU writes data to the AD62C's buffer memory using the sequence program's TO instruction.

Read: The A2CCPU reads data from the AD62C's buffer memory using the sequence program's FROM instruction.

### 5.2.2 Processing time

The processing time required to write data to and read data from the AD62C buffer memory is shown below.

| Items | Max. Processing Time |
|---|---|
| (1) Data write | [10 msec x (number of data feeds)] + *1 130 msec |
| (2) Data read | *1 :Total value of the AD62C internal processing time and the A2CCPU processing time |

**POINTS**

(1) Count start/stop by external input, preset, and the counter coincidence signal by external output respond in less than 10 msec.

(2) To increase the processing time responsiveness of sequence operations, use external I/O signals.

## 5.3 I/O Signals To/From the PC CPU

AD62C I/O signals to/from an A2CCPU are shown below. The following I/O device numbers apply when the AD62C's station number is 01 (X/Y00 to X/Y1F).

(1) Input signals (signal direction: AD62C → A2CCPU)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| X00 to X03 | (Unusable) | — |
| *1 X04 | Communications error detection | • Latched to ON when an error is detected in the AD62C.<br>• Switches OFF when the communications error detection reset signal (Y04) switches from OFF to ON. |
| X05 | Reset status detection | • Latched to ON when power to the AD62C is turned ON or the reset switch is turned ON.<br>• Switches OFF when the reset status detection reset signal (Y05) switches from OFF to ON. |
| X06 | (Unusable) | — |
| *2 X07 | Communications completed wait flag | • Set when data transmission from the A2CCPU is completed.<br>• Reset when a communications completed flag is received from the AD62C.<br>• Reset when the communications completed wait flag reset signal (Y07) switches from OFF to ON. |
| X08 to X1A | (Unusable) | — |
| X1B | Fuse blown detection | • Switches ON when a fuse is blown or when external power for the limit switch output is turned OFF. |
| X1C | Sampling/periodic counter ON/OFF flag | • Switches ON when the sampling/periodic counter function is executed. |
| X1D | Limit switch output READY flag | • Set when limit switch output is enabled.<br>• Reset when the dog setting has an error. |
| X1E | External preset request detection | • Latched to ON when an external preset request is given.<br>• Switches OFF when the external preset request detection signal reset command (Y1E) switches from OFF to ON. |
| X1F | Multiple-dog setting error detection | • Latched to ON when a multiple-dog setting error is detected in the AD62C.<br>• Switches OFF when the multiple-dog setting error detection reset command (Y1F) switches from OFF to ON. |

*1, *2: Input signals used on the A2CCPU side.

(2) Output signals (signal direction: A2CCPU → AD62C)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| Y00 to Y03 | (Unusable) | — |
| *1 Y04 | Communications error detection reset | • When this signal switches from OFF to ON, the communications error detection signal (X04) switches OFF and the error codes in the AD62C buffer memory are reset.<br>• Switches OFF when (X04) switches OFF. |
| Y05 | Reset status detection reset | • When this signal switches from OFF to ON, the reset status detection signal (X05) switches OFF.<br>• Switches OFF when (X05) switches OFF. |
| Y06 | (Unusable) | — |
| *2 Y07 | Communications completed wait flag reset | • When this signal switches from OFF to ON, the communications completed wait flag (X07) switches OFF.<br>• Switches OFF when (X07) switches OFF. |
| Y08 to Y17 | (Unusable) | — |
| Y18 | Count enable command | • Enables counting operations of the AD62C when switched ON. |
| Y19 | Decremental count command | • Valid only in the direction input mode and when a 1-phase pulse is input.<br>• Counts decrementally when this signal is ON.<br>• Cannot be used with an external input (øB). |
| Y1A | Preset command | • Executes preset operations. |
| Y1B | Ring counter command | • Starts the ring counter. |
| Y1C | Counter function selection start command | • Selects the counter function. |
| Y1D | Limit switch output enable command | • Enables limit switch output (8 channels in batch).<br>• When (Y1D) is OFF, this command is not output and all channels are OFF. |
| Y1E | External preset request detection reset command | • When this signal switches from OFF to ON, the external preset request detection flag (X1E) switches OFF.<br>• Switches OFF when (X1E) switches OFF. |
| Y1F | Multiple-dog setting error detection reset | • When this signal switches from OFF to ON, the multiple-dog setting error detection signal (X1F) switches OFF and the error codes of the AD62C buffer memory are reset.<br>• Switches OFF after (X1F) switches OFF. |

*1, *2: Output signals used on the A2CCPU side.

## 5.4 Buffer Memory Assignments

Table 5.1 shows the buffer memory assignments of the AD62C.

The next page gives detailed information about the settings of buffer memory addresses 14 to 149.

Initial values are set in the buffer memory when power to the AD62C is turned ON or when the AD62C is reset.

The contents in the buffer memory can be read/written using a FROM/TO instruction in an AD62C sequence program.

**Table 5.1 Buffer Memory Assignments**

| Addresses | Setting Contents | Initial Values | Read/write | Reference Sections |
|---|---|---|---|---|
| 0 | Present value (L) | 0 | Read only | 4.3 |
| 1 | Present value (H) | | | |
| 2 | Counter function selection count value (L) | 0 | | 3.5.1 |
| 3 | Counter function selection count value (H) | | | |
| 4 | Limit switch output state flag (CH 1 to CH 8) | 0 | | 3.4 |
| 5 | Pulse input mode setting | 0 | Read/write possible | 4 |
| 6 | Counter function selection setting | 0 | | 3.5 |
| 7 | Preset value setting (L) | 0 | | 3.2 |
| 8 | Preset value setting (H) | | | |
| 9 | Ring counter value setting (L) | 1024 | | 3.3 |
| 10 | Ring counter value setting (H) | | | |
| 11 | Sampling/periodic time setting | 1 | | 3.5.4 and 3.5.5 |
| 12 | Communications error code | 0 | | 9.1 |
| 13 | Multiple-dog setting error code | 0 | | |
| 14 to 30 | CH 1 limit switch output data setting | 0 | Read/write possible | 3.4 |
| 31 to 47 | CH 2 limit switch output data setting | 0 | | |
| 48 to 64 | CH 3 limit switch output data setting | 0 | | |
| 65 to 81 | CH 4 limit switch output data setting | 0 | | |
| 82 to 98 | CH 5 limit switch output data setting | 0 | | |
| 99 to 115 | CH 6 limit switch output data setting | 0 | | |
| 116 to 132 | CH 7 limit switch output data setting | 0 | | |
| 133 to 149 | CH 8 limit switch output data setting | 0 | | |

The following gives detailed information about the settings of buffer memory addresses 14 to 149 (limit switch output data setting of CH 1 to CH 8)

| Setting Contents | | Buffer Memory Addresses | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 14 to 30 CH.1 | 31 to 47 CH.2 | 48 to 64 CH.3 | 65 to 81 CH.4 | 82 to 98 CH.5 | 99 to 115 CH.6 | 116 to 132 CH.7 | 133 to 149 CH.8 |
| Number of multiple dogs for CH [ ] | | 14 | 31 | 48 | 65 | 82 | 99 | 116 | 133 |
| ····· CH [ ] Dog 0 ON address | (L) | 15 | 32 | 49 | 66 | 83 | 100 | 117 | 134 |
| | (H) | 16 | 33 | 50 | 67 | 84 | 101 | 118 | 135 |
| ····· CH [ ] Dog 0 OFF address | (L) | 17 | 34 | 51 | 68 | 85 | 102 | 119 | 136 |
| | (H) | 18 | 35 | 52 | 69 | 86 | 103 | 120 | 137 |
| ····· CH [ ] Dog 1 ON address | (L) | 19 | 36 | 53 | 70 | 87 | 104 | 121 | 138 |
| | (H) | 20 | 37 | 54 | 71 | 88 | 105 | 122 | 139 |
| ····· CH [ ] Dog 1 OFF address | (L) | 21 | 38 | 55 | 72 | 89 | 106 | 123 | 140 |
| | (H) | 22 | 39 | 56 | 73 | 90 | 107 | 124 | 141 |
| ····· CH [ ] Dog 2 ON address | (L) | 23 | 40 | 57 | 74 | 91 | 108 | 125 | 142 |
| | (H) | 24 | 41 | 58 | 75 | 92 | 109 | 126 | 143 |
| ····· CH [ ] Dog 2 OFF address | (L) | 25 | 42 | 59 | 76 | 93 | 110 | 127 | 144 |
| | (H) | 26 | 43 | 60 | 77 | 94 | 111 | 128 | 145 |
| ····· CH [ ] Dog 3 ON address | (L) | 27 | 44 | 61 | 78 | 95 | 112 | 129 | 146 |
| | (H) | 28 | 45 | 62 | 79 | 96 | 113 | 130 | 147 |
| ····· CH [ ] Dog 3 OFF address | (L) | 29 | 46 | 63 | 80 | 97 | 114 | 131 | 148 |
| | (H) | 30 | 47 | 64 | 81 | 98 | 115 | 132 | 149 |

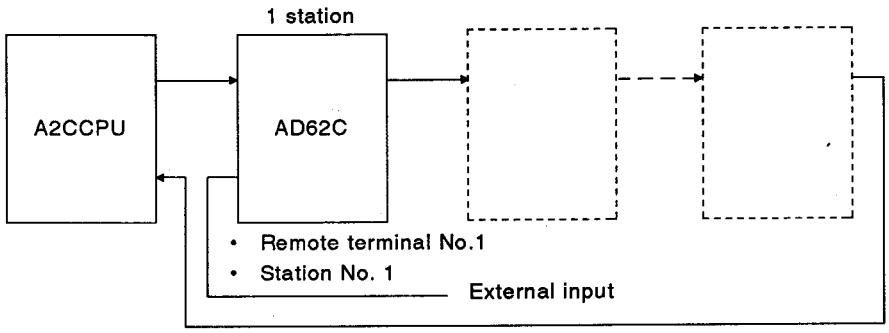
[ ] = Channel number displayed

## 5.5 Programming Examples

In this section, the procedures for using sequence program instructions and programming methods are explained using programming examples.

- The programming examples shown in this section are applicable when executing parameter remote terminal settings (MINI standard protocol selection) using the GPP function of a peripheral device.
- When using the A6GPP/A6PHP software package's SW3GP-GPPA, since parameter remote terminals cannot be set, the equivalent contents of the terminal settings must be written to a special register using a sequence program. The A2CCPU User's Manual gives details.

This section explains programming when an A2CCPU and AD62C are set as shown below.



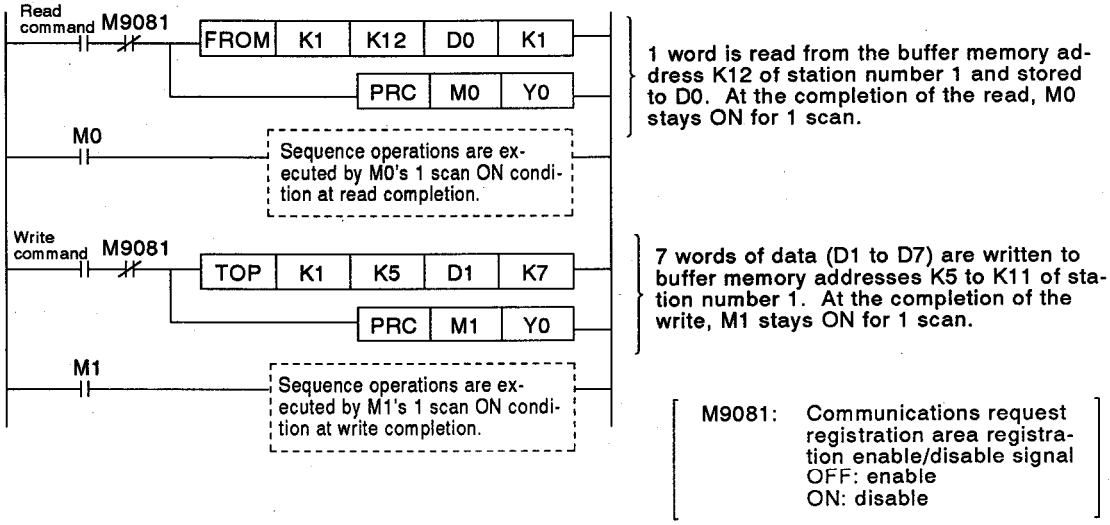

1) The MINI standard protocol is selected.
2) The mode is set to online automatic return enable.
3) The AD62C station number is set to "01" (occupying station Nos. 1 to 4).

**POINT**

If initial setting data is not set, SP.UNIT.ERR (error No. 46) occurs and the PC CPU stops operations.

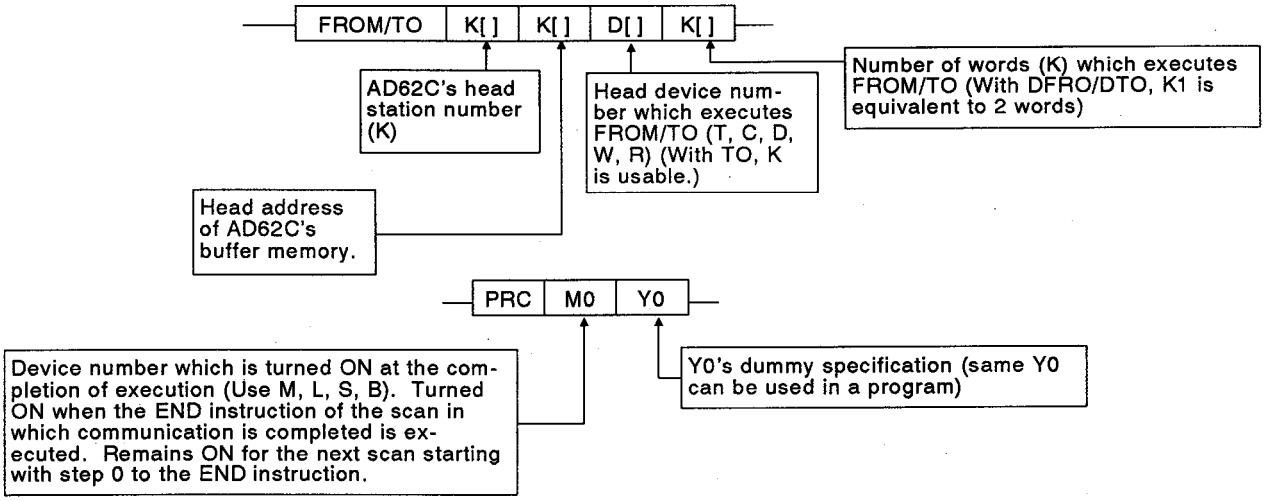
**[Basic programs]**

(1) Read/write processing program from/to the buffer memory




(2) FROM/TO and PRC instructions

For details, see the ACPU Programming Manual (Common Instructions).




**POINT**

When a FROM/TO instruction is executed by the A2CCPU sequence program, communication is executed via the link. When the PRC instruction execution complete device is turned ON, data communication ends.

### 5.5.1 Preset function programming example

(1) Preset function programming example using a sequence program

Create a program to count 2-phase pulses multiplied by one and to execute the preset function using the sequence program.

**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command.....M9038

(b) Count operation start command.....X20

(c) Present value read command.....X21

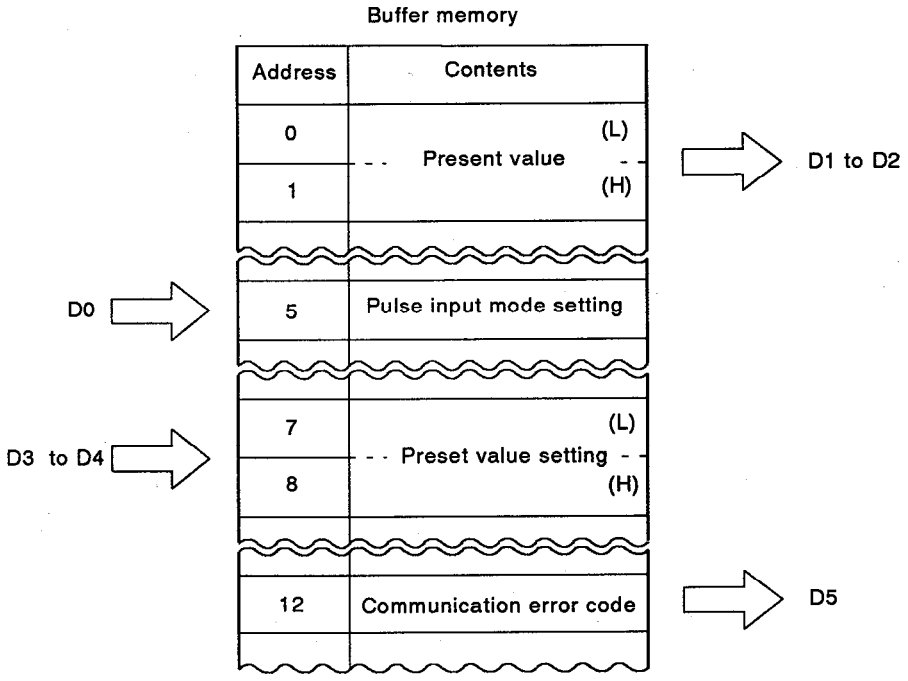
(d) Preset value write command.....X22

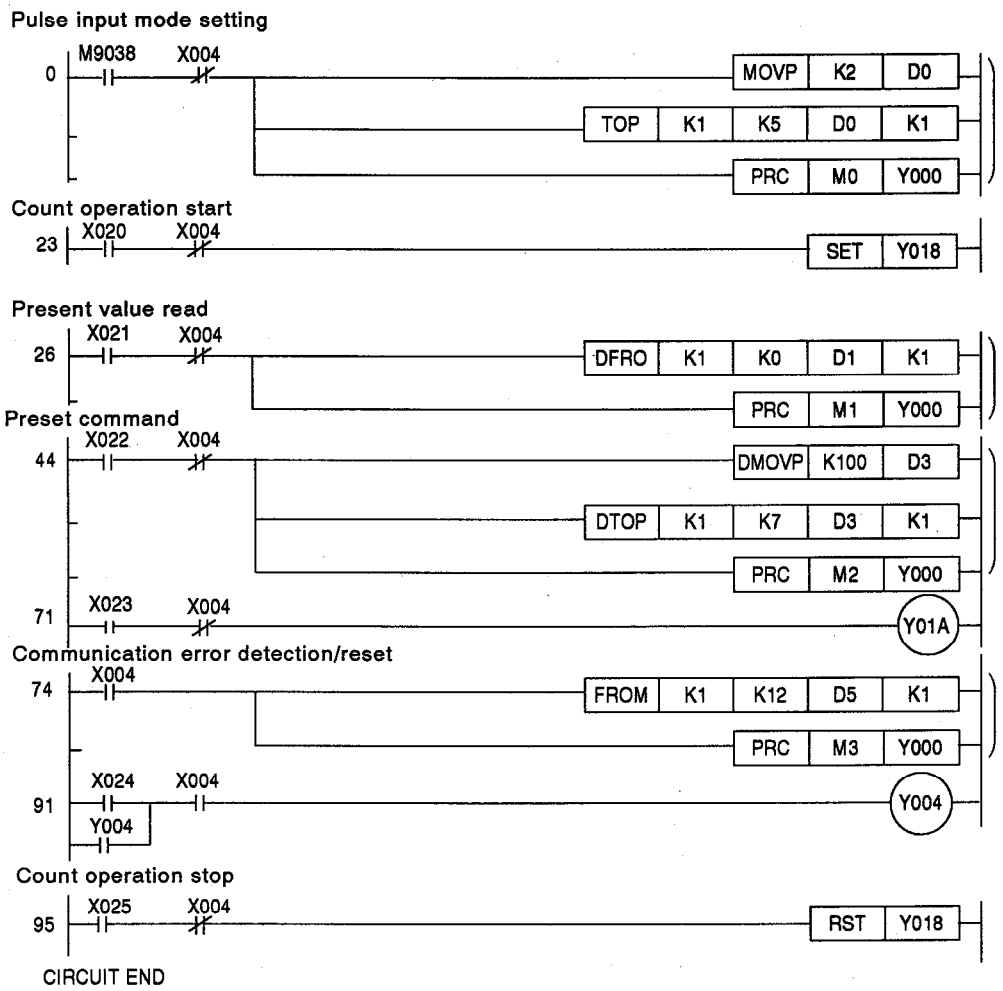
(e) Preset execute command.....X23

(f) Communication error reset command.....X24

(g) Count operation stop command.....X25

(b) Relationship between data register (D0 to D5) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
26
X021
X004
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Preset command
44
X022
X004
DMOVP K100 D3
DTOP K1 K7 D3 K1
PRC M2 Y000
Stores the preset value of 100 to buffer memory address7.
71
X023
X004
Y01A
Executes preset.
Communication error detection/reset
74
X004
FROM K1 K12 D5 K1
PRC M3 Y000
Reads the communication error code and stores it to device D5.
91
X024
X004
Y004
Y004
Resets the communication error.
Count operation stop
95
X025
X004
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

(2) Preset function programming example using an external input

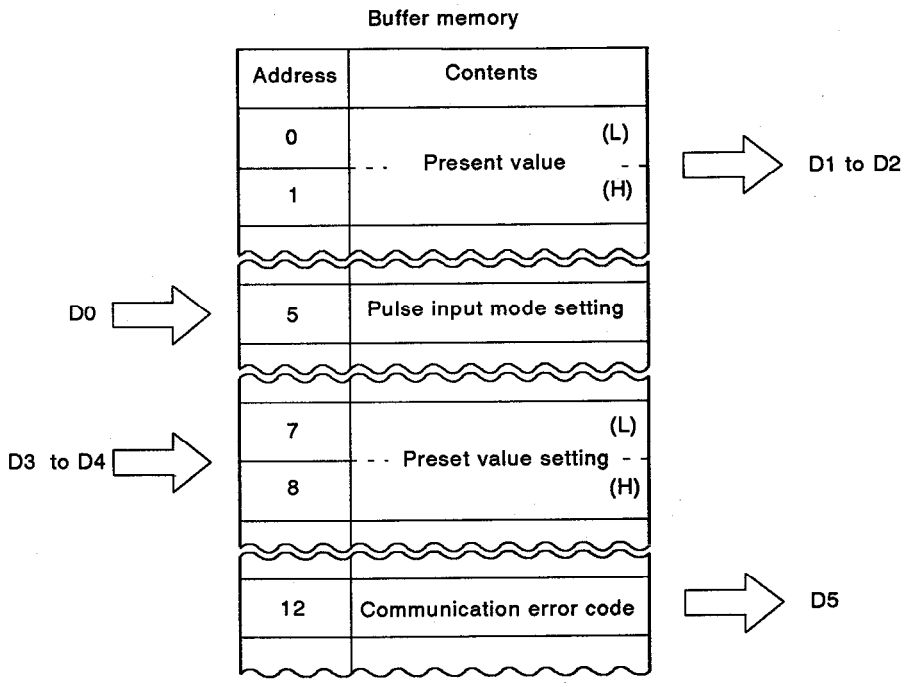
Create a program to count 2-phase pulses multiplied by one and to execute the preset function (applies voltage to PRESET terminal) with the external input.

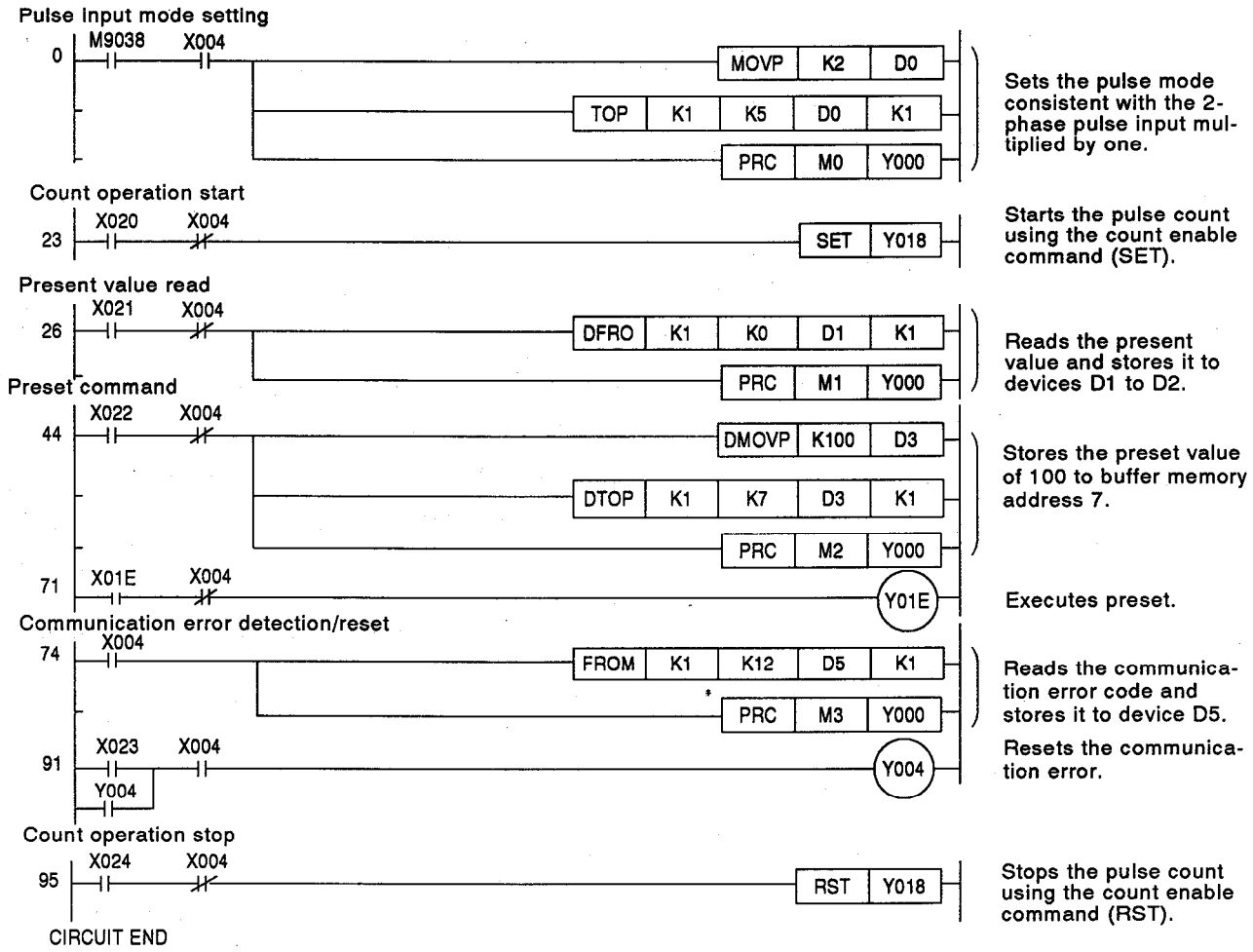
**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Count operation start command.....X20
(c) Present value read command.....X21
(d) Preset value write command.....X22
(e) External preset command detection flag reset command.....X23
(f) Communication error reset command.....X24
(g) Count operation stop command.....X25

(b) Relationship between data register (D0 to D5) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
26
X021
X004
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Preset command
44
X022
X004
DMOVP K100 D3
DTOP K1 K7 D3 K1
PRC M2 Y000
Stores the preset value of 100 to buffer memory address 7.
71
X01E
X004
Y01E
Executes preset.
Communication error detection/reset
74
X004
FROM K1 K12 D5 K1
PRC M3 Y000
Reads the communication error code and stores it to device D5.
91
X023
X004
Y004
Y004
Resets the communication error.
Count operation stop
95
X024
X004
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.2 Ring counter function programming example

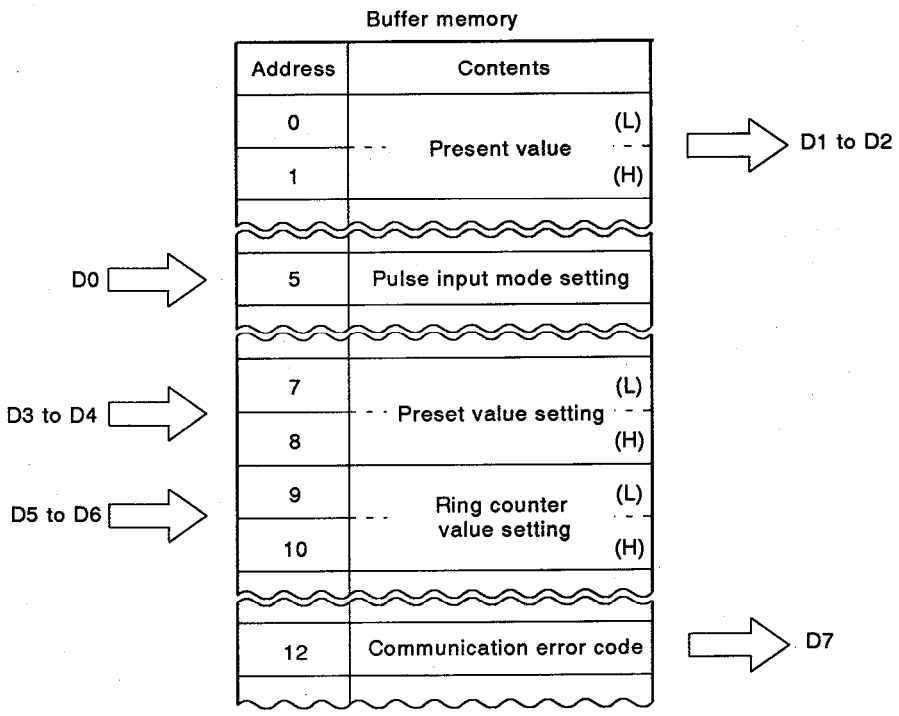
Create a program to count 2-phase pulses multiplied by one and to execute the ring counter function.

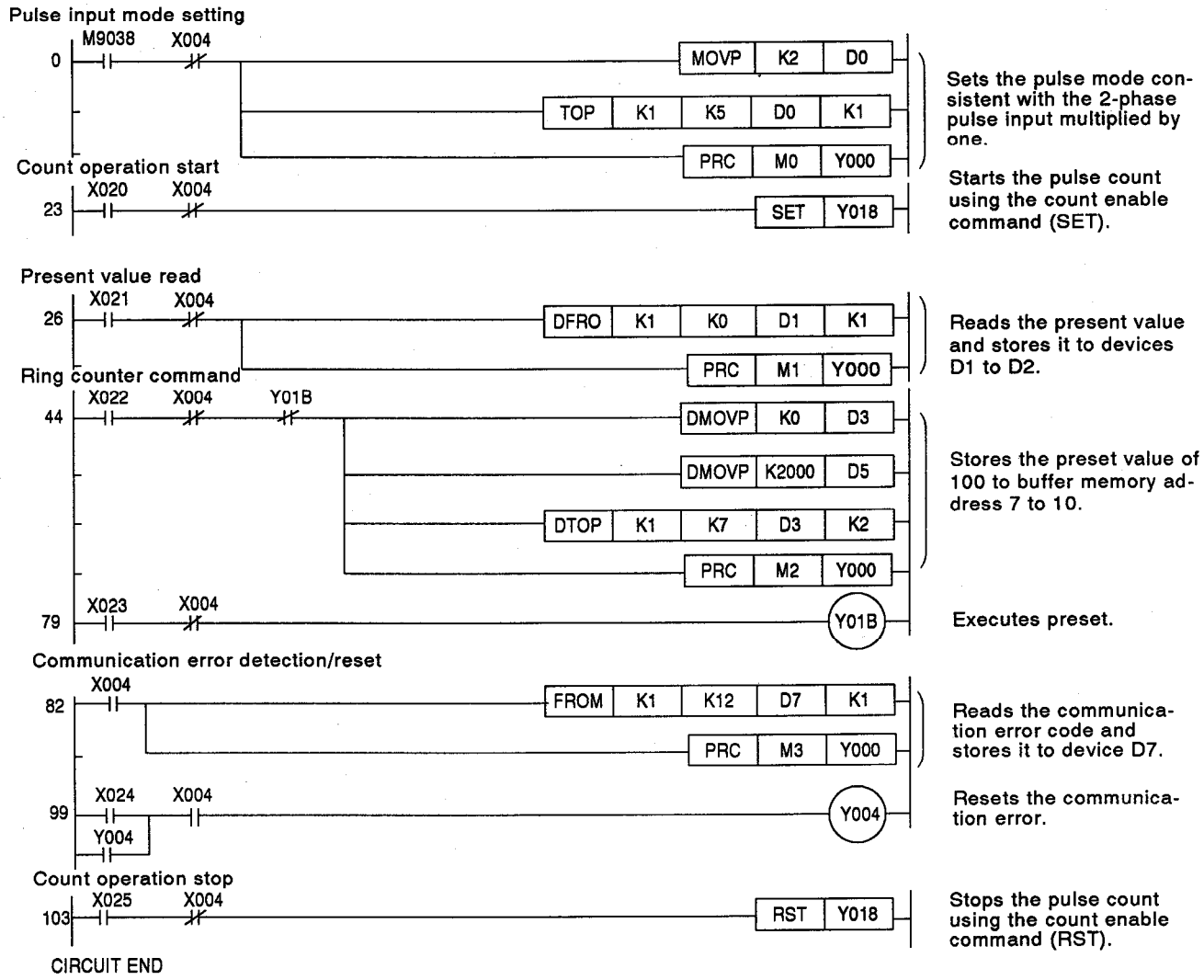
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Count operation start command.....X20
(c) Present value read command.....X21
(d) Preset value write command.....X22
(e) Ring counter command.....X23
(f) Communication error reset command.....X24
(g) Count operation stop command.....X25

(2) Relationship between data register (D0 to D5) and the buffer memory



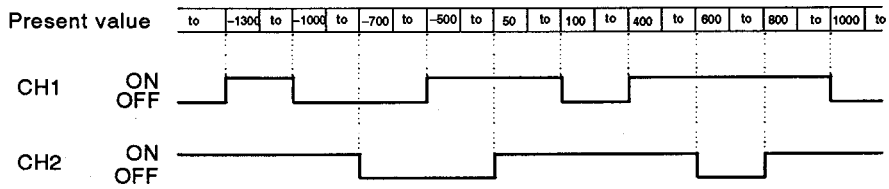

Pulse input mode setting
M9038
X004
0
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
X020
X004
23
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
X021
X004
26
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Ring counter command
X022
X004
Y01B
44
DMOVP K0 D3
DMOVP K2000 D5
DTOP K1 K7 D3 K2
PRC M2 Y000
Stores the preset value of 100 to buffer memory address 7 to 10.
X023
X004
79
Y01B
Executes preset.
Communication error detection/reset
X004
82
FROM K1 K12 D7 K1
PRC M3 Y000
Reads the communication error code and stores it to device D7.
X024
X004
99
Y004
Y004
Resets the communication error.
Count operation stop
X025
X004
103
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.3 Limit switch output function programming example

Create a program to count 2-phase pulses multiplied by one and to execute the limit switch function.

**[ Operation status ]**

ON/OFF status of the limit switch output is shown below:

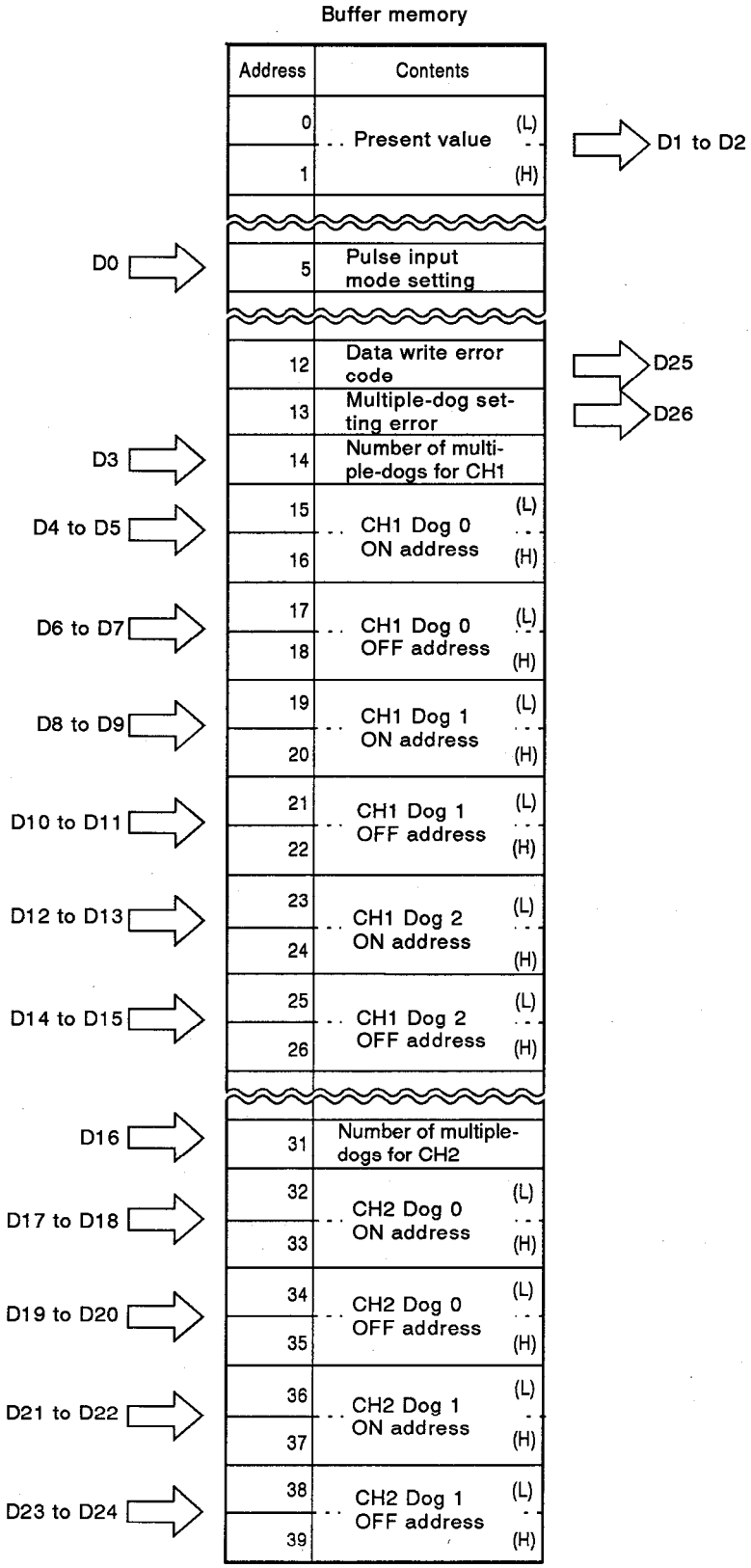


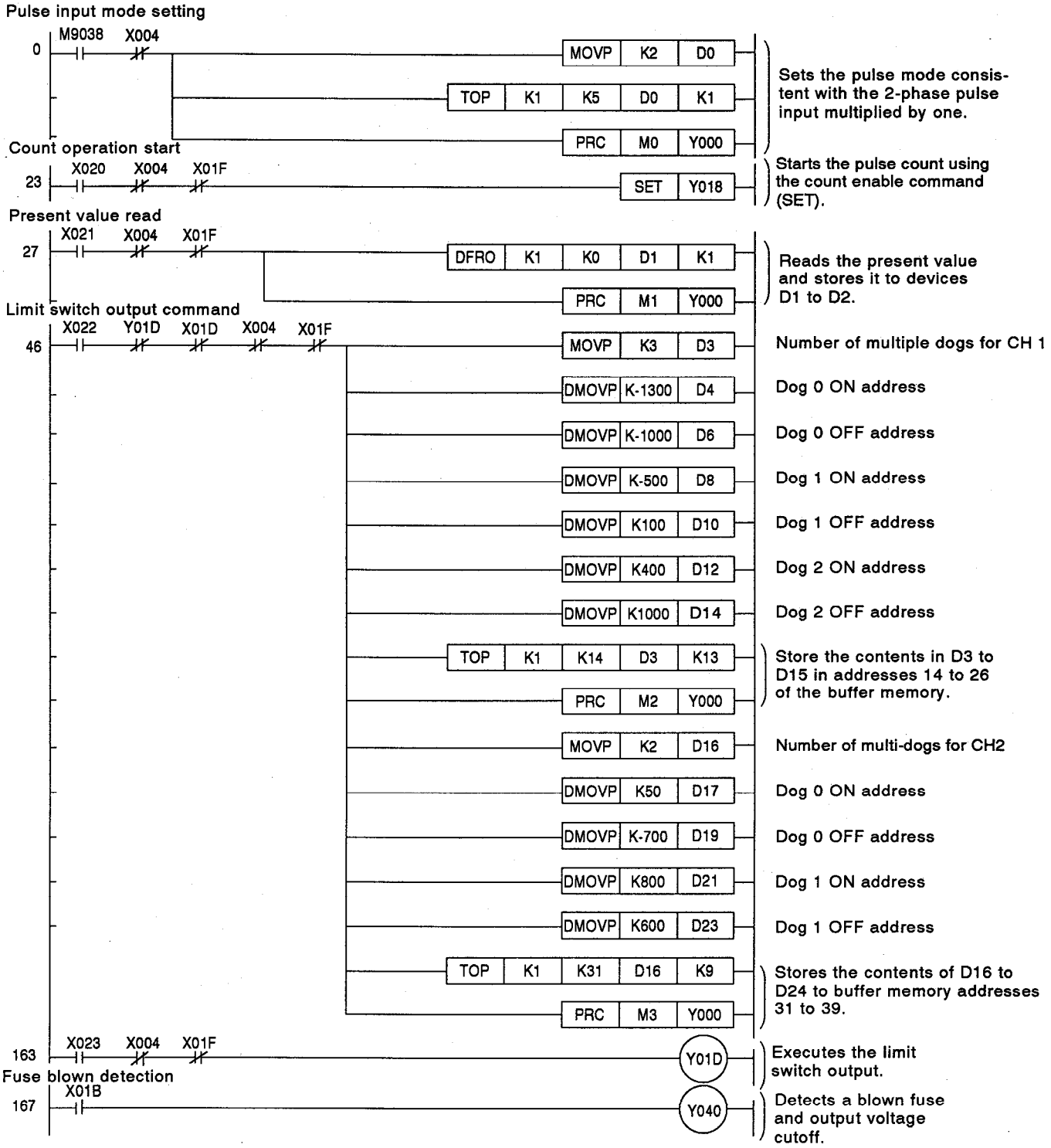

**[ Devices to be used ]**

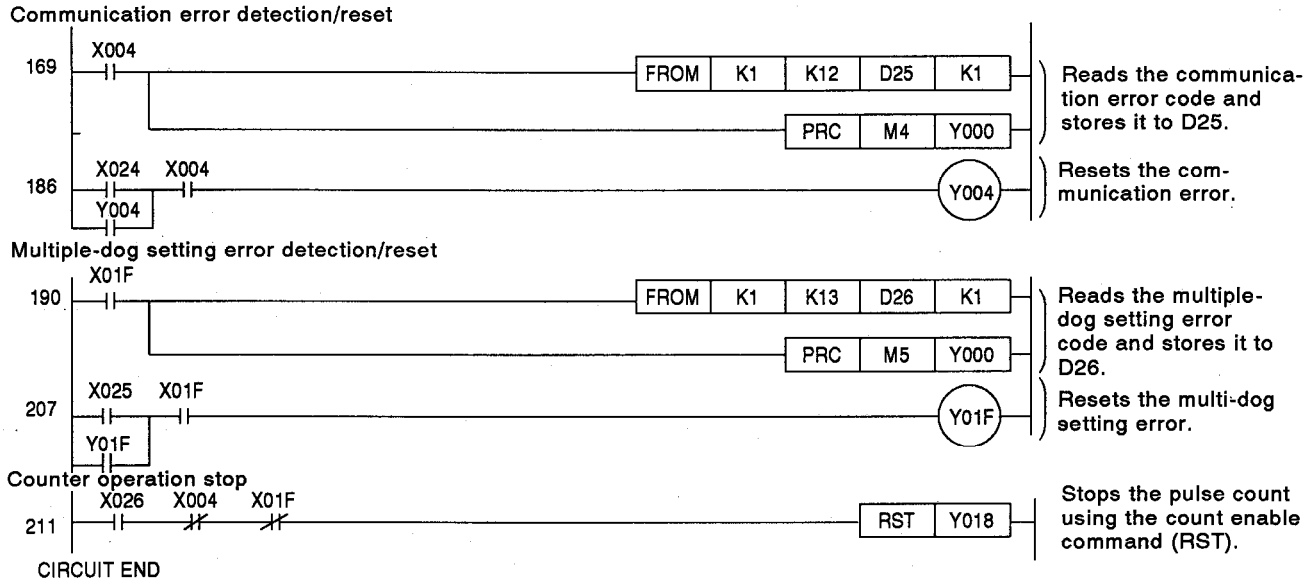
(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Fuse blown detection ..... X1B
(c) Count operation start command ..... X20
(d) Present value read command ..... X21
(e) Limit switch output data setting command ..... X22
(f) Limit switch output command ..... X23
(g) Communication error reset command ..... X24
(h) Multiple-dog setting error reset command ..... X26
(i) Count operation stop command ..... X25

(2) Relationship between the data register (D0 to D25) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
X01F
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
27
X021
X004
X01F
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Limit switch output command
46
X022
Y01D
X01D
X004
X01F
MOVP K3 D3
Number of multiple dogs for CH 1
DMOVP K-1300 D4
Dog 0 ON address
DMOVP K-1000 D6
Dog 0 OFF address
DMOVP K-500 D8
Dog 1 ON address
DMOVP K100 D10
Dog 1 OFF address
DMOVP K400 D12
Dog 2 ON address
DMOVP K1000 D14
Dog 2 OFF address
TOP K1 K14 D3 K13
PRC M2 Y000
Store the contents in D3 to D15 in addresses 14 to 26 of the buffer memory.
MOVP K2 D16
Number of multi-dogs for CH2
DMOVP K50 D17
Dog 0 ON address
DMOVP K-700 D19
Dog 0 OFF address
DMOVP K800 D21
Dog 1 ON address
DMOVP K600 D23
Dog 1 OFF address
TOP K1 K31 D16 K9
PRC M3 Y000
Stores the contents of D16 to D24 to buffer memory addresses 31 to 39.
163
X023
X004
X01F
Y01D
Executes the limit switch output.
Fuse blown detection
167
X01B
Y040
Detects a blown fuse and output voltage cutoff.


Communication error detection/reset
169
X004
FROM K1 K12 D25 K1
PRC M4 Y000
Reads the communication error code and stores it to D25.
186
X024 X004
Y004
Y004
Resets the communication error.
Multiple-dog setting error detection/reset
190
X01F
FROM K1 K13 D26 K1
PRC M5 Y000
Reads the multiple-dog setting error code and stores it to D26.
207
X025 X01F
Y01F
Y01F
Resets the multi-dog setting error.
Counter operation stop
211
X026 X004 X01F
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.4 Latch counter function programming example

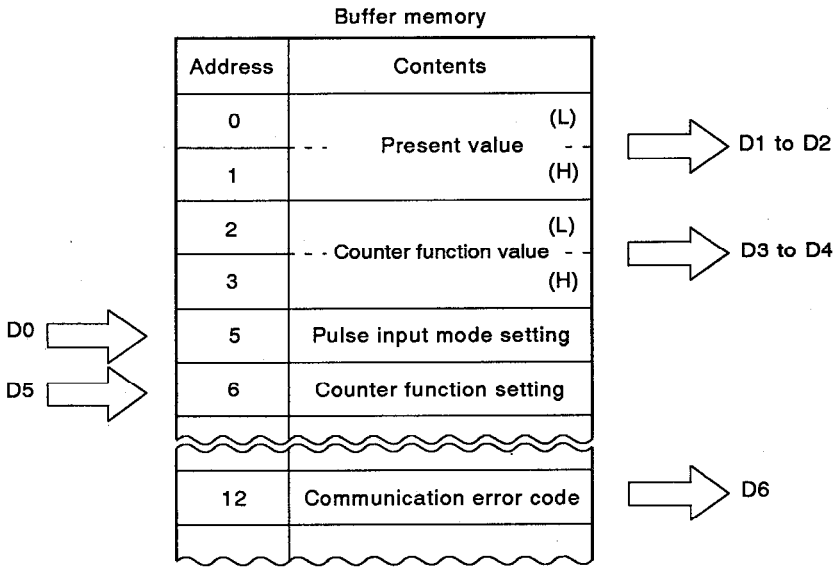
Create a program to count 2-phase pulses multiplied by one and to execute the latch counter.

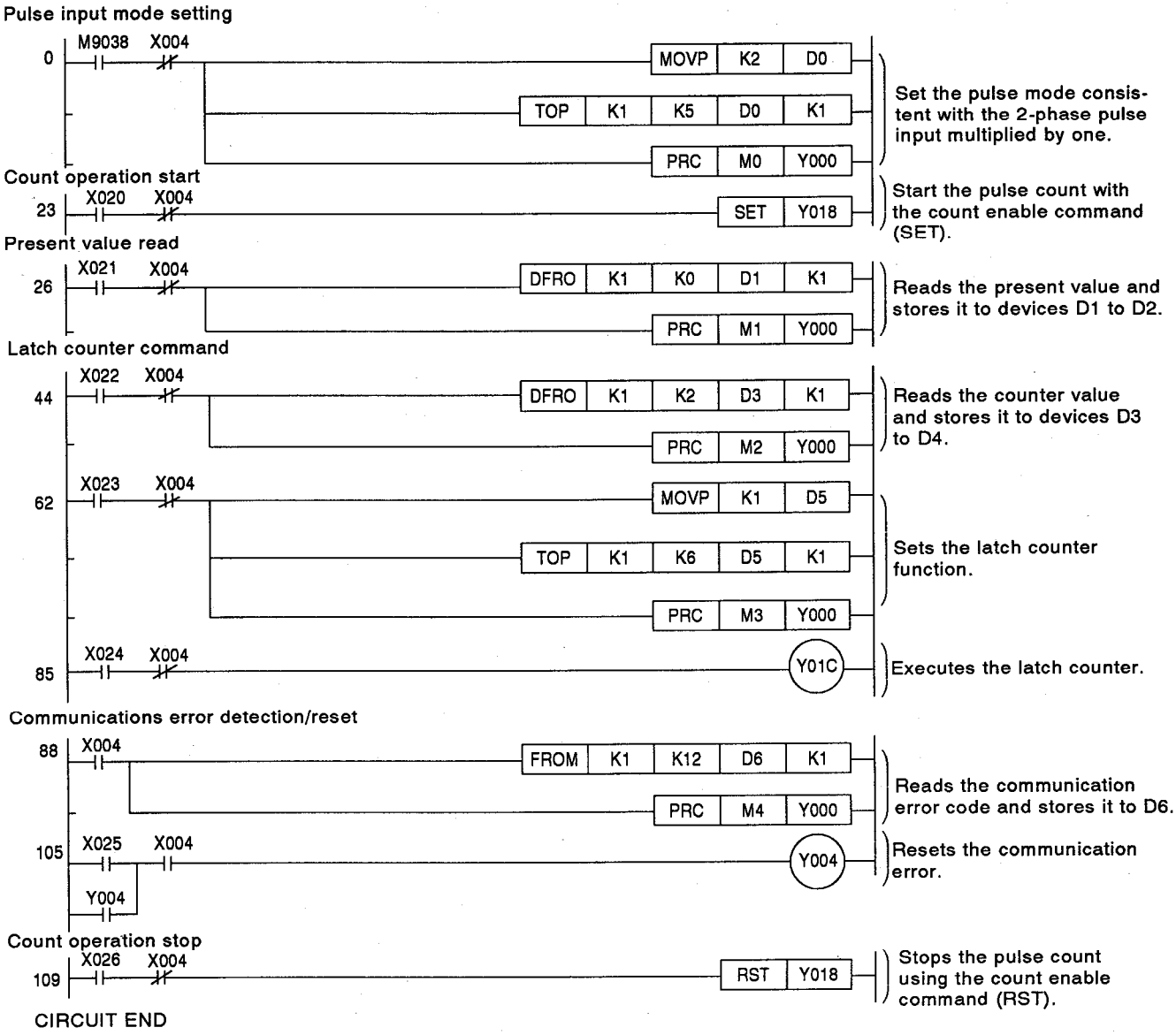
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Count operation start command ..... X20
(c) Present value read command ..... X21
(d) Counter function value read command ..... X22
(e) Counter function setting command ..... X23
(f) Latch counter command ..... X24
(g) Communication error reset command ..... X25
(h) Count operation stop command ..... X26

(2) Relationship between the data register (D0 to D6) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Set the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
SET Y018
Start the pulse count with the count enable command (SET).
Present value read
26
X021
X004
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Latch counter command
44
X022
X004
DFRO K1 K2 D3 K1
PRC M2 Y000
Reads the counter value and stores it to devices D3 to D4.
62
X023
X004
MOVP K1 D5
TOP K1 K6 D5 K1
PRC M3 Y000
Sets the latch counter function.
85
X024
X004
Y01C
Executes the latch counter.
Communications error detection/reset
88
X004
FROM K1 K12 D6 K1
PRC M4 Y000
Reads the communication error code and stores it to D6.
105
X025
X004
Y004
Y004
Resets the communication error.
Count operation stop
109
X026
X004
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.5 Sampling counter function programming example

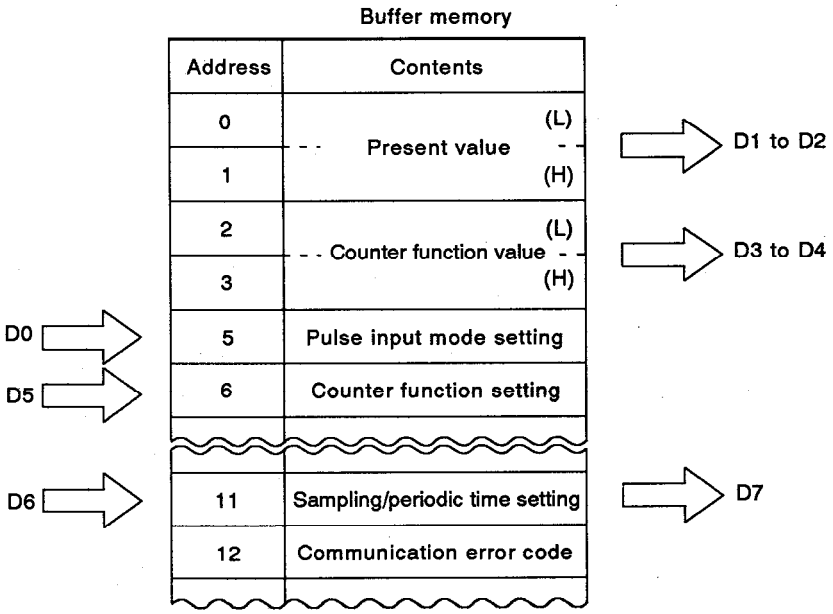
Create a program to count 2-phase pulses multiplied by one and to execute the sampling counter.

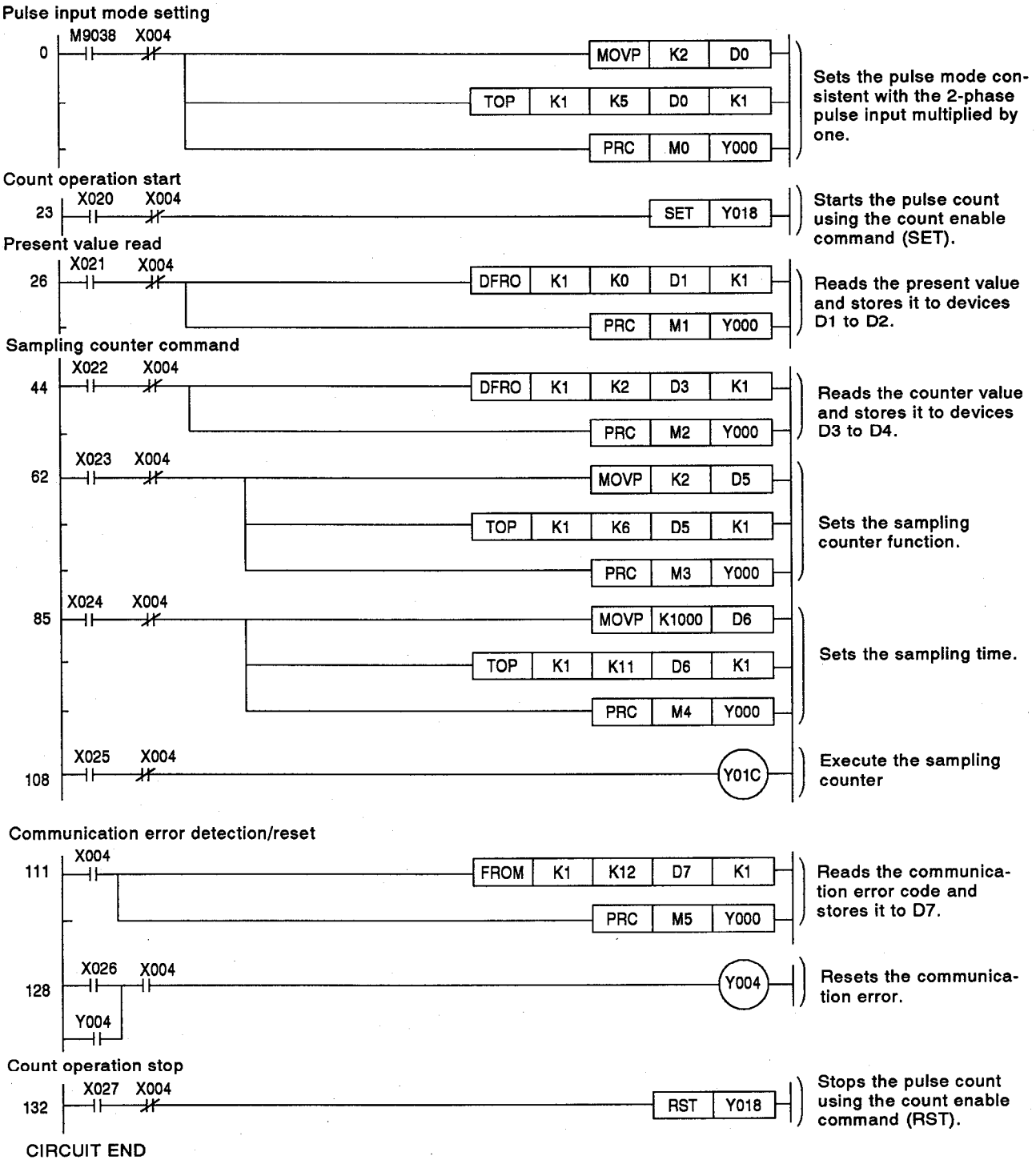
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Count operation start command.....X20
(c) Present value read command.....X21
(d) Counter function value read command.....X22
(e) Counter function setting command.....X23
(f) Sampling time setting command.....X24
(g) Sampling counter command:.....X25
(h) Communication error reset command:.....X26
(i) Count operation stop command:.....X27

(2) Relationship between the data register (D0 to D7) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
26
X021
X004
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Sampling counter command
44
X022
X004
DFRO K1 K2 D3 K1
PRC M2 Y000
Reads the counter value and stores it to devices D3 to D4.
62
X023
X004
MOVP K2 D5
TOP K1 K6 D5 K1
PRC M3 Y000
Sets the sampling counter function.
85
X024
X004
MOVP K1000 D6
TOP K1 K11 D6 K1
PRC M4 Y000
Sets the sampling time.
108
X025
X004
Y01C
Execute the sampling counter
Communication error detection/reset
111
X004
FROM K1 K12 D7 K1
PRC M5 Y000
Reads the communication error code and stores it to D7.
128
X026
X004
Y004
Y004
Resets the communication error.
Count operation stop
132
X027
X004
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.6 Periodic pulse counter function programming example

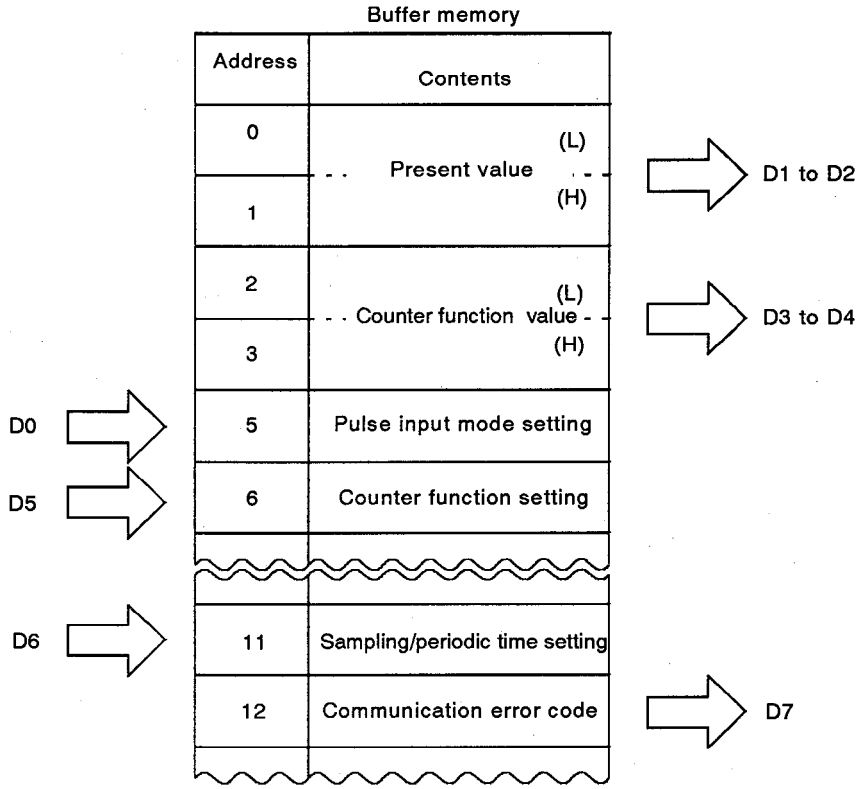
Create a program to count 2-phase pulses multiplied by one and to execute the periodic pulse counter function.

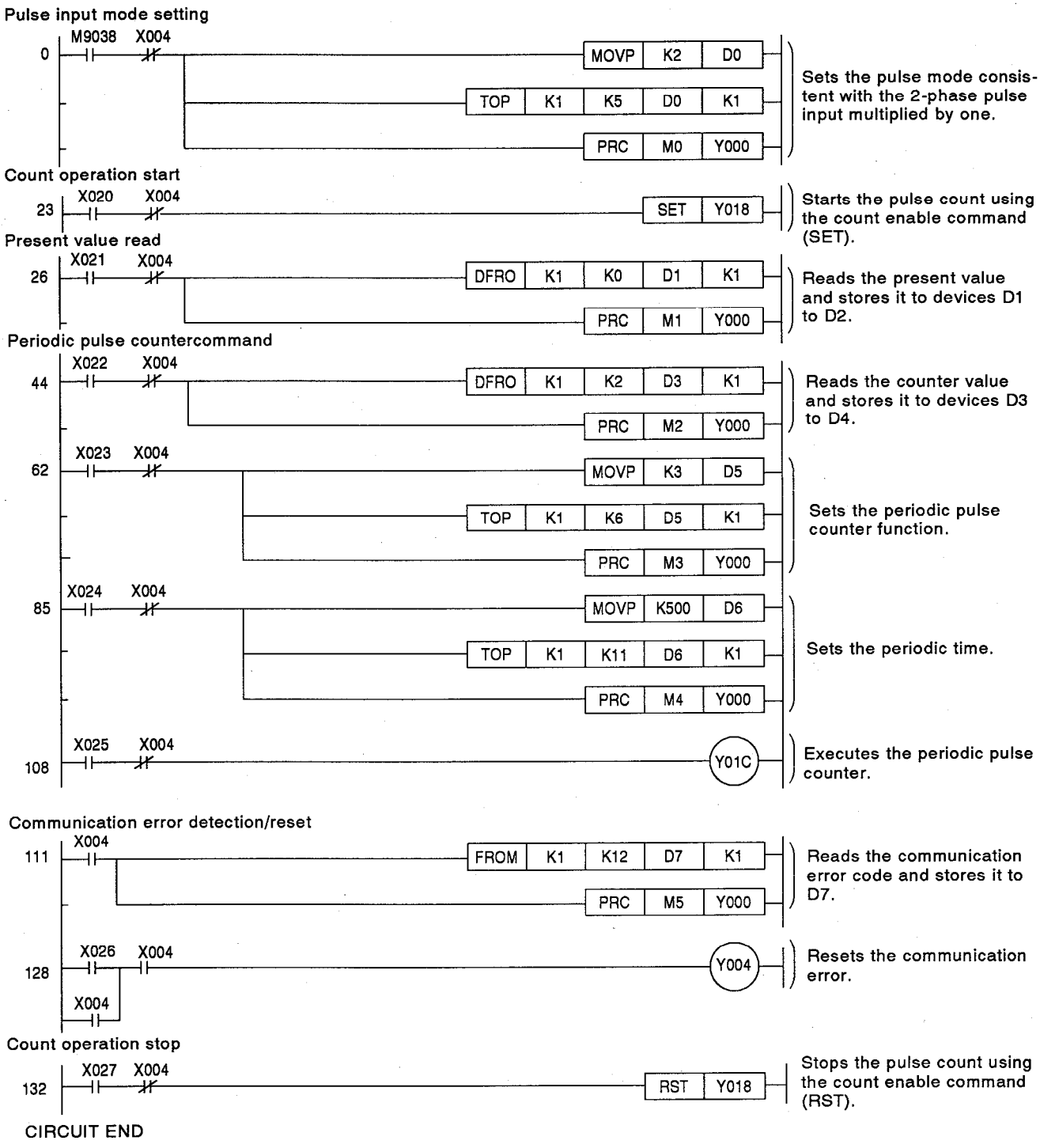
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Count operation start command ..... X20
(c) Present value read command ..... X21
(d) Counter function value read command ..... X22
(e) Counter function setting command ..... X23
(f) Periodic time setting command ..... X24
(g) Periodic pulse counter command ..... X25
(h) Communication error reset command ..... X26
(i) Count operation stop command ..... X27

(2) Relationship between the data register (D0 to D7) and the buffer memory




Pulse input mode setting
0
M9038
X004
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
23
X020
X004
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
26
X021
X004
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Periodic pulse countercommand
44
X022
X004
DFRO K1 K2 D3 K1
PRC M2 Y000
Reads the counter value and stores it to devices D3 to D4.
62
X023
X004
MOVP K3 D5
TOP K1 K6 D5 K1
PRC M3 Y000
Sets the periodic pulse counter function.
85
X024
X004
MOVP K500 D6
TOP K1 K11 D6 K1
PRC M4 Y000
Sets the periodic time.
108
X025
X004
Y01C
Executes the periodic pulse counter.
Communication error detection/reset
111
X004
FROM K1 K12 D7 K1
PRC M5 Y000
Reads the communication error code and stores it to D7.
128
X026
X004
X004
Y004
Resets the communication error.
Count operation stop
132
X027
X004
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 5.5.7 Count disable function programming example

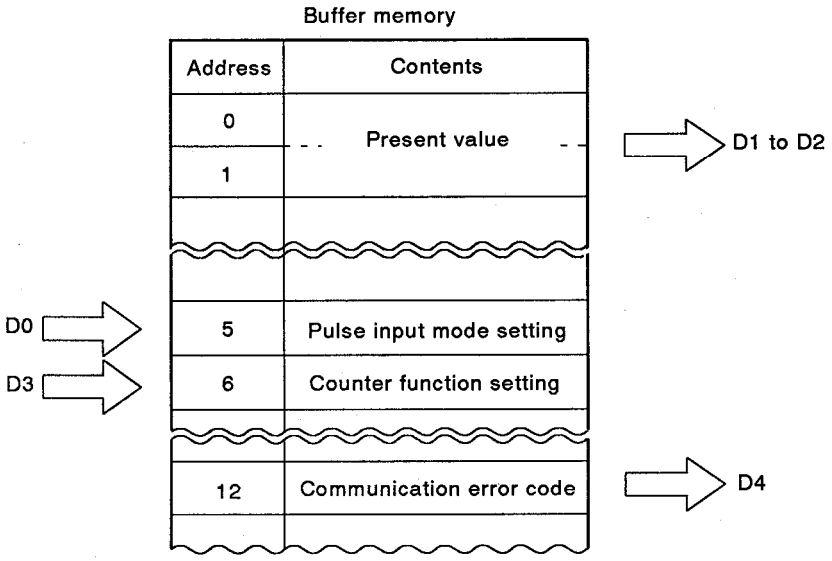
Create a program to count 2-phase pulses multiplied by one and to execute the count disable function.

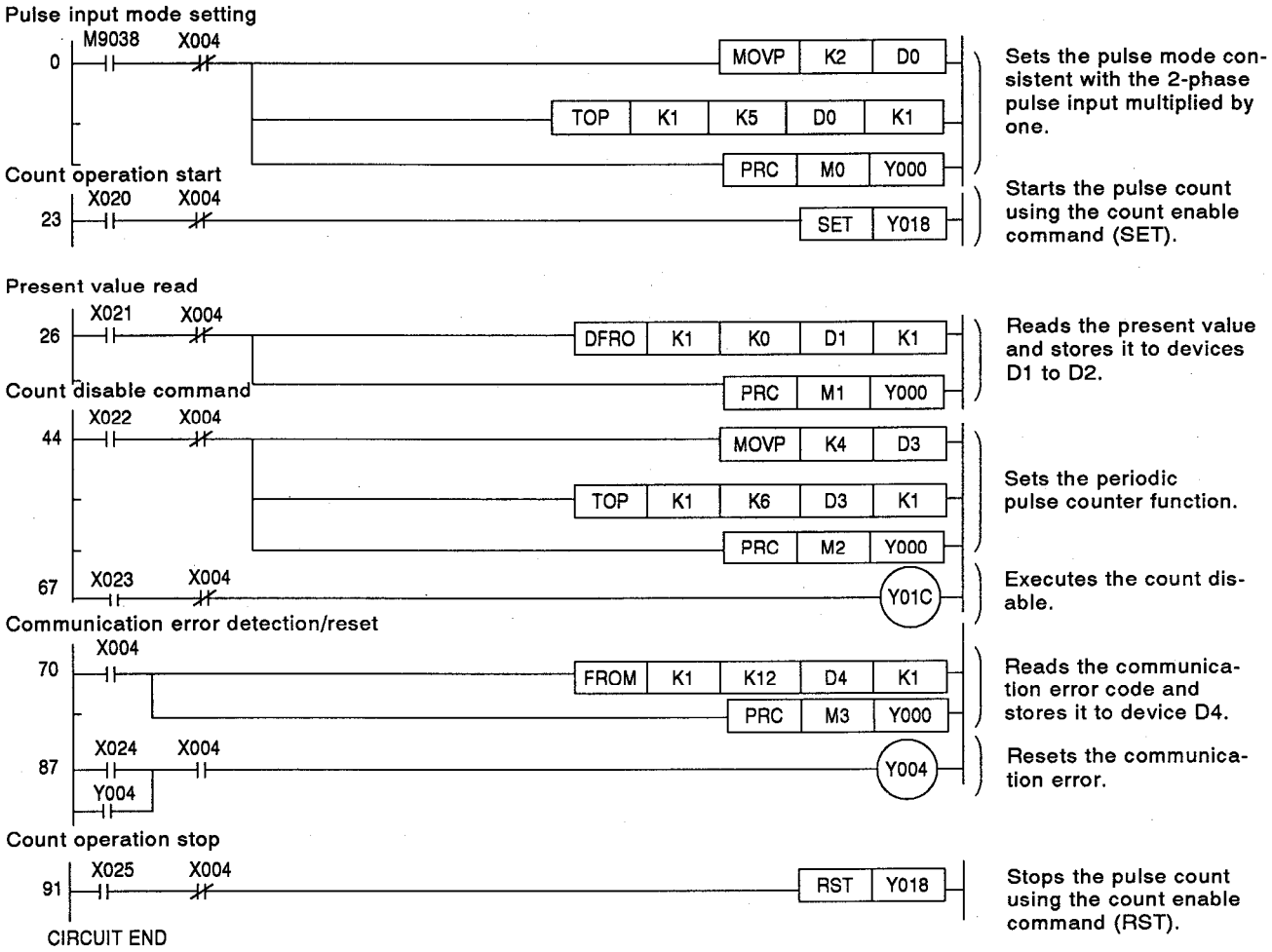
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Count operation start command.....X20
(c) Present value read command.....X21
(d) Count disable start command.....X22
(e) Count disable stop command.....X23
(f) Communication error reset command.....X24
(g) Count operation stop command.....X25

(2) Relationship between the data register (D0 to D4) and the buffer memory




Pulse input mode setting
M9038
X004
0
MOVP K2 D0
TOP K1 K5 D0 K1
PRC M0 Y000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
X020
X004
23
SET Y018
Starts the pulse count using the count enable command (SET).
Present value read
X021
X004
26
DFRO K1 K0 D1 K1
PRC M1 Y000
Reads the present value and stores it to devices D1 to D2.
Count disable command
X022
X004
44
MOVP K4 D3
TOP K1 K6 D3 K1
PRC M2 Y000
Sets the periodic pulse counter function.
67
X023
X004
Y01C
Executes the count disable.
Communication error detection/reset
X004
70
FROM K1 K12 D4 K1
PRC M3 Y000
Reads the communication error code and stores it to device D4.
X024
X004
87
Y004
Y004
Resets the communication error.
Count operation stop
X025
X004
91
RST Y018
Stops the pulse count using the count enable command (RST).
CIRCUIT END

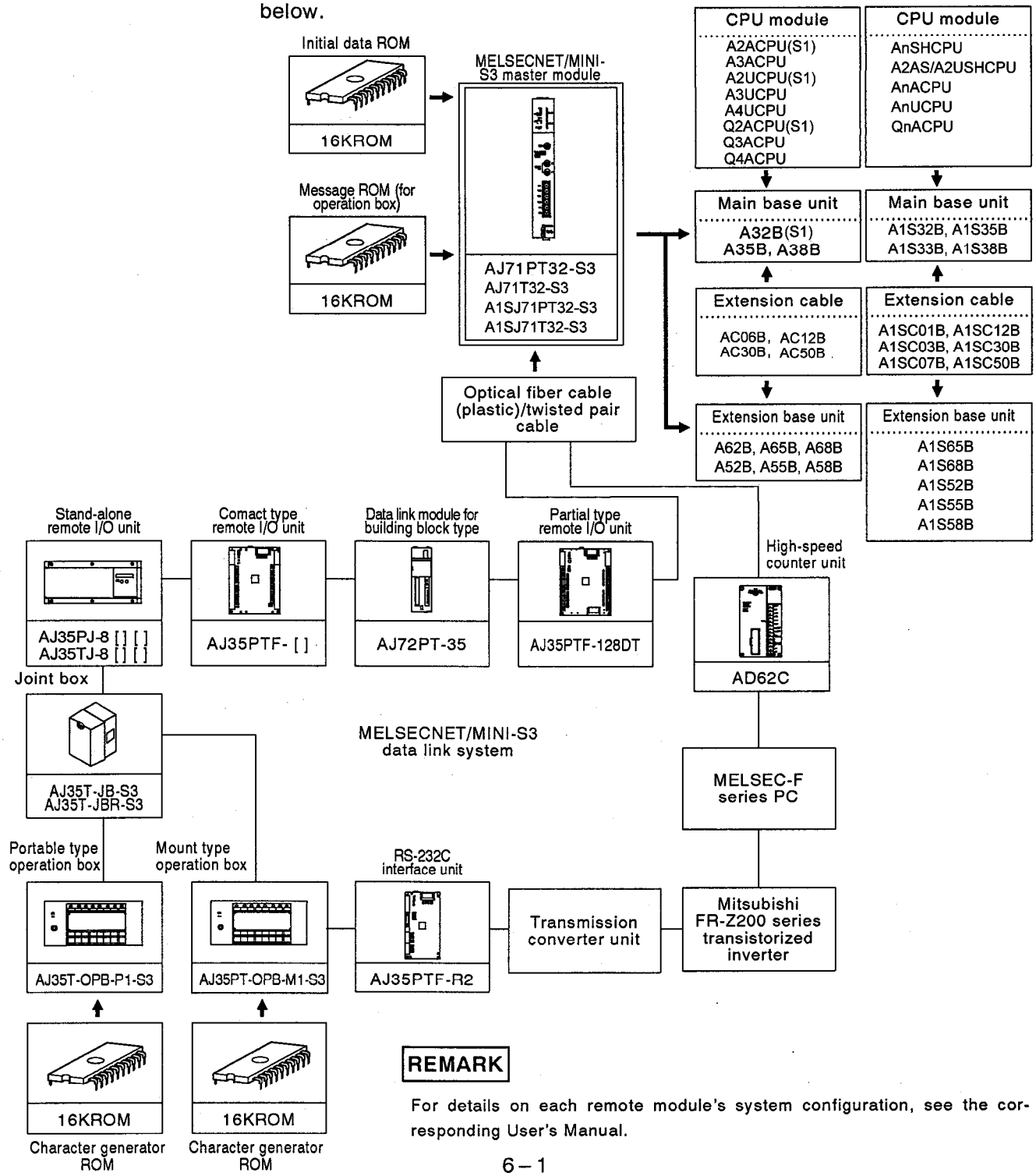
# 6. AnSH/A2AS/A2USH/Q2AS(H)/AnA/AnU/QnACPU AND A1S/AJ71PT32-S3 LINK

- When this link is executed, software Package "SW4GP-GPPA (for A6GPP or A6PHP) or "SW0IX-GPPAE (for IBM PC/AT)" are required.
- Since the MELSECNET/MINI-S3 automatic refresh setting cannot be used when software Package "SW3GP-GPPA" is used, follow the programming method described in Section 7 or use after correcting only I/O signal processing according to Section 7.

## 6.1 System Configuration

### 6.1.1 Overall configuration

The overall configuration of the AD62C using MELSECNET/MINI-S3 is shown below.




**REMARK**

For details on each remote module's system configuration, see the corresponding User's Manual.

### 6.1.2 Applicable systems

The AD62C can be linked to the following CPUs via the AJ71PT32-S3 master module.

| | | | |
|---|---|---|---|
| Applicable models | A1SHCPU<br>A2SHCPU<br>A2ACPU (P21/R21)<br>A2ACPU (P21/R21)-S1<br>A3ACPU (P21/R21)<br>A2ASCPU<br>A2USHCPU | A2UCPU<br>A2UCPU-S1<br>A3UCPU<br>A4UCPU | Q2AS(H)CPU<br>Q2AS(H)CPU-S1<br>Q2ACPU<br>Q2ACPU-S1<br>Q3ACPU<br>Q4ACPU |

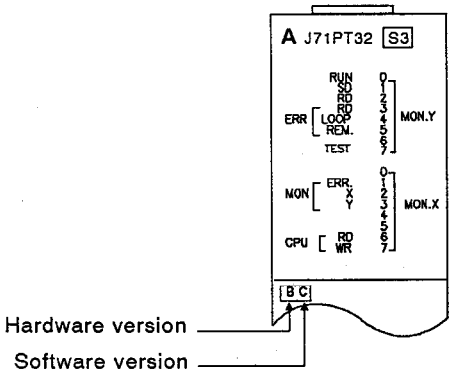
The AJ71PT32-S3 master module can be loaded into any slot and linked with the AD62C with the exception of (1) and (2) below. The number of device panels is unlimited.

(1) If the AD62C is loaded into an extension base unit (A55B, A58B) without a power supply module, the power capacity may be insufficient. Avoid loading as long as possible. If it is necessary to load, select power supply modules and extension cables with the power capacity of the main base unit's power supply module and extension cable voltage drops in mind. For details, see each CPU User's Manual.

(2) In a MELSECNET data link system, loading is possible to both a master station and a local station.

### 6.1.3 Precautions when constructing the system

(1) The software version shown below on the front of the A1S/AJ71PT32-S3 module must be "C" or later to use the AD62C. A module of software version "A, B" or "no" software version indication cannot be used.




(2) When using the AD62C in the MELSECNET/MINI-S3 data link system, use twisted pair cables.

(3) Since each AD62C occupies 4 stations (a total of 32 I/O points), be careful when assigning I/O signals.

(4) When using the AD62C, set the A1S/AJ71PT32-S3 as follows.

(a) Set the "jumper for mode selection" of the A1S/AJ71PT32-S3 to the extension mode (occupying 48 I/O points) of "48."

(b) Create the initial data ROM for the A1S/AJ71PT32-S3 extension mode (occupying 48 I/O points) by the SW0GP-MINIP and install it. For remote terminal data setting at the creation of the initial ROM, set the AD62C protocol to

4:MINI STANDARD PROTOCOL.

(c) For details, see each of the manuals below.

- MELSECNET/MINI-S3 master module type AJ71T32-S3, A1SJ71PT32-S3, A1SJ71T32-S3 User's Manual
- SW0GP-MINIP Operating Manual

(5) The AD62C requires a 24 VDC power supply.

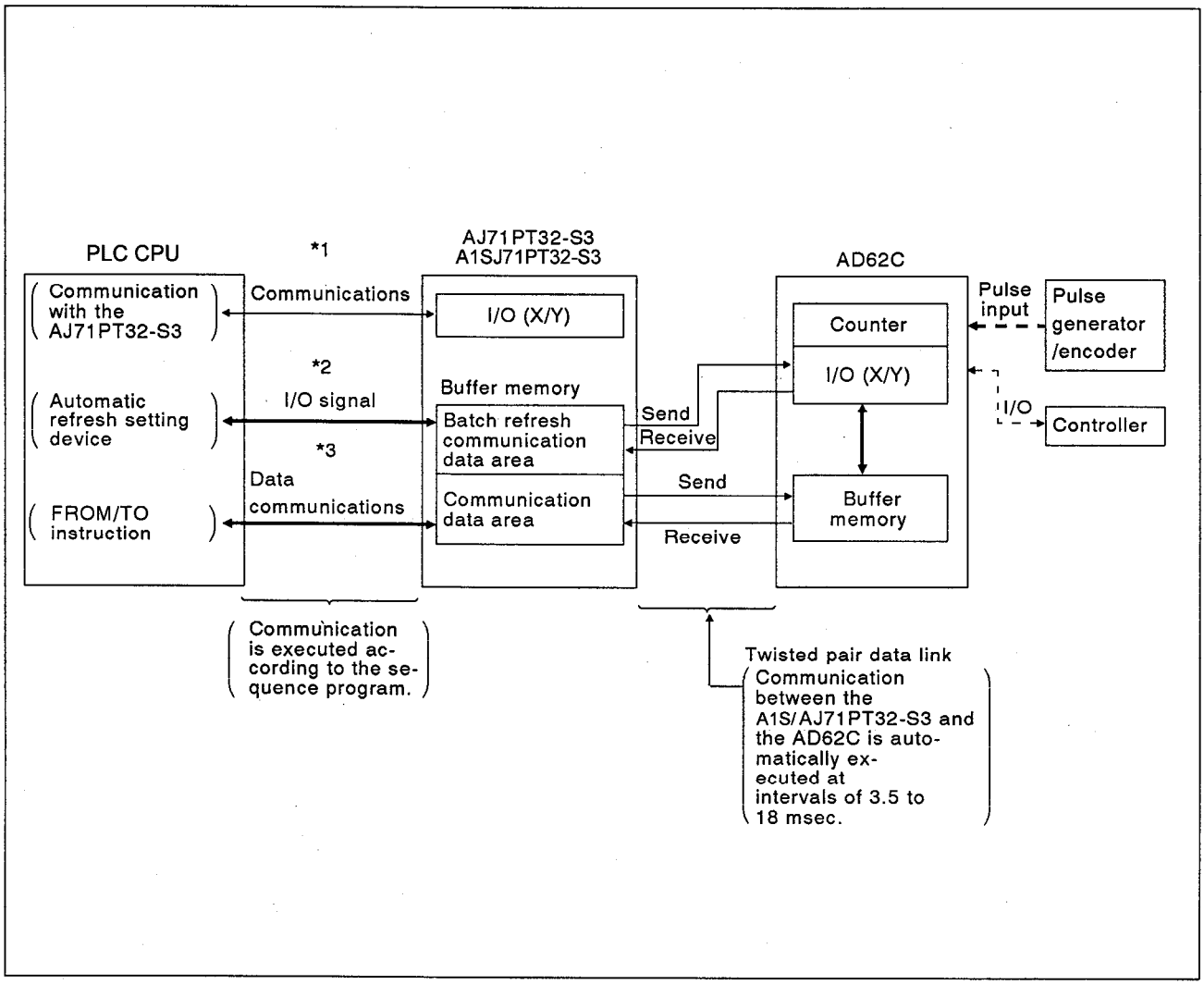
When supplying power from one power supply to multiple AD62Cs or to the link I/O modules, select cables and perform wiring taking voltage drops into consideration.

To calculate the receiving port voltage, see **[REMARK]** in Section 5.1.2.

## 6.2 Data Communication Processing

### 6.2.1 Communication method

(1) Communication between the AD62C and the AnSH/A2AS/A2USH/Q2AS(H)/AnA/AnU/QnACPU is executed via the A1S/ AJ71PT32-S3' buffer memory. The communication method is shown below.




*1: I/O signal communication between the PLC CPU and the A1S/AJ71PT32-S3 is executed. (I/O communication processing of communication start, error detection, etc.)

*2: Input signal communication between the PLC CPU and the A1S/AJ71PT32-S3, and between the A1S/AJ71PT32-S3 and the AD62C is executed. For details, see "I/O signal processing" in Section 6.2.2.

*3: Data communication between the PLC CPU and the A1S/AJ71PT32-S3, and between the A1S/AJ71PT32-S3 and the AD62C is executed. For details, see "buffer memory data processing" in Section 6.2.3.

### 6.2.2 I/O signal processing

I/O signals (X,Y) of the AD62C to PC CPU are processed via the A1S/AJ71PT32-S3 buffer memory.

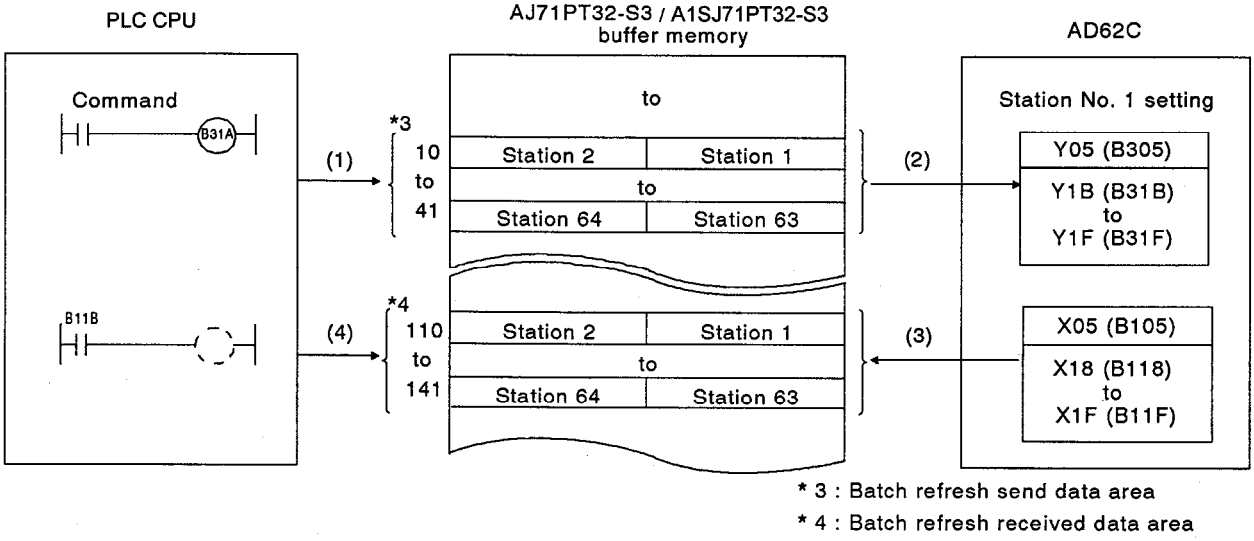
MELSECNET/MINI automatic refresh should be set by parameter settings of the SW4GP-GPPA or SW0IX-GPPAE software package and entered to the PLC CPU in advance.

By using the sequence program to turn ON/OFF the device numbers for which automatic refresh is set, AD62C I/O signals corresponding to the device number can be turned ON/OFF without acknowledging the A1S/AJ71PT32-S3 batch refresh send/receive buffer memory.

(1) The I/O signal processing method between the PLC CPU and the AD62C is shown below.

- The AD62C station number is set to 01. (X00 to X1F, Y00 to Y1F)
- The automatic refresh communication device of PLC CPU parameters is set to *1 B100 to B2FF (equivalent to input X) and *2 B300 to B4FF (equivalent to output Y).

*1 : B100 to B2FF ... 512 points (64 stations x 8 points)
*2 : B300 to B4FF ... 512 points (64 stations x 8 points)




* 3 : Batch refresh send data area
* 4 : Batch refresh received data area

(a) Output (Y) signal (communication order from (1) to (2))

- By using the sequence program, the PLC CPU turns ON/OFF the device equivalent to the AD62C output (Y) assigned by the automatic refresh setting and writes it to the A1S/AJ71PT32-S3 batch refresh send data area.
- The A1S/AJ71PT32-S3 writes the send data to the AD62C output signal area.

(b) Input (X) signal (communication order from (3) to (4))

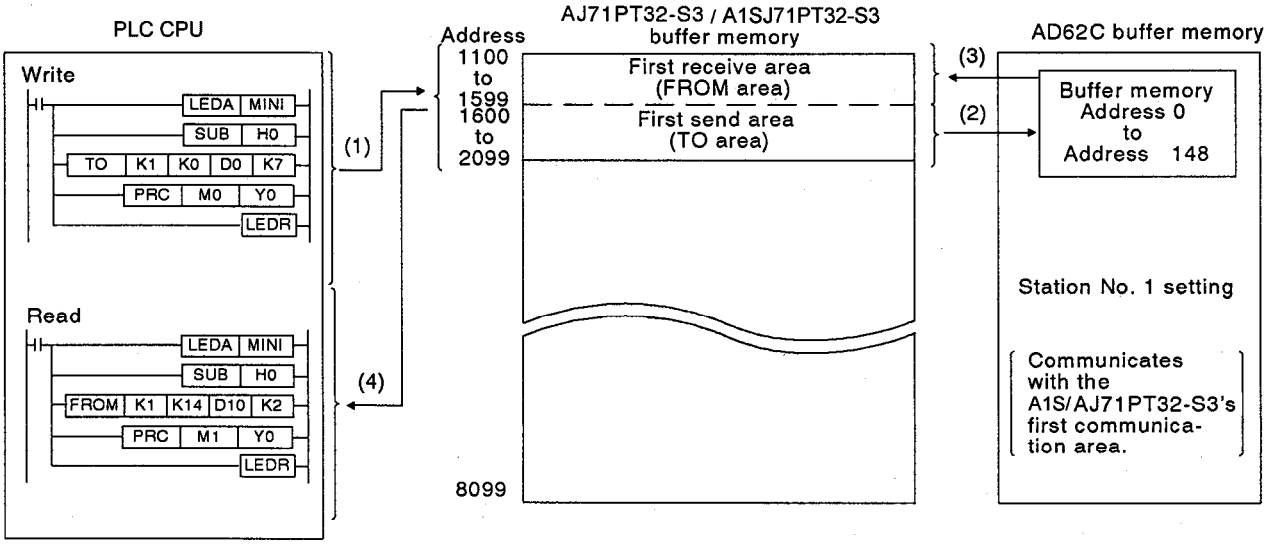
- The A1S/AJ71PT32-S3 always communicates with the AD62C and stores the AD62C input signal data in the batch refresh received data area.
- By using the sequence program, the PLC CPU reads the ON/OFF data of the device equivalent to the AD62C input (X) assigned by the automatic refresh setting from the A1S/AJ71PT32-S3 batch refresh received data area at every END processing, then turns the device ON/OFF.

### 6.2.3 Buffer memory data processing

The AD62C buffer memory data is processed via the A1S/ AJ71PT32-S3 buffer memory. However, by using the AnACPU dedicated read/write instructions, the AD62C buffer memory address can be specified directly to execute the TO/FROM instruction without acknowledging the A1S/AJ71PT32-S3 buffer memory address specification.

(1) The PLC CPU and AD62C buffer memory data processing method is shown below.

- The AD62C station number is set to 01.
- The A1S/AJ71PT32-S3 is loaded to slot 0. (head I/O No. ... H0)
- The AD62C is set to the first communication area of the remote terminal unit by the A1S/AJ71PT32-S3 initial ROM.




(a) Write to the AD62C buffer memory (communication order from (1) to (2))

- By using the sequence program dedicated write instruction, the PLC CPU writes to the AJ71PT32-S3 send area. The A1S/AJ71PT32- S3 writes to the AD62C buffer memory.
- At the completion of write, the PRC instruction execution-completed signal (M0) stays ON for 1 scan.

(b) Read from the AD62C buffer memory (communication order from (3) to (4))

- By using the sequence program dedicated read instruction, a read request is executed to the A1S/AJ71PT32-S3.
- The A1S/ AJ71PT32-S3 reads the data in AD62C buffer memory and stores it in the receive area.
- The PLC CPU reads the received data stored in the A1S/AJ71PT32-S3.
- At the completion of the read, the PRC instruction execution-completed signal (M1) stays ON for 1 scan.

### 6.2.4 Processing time

The processing time required to write data to and read data from the AD62C buffer memory is shown below.

| Items | Max. Processing Time |
|---|---|
| Data write | [t msec x (number of data words)] + *2 [(t msec x 5) + 80 msec] |
| Data read | *2: Total value of the AD62C internal processing time and the PC CPU processing time |

"t" is the I/O refresh time. It varies according to the number and type of connected remote module stations. Calculation of the I/O refresh time is shown below.

| Mode | Operation Mode Settings | I/O Refresh Time (msec) |
|---|---|---|
| Extension mode (48 points) | Automatic return enable (0) | t = 0.66 + (0.044 x R) + (0.25 x B) + (0.95 x T) |
| | Automatic return disable (1) | t = 0.54 + (0.058 x R) + (0.25 x B) + (0.95 x T) |
| | Communication stop at error detection | t = 0.54 + (0.051 x R) + (0.25 x B) + (0.95 x T) |

R : Total number of remote stations
B : Number of AJ35PTF-128DTs
T : Number of remote terminal units

## 6.3 I/O Signals To/From PLC CPU

### 6.3.1 AD62C I/O signals

AD62C I/O signals to/from PLC CPU are shown below. The following I/O device numbers apply when the AD62C's station number is 01 (X/Y00 to X/Y1F).

(1) Input signals (signal direction: AD62C → PLC CPU)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| X00 to X04 | (Unusable) | ———— |
| X05 | Reset status detection | • Latched to ON when power to the AD62C is turned ON or the reset switch is turned ON.<br>• Switches OFF when the reset status detection reset signal (Y05) switches from OFF to ON. |
| X06 to X1A | (Unusable) | ———— |
| X1B | Fuse blown detection | • Switches ON when a fuse is blown or when external power for the limit switch output is turned OFF. |
| X1C | Sampling/periodic counter ON/OFF flag | • Switches ON when the sampling/periodic counter function is executed. |
| X1D | Limit switch output READY flag | • Set when limit switch output is enabled.<br>• Reset when the dog setting has an error. |
| X1E | External preset request detection | • Latched to ON when an external preset request is given.<br>• Switches OFF when the external preset request detection signal reset command (Y1E) switches from OFF to ON. |
| X1F | Multiple-dog setting error detection | • Latched to ON when a multiple-dog setting error is detected in the AD62C.<br>• Switches OFF when the multiple-dog setting error detection reset command (Y1F) switches from OFF to ON. |

(2) Output signals (signal direction: PLC CPU → AD62C)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| Y00 to Y04 | (Unusable) | ———— |
| Y05 | Reset status detection reset | • When this signal switches from OFF to ON, the reset status detection signal (X05) switches OFF.<br>• Switches OFF when (X05) switches OFF. |
| Y06 to Y17 | (Unusable) | ———— |
| Y18 | Count enable command | • Enables counting operations of the AD62C when switched ON. |
| Y19 | Decremental count command | • Valid only in the direction input mode and when a 1-phase pulse is input.<br>• Counts decrementally when this signal is ON.<br>• Cannot be used along with an external input (øB). |
| Y1A | Preset command | • Executes preset operations. |
| Y1B | Ring counter command | • Starts the ring counter. |
| Y1C | Counter function selection start command | • Selects the counter function. |
| Y1D | Limit switch output enable command | • Enables limit switch output (8 channels in batch).<br>• When (Y1D) is OFF, this command is not output and all channels are OFF. |
| Y1E | External preset command detection reset command | • When this signal switches from OFF to ON, the external preset request detection flag (X1E) switches OFF.<br>• Switches OFF when (X1E) switches OFF. |
| Y1F | Multiple-dog setting error detection reset | • When this signal switches from OFF to ON, the multiple-dog setting error detection signal (X1F) switches OFF and the error codes of the AD62C buffer memory are reset.<br>• Switches OFF after (X1F) switches OFF. |

### 6.3.2 A1S/ AJ71PT32-S3 I/O signals

I/O signals between the A1S/ AJ71PT32-S3 and the PLC CPU in the extension mode are used when accessing the AD62C buffer memory.

For details about the I/O signals, see the MELSECNET/MINI-S3 Master Module User's Manual.

The list of I/O signals in the extension mode is shown below.

The "n" in the Device No. column of the table is the master module head I/O number. It is determined by the number of I/O points of the I/O modules loaded into the master module's front slot and by the master module's position.

( Example: When the master module head I/O number is "X/Y20"
X (n+0) to X (n+2F) = X20 to X4F
Y (n+0) to Y (n+2F) = Y20 to Y4F )

**Table 6.1 I/O Signal List in the Extension Mode**

| Device Nos. | Signals | | Device Nos. | Signals | |
|---|---|---|---|---|---|
| X(n+0) | Send-completed signal | For remote terminal unit No.1 | Y(n+0) | Send-completed signal | For remote terminal unit No.1 |
| X(n+1) | Read request signal | | Y(n+1) | Read request signal | |
| X(n+2) | Send-completed signal | For remote terminal unit No.2 | Y(n+2) | Send-completed signal | For remote terminal unit No.2 |
| X(n+3) | Read request signal | | Y(n+3) | Read request signal | |
| X(n+4) | Send-completed signal | For remote terminal unit No.3 | Y(n+4) | Send-completed signal | For remote terminal unit No.3 |
| X(n+5) | Read request signal | | Y(n+5) | Read request signal | |
| X(n+6) | Send-completed signal | For remote terminal unit No.4 | Y(n+6) | Send-completed signal | For remote terminal unit No.4 |
| X(n+7) | Read request signal | | Y(n+7) | Read request signa | |
| X(n+8) | Send-completed signal | For remote terminal unit No.5 | Y(n+8) | Send-completed signal | For remote terminal unit No.5 |
| X(n+9) | Read request signal | | Y(n+9) | Read request signal | |
| X(n+A) | Send-completed signal | For remote terminal unit No.6 | Y(n+A) | Send-completed signal | For remote terminal unit No.6 |
| X(n+B) | Read request signal | | Y(n+B) | Read request signal | |
| X(n+C) | Send-completed signal | For remote terminal unit No.7 | Y(n+C) | Send-completed signal | For remote terminal unit No.7 |
| X(n+D) | Read request signal | | Y(n+D) | Read request signal | |
| X(n+E) | Send-completed signal | For remote terminal unit No.8 | Y(n+E) | Send-completed signal | For remote terminal unit No.8 |
| X(n+F) | Read request signal | | Y(n+F) | Read request signal | |
| X(n+10) | Send-completed signal | For remote terminal unit No.9 | Y(n+10) | Send-completed signal | For remote terminal unit No.9 |
| X(n+11) | Read request signal | | Y(n+11) | Read request signal | |
| X(n+12) | Send-completed signal | For remote terminal unit No.10 | Y(n+12) | Send-completed signal | For remote terminal unit No.10 |
| X(n+13) | Read request signal | | Y(n+13) | Read request signal | |
| X(n+14) | Send-completed signal | For remote terminal unit No.11 | Y(n+14) | Send-completed signal | For remote terminal unit No.11 |
| X(n+15) | Read request signal | | Y(n+15) | Read request signal | |
| X(n+16) | Send-completed signal | For remote terminal unit No.12 | Y(n+16) | Send-completed signal | For remote terminal unit No.12 |
| X(n+17) | Read request signal | | Y(n+17) | Read request signal | |
| X(n+18) | Send-completed signal | For remote terminal unit No.13 | Y(n+18) | Send-completed signal | For remote terminal unit No.13 |
| X(n+19) | Read request signal | | Y(n+19) | Read request signal | |
| X(n+1A) | Send-completed signal | For remote terminal unit No.14 | Y(n+1A) | Send-completed signal | For remote terminal unit No.14 |
| X(n+1B) | Read request signal | | Y(n+1B) | Read request signal | |
| X(n+1C) | (Unusable) | | Y(n+1C) | (Unusable) | |
| X(n+1D) | | | Y(n+1D) | | |
| X(n+1E) | | | Y(n+1E) | | |
| X(n+1F) | | | Y(n+1F) | | |
| X(n+20) | Hardware fault | | Y(n+20) | | |
| X(n+21) | MINI-S3 link communications in progress | | Y(n+21) | | |
| X(n+22) | (Unusable) | | Y(n+22) | | |
| X(n+23) | Received data clear complete (for the AJ35PTF-R2) | | Y(n+23) | Received data clear request (for the AJ35PTF-R2) | |
| X(n+24) | Remote terminal unit error detection | | Y(n+24) | Remote terminal unit error detection reset | |
| X(n+25) | Test mode | | Y(n+25) | (Unusable) | |
| X(n+26) | MINI-S3 link error detection | | Y(n+26) | | |
| X(n+27) | MINI-S3 link communication error | | Y(n+27) | | |
| X(n+28) | ROM error | | Y(n+28) | MINI-S3 link communication start | |
| X(n+29) | (Unusable) | | Y(n+29) | (Unusable) | |
| X(n+2A) | | | Y(n+2A) | FROM/TO instruction response specification | |
| X(n+2B) | | | Y(n+2B) | Error station data clear specification | |
| X(n+2C) | | | Y(n+2C) | Buffer memory channel switching | |
| X(n+2D) | | | Y(n+2D) | Error reset | |
| X(n+2E) | | | Y(n+2E) | (Unusable) | |
| X(n+2F) | | | Y(n+2F) | | |

## 6.4 Buffer Memory Assignments

### 6.4.1 AD62C buffer memory

Table 6.2 shows the buffer memory assignments of the AD62C.

The next page gives detailed information about the settings of buffer memory addresses 14 to 149.

Initial values are set in the buffer memory when power to the AD62C is turned ON or when the AD62C is reset.

The contents of the buffer memory can be read/written using a FROM/TO instruction in an AD62C sequence program.

**Table 6.2 Buffer Memory Assignments**

| Addresses | Setting Contents | Initial Values | Read/write | Reference Sections |
|---|---|---|---|---|
| 0 | Present value (L) | 0 | Read only | 4.3.1 |
| 1 | Present value (H) | | | |
| 2 | Counter function selection count value (L) | 0 | | 3.5.1 |
| 3 | Counter function selection count value (H) | | | |
| 4 | Limit switch output state flag (CH 1 to CH 8) | 0 | | 3.4 |
| 5 | Pulse input mode setting | 0 | Read/write possible | 4 |
| 6 | Counter function selection setting | 0 | | 3.5 |
| 7 | Preset value setting (L) | 0 | | 3.2 |
| 8 | Preset value setting (H) | | | |
| 9 | Ring counter value setting (L) | 1024 | | 3.3 |
| 10 | Ring counter value setting (H) | | | |
| 11 | Sampling/periodic time setting | 1 | | 3.5.4 and 3.5.5 |
| 12 | Communication error code | 0 | | 9.1 |
| 13 | Multiple-dog setting error code | 0 | | |
| 14 to 30 | CH 1 limit switch output data setting | 0 | Read/write possible | 3.4 |
| 31 to 47 | CH 2 limit switch output data setting | 0 | | |
| 48 to 64 | CH 3 limit switch output data setting | 0 | | |
| 65 to 81 | CH 4 limit switch output data setting | 0 | | |
| 82 to 98 | CH 5 limit switch output data setting | 0 | | |
| 99 to 115 | CH 6 limit switch output data setting | 0 | | |
| 116 to 132 | CH 7 limit switch output data setting | 0 | | |
| 133 to 149 | CH 8 limit switch output data setting | 0 | | |

The following gives detailed information about the settings of buffer memory addresses 14 to 149 (limit switch output data setting of CH 1 to CH 8)

| Setting Contents | | Buffer Memory Addresses | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 14 to 30 CH.1 | 31 to 47 CH.2 | 48 to 64 CH.3 | 65 to 81 CH.4 | 82 to 98 CH.5 | 99 to 115 CH.6 | 116 to 132 CH.7 | 133 to 149 CH.8 |
| Number of multiple dogs for CH [ ] | | 14 | 31 | 48 | 65 | 82 | 99 | 116 | 133 |
| ··· CH [ ] Dog 0 ON address | (L) | 15 | 32 | 49 | 66 | 83 | 100 | 117 | 134 |
| | (H) | 16 | 33 | 50 | 67 | 84 | 101 | 118 | 135 |
| ··· CH [ ] Dog 0 OFF address | (L) | 17 | 34 | 51 | 68 | 85 | 102 | 119 | 136 |
| | (H) | 18 | 35 | 52 | 69 | 86 | 103 | 120 | 137 |
| ··· CH [ ] Dog 1 ON address | (L) | 19 | 36 | 53 | 70 | 87 | 104 | 121 | 138 |
| | (H) | 20 | 37 | 54 | 71 | 88 | 105 | 122 | 139 |
| ··· CH [ ] Dog 1 OFF address | (L) | 21 | 38 | 55 | 72 | 89 | 106 | 123 | 140 |
| | (H) | 22 | 39 | 56 | 73 | 90 | 107 | 124 | 141 |
| ··· CH [ ] Dog 2 ON address | (L) | 23 | 40 | 57 | 74 | 91 | 108 | 125 | 142 |
| | (H) | 24 | 41 | 58 | 75 | 92 | 109 | 126 | 143 |
| ··· CH [ ] Dog 2 OFF address | (L) | 25 | 42 | 59 | 76 | 93 | 110 | 127 | 144 |
| | (H) | 26 | 43 | 60 | 77 | 94 | 111 | 128 | 145 |
| ··· CH [ ] Dog 3 ON address | (L) | 27 | 44 | 61 | 78 | 95 | 112 | 129 | 146 |
| | (H) | 28 | 45 | 62 | 79 | 96 | 113 | 130 | 147 |
| ··· CH [ ] Dog 3 OFF address | (L) | 29 | 46 | 63 | 80 | 97 | 114 | 131 | 148 |
| | (H) | 30 | 47 | 64 | 81 | 98 | 115 | 132 | 149 |

[ ] = Channel number displayed

### 6.4.2 A1S/AJ71PT32-S3 buffer memory

There are communication (send/receive) data addresses for the A1S/AJ71PT32-S3 buffer memory according to dedicated read/write instructions between the A1S/AJ71PT32-S3 and the PLC CPU.

The assignment of buffer memory addresses which automatically communicate with the AD62C is shown below.

For details of the buffer memory, see the MELSECNET/MINI-S3 Master Module User's Manual.

| | Address (decimal) | | Contents | PC CPU Read/write Enable/disable |
|---|---|---|---|---|
| | 0 | Total number of remote stations | The range of the station numbers of all connected remote modules is set. | Read/write enable |
| | 1 | Number of retries | The number of retries at communication error occurrence is set. | |
| | | (Unused) | ——— | |
| | 4 | Line error check | Used to confirm line faulty areas. | |
| | | (Unused) | ——— | |
| *1 | 10 to 41 | Batch refresh send data | Data output to the batch refresh type remote I/O module are written. | |
| | | (Unused) | ——— | ——— |
| | 70 to 77 | Remote module's card data | Each connected remote module's type is stored. | Read only |
| | | (Unused) | ——— | ——— |
| | 90 to 93 | Accumulation faulty station detection | Station numbers of remote modules which are in communication error are stored. (Detection status is retained until reset.) | Read/write enable |
| | | (Unused) | ——— | ——— |
| | 100 to 103 | Faulty station detection | Station number of remote module which is in communication error is stored. (Communication status is always updated.) | Read only |
| | | (Unused) | ——— | |
| | 107 | Communication error code | The cause of the MINI-S3 link communication error signal being ON is stored. | |
| | 108 | Error detection code | The accumulated number of times the MINI-S3 link error detection turns ON is stored. | |
| | | (Unused) | ——— | |
| *2 | 110 to 141 | Batch refresh received data | Input data from batch refresh type remote I/O module are stored. | |
| | | (Unused) | ——— | |
| | 160 | Line error retry counter | The number of executions of retry processing when communication with all remote modules is disabled by line error is stored. | |
| | 161 to 192 | Retry counter | The number of times retry processing to faulty stations is executed is stored. | |
| | | (Unused) | ——— | |
| *3 | 195 | Remote terminal unit faulty stations | The station number of the remote terminal unit with which an error has occurred is stored. | |
| | 196 to 209 | Remote terminal unit error code | The cause of the remote terminal unit error detection signal [X (n + 24)] being ON is stored. | |
| | | (Unused) | ——— | ——— |
| | 250 to 282 | Partial refresh station | Partial refresh type remote I/O module station number and specification of the number of digits are written. | Read/write enable |
| | | (Unused) | ——— | |
| | 300 to 363 | Partial refresh send data | Data output to the partial refresh type remote I/O module are written. | |
| | | (Unused) | ——— | |
| | 598 | Partial refresh accumulation input error detection | Partial refresh type remote I/O module's input data received faulty station is stored. (Detection status is retained until reset.) | |
| | 599 | Partial refresh input error detection | Partial refresh type remote I/O module's input data received faulty station is stored. (Communication status is always undated.) | |
| | 600 to 663 | Partial refresh received data | Partial refresh type remote I/O module's input data are stored. | Read only |

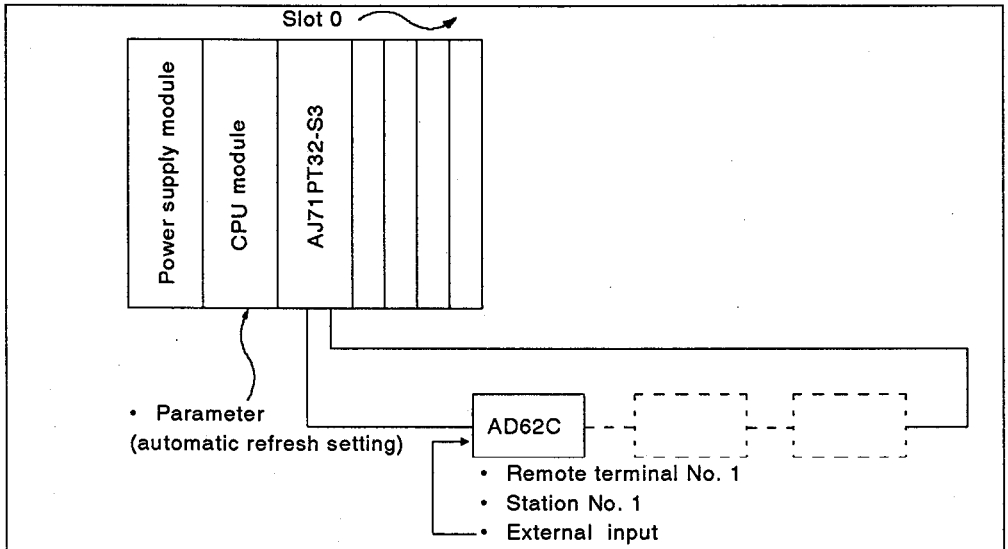
*1: Output signal data write area to the AD62C
*2: Store area of the input signal data from the AD62C
*3: Area which stores station number and error code when an AD62C error occurs. (See Section 9.1 for error codes.)

| | Address (decimal) | | | Contents | PC CPU Read/write Enable/disable |
|---|---|---|---|---|---|
| *4 | 858 | Received data clear specification | | The AJ35PTF-R2 station number which executes received data clear by the received data clear request signal [Y (n + 23)] is specified. | Read/write enable |
| | 859 | Received data clear range specification | | The receive buffer which is cleared when the received data clear is executed by the received data clear request signal [Y (n + 23)] is specified. | |
| | 860 to 929 | No-protocol mode parameter | | Parameters when using the AJ35PTF-R2 in a no-protocol mode are set. | |
| | 930 to 1099 | (Unused) | | ——— | ——— |
| | | CH0 | CH1 | | |
| *5 | 1100 to 2099 | Communication area for remote terminal No. 1 | Communication area for remote terminal No. 8 | Send data to the remote terminal unit write area, or, received data from the remote terminal unit store area. | Read/write enable |
| | 2100 to 3099 | Communication area for remote terminal No. 2 | Communication area for remote terminal No. 9 | | |
| | 3100 to 4099 | Communication area for remote terminal No. 3 | Communication area for remote terminal No. 10 | | |
| | 4100 to 5099 | Communication area for remote terminal No. 4 | Communication area for remote terminal No. 11 | | |
| | 5100 to 6099 | Communication area for remote terminal No. 5 | Communication area for remote terminal No. 12 | | |
| | 6100 to 7099 | Communication area for remote terminal No. 6 | Communication area for remote terminal No. 13 | | |
| | 7100 to 8099 | Communication area for remote terminal No. 7 | Communication area for remote terminal No. 14 | | |
| | | [Y (n + 2C) at OFF] | [Y (n + 2C) at ON] | | |

*4: Clear processing area of received data by the AD62C reset operation
*5: Buffer memory area for AD62C data transfer (1st module to 14th module)

## 6.5 Programming Examples

Programming under the following setting conditions of The PLC CPU, A1S/AJ71PT32-S3, and AD62C is explained below.




1) Input signal assignment (assigned to link relay B) of the PLC CPU parameter automatic refresh setting
   - Batch refresh received data
     ..... B100 to B2FF (For X00 to X1F of AD62C)
   - Batch refresh send data
     ..... B300 to B4FF (For Y00 to Y1F of AD62C)
2) A1S/ AJ71PT32-S3 is loaded to slot 0 (occupying 48 points: I/O No. X/Y00 to X/Y2F)
3) AD62C remote terminal number is set to "1" (initial ROM)
4) AD62C station number is set to "01" (occupying stations Nos. 1 to 4)

**[Basic programs]**

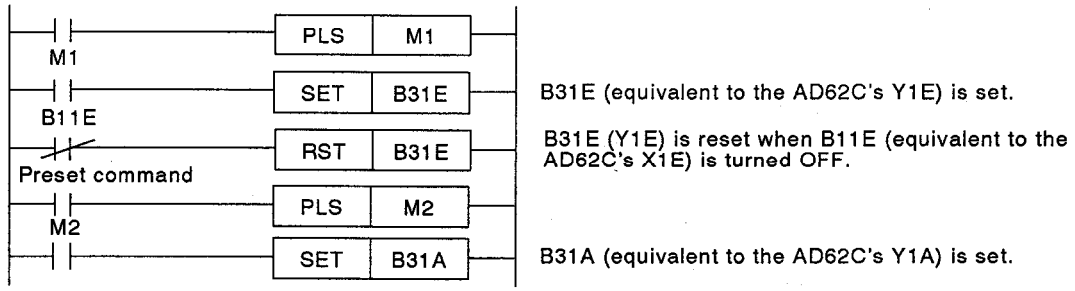
Basic programs to control the AD62C via the AJ71PT32-S3 are explained below.

(1) I/O signal processing program (X18 to X1F, Y18 to Y1F)

(a) Link relay "B" assigned by the parameter automatic refresh setting is used.

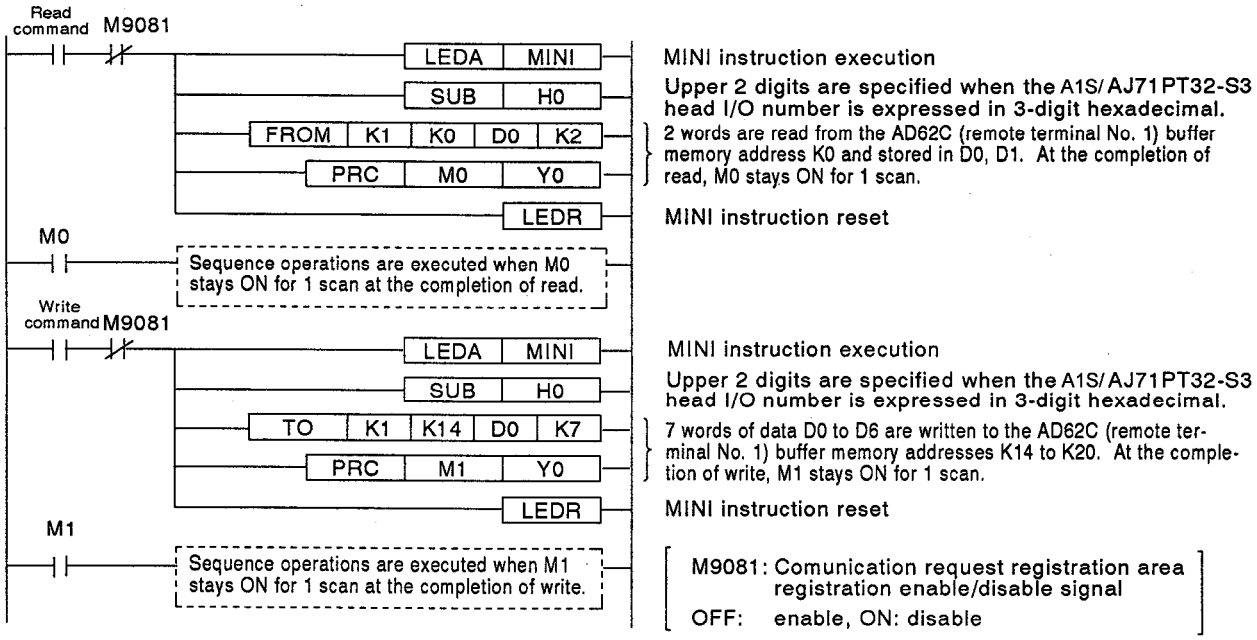
(b) The AD62C I/O signal (X/Y) equivalent to "B" is turned ON/OFF via the A1S/AJ71PT32-S3.

External preset request detection/reset command



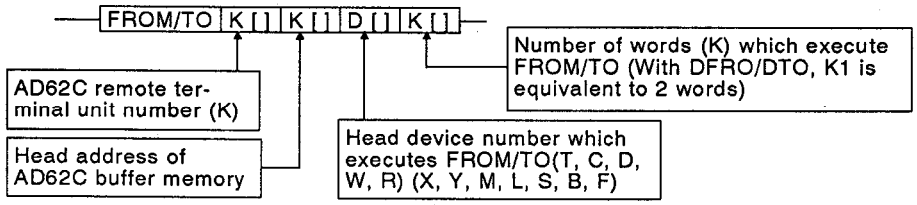
(2) Buffer memory processing program

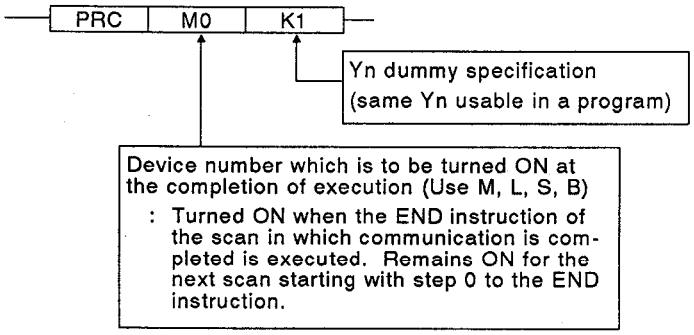
Read/write of buffer memory is executed by directly designating AD62C buffer memory addresses using PLC CPU dedicated instructions via the A1S/ AJ71PT32-S3. (The AD62C buffer memory can be used without acknowledging the A1S/ AJ71PT32-S3 buffer memory.)




(a) FROM/TO and PRC instructions

For details about FROM/TO and the PRC instruction, see the type AnSHCPU/AnACPU/AnUCPU/QCPU-A (A Mode) (Dedicated instructions) Programming Manual.



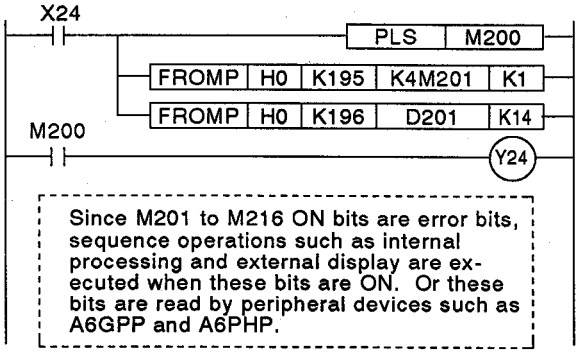

**POINT**

When the FROM/TO instruction is executed by the sequence program, data communication is executed via the A1S/ AJ71PT32-S3 buffer memory.

When the execution completion device of the PRC instruction is turned ON, data communications ends.

(3) Error detection program

A1S/AJ71PT32-S3 buffer memory K195 (remote terminal unit faulty station) and K196 to K209 (remote terminal unit error code) are read.




Buffer memory is read when X24 (error detection) is ON and reset command is executed.

Faulty station read (Faulty stations: M201 to M216 when bit ON)

The error codes of terminals No. 1 to No. 14 are read to D201 to D214.

When M200 is ON, Y24 turns ON and X24 turns OFF.

After staying ON for 1 scan, Y24 turns OFF.

(a) Error codes which are detected by A1S/AJ71PT32-S3 are shown below.

| Error Codes (decimal) | Error Names | Error Contents | Corrective Action(s) |
|---|---|---|---|
| 1 | Set data error | There is an error in the data set to the AD62C send area. | Set correct data. |
| 6 | WDT error | AD62C is malfunctioning. | Confirm the AD62C LED indicators and correct following AD62C troubleshooting procedure. |
| 8 | Send area set error | AD62C send area size is insufficient. | Set the send area of the required number of bytes as send data to the AD62C. |
| 9 | Communication error | Normal communications between the master module and the AD62C cannot be executed. | • Noise: Execute communications again.<br>• Check the AD62C for possible hardware fault. |
| 11 | | | |
| 10 | Receive area set error | AD62C receive area size is insufficient. | Set the receive area of the required number of bytes as received data from the AD62C. |

(b) In addition to the above error codes, an error code which the AD62C detects is sent to the A1S/AJ71PT32-S3 and is stored in the A1S/AJ71PT32-S3 buffer memory.
(For AD62C error codes, see Section 9.1.)

(4) Data clear processing program by AD62C reset operations and allowable communication time over

(a) When the AD62C's front reset switch is operated during communications, it is necessary to write the initial data again after detecting the reset operation and clearing the A1S/AJ71PT32-S3 received data by the sequence program.

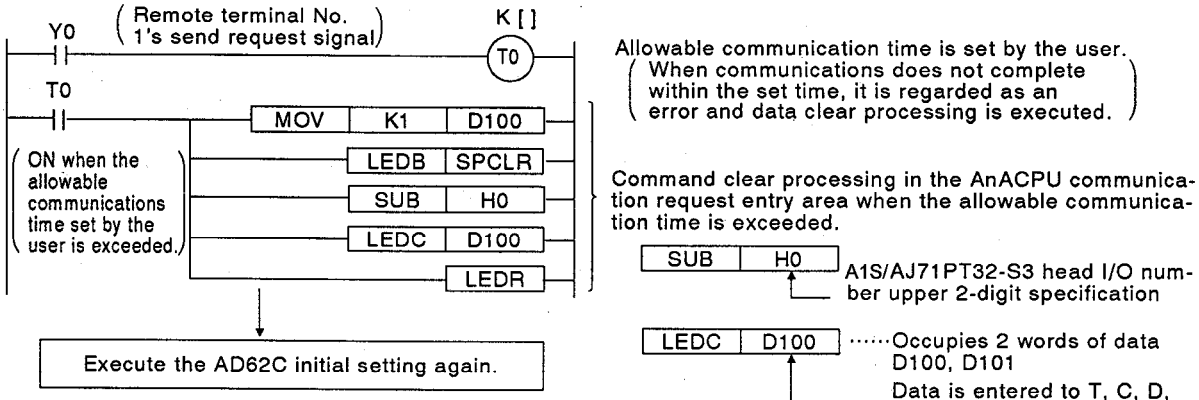
- If the initial setting is not executed again after reset operations, the AD62C will not operate correctly.
- Create a sequence program which clears command data in the PLC CPU communications request entry area during initial setting under the conditions when both the reset status detection and reset status detection reset signals are ON.

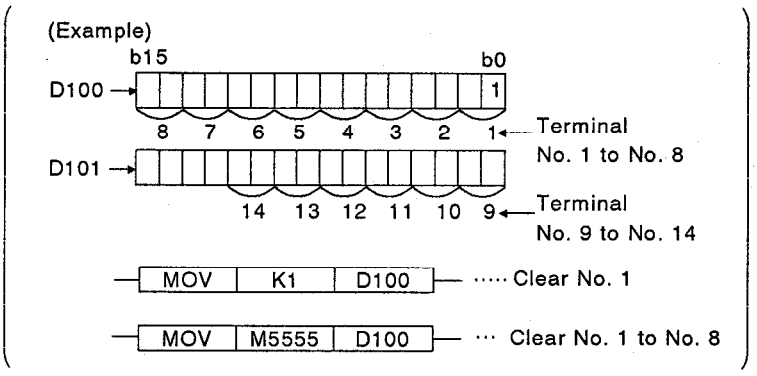
(b) When the reset switch is pressed and a non-sending status to the PLC CPU has occurred, such status will remain. Therefore, set the allowable communication time by the timer, execute data clear, and re-execute the send request.

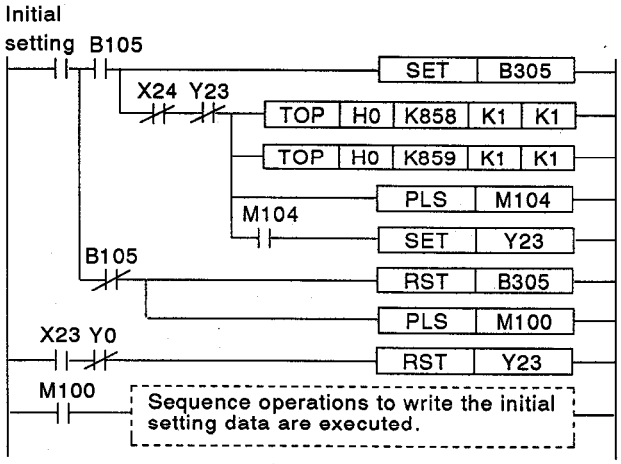
(c) For the detection of the AD62C reset status, create a program using parameter automatic refresh setting link relay "B" equivalent to AD62C I/O signals.

- Reset status detection ..... X05 ON → B105 ON
- Reset status detection is reset ..... Y05 ON → B305 ON

[When B305 (Y05) is ON, B105 (X05) turns OFF.]






The reset status detection is reset and command data in the PLC CPU communication request entry area is cleared.

With B105 (X05) ON by reset operations, A1S/AJ71PT32-S3 received data clear processing ("1" written to the buffer memory) is executed.

The master module is cleared so that communications can be executed again. However, the contents of the received data area will not be cleared.

At the completion of clear (X23 ON), the clear request (Y23) turns OFF and at the same time X23 turns OFF.

### 6.5.1 Preset function programming example

(1) Preset function programming example using a sequence program

Create a program to count 2-phase pulses multiplied by one and to execute the preset function using the sequence program.

**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command.....M9038

(b) Communication request command.....X30

(c) Intial setting execute command.....X31

(d) Count operation start command.....X32

(e) Preset value read command.....X33

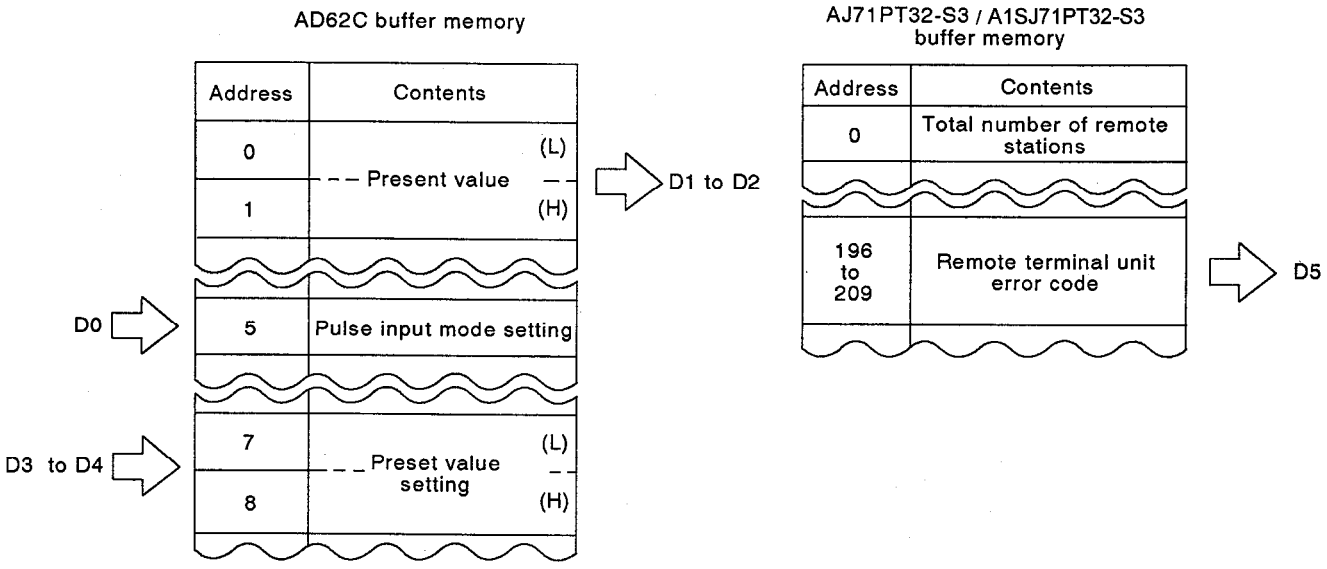
(f) Preset value write command.....X34

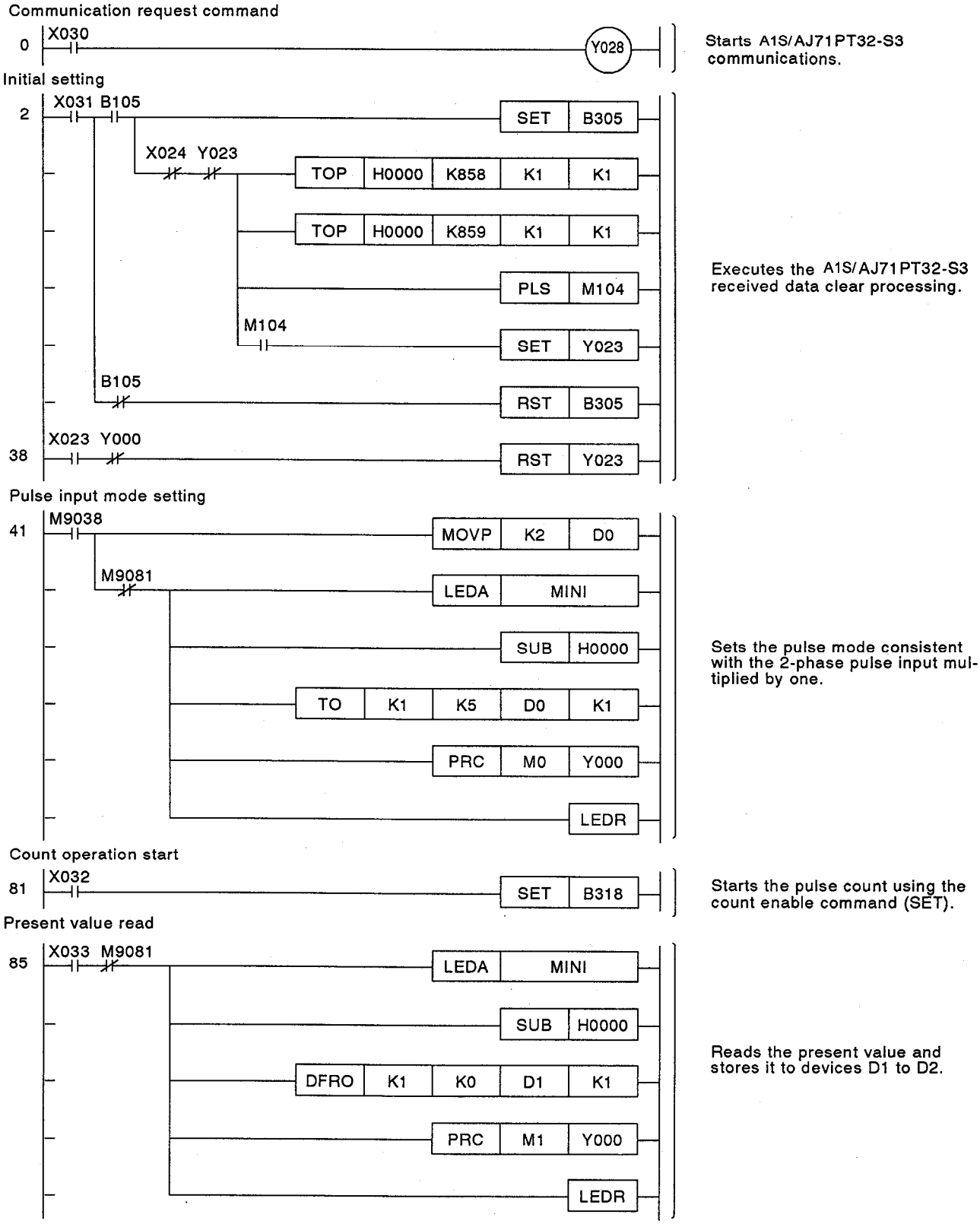
(g) Preset execute command.....X35

(h) Communication error reset command.....X36

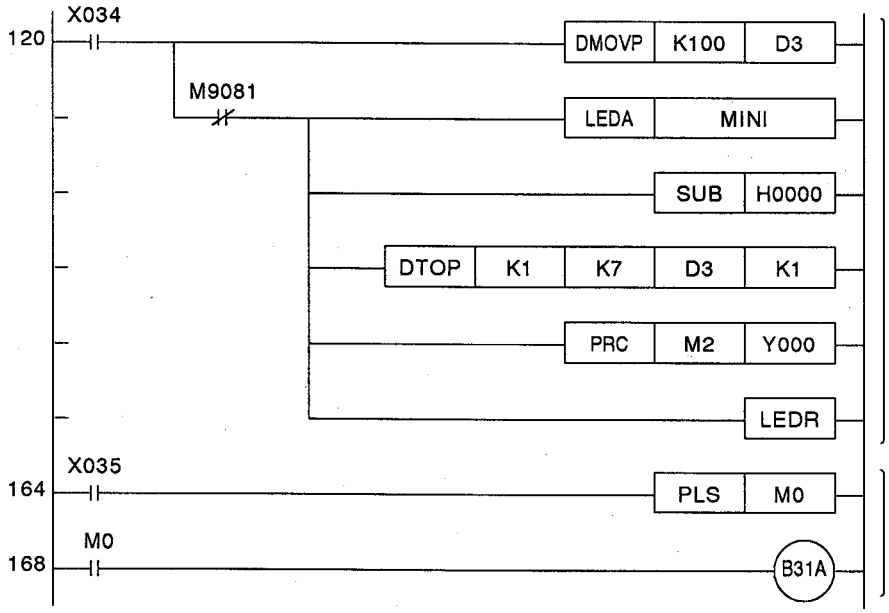
(i) Count operation stop command.....X37

(b) Relationship between the data register (D0 to D5) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Executes the A1S/AJ71PT32-S3 received data clear processing.
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR
Reads the present value and stores it to devices D1 to D2.

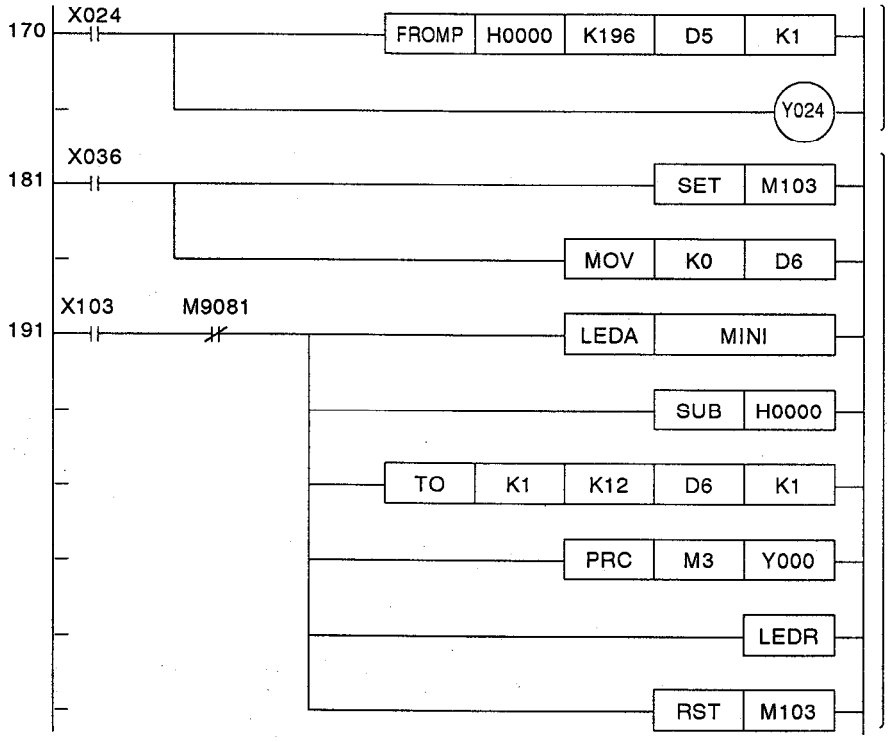
Preset command




Stores the preset value of 100 to buffer memory address 7.

Executes the preset.

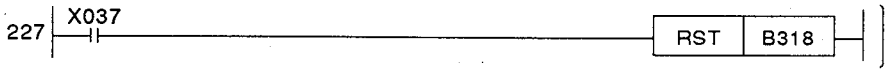
Communication error detection/reset




Reads the communication error code and stores it to device D5.

Resets the communication error.

Count operation stop




Stops the pulse count using the count enable command (RST).

CIRCUIT END

(2) Preset function programming example using an external input

Create a program to count 2-phase pulses multiplied by one and to execute the preset function with the external input.

**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command.....M9038

(b) Communication request command.....X30

(c) Intial setting execute command.....X31

(d) Count operation start command.....X32

(e) Preset value read command.....X33

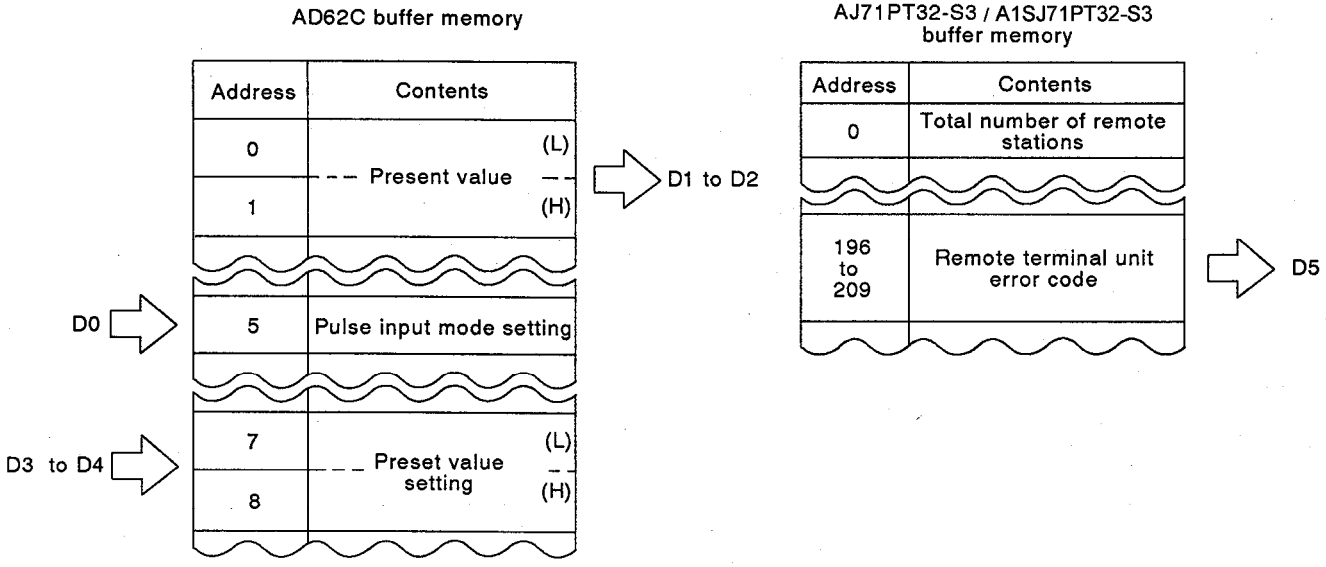
(f) Preset value write command.....X34

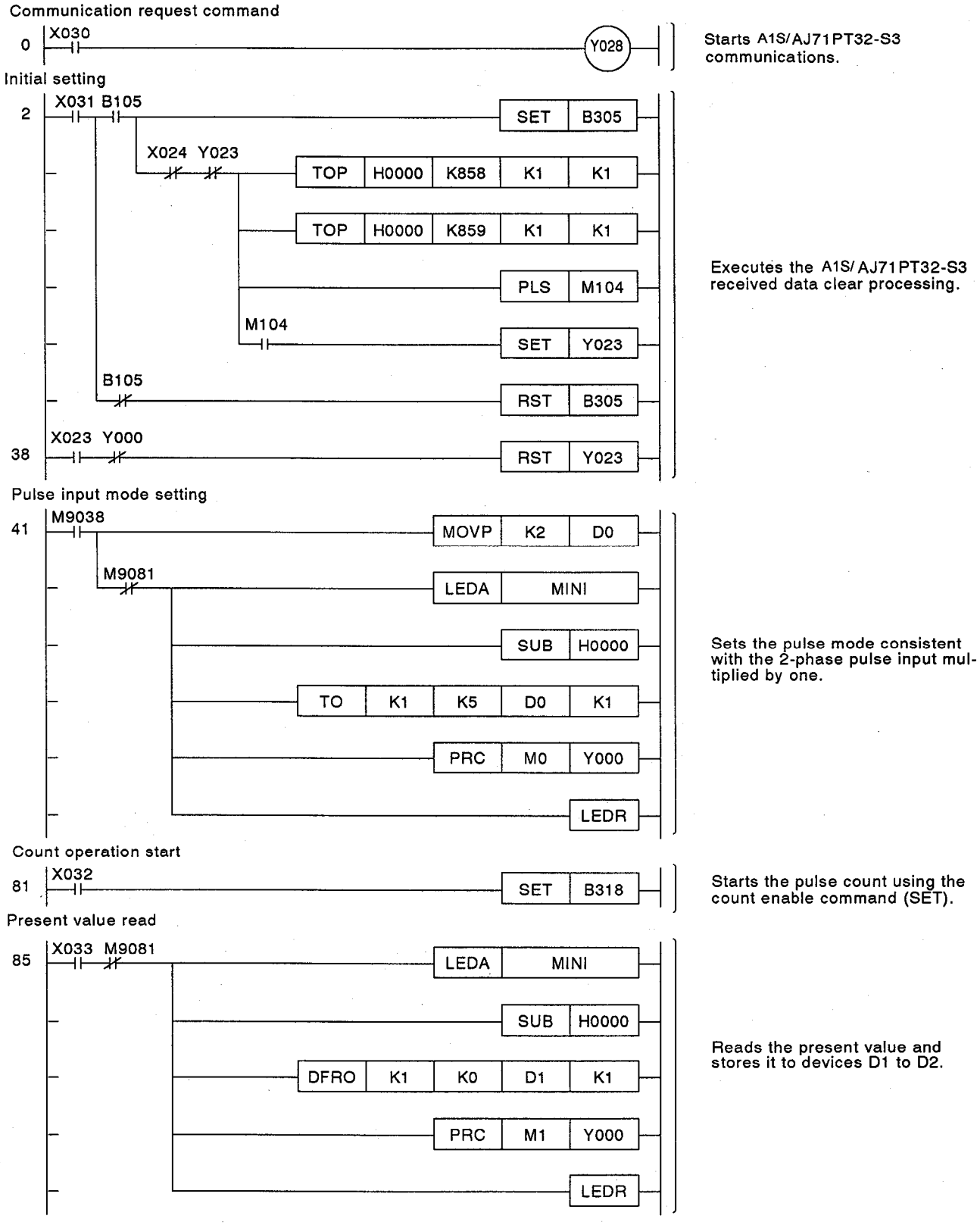
(g) External preset command derection flag reset command.....X1E

(h) Communication error reset command.....X35

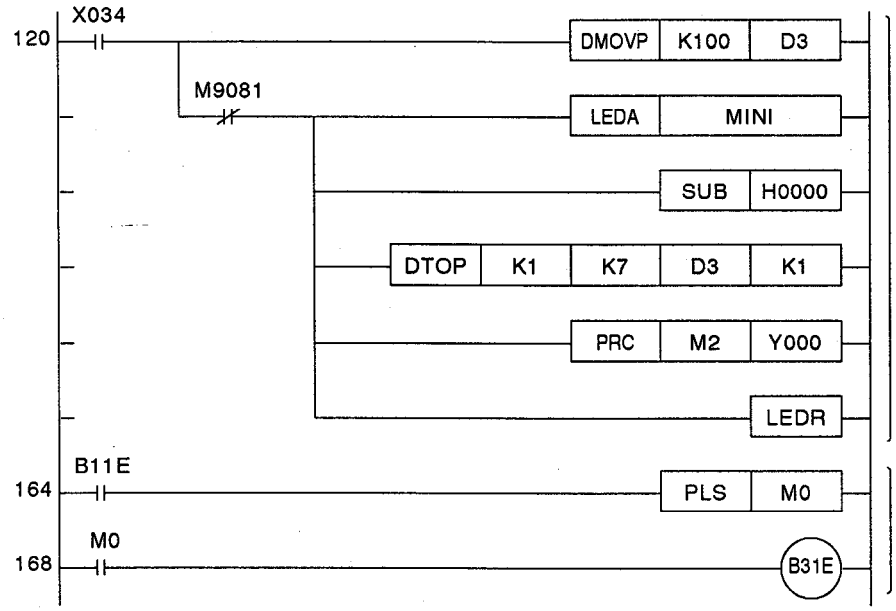
(i) Count operation stop command.....X36

(b) Relationship between the data register (D0 to D5) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Executes the A1S/AJ71PT32-S3 received data clear processing.
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR
Reads the present value and stores it to devices D1 to D2.

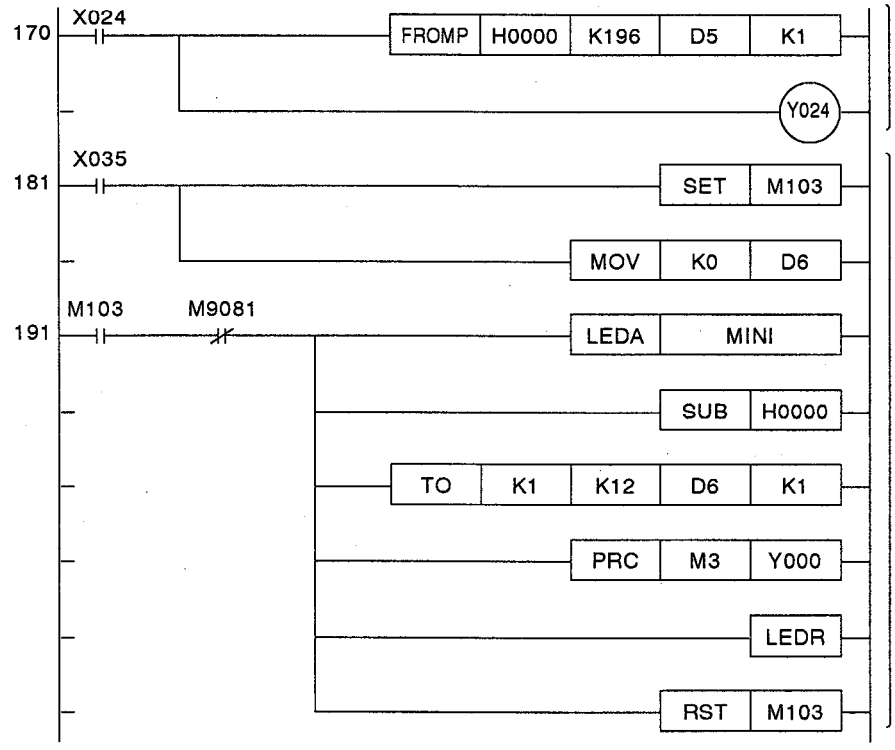
Preset command




Stores the preset value of 100 to buffer memory address 7.

Resets external preset command detection flag.

Communication error detection/reset




Reads the communication error code and stores it to device D5.

Resets the communication error.

Count operation stop


Stops the pulse count using the count enable command (RST).

CIRCUIT END

### 6.5.2 Ring counter function programming example

Create a program to count 2-phase pulses multiplied by one and to execute the ring counter function.

**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command ..... M9038

(b) Communication request command ..... X30

(c) Initial setting execute command ..... X31

(d) Count operation start command ..... X32

(e) Present value read command ..... X33

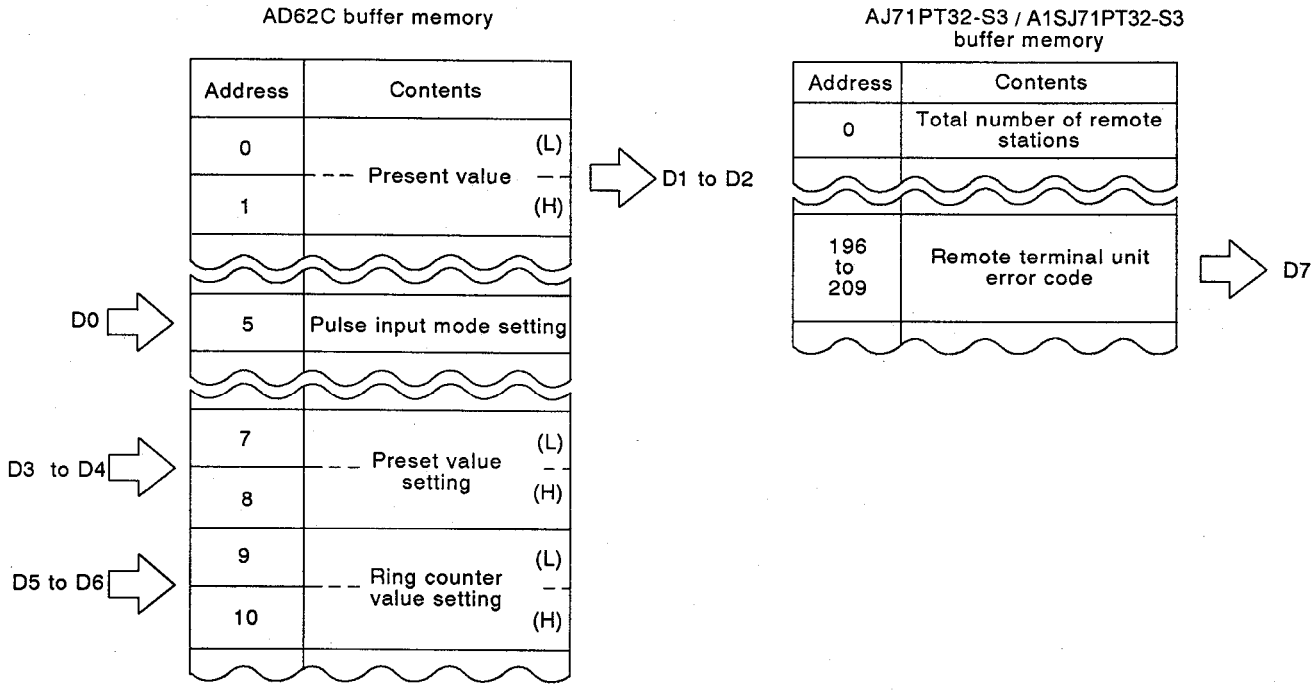
(f) Preset/ring count value write command ..... X34

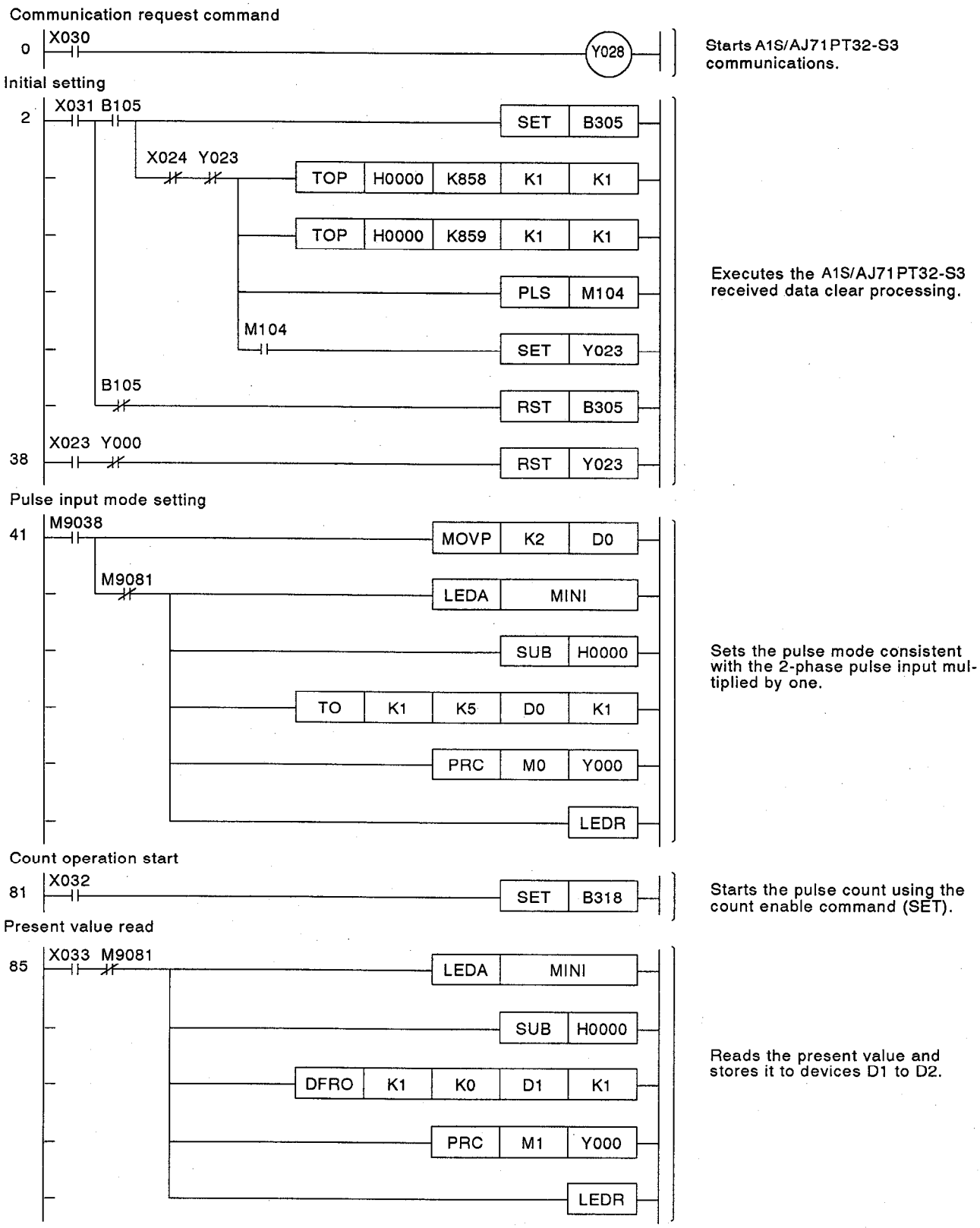
(g) Ring counter command ..... X35

(h) Communication error reset command ..... X36

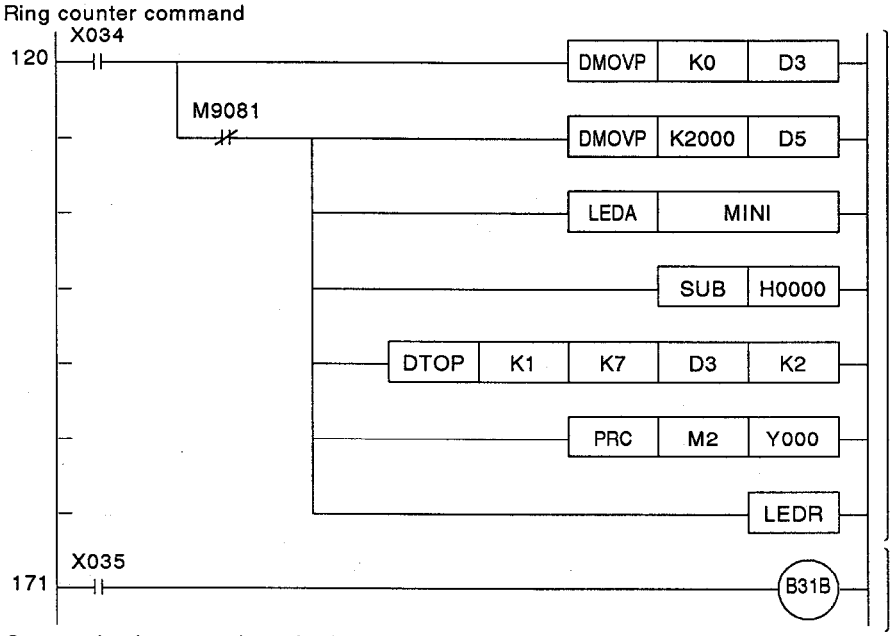
(i) Count operation stop command ..... X37

(2) Relationship between the data register (D0 to D7) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Executes the A1S/AJ71PT32-S3 received data clear processing.
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR
Reads the present value and stores it to devices D1 to D2.

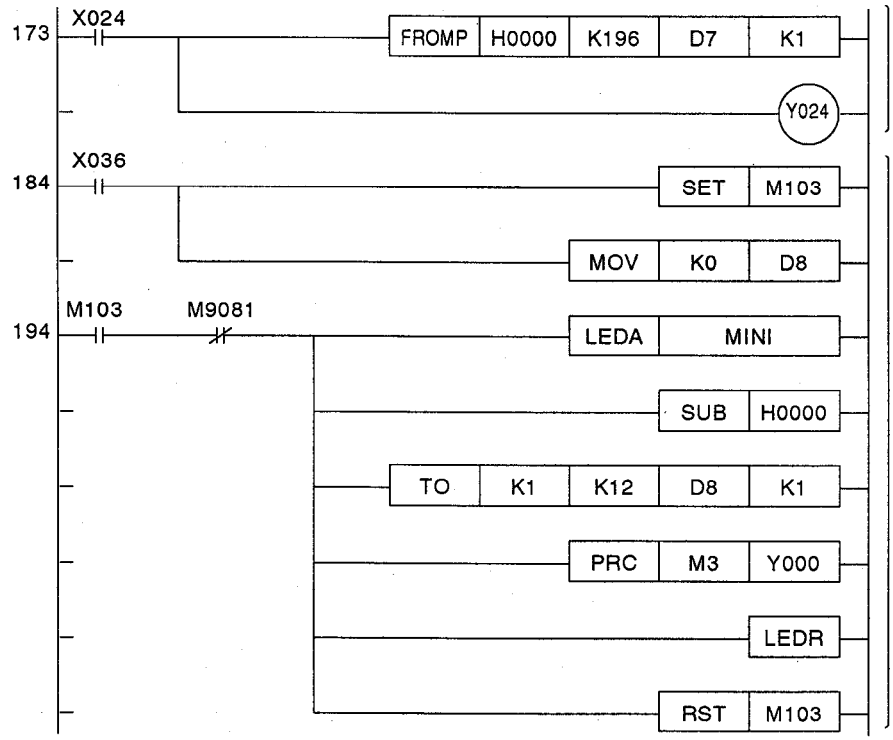
Ring counter command




Stores the preset value and ring counter value to buffer memory addresses 7 to 10.

Executes the ring counter.

Communication error detection/reset




Reads the communication error code and stores it to device D7.

Resets the communication error.

Count operation stop


Stops the pulse count using the count enable command (RST).

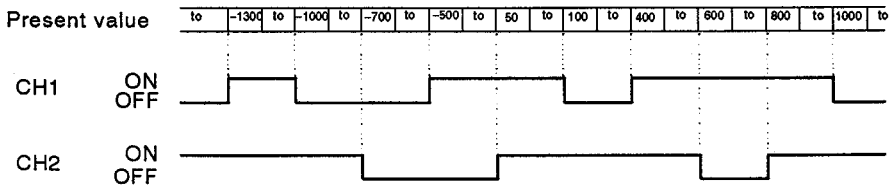
CIRCUIT END

### 6.5.3 Limit switch output function programming example

Create a program to count 2-phase pulses multiplied by one and to execute the limit switch function.

**[Operation status]**

ON/OFF status of the limit switch output is shown below:

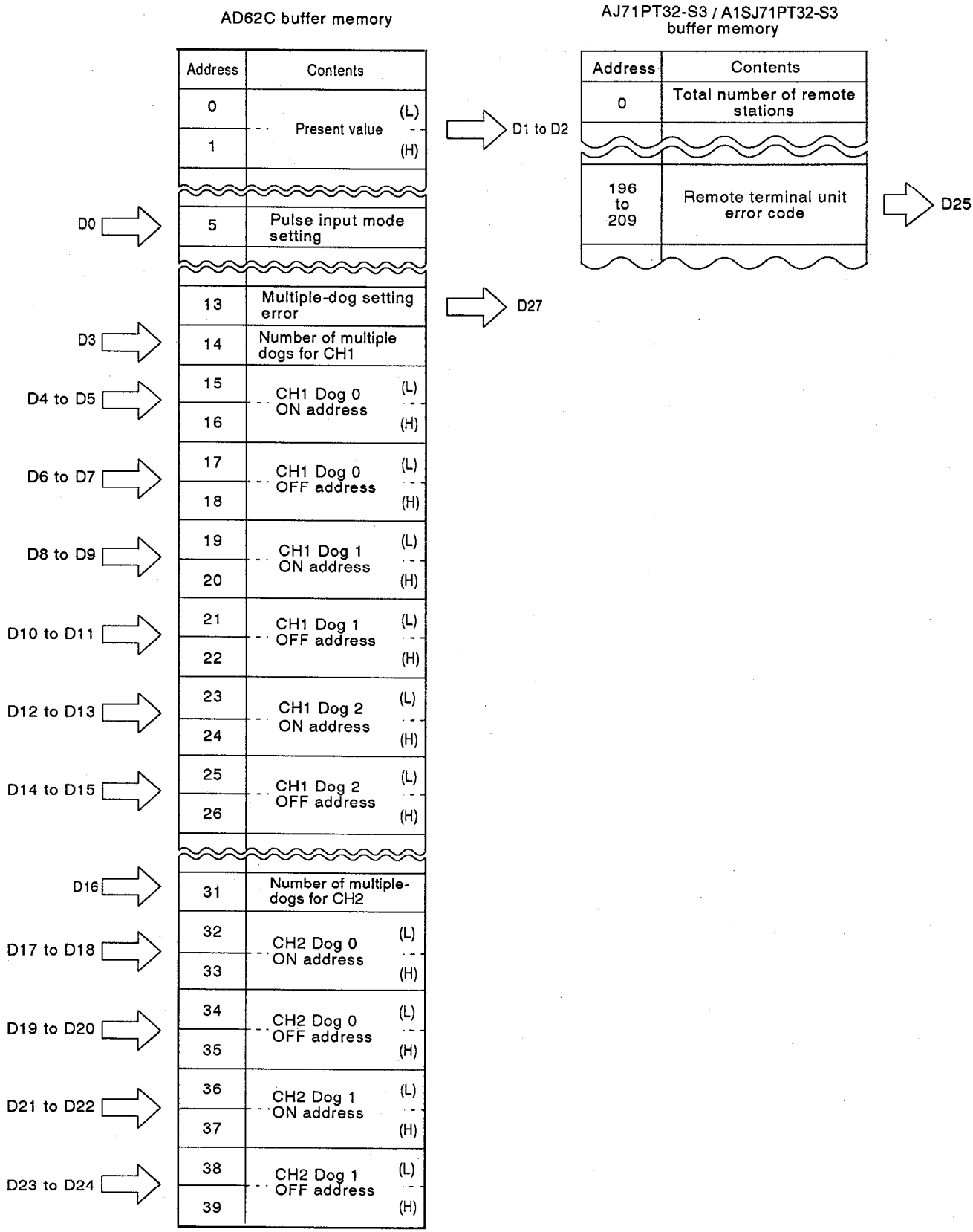


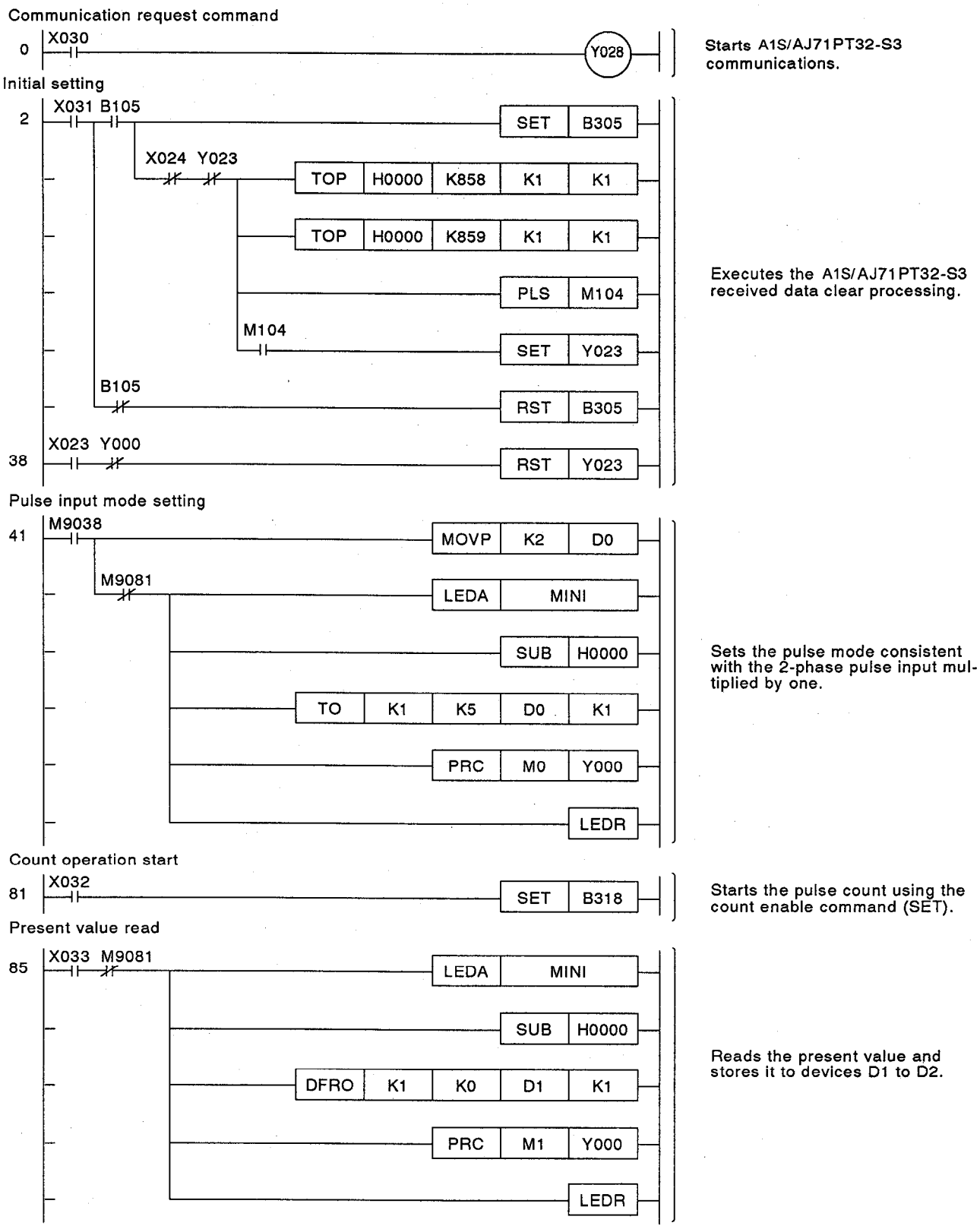

**[Devices to be used]**

(1) Execution commands

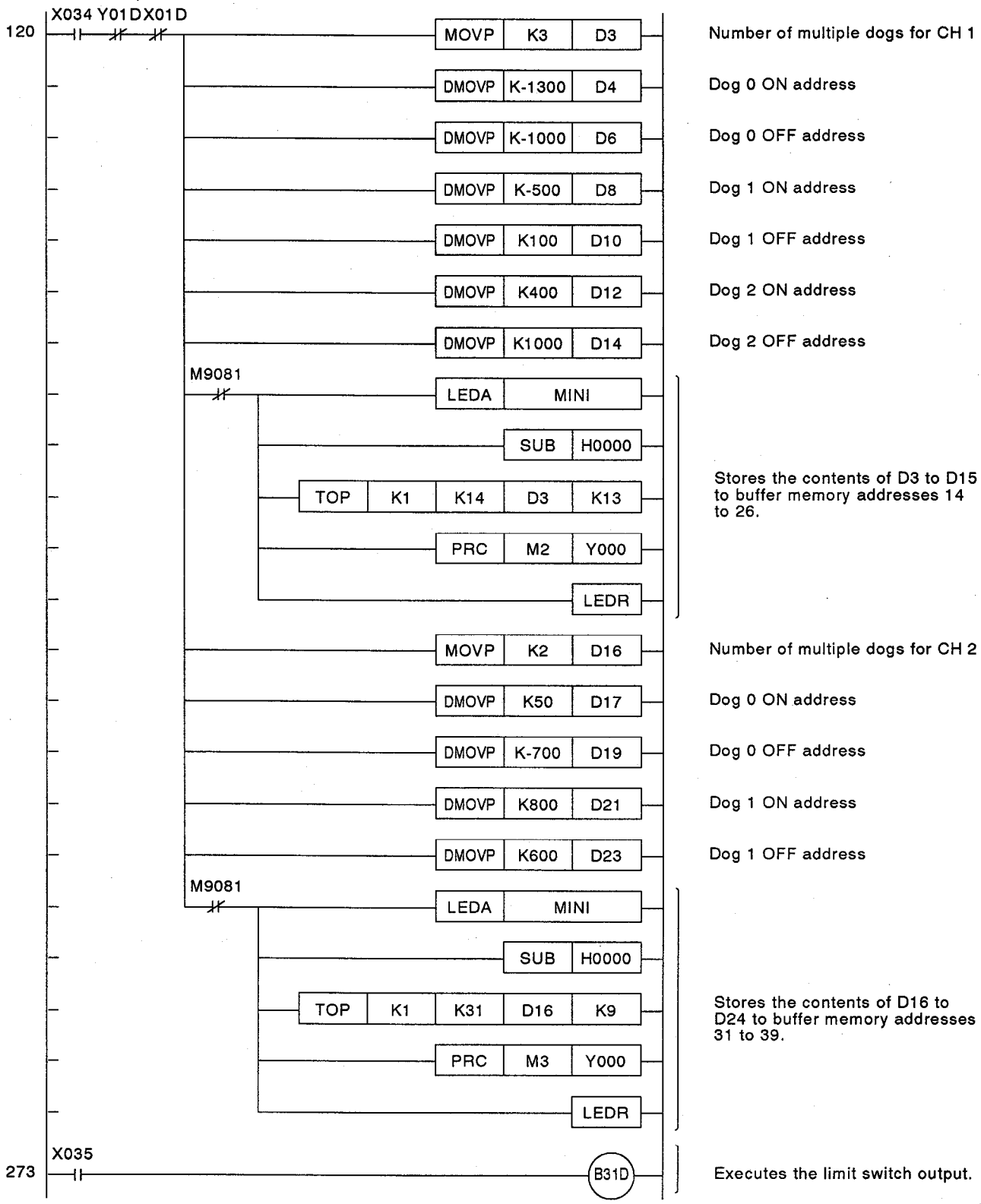
(a) Pulse input mode setting command ..... M9038
(b) Fuse blown detection ..... X1B
(c) Communication request command ..... X30
(d) Initial setting execute command ..... X31
(e) Count operation start command ..... X32
(f) Present value read command ..... X33
(g) Limit switch output data setting command ..... X34
(h) Limit switch output command ..... X35
(i) Communication error reset command ..... X36
(j) Multiple-dog setting error reset command ..... X37
(k) Count operation stop command ..... X38

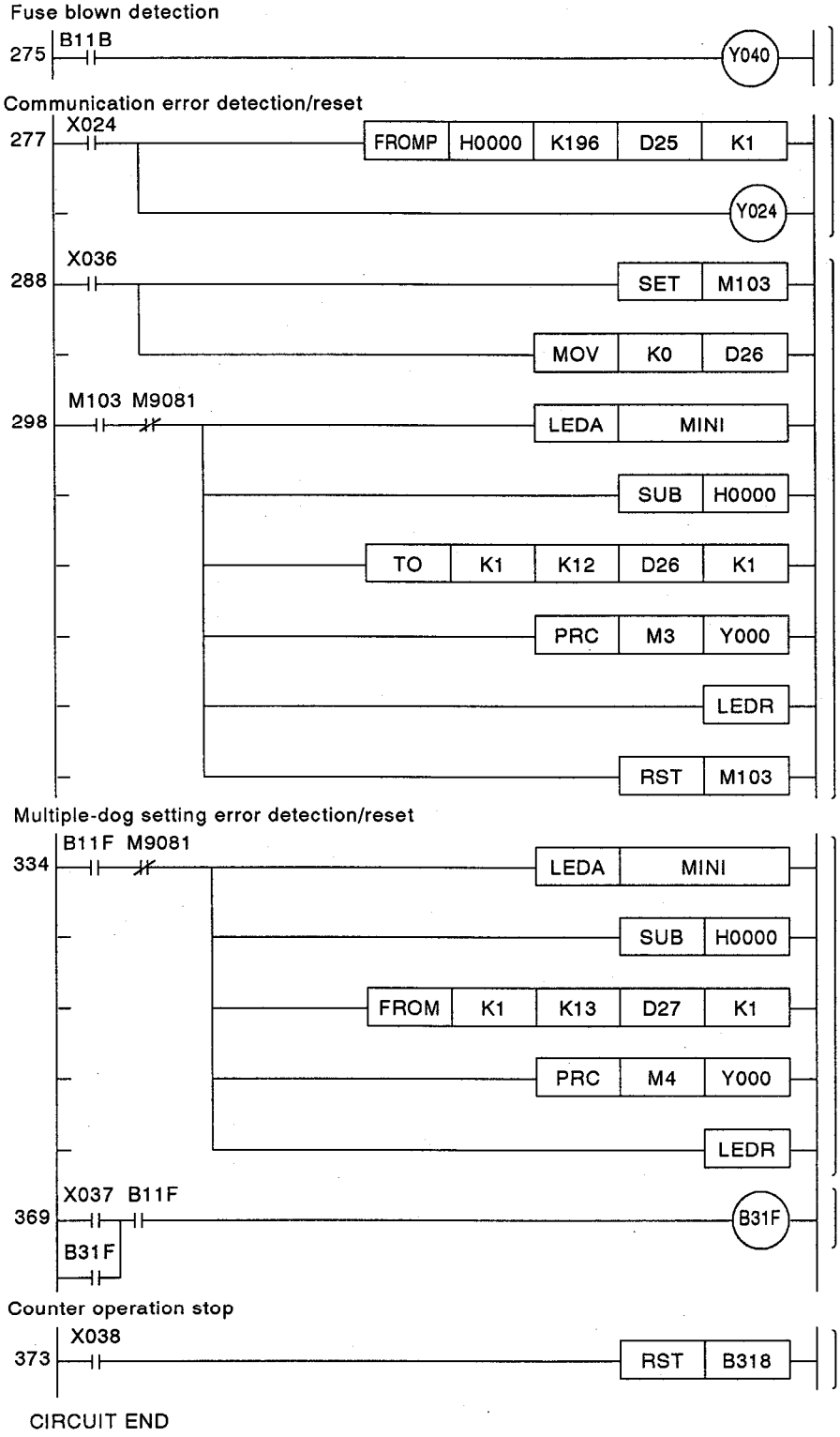
(2) Relationship between the data register (Do to D27) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
Executes the A1S/AJ71PT32-S3 received data clear processing.
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
Reads the present value and stores it to devices D1 to D2.
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR

Limit switch output command






Detects a blown fuse and output voltage cutoff.

Reads the communication error code and stores it to device D25.

Resets the communication error.

Reads the multiple-dog setting error code and stores it to device D27.

Resets the multiple-dog setting error.

Stops the pulse count using the count enable command (RST).

### 6.5.4 Latch counter function programming example

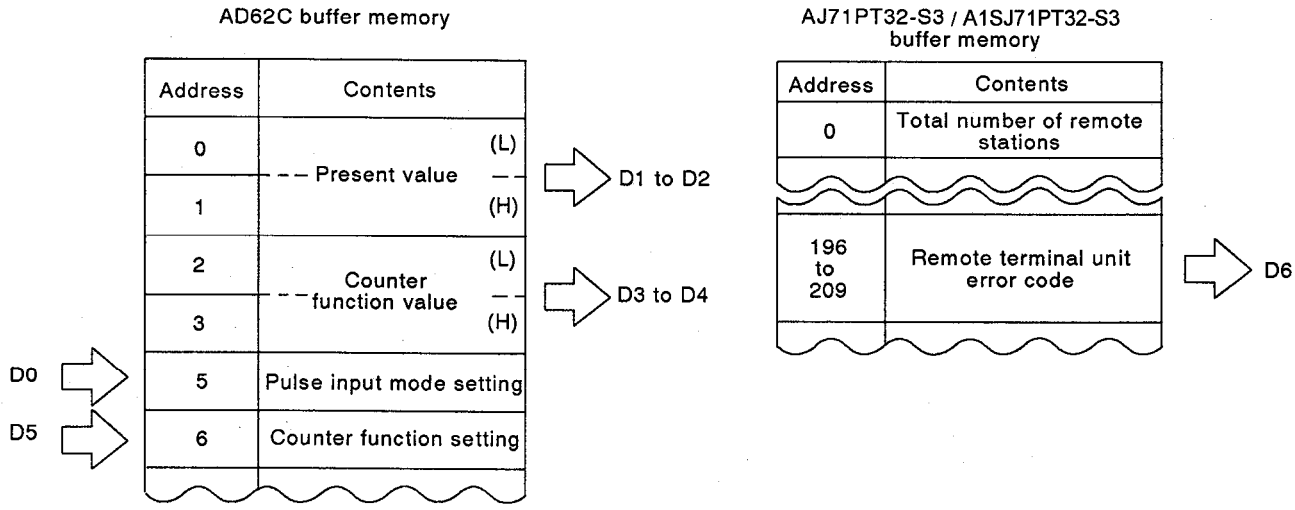
Create a program to count 2-phase pulses multiplied by one and to execute the latch counter.

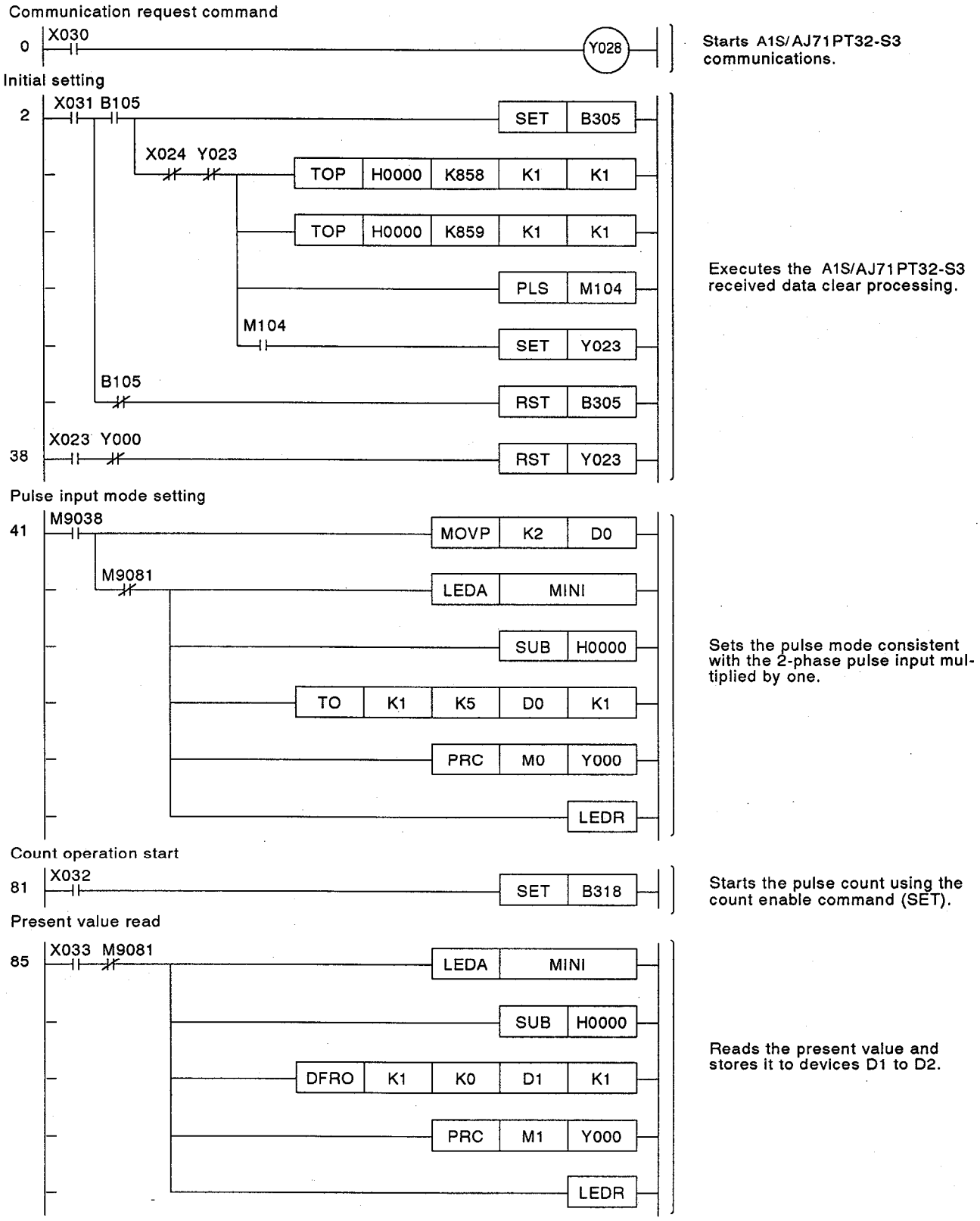
**[Devices to be used]**

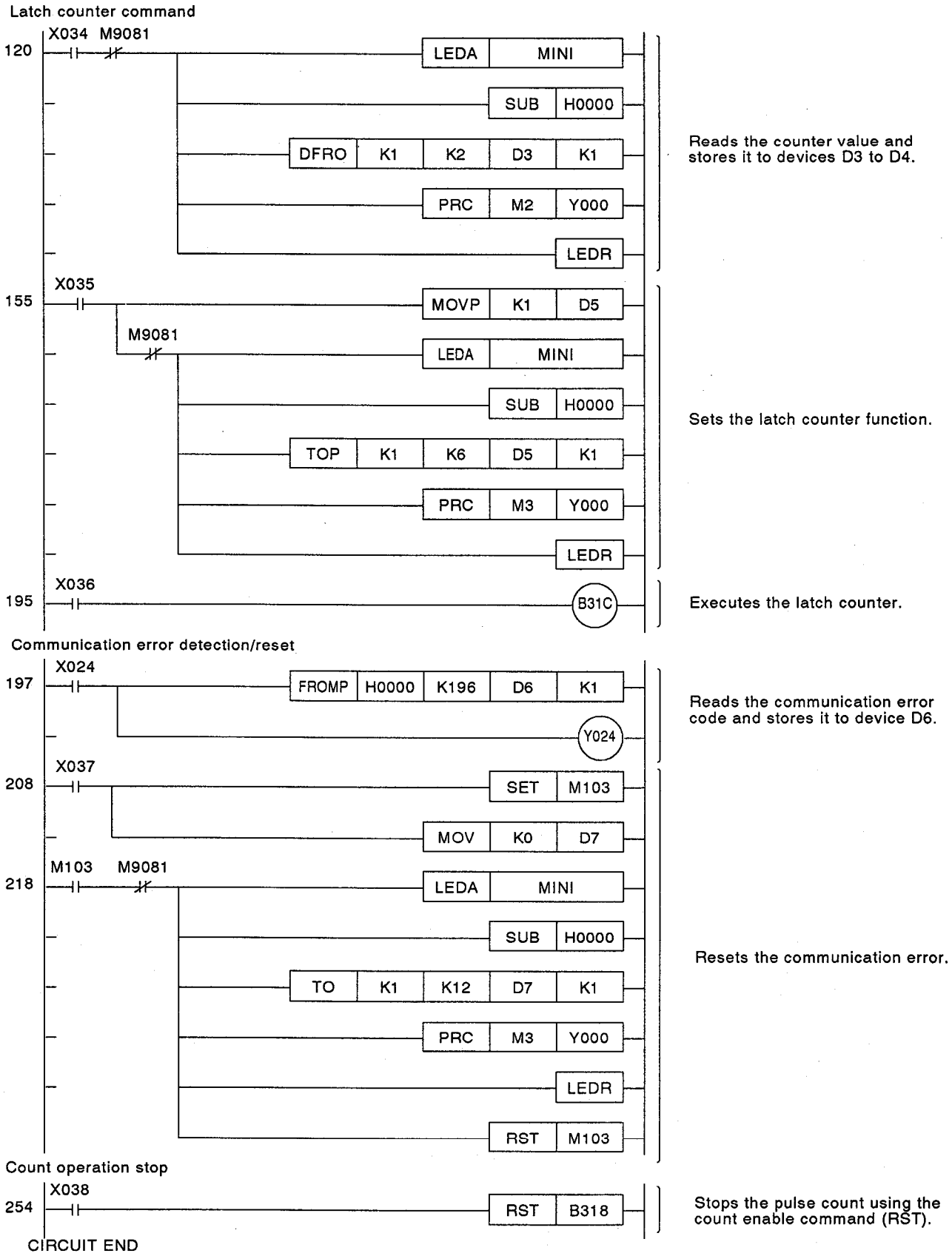
(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Communication request command ..... X30
(c) Initial setting execute command ..... X31
(d) Count operation start command ..... X32
(e) Present value read command ..... X33
(f) Counter function value read command ..... X34
(g) Counter function setting command ..... X35
(h) Latch counter command ..... X36
(i) Communication error reset command ..... X37
(j) Count operation stop command ..... X38

(2) Relationship between the data register (D0 to D6) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Executes the A1S/AJ71PT32-S3 received data clear processing.
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR
Reads the present value and stores it to devices D1 to D2.


Latch counter command
120
X034 M9081
LEDA MINI
SUB H0000
DFRO K1 K2 D3 K1
PRC M2 Y000
LEDR
Reads the counter value and stores it to devices D3 to D4.
155
X035
MOVP K1 D5
M9081
LEDA MINI
SUB H0000
TOP K1 K6 D5 K1
PRC M3 Y000
LEDR
Sets the latch counter function.
195
X036
B31C
Executes the latch counter.
Communication error detection/reset
197
X024
FROMP H0000 K196 D6 K1
Y024
Reads the communication error code and stores it to device D6.
208
X037
SET M103
MOV K0 D7
218
M103 M9081
LEDA MINI
SUB H0000
TO K1 K12 D7 K1
PRC M3 Y000
LEDR
RST M103
Resets the communication error.
Count operation stop
254
X038
RST B318
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 6.5.5 Sampling counter function programming example

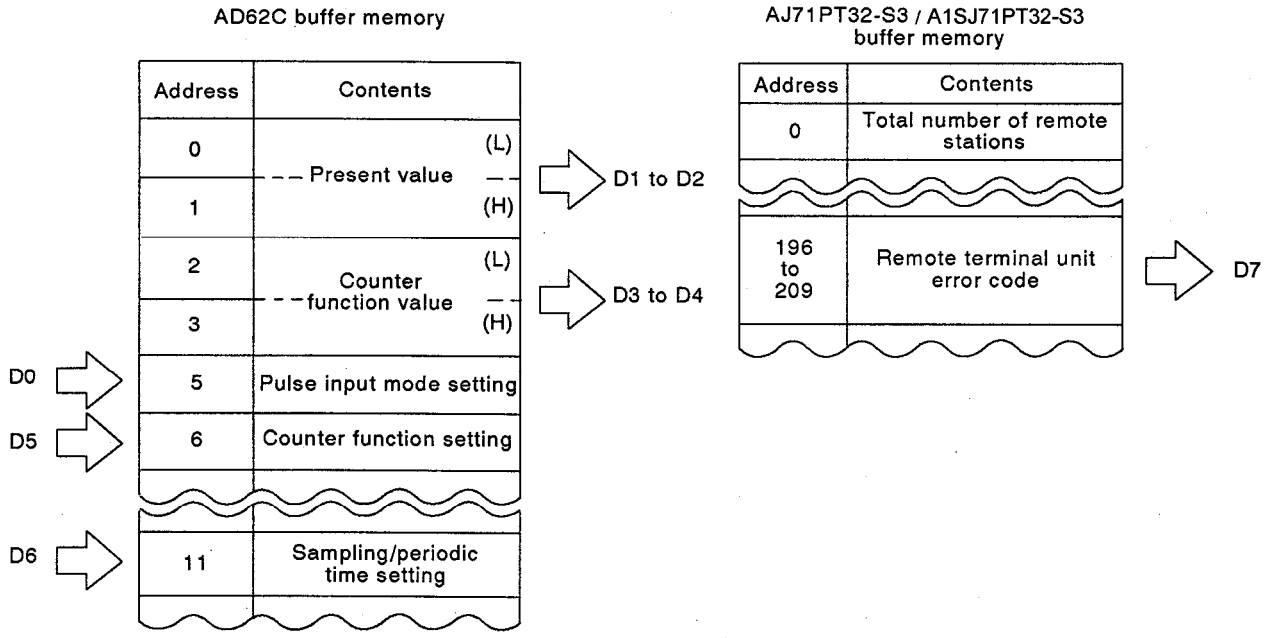
Create a program to count 2-phase pulses multiplied by one and to execute the sampling counter.

**[Devices to be used]**

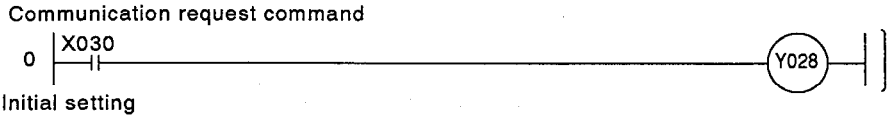
(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Communication request command ..... X30
(c) Initial setting execute command ..... X31
(d) Count operation start command ..... X32
(e) Present value read command ..... X33
(f) Counter function value read command ..... X34
(g) Counter function setting command ..... X35
(h) Sampling time setting command ..... X36
(i) Sampling counter command ..... X37
(j) Communication error reset command ..... X38
(k) Count operation stop command ..... X39

(2) Relationship between the data register (D0 to D7) and the buffer memory

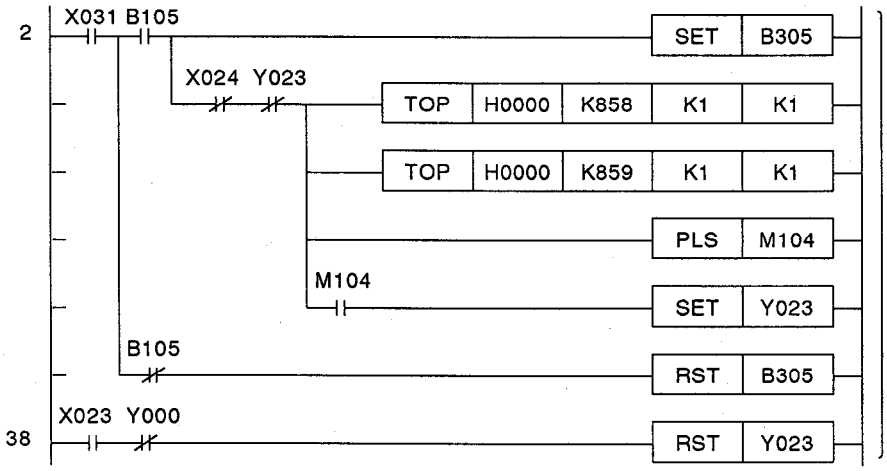


Communication request command



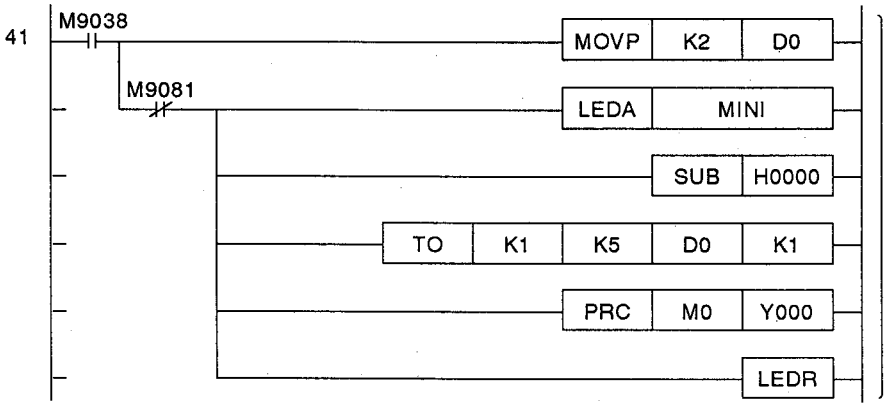

Starts A1S/AJ71PT32-S3 communications.

Initial setting




Executes the A1S/AJ71PT32-S3 received data clear processing.

Pulse input mode setting

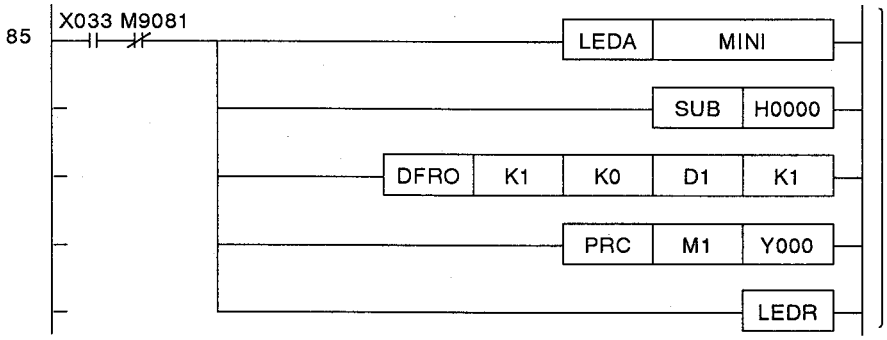



Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Count operation start

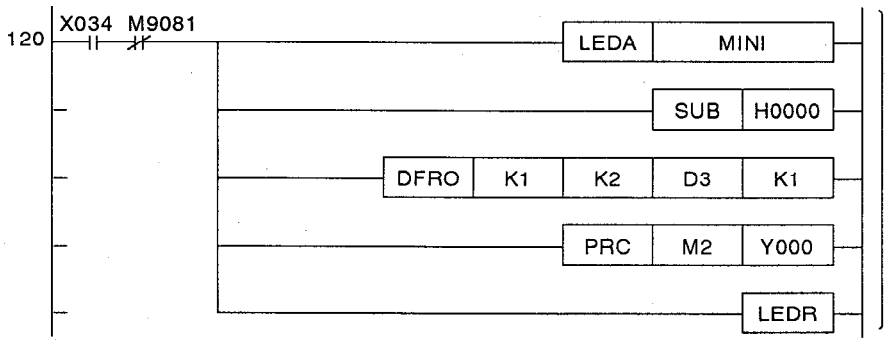

Starts the pulse count using the count enable command (SET).

Present value read

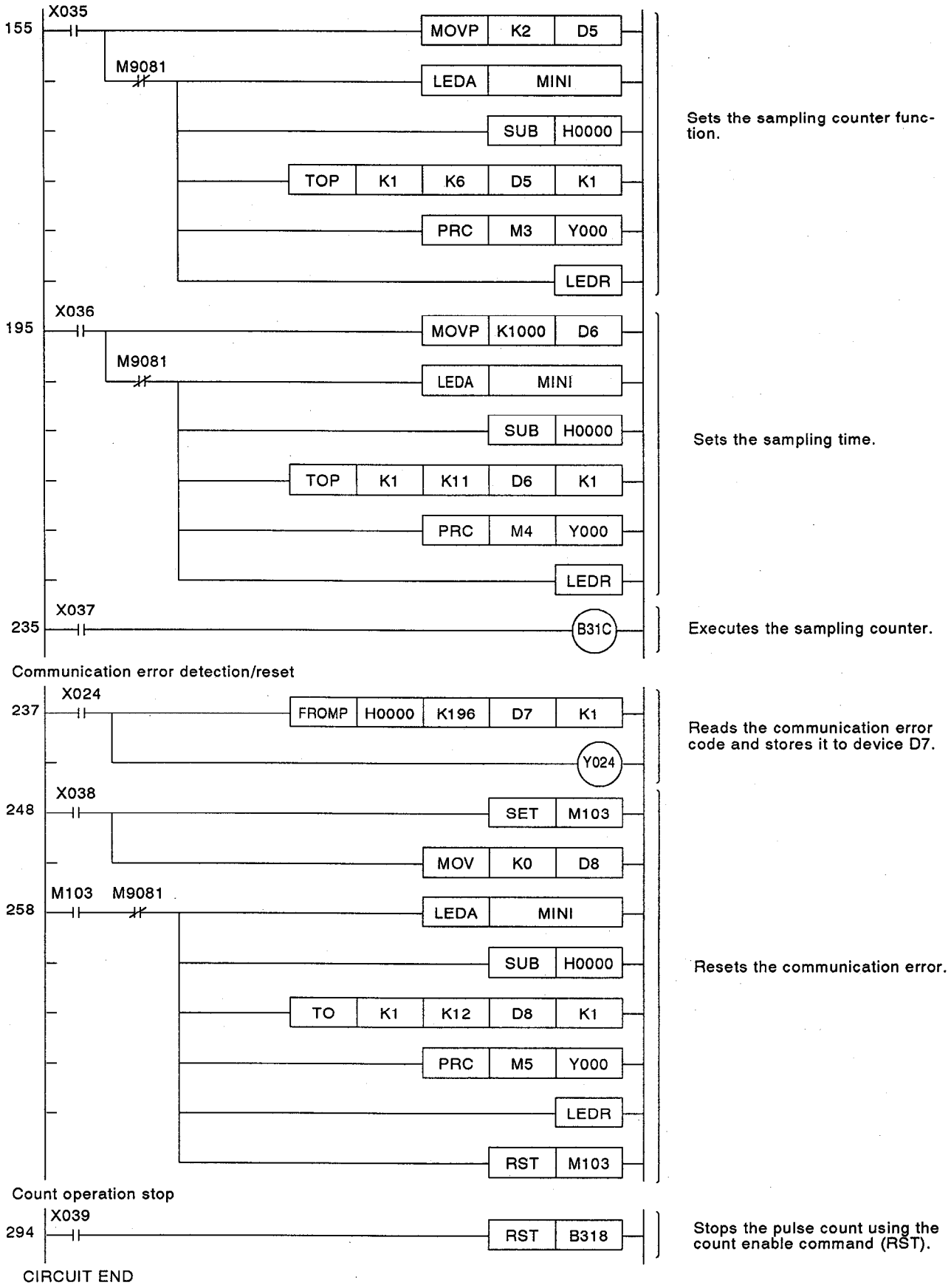



Reads the present value and stores it to devices D1 to D2.

Sampling counter command




Reads the counter value and stores it to devices D3 to D4.


155
X035
MOVP K2 D5
M9081
LEDA MINI
SUB H0000
TOP K1 K6 D5 K1
PRC M3 Y000
LEDR
Sets the sampling counter function.
195
X036
MOVP K1000 D6
M9081
LEDA MINI
SUB H0000
TOP K1 K11 D6 K1
PRC M4 Y000
LEDR
Sets the sampling time.
235
X037
B31C
Executes the sampling counter.
Communication error detection/reset
237
X024
FROMP H0000 K196 D7 K1
Y024
Reads the communication error code and stores it to device D7.
248
X038
SET M103
MOV K0 D8
258
M103 M9081
LEDA MINI
SUB H0000
TO K1 K12 D8 K1
PRC M5 Y000
LEDR
RST M103
Resets the communication error.
Count operation stop
294
X039
RST B318
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 6.5.6 Periodic pulse counter function programming example

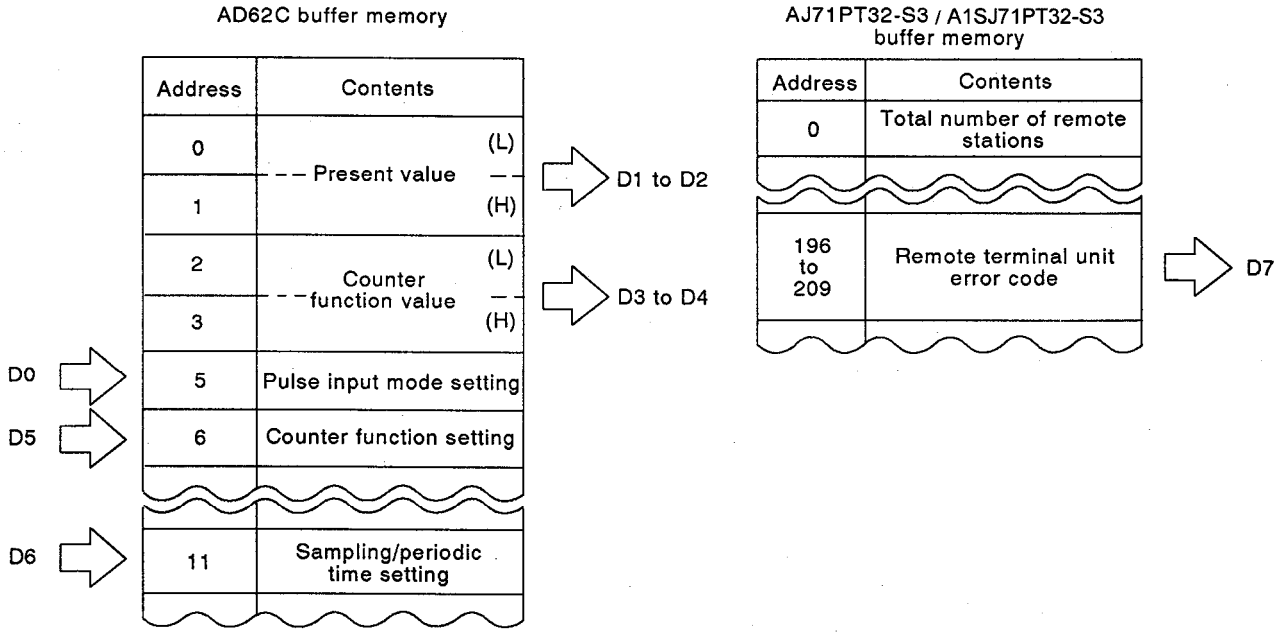
Create a program to count 2-phase pulses multiplied by one and to execute the periodic pulse counter function.

**[Devices to be used]**

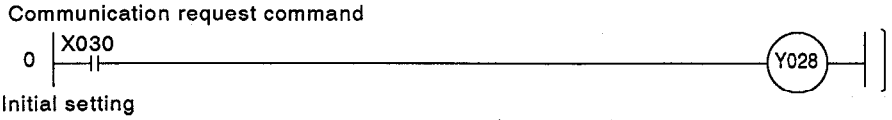
(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Communication request command.....X30
(c) Initial setting execute command.....X31
(d) Count operation start command.....X32
(e) Present value read command.....X33
(f) Counter function value read command.....X34
(g) Counter function setting command.....X35
(h) Periodic time setting command.....X36
(i) Periodic pulse counter command.....X37
(j) Communication error reset command.....X38
(k) Count operation stop command.....X39

(2) Relationship between the data register (D0 to D7) and the buffer memory

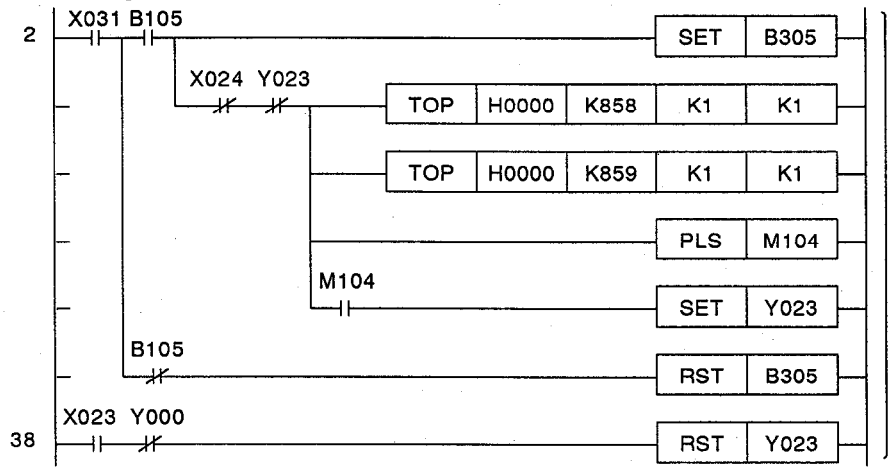


Communication request command



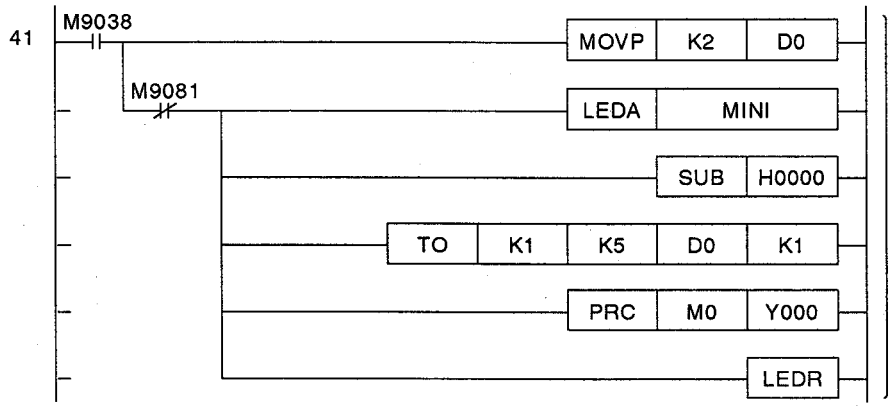

Starts A1S/AJ71PT32-S3 communications.

Initial setting




Executes the A1S/AJ71PT32-S3 received data clear processing.

Pulse input mode setting

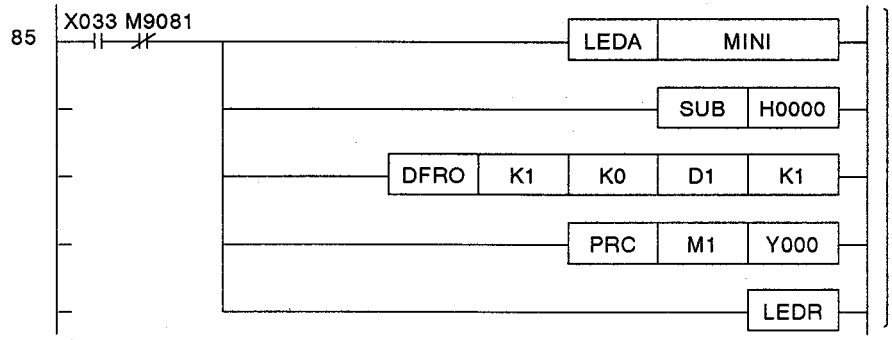



Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Count operation start

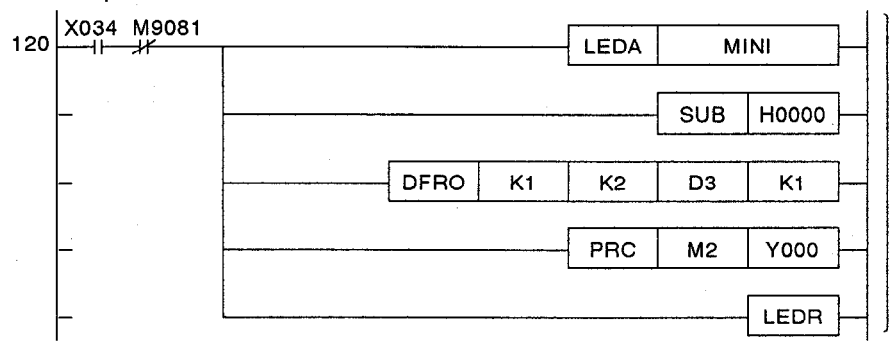

Starts the pulse count using the count enable command (SET).

Present value read

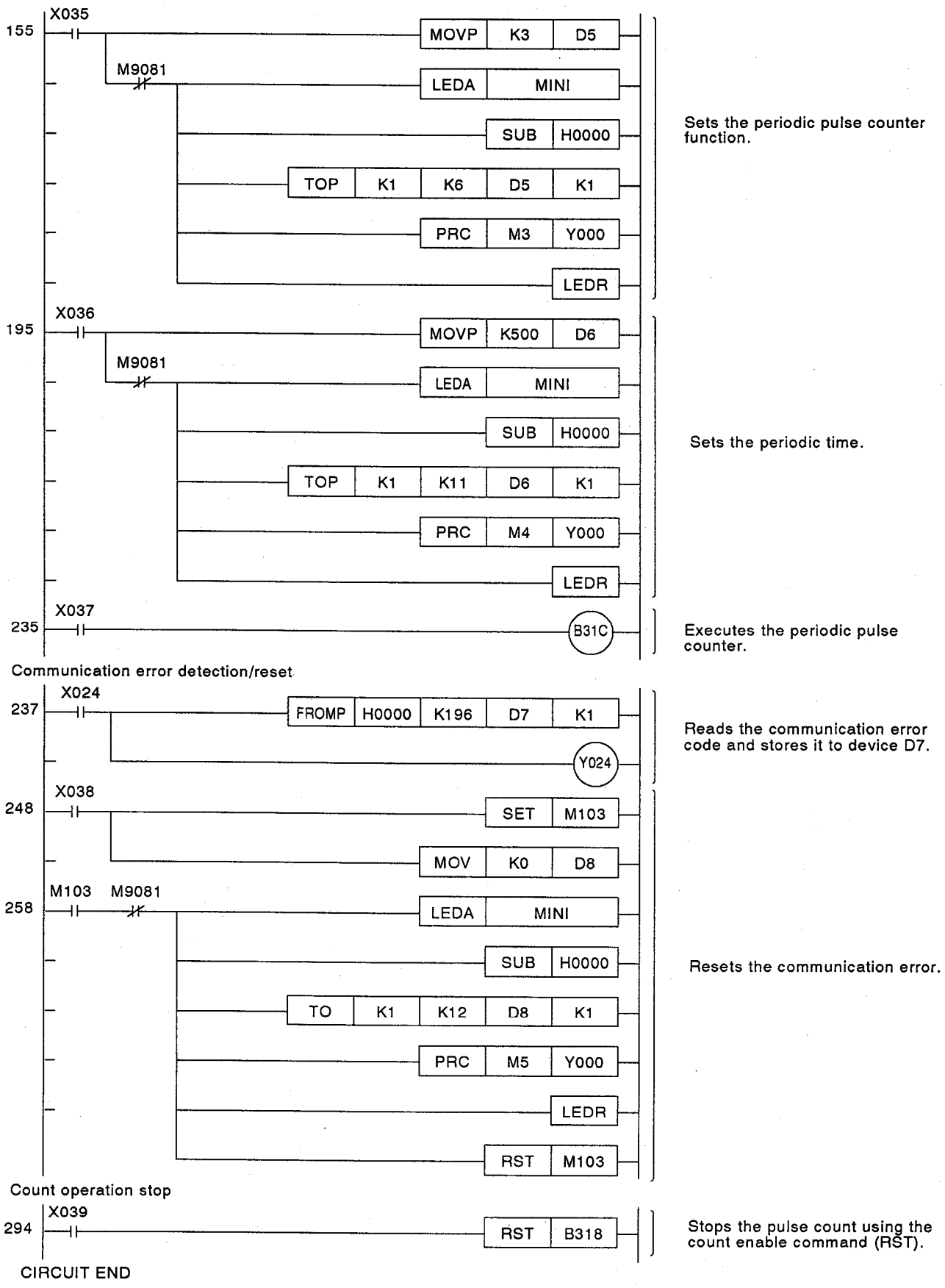



Reads the present value and stores it to devices D1 to D2.

Periodic pulse counter command




Reads the counter value and stores it to devices D3 to D4.


155
X035
MOVP K3 D5
M9081
LEDA MINI
SUB H0000
TOP K1 K6 D5 K1
PRC M3 Y000
LEDR
Sets the periodic pulse counter function.
195
X036
MOVP K500 D6
M9081
LEDA MINI
SUB H0000
TOP K1 K11 D6 K1
PRC M4 Y000
LEDR
Sets the periodic time.
235
X037
B31C
Executes the periodic pulse counter.
Communication error detection/reset
237
X024
FROMP H0000 K196 D7 K1
Y024
Reads the communication error code and stores it to device D7.
248
X038
SET M103
MOV K0 D8
258
M103 M9081
LEDA MINI
SUB H0000
TO K1 K12 D8 K1
PRC M5 Y000
LEDR
RST M103
Resets the communication error.
Count operation stop
294
X039
RST B318
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 6.5.7 Count disable function programming example

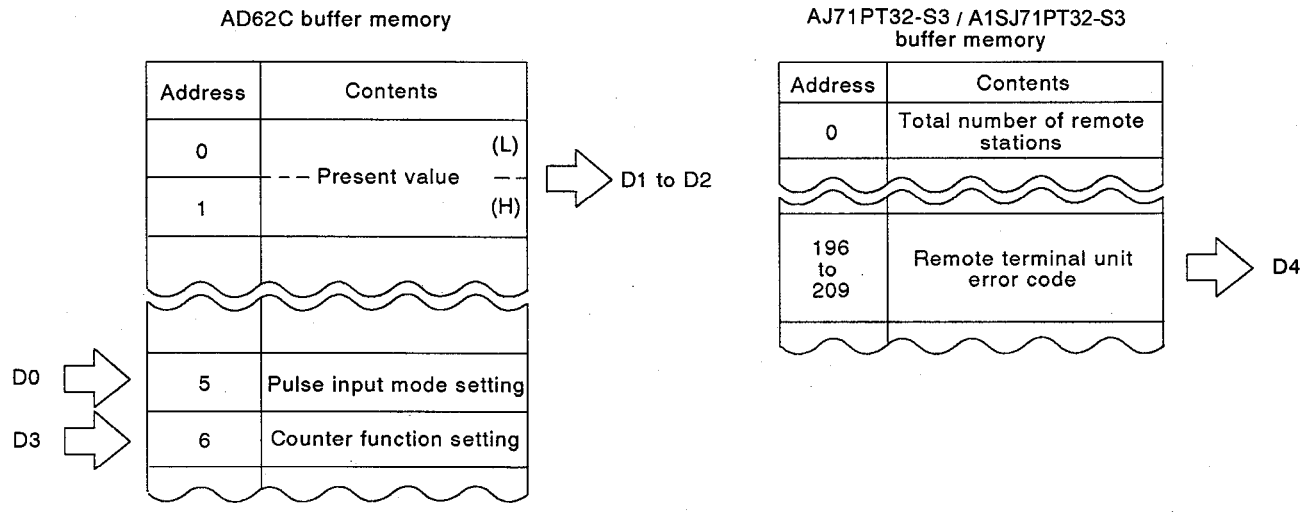
Create a program to count 2-phase pulses multiplied by one and to execute the count disable function.

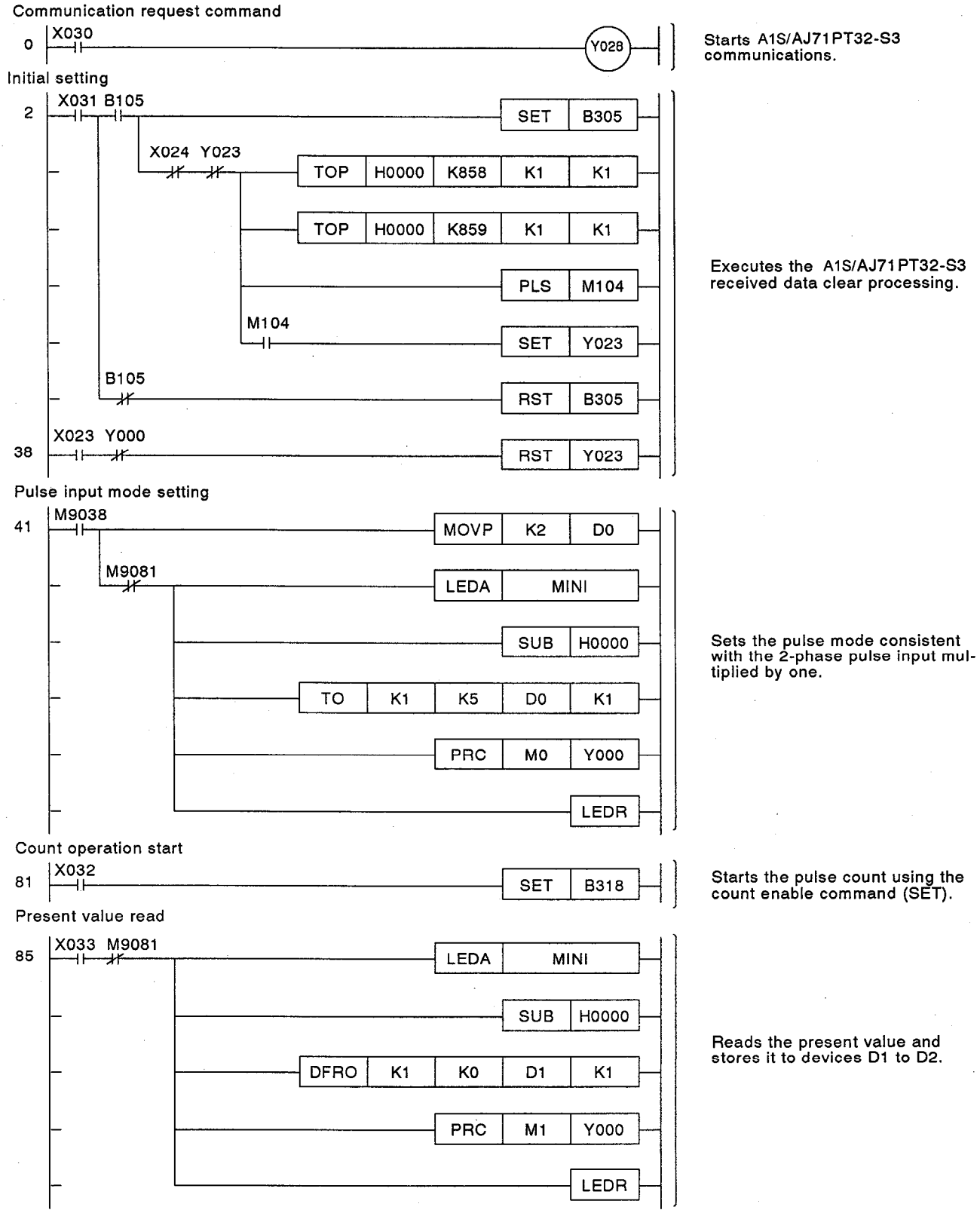
**[Devices to be used]**

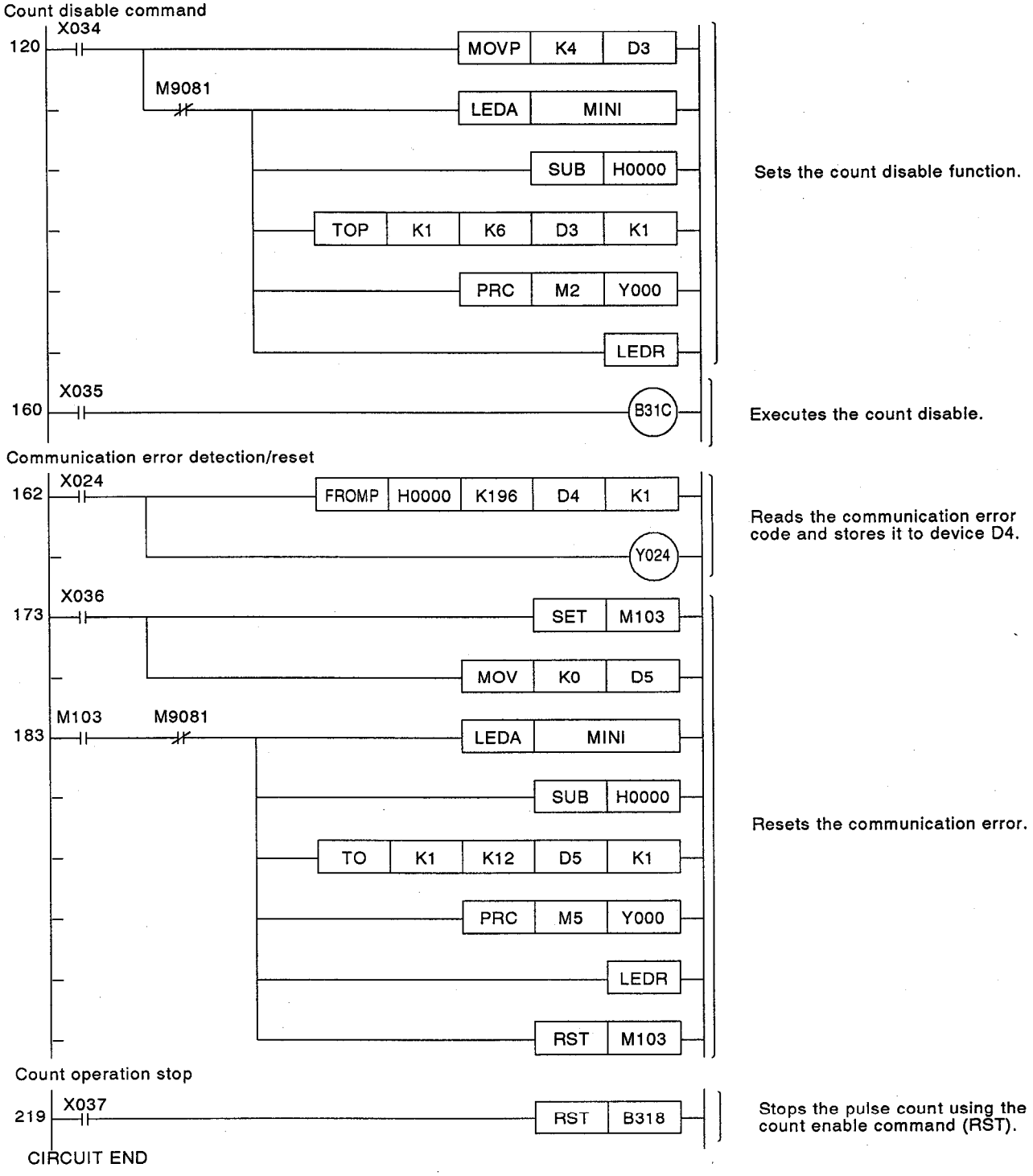
(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Communication request command.....X30
(c) Initial setting execute command.....X31
(d) Count operation start command.....X32
(e) Present value read command.....X33
(f) Count disable function setting command.....X34
(g) Count disable start command.....X35
(h) Communication error reset command.....X36
(i) Count operation stop command.....X37

(2) Relationship between the data register (D0 to D4) and the buffer memory




Communication request command
0
X030
Y028
Starts A1S/AJ71PT32-S3 communications.
Initial setting
2
X031 B105
SET B305
X024 Y023
TOP H0000 K858 K1 K1
TOP H0000 K859 K1 K1
PLS M104
M104
SET Y023
B105
RST B305
38
X023 Y000
RST Y023
Executes the A1S/AJ71PT32-S3 received data clear processing.
Pulse input mode setting
41
M9038
MOVP K2 D0
M9081
LEDA MINI
SUB H0000
TO K1 K5 D0 K1
PRC M0 Y000
LEDR
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.
Count operation start
81
X032
SET B318
Starts the pulse count using the count enable command (SET).
Present value read
85
X033 M9081
LEDA MINI
SUB H0000
DFRO K1 K0 D1 K1
PRC M1 Y000
LEDR
Reads the present value and stores it to devices D1 to D2.




Sets the count disable function.

Executes the count disable.

Reads the communication error code and stores it to device D4.

Resets the communication error.

Stops the pulse count using the count enable command (RST).

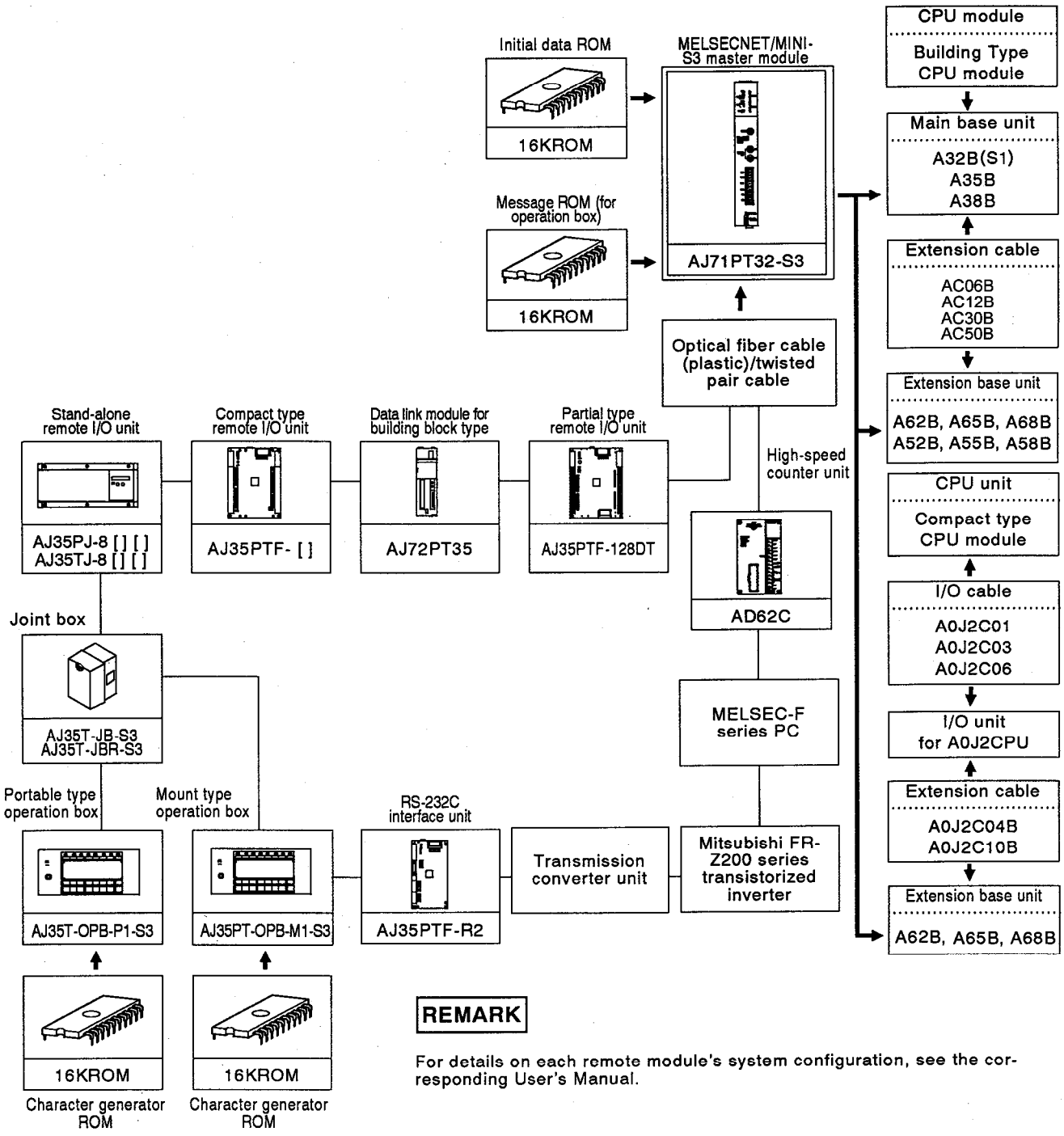
# 7. ACPU AND AJ71PT32-S3 (A1S/A2SCPU AND A1SJ71PT32-S3) LINKING

- See Section 5 for linking with an A2CCPU.
- See Section 6 for linking with an AnSH/A2AS/A2USH/Q2AS(H)/AnA/AnU/QnACPU. (Links described in this section can also be used.)
- This section also explains methods for linking with an A1SCPU and A1SJ71PT32-S3.

## 7.1 System Configuration When Linking with an ACPU and AJ71PT32-S3

### 7.1.1 Overall configuration

The overall configuration of the AD62C using MELSECNET/MINI-S3 is shown below.




**REMARK**

For details on each remote module's system configuration, see the corresponding User's Manual.

### 7.1.2 Applicable systems

The AD62C can be linked to the following CPUs via the AJ71PT32-S3 master module.

| Applicable models | |
|---|---|
| A0J2HCPU | A0J2CPU (P23/R23) |
| A1NCPU (P21/R21) | A1CPU (P21/R21) |
| A2NCPU (P21/R21) | A2CPU (P21/R21) |
| A2NCPU (P21/R21)-S1 | A2CPU (P21/R21)-S1 |
| A3NCPU (P21/R21) | A3CPU (P21/R21) |
| A3HCPU (P21/R21) | |
| A3MCPU (P21/R21) | |
| A2ACPU (P21/R21) | |
| A2ACPU (P21/R21)-S1 | |
| A3ACPU (P21/R21) | |

The AJ71PT32-S3 master module can be loaded into any slot and linked with the AD62C with the exception of (1) and (3) below. The number of device panels is unlimited.

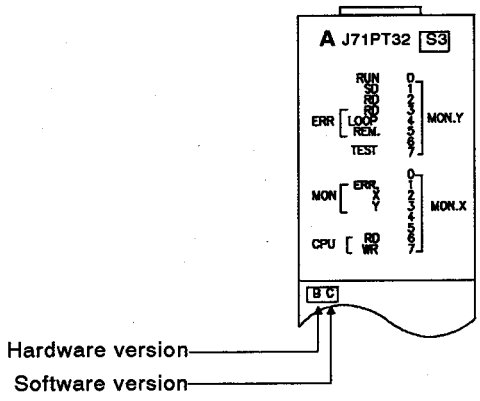
(1) If the AD62C is loaded into an extension base unit (A52B, A55B, A58B) without a power supply module, the power capacity may be insufficient. Avoid loading as long as possible. If it is necessary to load, select power supply modules and extension cables with the power capacity of the main base unit's power supply module and extension cable voltage drops in mind. For details, see each CPU User's Manual.

(2) The AJ71PT32-S3 master module cannot be loaded into the last slot of the 7th extension of the A3CPU (P21/R21).

(3) In a MELSECNET data link system, loading is possible to both a master station and a local station. The AJ71PT32-S3 master module cannot be used for a remote I/O station.

### 7.1.3 Precautions when constructing the system

(1) The software version shown below on the front of the AJ71PT32-S3 module must be "C" or later to use the AD62C. A module of software version "A, B" or "no" software version indication cannot be used.




(2) When using the AD62C in the MELSECNET/MINI-S3 data link system, use twisted pair cables.

(3) Since each AD62C occupies 4 stations (a total of 32 I/O points), be careful when assigning I/O signals.

(4) When using the AD62C, set the AJ71PT32-S3 as follows.

(a) Set the "jumper for mode selection" of the AJ71PT32-S3 to the extension mode (occupying 48 I/O points) of "48."

(b) Create the initial data ROM for the AJ71PT32-S3 extension mode (occupying 48 I/O points) by the SW0GP-MINIP and install it. For remote terminal data setting at the creation of the initial ROM, set the AD62C protocol to

4: MINI STANDARD PROTOCOL.

(c) For details, see each of the manuals below.

- AJ71PT32-S3 type MELSECNET/MINI-S3 Master Module User's Manual
- SW0GP-MINIP Operating Manual

(5) The AD62C requires a 24 VDC power supply.

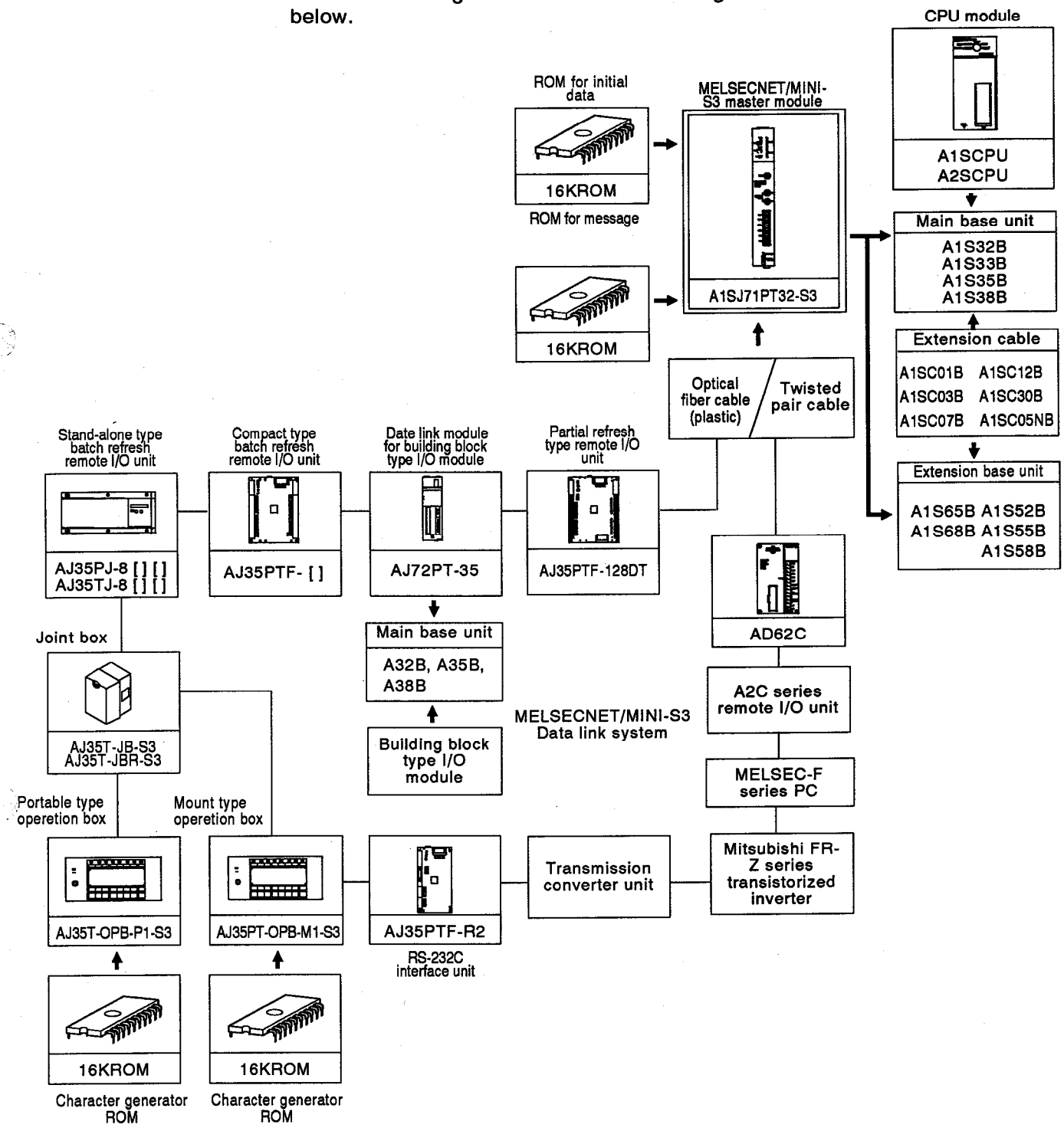
When supplying power from one power supply to multiple AD62Cs or to the link I/O modules, select cables and perform wiring taking voltage drops into consideration.

To calculate the receiving port voltage, see **[REMARK]** in Section 5.1.2.

## 7.2 System Configuration When Linking with an A1S/A2SCPU and A1SJ71PT32-S3

### 7.2.1 Overall configuration

The overall configuration of the AD62C using MELSECNET/MINI-S3 is shown below.



### 7.2.2 Applicable A-Series system

The AD62C can be linked to the following PLC CPU via the A1SJ71PT32-S3 master module.

| Applicable models | |
|---|---|
| A1SCPU | A2SCPU |

The A1SJ71PT32-S3 master module can be installed into any slot with the exception of item (1) below.

A maximum of five modules can be installed in the extension mode (occupying 48 points).

(1) If the A1SJ71PT32-S3 master module is installed in an extension base unit without a power supply (A1S52B, A1S55B, or A1S58B extension base unit), power shortages can happen.

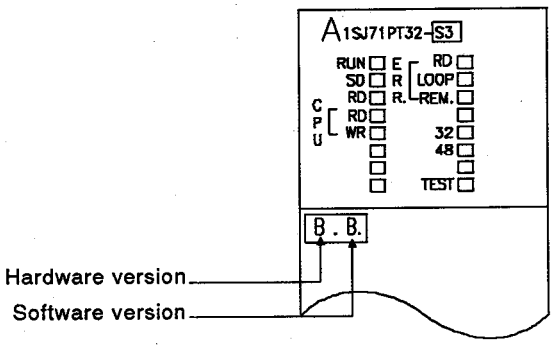
Therefore, use of these units should be avoided.

If this installation cannot be avoided, take the power supply capacity of the main base unit and the voltage drop of the extension cable into consideration when selecting the module and extension cable.

(The user's manual of the corresponding CPU module gives details.)

### 7.2.3 Precautions when constructing the system

(1) The software version shown below on the front of the A1SJ71PT32-S3 module must be "B" or later to use the AD62C.




(2) When using the AD62C in the MELSECNET/MINI-S3 data link system, use twisted pair cables.

(3) Since each AD62C occupies 4 stations (a total of 32 I/O points), be careful when assigning I/O signals.

(4) When using the AD62C, set the A1SJ71PT32-S3 as follows.

(a) Set the "jumper for mode selection" of the A1SJ71PT32-S3 to the extension mode (occupying 48 I/O points) of "48".

(b) Create the initial data ROM for the A1SJ71PT32-S3 extension mode (occupying 48 I/O points) using the SW0GP-MINIP and install it. For remote terminal data setting at the creation of the initial ROM, set the AD62C protocol to

4: MINI STANDARD PROTOCOL.

(c) For details, see each of the manuals below.

- A1SJ71PT32-S3 type MELSECNET/MINI-S3 Master Module User's Manual
- SW0GP-MINIP Operating Manual

(5) The AD62C requires 24 VDC power supply.

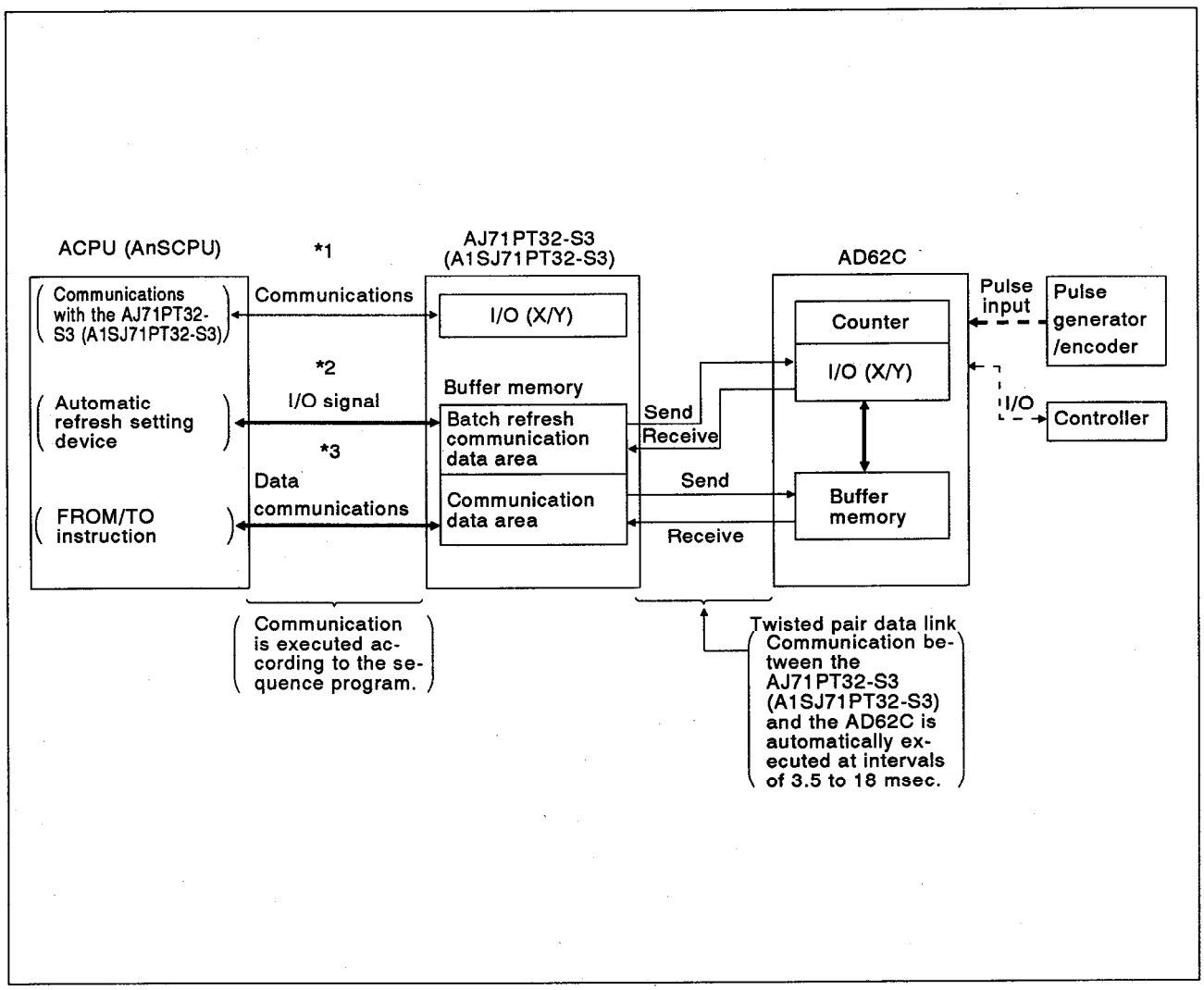
When supplying power from one power supply to multiple AD62Cs or to the link I/O modules, select cables and perform wiring taking voltage drops into consideration.

To calculate the receiving port voltage, see **[REMARK]** in Section 5.1.2.

## 7.3 Data Communication Processing

### 7.3.1 Communication method

(1) Communication between the AD62C and the PLC CPU is executed via the A1S/AJ71PT32-S3's buffer memory.
The communication method is shown below.




*1: I/O signal communication between the ACPU and the AJ71PT32-S3 (the AnSCPU and A1SJ71PT32-S3) is executed. (I/O communication processing of communication start, error detection, etc.)

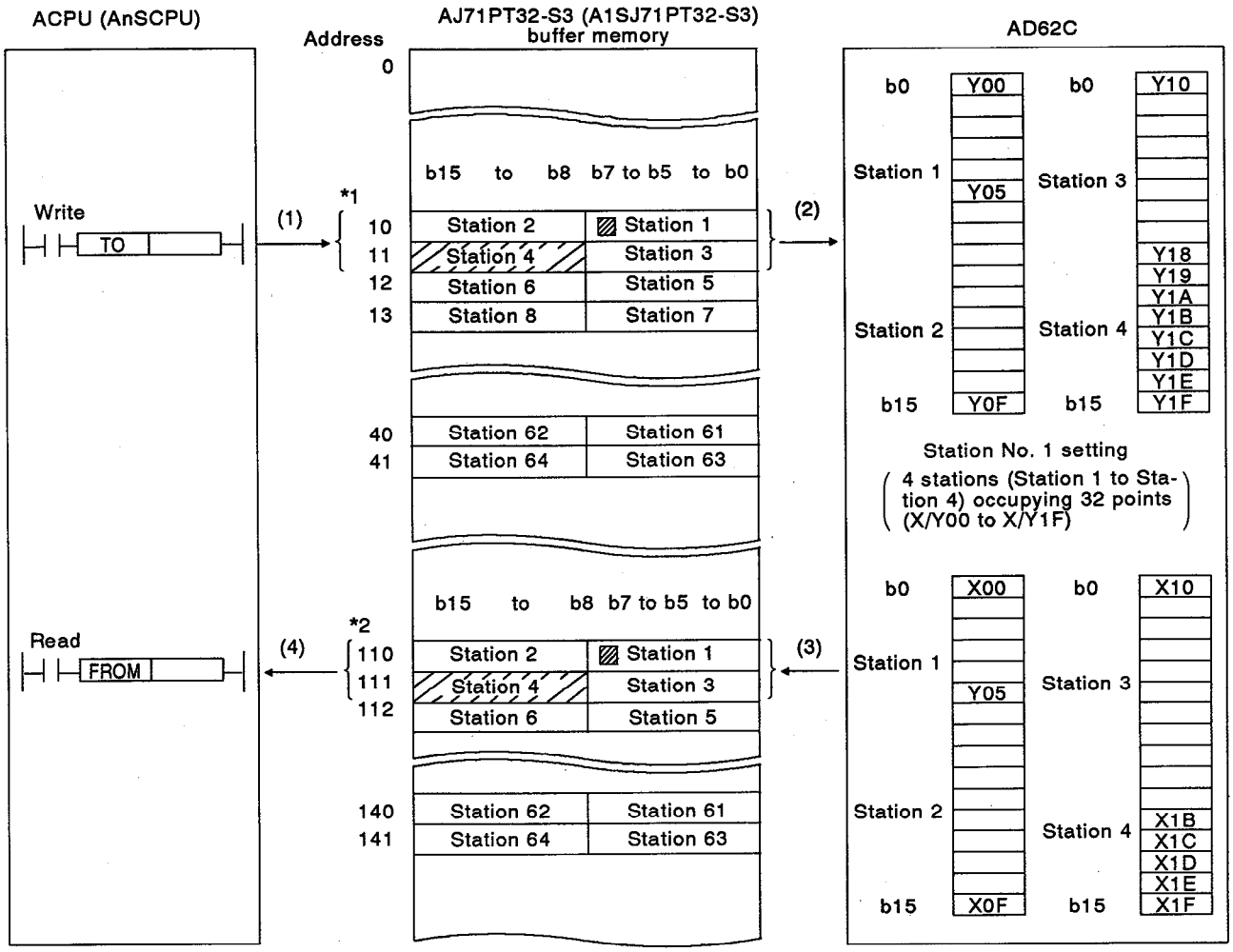
*2: Input signal communication between the ACPU and the AJ71PT32-S3 (the AnSCPU and A1SJ71PT32-S3), and between the AJ71PT32-S3 and the AD62C (the A1SJ71PT32-S3 and the AD62C) is executed. For details, see "I/O signal processing" in Section 7.2.2.

*3: Data communication between the ACPU and the AJ71PT32-S3 (the AnSCPU and the A1SJ71PT32-S3), and between the AJ71PT32-S3 and the AD62C (the A1SJ71PT32-S3 and the AD62C) is executed. For details, see "buffer memory data processing" in Section 7.2.3.

### 7.3.2 I/O signal processing

I/O signals (X,Y) of the AD62C to the PLC CPU are processed via the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory.

(1) The I/O signal processing method between the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory and the AD62C is shown below. (The AD62C station number is set to 01.)




*1: Addresses 10 to 41 ····· Batch refresh send data area
*2: Addresses 110 to 141 ···· Batch refresh received data area

(a) Output (Y) signal (communication order from (1) to (2))

- By using the sequence program's TO instruction, the ACPU (AnSCPU) writes data to the AJ71PT32-S3 (A1SJ71PT32-S3) batch refresh send data area.
- The AJ71PT32-S3 (A1SJ71PT32-S3) writes the send data to the AD62C output signal area.

(b) Input (X) signal (communication order from (3) to (4))

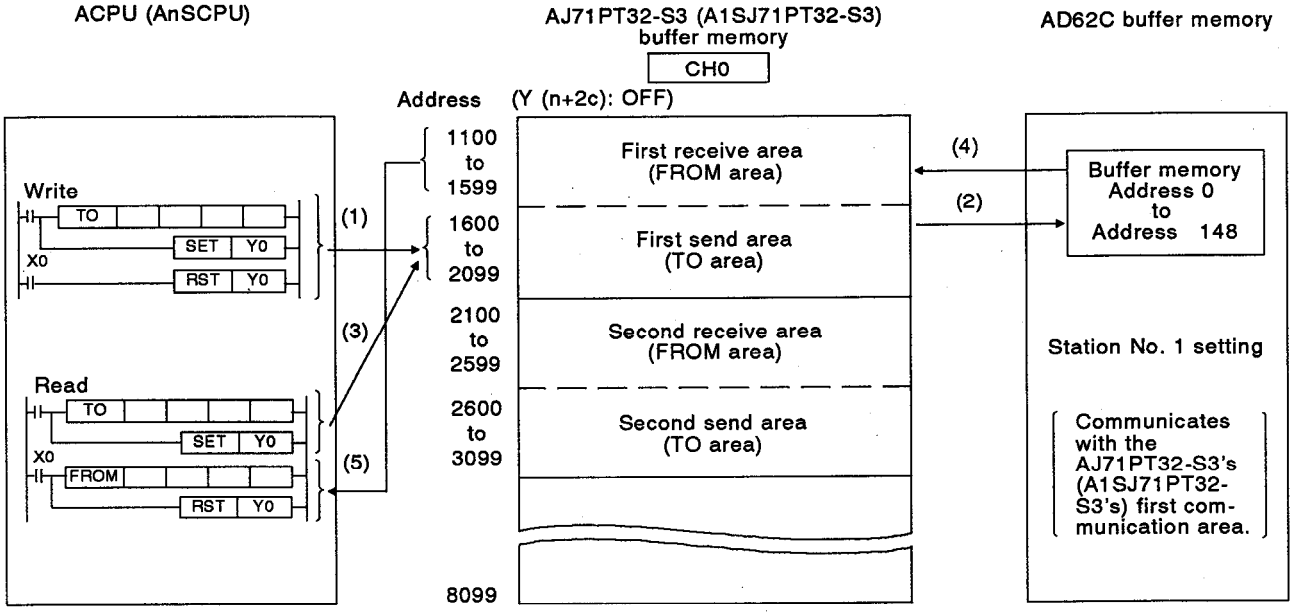
- The AJ71PT32-S3 (A1SJ71PT32-S3) always communicates with the AD62C and stores the AD62C input signal data in the batch refresh received data area.
- By using the sequence program's FROM instruction, the ACPU (AnSCPU) reads data from the AJ71PT32-S3 (A1SJ71PT32-S3) received data area.

### 7.3.3 Buffer memory data processing

The AD62C buffer memory data is processed by a sequence program via the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory.

(1) The AJ71PT32-S3 (A1SJ71PT32-S3) and AD62C buffer memory data processing method is shown below.

- The AD62C station number is set to 01.
- The AD62C is set to the first communication area of the remote terminal unit by the AJ71PT32-S3 (A1SJ71PT32-S3) initial ROM.



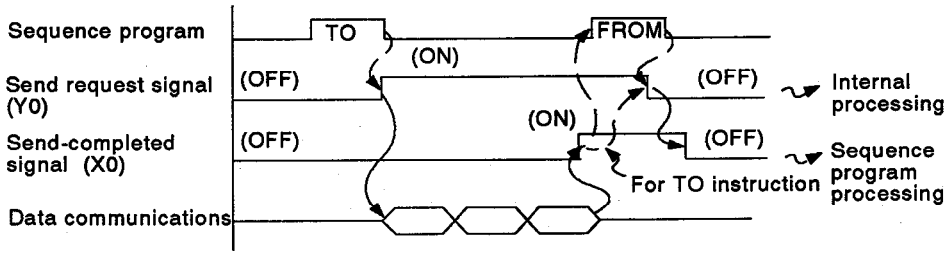

(a) Write to the AD62C buffer memory (communication order from (1) to (2))

- By using the sequence program's TO instruction, the ACPU (AnSCPU) writes to the AJ71PT32-S3 (A1SJ71PT32-S3) send area.
- The AJ71PT3-S3 (A1SJ71PT32-S3) writes to the AD62C buffer memory when the send request signal (Y0) is set.

(b) Read from the AD62C buffer memory (communication order from (3),(4) to (5))

- By using the sequence program's TO instruction, the ACPU (AnSCPU) writes (read request, head address, number of words to be read) to the AJ71PT32-S3 (A1SJ71PT32-S3) send area.
- With the send request signal (Y0) set, the AJ71PT32-S3 (A1SJ71PT32-S3) reads the data of the specified number of words to be read from the AD62C buffer memory specified head address according to the send data by the TO instruction. Then the AJ71PT32-S3 (A1SJ71PT32-S3) stores the data to the receive area and turns ON the send-completed signal (X0).
- The received data are read from the AJ71PT32-S3 (A1SJ71PT32-S3) receive area by the sequence program's FROM instruction when the send-completed signal (X0) is ON.

(c) Processing time




### 7.3.4 Processing time

The processing time required to write data to and read data from the AD62C buffer memory is shown below.

| Items | Max. Processing Time |
|---|---|
| Data write | [t msec x (number of data words)] + *2 [(t msec x 5) + 80 msec] |
| Data read | *2: Total value of the AD62C internal processing time and the PC CPU processing time |

"t" is the I/O refresh time. It varies according to the number and type of connected remote module stations. Calculation of the I/O refresh time is shown below.

| Mode | Operation Mode Settings | I/O Refresh Times (msec) |
|---|---|---|
| Extension mode (48 points) | Automatic return enable (0) | t = 0.66 + (0.044 x R) + (0.95 x B) + (0.95 x T) |
| | Automatic return disable (1) | t = 0.54 + (0.058 x R) + (0.25 x B) + (0.95 x T) |
| | Communication stop at error detection (2) | t = 0.54 + (0.051 x R) + (0.25 x B) + (0.95 x T) |

R: Total number of remote stations
B: Number of AJ35PTF-128DTs
T: Number of remote terminal units

**POINTS**

(1) Count start/stop by external input, preset, and the counter coincidence signal by external output respond in less than 10 msec.

(2) To increase the processing time responsiveness of sequence operations, use external I/O signals.

## 7.4 I/O Signals To/From PLC CPU

### 7.4.1 AD62C I/O signals

AD62C I/O signals to/from PLC CPU are shown below. The following I/O device numbers apply when the AD62C's station number is 01 (X/Y00 to X/Y1F).

(1) Input signals (signal direction: AD62C → PLC CPU)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| X00 to X04 | (Unusable) | ——— |
| X05 | Reset status detection | • Latched to ON when power to the AD62C is turned ON or the reset switch is turned ON.<br>• Switches OFF when the reset status detection reset signal (Y05) switches from OFF to ON. |
| X06 to X1A | (Unusable) | ——— |
| X1B | Fuse blown detection | • Switches ON when a fuse is blown or when external power for the limit switch output is turned OFF. |
| X1C | Sampling/periodic counter ON/OFF flag | • Switches ON when the sampling/periodic counter function is executed. |
| X1D | Limit switch output READY flag | • Set when limit switch output is enabled.<br>• Reset when the dog setting has an error. |
| X1E | External preset request detection flag | • Latched to ON when an external preset request is given.<br>• Switches OFF when the external preset request detection signal reset command (Y1E) switches from OFF to ON. |
| X1F | Multiple-dog setting error detection | • Latched to ON when a multiple-dog setting error is detected in the AD62C<br>• Switches OFF when the multiple-dog setting error detection reset command (Y1E) switches from OFF to ON. |

(2) Output signals (signal direction: PLC CPU → AD62C)

| Device Nos. | Signals | Operating Conditions |
|---|---|---|
| Y00 to Y04 | (Unusable) | ——— |
| Y05 | Reset status detection reset | • When this signal switches from OFF to ON, the reset status detection signal (X05) switches OFF.<br>• Switches OFF when (X05) switches OFF. |
| Y06 to Y17 | (Unusable) | ——— |
| Y18 | Count enable command | • Enables counting operations of an AD62C when switched ON. |
| Y19 | Decremental count command | • Valid only in the direction input mode and when a 1-phase pulse is input.<br>• Counts decrementally when this signal is ON.<br>• Cannot be used along with an external input (øB). |
| Y1A | Preset command | • Executes preset operations. |
| Y1B | Ring counter command | • Starts the ring counter. |
| Y1C | Counter function selection start command | • Selects the counter function. |
| Y1D | Limit switch output enable command | • Enables limit switch output (8 channels in batch).<br>• When (Y1D) is OFF, this command is not output and all channels are OFF. |
| Y1E | External preset command detection reset command | • When this signal switches from OFF to ON, the external preset request detection flag (X1E) switches OFF.<br>• Switches OFF when (X1E) switches OFF. |
| Y1F | Multiple-dog setting error detection reset | • When this signal switches from OFF to ON, the multiple-dog setting error detection signal (X1F) switches OFF and the error codes of the AD62C buffer memory are reset.<br>• Switches OFF after (X1F) switches OFF. |

### 7.4.2 AJ71PT32-S3 (A1SJ71PT32-S3) I/O signals

I/O signals between the AJ71PT32-S3 (A1SJ71PT32-S3) and the PLC CPU in the extension mode are used when accessing the AD62C buffer memory.

For details about the I/O signals, see the MELSECNET/MINI-S3 Master Module User's Manual.

The list of I/O signals in the extension mode is shown below.

The "n" in the Device Nos. column of the table is the master module head I/O number. It is determined by the number of I/O points of the I/O modules loaded into the master module's front slot and by the master module's position.

( Example: When the master module head I/O number is "X/Y20"
X(n+0) to X(n+2F) = X20 to X4F
Y(n+0) to Y(n+2F) = Y20 to Y4F )

**Table 7.1 I/O Signal List in the Extension Mode**

| Device Nos. | Signals | | Device Nos. | Signals | |
|---|---|---|---|---|---|
| X(n+0) | Send-completed signal | For remote terminal unit No.1 | Y(n+0) | Send-completed signal | For remote terminal unit No.1 |
| X(n+1) | Read request signal | | Y(n+1) | Read request signal | |
| X(n+2) | Send-completed signal | For remote terminal unit No.2 | Y(n+2) | Send-completed signal | For remote terminal unit No.2 |
| X(n+3) | Read request signal | | Y(n+3) | Read request signal | |
| X(n+4) | Send-completed signal | For remote terminal unit No.3 | Y(n+4) | Send-completed signal | For remote terminal unit No.3 |
| X(n+5) | Read request signal | | Y(n+5) | Read request signal | |
| X(n+6) | Send-completed signal | For remote terminal unit No.4 | Y(n+6) | Send-completed signal | For remote terminal unit No.4 |
| X(n+7) | Read request signal | | Y(n+7) | Read request signa | |
| X(n+8) | Send-completed signal | For remote terminal unit No.5 | Y(n+8) | Send-completed signal | For remote terminal unit No.5 |
| X(n+9) | Read request signal | | Y(n+9) | Read request signal | |
| X(n+A) | Send-completed signal | For remote terminal unit No.6 | Y(n+A) | Send-completed signal | For remote terminal unit No.6 |
| X(n+B) | Read request signal | | Y(n+B) | Read request signal | |
| X(n+C) | Send-completed signal | For remote terminal unit No.7 | Y(n+C) | Send-completed signal | For remote terminal unit No.7 |
| X(n+D) | Read request signal | | Y(n+D) | Read request signal | |
| X(n+E) | Send-completed signal | For remote terminal unit No.8 | Y(n+E) | Send-completed signal | For remote terminal unit No.8 |
| X(n+F) | Read request signal | | Y(n+F) | Read request signal | |
| X(n+10) | Send-completed signal | For remote terminal unit No.9 | Y(n+10) | Send-completed signal | For remote terminal unit No.9 |
| X(n+11) | Read request signal | | Y(n+11) | Read request signal | |
| X(n+12) | Send-completed signal | For remote terminal unit No.10 | Y(n+12) | Send-completed signal | For remote terminal unit No.10 |
| X(n+13) | Read request signal | | Y(n+13) | Read request signal | |
| X(n+14) | Send-completed signal | For remote terminal unit No.11 | Y(n+14) | Send-completed signal | For remote terminal unit No.11 |
| X(n+15) | Read request signal | | Y(n+15) | Read request signal | |
| X(n+16) | Send-completed signal | For remote terminal unit No.12 | Y(n+16) | Send-completed signal | For remote terminal unit No.12 |
| X(n+17) | Read request signal | | Y(n+17) | Read request signal | |
| X(n+18) | Send-completed signal | For remote terminal unit No.13 | Y(n+18) | Send-completed signal | For remote terminal unit No.13 |
| X(n+19) | Read request signal | | Y(n+19) | Read request signal | |
| X(n+1A) | Send-completed signal | For remote terminal unit No.14 | Y(n+1A) | Send-completed signal | For remote terminal unit No.14 |
| X(n+1B) | Read request signal | | Y(n+1B) | Read request signal | |
| X(n+1C) | (Unusable) | | Y(n+1C) | (Unusable) | |
| X(n+1D) | | | Y(n+1D) | | |
| X(n+1E) | | | Y(n+1E) | | |
| X(n+1F) | | | Y(n+1F) | | |
| X(n+20) | Hardware fault | | Y(n+20) | | |
| X(n+21) | MINI-S3 link communications in progress | | Y(n+21) | | |
| X(n+22) | (Unusable) | | Y(n+22) | | |
| X(n+23) | Received data clear complete (for the AJ35PTF-R2) | | Y(n+23) | Received data clear request (for the AJ35PTF-R2) | |
| X(n+24) | Remote terminal unit error detection | | Y(n+24) | Remote terminal unit error detection reset | |
| X(n+25) | Test mode | | Y(n+25) | (Unusable) | |
| X(n+26) | MINI-S3 link error detection | | Y(n+26) | | |
| X(n+27) | MINI-S3 link communications error | | Y(n+27) | | |
| X(n+28) | ROM error | | Y(n+28) | MINI-S3 link communication start | |
| X(n+29) | (Unusable) | | Y(n+29) | (Unusable) | |
| X(n+2A) | | | Y(n+2A) | FROM/TO instruction response specification | |
| X(n+2B) | | | Y(n+2B) | Error station data clear specification | |
| X(n+2C) | | | Y(n+2C) | Buffer memory channel switching | |
| X(n+2D) | | | Y(n+2D) | Error reset | |
| X(n+2E) | | | Y(n+2E) | (Unusable) | |
| X(n+2F) | | | Y(n+2F) | | |

## 7.5 Buffer Memory Assignments

### 7.5.1 AD62C buffer memory

Table 7.2 shows the buffer memory assignments of the AD62C.

The next page gives detailed information about the settings of buffer memory addresses 14 to 149.

Initial values are set in the buffer memory when power to the AD62C is turned ON or when the AD62C is reset.

The contents of the buffer memory can be read/written using a FROM/TO instruction in an AD62C sequence program.

**Table 7.2 Buffer Memory Assignments**

| Addresses | Setting Contents | Initial Values | Read/Write | Reference Sections |
|---|---|---|---|---|
| 0 | Present value (L) | 0 | Read only | 4.3 |
| 1 | Present value (H) | | | |
| 2 | Counter function selection count value (L) | 0 | | 3.5.1 |
| 3 | Counter function selection count value (H) | | | |
| 4 | Limit switch output state flag (CH 1 to CH 8) | 0 | | 3.4 |
| 5 | Pulse input mode setting | 0 | Read/write possible | 4 |
| 6 | Counter function selection setting | 0 | | 3.5 |
| 7 | Preset value setting (L) | 0 | | 3.2 |
| 8 | Preset value setting (H) | | | |
| 9 | Ring counter value setting (L) | 1024 | | 3.3 |
| 10 | Ring counter value setting (H) | | | |
| 11 | Sampling/periodic time setting | 1 | | 3.5.4 and 3.5.5 |
| 12 | Communication error code | 0 | | 9.1 |
| 13 | Multiple-dog setting error code | 0 | | |
| 14 to 30 | CH 1 limit switch output data setting | 0 | Read/write possible | 3.4 |
| 31 to 47 | CH 2 limit switch output data setting | 0 | | |
| 48 to 64 | CH 3 limit switch output data setting | 0 | | |
| 65 to 81 | CH 4 limit switch output data setting | 0 | | |
| 82 to 98 | CH 5 limit switch output data setting | 0 | | |
| 99 to 115 | CH 6 limit switch output data setting | 0 | | |
| 116 to 132 | CH 7 limit switch output data setting | 0 | | |
| 133 to 149 | CH 8 limit switch output data setting | 0 | | |

The following gives detailed information about the settings of buffer memory addresses 14 to 149 (limit switch output data setting of CH 1 to CH 8)

| Setting Contents | | Buffer Memory Addresses | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 14 to 30 CH.1 | 31 to 47 CH.2 | 48 to 64 CH.3 | 65 to 81 CH.4 | 82 to 98 CH.5 | 99 to 115 CH.6 | 116 to 132 CH.7 | 133 to 149 CH.8 |
| Number of multiple dogs for CH [ ] | | 14 | 31 | 48 | 65 | 82 | 99 | 116 | 133 |
| ·· CH [ ] Dog 0 ON address | (L) | 15 | 32 | 49 | 66 | 83 | 100 | 117 | 134 |
| | (H) | 16 | 33 | 50 | 67 | 84 | 101 | 118 | 135 |
| ·· CH [ ] Dog 0 OFF address | (L) | 17 | 34 | 51 | 68 | 85 | 102 | 119 | 136 |
| | (H) | 18 | 35 | 52 | 69 | 86 | 103 | 120 | 137 |
| ·· CH [ ] Dog 1 ON address | (L) | 19 | 36 | 53 | 70 | 87 | 104 | 121 | 138 |
| | (H) | 20 | 37 | 54 | 71 | 88 | 105 | 122 | 139 |
| ·· CH [ ] Dog 1 OFF address | (L) | 21 | 38 | 55 | 72 | 89 | 106 | 123 | 140 |
| | (H) | 22 | 39 | 56 | 73 | 90 | 107 | 124 | 141 |
| ·· CH [ ] Dog 2 ON address | (L) | 23 | 40 | 57 | 74 | 91 | 108 | 125 | 142 |
| | (H) | 24 | 41 | 58 | 75 | 92 | 109 | 126 | 143 |
| ·· CH [ ] Dog 2 OFF address | (L) | 25 | 42 | 59 | 76 | 93 | 110 | 127 | 144 |
| | (H) | 26 | 43 | 60 | 77 | 94 | 111 | 128 | 145 |
| ·· CH [ ] Dog 3 ON address | (L) | 27 | 44 | 61 | 78 | 95 | 112 | 129 | 146 |
| | (H) | 28 | 45 | 62 | 79 | 96 | 113 | 130 | 147 |
| ·· CH [ ] Dog 3 OFF address | (L) | 29 | 46 | 63 | 80 | 97 | 114 | 131 | 148 |
| | (H) | 30 | 47 | 64 | 81 | 98 | 115 | 132 | 149 |

[ ] = Channel number displayed

### 7.5.2 AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory

There are communication (send/receive) data addresses for the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory according to dedicated read/write instructions between the AJ71PT32-S3 (A1SJ71PT32-S3) and the PLC CPU.
The assignment of buffer memory addresses which automatically communicate with the AD62C is shown below.
For buffer memory details, see the MELSECNET/MINI-S3 Master Module User's Manual.

| | Address (decimal) | | Contents | PC CPU Read/write Enable/disable |
|---|---|---|---|---|
| | 0 | Total number of remote stations | The range of the station numbers of all connected remote modules is set. | Read/write enable |
| | 1 | Number of retries | The number of retries at communication error occurrence is set. | |
| | | (Unused) | ——— | |
| | 4 | Line error check | Used to confirm line faulty areas. | |
| | | (Unused) | ——— | |
| *1 | 10 to 41 | Batch refresh send data | Data output to the batch refresh type remote I/O module are written. | |
| | | (Unused) | ——— | ——— |
| | 70 to 77 | Remote module's card data | Each connected remote module's type is stored. | Read only |
| | | (Unused) | ——— | ——— |
| | 90 to 93 | Accumulation faulty station detection | Station numbers of remote modules which are in communication error are stored. (Detection status is retained until reset.) | Read/write enable |
| | | (Unused) | ——— | ——— |
| | 100 to 103 | Faulty station detection | Station number of remote module which is in communication error is stored. (Communication status is always updated.) | Read only |
| | | (Unused) | ——— | |
| | 107 | Communication error code | The cause of the MINI-S3 link communication error signal being ON is stored. | |
| | 108 | Error detection code | The accumulated number of times the MINI-S3 link error detection turns ON is stored. | |
| | | (Unused) | ——— | |
| *2 | 110 to 141 | Batch refresh received data | Input data from batch refresh type remote I/O module are stored. | |
| | | (Unused) | ——— | |
| | 160 | Line error retry counter | The number of executions of retry processing when communication with all remote modules is disabled by line error is stored. | |
| | 161 to 192 | Retry counter | The number of times retry processing to faulty stations is executed is stored. | |
| | | (Unused) | ——— | |
| | 195 | Remote terminal unit faulty stations | The station number of the remote terminal unit with which an error has occurred is stored. | |
| *3 | 196 to 209 | Remote terminal module error code | The cause of the remote terminal unit error detection signal [X (n + 24)] being ON is stored. | |
| | | (Unused) | ——— | ——— |
| | 250 to 282 | Partial refresh station | Partial refresh type remote I/O module station number and specification of the number of digits are written. | Read/write enable |
| | | (Unused) | ——— | |
| | 300 to 363 | Partial refresh send data | Data output to the partial refresh type remote I/O module are written. | |
| | | (Unused) | ——— | |
| | 598 | Partial refresh accumulation input error detection | Partial refresh type remote I/O module's input data received faulty station is stored. (Detection status is retained until reset.) | |
| | 599 | Partial refresh input error detection | Partial refresh type remote I/O module's input data received faulty station is stored. (Communication status is always undated.) | |
| | 600 to 663 | Partial refresh received data | Partial refresh type remote I/O module's input data are stored. | Read only |

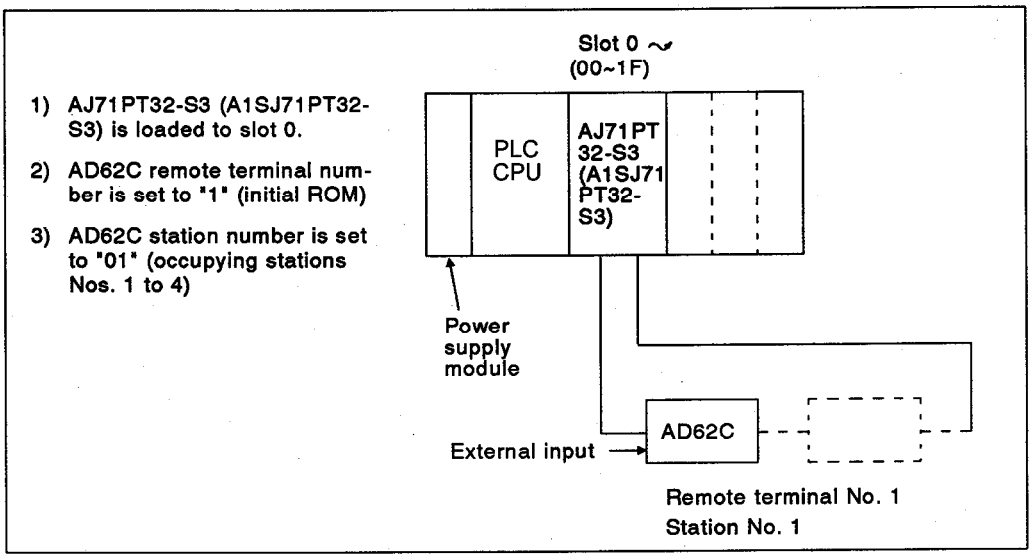
*1: Output signal data write area to the AD62C
*2: Store area of the input signal data from the AD62C
*3: Area which stores station number and error code when an AD62C error occurs. (See Section 9.1 for error codes.)

| | Address (decimal) | | | Contents | PC CPU Read/write Enable/disable |
|---|---|---|---|---|---|
| *4 | 858 | Received data clear specification | | The AJ35PTF-R2 station number which executes received data clear by the received data clear request signal [Y (n + 23)] is specified. | Read/write enable |
| | 859 | Received data clear range specification | | The receive buffer which is cleared when the received data clear is executed by the received data clear request signal [Y (n + 23)] is specified. | |
| | 860 to 929 | No-protocol mode parameter | | Parameters when using the AJ35PTF-R2 in a no-protocol mode are set. | |
| | 930 to 1099 | (Unused) | | ——— | ——— |
| | | CH0 | CH1 | | |
| *5 | 1100 to 2099 | Communication area for remote terminal No. 1 | Communication area for remote terminal No. 8 | Send data to the remote terminal module write area, or, received data from the remote terminal module store area. | Read/write enable |
| | 2100 to 3099 | Communication area for remote terminal No. 2 | Communication area for remote terminal No. 9 | | |
| | 3100 to 4099 | Communication area for remote terminal No. 3 | Communication area for remote terminal No. 10 | | |
| | 4100 to 5099 | Communication area for remote terminal No. 4 | Communication area for remote terminal No. 11 | | |
| | 5100 to 6099 | Communication area for remote terminal No. 5 | Communication area for remote terminal No. 12 | | |
| | 6100 to 7099 | Communication area for remote terminal No. 6 | Communication area for remote terminal No. 13 | | |
| | 7100 to 8099 | Communication area for remote terminal No. 7 | Communication area for remote terminal No. 14 | | |
| | | [Y (n + 2C) at OFF] | [Y (n + 2C) at ON] | | |

*4: Clear processing area of received data by the AD62C reset operation
*5: Buffer memory area for AD62C data transfer (1st module to 14th module)

## 7.6 Programming Examples

Programming under the following setting conditions of PLC CPU, AJ71PT32-S3 (A1SJ71PT32-S3), and AD62C is explained below.



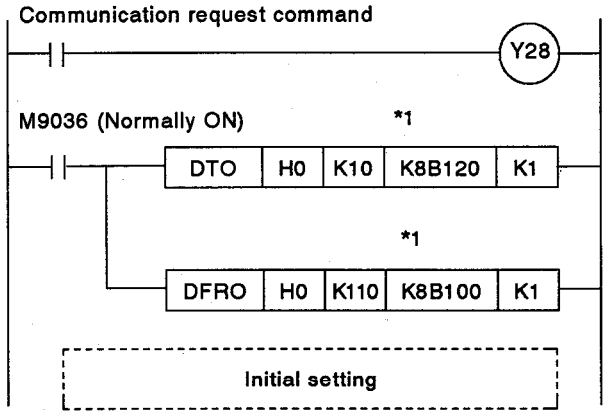

**REMARK**

When the AJ71PT32-S3 (A1SJ71PT32-S3) is loaded into slot 0 of the extension base of A0J2H/A0J2CPU, the upper 2 digits of the FROM/TO instruction head I/O number will be H10 because 64-point I/O numbers (100 to 13F) are occupied.

**[Basic programs]**

Basic programs to the AJ71PT32-S3 (A1SJ71PT32-S3) are explained below.

(1) I/O signal processing program




Communication start (Y28) is turned ON.

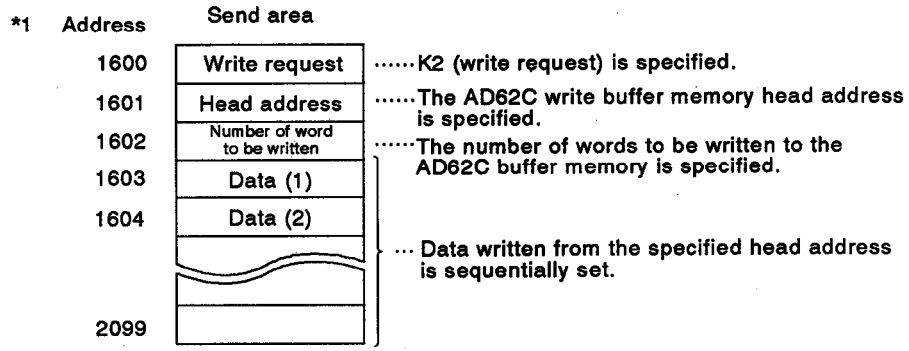
ON/OFF data of B120 to B13F (equivalent to AD62C Y00 to Y1F) are written to AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory addresses 10 and 11.

Read from AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory addresses 110 and 111 to B100 to B11F (equivalent to AD62C X00 to X1F).

*1: Since the A0J2CPU (P23/R23) and A1 to A3CPU (P21/R21) cannot use bit devices, use data register (D) to execute read/write.

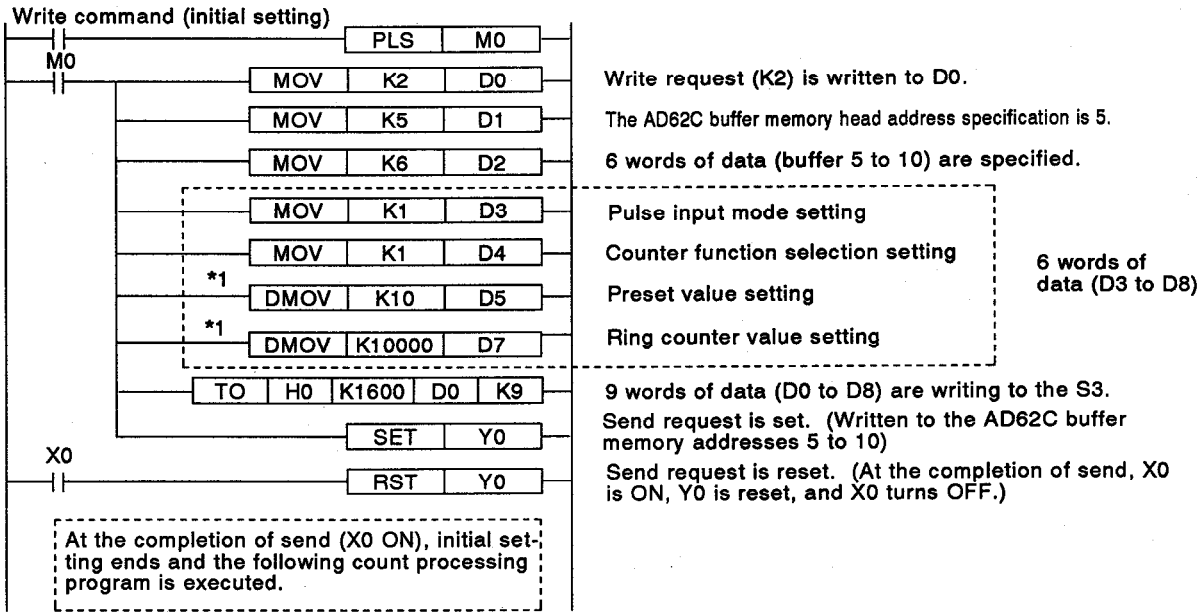
(2) Program to write to the buffer memory

(a) AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory write area details (1st module's address)




*1: Data content from the head addresses of modules 2 to 14 is the same.

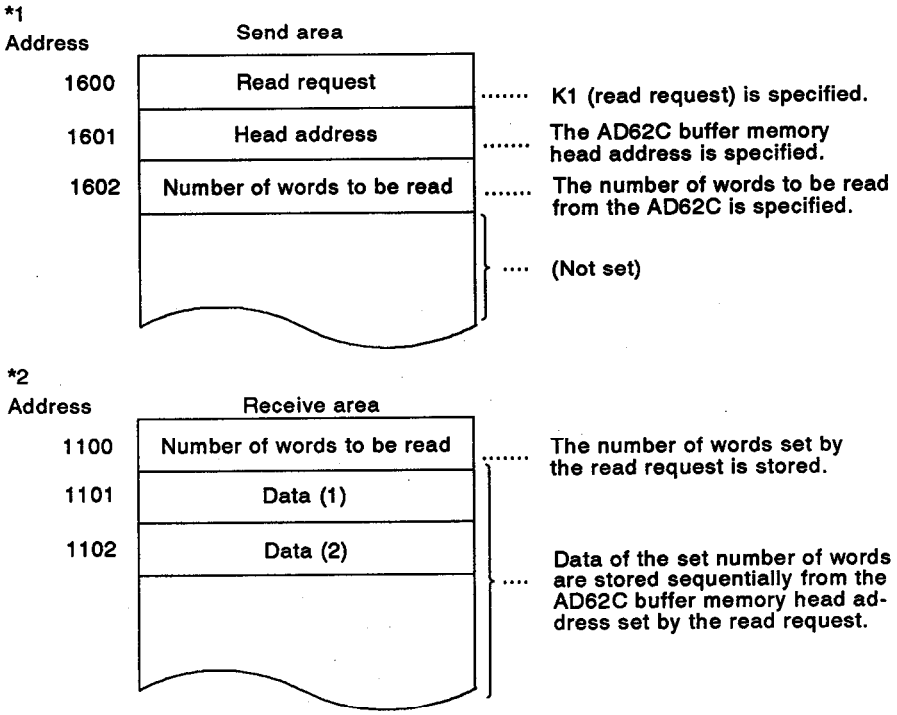
(b) Write program




*1: Since there is no DMOV instruction for the A0J2CPU (P23/R23), use the MOV instruction.

(3) Read program from the buffer memory

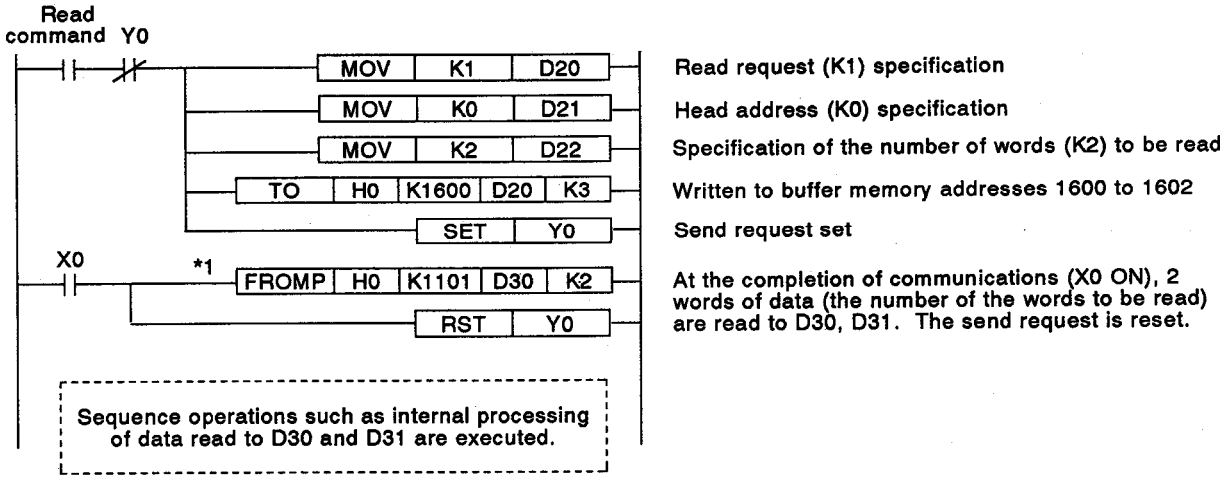
(a) AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory write and read area details (1st module's address)




*1,*2: Data content from the head addresses of modules 2 to 14 is the same.

(b) Read program

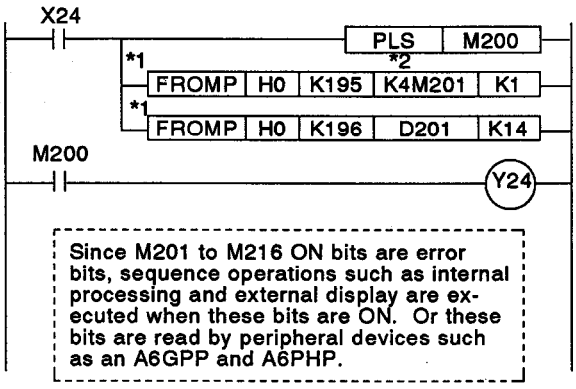
The read conditions are set and written to the send area. At the completion of read, received data is read from the receive area.




*1: Since there is no FROMP instruction for the A0J2CPU (P23/R23), execute the FROM instruction by converting it a pulse instruction using an internal relay.

(4) Error detection program

AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory K195 (remote terminal unit faulty station) and K196 to K209 (remote terminal module error code) are read.




Buffer memory is read when X24 (error detection) is ON and reset command is executed.

Faulty station read (Faulty stations: M201 to M216 when bit ON)

The error codes of terminals No. 1 to No. 14 are read to D201 to D214.

When M200 is ON, Y24 turns ON and X24 turns OFF. After staying ON for 1 scan, Y24 turns OFF.

*1: Since there are no pulse instructions for the A0J2CPU (P23/R23), convert a FROM instruction to pulse instruction using the internal relay.

*2: With A0J2CPU (P23/R23) and A1 to A3CPU (P21/R21), read the data to data register (D).

(a) The error codes which are detected by the AJ71PT32-S3 (A1SJ71PT32-S3) are shown below.

| Error Codes (decimal) | Error Names | Error Contents | Corrective Action(s) |
|---|---|---|---|
| 1 | Set data error | There is an error in the data set to the AD62C send area. | Set correct data. |
| 6 | WDT error | AD62C is malfunctioning. | Confirm the AD62C LED indicators and correct following the AD62C troubleshooting procedure. |
| 8 | Send area set error | AD62C send area size is insufficient. | Set the send area of the required number of bytes as send data to the AD62C. |
| 9 | Communication error | Normal communication between the master module and the AD62C cannot be executed. | • Noise····Execute communication again.<br>• Check the AD62C for possible hardware fault. |
| 11 | | | |
| 10 | Receive area set error | AD62C receive area size is insufficient. | Set the receive area of the required number of bytes as received data from the AD62C. |

(b) In addition to the above error codes, an error code which the AD62C detects is sent to the AJ71PT32-S3 (A1SJ71PT32-S3) and is stored in the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory. (For AD62C error codes, see Section 9.1.)

(5) Data clear processing program by AD62C reset operations and allowable communication time over

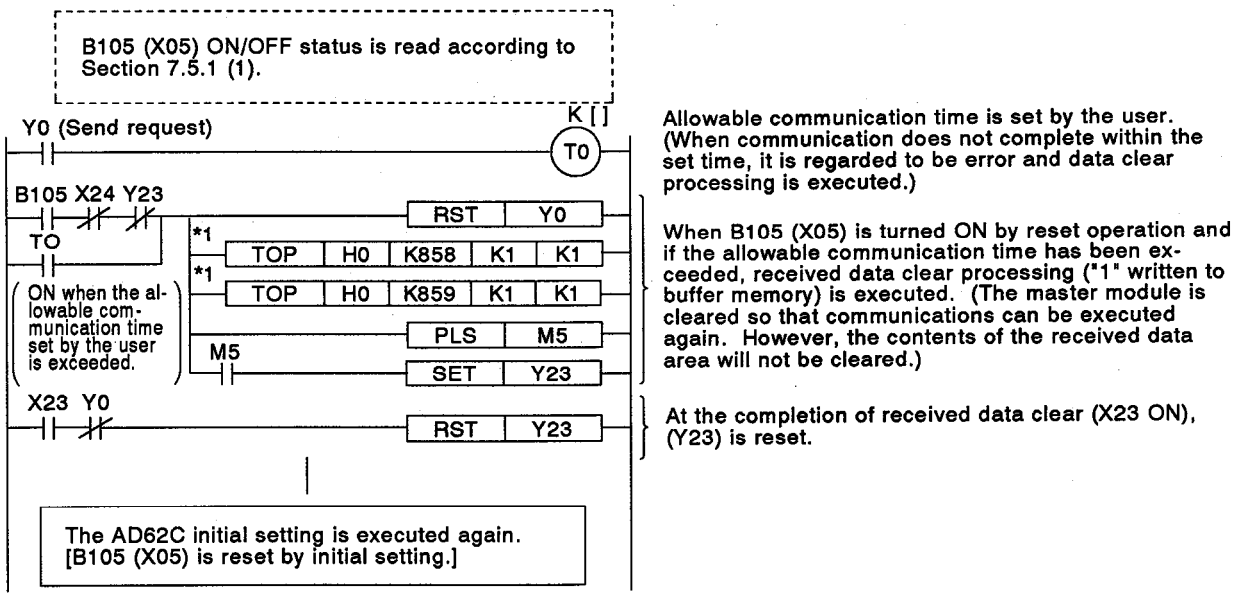
(a) When the AD62C's front reset switch is operated during communications, it is necessary to write the initial data again after detecting the reset operation and clearing the AJ71PT32-S3 (A1SJ71PT32-S3) received data using the sequence program.

> If initial setting is not executed again after reset operations, the AD62C will not operate correctly.

(b) The detection of the AD62C reset signal is executed by the device number assigned to AD62C I/O signals.

- Reset status detection ..... X05 ON
- Reset status detection is reset ..... Y05 ON (When Y05 is ON, X05 turns OFF.)

(c) Reset signal read/write are executed according to Section 7.5 (1).




*1: Since there is no pulse TO instruction for the A0J2CPU (P23/R23), execute the TO instruction after converting it into pulse instruction using an internal relay.

### 7.6.1 Preset function programming example

(1) Preset function programming example using a sequence program

Create a program to count 2-phase pulses multiplied by one and to execute the preset function using the sequence program.

**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command.....M9038

(b) Communication request command.....X30

(c) Count operation start command.....X31

(d) Present value read command.....X32

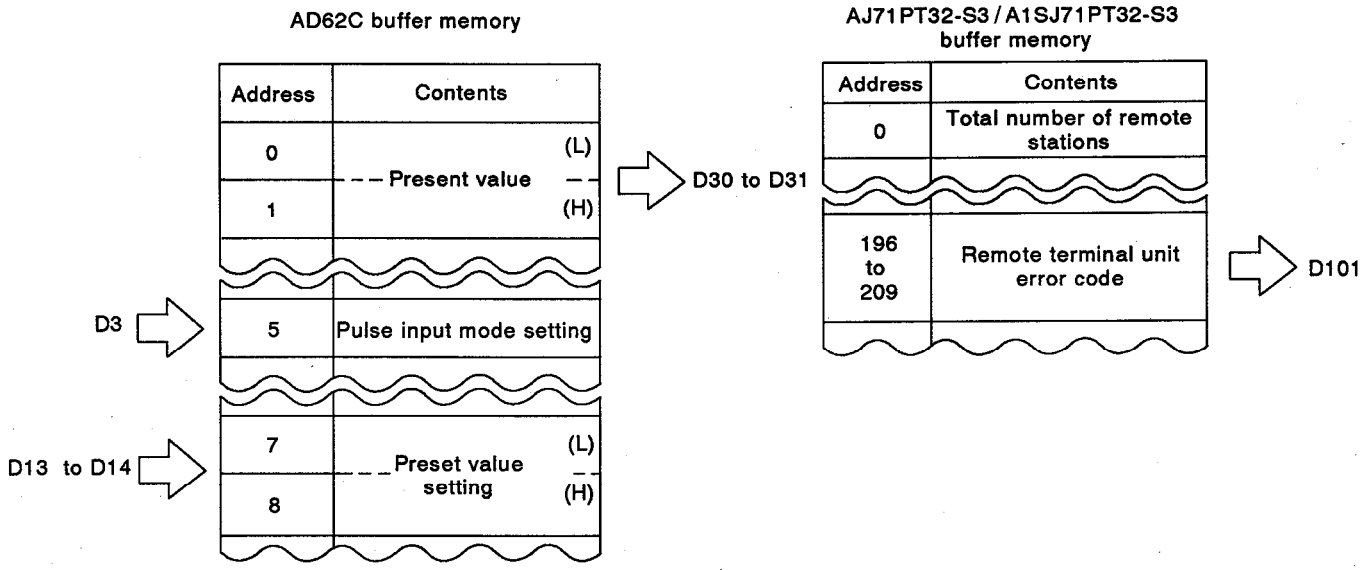
(e) Preset value write command.....X33

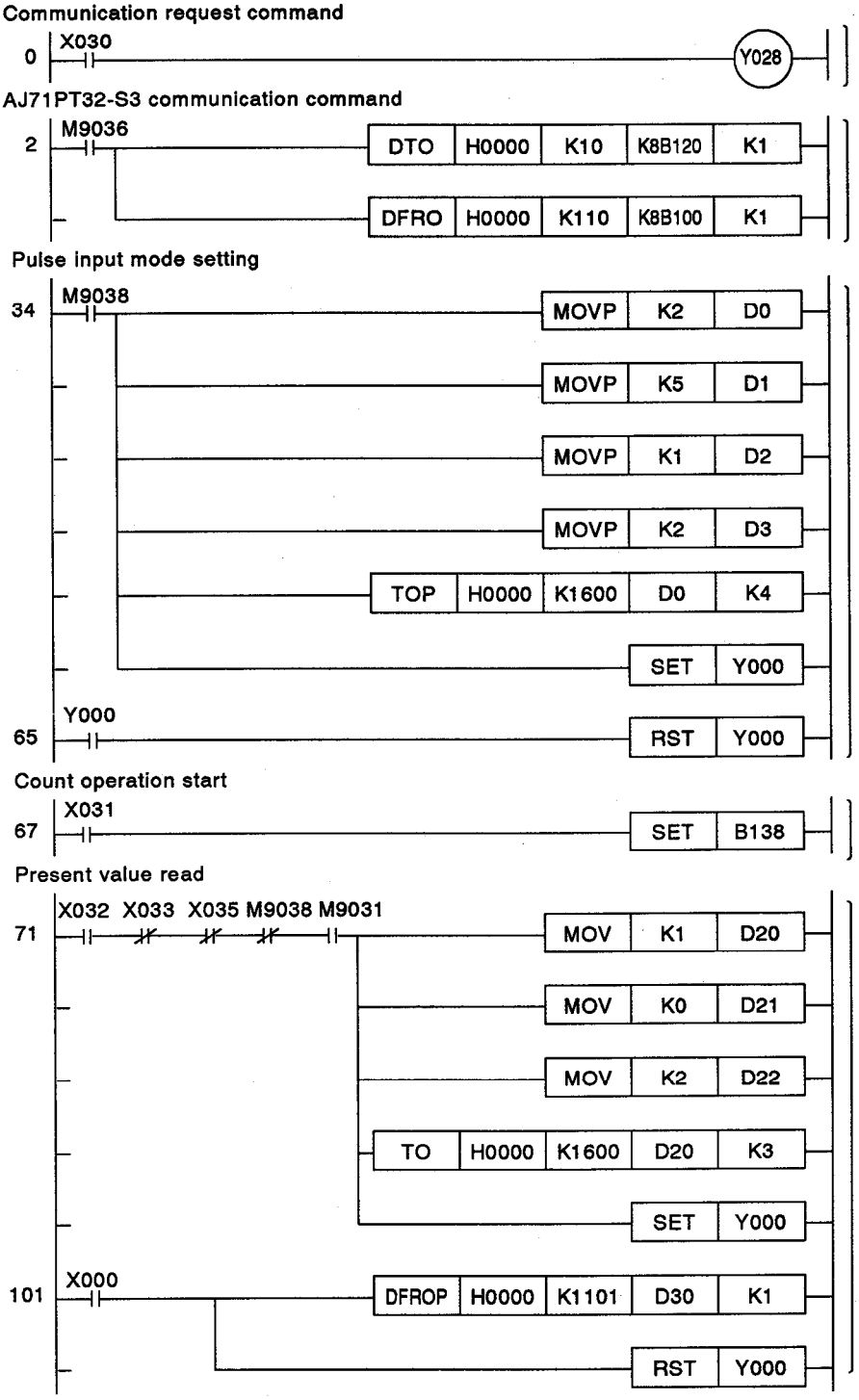
(f) Preset execute command.....X34

(g) Communication error reset command.....X35

(h) Count operation stop command.....X36

(b) Relationship between the data register and the buffer memory





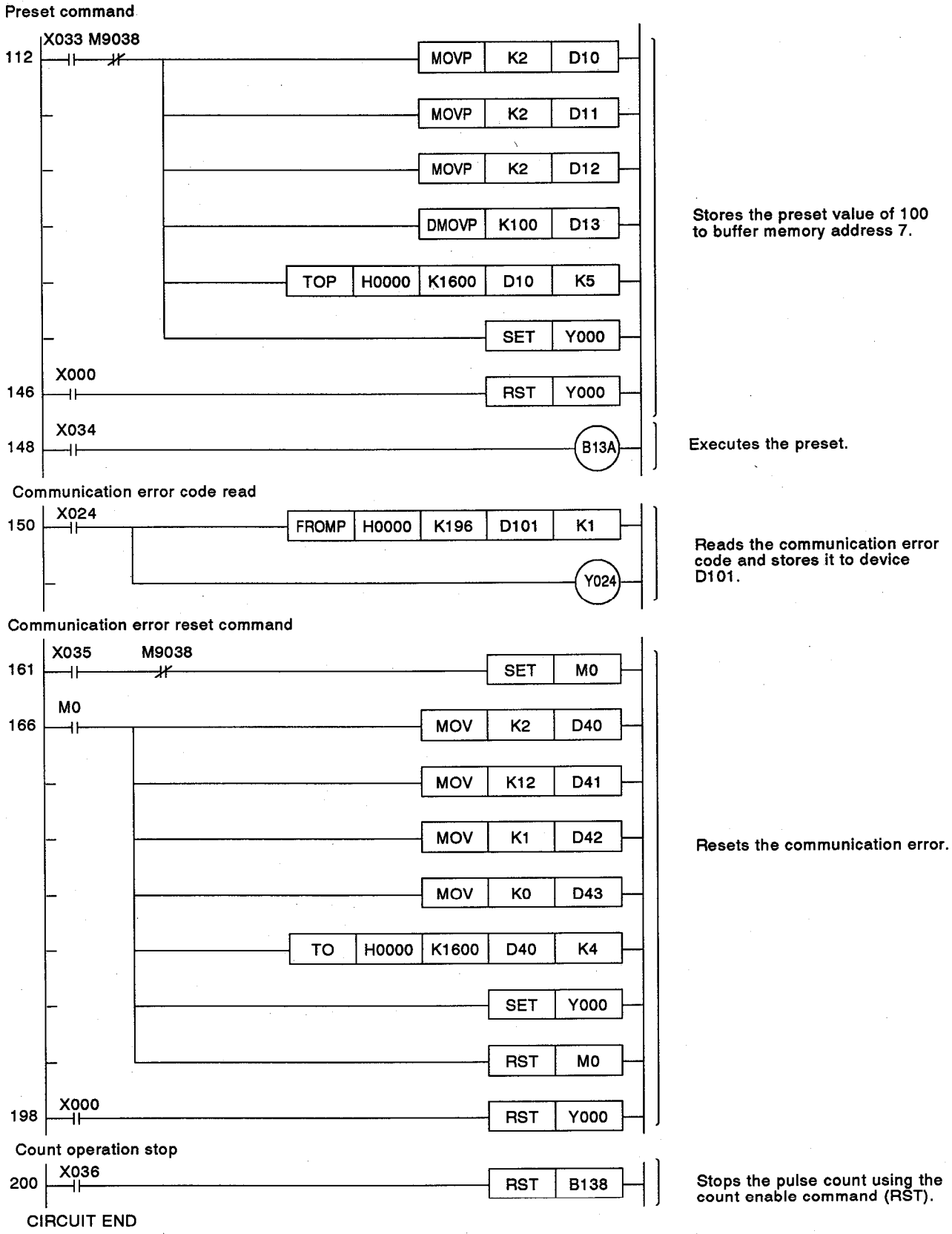

Starts A1S/AJ71PT32-S3 communications.

Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.


Preset command
112
X033 M9038
MOVP K2 D10
MOVP K2 D11
MOVP K2 D12
DMOVP K100 D13
TOP H0000 K1600 D10 K5
SET Y000
146
X000
RST Y000
148
X034
B13A
Stores the preset value of 100 to buffer memory address 7.
Executes the preset.
Communication error code read
150
X024
FROMP H0000 K196 D101 K1
Y024
Reads the communication error code and stores it to device D101.
Communication error reset command
161
X035
M9038
SET M0
166
M0
MOV K2 D40
MOV K12 D41
MOV K1 D42
MOV K0 D43
TO H0000 K1600 D40 K4
SET Y000
RST M0
198
X000
RST Y000
Resets the communication error.
Count operation stop
200
X036
RST B138
Stops the pulse count using the count enable command (RST).
CIRCUIT END

(2) Preset function programming example using an external input

Create a program to count 2-phase pulses multiplied by one and to execute the preset function with the external input.

**[Devices to be used]**

(a) Execution commands

(a) Pulse input mode setting command ..... M9038

(b) Communication request command ..... X30

(c) Count operation start command ..... X31

(d) Present value read command ..... X32

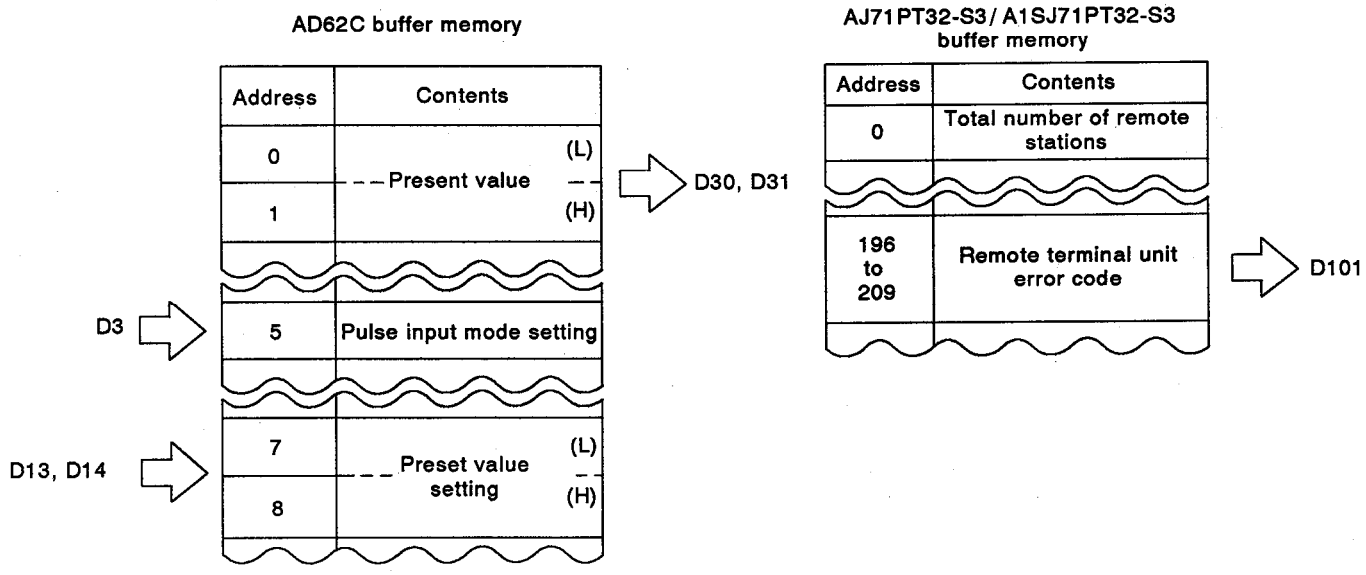
(e) Preset value write command ..... X33

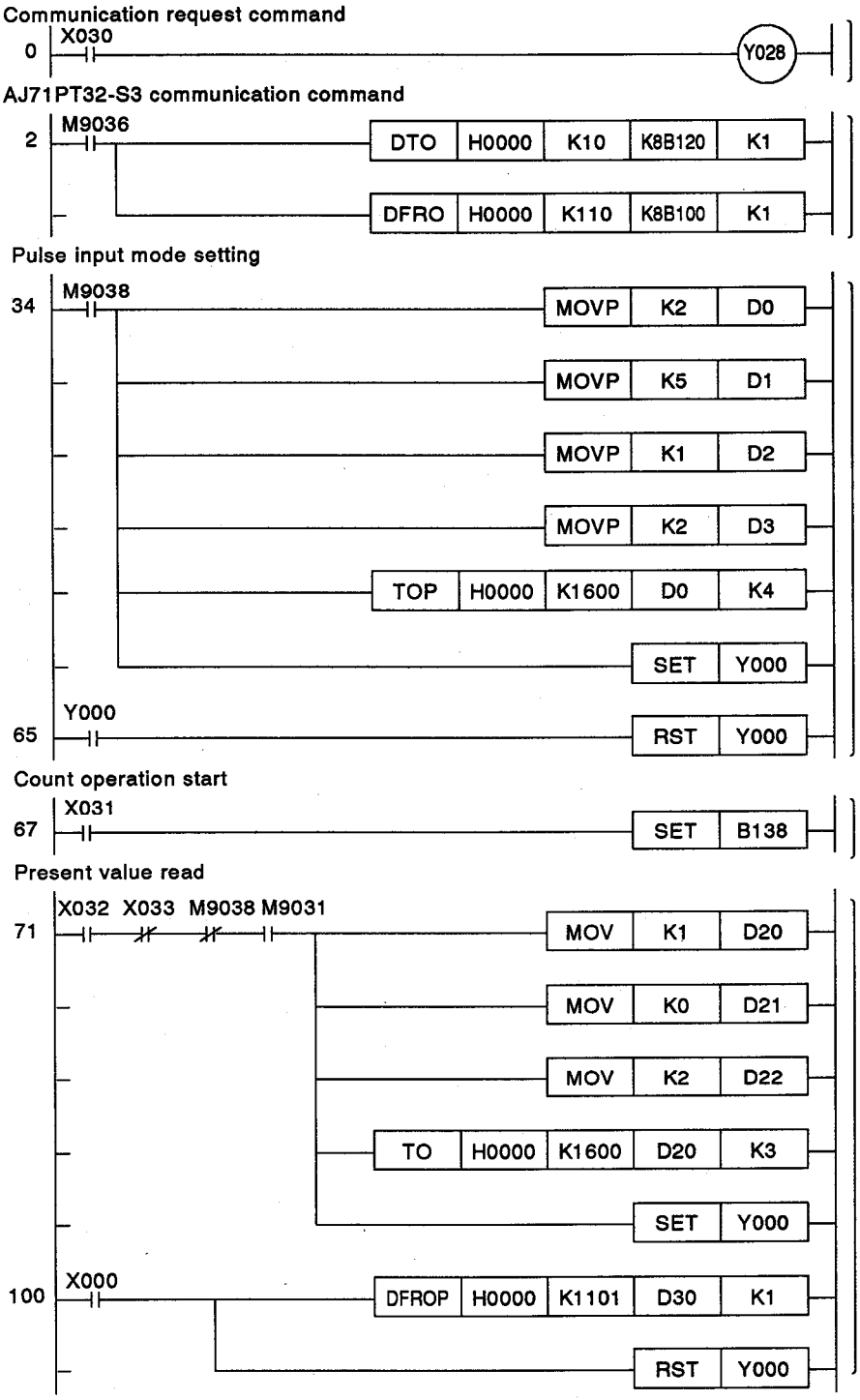
(f) External preset command detection flag reset command ..... X1E

(g) Communication error reset command ..... X34

(h) Count operation stop command ..... X35

(b) Relationship between the data register and the buffer memory





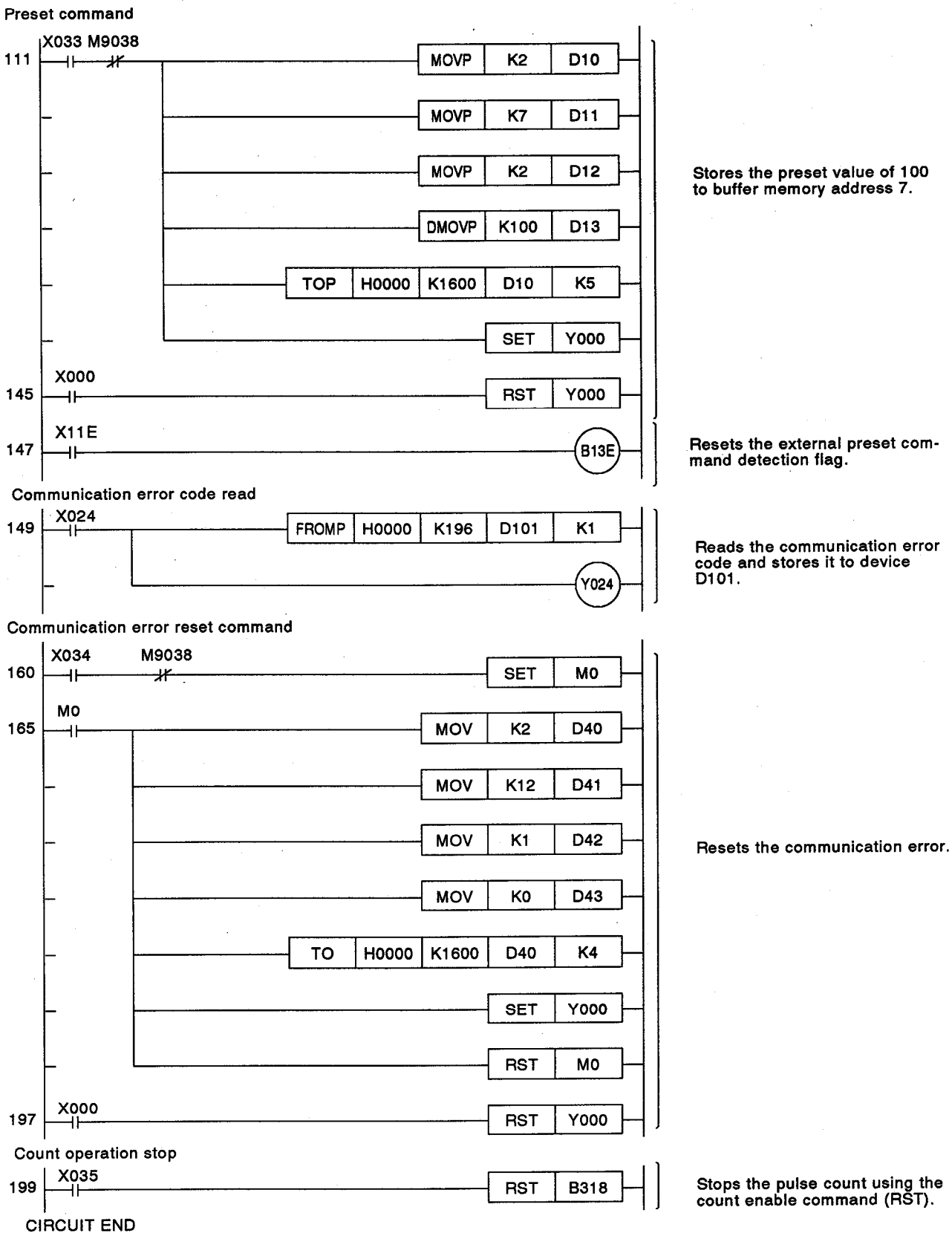

Starts A1S/AJ71PT32-S3 communications.

Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.


Preset command
111
X033 M9038
MOVP K2 D10
MOVP K7 D11
MOVP K2 D12
DMOVP K100 D13
TOP H0000 K1600 D10 K5
SET Y000
145
X000
RST Y000
147
X11E
B13E
Stores the preset value of 100 to buffer memory address 7.
Resets the external preset command detection flag.
Communication error code read
149
X024
FROMP H0000 K196 D101 K1
Y024
Reads the communication error code and stores it to device D101.
Communication error reset command
160
X034
M9038
SET M0
165
M0
MOV K2 D40
MOV K12 D41
MOV K1 D42
MOV K0 D43
TO H0000 K1600 D40 K4
SET Y000
RST M0
197
X000
RST Y000
Resets the communication error.
Count operation stop
199
X035
RST B318
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 7.6.2 Ring counter function programming example

Create a program to count 2-phase pulses multiplied by one and to execute the ring counter function.

**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038

(b) Communication request command.....X30

(c) Count operation start command.....X31

(d) Present value read command.....X32

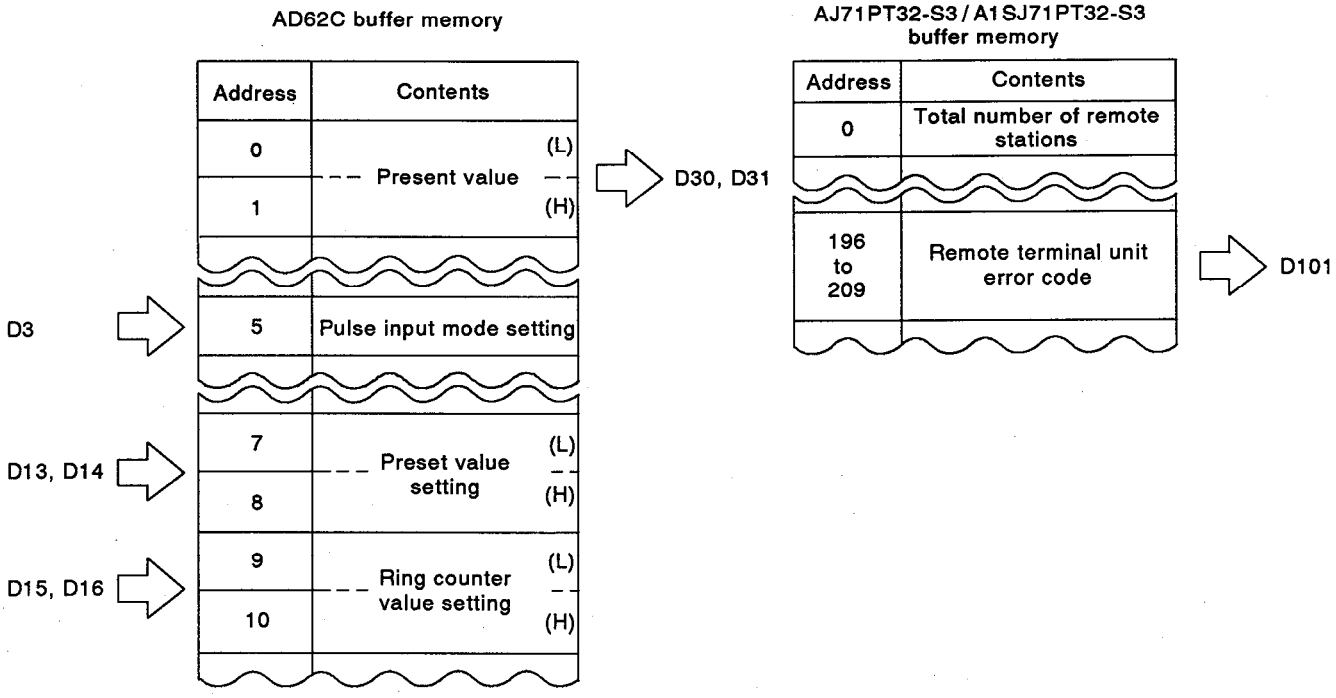
(e) Preset/ring count value write command.....X33

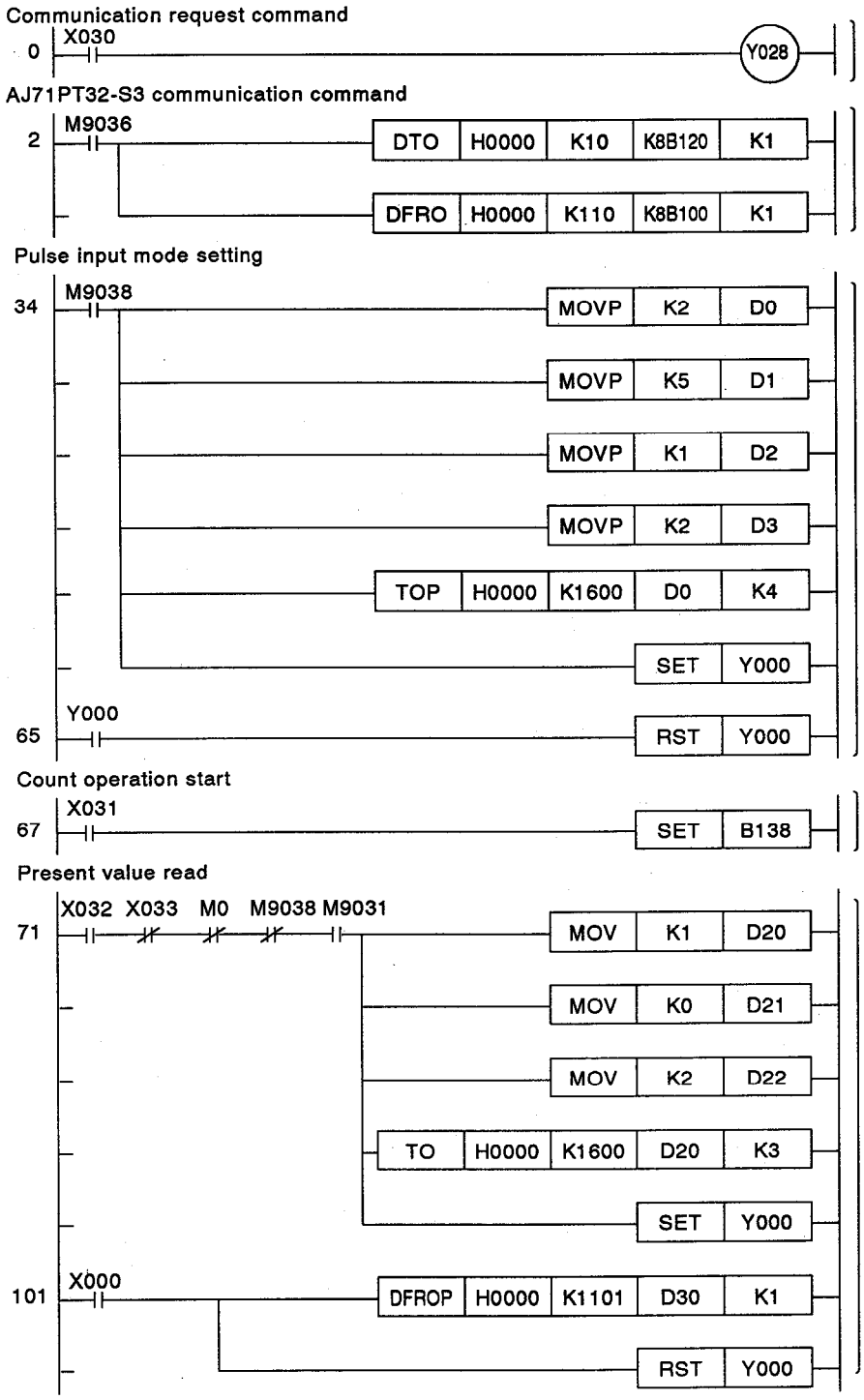
(f) Ring counter command.....X34

(g) Communication error reset command.....X35

(h) Count operation stop command.....X36

(2) Relationship between the data register and the buffer memory





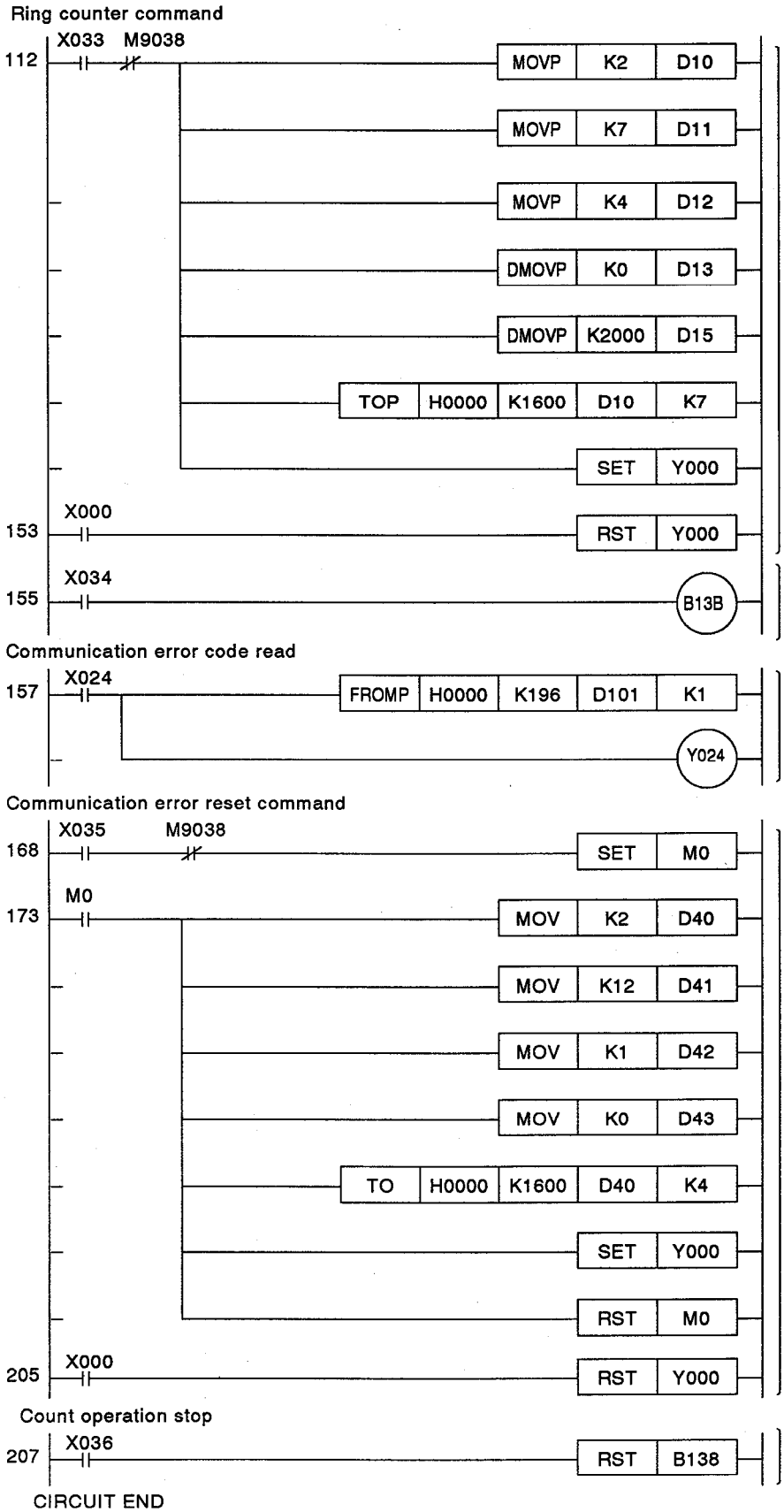

Starts A1S/AJ71PT32-S3 communications.

Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.




Stores the preset value and ring counter value to buffer memory addresses 7 to 10.

Executes the ring counter.

Reads the communication error code and stores it to device D101.

Resets the communication error.

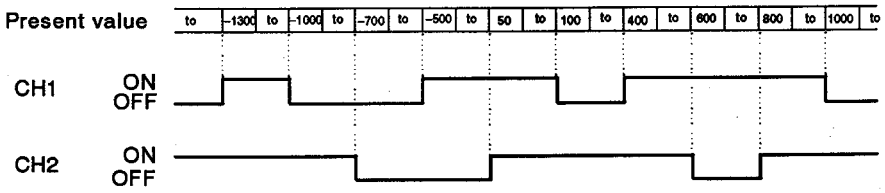
Stops the pulse count using the count enable command (RST).

### 7.6.3 Limit switch output function programming example

Create a program to count 2-phase pulses multiplied by one and to execute the limit switch function.

**[Operation status]**

ON/OFF status of the limit switch output is shown below:

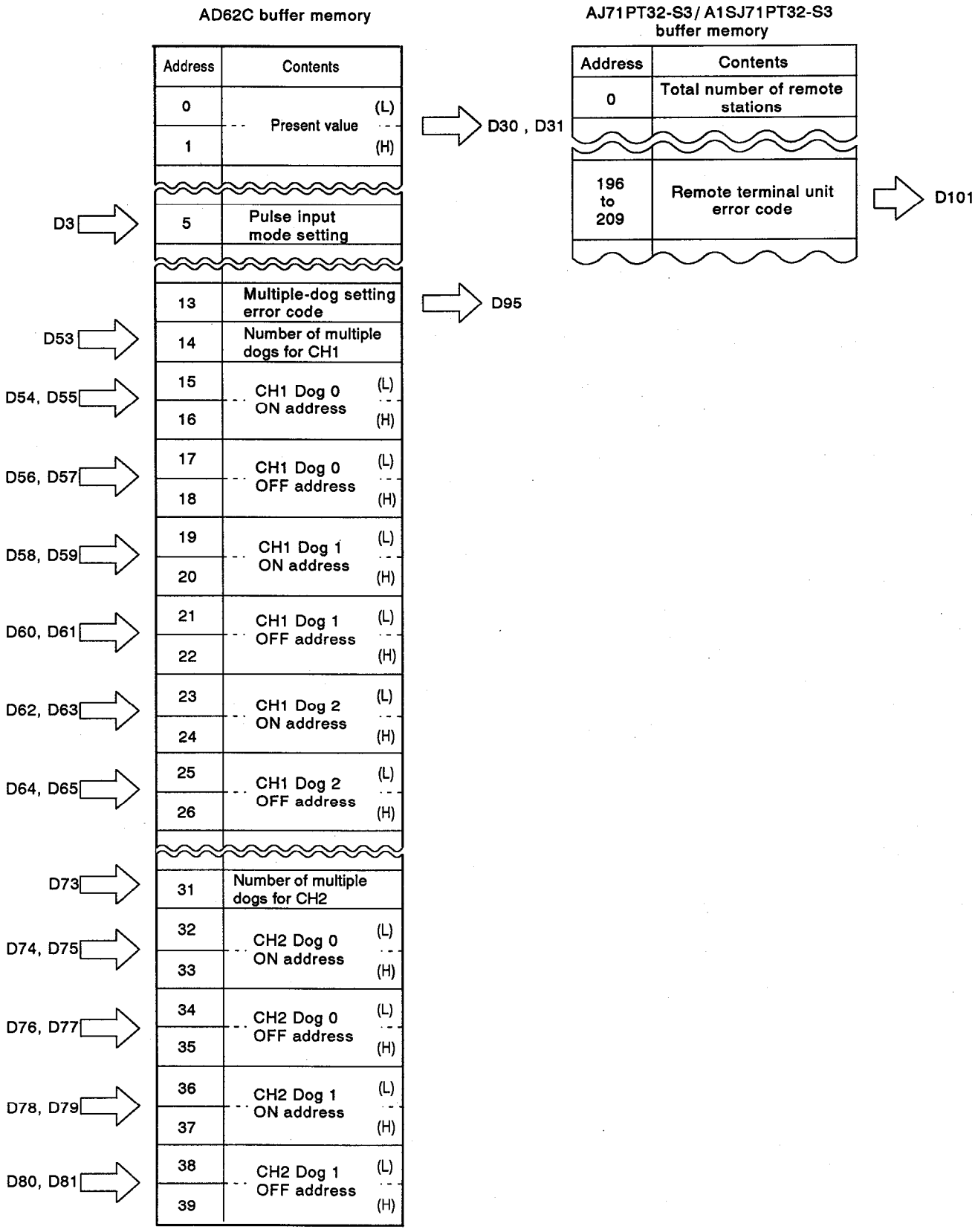



**[Devices to be used]**

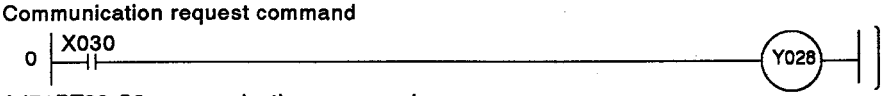
(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Communication request command ..... X30
(c) Fuse blown detection ..... B11B
(d) Count operation start command ..... X31
(e) Present value read command ..... X32
(f) Limit switch output data setting command ..... X33, 34
(g) Limit switch output command ..... X35
(h) Communication error reset command ..... X36
(i) Multple-dog setting error reset command ..... X37
(j) Count operation stop command ..... X38

(2) Relationship between the data register and the buffer memory

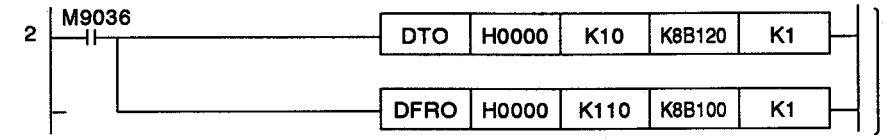


Communication request command



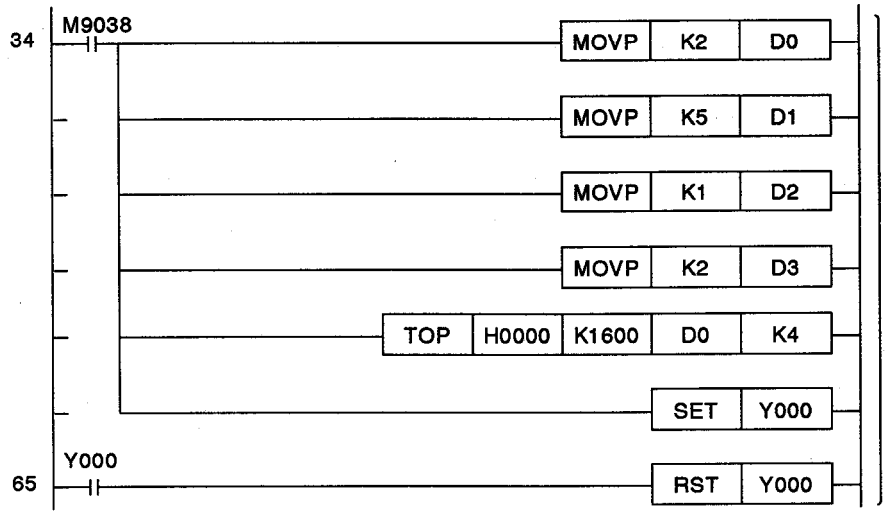

Starts A1S/AJ71PT32-S3 communications.

AJ71PT32-S3 communication command



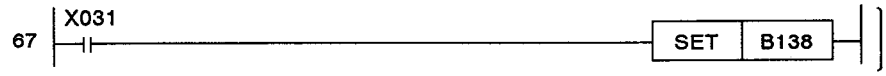

Always writes and reads to/from A1S/AJ71PT32-S3.

Pulse input mode setting



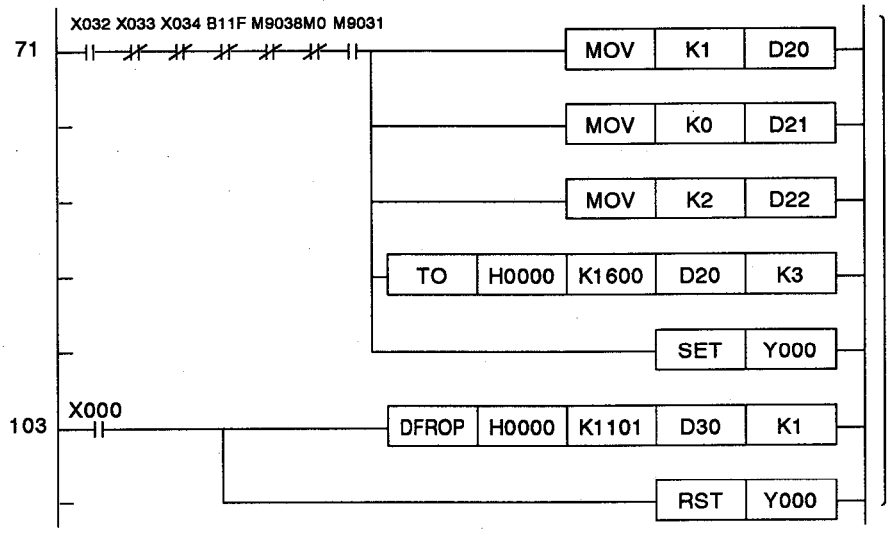

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Count operation start



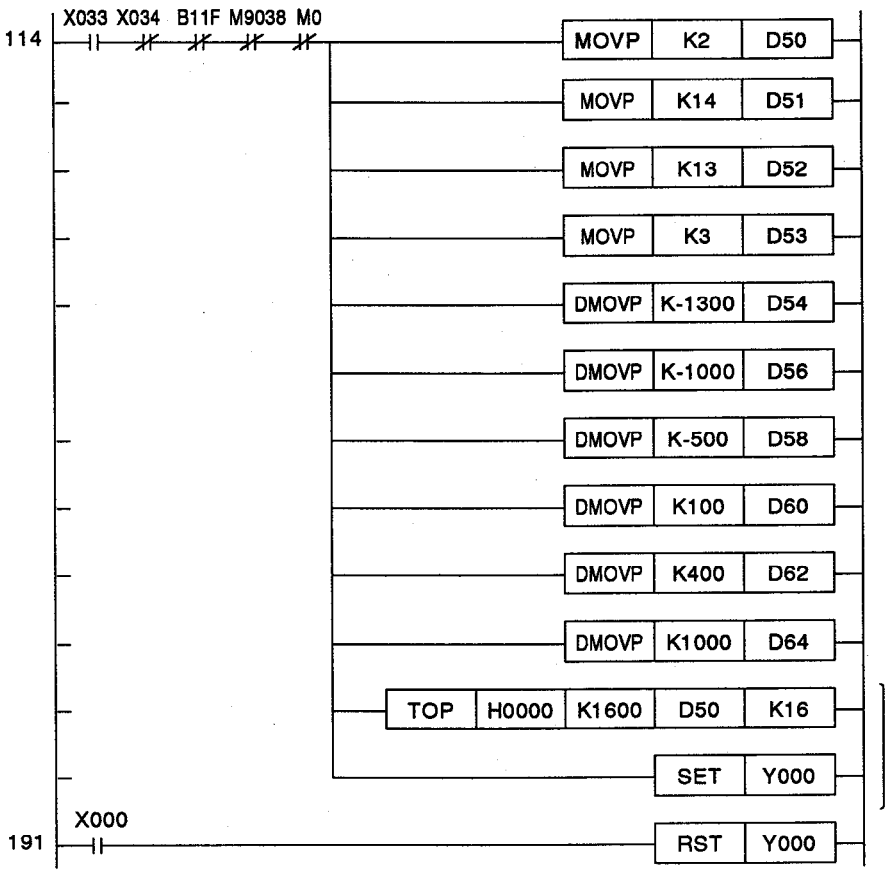

Start the pulse count using the count enable command (SET).

Present value read




Reads the present value and stores it to devices D30 to D31.

Limit switch output command No.1




Number of multiple dogs for CH 1

Dog 0 ON address

Dog 0 OFF address

Dog 1 ON address

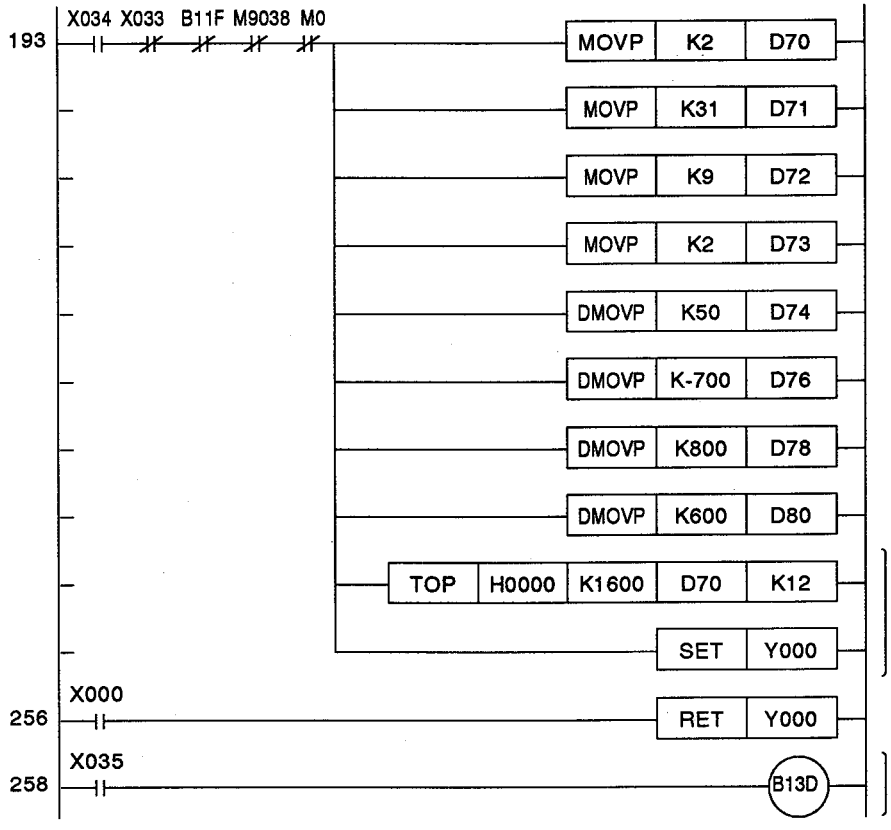
Dog 1 OFF address

Dog 2 ON address

Dog 2 OFF address

Stores the contents of D53 to D65 to buffer memory addresses 14 to 26.

Limit switch output command No.2




Number of multiple dogs for CH 2

Dog 0 ON address

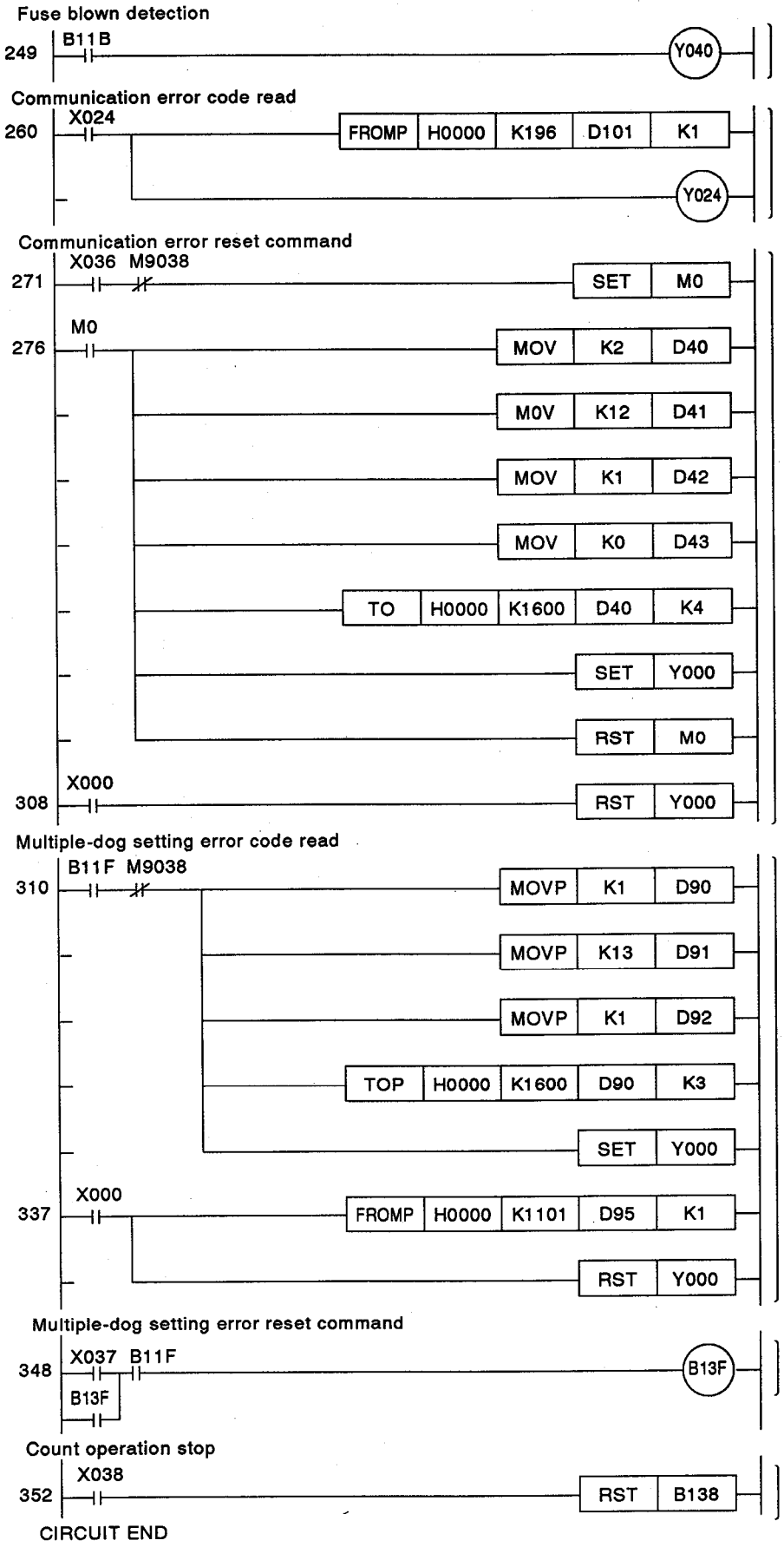
Dog 0 OFF address

Dog 1 ON address

Dog 1 OFF address

Stores the contents of D73 to D81 to buffer memory addresses 31 to 39.

Executes the limit switch output.




Detects a blown fuse and output voltage cutoff.

Reads the communication error code and stores it to device D101.

Resets the communication error.

Reads the multiple-dog setting error code and stores it to device D95.

Resets the multiple-dog setting error.

Stops the pulse count using the count enable command (RST).

### 7.6.4 Latch counter function programming example

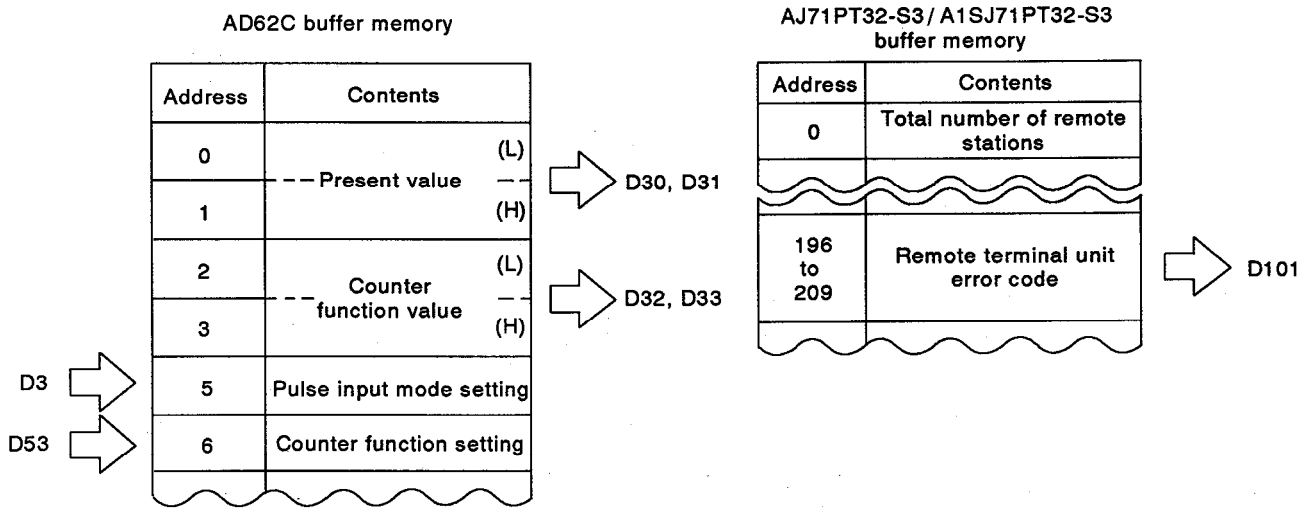
Create a program to count 2-phase pulses multiplied by one and to execute the latch counter.

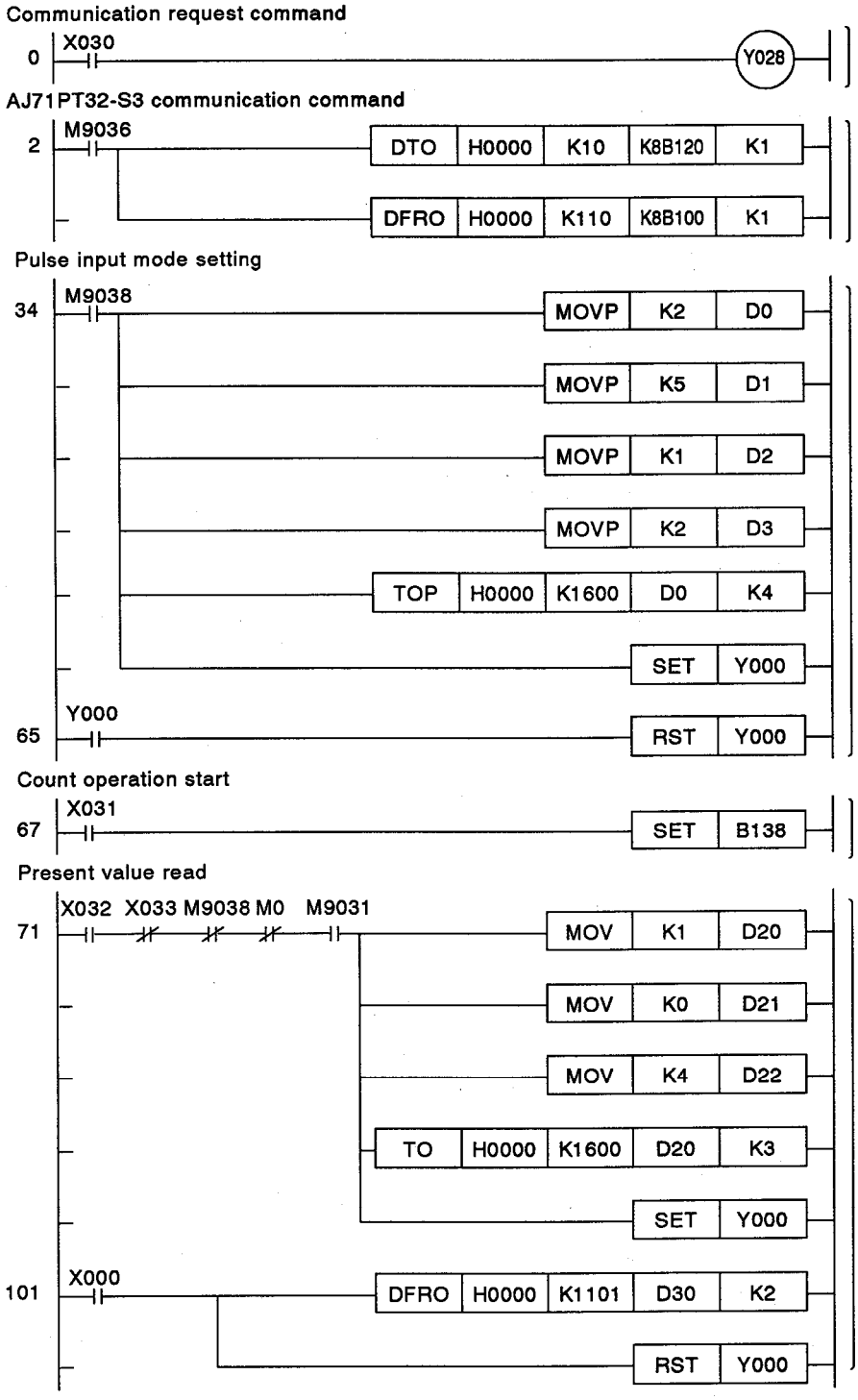
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Communication request command ..... X30
(c) Count operation start command ..... X31
(d) Present value read command, Counter function value read command ..... X32
(e) Counter function setting command ..... X33
(f) Latch counter command ..... X34
(g) Communication error reset command ..... X35
(h) Count operation stop command ..... X36

(2) Relationship between the data register and the buffer memory






Starts A1S/AJ71PT32-S3 communications.

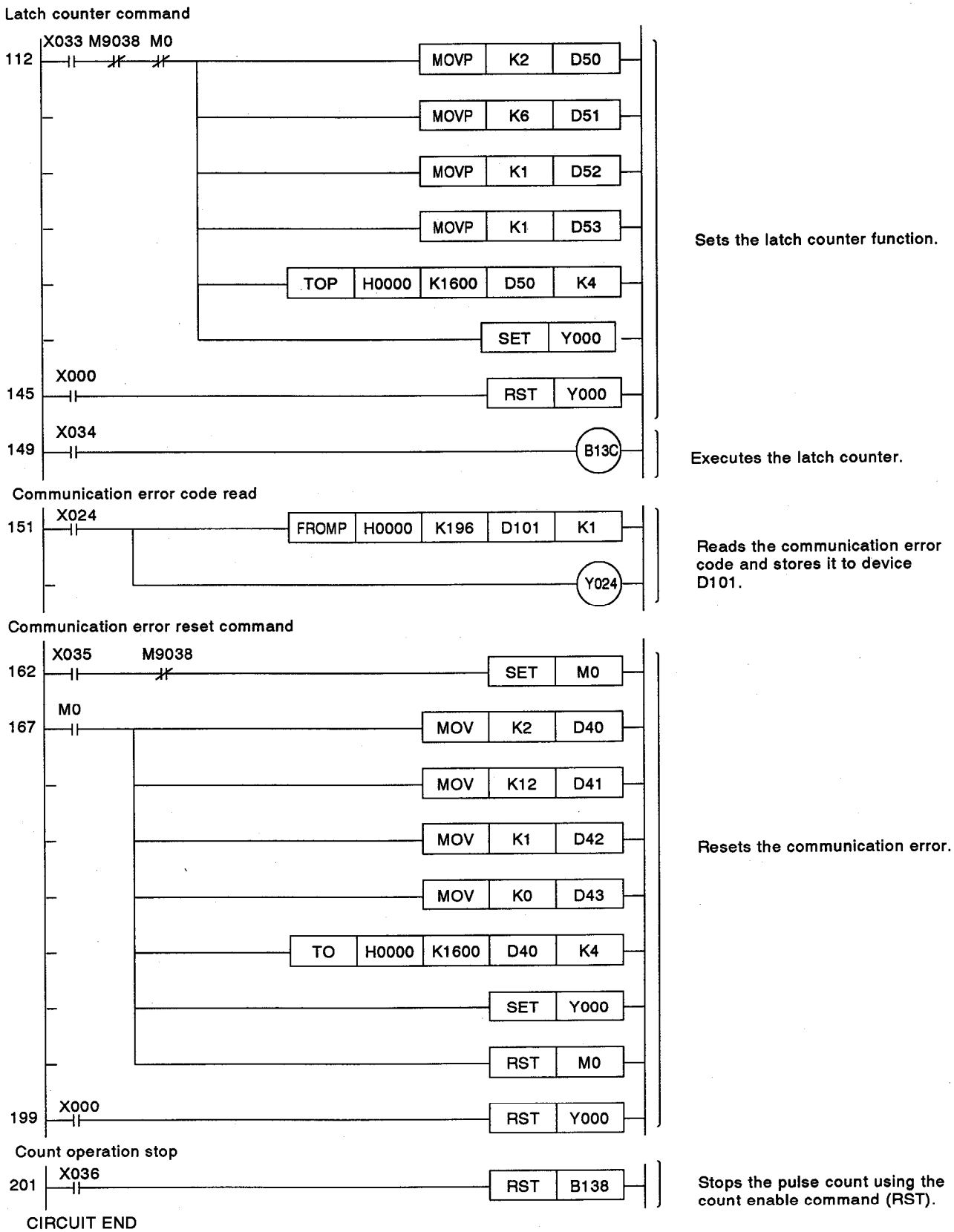
Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.

Reads the counter function selection count value and stores it to devices D32 to D33.


Latch counter command
112
X033 M9038 M0
MOVP K2 D50
MOVP K6 D51
MOVP K1 D52
MOVP K1 D53
TOP H0000 K1600 D50 K4
SET Y000
145
X000
RST Y000
149
X034
B13C
Sets the latch counter function.
Executes the latch counter.
Communication error code read
151
X024
FROMP H0000 K196 D101 K1
Y024
Reads the communication error code and stores it to device D101.
Communication error reset command
162
X035 M9038
SET M0
167
M0
MOV K2 D40
MOV K12 D41
MOV K1 D42
MOV K0 D43
TO H0000 K1600 D40 K4
SET Y000
RST M0
199
X000
RST Y000
Resets the communication error.
Count operation stop
201
X036
RST B138
Stops the pulse count using the count enable command (RST).
CIRCUIT END

### 7.6.5 Sampling counter function programming example

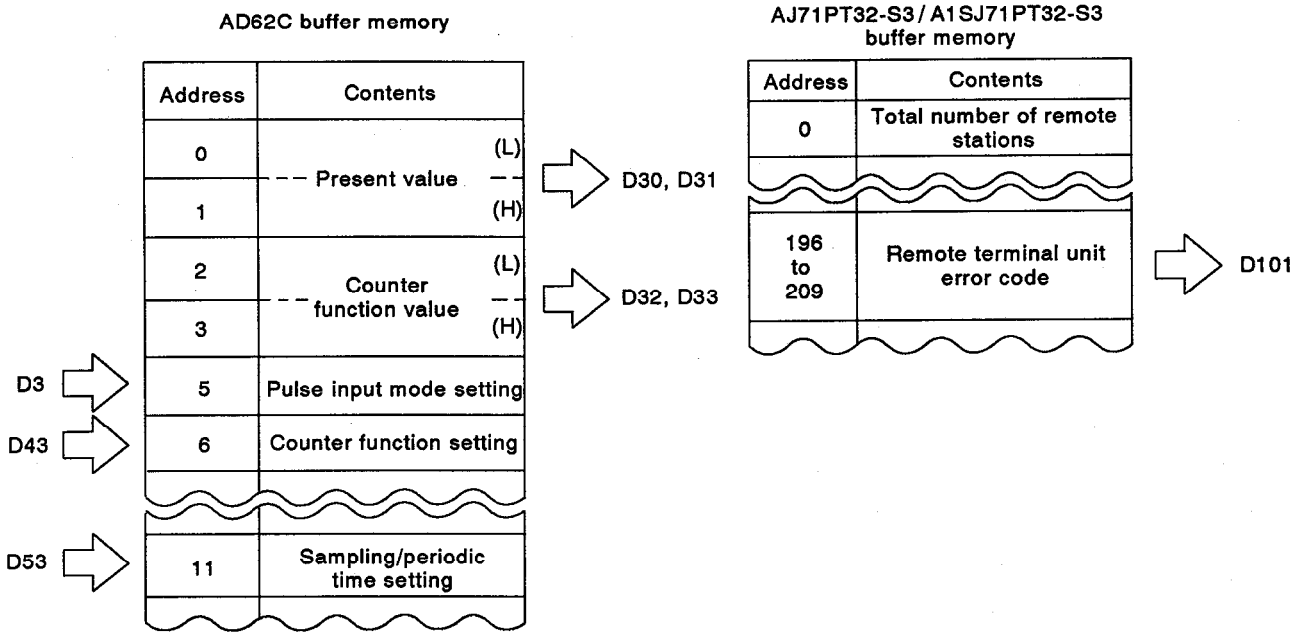
Create a program to count 2-phase pulses multiplied by one and to execute the sampling counter.

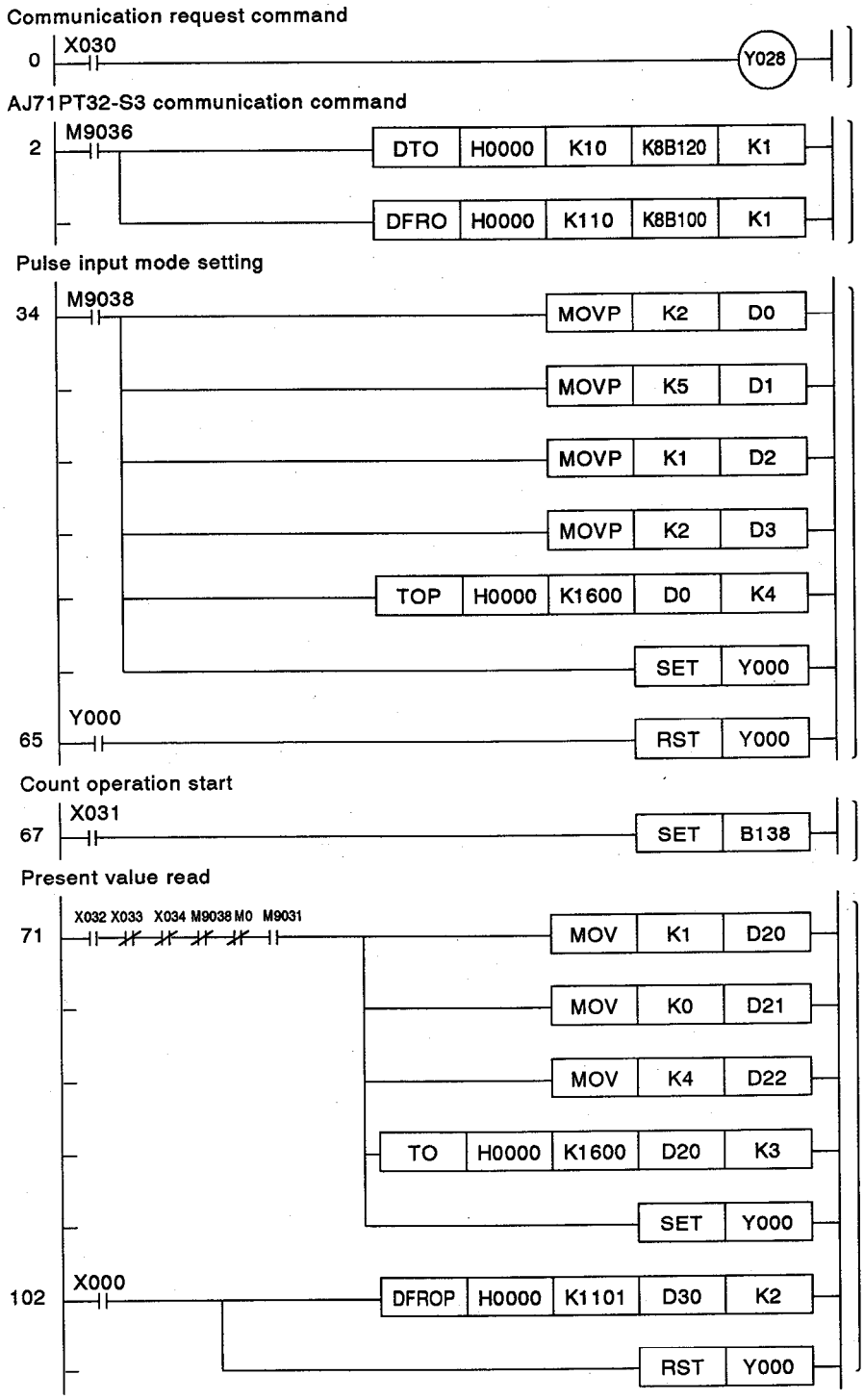
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Communication request command.....X30
(c) Count operation start command.....X31
(d) Present value read command, Counter function value read command.....X32
(e) Counter function setting command.....X33
(f) Sampling time setting command.....X34
(g) Sampling counter command:.....X35
(h) Communication error reset command:.....X36
(i) Count operation stop command:.....X37

(2) Relationship between the data register and the buffer memory






Starts A1S/AJ71PT32-S3 communications.

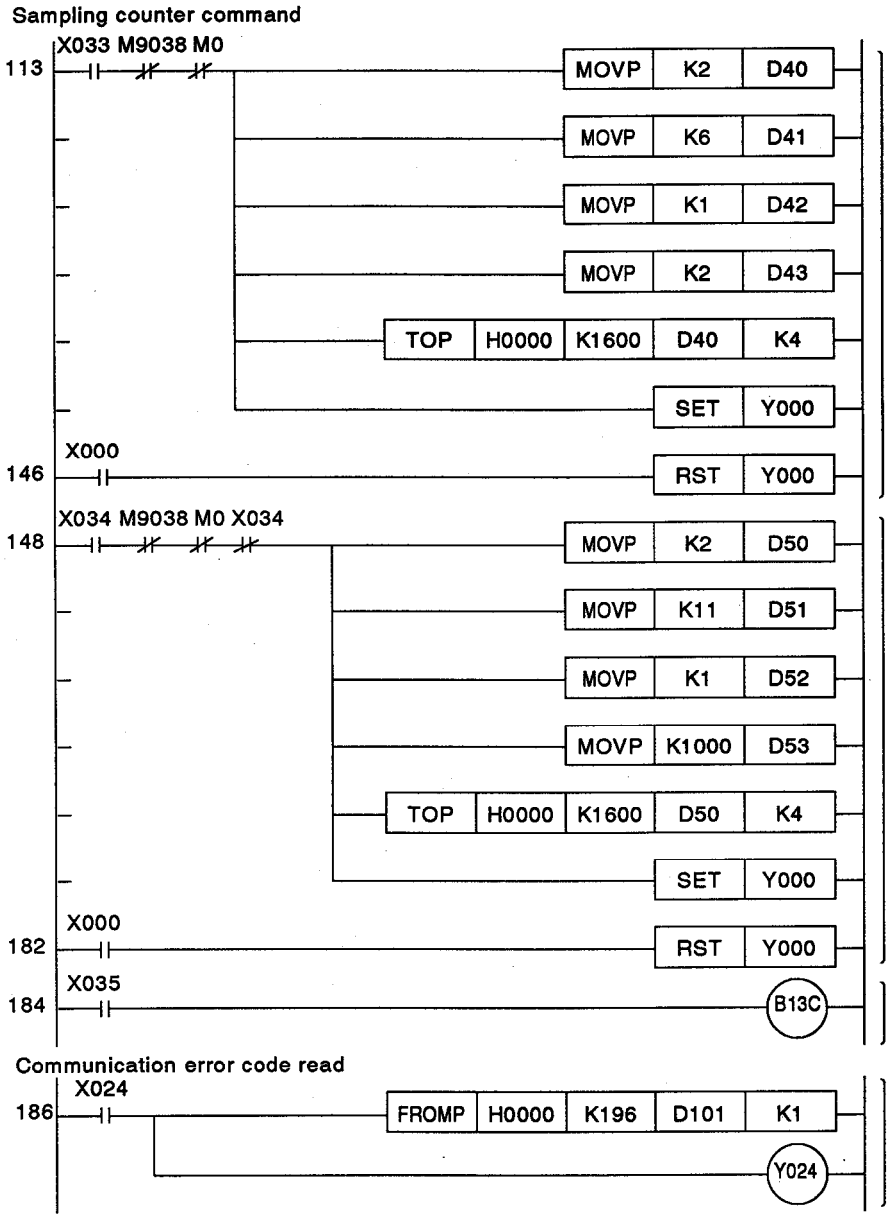
Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.

Reads the counter function selection count value and stores it to devices D32 to D33.

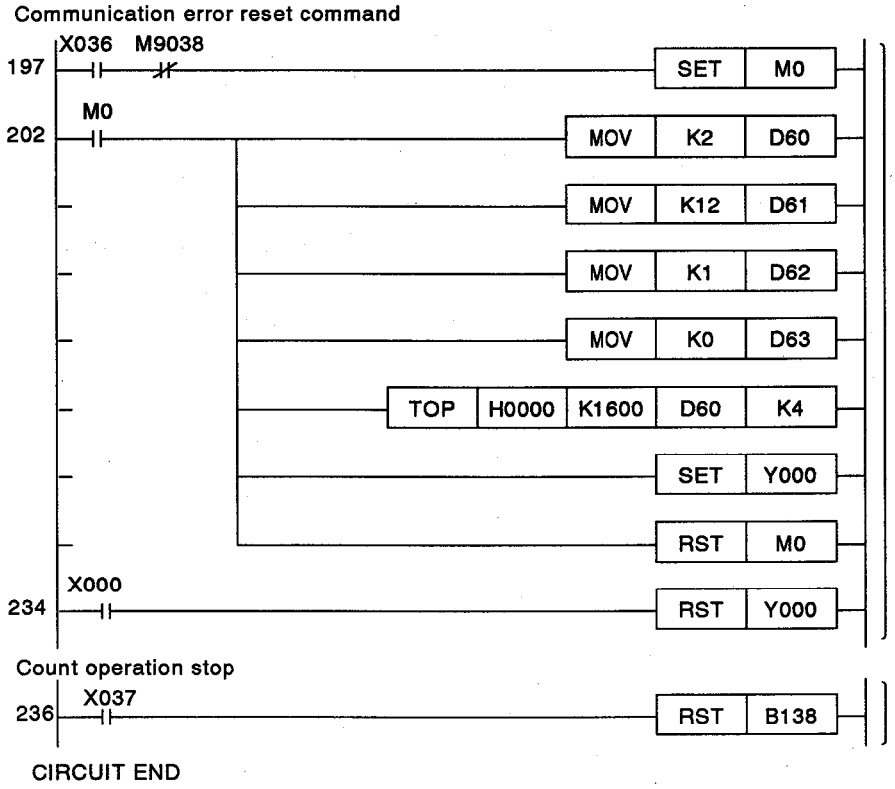



Sets the sampling counter function.

Sets the sampling time.

Executes the sampling counter.

Reads the communication error code and stores it to device D101.




Resets the communication error.

Stops the pulse count using the count enable command (RST).

### 7.6.6 Periodic pulse counter function programming example

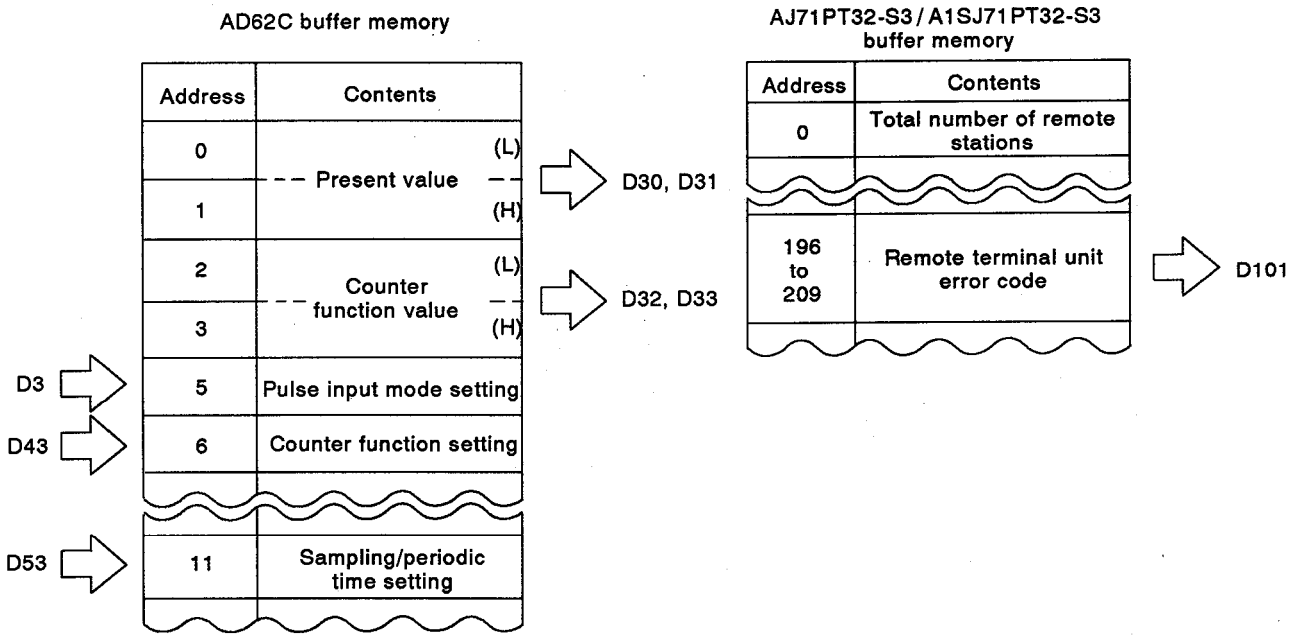
Create a program to count 2-phase pulses multiplied by one and to execute the periodic pulse counter function.

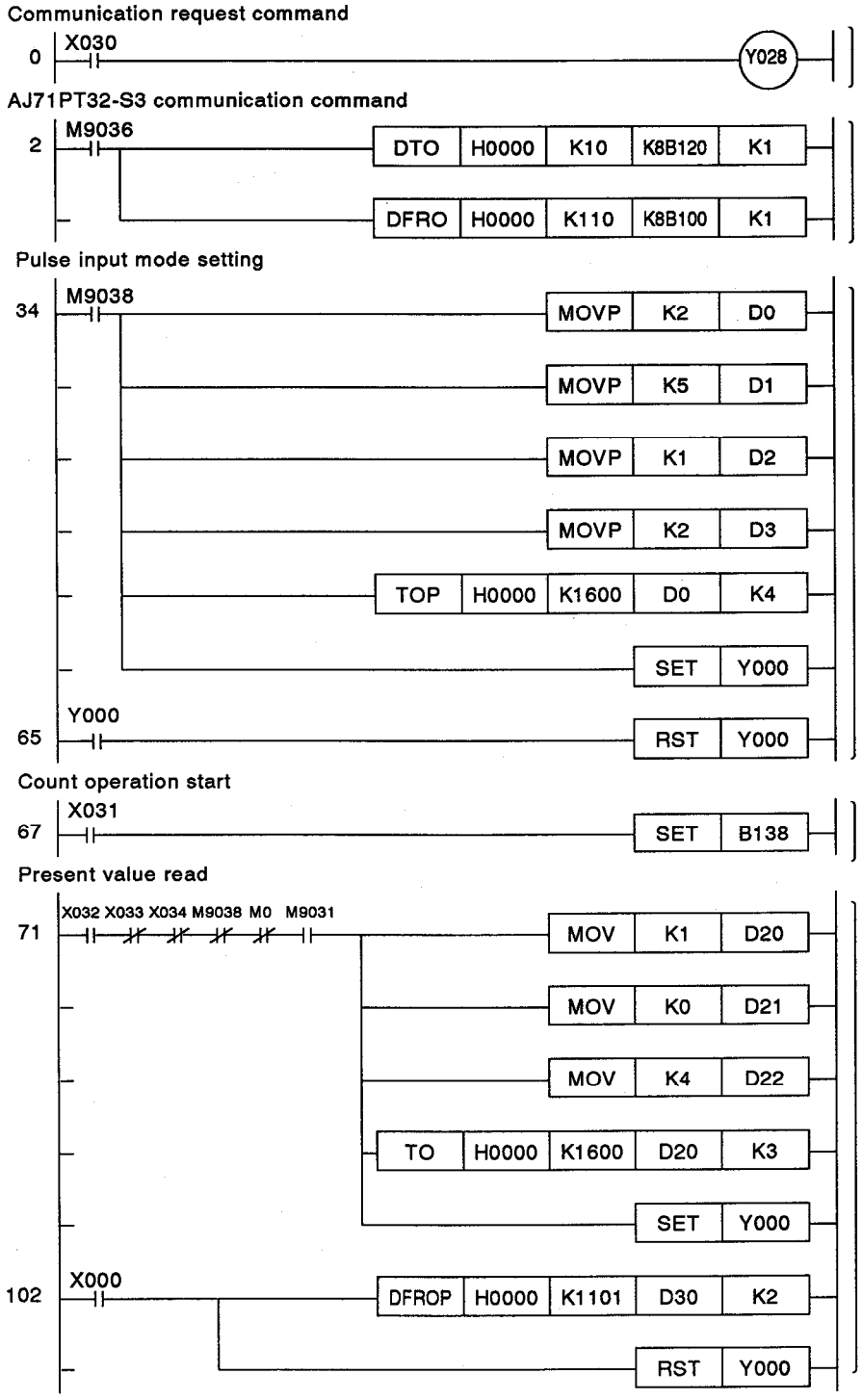
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command ..... M9038
(b) Communication request command ..... X30
(c) Count operation start command ..... X31
(d) Present value read command, counter function value read command ..... X32
(e) Counter function setting command ..... X33
(f) Periodic time setting command ..... X34
(g) Periodic pulse counter command ..... X35
(h) Communication error reset command ..... X36
(i) Count operation stop command ..... X37

(2) Relationship between the data register and the buffer memory






Starts A1S/AJ71PT32-S3 communications.

Always writes and reads to/from A1S/AJ71PT32-S3.

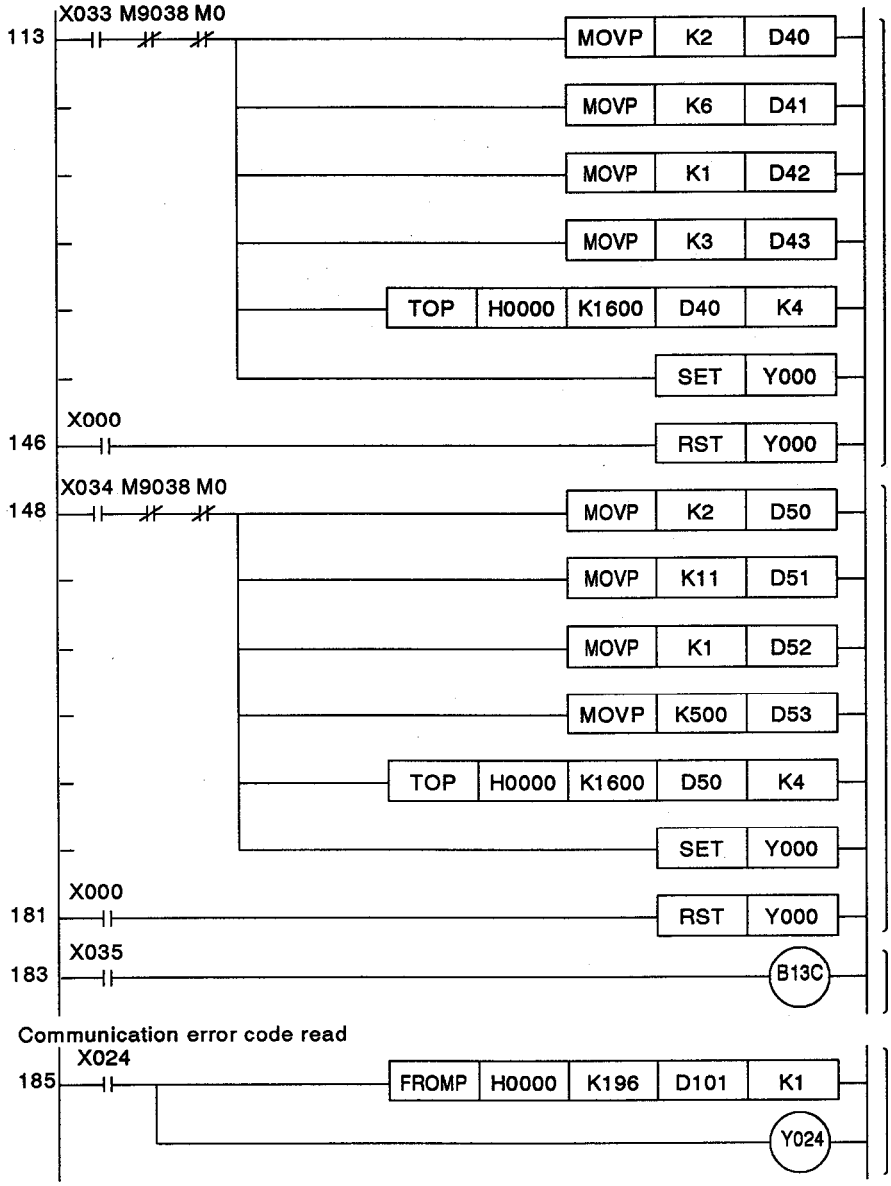
Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.

Reads the counter function selection count value and stores it to devices D32 to D33.

Periodic pulse counter command




Sets the periodic pulse counter function.

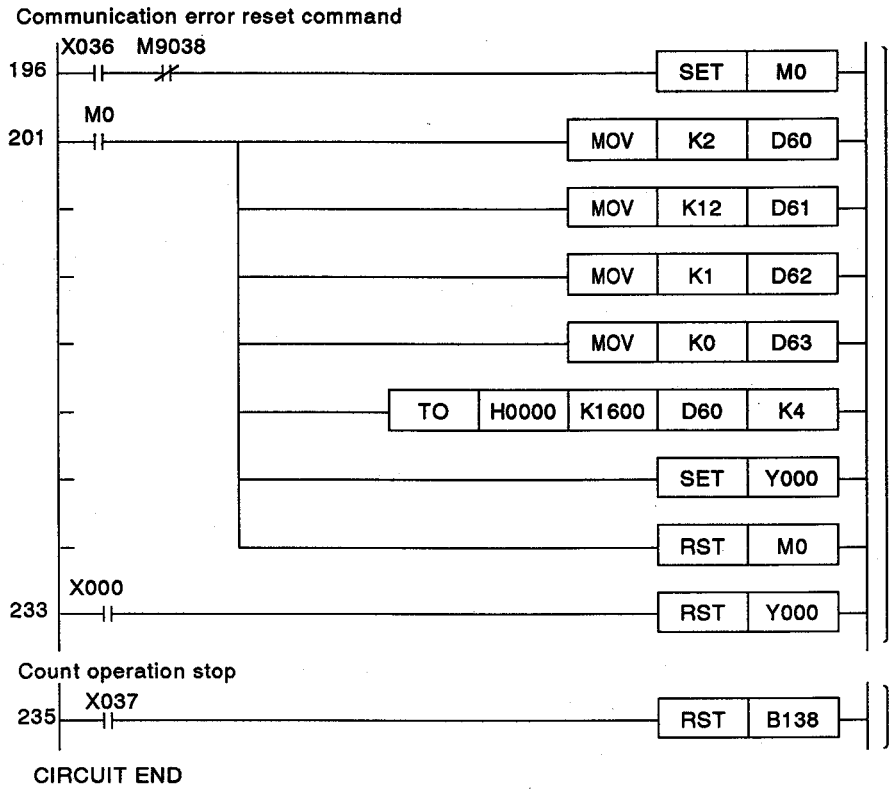
Sets the periodic time.

Executes the periodic pulse counter.

Communication error code read




Reads the communication error code and stores it to device D101.




Resets the communication error.

Stops the pulse count using the count enable command (RST).

### 7.6.7 Count disable function programming example

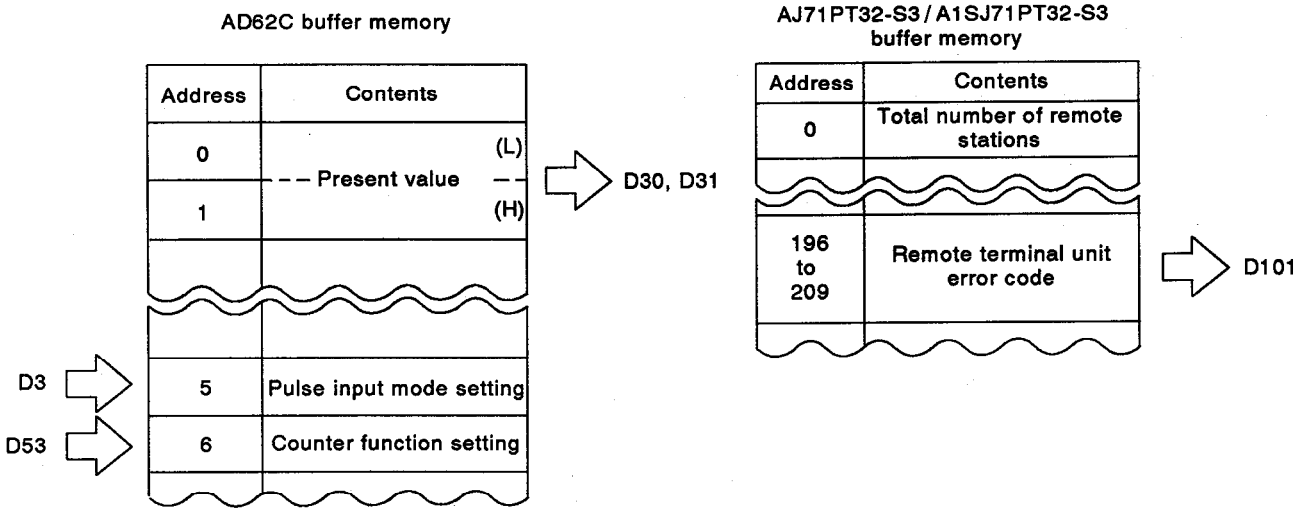
Create a program to count 2-phase pulses multiplied by one and to execute the count disable function.

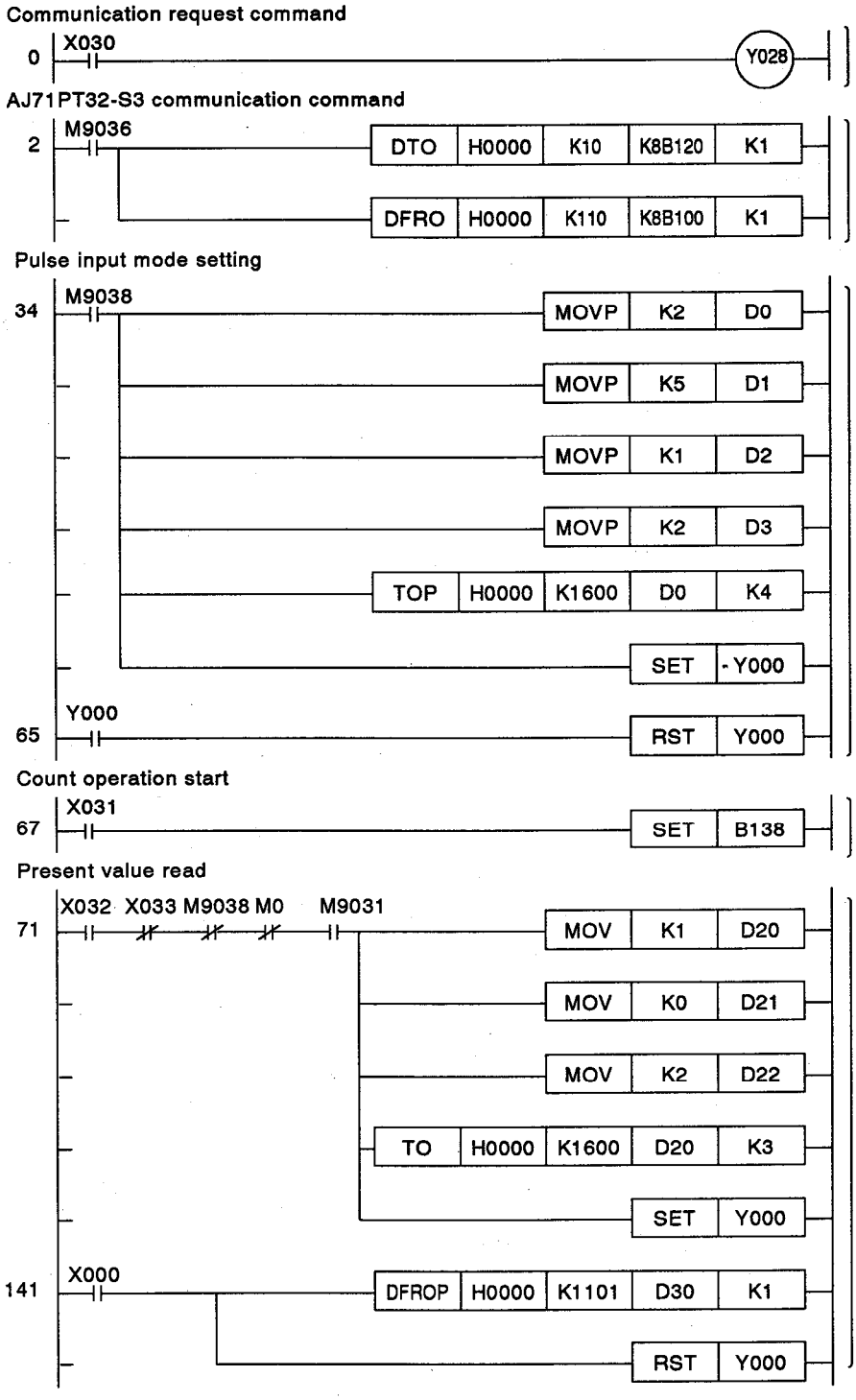
**[Devices to be used]**

(1) Execution commands

(a) Pulse input mode setting command.....M9038
(b) Communication request command.....X30
(c) Count operation start command.....X31
(d) Present value read command.....X32
(e) Count disable function setting command.....X33
(f) Count disable start command.....X34
(g) Communication error reset command.....X35
(h) Count operation stop command.....X36

(2) Relationship between the data register and the buffer memory






Starts A1S/AJ71PT32-S3 communications.

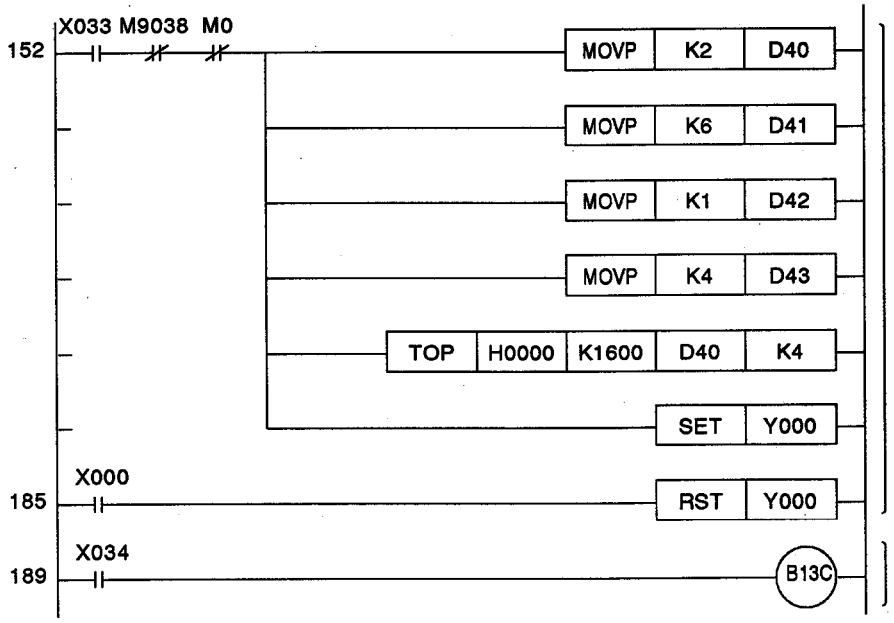
Always writes and reads to/from A1S/AJ71PT32-S3.

Sets the pulse mode consistent with the 2-phase pulse input multiplied by one.

Starts the pulse count using the count enable command (SET).

Reads the present value and stores it to devices D30 to D31.

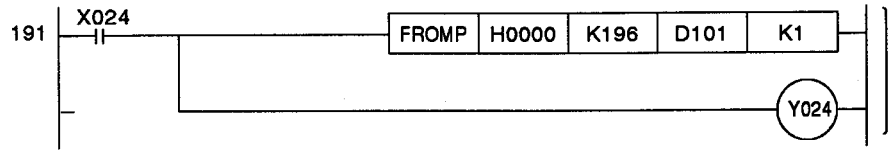
Count disable command




Sets the count disable function.

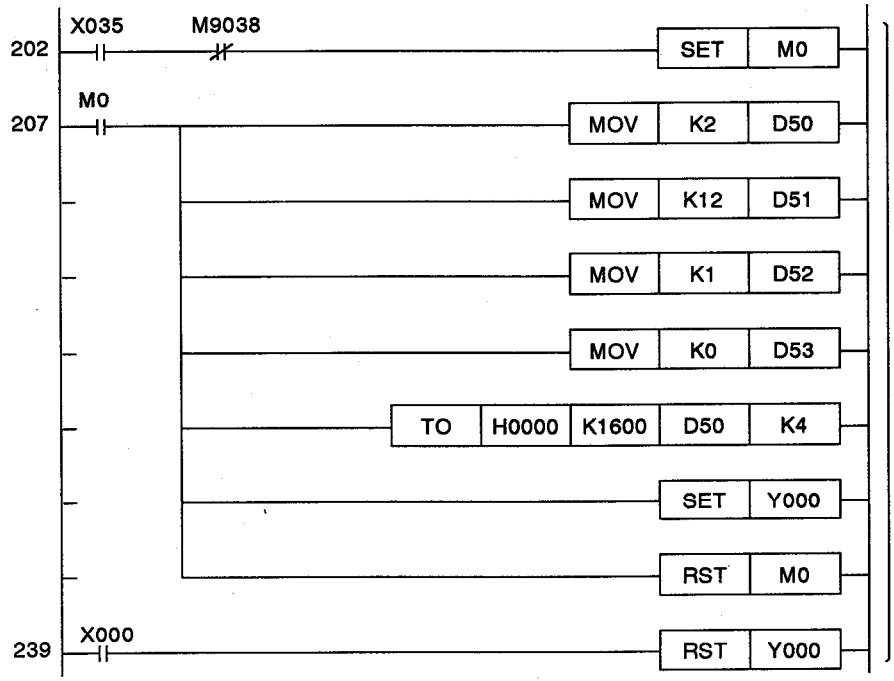
Executes the count disable.

Communication error code read




Reads the communication error code and stores it to device D101.

Communication error reset command




Resets the communication error.

Count operation stop


Stops the pulse count using the count enable command (RST).

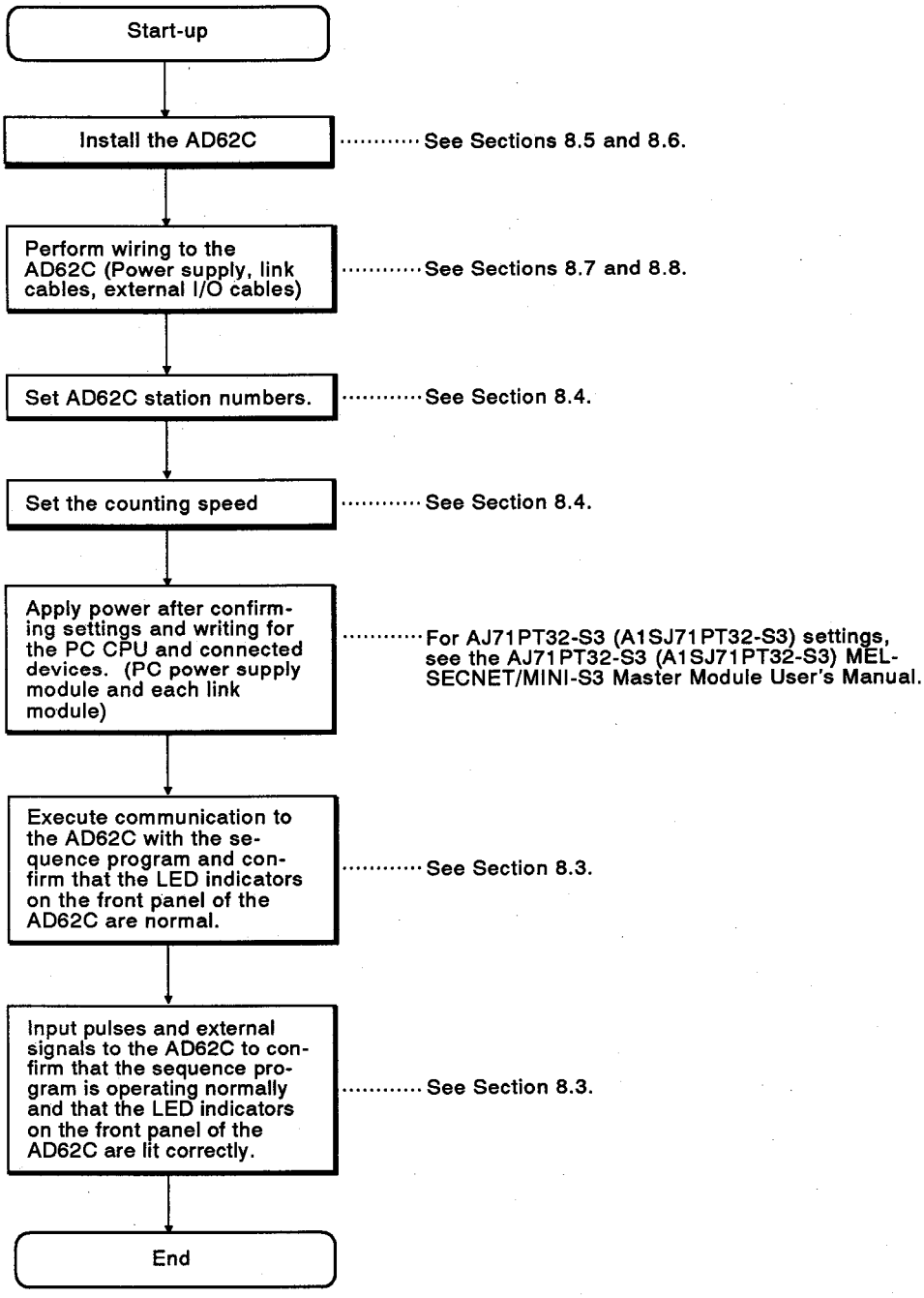
CIRCUIT END

# 8. INSTALLATION AND PRE-OPERATION SETTING PROCEDURES

Pre-operation procedures for the AD62C, the names and settings for each part of the AD62C, and the wiring method are explained in this section.

## 8.1 Pre-Operation Setting Procedures

Pre-operation setting procedures for the AD62C are explained below.



## 8.2 Handling Precautions

Handling precautions for the AD62C are explained below.

(1) The case is aluminum diecast. However, since the LED display is made of resin and the printed circuit board is embedded in the case, protect it from impact.

(2) Do not remove the printed circuit board from the case.

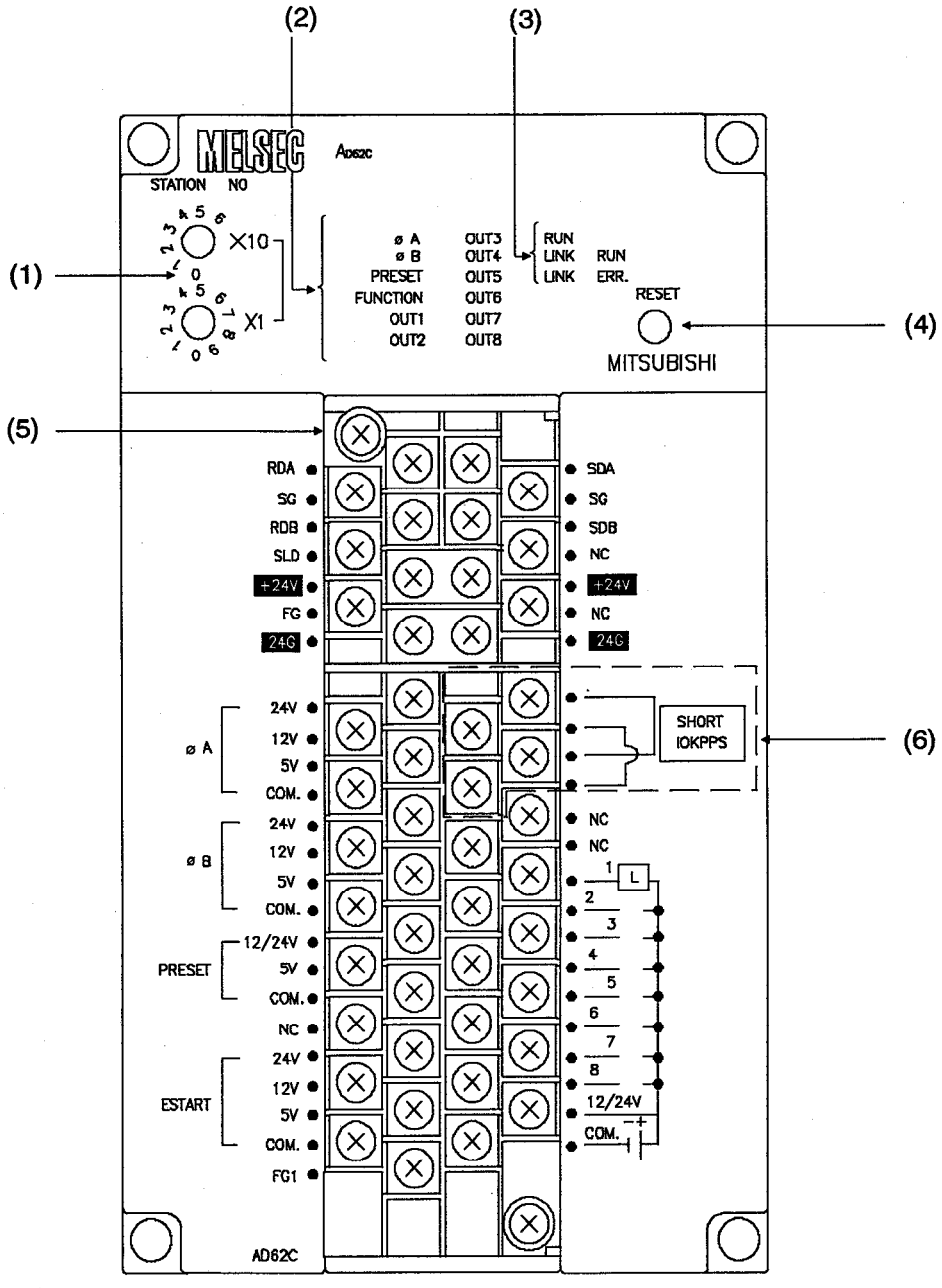
(3) When wiring, be sure that no wire offcuts remain around the terminal block.

(4) Tighten the terminal block's terminal screws (M3.5 screw) within a tightening torque range of 69 to 98 N-cm.

(5) Tighten the AD62C's installation screws (M4 screw) within a tightening torque range of 78 to 118 N-cm.

## 8.3 Nomenclature

This section gives the nomenclature of the AD62C.

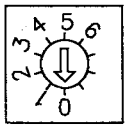
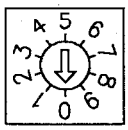


<table>
<tr><th>Nos.</th><th>Names</th><th>Descriptions</th></tr>
<tr><td>(1)</td><td>Station number setting switches</td><td>• Sets the station number from 01 to 61 using rotary switches.<br>• Station 00 is a bypass function. (Section 8.4.1 gives details.)</td></tr>
<tr><td>(2)</td><td>Operating state indicator LEDs</td><td>Operating state indicator LEDs
<table>
<tr><th>LED Names</th><th>Confirmation Contents</th></tr>
<tr><td>øA (A input indicator)</td><td>Lit when voltage is applied to the phase A pulse input terminal.</td></tr>
<tr><td>øB (B input indicator)</td><td>Lit when voltage is applied to the phase B pulse input terminal.</td></tr>
<tr><td>PRESET<br>(external preset input detection)</td><td>• Lit and latched when voltage is applied to the preset input terminal.<br>• OFF when the external preset detection reset signal is ON.</td></tr>
<tr><td>FUNCTION</td><td>Lit when voltage is applied to the F.START terminal.</td></tr>
<tr><td>OUT 1 to OUT 8</td><td>Limit switch output function.<br>Lit by turning ON the limit switches of each channel.<br>Turned OFF by turning OFF the limit switches of each channel.</td></tr>
</table></td></tr>
<tr><td>(3)</td><td>Operating state indicator LEDs</td><td>Operating state, error contents, etc. indicator LEDs
<table>
<tr><th>LED Names</th><th>Confirmation Contents</th></tr>
<tr><td>RUN</td><td>• ON ····· Running normally<br>• Flashing ···· Write data error *1<br>• OFF ····· 24 VDC is OFF or a WDT error *1</td></tr>
<tr><td>LINK RUN</td><td>• ON ····· Link is normal.<br>• OFF ····· Link error detected during power ON. *1</td></tr>
<tr><td>LINK ERR.</td><td>• ON ····· Detected. *1<br>• OFF ····· Link is normal.</td></tr>
</table>
*1: Section 9 gives details about errors.</td></tr>
<tr><td>(4)</td><td>Reset switch</td><td>AD62C hardware reset (initialization) switch</td></tr>
<tr><td>(5)</td><td>I/O terminal block</td><td>• Terminal block for data link cable wiring, 24 V power supply wiring, and I/O wiring.<br>(Sections 8.7 and 8.8 give details about wiring.)</td></tr>
<tr><td>(6)</td><td>Count speed switching terminal</td><td>• Switches setting between 50K and 10K by shorting or opening these terminals. (Section 8.4.2 gives details.)</td></tr>
</table>

## 8.4 Settings

### 8.4.1 Station number settings

(1) This section explains settings for the AD62C station number setting switches.

| | Settings |
|---|---|
|  X 10<br>  X 1 | (1) Tens digit switch: Sets the first digit of the station number.<br>(2) Ones digit switch: Sets the second digit of the station number.<br>(3) Set station numbers in the range of 01 to 61. (occupies 4 stations/module)<br>(4) Set station number 00 as a bypass function (relay). |

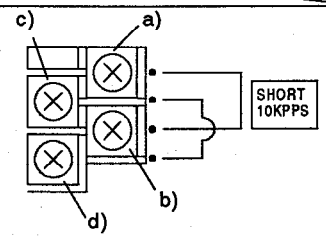
(2) The switch number is factory-set to "00".

(3) For precautions about station number settings when connected to a MELSECNET/MINI-S3, see the following manuals:

- A2CCPU User's Manual
- AJ71PT32-S3 (A1SJ71PT32-S3) MELSECNET/MINI-S3 Master Module User's Manual

### 8.4.2 Counting speed settings

(1) This section explains counting speed settings.

| | Settings |
|---|---|
|  | (1) The counting speed is set to 10K pulses/s by shorting a) and b) or c) and d) using a silkscreen print.<br>(2) The counting speed is set to 50K pulses/s by opening a), b), c), and d) (no terminal is connected). |

(2) Counting speeds can be set by changing the settings as indicated below.

(a) When the counting speed is set to 50K pulses/s:

Pulses to a maximum of 50K pulses/s can be counted in both 1-phase and 2-phase inputs.

(b) When the counting speed is set to 10K pulses/s.

Pulses to a maximum of 10K pulses/s in 1-phase input or to a maximum of 7K pulses/s in 2-phase input can be counted.

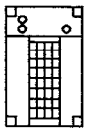
## 8.5 Mounting Procedures

This section gives mounting procedures of the AD62C including mounting directions and use of the DIN rail adapter.

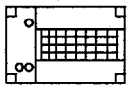
### 8.5.1 Mounting directions

(1) The AD62C can be mounted in any direction (Front side must not face downward.)

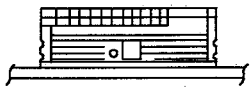
(2) Examples



Upright



Horizontal



Front side up

### 8.5.2 DIN rail adapter

This section describes the specifications and handling instructions of the DIN rail adapter.

(1) Type · dimensions · weight

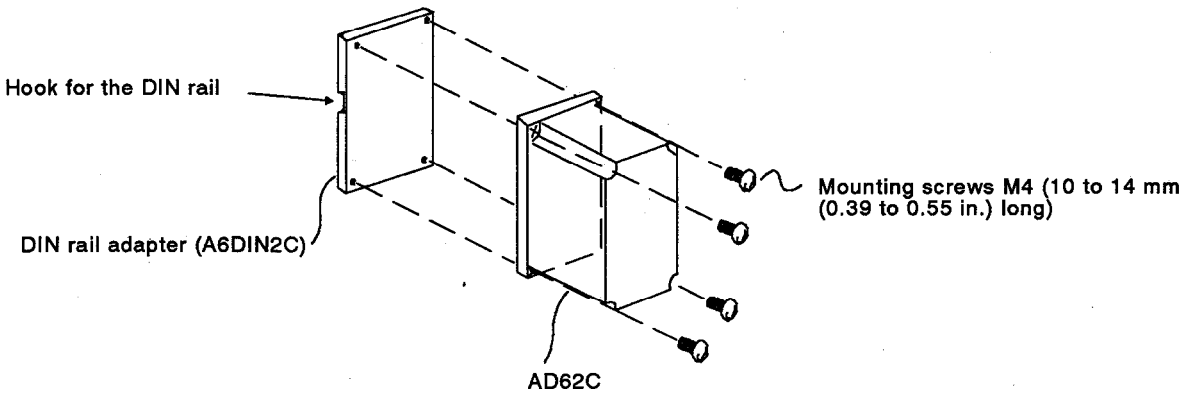
| Type | A6DIN2C |
|---|---|
| Dimensions | 172 (6.77) x 104 (4.09) x 10 mm (0.39 in) |
| Weight | 0.1 kg |

(2) Handling instructions

(a) Do not drop or give hard shocks to the DIN rail adapter since it is made of plastic.

(b) Use 4 M4 screws 10 mm to 14 mm (0.55 in. to 0.39 in.) long to attach a DIN rail adapter to a module. Torque range should be 78 to 118 N-cm.

(3) Attaching to the AD62C module



### 8.5.3 Mounting to the DIN rail

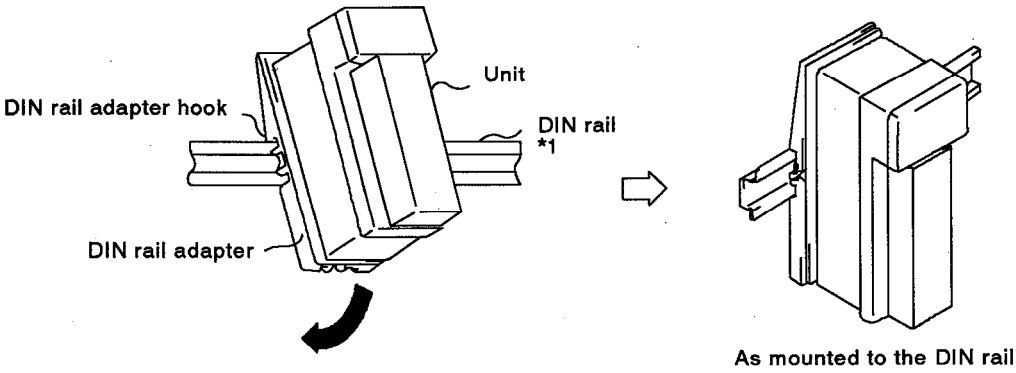
Installation to and removal from the DIN rail is explained below.

(1) Mounting procedure

After attaching the DIN rail adapter to the unit, mount the unit to the DIN rail as follows.

(a) Engage the hook of the adapter with the rail from above the rail.

(b) Push the unit onto the rail and attach it in position.




*1: The A2CCPU(P21/R21) User's Manual gives details about DIN rail mounting intervals.

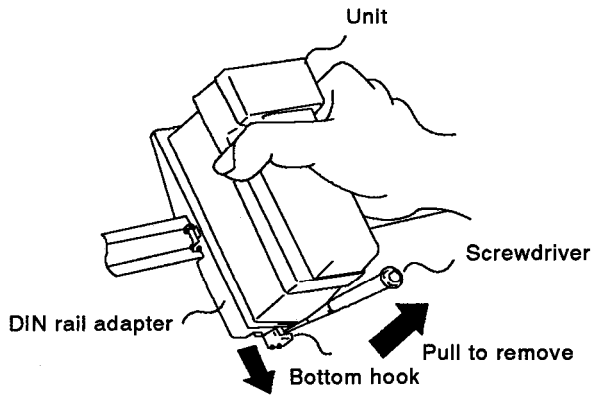
(c) When two adapters with unit are mounted to the rail side by side without leaving a clearance between them, a 4 mm (0.16 in.) clearance is allowed between the units. (See Appendix 2. External Dimensions for dimensions of the DIN adapter.)

(2) Removing procedure

Remove the unit from the DIN rail as follows.

(a) Pull down the bottom hook of the adapter using a screwdriver.

(b) Pull the unit away from the rail while pulling down the bottom hook.



## 8.6 Wiring of Data Link Cables

### 8.6.1 Handling instructions for twisted pair cables

Handle cables with special care.

(1) Do not press on the cable with rigid and sharp-edged material.

(2) Do not twist the cable too much.

(3) Do not put strong tension the cable.

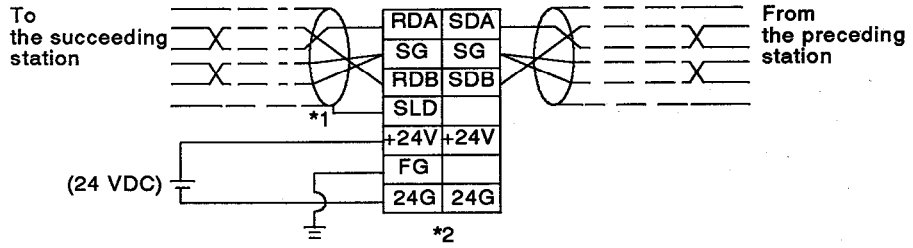
(4) Do not step on the cable.

(5) Do not put things on the cable.

(6) Do not damage the insulation of the cable.

### 8.6.2 Twisted pair cable connections

Twisted pair cables are connected as shown below.




*1: Wire the shield to the SLD terminal.

*2: Terminal screws are M3.5 screws. Use solderless terminals matching terminal screws.

**POINTS**

Twisted pair cables must be connected so that they may not be influenced by noise or surge induction.

(1) Do not lay the cables close to nor bind them together with main circuit wires, high-tension wires or load carrying wires. (allow 100 mm (3.94 in.) or more clearance)

(2) When connecting to a remote module terminal block, allow maximum clearance between twisted pair cables and module power supply lines and I/O signal wires.

(3) Do not use a part of twisted pair cables (such as 1 pair among 3 pairs) for power supply.

## 8.7 Connecting External Devices

### 8.7.1 Wiring instructions

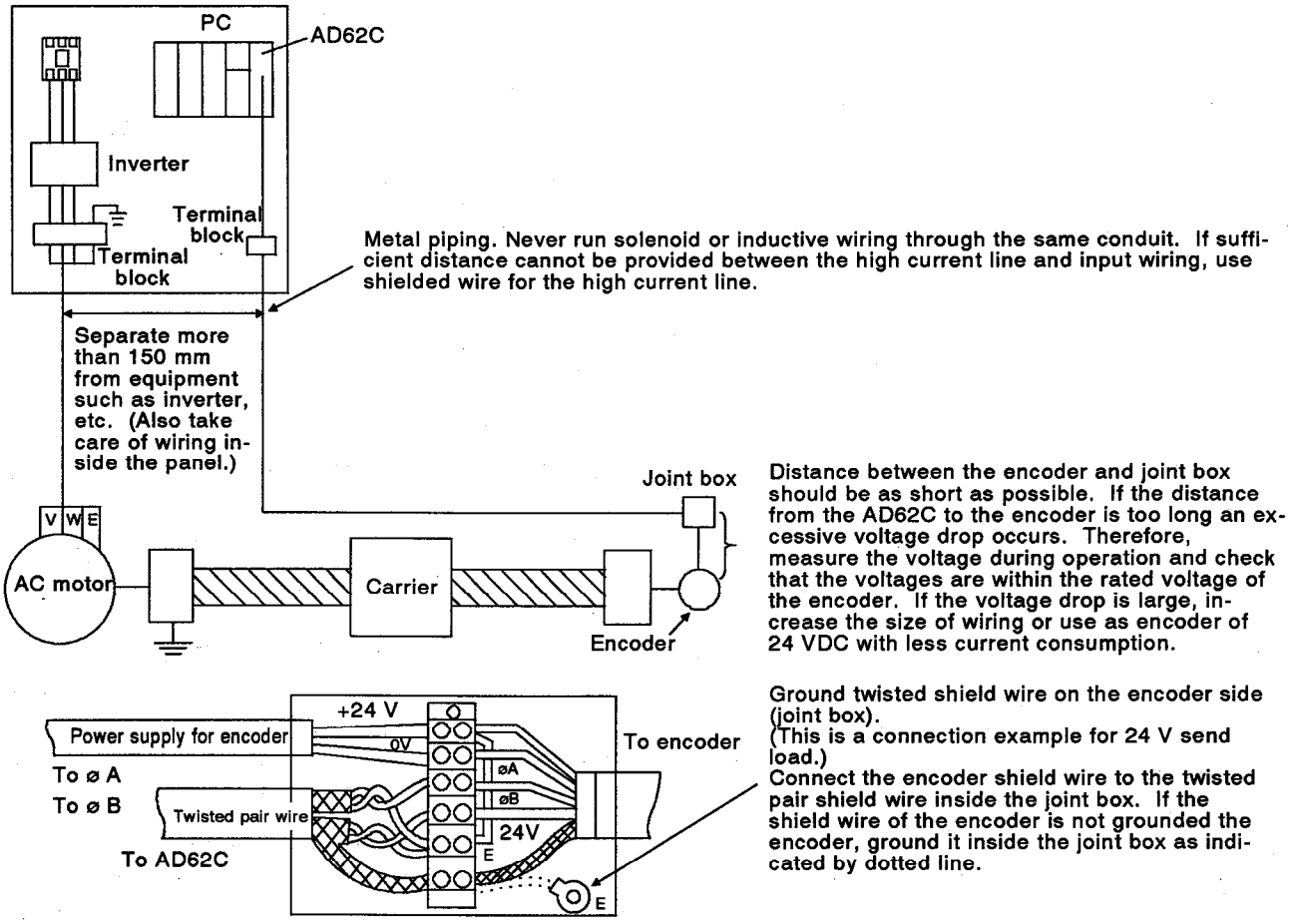
(1) When using high speed pulse inputs, take the following precautions against wiring noise.

(a) Be sure to use shielded twisted pair cables. Also provide Class 3 grounding.

(b) Do not run a twisted pair cable in parallel with power cables or other I/O lines which may generate noise. Run cables at least 150 mm (5.91 in.) away from the above described lines and over the shortest distance possible.

(2) For 1-phase input, connect the count input signal only to phase A; for 2-phase input, connect to phases A and B.

(3) If the AD62C picks up pulse noises, it will miscount.
Noise precautions are shown below.



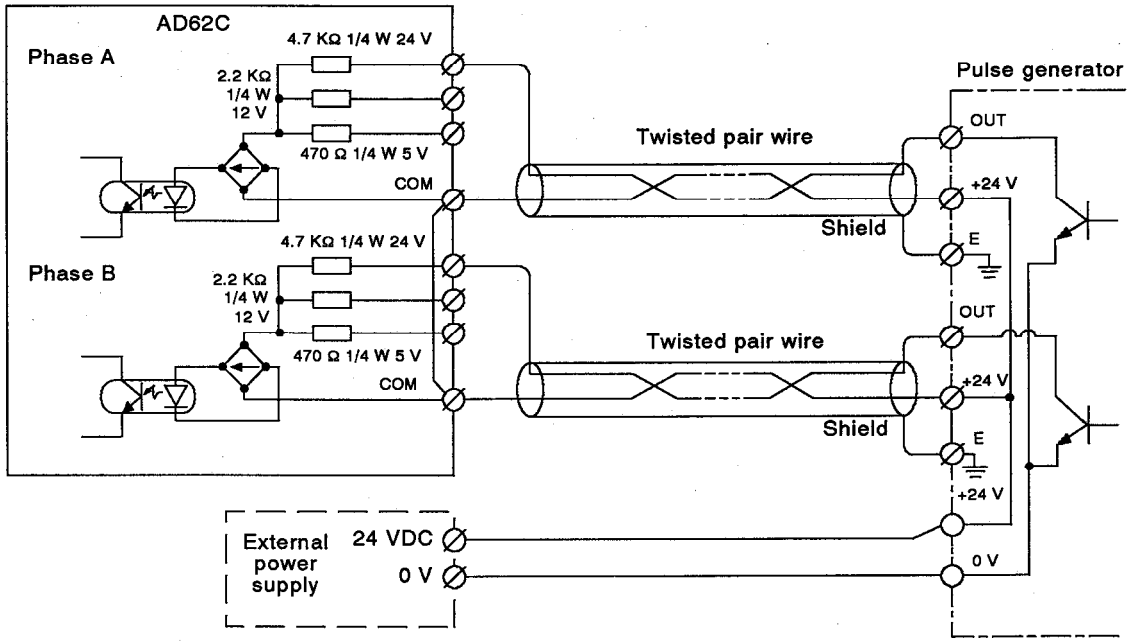

**POINT**

Before applying power to the pulse generator, confirm that the power supply matches the voltage indication levels of phase A and B input terminals. Applying 24 V to a 5 V terminal will cause damage to pulse generator.

### 8.7.2 Wiring example for the connection of the unit to the pulse generator

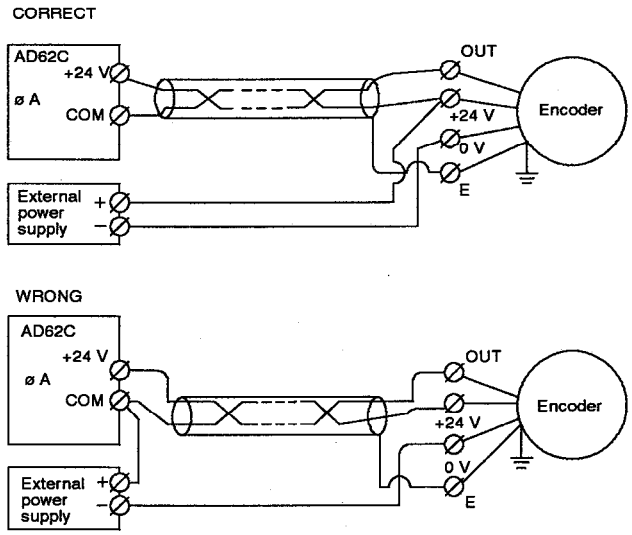
(1) Wiring example for the connection with the open collector output pulse generator

Connection of a 24 VDC pulse generator



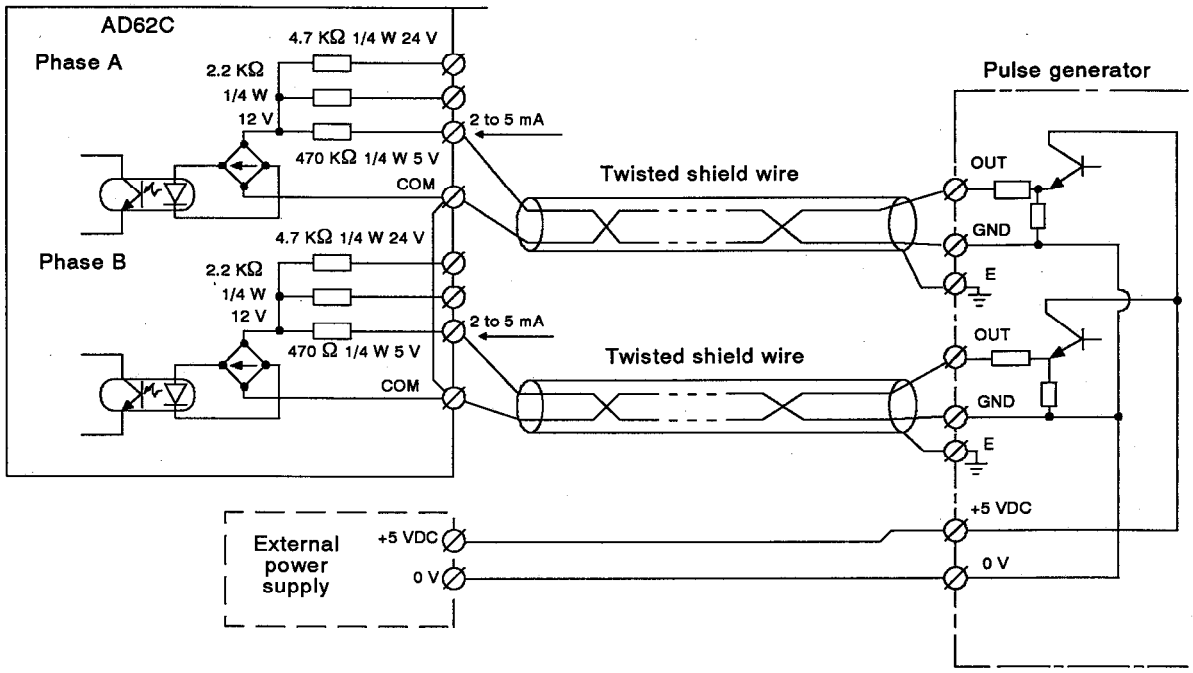

**POINT**

In order to minimize any interference from noise on the encoder power supply, the encoder signal and supply lines should be wired as follows:



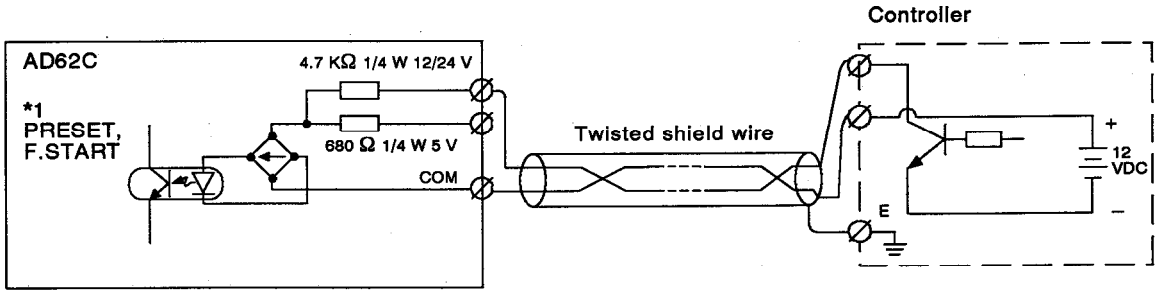
(2) Voltage output pulse generator and wiring examples

Connection of 5 VDC pulse generator



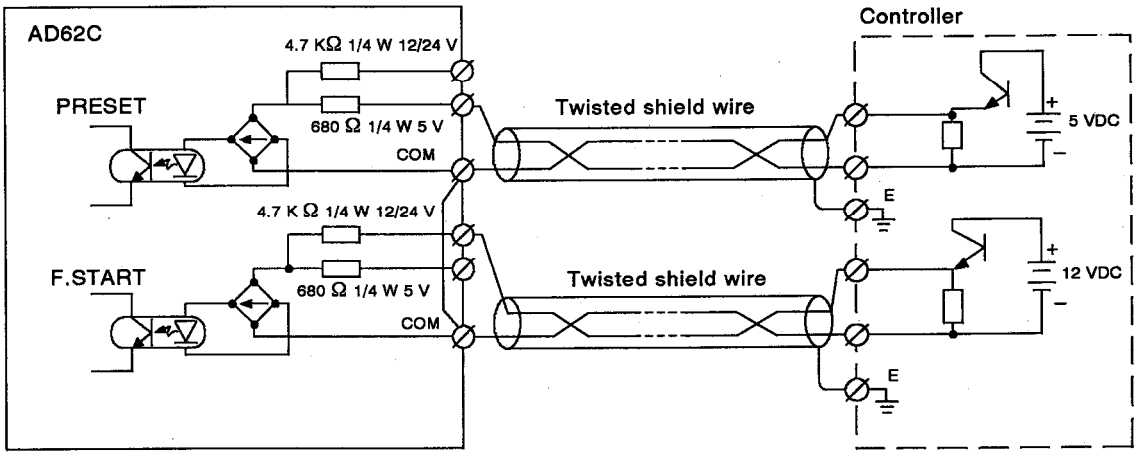
### 8.7.3 Wiring example for the connection of a controller to external input terminals (PRESET, F.START)

(1) Connection of a controller to AD62C external input terminals (PRESET, F.START)



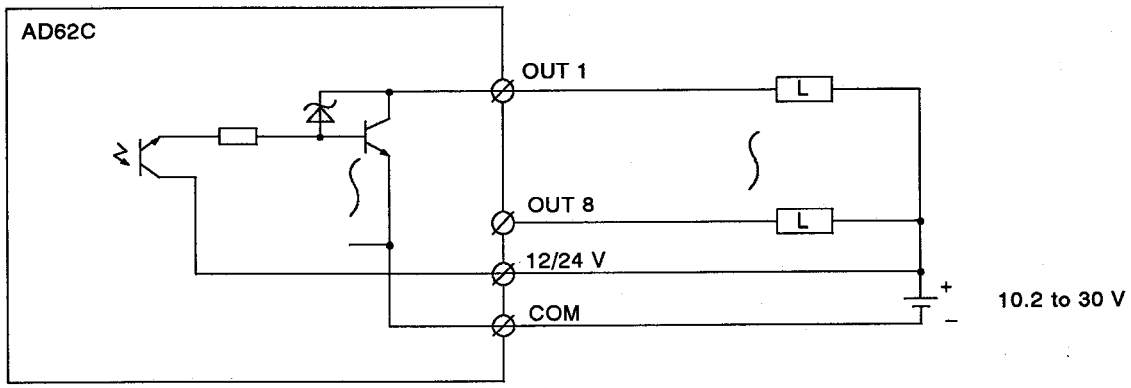

*1: The interface for PRESET input and F.START input is the same.

(2) Connection of source load (voltage output type)




### 8.7.4 Wiring examples at external output (OUT 1 to OUT 8) terminals

To use the OUT terminals, the internal photocoupler should be activated. For this purpose, 10.2 to 30 V external power is necessary. Connection methods are as follows:



# 9. TROUBLESHOOTING

This section explains the AD62C error codes, LED indications, and troubleshooting for count operation errors.

## 9.1 Error Codes

(1) If an error occurs (RUN LED flashes) when executing a FROM/TO instruction, the error codes shown in Table 9.1 will be stored to buffer memory (address 12) for communications error code storage, or to (address 13) for multiple-dog setting error storage.

**Table 9.1 Error Code List**

| Errors | Error Codes | Causes | Corrective Actions |
|---|---|---|---|
| Communication errors | 100 | Data has been read from buffer memory address 150 or later. | Correct the sequence program from which address 150 or later has been read. |
| | 101 | Data has been written to buffer memory addresses 0 to 4, or 150 or later. | Correct the sequence program from which addresses 0 to 4, or 150 or later have been read. |
| | *1 102 | A command other than read (01H) or write (02H) has been received. | Take appropriate measures to prevent noise interference. Execute communications again. |
| | *1 103 | "0" number of read/write specified words has been received. | |
| | *1 104 | Data has been received when a FROM instruction is executed. | |
| | *1 105 | The number of words specified for write command data is different of that of received data. | |
| | 110 | A value outside the range of 0 to 4 was set to the pulse input mode setting buffer memory (address 5) | See Section 4, and set a value from 0 to 4. |
| | 111 | A value outside the range of 0 to 4 was set to the counter setting buffer memory (address 6). | See Section 3, and set a value from 0 to 4. |
| | 112 | "0" was set to the sampling/periodic time setting buffer memory (address 11). | Set a value within the range of 1 to 65535. |
| | 113 | The preset value is the same as the ring counter value. | Set the values so that they are not the same. |
| | 114 | A preset value or counter value was written do the buffer memory while the ring counter command (Y1B) was ON. | Turn OFF the ring counter command, cancel the ring counter function, and execute the write. |
| Multiple-dog setting error | 2( )[ ] | The ON/OFF position data setting values of dogs 0 to 3 for a channel are not in ascending order. | Set the limit switch output ON/OFF position data so that the values are in ascending order for each dog. |
| | 3( )[ ] | A value outside the range of 0 to 4 was set in the multiple-dog setting. | Set a value of 0 to 4. |

*1: These errors occur because of noise. Therefore, attempt the same operation again, and/or take appropriate measures to prevent noise interference.

( ) indicates a channel containing the first error during an operation.

[ ] indicates a dog containing the first error during an operation.

(2) The error codes for communication errors and multiple-dog setting errors are reset as shown below.

| Errors | Reset Operations |
|---|---|
| Communi-cation errors | • Switch ON the communications error detection reset signal (Y04).<br>• Write "0" to buffer memory address 12. |
| Multiple-dog setting errors | • Switch ON the multiple-dog setting error detection reset signal (Y1F).<br>• Write "0" to buffer memory address 13. |

## 9.2 RUN LED is Flashing/OFF

(1) When flashing

| Check Item | Corrective Action |
|---|---|
| Is there data which cannot be written to or read from the AD62C? | Read the AD62C error code, confirm using the error code list in Section 9.1, and correct the sequence program. |

(2) When OFF

| Check Items | Corrective Actions |
|---|---|
| Is the 24 VDC power supply charged? | • Turn ON the power supply. |
| Is the 24 VDC within the rated voltage? | • Set the voltage to 15.6 to 31.2 V. |
| Is the wiring correct? | • Check for cut wires and erroneous wiring and correct. |
| Is there a hardware fault detected (watchdog timer error)? | • After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.)<br>• If the LED is OFF, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative. |

## 9.3 LINK RUN LED is OFF

| Check Items | Corrective Actions |
|---|---|
| Is the RUN LED lit? | • When the RUN LED is flashing or OFF, correct according to Section 9.2. |
| Is a hardware error detected? | • After confirming that the power supply is correct, turn it ON/OFF repeatedly. (Confirm whether or not the link hardware is faulty because of noise, etc.)<br>• If the LED is OFF, AD62C link hardware is faulty. Consult your nearest Mitsubishi representative. |

## 9.4 LINK ERR.LED is ON

| Check Item | Corrective Actions |
|---|---|
| Is the communication cable wiring correct? | • Confirm whether link data communication is disabled due to cable wire breakage, terminal block faulty connections, or wiring faults, and correct.<br>• If the LED does not turn OFF when the wiring is correct, AD62C link hardware is faulty. Consult your nearest Mitsubishi representative. |

## 9.5 Count Value Is Incorrect

| Check Items | Corrective Actions |
|---|---|
| Is the counter input specification correct? | • Check the counter input with the specification conditions in Section 2.2. |
| Is the sequence program data handled in 32-bit binary? | • Correct the sequence program so that its data can be handled in 32-bit binary. |
| Is the phase setting for the sequence program input pulses correct? | • Set 0 to 4 (see Section 4) to the mode register. (The default value is 0.) |
| Is twisted shield wire used for counter input wiring? | • Use twisted shield wire for counter input wiring. |
| Are spurious counter values related to the operation of other equipment? | • Separate wiring of related equipment. |
| Does noise come in through the ground of the AD62C? | • Disconnect the AD62C from the ground.<br>• If the AD62C contacts the ground, separate it from the ground. |
| Have adequate measures been taken against noise in the panel? | • Provide CR surge suppression to magnetic switches, etc. |
| Is sufficient distance provided between heavy current equipment and counter input line? | • Independently wire counter input line. Separate wire in panel 150 mm (5.91 in.) or more from power line. |
| Do the pulse input waveform, rise, and fall conform to the specifications? | • Monitor and confirm the input waveform using a synchroscope. If the rise and fall are outside the specified values, resulting in a faulty waveform, correct the waveform. |

(1) If counter operations cannot be executed correctly even if the above check items are correct, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative.

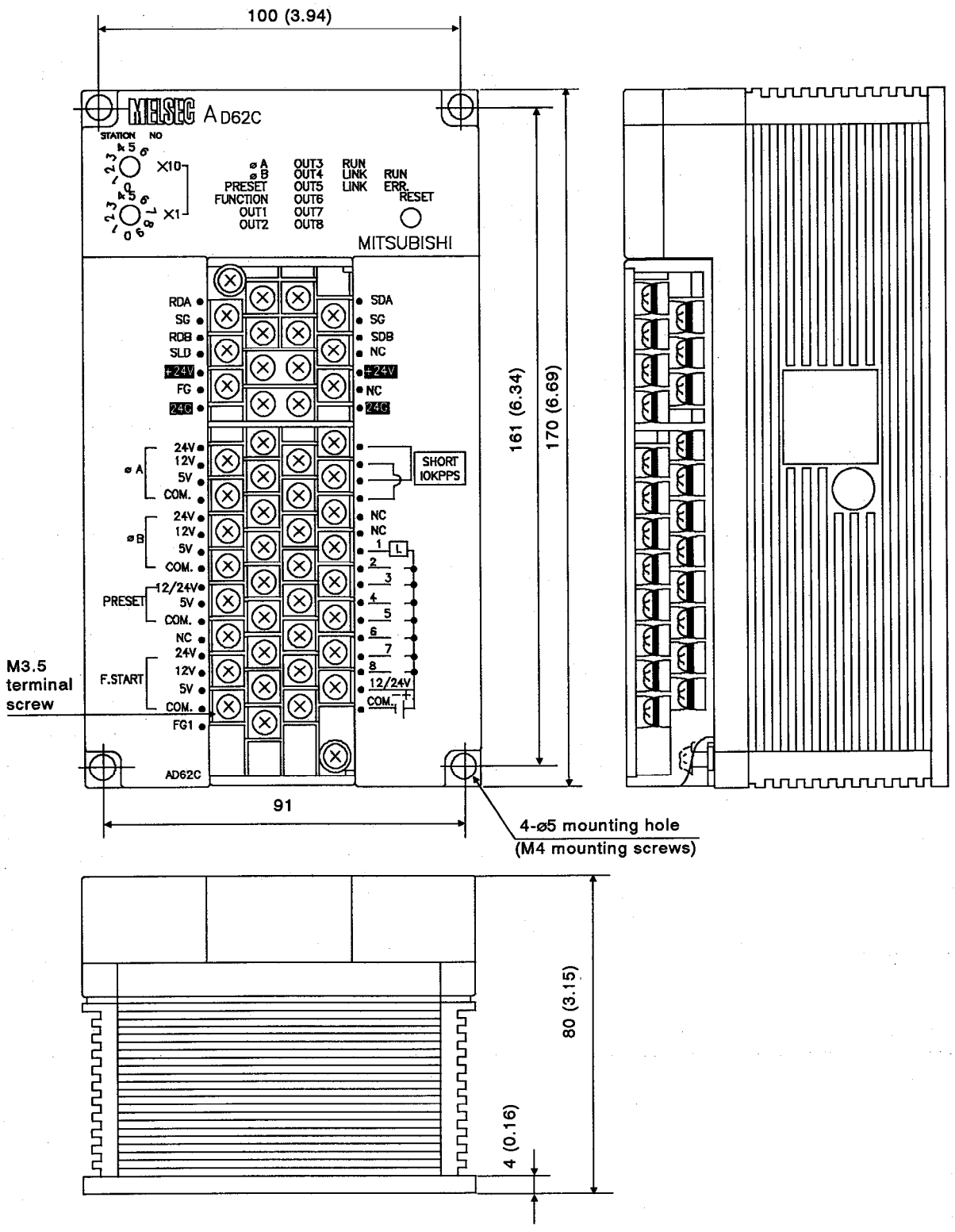
## 9.6 Count Operations Not Executing

| Check Items | Corrective Actions |
|---|---|
| Are the RUN and LINK RUN LEDs lit? | • Correct according Sections 9.2 and 9.3 if they are flashing or OFF. |
| Is the LINK ERR. LED OFF? | • Correct according to Section 9.4 is the LINK ERR. LED is ON. |
| Is the external wiring of phases øA and B correct? | • Check the external wiring and correct. |
| Are phases øA and øB LEDs lit by directly applying voltage to the count input terminal? | • If yes, check the external wiring and pulse generator and correct.<br>• If no, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative. |
| Is the enable LED ON? | • If it is OFF, correct the sequence program so that it is turned ON. |
| Do the set AD62C station number and the station number specified by the sequence program match? | • With the A2CCPU, match the AD62C station number and program setting.<br>• With the AJ71PT32-S3 (A1SJ71PT32-S3), match the program setting to the AJ71PT32-S3 (A1SJ71PT32-S3) buffer memory corresponding to the AD62C station number. |
| Is the phase specified to the AD62C buffer memory by the sequence program written with a correct value? | • Set the 1-phase specification of phase øA to the mode register or correct. |
| Are the PC CPU or AJ71PT32-S3 (A1SJ71PT32-S3) indicating an error? | • If it is the PC CPU, refer to the troubleshooting section of the manual of the PC CPU being used for corrective procedures.<br>• If it is the AJ71PT32-S3 (A1SJ71PT32-S3), return to the normal operating state according to the troubleshooting section of the AJ71PT32-S3 (A1SJ71PT32-S3) manual. |
| Is the counter function selection start command (Y1C) ON; or is the voltage applied to the F.START terminal? | • When the count disable function was set by the counter function selection, turn OFF Y1C or the F.START terminal. |

(1) If count operations cannot be executed even when the above check items are correct, the AD62C hardware is faulty. Consult your nearest Mitsubishi representative.

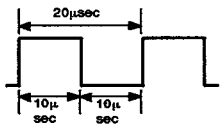
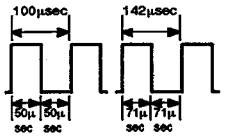
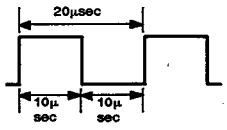
# APPENDICES

## APPENDIX 1 DIMENSION



## APPENDIX 2 COMPARING THE AD62C AND AD61C

### Table 1 Performance Comparison

| Item | | | Specifications | | |
|---|---|---|---|---|---|
| | | | AD62C | | AD61C |
| | | | Counting Speed Setting (50K) | Counting Speed Setting (10K) | |
| Number of I/O occupied points | | | 32 | | |
| Number of channels | | | 1 | | 2 |
| Count input signal | Phase | | 1-phase input, 2-phase input | | |
| | Signal level (øA, øB) | | 5 VDC / 12 VDC / 24 VDC } 2 to 5 mA | | |
| Counter | Counting speed | 1-Phase input | 50K pulse/s | 10K pulse/s | 50K pulse/s |
| | | 2-Phase input | 50K pulse/s | 7K pulse/s | 50K pulse/s |
| | Counting Range | | -2147483648 to 2147483647 (signed 32-bit binary) | | 0 to 16777215 (signed 32-bit binary) |
| | Type | | UP/DOWN preset counter + ring counter function | | |
| | Min. Count pulse width (Input leading edge/fall time should be 5 µsec or less; duty ration is 50 %.) | |  (1-phase input, 2-phase input) |  (1-phase input) (2-phase input) |  (1-phase input, 2-phase input) |
| Comparison output | Comparison range | | Signed 32-bit binary | | Signed 24-bit binary |
| | Comparison results | | Limit switch output<br>NO contact operation:<br>Dog ON address ≤ Counter value ≤ Dog OFF address<br>NC contact operation:<br>Dog OFF address ≤ Counter value ≤ Dog ON address | | Set value < Counter value<br>Set value = Counter value<br>Set value > Counter value |
| External input | | | Preset / Function start | 12/24 VDC, 3/6 mA 5 VDC, 5 mA | Preset / Count disable | 12/24 VDC, 3/6 mA 5 VDC, 5 mA |
| External output | | | Comparison output | Transistor (open collector) output 12/24 VDC, 0.1 A/point, 0.8 A/common | Match output | Transistor (open collector) output 12/24 VDC, 0.3mA |
| Current consumption | | | 24 VDC, 0.15 A | | 24 VDC, 0.15 A | |

# WARRANTY

Please confirm the following product warranty details before using this product.

## 1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.
However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

### [Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.
Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

### [Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

## 2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
(2) Product supply (including repair parts) is not available after production is discontinued.

## 3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

## 4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

## 5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

## 6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.
In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.
However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

# High Speed Counter Module Type AD62C

# User's Manual

| | |
|---|---|
| MODEL | AD62C-U-E |
| MODEL CODE | 13JE17 |
| IB(NA)-66400-B(0410)MEE | |

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : 1-8-12, OFFICE TOWER Z 14F HARUMI CHUO-KU 104-6212,JAPAN
NAGOYA WORKS : 1-14 , YADA-MINAMI 5-CHOME , HIGASHI-KU, NAGOYA , JAPAN