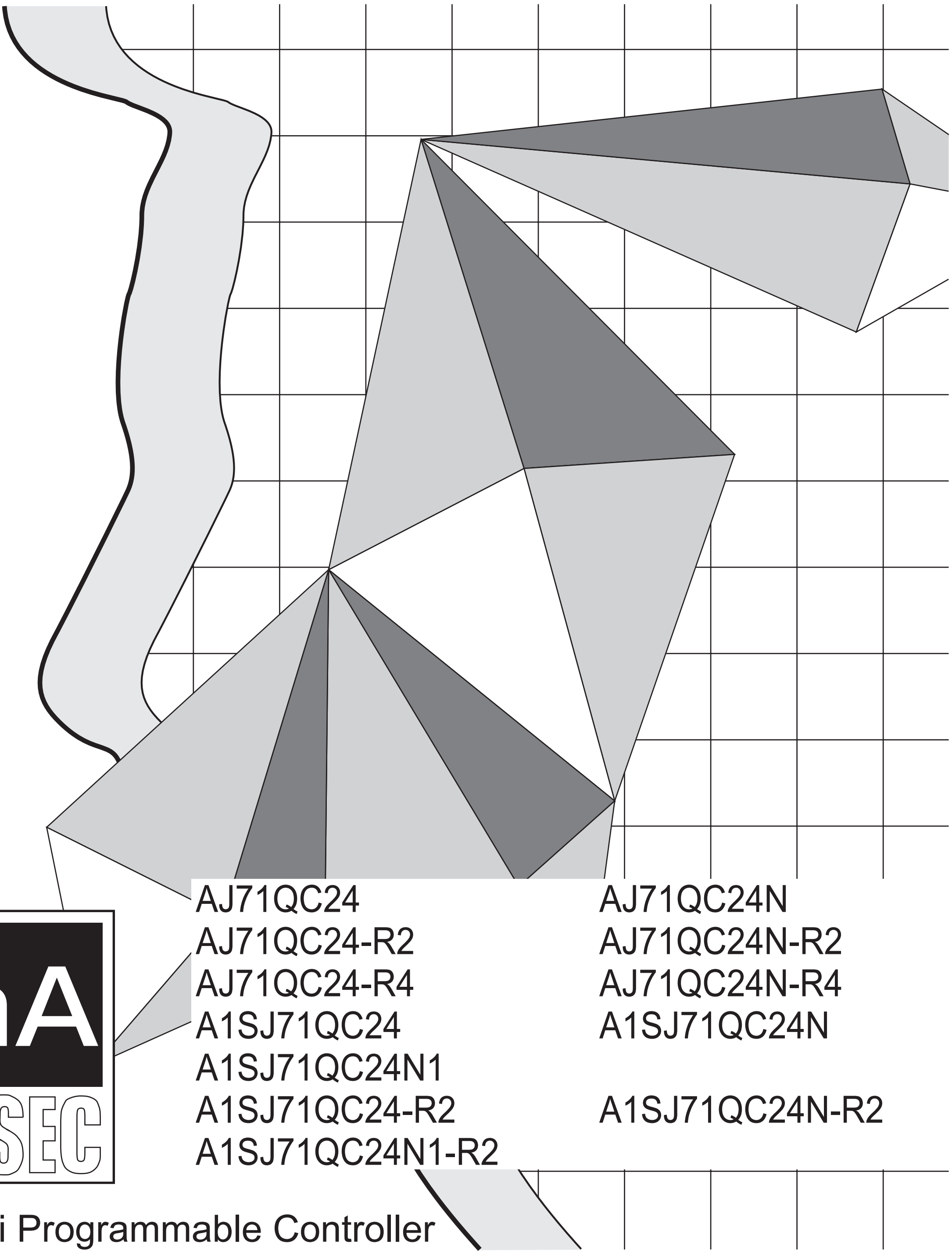
MITSUBISHI

QnA SERIES

Serial Communications Module

User's Manual (Modem Function Additional Version)



AJ71QC24
AJ71QC24-R2
AJ71QC24-R4
A1SJ71QC24
A1SJ71QC24N1
A1SJ71QC24-R2
A1SJ71QC24N1-R2

AJ71QC24N
AJ71QC24N-R2
AJ71QC24N-R4
A1SJ71QC24N
A1SJ71QC24N-R2

Mitsubishi Programmable Controller

● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual. Also pay careful attention to safety and handle the module properly.

These precautions apply only to Mitsubishi equipment. For the safety instructions of the programmable controller system, please read the user's manual of the CPU module to use.

These ● SAFETY PRECAUTIONS ● classify the safety precautions into two categories: "⚠WARNING" and "⚠CAUTION".

⚠WARNING	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠CAUTION	Indicates that incorrect handling may cause hazardous conditions, resulting in minor or moderate injury or property damage.

Depending on circumstances, procedures indicated by ⚠CAUTION may also be linked to serious results.

In any case, it is important to follow the directious for usage.

Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠WARNING

- When using the notification function, the pager receiver may not be contacted due to the frequency transmission status from the system setup environment and error on the receiver side.
  To ensure the safety of the PLC system, install a call circuit with a lamp display or buzzer sound.
- When performing the control of the PLC in operation (especially changing data, program, and operation status (remote run/stop)) by connecting a personal computer, etc. to the special function module, configure an interlock circuit in a sequence program so the safety of the overall system is always maintained.
  Especially, when this control is performed to a remote PLC from an external device, troubles that have occurred on the PLC side may not be able to immediately be handled if there is a data communication error. Define a troubleshooting agreement between external devices and the PLC CPU for data communication error occurrences, as well as construct an interlock circuit in the sequence program.

⚠CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 100mm (3.9 inch) or more from each other.
  Not doing so could result in noise that would cause malfunction.

[INSTALLATION PRECAUTIONS]

⚠CAUTION

- Use the PLC in an environment that meets the general specifications contained in the User's manual of the CPU module. Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, malfunction, and damage to or deterioration of the product.
- Before installing or placing wiring, be sure to shut off all phases of external power supply used by the system. If you do not switch off the external power supply, it will cause electric shock or damage to the product.
- While pressing the installation lever located at the bottom of module, insert the module fixing tab into the fixing hole in the base unit until it stops. Then, securely mount the module with the fixing hole as a supporting point.
  (The Q2AS series module shall be fastened by screws in the base module at the specified torque.)
  If the module is not properly installed, it may result in malfunction, failure, or fallout.
- Tighten the screws within the range of specified torque.
  If the screws are loose, it may result in fallout, short circuits, or malfunction.
  Tightening the screws too far may cause damage to the screw and/or the module, resulting in fallout, short circuits, or malfunction.
- Do not directly touch the module's conductive parts or electronic components. Doing so could cause malfunction or failure in the module.

[WIRING PRECAUTIONS]

⚠CAUTION

- Be sure to fix communication cables leading from the module by placing them in the duct or clamping them. Cables not placed in the duct or without clamping may hang or shift, allowing them to be accidentally pulled, which may result in a module malfunction and cable damage.
- Perform correct pressure-displacement, crimp-contact or soldering for wire connections using the tools specified by the manufactures. Attach connectors to the module securely.
- Before connecting the cables, check the type of interface to be connected.
  Connection, or erroneous wiring, to the wrong interface may failure the module and external devices.
- When connecting an external device to the AJ71QC24(N)-R4 RS-422 interface, do not connect a device that must receive power from the AJ71QC24(N)-R4.
  If you connect the device, it will cause failure to the module or external device.
- Tighten the terminal screws within the range of specified torque.
  If the terminal screws are loose, it may result in short circuits or malfunction.
  Tightening the screws too far may cause damage to the screw and/or the module, resulting in fallout, short circuits, or malfunction.
- When detaching the communication cable from the module, do not pull the cable portion. For cables with connectors, hold the connector at the junction to the module, then detach it. For cables without connectors, first loosen the screw at the junction, then detach the cable.
  Pulling the cable portion while it is connected to the module may cause a malfunction or damage to the module and cable.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module.
  Such debris could cause fires, failure, or malfunction.

[STARTING AND MAINTENANCE PRECAUTIONS]

⚠WARNING

- Do not touch the connector while the power is on. Doing so could cause malfunction.
- Before cleaning or retightening screws, be sure to shut off all phases of the external power supply used by the system. If you do not switch off the external power supply, it will cause failure or malfunction of the module. If the screws are loose, it may result in fallout, short circuits, or malfunction. Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

⚠CAUTION

- Do not disassemble or modify the modules. Doing so could cause failure, malfunction, injury, or fire.
- Before mounting or removing the module, be sure to shut off all phases of external power supply used by the system. If you do not switch off the external power supply, it will cause failure or malfunction of the module.
- Always make sure to touch the grounded metal to discharge the electricity charged in the body, etc., before touching the module.
  Failure to do so may cause a failure or malfunctions of the module.

[OPERATING PRECAUTIONS]

⚠WARNING

- Do not write data into the “system area” of the buffer memory of special function modules. Also, do not output the “prohibited to use” signal as the output signal to a special function module from the PLC CPU.
  Writing data into the “system area” or outputting a signal for “prohibited to use” may cause system malfunction in the PLC.

⚠CAUTION

- Before performing the control of the PLC in operation (especially changing data, program, and operation status (remote run/stop)) by connecting a personal computer, etc. to the special function module, read this manual carefully and confirm if the overall safety is maintained.
  Failure to perform correct operations to change data, program, or the status may result in system malfunction, machine damage, or an accident.
- When using the module while values, such as buffer memory set values, are registered in the EEPROM, do not turn off the power supply for the module loading station nor reset the PLC CPU. If the power supply for the module loading station is turned off or the PLC CPU is reset while any values are registered, the data contents in the EEPROM become inconsistent and as a result the values must be set again in the buffer memory, etc. and reregistered to the EEPROM. Also, this may cause failure and malfunction of the module.

[DISPOSAL PRECAUTIONS]

⚠CAUTION

- When disposing of this product, treat it as industrial waste.

● CONDITIONS OF USE FOR THE PRODUCT ●

(1) Mitsubishi C Controller system ("the PRODUCT") shall be used in conditions;
i) where any problem, fault or failure occurring in the PRODUCT, if any, shall not lead to any major or serious accident; and
ii) where the backup and fail-safe function are systematically or automatically provided outside of the PRODUCT for the case of any problem, fault or failure occurring in the PRODUCT.

(2) The PRODUCT has been designed and manufactured for the purpose of being used in general industries.
MITSUBISHI SHALL HAVE NO RESPONSIBILITY OR LIABILITY (INCLUDING, BUT NOT LIMITED TO ANY AND ALL RESPONSIBILITY OR LIABILITY BASED ON CONTRACT, WARRANTY, TORT, PRODUCT LIABILITY) FOR ANY INJURY OR DEATH TO PERSONS OR LOSS OR DAMAGE TO PROPERTY CAUSED BY the PRODUCT THAT ARE OPERATED OR USED IN APPLICATION NOT INTENDED OR EXCLUDED BY INSTRUCTIONS, PRECAUTIONS, OR WARNING CONTAINED IN MITSUBISHI'S USER, INSTRUCTION AND/OR SAFETY MANUALS, TECHNICAL BULLETINS AND GUIDELINES FOR the PRODUCT.
("Prohibited Application")
Prohibited Applications include, but not limited to, the use of the PRODUCT in;

- Nuclear Power Plants and any other power plants operated by Power companies, and/or any other cases in which the public could be affected if any problem or fault occurs in the PRODUCT.
- Railway companies or Public service purposes, and/or any other cases in which establishment of a special quality assurance system is required by the Purchaser or End User.
- Aircraft or Aerospace, Medical applications, Train equipment, transport equipment such as Elevator and Escalator, Incineration and Fuel devices, Vehicles, Manned transportation, Equipment for Recreation and Amusement, and Safety devices, handling of Nuclear or Hazardous Materials or Chemicals, Mining and Drilling, and/or other applications where there is a significant risk of injury to the public or property.

Notwithstanding the above, restrictions Mitsubishi may in its sole discretion, authorize use of the PRODUCT in one or more of the Prohibited Applications, provided that the usage of the PRODUCT is limited only for the specific applications agreed to by Mitsubishi and provided further that no special quality assurance or fail-safe, redundant or other safety features which exceed the general specifications of the PRODUCTs are required. For details, please contact the Mitsubishi representative in your region.

REVISIONS

* The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
Mar. 1996	IB-66612-A	First edition
Sep. 1996	IB-66612-B	Correction: Section 1.3, 1.4 (Table), 1.5.2 (Table), 2.1 (1) (2), 2.2 (1) (3), 2.3.2 (2) (Table),2.3.3 (2) (Table), 2.4.2 (1), 3.1 (Table), 3.2.1 (1) (2) (3), 4.2, 4.3 (POINT), 4.3.2 (9), 4.4, 4.5.1, 4.6.1, 4.6.2, 4.7.1, 4.7.2 (1) (3) (POINT), 4.7.3 (1) (POINT), 4.9.1 (1) (POINT), 5.4.1 (Table), 5.4.2 (1) (Table), 5.7 (4), 5.9 (6), 6.1.5 (Note), 6.2.1 (1) (3) (Table), 6.2.10 (1) (2) (3), 6.3.1, 6.3.1.1, 6.3.2, 6.3.2.2 (Table), 6.5.1 (1), 6.6.1 (2), 6.6.4 (POINT), 6.6.6 (2) (POINT), 6.6.7 (2) (POINT), 6.7.1 (1) (Table), 6.13.1 (2), 8.6.1 (Table), 11.3.3②, 11.3.4, 11.8 (4), 12.1.2 (Table), 14.7 (Table), 14.7.1 (2), 16.4 (POINT), 21.2.12, 21.2.13, 21.2.14, Appendix 4, Appendix 5 Addition: Section 1.1.2 (2), 1.3, 1.5.1 (1) (Table), 2.2 (1) (3), 2.3 (Table), 3.1 (Table), 3.2.1, 3.5 (2), 4.1, 4.2, 4.3.2 (Table) (9), 4.4, 4.5.1, 4.5.2, 4.6.1, 4.6.2, 4.7.1, 4.7.2 (2), 4.7.3 (1), 4.9, 4.9.2, 4.10, 5.4.1 (Table), 5.4.2 (1) (Table), 5.9 (7), 6.1.4 (5) (POINT), 6.1.5 (1), 6.2.1 (3) (POINT), 6.3, 6.3.2, 6.3.2.1, 6.3.2.2, 6.3.2.3, 6.3.2.4, 6.6.1 (2), 8.6.2 (1), 8.7 (4), 14.2 (2), 14.5.3, 15, 16.3 (1), 16.4 (2) (POINT), 19.2 (Table), 21.2.11, Appendix 4, Appendix 5
Apr. 1998	IB-66612-C	Correction: Entire manual (A1SJ71QC24N (-R2) and Corresponding Additional Explanation for AJ71QC24N (-R2/R4) (SH-3630-B) reflected, as well as revision of contents and numbering of chapters/sections due to additions of the above named chapters and sections, change of abbreviation (QC24 → QC24(N)) Section 1.5.1 (1), 2.2, 3.5 (POINT), 5.4.1, 6.3.2.2 (1), 9.3.4 (1), Appendix 3.1 (1) Addition: "Safety Precautions", Entire manual (A1SJ71QC24N (-R2) added, Corresponding Additional Explanation for AJ71QC24N (-R2/R4) (SH-3630-B)
Sep. 1998	IB-66612-D	Correction: Section 3.3.1(2), 3.3.3(2), 4.2(2) (3)*2, 4.3.2, 4.7.4(1)(b), 5.4.3(2)②, 6.2.1(3), Appendix 5 Addition: Section 4.2*4, 6.2.1(3)*2

Print Date	*Manual Number	Revision
Jan. 1999	IB-66612-E	Correction: Summary of contents (Chapter 14, Chapter 22 and number of pages in appendix have been changed) Contents (Chapter 14, Chapter 22, Appendix), Section 3.2.1(3), 3.3.1(3), Section 4.3.2(3)①, Section 6.2.1((3)Table 6.1, *2), Section 11.3.3(2)(Buffer memory diagram), Section 14.8.4 to 14.11(page number), Section 16.1.2(2), Appendix 1.1.1(2)(b)②③, Index Addition: Contents (Appendix 8), Section 1.2.1(2) Point(2), Section 3.3.1(*), Section 14.8.2 Point(4), 14.8.3(Point (4), Remark), Section 22.2(Remark), Appendix 8
Jan. 2000	IB-66612-F	Correction: Safety Precautions, Section 1.4, 1.5.1(1), Section 2.2(3), Section 3.3.3(2), Section 4.3.2(9), 4.5.1(2), 4.9.1, Section 5.2(Point), 5.4.1, 5.4.3, Section 6.1(2)③, 6.3.2.2, 6.7.2(2), 6.7.3(2), Section 11.3.1(Point), Section 18.4.1, 18.5.1, Whole secion of 20.4 (Control data), Section 21.4.8(3), 21.4.9(2), Section 22.1.1(7F24H), Appendix 3.1(2)(3), Appendix 4 Addition: Section 4.7.3(1)(h), 4.7.4(1)(f), Section 5.9(8), 5.10, Section 22.1.1(7164H)
Mar. 2003	IB-66612-G	Correction: Safety Precautions, Section 4.3.1, 4.3.2, Section 5.4.1, 5.7, Section 6.2.1, 6.2.10, Section 7.4.1, Section 8.4.1, 8.4.2, Section 9.1, 9.3.1, 9.3.4, Section 12.6, 12.7.2, Section 13.1.2, 13.1.3, 13.2.2, Section 14.7.1, 14.7.3, 14.9, Section 16.4.4, Section 18.4.2, Section 21.1, 21.2, 21.3.2, 21.3.4, 21.3.5, 21.4, 21.5.1, Section 22.1.1, 22.1.4, Appendix 6, Appendix 7, Appendix 8 Addition: Section 1.1.2(13)
Dec. 2003	IB-66612-H	Correction: Section 21.4.8(4)③
Feb. 2006	IB-66612-I	Addition model: A1SJ71QC24N1, A1SJ71QC24N1-R2 Correction: Safety Precautions, MANUALS, Section 1.1.2(11), 1.3, 1.5.1, Section 3.1, 3.3.1(2), 3.4, 3.5(40H, 21FH), Section 4.2, 4.3.2, 4.7.3(1)(d), 4.9.2, Section 5.4.1, 5.7, Section 6.2.1(3), Section 9.3.1, Section 14.1, 14.3.1, Section 19.2, Section 20.4, Section 21.3.1, 21.3.4, Appendix 5, 7 Addition: Section 14.12, Section 22.1, Appendix 1.3, 3.3

Print Date	*Manual Number	Revision
Jul.,2006	IB-66612-J	Correction: Section 3.4, 3.5, 4.9.2, 5.9, 14.1, 14.7.1, 20.4.3, 21.3.4, 22.1.1, 22.2.12 Addition: Section 19.6
Apr., 2011	IB-66612-K	Correction: Section 3.3.2, 3.3.3, 3.4, 4.6, 4.6.1, 4.6.2, 4.8.1, 9.3.4, 14.3.1, 16.1.2, 20.4.1, 20.4.2, 20.4.3, 20.4.4, 22.1.1, Appendix 1.3, Appendix 5, Appendix 7.1, WARRANTY Addition: CONDITIONS OF USE FOR THE PRODUCT

Japanese Manual Version SH-3534-N

INTRODUCTION

Thank you for purchasing the Mitsubishi programmable controller MELSEC-QnA Series.

Before using your MELSEC-QnA Series, please read this manual thoroughly to gain an understanding of the functions and performances of the QnA Series PLC so that the equipment is used to its optimum.

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MANUALS

The following manuals pertain to the serial communication module.

Related Manuals

Manual Name		Manual No. (Model Code)
AJ71QC24 Serial Communication Module Guidebook Centered about the basic functions of the serial communication module, this manual describes the basic method of transferring data with external devices using each protocol. This manual applies to all the serial communication modules. (Sold separately)		IB-66622 (13JF11)
Computer Link Module Guidebook This manual describes the basic method of transferring data with external devices (computer, etc.) in each computer link mode. Refer to it when transferring data using dedicated protocols A compatible frames. This manual applies to all the serial communication modules. (Sold separately)		SH-3510 (13JE76)
Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function) This manual describes how to use the control procedure and commands when transferring data using dedicated protocol A compatible frames. It is common to all the serial communication modules. When using commands, read Section 5.4 (description of A compatible frame commands) of this manual. (Sold separately)		SH-3511 (13JE77)
Serial Communication Module User's Manual (Hardware) This manual describes the system configuration when using the module, module specifications, settings up to operation, starting procedure, and module outline dimensions. (included in the product)	AJ71QC24	IB-66609 (13J822)
	AJ71QC24-R2	IB-66610 (13J823)
	AJ71QC24-R4	IB-66611 (13J824)
	A1SJ71QC24	IB-66686 (13J853)
	A1SJ71QC24-R2	
	AJ71QC24N	IB-66765 (13JL12)
	AJ71QC24N-R2	
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	A1SJ71QC24N	IB-66815 (13JL37)
	A1SJ71QC24N-R2	
	A1SJ71QC24N1	IB-0800330 (13JP85)
	A1SJ71QC24N1-R2	

How to Use This Manual

This manual explains functions, specifications and usage for all serial communication modules listed below:

- AJ71QC24
- AJ71QC24-R2
- AJ71QC24-R4
- A1SJ71QC24
- A1SJ71QC24-R2
- AJ71QC24N
- AJ71QC24N-R2
- AJ71QC24N-R4
- A1SJ71QC24N
- A1SJ71QC24N-R2
- A1SJ71QC24N1
- A1SJ71QC24N1-R2

Use each of the functions for the serial communication modules.

• How to use this User's Manual

When verifying functions and specifications

- Verify the functions, specifications, etc. that are common for all serial communication modules according to Chapter 1 through Chapter 3.

When starting up the module

- Verify the procedures up to the operation of the serial communication modules according to Chapter 4 and perform switch settings and connections to external devices.

When performing data communication using dedicated protocols

- Perform switch settings and connections with external devices for dedicated protocols according to Chapter 4 and start up the serial communication module.
- Verify the specifications for communication functions, initial setting items for the required buffer memory, communication procedures with external devices and cautionary notes for dedicated protocols according to Chapter 5.
- Perform initial settings for the required buffer memory according to Chapter 14.
- When accessing the PLC using the QnA frame or QnA extension frame from external devices, perform the procedure described in Chapter 6. When accessing the PLC using the QnA simplified frame, perform the procedure described in Chapter 8. When accessing the PLC from external devices using A-compatible frames, perform the procedure described in the Computer Link/Multi-Drop Link Module User's Manual (Computer Link Functions, Printer Functions).
- When sending data to external devices from the PLC CPU using the QnA frame or QnA extension frame, see Section 6.9 or Chapter 7.

When performing data communication using non-procedure protocol

- Perform switch settings and connections with external devices for non-procedure protocols according to Chapter 4 and start up the serial communication module.
- Read Chapter 9 to verify the specifications for communication functions, methods of data transmission and reception between the PLC CPU and external devices, I/O signals used, initial setting items for the required buffer memory, and cautionary items for non-procedure protocols.
- Perform initial settings for the required buffer memory according to Chapter 14.
- When communicating data with arbitrary format, perform the procedure described in Chapter 10.
- When communicating data by registering user-designated fixed message format beforehand to the serial communication module, perform the procedure described in Chapter 11.

When communicating data using bidirectional protocols

- Perform switch settings and connections with external devices for bidirectional protocols according to Chapter 4 and start up the serial communication module.
- Read Chapter 12 to verify the specifications for communication functions, methods of data transmission and reception between the PLC CPU and external devices, I/O signals used, initial setting items for the required buffer memory, and cautionary items for the bidirectional protocol.
- Perform initial settings for the required buffer memory according to Chapter 14.
- When communicating data, perform the procedure described in Chapter 13.

When using special functions

- Use the function only after verifying the function specifications and usage, I/O signals used, initial setting items for the required buffer memory and cautionary items described in Chapter 14 through Chapter 21.
- When communicating data using any of the protocols via the modem function, start up the serial communication module according to Chapter 21, perform line connection to the destination module, and then perform data communication.
- Terminate data communication according to Chapter 21.

When verifying error codes and performing troubleshooting

- Verify error contents and corrective actions according to Chapter 22.

• Verifying available functions

The AJ71QC24N(-R2, R4)/A1SJ71QC24N(-R2) are equipped with the following functions that are new from AJ71QC24(-R2, R4)/A1SJ71QC24(-R2).

Refer to the following sections and tables to verify functions available to your module:

- Specification comparison indicated in Section 1.4
- Tables shown in the upper-right corner of the first page of each chapter or section in which the corresponding function is explained.
  (Shown only on pages explaining functions that have limitations on usage availability.)

Applicable module	**AJ71QC24**			**A1SJ71QC24**		**AJ71QC24N**			**A1SJ71QC24N**	
	–	**-R2**	**-R4**	**–**	**-R2**	**–**	**-R2**	**-R4**	**–**	**-R2**
Function availability	×	×	×	×	×	△	△	△	○	○
Remark	–					Usable in software version B and later			–	

○ : Usable (No restrictions) △ : Usable (Some restrictions) × : Unusable

* For the △ indication, restrictions and applicable function versions and software versions are noted in the remark column.

• Module replacement

- Replace modules according to Appendix 1.

MEMO

COMMON

This section outlines the functions for data communication between external devices and PLC CPU through the serial communication module and describes the features and system configuration, serial communication module specifications, and procedures before starting data communications.

When using the serial communications module, read Chapters 1 to 3 once.

When starting the system, set the module switches, connect the serial communications module to the external devices, and perform a perform check according to Chapter 4.

Section 4.1 outlines the module starting procedure.

1. OVERVIEW

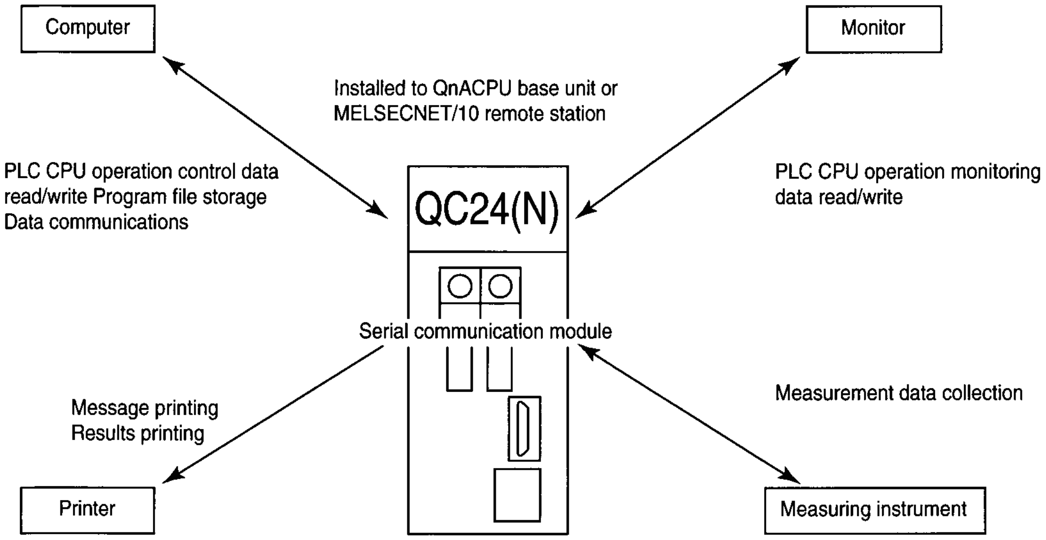
This user's manual describes the specifications, starting procedure, data communications functions, and how to use the special functions of each serial communication module listed in Section 1.3.
When applying the following program examples to the actual system, make sure to examine the applicability and confirm that it will not cause system control problems.

1.1 Overview and Features of Serial Communication Module

1.1.1 Overview

The serial communication module (hereafter called QC24(N)) is used to transfer data between an MELSEC-QnA Series PLC CPU and external devices for the following purposes.

① Read and write data handled by the PLC CPU
② Control the operation of the PLC CPU
③ Store (upload/download) PLC CPU program files
④ Transfer arbitrary data between PLC CPU and external devices



POINT

The following guidebook is available (sold separately). Use it when using the QC24 for the first time. This guidebook uses illustrations and sample programs to describe everything from switch setting to operation based on a simple system configuration so that you can easily understand how to use the basic functions of the module.
Serial Communication Module Guidebook...........IB-66622
* When using QC24N, read the manual by replacing QC24 with QC24N.

1.1.2 Features

The following describes the features common to all ten types of serial communication modules.

1 Support of three data communication functions

(a) Data communications with external devices is possible using dedicated protocols, non procedure protocol, or bidirectional protocol.

Data can be transferred between PLC CPU and external devices by setting the data communications functions for each QC24(N) interface according to the application.

- Dedicated protocols .... QC24(N) communications procedure. PLC CPU device memory can be read and written by sending command messages from external devices.
- Non procedure protocol.......... User communications procedure. Arbitrary data can be transferred between PLC CPU and external devices.
- Bidirectional protocol .... QC24(N) communications procedure. Arbitrary data can be transferred between PLC CPU and external devices.

(b) Section 1.2 outlines the data communications functions. (Detailed description Chapter 5 to Chapter 13)

2 RS-232C, RS-422, and RS-485 standard serial transfer is possible.

(a) The QC24(N) has two interfaces selected from among the RS-232C, RS-422, and RS-422/485 standards. (Detailed description Section 1.3)

(b) Serial transmission is possible by QC24(N) interface. Data can be transferred between the PLC CPU and a computer, ID module, bar code reader, controller, and other external device. (Detailed description Chapter 2)

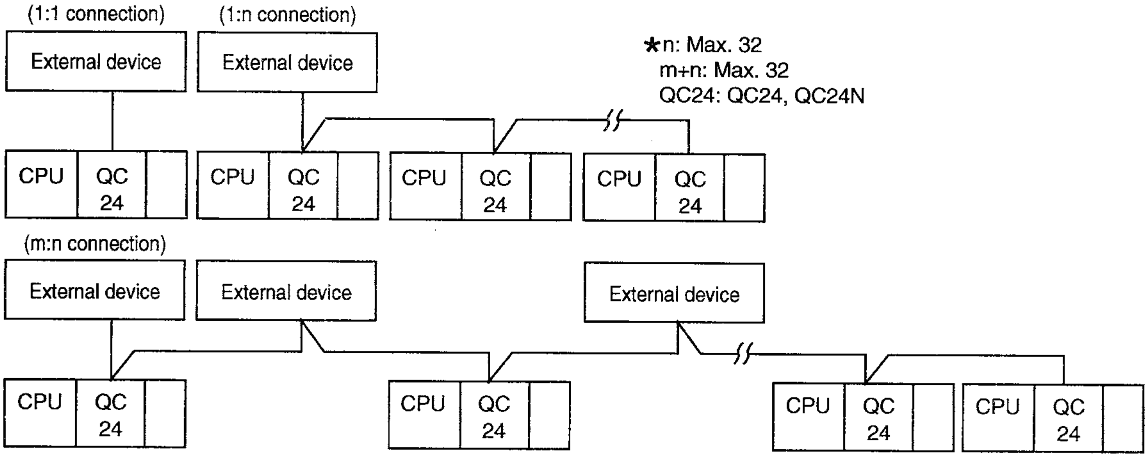
3 Various data communication systems can be built.

The QC24(N) has a function that operates its two interfaces independently and a function that links the operation of its two interfaces.

(a) Independent operation (Two QC24(N) interfaces operate independently)

① External functions and QC24(N) are connected in a 1:1, 1:n, or m:n configuration for each QC24(N) interface.

- RS-232C and RS-422 interfaces .... 1:1 connection
- RS-422/485 interface .... 1:1, 1:n, or m:n connection



② Sets the data communications function (dedicated protocol, non procedure protocol, bidirectional protocol) and transmission parameters for each QC24(N) interface.

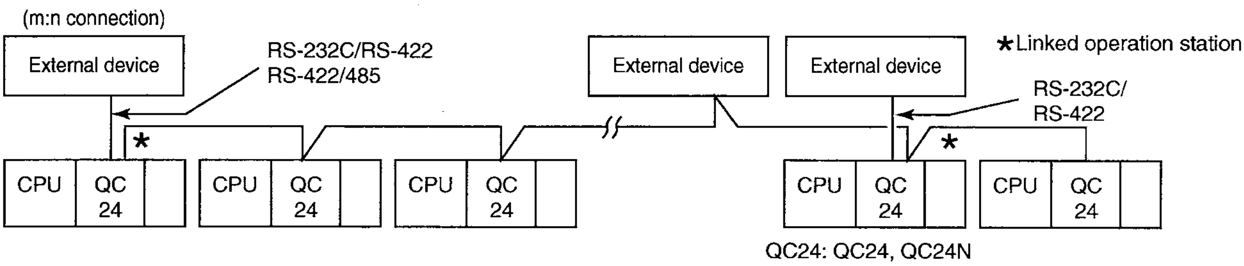
③ Data communications matched to the communications objective performed between bidirectionally connected external devices and PLC CPU.

(b) Linked operation (Two QC24(N) interfaces are linked and operated)

① External devices and the QC24(N) are connected to the two QC24(N) interfaces using a 1: n or m:n configuration.

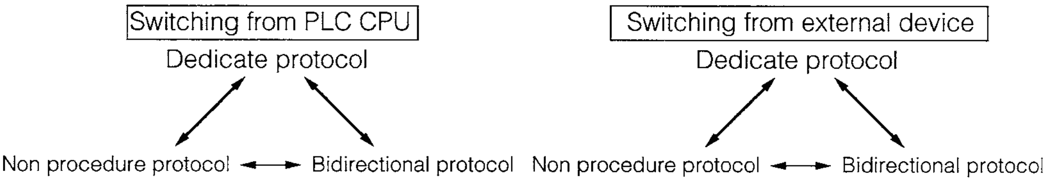
② Sets the same data communications function (dedicated protocol, non procedure protocol) and same transmission parameters for the two QC24(N) interfaces.

③ The same data communications function can transfer data between bidirectionally connected external devices and PLC CPU. (Detailed description Section 4.3.1 *2)



4 Data communications function and transmission parameters can be changed.

(a) Data communications can be continued by changing (mode switching) the data communications function set at each interface.



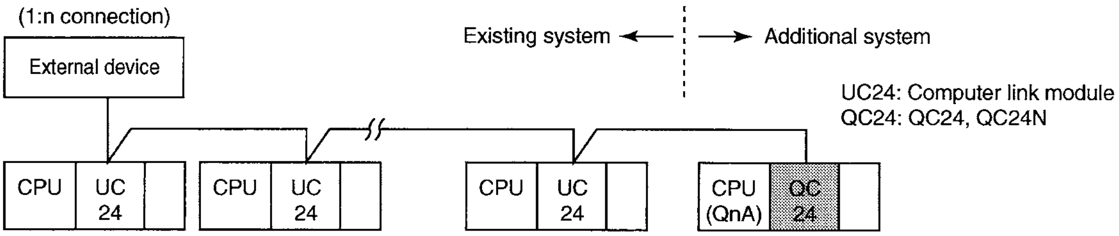
(b) The transmission parameters (transmission rate, etc.) of the objective interface can also be changed during mode switching. (Detailed description Chapter 18)

5 Incorporation into an existing system is possible.

(a) When external devices and computer link modules are multidrop connected in a 1: n or m:n configuration through an RS-422/485 interface, the QC24(N) can be incorporated into a multidrop link.

(b) When the QC24(N) was incorporated into an existing system, external devices can access the PLC using dedicated protocol ASCII mode frames. (See Section 1.2.1.)

(Detailed description Section 5.3)



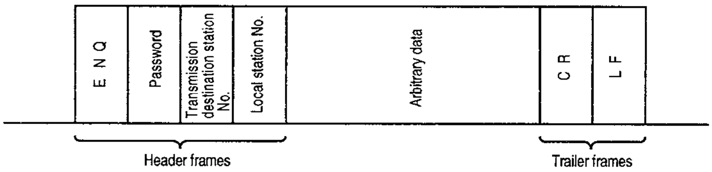
6 Data can be transferred in a message format matched to the specifications of the external device

(a) By registering the data list (user frame) of messages that can be transferred by external devices beforehand, the next data communications can be carried out by registered frame.

- Dedicated protocol .... Data transmission from PLC CPU to external devices by on-demand function.
- Non procedure protocol .... Data communication between PLC CPU and external devices

(Detailed description Chapter 7, Chapter 11)

* For instance, multiple header frames and trailer frames (both are called user frames) with the following meaning can be registered to the QC24(N) in advance.
By designating the preregistered user frame number and arbitrary data when transmitting data to an external device, the data can be transmitted in the order shown below.
When receiving data from an external device, by setting the user frame number registered when the QC24(N) was started for receiving use in advance, an arbitrary data field can be read to the PLC CPU whenever a message with the registered contents is received.



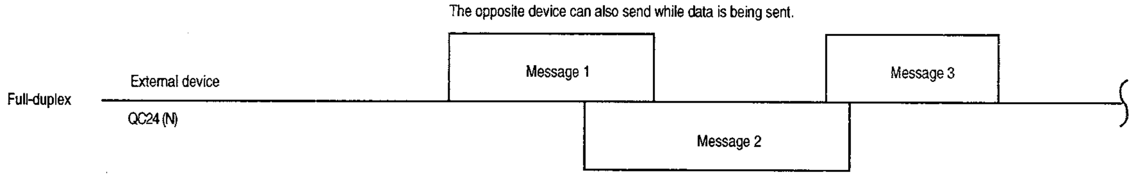
The QC24(N) sends data by adding the header frames and trailer frames to arbitrary data.
During data reception, the QC24(N) stores the arbitrary data field to buffer memory as receive data.

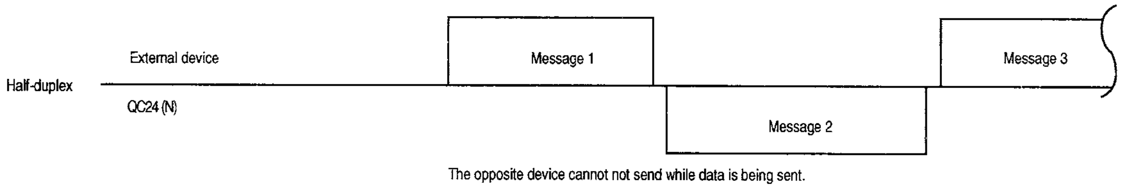
7 Half-duplex communications is possible.

(a) The QC24(N) can transfer data with external devices in the full-duplex and half-duplex modes. (See Section 3.1.)

(b) To transmit data to an external device for half-duplex communications, the QC24(N) RS-232C interface can be switched to the half-duplex mode.

(Detailed description Section 14.5)





8 Transmission control matched to the external device is possible.

(a) QC24(N) data transmission and reception to and from external devices can be controlled using control signal ON/OFF or by sending and receiving control codes.

(b) The following transmission controls are possible for each QC24(N) interface. Transmission control matched to the specifications of the external device can be set for each interface. (Detailed description Section 14.3)

Interface	DTR/DSR signal control	RS/CS signal control	CD signal control	DC code control
RS-232C interface	○	○	○	○
RS-422 interface	○	×	×	○
RS-422/485 interface	×	×	×	○

○: Yes, ×: No (DTR/DSR signal control and DC code control are selective.)

① DTR/DSR signal control

- This control uses the DTR (ER) and DSR (DR) signals to notify the sending device whether or not receiving device is ready to receive data.
- The user controls data communications by the QC24(N) by setting [Execute Control].

② RS/CS signal control

- This control uses the RS (RTS) and CS (CTS) signals to notify the sending device whether or not the receiving device is ready to receive data. It is controlled by the QC24(N).

③ CD signal control

- This control uses the CD signal to detect if an external device is ready to send and receive. The QC24(N) controls data transmission and reception.
- The user implements this control by setting [Check CD terminal].
- When [Do Not Check CD Terminal] was set, data is sent and received without regard to the status of the CD signal.

④ DC code control

- This controls notifies the sending device whether or not the receiving device is ready to receive data by sending and receiving DC1 and DC3 code data.
  It also posts the valid range of the send data to the opposite device by enclosing the user data in DC2 and DC4 code data.
- The user controls data communication by the QC24(N) by setting [Enable] for the relevant control.

9 **Data communications parameters and user frames can be registered.**

The following parameters for data communication with external devices and the user frames described in item 6 can be registered to the QC24(N) EEPROM and buffer memory.

(Detailed description Chapter 15, Chapter 16)

(a) Values (including parameters changed by the user) set to QC24(N) buffer memory special applications area

The values set to the special applications area can be registered to the QC24(N) EEPROM and used as the default values when the QC24(N) is started.
After registration, that part of the sequence program at which the default value was changed is not longer necessary.

(b) User frame user

Up to 200 registered frames can be registered to the QC24(N) EEPROM and up to 31 registered frames can be registered to the QC24(N) buffer memory. Data containing user frames can be transferred by designating the registration numbers before data communication.
When sending to an external device, designation of the same data list as the user frames can be omitted.
When receiving data from an external device, the QC24(N) processes only those messages containing the user-designated user frames.
Therefore, checking of the received data can be reduced.

10 **Response messages are sent even when the QnACPU stops.**

When transferring data using dedicated protocol, the QC24(N) sends a response message to the external device even if the access station (including the local station) stops and cannot be accessed.

11 High-speed communication

The data communication between QC24N and the external device can be executed in a high-speed. (Detailed description Chapter 4)

	Transmission speed (BPS) setting range	Remarks
QC 24	300 to 19200	—
QC24N	300 to 115200	The sum of CH1 and CH2 can be selected within 115200BPS. *1

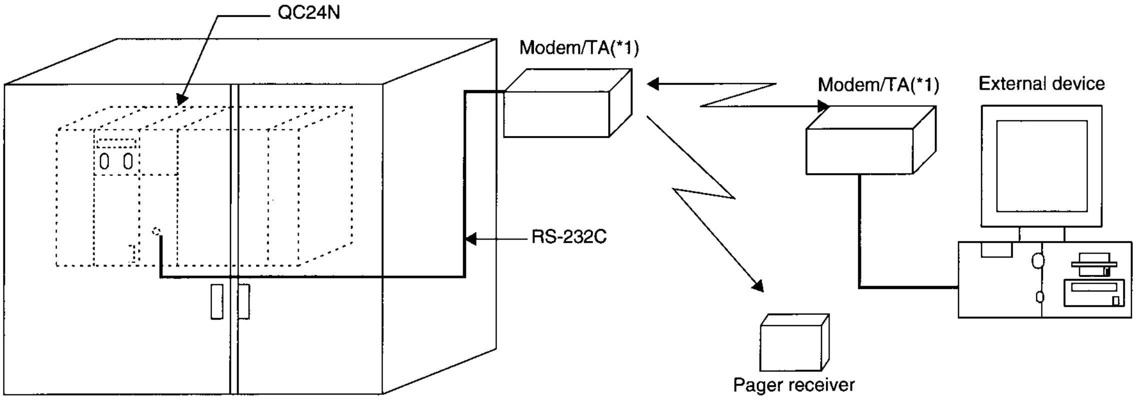
*1 For A1SJ71QC24N1(-R2), the sum of CH1 and CH2 can be selected within 230400BPS.

12 Data communication using a public line with the modem function

(a) Using the public line/internal line/digital line (ISDN), data communication between the PLC CPU and external device from remote area via QC24N RS-232C interface by full-duplex communication.

(Communication from dedicated protocol, non-procedure protocol, and bidirectional protocol)

(b) Messages can be sent to notify the PLC system maintenance information by pager receiver (pager) (Detailed description Chapter 21)



*1 TA: terminal adapter

POINT

Above “High-speed communication” and “Data communication with the modem function” can be performed with the following QC24N only.

	The manufactured date of the module to use the function	
	High-speed communication (see Section 4.3.2)	Data communication with the modem function (see Chapter 21)
AJ71QC24N	(All usable)	The products with 9804 □ or later printed on the DATE column on rated plate.
AJ71QC24N-R2		
AJ71QC24N-R4		
A1SJ71QC24N		(All usable)
A1SJ71QC24N-R2		
A1SJ71QC24N1		
A1SJ71QC24N1-R2		

* Read from Section 4.2 to check the manufactured date and software of the module.

1.2 Overview and Features of Data Communications Functions

The QC24(N) has three data communications functions for transferring data between external devices and PLC CPU. These functions are dedicated protocols, non procedure protocol, and bidirectional protocol.

The following outlines these data communications functions and describes their features.

1.2.1 Overview and features of dedicated protocols

1 **General Description**

Dedicated protocols QC24(N) communications procedures. External devices can read and write PLC CPU device data and sequence program files by sending command messages to the QC24(N). The following message formats and frames can be send and received between external devices and the QC24(N).

Data communications can be carried out in the message format matched to the data communications objective and external device specifications.

(Mode No.)

Dedicated protocols — ASCII mode (format 1 to 4) *1 — QnA frame .... 1 to 4
— QnA extension frame...... 1 to 4
— A compatible frame .... 1 to 4
— QnA simplified frame ...... 1 to 4
— Binary mode (format 5) — QnA extension frame......... 5

*1 Section 5.2 describes each mode and frame.

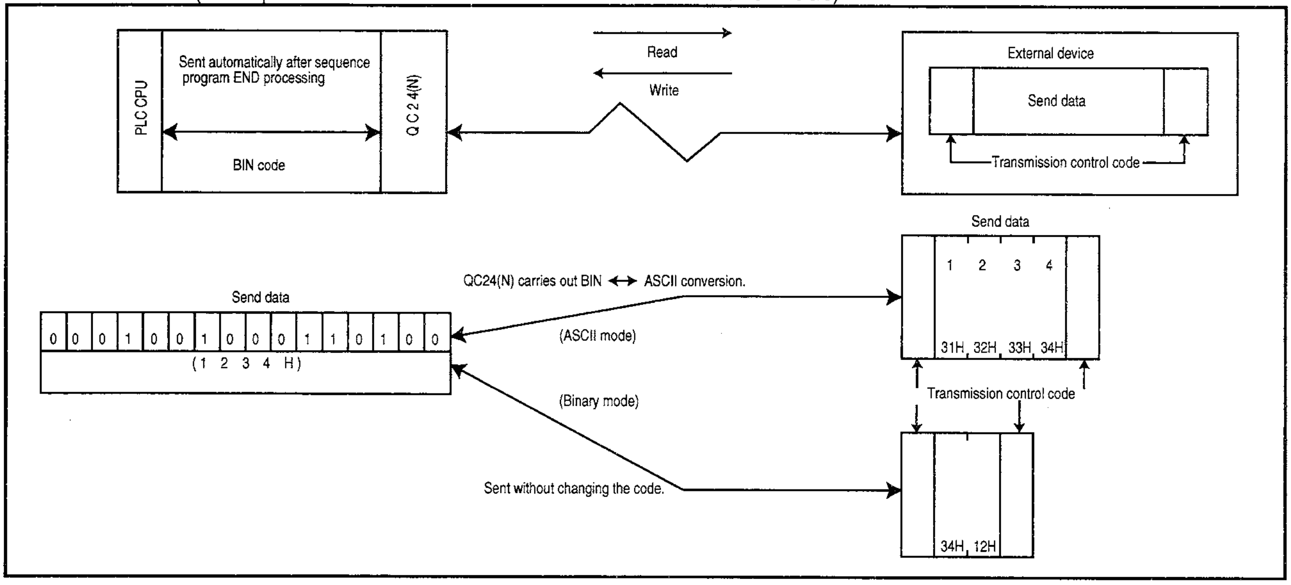
(a) Data communications in ASCII mode
  ① Transfers all ASCII code data.
  ② The QC24(N) converts the send and receive data from BIN to ASCII code as shown below.
  ③ When an external device sends a message in the set format, the QC24(N) judges the type of frame received and processes it accordingly.

(Detailed description Chapter 5, Chapter 6, Chapter 8)

(b) Data communication in binary mode
  ① Transfers all binary code data.
  ② Since the amount of message data is about one-half that of an ASCII mode QnA extension frame, the data transmission time is also cut in half.

(Detailed description Chapter 6)

(Example of send data in each data communications mode)

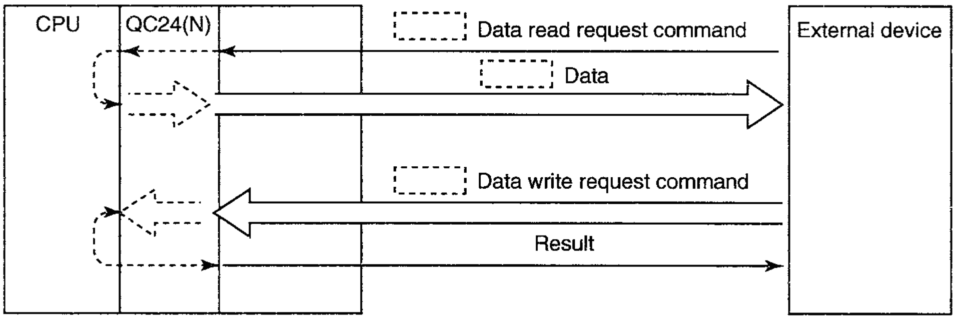


2 Features

(a) Communication on-demand from external device

① The external device issues a data read or write request.

② The external device sends a command message to the QC24(N) and reads/writes data/sequence program, etc. to/from the PLC CPU and various special function modules.



③ A sequence program for data communications is unnecessary, except when external devices and PLC CPU transfer data through the QC24(N) buffer memory.

④ When an external device sends a command message, the following operations are performed:

ⓐ PLC CPU device and special function module buffer memory read and write

- The external device monitors operation of the PLC CPU and performs data decoding, production management, etc.
- Production directives are given by writing data.

ⓑ Program storage and modification

- The sequence program, parameters, and other file data stored in the PLC CPU can be read to an external device and stored. (Uploading to external device)
- File data stored in an external device can be written to the PLC CPU and the execution program and other data can be modified (replaced), as required. (Downloading from external device)

ⓒ PLC CPU file control

- Files stored in the QnACPU can be read/written, created/deleted, and checked and the file area can be rearranged.

ⓓ PLC CPU remote control

- The PLC CPU can be remotely controlled from an external device. (Remote RUN/STOP/PAUSE/latch clear/reset)

ⓔ PLC CPU input signal control

- The input signals (input signals allocated to the QC24(N)) of the PLC CPU installed in the QC24(N) can be turned on and off.
- PLC CPU simultaneous starting, emergency stop, and data transmission from PLC CPU to external device can be controlled.
- These functions are called “global functions”.

(b) Transmission on-demand from PLC CPU

① The PLC CPU issues a data transmission request.

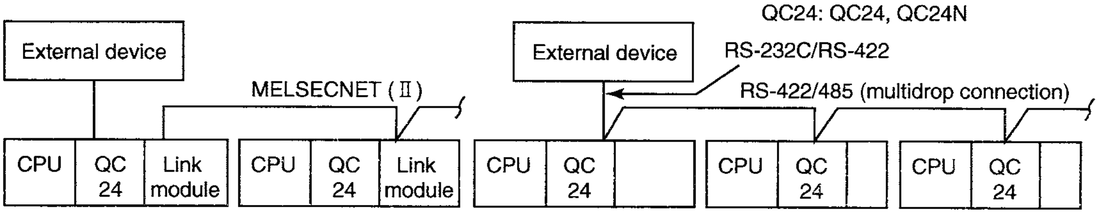
② When emergency data must be sent from PLC CPU to an external device, the PLC CPU issues a transmit request and the QC24(N) sends the designated data to the external device.

③ This function is called the “on-demand function”. It can be used when the QC24(N) and external device are connected in a 1:1 configuration.

④ A sequence program for sending data to external devices is necessary.

(c) Access to another station's PLC CPU from an external device

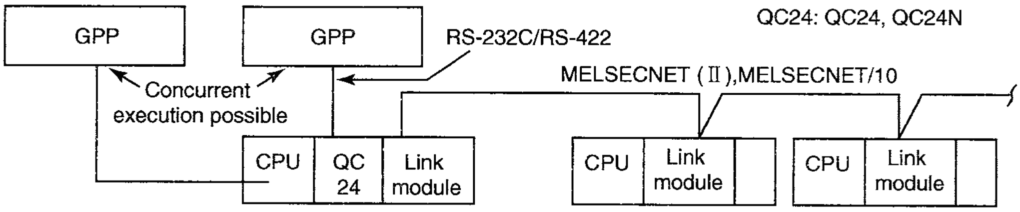
① An external device can access another station's PLC CPU as described in (a) ④ above through a QC24(N) connected in a multidrop configuration using a data link system (MELSECNET (II), MELSECNET/B), network system (MELSECNET/10), or an RS-422/485 interface.



(d) Access to QnACPU from GPP function

① The QC24(N) CH1 RS-232C/RS-422 interface is set to the binary mode and the QnACPU compatible GPP function peripheral device is connected.

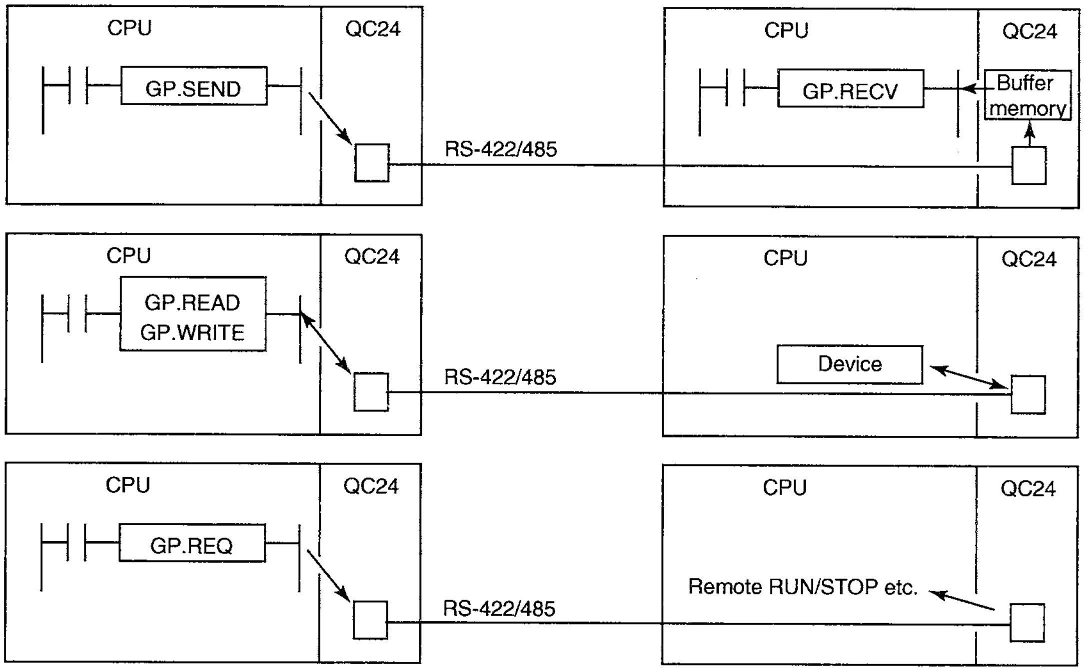
② The GPP function can access the PLC CPU installed in the QC24(N) and the PLC CPU of another station of a data link system or network system.
(Equivalent to connecting a QnACPU compatible GPP function peripheral device to the PLC CPU.)



* In the figure above, each GPP function can monitor and test the same, or different, station.

(e) Access to another station from the PLC CPU through the QC24(N)

① The QnACPU of another station connected in a multidrop configuration can be accessed through the QC24(N) by sequence program link instruction (SEND/RECV, READ/WRITE, REQ).



QC24: QC24, QC24N

POINTS

1. "Multiple block batch read and write" used for communication via the QnA/QnA extension frame and "communication via the QnA simplified frame" are available on all of the following QC24Ns (*1):

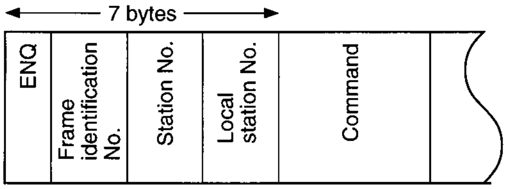
   AJ71QC24N AJ71QC24N-R2 AJ71QC24N-R4
   A1SJ71QC24N A1SJ71QC24N-R2 A1SJ71QC24N1 A1SJ71QC24N1-R2

   The QnACPUs that can perform "multiple block batch read and write" are shown in Section 1.4.

   *1 Functional overview of the above QC24N models

   (1) Multiple block batch read/write (see Section 6.2.10)
   - Data read and write can be performed via communication between using the QnA frame or QnA extension frame of the dedicated protocol.
   - Batch read and batch write of data may be performed by treating n points of QnACPU word device or bit device (one point is equivalent to 16 bits) as one block, or by designating multiple blocks randomly for external devices.

   (2) Communication via the QnA simplified frame (see Chapter 8)
   - The QnA simplified frame is used for communicating data in the ASCII mode of the dedicated protocol (format 1 to format 4), in which the message format is simplified.
   - Communication via this frame may be used for batch read/write of device, device monitoring, etc.
   - Since the amount of transmission data is decreased, message processing on the external device side is made easier, which reduces the transfer time.



(Example) The head part of transmission data when data read is requested (for format 1)

2. Communication programs in the personal computers to be connected to Ethernet or computer link can be simplified by using the following communication support software tools manufactured by Mitsubishi Electric, which support communication between MELSEC-A or QnA series PLC and personal computers.

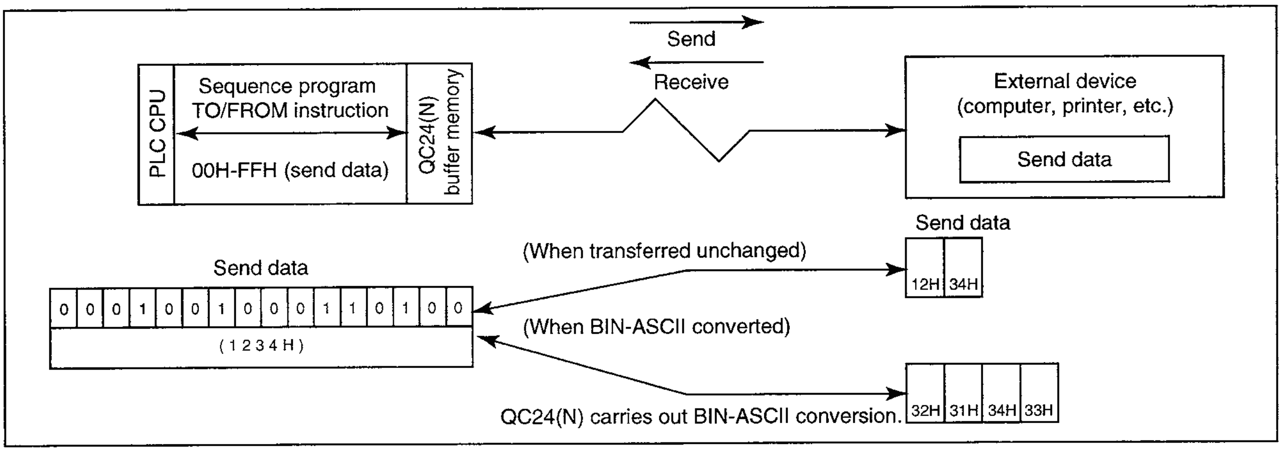
   - SWnD5F-ACT-E type basic communication support tool

   The overview and application examples of basic communication support tools are shown in Appendix 7. See when necessary.

1.2.2 Overview and features of non procedure protocol

1 Overview of functions

Arbitrary data can be transferred between an external device and the PLC CPU using the user communication procedure. The user decides the format of the messages transferred by the external devices and the QC24(N).



2 Features

(a) Transmission from PLC CPU

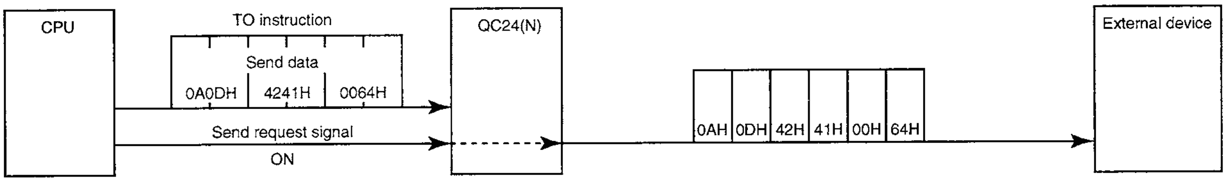
① Data can be sent to an external device by writing the send data to the QC24(N) buffer memory and turning on the send request signal using the TO instruction from the sequence program.

② The format of the data sent by the QC24(N) can be selected from among two types to match the specifications of the external device.

- Designated data sent unchanged. (Not converted)
- Designated data BIN-ASCII converted. (Converted by QC24(N))

(Detailed description Chapter 9 to Chapter 11)

(Example of transmission of designated data unchanged)



(b) Reception from external device

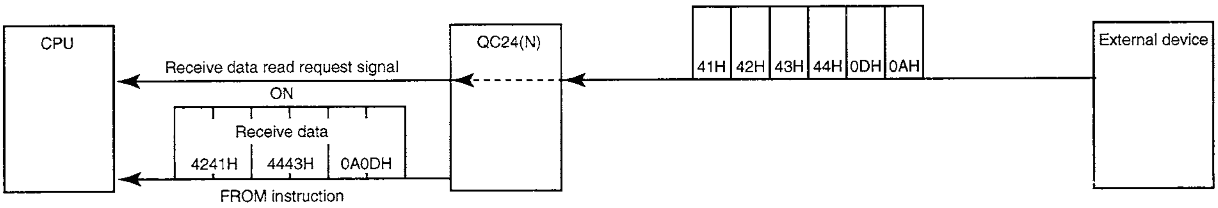
① The data received from an external device can be read from the QC24(N) buffer memory to the PLC CPU using the FROM instruction.

② The format of the data read by the PLC CPU can be selected from among two types to match the specifications of the external device.

- Receive data read unchanged. (Not converted)
- Received data BIN-ASCII converted, then read. (Converted by QC24(N))

(Detailed description Chapter 9 to Chapter 11)

(Example of reading of receive data unchanged)



③ By presetting the read conditions, the receive data can be read to the PLC CPU by the following methods. (Detailed description Section 9.3)

ⓐ When variable length data received

- The user can set the receive completed code to the QC24(N) buffer memory.
- When the QC24(N) receives the receive completed code data from the external device, it can read the data received up to that point to the PLC CPU.

ⓑ When fixed length data received

- The user can set the receive completed code to the QC24(N) buffer memory.
- When the QC24(N) received the number of receive completed data from the external device, it can read the receive data up to that point to the PLC CPU.

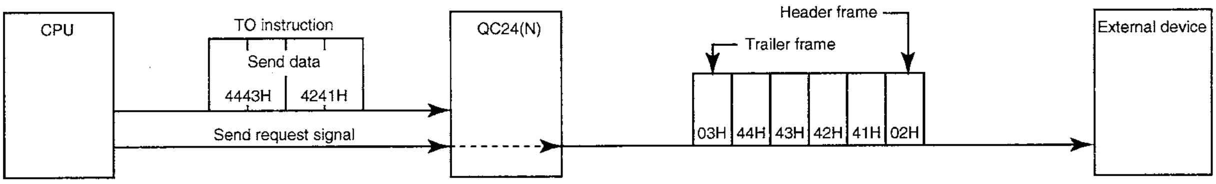
(c) Data communications in the message format matched to the specifications of the external device

By registering the messages transmitted by the external device and the header frame and trailer frame of the messages that can be received by the external device to the QC24(N) in advance as user frames, data can be transferred by registered frame.

(Detailed description Chapter 11)

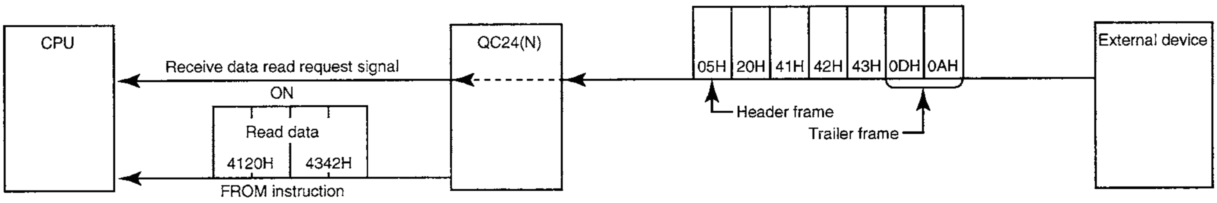
① When sending from the PLC CPU

The QC24(N) adds header frame and trailer frame data to the send data designated by the PLC CPU and sends the data.



② When PLC CPU receives data

When the data from the header frame to the trailer frame was received, it can be read to the PLC CPU.



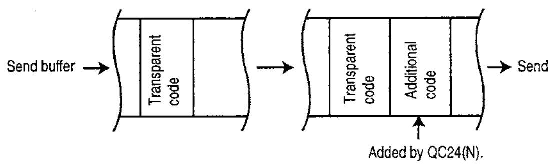
* The user frames shown above can be registered to the QC24(N) buffer memory (maximum 31 frames) and EEPROM (maximum 200 frame) from the PLC CPU or an external device in advance.
Up to 80 bytes can be registered in one user frame. The sum check code and QC24(N) set station number can be designated for addition to transmit message or for receive message check. (The QC24(N) carries out the addition/check.)
Only one or more user frames can be sent to an external device on command from the PLC CPU.

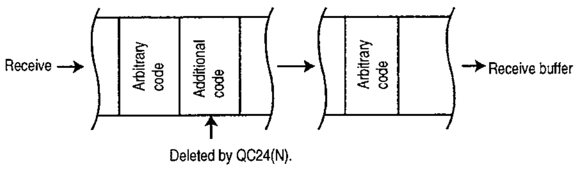
(d) Transparent code setting

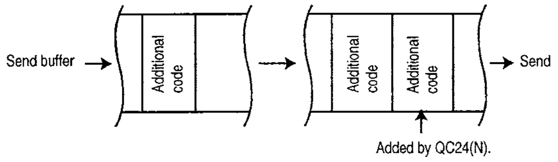
① The following codes can be preset to the QC24(N) so that one byte of data for transmission control of the external device can be handled as user data when data is transferred in binary code.

- Transparent code .... One byte data for transmission control
- Additional code .... One byte data that is sent by adding it in front of the transparent code and additional code during transmission.
  Data that is deleted during reception (The one byte of data immediately following this data is received.)

② When the QC24(N) detects sent transparent code data during data transmission, it sends the data by adding send additional code data before the transparent code data.
When the QC24(N) detects send additional code data, it adds data of the same code before the additional code data.
When the QC24(N) detects receive additional code data during reception, it deletes the additional code data and stores the data (1 byte) immediately following it to the receive area. (Detailed description Section 9.2, Section 14.10)





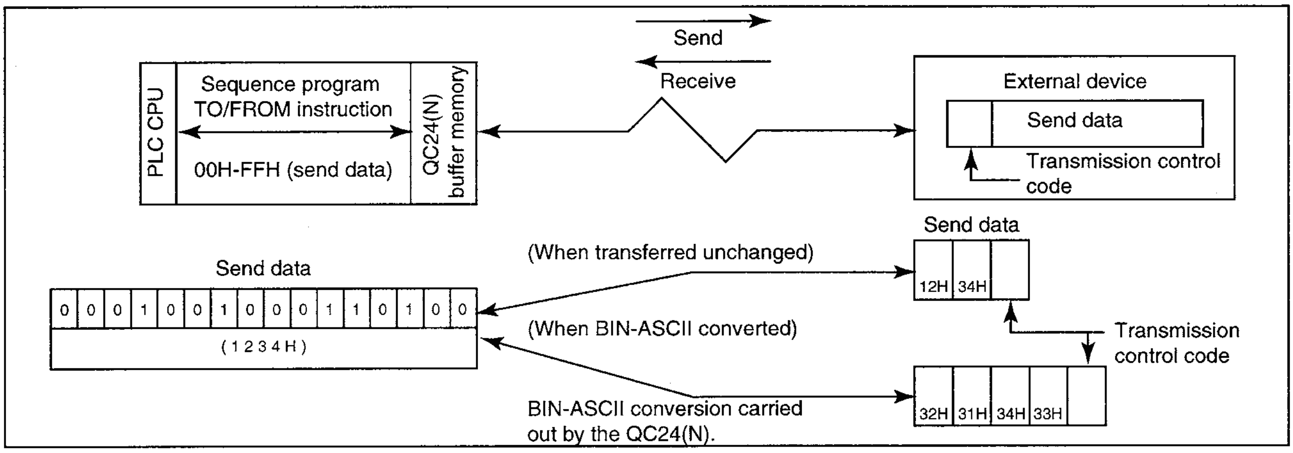


1.2.3 Overview and features of bidirectional protocol

1 General description of functions

When external devices and the QC24(N) are connected in a 1:1 configuration, arbitrary data can be transferred between the external devices and the QC24(N) using the QC24(N) communication procedure.

The user decides the format of the user data part of the messages transferred between external devices and the QC24(N).



2 Features

(a) Transmission from PLC CPU

① Data can be sent to an external device by writing the send data to the QC24(N) buffer memory and turning on the send request using the TO instruction from the sequence program.

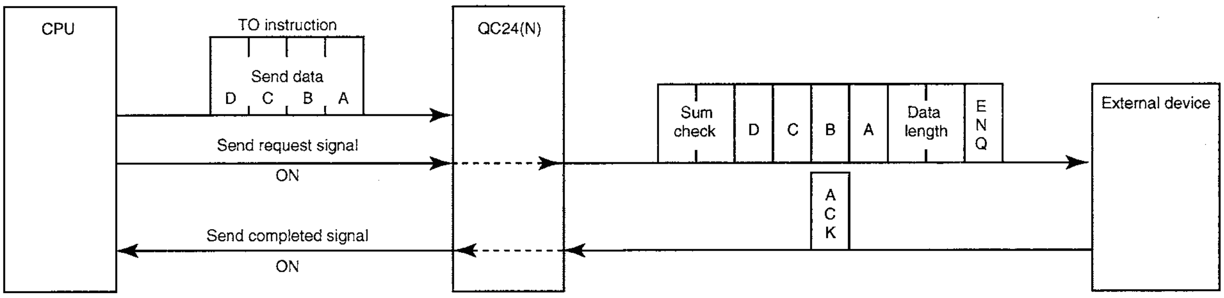
② When a transmission control code and other data is added to the send data and a response to transmission is received from the external device, transmission is completed.

③ The format of the data sent by the QC24(N) can be selected from two different formats to match the specifications of the external device.

- Send designated data unchanged. (Not converted)
- BIN-ASCII convert designated data and sent the converted data. (Converted by QC24(N))

(Detailed description Chapter 12, Chapter 13)

(Example of transmission of designated data unchanged)



(b) Reception from external device

① Data received from an external device can be read from the QC24(N) buffer memory to the PLC CPU using the FROM instruction.

② The QC24(N) removes the control codes and other data from the data received from the external device.

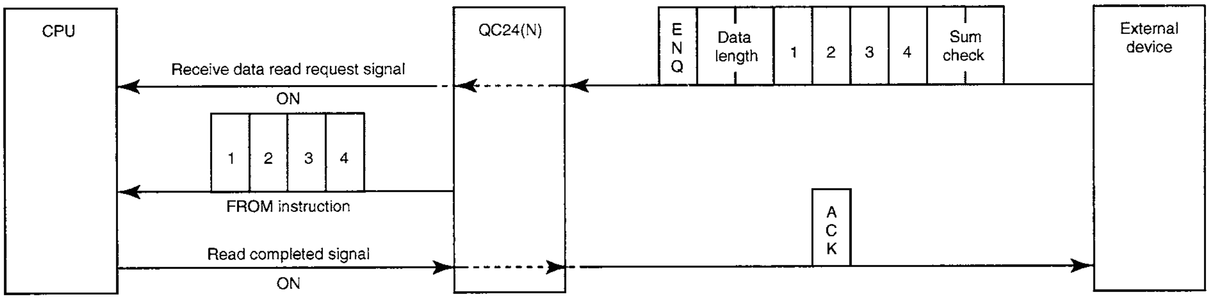
③ When the PLC CPU reads the data with the control codes and other data removed, the QC24(N) sends a response message to the external device.

④ The format of the data read by the PLC CPU can be selected from two different formats to match the specifications of the external device.

- Read receive data unchanged. (Not converted)
- ASCII-BIN convert receive data and read the converted data. (Converted by QC24(N))

(Detailed description Chapter 12, Chapter 13)

(Example of reading the receive data unchanged)



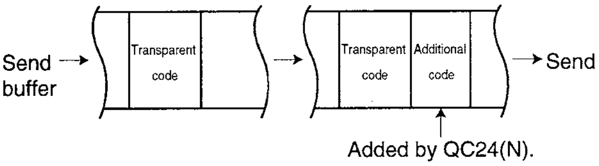
(c) Transparent code setting

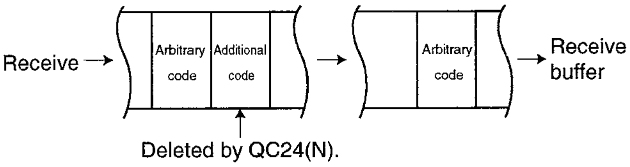
① When binary code data is received, the following codes can be preset so that the one byte data for transmission control of the external device is handled as user data.

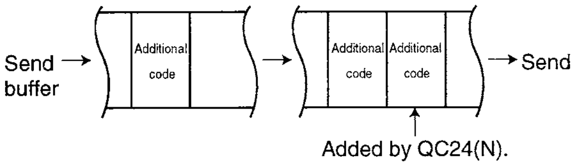
- Transparent code ..... One byte data for transmission control
- Additional code .... One byte data sent by adding it immediately before the transparent code and additional code during transmission.

Data that is deleted during reception. (The one byte of data immediately following this code is received.)

② When the QC24(N) detects send transparent code data during data transmission, it adds the send additional code data immediately before the transparent code data and sends the data.
When the QC24(N) detects send additional code data, it adds data of the same code immediately before the additional code data and sends the data.
When the QC24(N) detects receive additional code data while receiving data, it deletes the additional code data and stores the data (1 byte) immediately following the additional code data to the receive area.
(Detailed description Section 12.2, Section 14.10)







1.3 Overview Product in the Same Package of Objective Serial Communication Modules

The following lists the types of objective serial communication modules described in this manual and outlines the modules and describes product in the same package.

Model name	Overview	Included in package
AJ71QC24 AJ71QC24N	(1) QnACPU compatible serial communication module. (2) One RS-232C interface channel and one RS-422/485 interface channel are installed. CH1: RS-232C (D-sub 25 pins) CH2: RS-422/485 (Two-piece terminal block)	AJ71QC24/A1SJ71QC24N main module 1 unit Terminal resistor 330 ohm 1/4 W (orange orange brown ⬚) 2 units Terminal resistor 110 ohm 1/2 W (brown brown brown ⬚) 2 units
AJ71QC24-R2 AJ71QC24N-R2	(1) QnACPU compatible serial communication module. (2) Two RS-232C interface channels are installed. CH1: RS-232C (D-sub 25 pins) CH2: RS-232C (D-sub 25 pins)	AJ71QC24-R2/AJ71QC24N-R2 main module 1 unit
AJ71QC24-R4 AJ71QC24N-R4	(1) QnACPU compatible serial communication module. (2) One RS-422 interface channel and one RS-422/485 interface channel are installed. CH1: RS-422 (D-sub 25 pins) CH2: RS-422/485 (Two-piece terminal block)	AJ71QC24-R4/AJ71QC24N-R4 main module 1 unit Terminal resistor 330 ohm 1/4 W (orange orange brown ⬚) 2 units Terminal resistor 110 ohm 1/2 W (brown brown brown ⬚) 2 units
A1SJ71QC24 A1SJ71QC24N A1SJ71QC24N1	(1) QnACPU compatible serial communication module. (2) One RS-232C interface channel and one RS-422/485 interface channel are installed. CH1: RS-232C (D-sub 9 pins) CH2: RS-422/485 (Two-piece terminal block)	A1SJ71QC24/A1SJ71QC24N/A1SJ71QC24N1 main module 1 unit Terminal resistor 330 ohm 1/4 W (orange orange brown ⬚) 2 units Terminal resistor 110 ohm 1/2 W (brown brown brown ⬚) 2 units
A1SJ71QC24-R2 A1SJ71QC24N-R2 A1SJ71QC24N1-R2	(1) QnACPU compatible serial communication module. (2) Two RS-232C interface channel are installed. CH1: RS-232C (D-sub 9 pins) CH2: RS-232C (D-sub 9 pins)	A1SJ71QC24-R2/A1SJ71QC24N-R2/A1SJ71QC24N1-R2 main module 1 unit

Notes

The connection between the external equipment and the QC24(N) can be done using the following combinations.

(1) The connection combinations with each interface of the QC24(N) are as follows.
  - * RS-232C .... External equipment and QC24(N) are connected 1:1.
  - * RS-422 .... External equipment and QC24(N) are connected 1:1.
  - * RS-422/485 .... External equipment and QC24(N) are connected 1:1, 1:n, and m:n.

(2) When 2 QC24(N) interfaces are used a connection of external equipment and QC24(N) of 2: 1, 2: n, and m:n can be used.

1.4 Comparison of Specifications with Computer Link Module AJ71UC24

The following shows the differences between specifications of the QC24(N) and the AJ71UC24.

When using the external device program of a computer link module for data communications using dedicated protocols to communicate with the QC24(N), see Section 5.4.3 and Appendix 1.

(*1)

Functions				QC24N	QC24	AJ71UC24
Communications using dedicated protocols	Communication frame	Communications using ASCII data	QnA frame	Enable		Disable
			QnA extension frame			
			A compatible frame	Enable		
			QnA simplified frame	Enable	Disable	Disable
		Communications using binary data	QnA extension frame	Enable		Disable
	Communication by read and write with the device memory	Other than those listed below		Enable		
		Multiple block batch read, batch write		Enable (*2)	Disable	Disable
		Read/write device memory	QnACPU	Enable		Enable(AnACPU range only)
			Other than QnACPU	Enable (AnUCPU range only)		Enable
		Access to other stations via data link or network		Enable (access range extension)		Enable
	Transmission from PLC CPU (on-demand)			Enable (user entry frames can be used)		Enable
	Access to other stations using QnACPU link-dedicated instruction			Possible through QC24(N)		Impossible through UC24
	Connection of QnACPU compatible GPP function peripheral device (SWn□-GPPQ)			Connectable through QC24(N)		Not connectable through UC24
	Connection of peripheral device for GPP function software for Windows (SWID5C/F-GPPW-E or later)			Enable		
	Communication between an external device and the PLC CPU through m:n connection			Enable		
Communications using non procedure protocol	Transmission and reception by an arbitrary format			Enable		
	Transmission and reception by the user entry frame			Enable		Enable (send only)
	Transmission and reception by ASCII-BIN conversion			Enable (conversion by QC24(N))		Disable
	Transmission and reception by the transparent code designation			Enable		Disable
Communications using bidirectional protocol	Transmission and reception by an arbitrary format			Enable		
	Transmission and reception by ASCII-BIN conversion			Enable (conversion by QC24(N))		Disable
	Transmission and reception by the transparent code designation			Enable		Disable
Communication by public line using the modem function				Enable (*3)	Disable	Disable
Transmission control	DC code control			Enable		
	DTR/DSR signal control					
Half-duplex communications control				Enable		
Mode switching				Enable (forced switching only)		Enable
Independent operation of two I/F	Setting of same protocol			Enable		Disable
	Setting of different protocol			Enable		
Linked operation of two I/F (same protocol)				Enable		Enable (with restrictions)
EEPROM registration of buffer memory initial setting value				Enable		Disable
EEPROM registration of user entry frame				Enable		Disable
Connection to external device	1:1, 1:n			Enable		
	m:n			Enable (with restrictions on station No.)		Enable
Transfer of I/O signal by multidrop link function				Disable		Enable
Installable PLC				QnACPU, MELSECNET/10 remote station only		QnACPU, previous CPU
Data transmission speed (BPS)				115200 maximum	19200 maximum	19200 maximum

*1 The functions that are "usable" for both the QC24N and QC24 are used in the same way.

However, the time required for access processing to the PLC CPU and message transmission processing to external devices are shortened on QC24N due to the increased speed in internal processing.

*2 The PLC CPU that can be accessed are the host with QC24N installed and remote stations via MELSECNET/10 as shown below.

Function	**PLC CPU**		
	QnA	**Q2AS (H)**	**Q4AR**
Multiple block batch read/batch write	(Products 9707B or later) *		(All possible)

Manufactured date Function version (Mentioned only B or later)

* The products with 9707 B or later printed on the package display and the date column on rated plate of the module are the products with this function added.

*3 Using the QC24N RS-232C interface (1 channel only), the exchange via public line, etc. is possible using the modem function.

	AJ71QC24N **AJ71QC24N-R2**	**A1SJ71QC24N** **A1SJ71QC24N-R2** **A1SJ71QC24N1** **A1SJ71QC24N1-R2**	**AJ71QC24N-R4**
Modem function	(Products 9804 ☐ or later) *	(All possible)	(Unusable)

Function version (Mentioned only B or later)

Manufactured date

* Modules equipped with the modem function have the indication of 9804 ☐ or later in the DATE column of the rated plate on the main module and on the shipment box.

1.5 Generics, Abbreviations, and Terminology Used in This Manual

1.5.1 Generics and abbreviations

Objective modules generics and abbreviations

The following table lists the serial communication modules and PLC CPU modules in this manual by generic and abbreviation. When the objective model name must be clarified, the module model name is given.

Abbreviation/generic	Description/objective module
Large-type QC24	AJ71QC24, AJ71QC24-R2, AJ71QC24-R4
Large-type QC24N	AJ71QC24N, AJ71QC24N-R2, AJ71QC24N-R4
Large-type QC24(N)	Large-type QC24, Large-type QC24N
Small-type QC24	A1SJ71QC24, A1SJ71QC24-R2
Small-type QC24N	A1SJ71QC24N, A1SJ71QC24N-R2
Small-type QC24(N)	Small-type QC24, Small-type QC24N
ACPU PLC CPU	Accessible PLC CPU module shown in Section 2.2 (Including PLC CPU with MELSECNET data link function) Entered in illustration as CPU.
An(N)CPU or An(N)	A1CPU, A1NCPU, A2CPU, A2CPU-S1, A2NCPU, A2NCPU-S1, A3CPU, A3NCPU among ACPUs
AnSCPU or AnS	A1SCPU, A1SJCPU, A1SHCPU, A1SJHCPU, A2SCPU, A2SHCPU among ACPUs
AnACPU	A2ACPU, A2ACPU-S1, A3ACPU, A2ACPUP21/R21, A2ACPUP21/R21-S1, A3ACPUP21/R21 of ACPU
AnUCPU	A2UCPU, A2UCPU-S1, A3UCPU, A4UCPU, A2ASCPU, A2ASCPU-S1 of ACPU
AnA/AnU/QnACPU	AnACPU, AnUCPU, QnACPU
AnU/QnACPU	AnUCPU, QnACPU
AJ71QC24 (-R2,R4)	AJ71QC24, AJ71QC24-R2, AJ71QC24-R4
AJ71QC24N (-R2,R4)	AJ71QC24N, AJ71QC24N-R2, AJ71QC24N-R4
AJ71QC24(N)	AJ71QC24, AJ71QC24N
AJ71QC24(N)-R2	AJ71QC24-R2, AJ71QC24N-R2
AJ71QC24(N)-R4	AJ71QC24-R4, AJ71QC24N-R4
A1SJ71QC24 (-R2)	A1SJ71QC24, A1SJ71QC24-R2
A1SJ71QC24N (-R2)	A1SJ71QC24N, A1SJ71QC24N-R2, A1SJ71QC24N1, A1SJ71QC24N1-R2
A1SJ71QC24(N)	A1SJ71QC24, A1SJ71QC24N, A1SJ71QC24N1
A1SJ71QC24(N)-R2	A1SJ71QC24-R2, A1SJ71QC24N-R2, A1SJ71QC24N1-R2
LP21/BR11	AJ71LP21, AJ71BR11, AJ71LR21, A1SJ71LP21, A1SJ71BR11
LP25/BR15	AJ72LP25, AJ72BR15
QC24	AJ71QC24, AJ71QC24-R2, AJ71QC24-R4, A1SJ71QC24, A1SJ71QC24-R2 (*1)
QC24N	AJ71QC24N, AJ71QC24N-R2, AJ71QC24N-R4, A1SJ71QC24N, A1SJ71QC24N-R2, A1SJ71QC24N1, A1SJ71QC24N1-R2 (*1)
QC24(N)	QC24, QC24N (*1)
QnACPU	Q2ACPU, Q2ACPU-S1, Q3ACPU, Q4ACPU, Q2ASCPU, Q2ASCPU-S1, Q2ASHCPU, Q2ASHCPU-S1 of ACPU
QLP21/QBR11	AJ71QLP21, AJ71QBR11
QLP25/QBR15	AJ72QLP25(G), AJ72QBR15, A1SJ72QLP25, A1SJ72QBR15

*1 Diagrams applicable for QC24 and QC24N denote that they are for both of the two types using the expression as below:

QC24 : QC24, QC24N

2 Other generics and abbreviations

This manual uses the following generics and abbreviations to describe the data communications functions, etc. of the QC24(N). When the objective of the description must be clearly shown, the name/module name is entered.

Abbreviation/generic	Description
External device	Computer, display, measuring instrument, ID module, bar code reader, controller, computer link module given below, other QC24(N), etc. that connect to the QC24(N) to implement data communications.
Computer	External device that can send/receive data using dedicated protocols and bidirectional protocol.
Computer link module C24, UC24	Modules with the model names given below. Abbreviated C24 or UC24 in illustrations. AJ71UC24, A1SJ71(U)C24-R2, A1SJ71(U)C24-PRF, A1SJ71(U)C24-R4, A1SCPU24, A2CCPUC24, A2CCPU24-PRF
Data communications functions	Dedicated protocols, non procedure protocol, bidirectional protocol
Data link systems	MELSECNET(II), MELSECNET/B data link system
Network system	MELSECNET/10 network system
Network/data link systems	Network system, data link system
I/F	Interface
RS-232C (interface)	RS-232C interface
RS-422 (interface)	RS-422 interface
RS-422/485 (interface)	RS-422 and RS-485 interfaces. When only RS-485 must be shown, it is entered as RS-485.

1.5.2 Definition and description of terminology

The following gives the meaning and describes the terms used in the QC24(N) associated manuals, including this manual.

Term	Description
ASCII mode	Mode that transfers data between an external device and QC24(N) by all ASCII code characters when using dedicated protocols. At the PLC, the QC24(N) carries out BIN-ASCII conversion of the send/receive data. See Chapters 5 to 8 for more information.
Dedicated protocols	QC24(N) communication procedure. One of the data communication functions for accessing the PLC CPU from an external device. Two data communication methods are available: data communications in ASCII mode and data communications in binary mode. See Chapters 5 to 8 for more information.
Bidirectional protocol	QC24(N) communications procedure. One of the data communications functions for transferring arbitrary data between an external device and the PLC CPU. See Chapters 12 and 13 for more information.
Independent operation	Operation of the QC24(N) when transferring data with external devices using the function set by mode switch without linking by the two QC24(N) interfaces.
Binary mode	Mode that transfers data between external device and QC24(N) by all binary code numeric data when data is transferred using the dedicated protocols. See Chapters 5 to 7 for more information.
Multidrop connection	Name of connection when multiple external devices and other QC24(N) are connected in a 1:n or m:n configuration using the RS-422/485 interface of the QC24(N). See Section 4.7.4 for more information.
Non procedure protocol	A data communications function for transferring arbitrary data between an external device and the PLC CPU using the user communication procedure. See Chapters 9 to 11 for more information.
Message transmission function (printer function)	Function that registers character data (message) to be sent to an external device (primarily a printer) to the QC24(N) beforehand and sends only multiple user frames by non procedure protocol. (Transmits by directive from the PLC CPU)
User frame	Fixed format part of messages transferred between an external device and the QC24(N) using the following functions. (Conforms to external device specifications.) It is used by registering the header and trailer data lists (transmission control code, QC24(N) station number, check sum, fixed data, etc.) in the message to the QC24(N). • Dedicated protocols on-demand function • Data communications using non procedure protocol See Chapter 7 and Chapter 11 for more information.
Linked operation	Operation of the QC24(N) when transferring data with external devices while linking them using the two QC24(N) when the external device and QC24(N) system configuration is 1:n or m:n and the external devices are connected by the two QC24(N) interfaces. The two interfaces can transfer data by the same data communication function (dedicated protocols (same format) or non procedure protocol) and same transmission specifications. (Bidirectional protocol linked operation is impossible.) See Section 4.3.1 *2 for more information.

Term	Description
A compatible frame	A QC24N message format for transferring data using the dedicated protocol ASCII mode (format 1 to 4). (This is the same message format as that used for the computer link module, and the device memory of the PLC CPU may be accessed.) The summary is described in Section 5.4.2. See Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function) for more information.
QnA frame	A QC24(N) message format for transferring data using the dedicated protocol ASCII mode (format 1 to 4). See Chapters 5 and 6 for more information.
QnA extension frame	A QC24(N) message frame for transferring data using the dedicated protocols. (Extends the accessible range from QnA frame.) See Chapters 5 and 6 for more information.
QnA (extension) frame	Generic of QnA frame and QnA extension frame.
QnA simplified frame	A QC24N message format for transferring data using the dedicated protocol ASCII mode (format 1 to 4). The message format in this frame is simplified in comparison with the QnA (extension) frame, and since the amount of transmission data is decreased, message processing on the external device side is made easier, which reduces message transfer time. Communication via this frame supports batch read/write and monitoring of a device. See Chapter 8 for more information.

2. SYSTEM CONFIGURATIONS AND AVAILABLE FUNCTIONS

The system configurations for data communications using the QC24(N) are available: external device and QC24(N) (PLC CPU side) 1:1, 1:n (n: max. 32) and m:n (total of m+n: max. 32).

This section describes the PLC system configuration, types of system configurations with external devices, and the QC24(N) data communications functions that can be used with each system configuration.

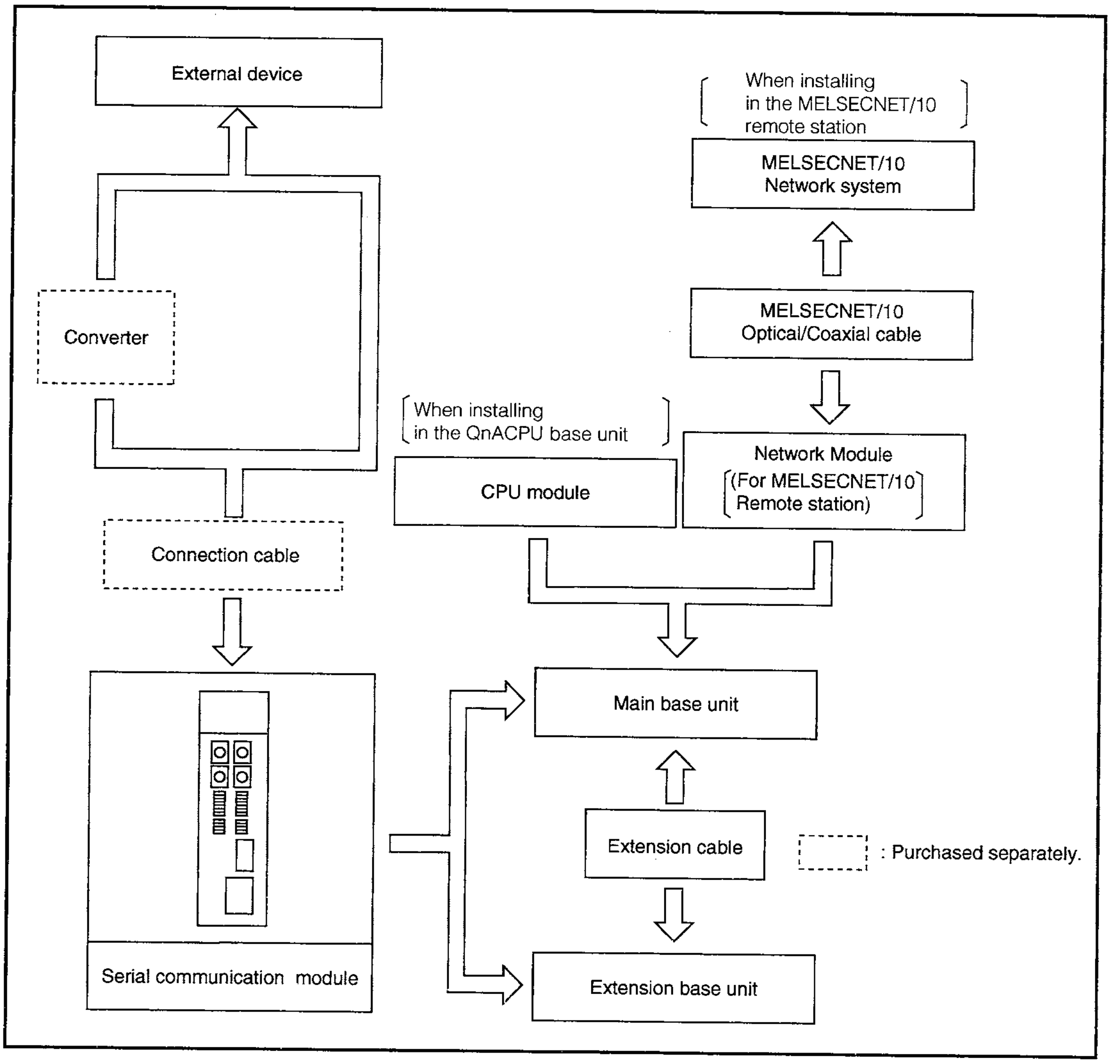
Build a QC24(N) and external devices data communications system by matching the QC24(N) and external device specifications.

POINT

See Chapter 21 for the system configuration in accordance with the external device side and cautionary items for system configuration using the QC24N modem function.

2.1 Overall Configurations

1 **When installed to QnACPU base unit**



2.2 Applicable Systems

The QC24(N) can be used in the systems described below.

1 Applicable CPU and network modules and Installable Number of Module

The table below shows the applicable CPU and network modules (for remote station) and the number of QC24(N) that can be connected.

Applicable Modules		Installable Number of Module	Notes
CPU modules	Q2A (S1), Q3A, Q4A, Q4AR, Q2AS (S1) Q2ASH (S1)	Unlimited	· Installable the QC24(N) by the combination of usable large-type/ small-type CPU modules and QC24(N) and within the number of CPU module/remote station I/O signals.
Network modules	AJ72QLP25 AJ72QBR15 A1SJ72QLP25 A1SJ72QBR15		

2 Applicable base unit

The QC24(N) can be inserted into any slot of a main base unit or extension base unit with these two exceptions:

(a) Do not insert the QC24 into an extension base unit without a power supply module (A52B, A55B, A58B type extension base unit).
The power supply capacity may be insufficient.
When inserting the QC24 into a main base unit, take into account the current capacity of the power supply module of the main base unit and the voltage drop of the extension cable. (See the CPU Module (see 1) User's Manual for more information.)

(b) The QC24(N) can be installed in a QnACPU PLC CPU station base unit and MELSECNET/10 remote station. It cannot be installed in stations other than QnACPU PLC CPU stations and in MELSECNET (II) and MELSECNET/B remote stations.

3 Accessible PLCs

The following describes the PLCs that can be accessed from external devices using the dedicated protocols.

① PLC CPU

The PLC CPUs that can be accessed from external devices include access through a data link system or network system.
External devices can access the PLC CPU device memory and special functions module buffer memory.

PLC CPU	A0J2	A0J2H	A1	A1N	A1S	A1SH	A1SJ
	A1SJH	A2 (S1)	A2N (S1)	A2A (S1)	A2U (S1)	A2S	A2SH
	A2AS (S1)	A2C	A2CJ	A52G	A3	A3N	A3A
	A3U	A3H	A3M	A4U			
	Q2A (S1)	Q3A	Q4A	Q4AR	Q2AS (S1)	Q2ASH (S1)	

② Remote station

The following lists the remote stations that can be accessed from external devices over a data link system or network system.

External devices can access the buffer memory of the special functions module of the remote stations that can be connected by the link modules with the model names shown below.

MELSECNET/10	AJ72QLP25 AJ72QBR15 A1SJ72QLP25 A1SJ72QBR15 AJ72LP25(G) AJ72BR15
MELSECNET (II)	AJ72P25 AJ72R25
MELSECNET/B	AJ72T25B A1SJ72T25B

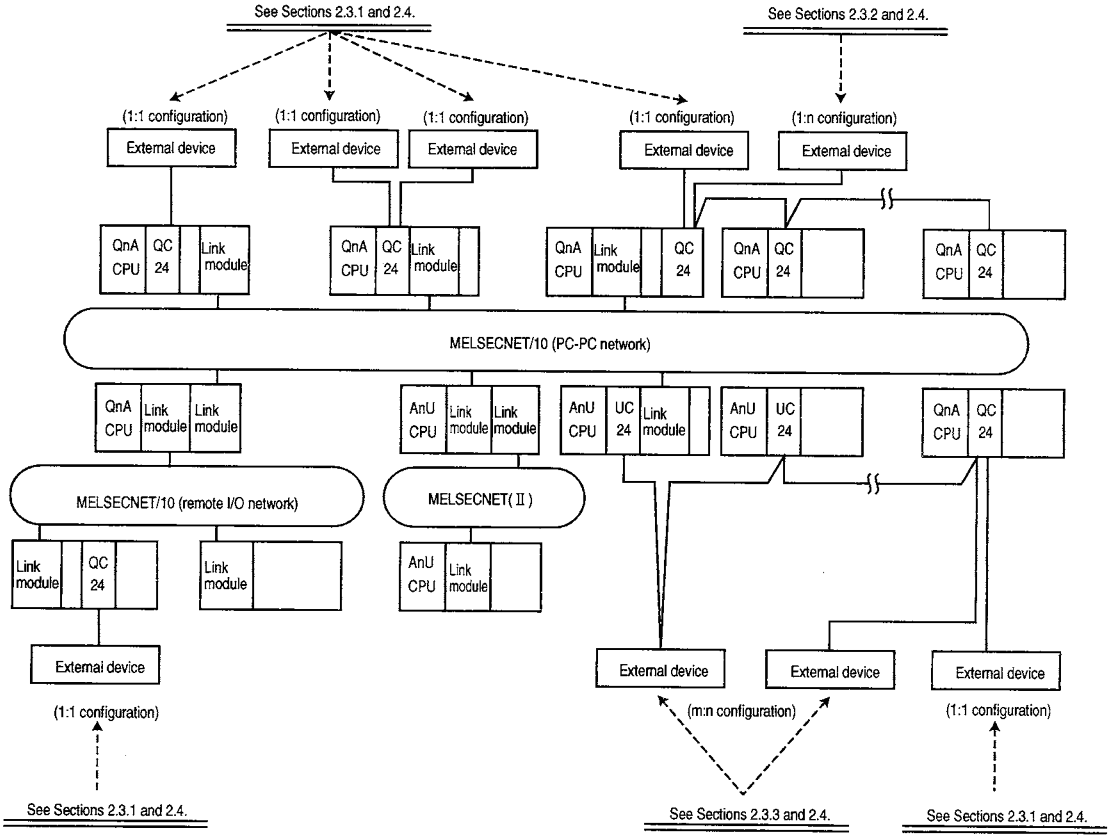
③ Relay module

The following shows the link modules that can be inserted in each data link system or network system when external devices access the PLC of another station over a data link system or network system. External devices can access systems relayed by link modules with the model names shown below.

MELSECNET/10	AJ71QLP21(S/G) AJ71QBR11 A1SJ71QLP21 A1SJ71QBR11 AJ71LP21 AJ71BR11 AJ71LR21 A1SJ71LP21 A1SJ71BR11

2.3 External Devices and PLC CPU System Configurations and Available Functions

The following describes the kinds of external device and PLC CPU system configurations and the QC24(N) data communications functions that can be used by each configuration.



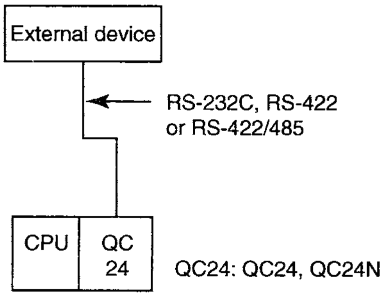
QC24: QC24, QC24N

Note

The table below shows the kinds of interface, available system configurations, and communication methods of each QC24(N). See the following pages for descriptions.

Model name	Interface	External device and QC24(N) connection	Communication system
AJ71QC24(N) A1SJ71QC24(N)	Independent operation and linked operation	—	—
	CH1: RS-232C	1:1	Full-duplex/half-duplex (selected by buffer memory)
	CH2: RS-422/485	1:1 or 1:n	Full-duplex/half-duplex
		m:n	Half-duplex
AJ71QC24(N)-R2 A1SJ71QC24(N)-R2	Independent operation only	—	—
	CH1: RS-232C	1:1	Full-duplex/half-duplex (selected by buffer memory)
	CH2: RS-232C	1:1	Full-duplex/half-duplex (selected by buffer memory)
AJ71QC24(N)-R4	Independent operation and linked operation	—	—
	CH1: RS-422	1:1	Full-duplex/half-duplex
	CH2: RS-422/485	1:1 or 1:n	Full-duplex/half-duplex
		m:n	Half-duplex
Notes	(1) The two QC24(N) interfaces are linked by the same function only when the external device and QC24(N) connection configuration is 1:n or m:n. (2) The communication systems of each QC24(N) protocol are shown below. Data can be transferred with external devices over either of the QC24(N) interfaces. • Dedicated protocols .... Half-duplex communications (When on-demand function used: full-duplex/half duplex communications) • Non procedure protocol .... Full-duplex/half-duplex communications • Bidirectional protocol .... Full-duplex/half-duplex communications		

2.3.1 1:1 ratio of external device to PLC CPU



★The 1:1 system shown at the left can be built for each QC24(N) interface.

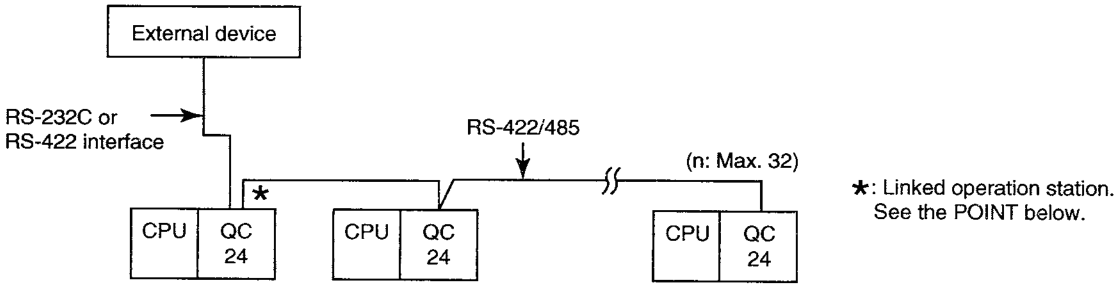
Function		External device communications (control)			Reference section
		RS-232C	RS-422	RS-422/485	
Communications using dedicated protocols	Communications by transmission of commands from external device using each frame in the ASCII mode. (QnA frame, QnA extension frame, A compatible frame, QnA simplified frame)	○	○	○	Chapter 5 Chapter 6 Chapter 8
	Communications by transmission of commands from external device using QnA extension format in the binary mode.	○	○	○	
	Communications from PLC CPU to external device using each frame above and user frames. (On-demand function)	○	○	○	Section 6.9, Chapter 7
	Access to another station over a data link system, network system, or multidrop connection.	○	○	○	Section 2.4
	Access to another station through QC24(N) by QnACPU link dedicated instruction.	*1	*1	*1	Chapter 20
	Access to QnACPU from QnACPU compatible GPP function peripheral device through the QC24(N). (Binary mode CH1 side only)	○	○	×	Section 4.9
	Registration of user frame.	○	○	○	Chapter 16
	Mode switching (forced mode switching)	○	○	○	Chapter 18
Communications using non procedure protocol	Communications between PLC CPU and external device	○	○	○	Chapter 9 to Chapter 11
	Communications using user frames	○	○	○	
Communications using bidirection protocol	Communications between PLC CPU and external device	○	○	○	Chapter 12 to Chapter 13
Independent operation of two I/F		○	○	○	
Linked operation of two I/F		—	—	—	
Transmission control	DTR/DSR signal control (DC code control and selection)	○	×	×	Section 14.3
	RS/CS signal control	○	×	×	
	CD signal control	○	×	×	
	DC code control (DTR/DSR control and selection)	○	○	○	
Half-duplex communications control		○	×	×	Section 14.5
Communication by public line using the modem function		○	×	×	Chapter 21

○: Relevant function available ×: Relevant function unavailable —: Outside the objective

*1 Available when QC24(N) connected as an external device.

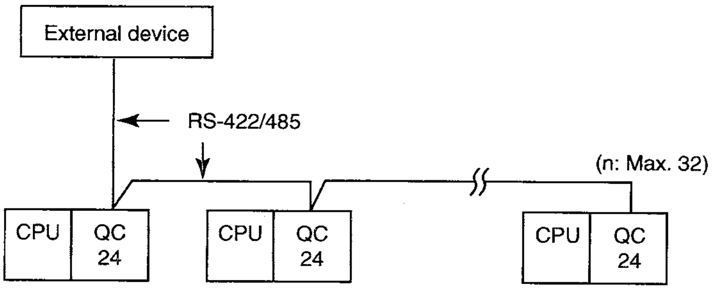
2.3.2 1:n ratio of external device to PLC CPU

1 When external device connected by RS-232 or RS-422 interface



QC24: QC24, QC24N

2 When external device connected by RS-422/485 interface



QC24: QC24, QC24N

POINT

When an external device connected to the QC24(N) using the RS-232C or RS-422 interface accesses the PLC CPU of a station other than the connected station, the QC24(N) connected to the external device must be set to the linked operation mode.

Function		External device communications (control)			Reference section
		RS-232C	RS-422	RS-422/485	
Communications using dedicated protocols	Communications by transmission of commands from external device using each frame in the ASCII mode. (QnA frame, QnA extension frame, A compatible frame, QnA simplified frame)	○	○	○	Chapter 5 Chapter 6 Chapter 8
	Communications by transmission of commands from external device using QnA extension frame in the binary mode.	○	○	○	
	Transmission from PLC CPU to external device using each frame above and user frames. (On-demand function)	×	×	×	
	Access to another station over a data link system, network system, or multidrop link.	○	○	○	Section 2.4
	Access to another station through QC24(N) by QnACPU link dedicated instruction	*1	*1	○	Chapter 20
	Access to QnACPU from QnACPU compatible GPP function peripheral device through QC24(N) (CH1 side in binary mode only)	○	○	×	Section 4.9
	Registration of user frames	○	○	○	Chapter 16
	Mode switching (forced mode switching)	○	○	○	Chapter 18
Communications using non procedure protocol	Communications between PLC CPU and external device	○	○	○	Chapter 9 to Chapter 11
	Communications using user frames	○	○	○	
Communications using bidirectional protocol	Communications between PLC CPU and external device	×	×	×	
Independent operation of two I/F		○	○	○	
Linked operation of two I/F		*2			Section 4.3.1 *2
Transmission control	DTR/DSR signal control (DC code control and selection)	○	×	×	Section 14.3
	RS/CS signal control	○	×	×	
	CD signal control	○	×	×	
	DC code control (DTR/DSR control and selection)	○	○	○	
Half-duplex communications control		○	×	×	Section 14.5
Communication by public line using the modem function		×	×	×	Chapter 21

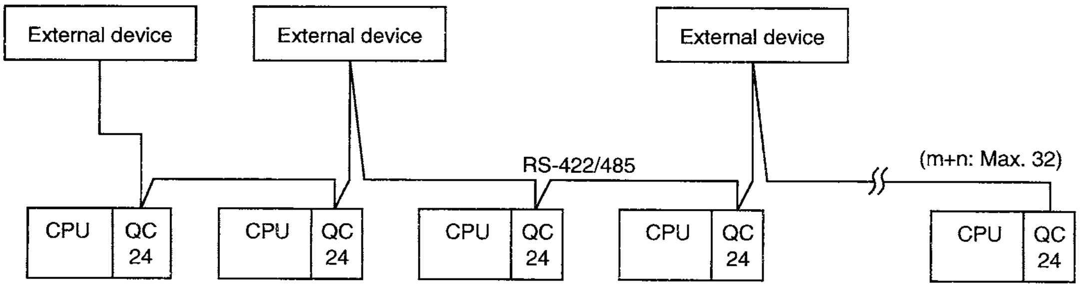
○: Relevant function available ×: Relevant function unavailable

*1 Available when QC24(N) connected as an external device.

*2 Linked actions are possible between the RS-232C/RS-422 interface and RS422/485 interface of the following QC24(N)s:
- AJ71QC24 AJ71QC24-R4 A1SJ71QC24
- AJ71QC24N AJ71QC24N-R4 A1SJ71QC24N A1SJ71QC24N1

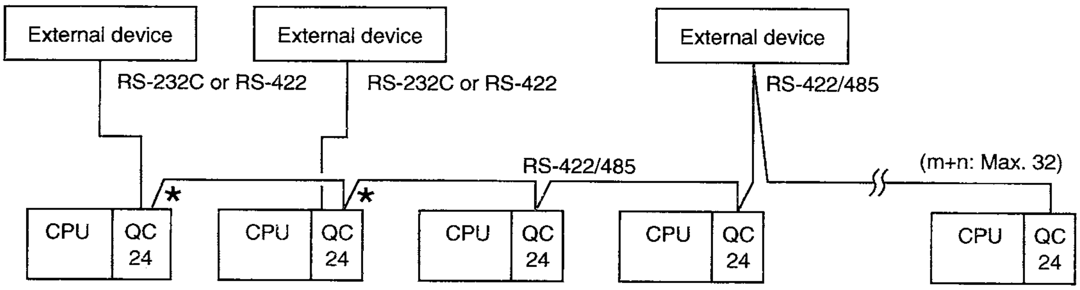
2.3.3 m:n ratio of external device to PLC CPU

1 **When external device connected only by RS-422/485 interface**



QC24: QC24, QC24N

2 **When external device connected by RS-232C, RS-422, or RS-422/485 interface**



*: Linked-operation station.
See POINTS (2).
QC24: QC24, QC24N

POINTS

(1) For an m:n system configuration, up to 32 external devices and PLC CPUs can be connected. With this system, the external devices can access the PLC CPU using dedicated protocol formats 1 and 2 and format 4.
Dedicated protocol formats 3 and 5 and non procedure protocol and bidirectional protocol cannot be used to transfer data.

(2) When the external devices connected to the QC24(N) using RS-232C or RS-422 interface access another external device or the PLC CPU of a station other than the connected station, the QC24(N) connected to the external device must be set to the linked operation mode.

Function		External device communications (control)			Reference section
		RS-232C	RS-422	RS-422/485	
Communications using dedicated protocols	Communications by transmission of commands from external device using each frame in the ASCII mode. (QnA frame, QnA extension frame, A compatible frame, QnA simplified frame)	o	o	o	Chapter 5 Chapter 6 Chapter 8
	Communications by transmission of commands from external device using QnA extension frame in the binary mode	×	×	×	
	Transmission from PLC CPU to external device using each frame above and user frames (On-demand function)	×	×	×	
	Access to another station over a data link system, network system, or multidrop link.	o	o	o	Section 2.4
	Access to another station through QC24(N) using QnACPU link dedicated instruction.	×	×	×	
	Access to another station from QnACPU compatible GPP function peripheral device through QC24(N). (CH1 side in binary mode only)	×	×	×	
	Registration of user frames	o	o	o	Chapter 16
	Mode switching (forced mode switching)	o	o	o	Chapter 18
Communications using non produce protocol	Communication between PLC CPU and external device.	×	×	×	
	Communications using user frames.	×	×	×	
Communications using bidirectional protocol	Communications between PLC CPU and external device.	×	×	×	
Independent operation of two I/F		o	o	o	
Linked operation of two I/F		*1			Chapter 4.3.1 *2
Transmission control	DTR/DSR signal control (DC code control and selection)	o	×	×	Section 14.3
	RS/CS signal control	o	×	×	
	CD signal control	o	×	×	
	DC code control (DTR/DSR control and selection)	o	o	o	
Half-duplex communications control		o	×	×	Section 14.5
Communication by public line using the modem function		×	×	×	Chapter 21

o: Relevant function available ×: Relevant function unavailable

*1 Linked actions are possible between the RS-232C/RS-422 interface and RS422/485 interface of the following QC24(N)s:
- AJ71QC24 AJ71QC24-R4 A1SJ71QC24
- AJ71QC24N AJ71QC24N-R4 A1SJ71QC24N A1SJ71QC24N1

2.4 Combining the QC24(N) with a Data Link System and Network System

By installing the QC24(N) in a QnACPU station connected to a data link system (MELSECNET (II), MELSECNET/B) or network system (MELSECNET/10) or to the remote station of a network system, external devices can use the dedicated protocols to access the PLC CPU of other stations.

All devices can access the PLC CPU of the master station and local station of the other station data link system and management station and main station of a network system, and a multidrop link PLC CPU.

The buffer memory of the special functions module of remote stations can be accessed.

The following uses an example to show the PLC range that can be accessed from external stations when the QC24(N) is installed in a data link system or network system station.

When accessing another station's PLC on a data link system or network system, always read this section.

When another station's PLC is not accessed, you do not have to read this section.

POINTS

(1) Another station's PLC CPU on a data link system or network system cannot use the on-demand function that sends data from PLC CPU to external device.

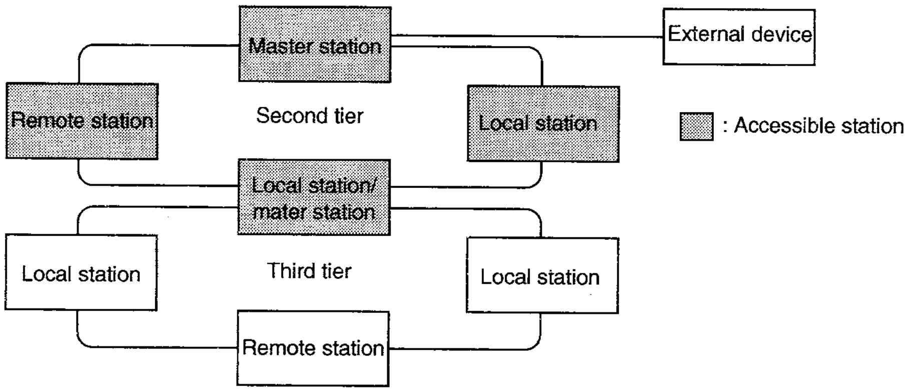
(2) External devices cannot access A0J2CPUP23/R23 and A0J2P25/R25 stations on a data link system.

(3) Section 5.3 describes in detail the relationship between the QC24(N) station and accessible range.

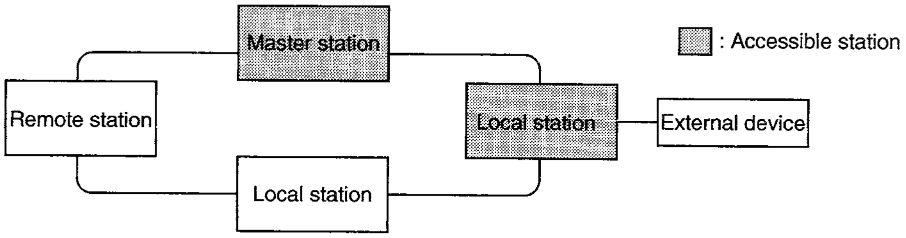
2.4.1 Data link system

By installing the QC24(N) in a QnACPU station connected by a data link system, external device can access the PLC CPU of other stations (master station, local station, remote station) on the data link system containing the QC24(N) station.

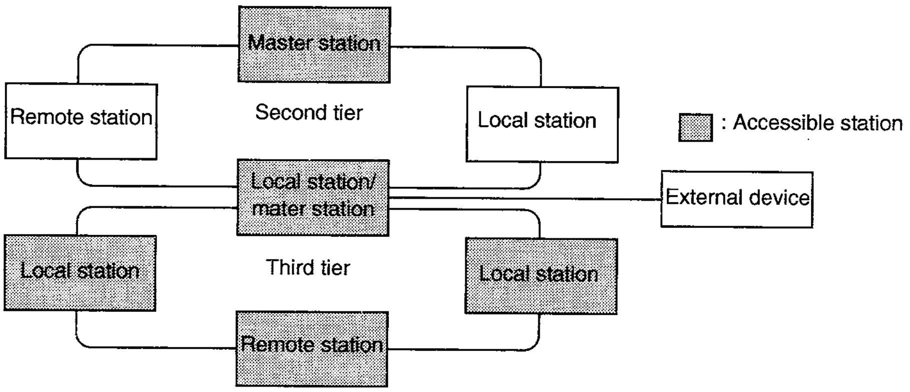
1 **When QC24(N) installed in second tier master station of data link system**



2 **When QC24(N) installed in local station of data link system**



3 **When QC24(N) installed in third tier master station of data link system**



POINT

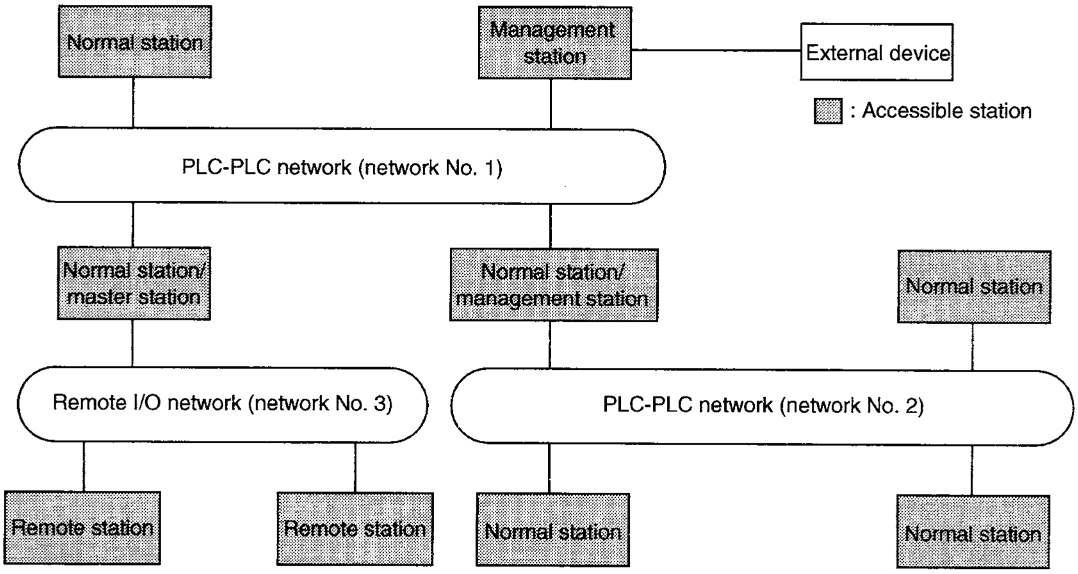
Regarding the tiers (any tier for three-tier system) shown in the illustrations in 1 through 3 above, the accessible stations also apply to the MELSECNET/B.

2.4.2 Network system

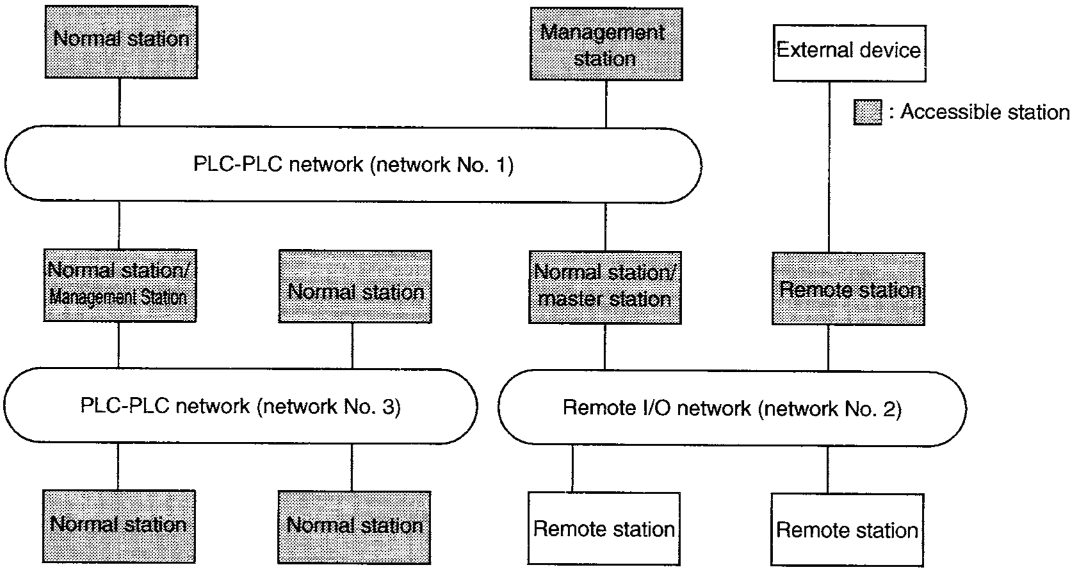
By installing the QC24(N) in a QnACPU station or remote station connected by a network system, external devices can access the PLC of other stations (management station, normal station, remote station) on the designated network system.

The routing parameters and MELSECNET/10 parameters for accessing other stations must be set at the relevant stations. (Each station on another network that relays multiple stations can be accessed using routing parameters.)

1 **When QC24(N) installed in PLC-PLC network management station/normal station and remote I/O network master station**



2 **When QC24(N) installed in remote station of remote I/O network**



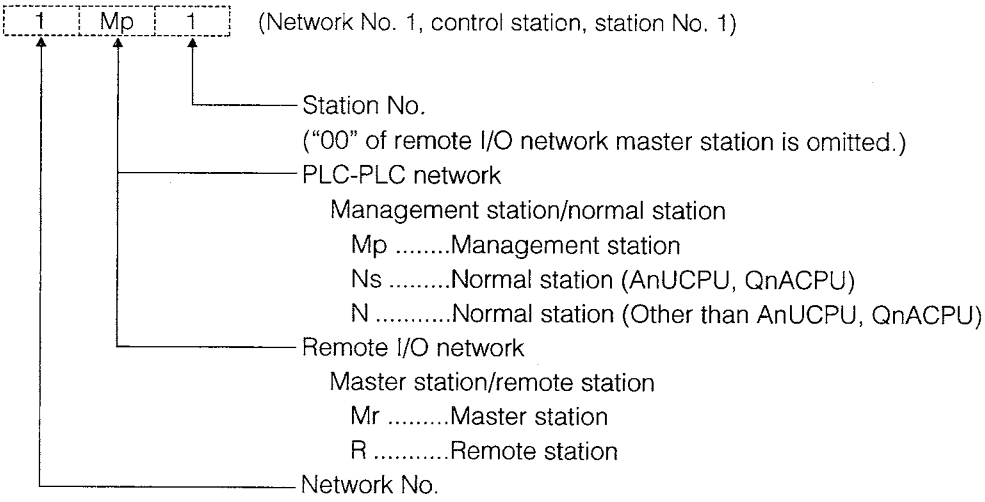
2.4.3 When data link system and network system mixed

With a system that connects a data link system and a network system at an intermediate station, by installing the QC24(N) in any station, external devices can access the PLC of other stations on the designated data link system/network system.

The following uses examples to show the range of access to other stations, including multidrop links.

(Meaning of symbols of each station shown in the illustrations.)

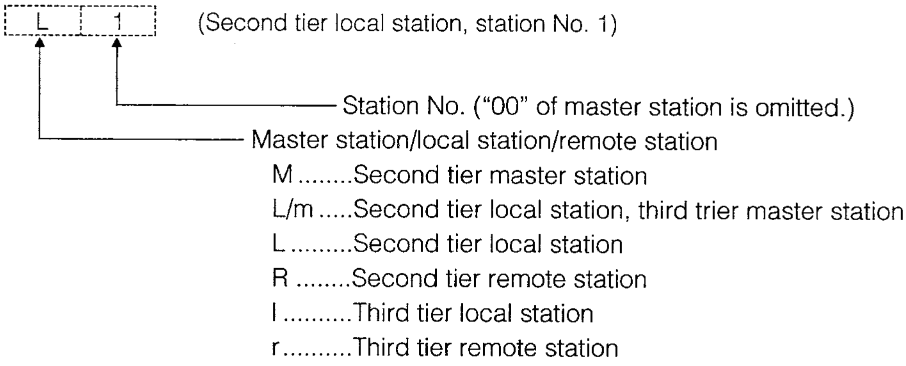
- Network system (MELSECNET/10)



(Network No. 1, control station, station No. 1)

Station No.
("00" of remote I/O network master station is omitted.)
PLC-PLC network
Management station/normal station
Mp ....Management station
Ns ....Normal station (AnUCPU, QnACPU)
N ....Normal station (Other than AnUCPU, QnACPU)
Remote I/O network
Master station/remote station
Mr ....Master station
R ....Remote station
Network No.

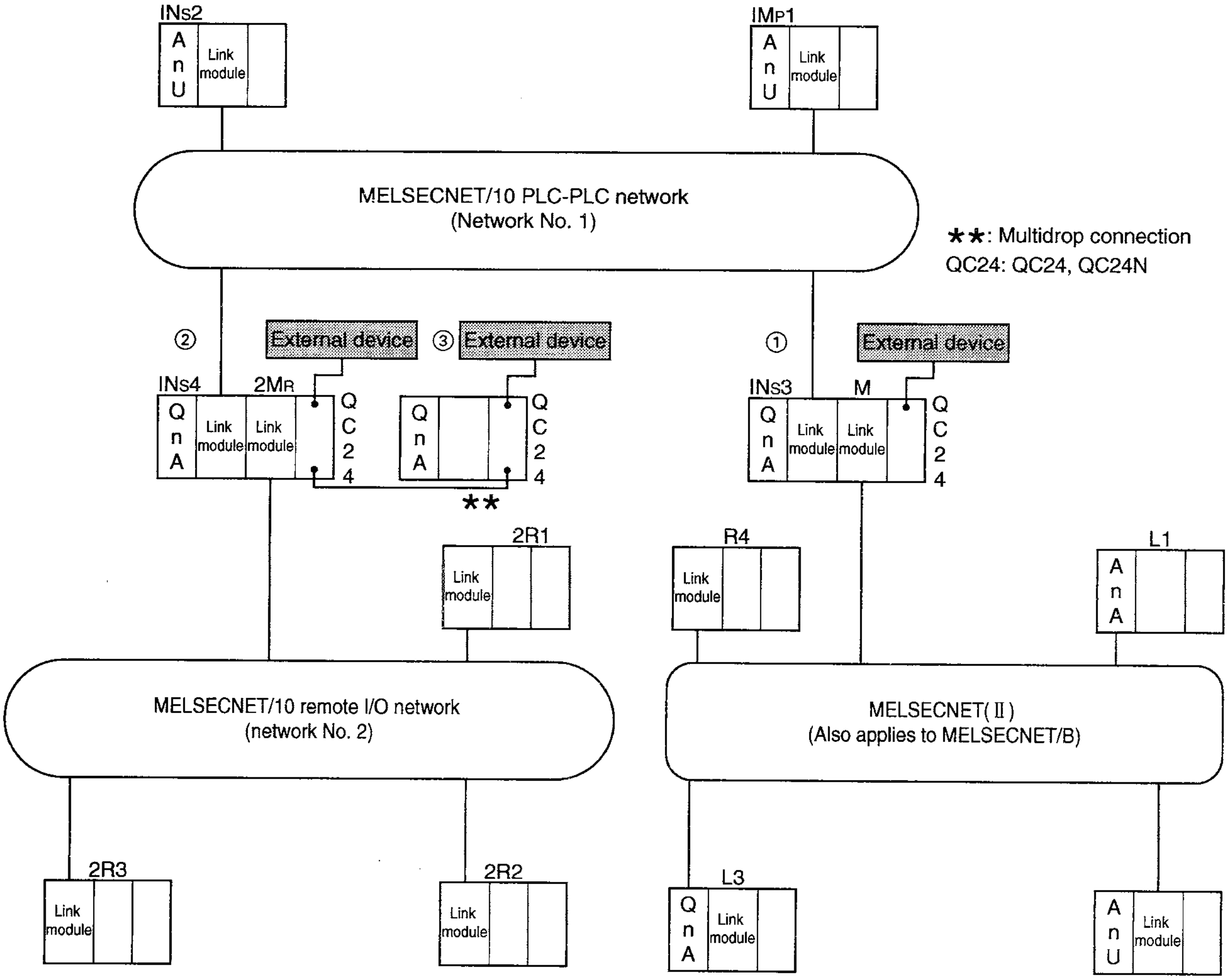
- Data link system (MELSECNET(II), MELSECNET/B)



(Second tier local station, station No. 1)

Station No. ("00" of master station is omitted.)
Master station/local station/remote station
M ....Second tier master station
L/m .....Second tier local station, third trier master station
L ....Second tier local station
R ....Second tier remote station
l ....Third tier local station
r..........Third tier remote station

1 Accessible range when intermediate station is QnACPU

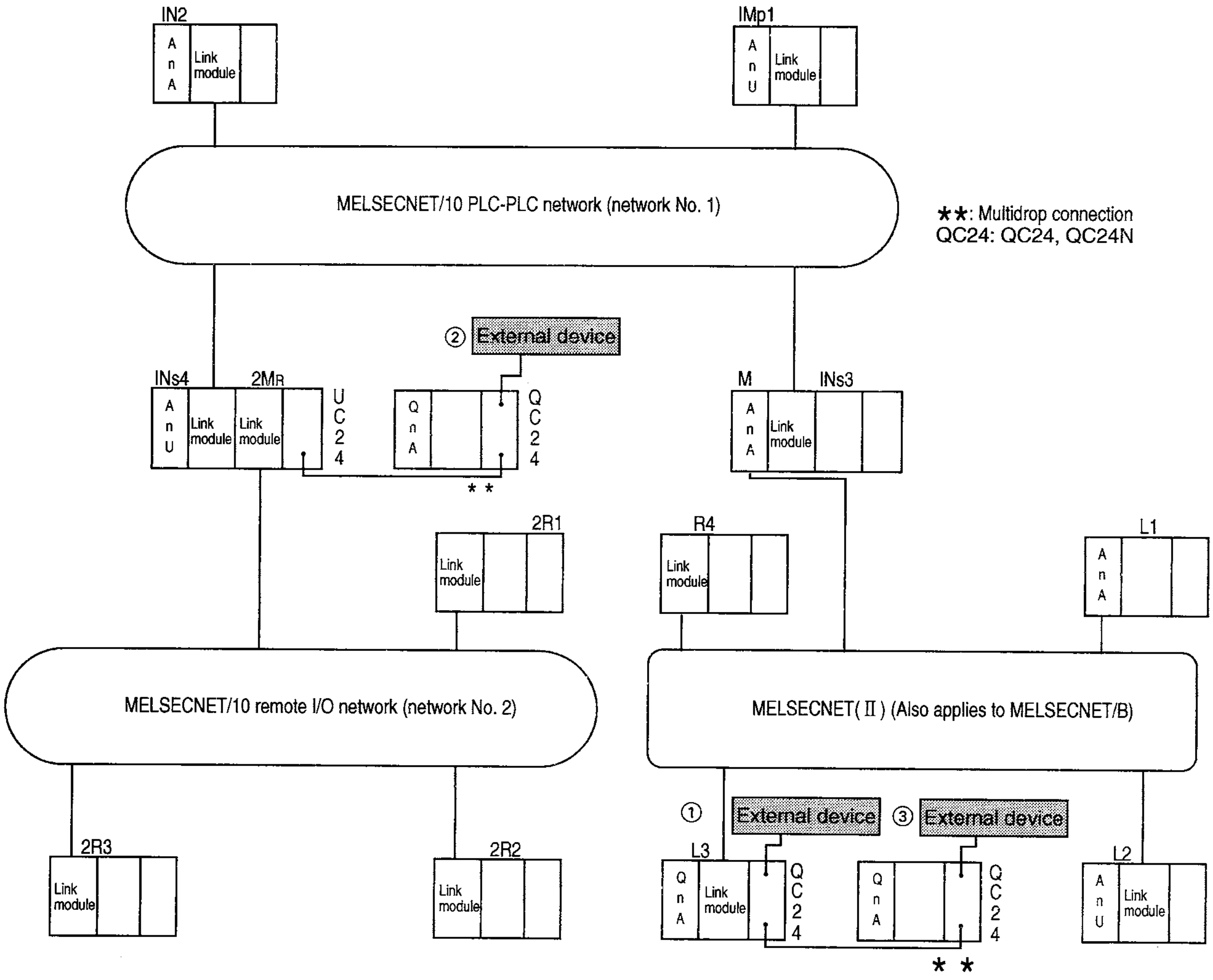


★★: Multidrop connection
QC24: QC24, QC24N

Stations accessible from external device	Station to which external device connected											
	1Mp1	1Ns1	1Ns3 M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	③
①	○	○	○	○	○	○	○	○	○	○	○	○
②	○	○	○	○	○	○	○	×	×	×	×	○
③	○	○	○	○	○	○	○	×	×	×	×	○

○: Accessible
×: Not accessible

2 Access range when intermediate station is not a QnACPU



**: Multidrop connection
QC24: QC24, QC24N

Stations accessible from external device	Station to which external device connected												
	1Mp1	1N2	1Ns3 M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	②	③
①	×	×	○	×	×	×	×	×	×	○	×	×	○
②	○	○	○	○	○	○	○	×	×	×	×	○	×
③	×	×	○	×	×	×	×	×	×	○	×	×	○

○ : Accessible
× : Not accessible

3. SPECIFICATIONS

The following shows the QC24(N) data specifications, interface specifications, and other specifications.

Refer to the User's Manual of the QnACPU used for the QC24(N) general specifications. See the User's Manual (Hardware) of the QC24(N) used for the hardware specifications.

3.1 Transmission Specifications

The following shows the QC24(N) transmission specifications. The transmission specifications when communicating via the modem function are explained in Section 21.3.1. The communication specifications between modem/TA of local station QC24N end and the QC24N that are not listed in Section 21.3.1 have the specifications shown in the table below:

<table>
<tr><th colspan="2">Item</th><th colspan="5">Specifications</th></tr>
<tr><td colspan="2">Interface (H/W specifications)</td><td colspan="2">AJ71QC24, AJ71QC24N,
A1SJ71QC24, A1SJ71QC24N,
A1SJ71QC24N1</td><td colspan="2">AJ71QC24-R2, AJ71QC24N-R2,
A1SJ71QC24-R2, A1SJ71QC24N-R2,
A1SJ71QC24N1-R2</td><td>AJ71QC24-R4
AJ71QC24N-R4</td></tr>
<tr><td></td><td>CH1</td><td colspan="2">Conform to RS-232C (Full-duplex/half-duplex communications) *1</td><td colspan="2">Conform to RS-232C (Full-duplex/half duplex communications) *1</td><td>Conform to RS-422 Full-duplex/half-duplex (communications)</td></tr>
<tr><td></td><td>CH2</td><td colspan="2">Conform to RS-422/485 (Full-duplex/half-duplex communications)</td><td colspan="2">Conform to RS-232C (Full-duplex/half-duplex communications) *1</td><td>Conform to RS-422/485 (Full-duplex/half-duplex communications)</td></tr>
<tr><td colspan="2">Data communications function communications system</td><td colspan="5">—</td></tr>
<tr><td></td><td>Dedicated protocols</td><td colspan="5">Half-duplex communications (When on-demand function used: full-duplex communications/half-duplex communications)</td></tr>
<tr><td></td><td>Non procedure protocol</td><td colspan="5">Full-duplex communications/half-duplex communications</td></tr>
<tr><td></td><td>Bidirectional protocol</td><td colspan="5">Full-duplex communications/half/duplex communications</td></tr>
<tr><td colspan="2">Synchronization system</td><td colspan="5">Start-stop synchronization (asynchronous system)</td></tr>
<tr><td rowspan="2">Transmission speed (BPS)</td><td>QC24</td><td colspan="5">300, 600, 1200, 2400, 4800, 9600, 19200 *2</td></tr>
<tr><td>QC24N</td><td colspan="5">300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 14400, 28800, 57600, 115200 *2</td></tr>
<tr><td colspan="2">Data format (number of bits)</td><td colspan="5">*Data bits-stop bits format selected by switch.</td></tr>
<tr><td></td><td>Start bits</td><td colspan="5">1</td></tr>
<tr><td></td><td>Data bits</td><td colspan="5">7 / 8</td></tr>
<tr><td></td><td>Parity bits</td><td colspan="5">1 (YES)/0 (NO) *When YES, ODD/EVEN is selected. *3</td></tr>
<tr><td></td><td>Stop bits</td><td colspan="5">1 / 2</td></tr>
<tr><td colspan="2">Access cycle</td><td colspan="5">—</td></tr>
<tr><td></td><td>Dedicated protocols</td><td colspan="5">Processes one request during installed PLC CPU END processing.
(Can be changed to process multiple requests by PLC CPU parameter.)
When the QC24 is installed in a remote station, processes one request during each link scan.
(Number of scans that must be processed/number of link scans depends on the contents of the request. (See Appendix 3.))</td></tr>
<tr><td></td><td>Non procedure protocol</td><td colspan="5" rowspan="2">Sends each time a send request is issued. Can receive at any time.</td></tr>
<tr><td></td><td>Bidirectional protocol</td></tr>
<tr><td colspan="2">Error detection</td><td colspan="5">—</td></tr>
<tr><td></td><td>Parity check</td><td>YES/NO</td><td colspan="4">*All protocols. When YES, ODD/EVEN is selected by switch. *3</td></tr>
<tr><td></td><td>Sum check code</td><td>YES/NO</td><td colspan="4">*Dedicated protocols/bidirection protocol selected by switch.
*Non procedure protocol selected by user frame.</td></tr>
<tr><td colspan="2" rowspan="5">Transmission control</td><td></td><td>RS-232C</td><td>RS-422</td><td>RS-422/485</td><td rowspan="5">DTR/DSR signal control and DC code control are selected by the user.</td></tr>
<tr><td>DTR/DSR signal control</td><td>YES</td><td>YES</td><td>NO</td></tr>
<tr><td>RS/CS signal control</td><td>YES</td><td>NO</td><td>NO</td></tr>
<tr><td>CD signal control</td><td>YES</td><td>NO</td><td>NO</td></tr>
<tr><td>DC code control</td><td>YES</td><td>YES</td><td>YES</td></tr>
<tr><td colspan="2">Number of EEPROM writes</td><td colspan="5">Max. 100,000 times for same area.</td></tr>
</table>

(Continued on next page)

(Continued from preceding page)

<table>
<tr><th colspan="2">Item</th><th colspan="3">Specifications</th></tr>
<tr><td colspan="2" rowspan="2">Circuit connection
(External device: PLC)</td><td>AJ71QC24, AJ71QC24N,
A1SJ71QC24, A1SJ71QC24N,
A1SJ71QC24N1</td><td>AJ71QC24-R2, AJ71QC24N-R2,
A1SJ71QC24-R2, A1SJ71QC24N-R2,
A1SJ71QC24N1-R2</td><td>AJ71QC24-R4
AJ71QC24N-R4</td></tr>
<tr><td colspan="3">For independent operation of each interface</td></tr>
<tr><td rowspan="3">CH1</td><td>Dedicated protocols</td><td rowspan="3">1:1</td><td rowspan="3">1:1</td><td rowspan="3">1:1</td></tr>
<tr><td>Non procedure protocol</td></tr>
<tr><td>Bidirectional protocol</td></tr>
<tr><td rowspan="3">CH2</td><td>Dedicated protocols</td><td>1:1, 1:n, m:n *4</td><td rowspan="2">1:1</td><td>1:1, 1:n, m:n *4</td></tr>
<tr><td>Non procedure protocol</td><td>1:1, 1:n *4</td><td>1:1, 1:n *4</td></tr>
<tr><td>Bidirectional protocol</td><td>1:1</td><td>1:1</td><td>1:1</td></tr>
<tr><td colspan="2"></td><td colspan="3">For linked operation between interfaces</td></tr>
<tr><td rowspan="3">CH1 · 2</td><td>Dedicated protocols</td><td>1:n, m:n *4</td><td rowspan="3">Linked operation impossible</td><td>1:n, m:n *4</td></tr>
<tr><td>Non procedure protocol</td><td>1:n *4</td><td>1:n *4</td></tr>
<tr><td>Bidirectional protocol</td><td>Data communications impossible</td><td>Data communications possible</td></tr>
<tr><td colspan="2">Transmission distance
(total distance)</td><td colspan="3"><table><tr><th>— Interface</th><th>Transmission distance</th></tr><tr><td>RS-232C</td><td>Up to 15 m (49.21 ft.)</td></tr><tr><td>RS-422</td><td>Up to 1200 m (3937 ft.) *5</td></tr><tr><td>RS-422/485</td><td>Up to 1200 m (3937 ft.)</td></tr></table></td></tr>
<tr><td colspan="2" rowspan="2">5VDC internal current drain</td><td>AJ71QC24 : 0.3A
A1SJ71QC24 : 0.24A</td><td>AJ71QC24-R2 : 0.2A
A1SJ71QC24-R2 : 0.155A</td><td>AJ71QC24-R4 : 0.38A</td></tr>
<tr><td>AJ71QC24N : 0.4A
A1SJ71QC24N : 0.35A
A1SJ71QC24N1 : 0.38A</td><td>AJ71QC24N-R2 : 0.3A
A1SJ71QC24N-R2 : 0.3A
A1SJ71QC24N1-R2 : 0.30A</td><td>AJ71QC24N-R4 : 0.6A</td></tr>
<tr><td colspan="2" rowspan="2">Weight</td><td>AJ71QC24 : 0.385kg (0.85lb)
A1SJ71QC24 : 0.294kg (0.65lb)</td><td>AJ71QC24-R2 : 0.37kg (0.81lb)
A1SJ71QC24-R2 : 0.249kg (0.55lb)</td><td>AJ71QC24-R4 : 0.385kg (0.85lb)</td></tr>
<tr><td>AJ71QC24N : 0.385kg (0.85lb)
A1SJ71QC24N : 0.296kg (0.65lb)
A1SJ71QC24N1 : 0.30kg (0.66lb)</td><td>AJ71QC24N-R2 : 0.37kg (0.81lb)
A1SJ71QC24N-R2 : 0.258kg (0.57lb)
A1SJ71QC24N1-R2 : 0.26kg (0.57lb)</td><td>AJ71QC24N-R4 : 0.385kg (0.85lb)</td></tr>
<tr><td colspan="2">Number of occupying I/Os</td><td colspan="3">32 (occupy one slot) *6</td></tr>
<tr><td colspan="2">Recommended cable</td><td colspan="3">—</td></tr>
<tr><td></td><td>RS-232C</td><td colspan="3">7/0.127 □ P HRV.SV....Outside diameter 8.5mm (0.33 in.) or more
(Oki Electric Wire Co., Ltd....Number of pairs designated in □.)</td></tr>
<tr><td></td><td>RS-422</td><td colspan="3" rowspan="2">SPEV(SB)-MPC-0.2 × 3P....Outside diameter Approx. 6.5mm (0.26 in.)
SPEV(SB)-0.2 × 3.............. Outside diameter Approx. 7.5 mm (0.3 in.)
[Both Mitsubishi Electric Wire Industry Co., Ltd.] *7</td></tr>
<tr><td></td><td>RS-422/485</td></tr>
</table>

*1 Set to transfer data with external devices by full-duplex communications system when the QC24(N) is started. Switch to half-duplex communications system as described in Section 14.5.

*2 Transmission rate setting range differs with simultaneous use and the communication system of the two interfaces.
Transfer data within the range given in Section 4.3.2.

*3 Parity bit is vertical parity.
When handling the parity bit, use switch setting to select odd parity/even parity.

*4 The total number of n, m+n is maximum 32.

*5 When an QnACPU compatible GPP function peripheral device is connected, the maximum transmission distance is 30 m (98.4 ft.).

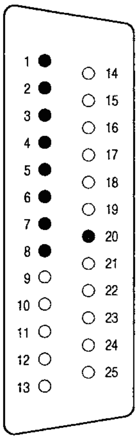
*6 When using the GPP function to allocate I/O, set special 32 points.
When registering the model name, register [AJ71QC24].

*7 Recommended cables SPEV(SB)-MPC-0.2 × 3P and SPEV(SB)-0.2 × 3P have the same electrical characteristics, but their outline dimensions and internal wire colors are different.

3.2 RS-232C Specification

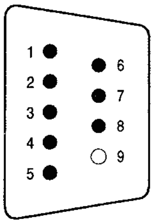
3.2.1 RS-232C connector specifications

The following describes the specifications of the RS-232C connector that connects the QC24(N) to an external device.



Pin number	Name	Signal abbreviation	Signal direction QC24(N)↔External device
1	FG	Frame ground	←→
2	SD (TXD)	Send data	→
3	RD (RXD)	Receive data	←
4	RS (RTS)	Request to send	→
5	CS (CTS)	Clear to send	←
6	DSR (DR)	Data set ready	←
7	SG	Signal ground	←→
8	CD	Receive carrier detection	←
20	DTR (ER)	Data terminal ready	→

Specifications of the RS-232C connector (25-pin)



Pin number	Name	Signal abbreviation	Signal direction QC24(N)↔External device
1	CD	Receive carrier detection	←
2	RD (RXD)	Receive data	←
3	SD (TXD)	Send data	→
4	DTR (ER)	Data terminal ready	→
5	SG	Signal ground	←→
6	DSR (DR)	Data set ready	←
7	RS (RTS)	Request to send	→
8	CD (CTS)	Clear to send	←

Specifications of the RS-232C connector (9-pin)

1 The control signals are described below. (The pin numbers of the 25-pin connector/9-pin connector are enclosed in parentheses.)

When transmitting data, the status of the DTR, DSR, RS, and CD control signals can be checked using the QC24(N) buffer memory (address 254H). See Section 19.2.

① RS signal (4/7)

The QC24(N) turns ON/OFF the RS signal as shown below according to the communication system. (The user can change the communication system.) (See Section 14.5.)
The RS signal is not turned OFF even when receive data cannot be stored in the QC24(N).

- When the communication system is full-duplex communications, if the QC24(N) ready signal (X (n+1) E) is ON, the QC24(N) turns ON the RS signal.
- When the communication system is half-duplex communications, when the QC24(N) sends data to an external device, it turns ON the RS signal.

② CS signal (5/8)

The QC24(N) can not send data to an external device only when this signal is OFF.
Be sure that this signal is always turned ON when the external device is ready to receive.

③ DSR signal (6/6)

- During DTR/DSR control, if this signal is OFF, the QC24(N) does not send data to the external device.
  Be sure that this signal is always turned ON when the external device is ready to receive.
- If DTR/DSR control is not implemented, the DSR signal status is ignored.

④ CD signal (8/1)

- The QC24(N) operates according to the CD terminal check setting.
  (See Section 4.7.2 3 .)

	CD terminal check enabled	CD terminal check disabled
Full-duplex	The QC24(N) performs send processing when the CD signal (receive carrier detection) is ON. If the CD signal is turned off during data communication, the QC24(N) initializes the transmission sequence.	The QC24(N) performs send processing regardless of the ON/OFF status of the CD signal. This enables data communications with an external device that cannot turn the CD signal ON/OFF.
Half-duplex	See Section 14.5.	Setting impossible.

⑤ DTR signal (20/4)

- If DTR/DSR control is implemented, the QC24(N) turns this signal ON/OFF as follows:

  If a dedicated protocol or bidirectional protocol is currently used, the QC24(N) turns ON the DTR signal when communications is enabled.

  For communications using the non procedure protocol, this signal is turned ON/OFF according to the vacant size of the receive data storage OS area. (When the QC24(N) is ready to receive data, it turns on the DTR signal.)

  When the DTR signal is OFF, the receive data is stored in the OS area. Thus, use the sequence program to read the receive data.
- If DTR/DSR control is not implements, the DTR signal is always ON.

2 The ON and OFF states of each signal indicate the following conditions:

	(Output side)	(Input side)
ON	5VDC to 15VDC,	3VDC to 15VDC
OFF	-5VDC to –15VDC,	-3VDC to –15VDC

3 **Interface connector**

- The QC24(N) uses the following type of RS-232C interface connector.

  Use a matching connector (25-pin/9-pin).
  25-pin D-sub (female) screw type / 9-pin D-sub (female) screw type
  17L-10250-27-D9AC (DDK Ltd.) / 17L-10090-27-D9AC (DDK Ltd.)

3.2.2 RS-232C cable

Use a 15 m (49.21 ft.), or shorter, cable conforming to the RS-232C standard as the RS-232C cable.

(Recommended cable)

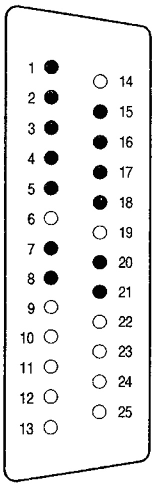
7/0. 127 □P HRV-SV.........(Oki Electric Wire Co., Ltd)
↑
Designates the number of pairs.
For 13 pairs (7/0.127 13P HRV-SV)

3.3 RS-422 and RS-422/485 Specifications

3.3.1 RS-422 connector and RS-422/485 terminal block specifications

The following describes the specifications of the RS-422 connector and RS-422/485 terminal block that connect the QC24(N) to an external device.

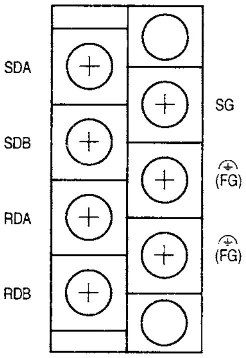
(RS-422 connector specifications)



Pin number	Signal abbreviation	Signal name	Signal direction QC24(N)↔External device	Notes
1	FG	Frame ground	←→	—
2	RDA	Receive data (+)	←	
3	SDA	Send data (+)	→	
4	DSRA	Data set ready (+)	←	
5	DTRA	Data terminal ready (+)	→	
7	SG	Signal ground	←→	
8	SG	Signal ground	←→	
12	—	—		No connection
13	—	—		
15	RDB	Receive data (–)	←	—
16	SDB	Send data (–)	→	
17	DSRB	Data set ready (–)	←	
18	DTRB	Data terminal ready (–)	→	
20	SG	Signal ground	←→	
21	SG	Signal ground	←→	
24	—	—		No connection
25	—	—		

* The SG signal for pin numbers 7, 8 and 20 are connected inside the module.

(RS-422/485 terminal block specifications)



Signal abbreviation	Signal direction	Signal direction QC24(N)↔External device
SDA	Send data (+)	→
SDB	Send data (–)	→
RDA	Receive data (+)	←
RDB	Receive data (–)	←
SG	Signal ground	←→
FG	Frame ground	←→

1 **The following describes the control signals.**

① DSRA, DSRB

- If these signals remain ON during data communication from the QC24(N) to an external device, data is transmitted.
- Be sure that these signals are always turned ON when the external device is ready to receive.

② DTRA, DTRB

- If the QC24(N) is ready to transfer data, these signals are turned on.
- Send data from the external device when these signals are ON.

2 **Terminating resistor**

Connect the terminating resistor according to Section 4.7.3 and 4.7.4.

3 **Interface connector**

- The QC24(N) RS-422 interface connector type is shown below. Use a matching connector.

  25-pin D-sub (female) screw-fixing type
  17L-10250-27-D9AC (DDK Ltd.)

3.3.2 RS-422 and RS-422/485 cable specifications

1 Use a 1200 m (3937 ft.), or shorter, shielded cable that satisfies the same specifications as the RS-422/485 cable below as the RS-422 cable.

POINTS

(1) When a MELSEC-QnA Series GPP function peripheral device is connected, the maximum cable length is 30m (98.4 ft.). Use the special RS-422 cable (AC30R4, etc.).

(2) When an external device other than the device of (1) above is connected and the external device conforms to the RS-422 standard, the maximum cable length is 1200 m (3937 ft.).

(3) The connector shown in Section 3.3.1 3 is used to connect to the RS-422 interface (CH1) of the AJ71QC24(N)-R4.

2 Use a 1200m (3937 ft.), or shorter cable, that satisfies the following specifications as the RS-422/485 cable (cable that connects to the QC24(N) terminal block).

Also make the total distance within 1200 m (3937 ft.) when two or more de-vices are connected to the QC24(N) in a 1:n or m:n configuration.

Item	Description
Cable type	Shielded cable
Number of pairs	3P
Conductor resistance (20C˚)	88.0 Ω/km or less
Insulation resistance	10000 MΩ/km or more
Dielectric strength	500VDC, 1 minute
Electrostatic capacitance (1 kHz)	60nF/km or less on average
Characteristic impedance (100 kHz)	110 ± 10Ω
Recommended conductor size	0.2 mm^2 to 0.75 mm^2

(Recommended cable)

SPEV (SB)-MPC-0.2 × 3P
SPEV (SB)-0.2 × 3P } .... (Mitsubishi Electric Wire Industry Co., Ltd.)

* SPEV (SB)-MPC-0.2 × 3P and SPEV (SB)-0.2 × 3P have the same electrical characteristics, but different outside diameter and internal wire colors.

3.3.3 Precautions when sending data using RS-422 and RS-422/485 circuit

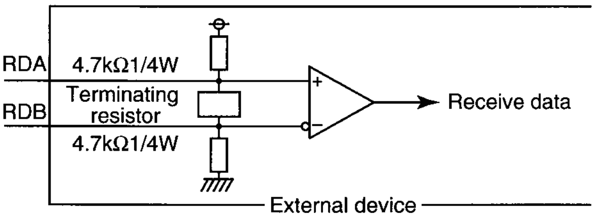
The following precautions must be observed when transferring data with an external device through the QC24(N) RS-422 or RS-422/485 interface.

Take the following into account when the transferring data with the external device.

1 **Error receive data countermeasures at external device during RS-422 or RS-422/485 connection**

If the external device may receive erroneous data, install a pull-up or pull-down resistor to the external device.

Installing a pull-up or pull-down resistor (resistance value criteria: approx. 4.7 kΩ 1/4 W) can prevent the reception of erroneous data.



POINT

When there is a pull-up or pull-down resistor at the external device, erroneous data is not received.

Note

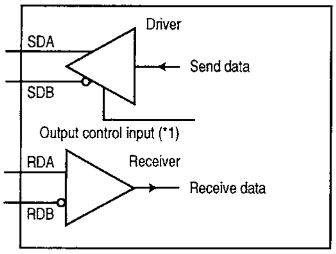
The following describes the case when a pull-up or pull-down resistor is not installed to the external device.
When no station is sending, the send line becomes high impedance and noise, etc. may cause the send line to change and the external device to receive erroneous data.
In this case, there is probably a parity error or framing error.
Therefore, skip the erroneous data.
Since the first data during data reception is fixed in the following cases, also skip the receive data until the head data is received.

- When using a dedicated protocol to send data
  The user selects the first data according to the mode and format used.
- When sending data using user frames with non procedure protocol
  The user selects the head data according to the user frames registered in the QC24(N).

2 RS-422/485 interface operation

① RS-422-485 interface construction

The following illustrations show the construction of the QC24(N) RS-422/485 interface driver (send)/receiver (receive).



*1 "Output control input" (also called send gate) of the driver section of the illustration at the left determines whether or not data from SDA/SDB is output to the outside.

② RS-422/485 interface operation

When the "output control input" in the illustration above is ON, the interface enters the low impedance state (state in which data can be sent).

When the "output control input" is OFF, the interface enters the high impedance state (state in which data is not sent).

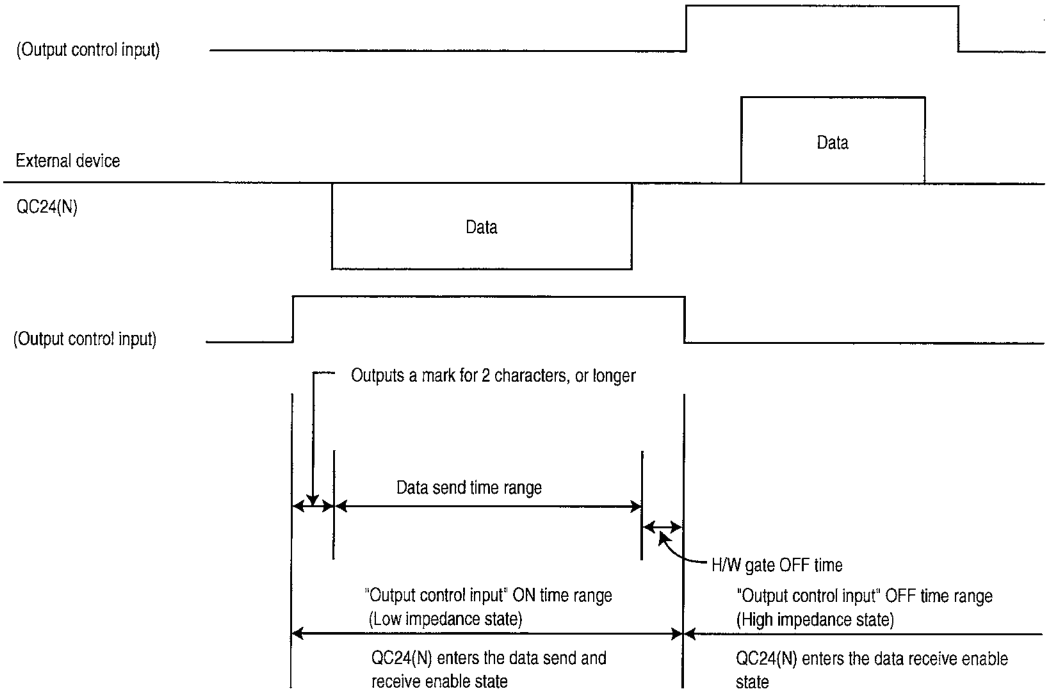
③ QC24(N) send start timing and send processing completion timing

- Send start timing

  During data transmission, the QC24(N) outputs the actual data after sending a mark for 2 characters, or longer, after the high impedance set by the operations described in ① and ② above is reset.

- Send processing completion timing

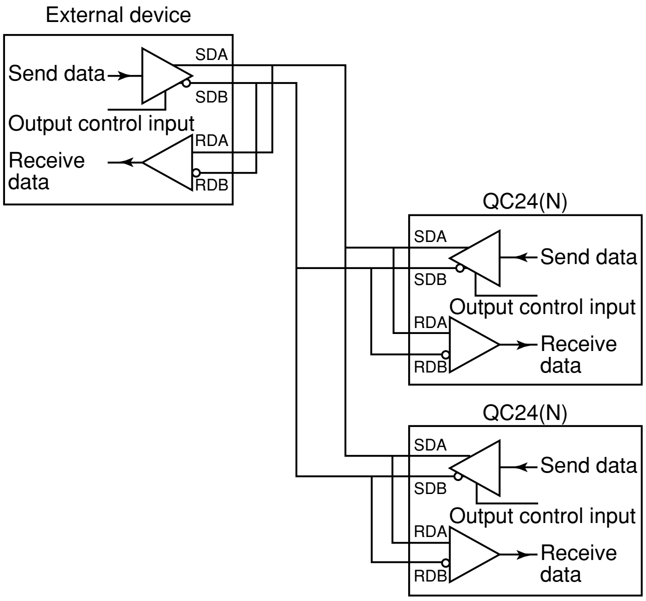
  The QC24(N) requires several μs as H/W gate OFF time before it can complete the send processing (make the impedance high state) after data seniding is finished.



POINTS

(1) When external device and QC24(N) connected in m:n configuration
When the send signal of each device is connected as shown below, if the "output control input" is turned ON at two or more devices, the relevant devices output (send) data at the same time.
For the external device to transfer data normally,
- "Output control input" must be turned ON only when sending data.
- "Output control input" must be turned OFF when not sending data.

The QC24(N) side automatically controls the output control input.



(2) When the QC24(N) is used, if operation of the two interfaces is linked (see Section 4.3.1 *2), the time to send one character becomes the QC24(N) H/W gate OFF time.
(The QC24(N) turns OFF the gate after the one-character send time.)

* The QC24(N)s that support link actions between two interfaces:
· AJ71QC24 AJ71QC24N
· AJ71QC24-R4 AJ71QC24N-R4
· A1SJ71QC24 A1SJ71QC24N A1SJ71QC24N1

3.4 PLC CPU Input/Output Signals Table

The following shows the QC24(N) I/O signals sent to and received from the PLC CPU.

(n) appended to the X and Y signals is determined by the number of the I/O signals of the slot into which the QC24(N) is inserted.

(Example: If the QC24(N) is inserted into slot 0 of the main base unit, Xn0→X0.)

The descriptions beginning from Section 4 use the representation shown in the Input Signal and Output Signal columns of the table.

1 **I/O signals table**

Signal direction: QC24(N)→PLC CPU			Signal direction: PLC CPU→QC24(N)		
Device No.	**Signal name**		**Device No.**	**Signal name**	
Xn0	CH1	Transmission ended normally	Yn0	CH1	Send request
Xn1		Transmission ended abnormally	Yn1		Receive data read complete
Xn2		Busy performing transmission processing	Yn2		Remote switching request (stop request during processing)
Xn3		Receive data read request	Yn3 to Yn6	(Prohibited to use)	
Xn4		Receive error detection			
Xn5	—				
Xn6	CH1	Mode switching (initial processing) *1	Yn7	CH2	Send request
Xn7	CH2	Transmission ended normally	Yn8		Receive data read complete
Xn8		Transmission ended abnormally	Yn9		Mode switching request (stop request during processing)
Xn9		Busy performing transmission processing	YnA to YnD	(Prohibited to use)	
XnA		Receive data read request			
XnB		Receive error detected			
XnC	—				
XnD	CH2	Mode switching (initial processing) *1			
XnE	CH1 ERR. LED ON		YnE	CH1 ERR. LED OFF request	
XnF	CH2 ERR. LED ON		YnF	CH2 ERR. LED OFF request	
X (n+1) 0	Initialization ended		Y (n+1) 0	Initialization request (standby request)	
X (n+1) 1	Dialing		Y (n+1) 1	Connection request	
X (n+1) 2	Connecting		Y (n+1) 2	Modem disconnection request	
X (n+1) 3	Initialization/connection ended abnormally		Y (n+1) 3	(Prohibited to use)	
X (n+1) 4	Modem disconnection ended		Y (n+1) 4	Notification-issued request	
X (n+1) 5	Notification ended normally		Y (n+1) 5	(Prohibited to use)	
X (n+1) 6	Notification ended abnormally		Y (n+1) 6		
X (n+1) 7	EEPROM read complete		Y (n+1) 7	EEPROM read request	
X (n+1) 8	EEPROM write complete		Y (n+1) 8	EEPROM write request	
X (n+1) 9	EEPROM system parameters write complete		Y (n+1) 9	EEPROM system parameters write request	
X (n+1) A	CH1	Global signal	Y (n+1) A	(Prohibited to use)	
X (n+1) B	CH2	Global signal	Y (n+1) B		
X (n+1) C	System parameters default complete		Y (n+1) C	System parameters default request	
X (n+1) D	—		Y (n+1) D to Y (n+1) F	(Prohibited to use)	
X (n+1) E	QC24 ready (access possible) *2				
X (n+1) F	Watchdog timer error *3				

*4

*1 The mode switching signal (Xn6/XnD) turns ON when the following function is executed.
- Mode switching, transmission sequence initialization, reception data clear, user frame use enable/disable designation, PLC CPU information clear

While the mode switching signal (Xn6/XnD) is ON, do not issue a communication request to the target interface.
(The communication processing of the QC24(N) is stopped while the mode switching signal (Xn6/XnD) is ON.)

*2 The QC24(N) ready signal (X (n+1) E) is turned ON when the PLC CPU can access the QC24(N).
Use this signal as the FROM/TO instruction, etc. interlock signal.

*3 The watchdog timer error signal (X (n+1) F) is turned on when the QC24(N) cannot operate normally. When this signal is turned on, the PLC CPU must be reset.

*4 X(n+1)0 to X(n+1) of the input signals and Y(n+1)0 to Y(n+1)6 of the output signals are the signals handled by the QC24N that can use modem functions shown in Section 1.4. The QC24(N)s that can not use the modem functions will be handled as follows:
X(n+1)0 to X(n+1)6 input signals : Unused
Y(n+1)0 to Y(n+1)6 output signals : Prohibited to use

IMPORTANT

Of the output signals for the special function modules from the PLC CPU, do not turn on the "Prohibited to use" signal.
If the "Prohibited to use" signal is output, PLC system may result in malfunctions.

2 Input signals (QC24(N)→PLC CPU)

There are 32 input signals, from Xn0 to X (n+1) F. All of them turns QC24 (N) ON/OFF.

Input signal and objective I/F		Signal abbreviation		Objective protocol			Reference section
CH1	CH2			Dedicated protocol	Non procedure protocol	Bidirectional protocol	
Xn0	—	CH1	Transmission ended normally	○ (On-demand)	○	○	Section 6.9, Chapter 7 Section 20.5.1, Chapter 9 to 11 Chapter 12 to 13
Xn1			Transmission ended abnormally				
Xn2			Performing transmission processing				
Xn3			Receive data read request	○ (RECV instruction use)	○	○	
Xn4			Receive error detection				
—		—		—			—
Xn6	—	CH1	Mode switching (initial processing) *1	○			Chapter 18
	Xn7	CH2	Transmission normally completed	○ (On-demand)	○	○	Section 6.9, Chapter 7 Section 20.5.1, Chapter 9 to 11 Chapter 12 to 13
	Xn8		Transmission ended abnormally				
—	Xn9		Busy performing transmission processing				
	XnA		Receive data read request	○ (RECV instruction use)	○	○	
	XnB		Receive error detected				
—		—		—			—
—	XnD	CH2	Mode switching (initial processing) *1	○			Chapter 18
XnE	—	CH1 ERR. LED ON		○			Section 19.1.3
—	XnF	CH2 ERR. LED ON					
X (n+1) 0		Initialization ended		○			Chapter 21
X (n+1) 1		Dialing					
X (n+1) 2		Connecting					
X (n+1) 3		Initialization/connection ended abnormally					
X (n+1) 4		Modem disconnection ended					
X (n+1) 5		Notification ended normally					
X (n+1) 6		Notification ended abnormally					
X (n+1) 7		EEPROM read complete		○			Chapter 16
X (n+1) 8		EEPROM write complete		○			
X (n+1) 9		EEPROM system parameters write complete		○			Chapter 15
X (n+1) A	—	CH1	Global	○	—	—	Section 6.8
—	X (n+1) B	CH2	Global				
X (n+1) C		System parameters default complete		○			Section 15.3.2
—		—		—			—
X (n+1) E		QC24 ready (accessible)		○			—
X (n+1) F		Watchdog timer error		○			—

*4

For *1 to *4, see *1 to *4 of 1.

3 Output signals (PLC CPU→QC24(N))

There are 32 output signals, from Yn0 to Y (n+1) F. All of them can be turned ON/OFF with sequence program.

Input signal and objective I/F		Signal abbreviation	Objective protocol			Reference section
CH1	CH2		Dedicated protocol	Non Procedure protocol	Bidirectional protocol	
Yn0	—	Send request	○ (On-demand)	○	○	Section 6.9 Chapter 7 Section 20.5.1 Chapter 9 to 11 Chapter 12 to 13
Yn1		Receive data read complete	—	○	○	
Yn2		Mode switching request (stop request during processing)	○			Chapter 18
—		(Yn3 to Yn6 are prohibited to use.)	—			—
—	Yn7	Send request	○ (On-demand)	○	○	Section 6.9 Chapter 7 Section 20.5.1 Chapter 9 to 11 Chapter 12 to 13
	Yn8	Receive data read complete	—	○	○	
	Yn9	Mode switching request (stop request during processing)	○			Chapter 18
—		(YnA to YnD are prohibited to use.)	—			—
YnE	—	CH1 ERR. LED OFF request	○			Section 19.1.3
—	YnF	CH2 ERR. LED OFF request				
Y (n+1) 0		Initialization request (standby request)	○			Chapter 21
Y (n+1) 1		Connection request				
Y (n+1) 2		Modem disconnection request				
Y (n+1) 3		(Prohibited to use)				
Y (n+1) 4		Notification-issued request				
—		(Y (n+1) 5 and Y (n+1) 6 are prohibited to use.)				
Y (n+1) 7		EEPROM read request	○			Chapter 16
Y (n+1) 8		EEPROM write request	○			
Y (n+1) 9		EEPROM system parameters write request	○			Chapter 15
—		(Y (n+1) A and Y (n+1) B are prohibited to use.)	—			—
Y (n+1) C		System parameters default request	○			Section 15.3.2
—		(Y (n+1) D to Y (n+1) F are prohibited to use.)	—			—

For *4, see *4 of 1.

*4

IMPORTANT

Of the output signals for the special function modules from the PLC CPU, do not turn on the "Prohibited to use" signal.
If the "Prohibited to use" signal is output, PLC system may result in malfunctions.

3.5 Buffer Memory Applications and Allocation

The term "buffer memory" used in this manual refers to a memory area of the QC24(N) used to store the control and communications data which is sent between an external device and the PLC CPU.

1 **Buffer memory applications**

There are two types of buffer memory area: user area and special applications area.

(a) User area (5888 words area from address 400H to address 1AFFH)

The user area is made up of the following four areas. Do not overlap these areas.

① Non procedure protocol/bidirectional protocol data receive area

This area stores the data received from an external device.

② Non procedure protocol/bidirectional data send area

This area stores the data to be send from the sequence program to an external device.

③ On-demand data storage area

This area stores the data to be sent from the sequence program to an external device using the dedicated protocol on-demand function.

④ Area when using buffer memory read/write commands

This area stores the data when communication is carried using dedicated protocol buffer memory read/write commands.

(b) Special applications area (area from addresses 0H to 3FFH and 1B00H to 1FFFH)

The applications of this memory area are fixed. It is used to determine the data communications format and to change the allocation of the memory area of item (a) above.

One of the following default values is written to the special applications area when the power is turned on or the PLC CPU is reset.

① QC24(N) default values (See table 2.)

② Default values registered to the EEPROM by the user (See User values in Chapter 15.)

The default values can be changed to match the transmission purpose, application, and external device specifications.

POINTS

(1) Special applications area parameters (including parameters changed by the user) can be registered to the QC24(N) EEPROM.
It is recommended that after checking that data communications with the external device is normal, the parameters stored in the special applications area is registered to the QC24(N) EEPROM and used as the default values when the QC24(N) is started.

* Using the parameters registered to the QC24(N) EEPROM as the de-fault values eliminates the need for a sequence program of the default modification part.

(2) See Section 14.1 for a description of the areas that can be registered to the QC24(N) EEPROM and Chapter 15 for a description of registration.

2 Buffer memory allocation tables

The buffer memory consists of 16-bit addresses.

The following tables list the name and default values for each buffer memory address.

(How to read the addresses in the tables and the addresses given in the I/F column)

When associating the parameters of the relevant area with the CH1 and CH2 bidirectional interfaces, the address is entered in the center of the column as described below.

When associating the parameters of the relevant area with the CH1 or CH2 interface, the address is entered at the objective CH side as shown below.

Shows the address of the relevant area by a decimal number.
↓
☐H (☐)
↑
Shows the address of the relevant area by a hexadecimal number.

(Meaning of symbols shown in objective protocol field in the tables.)

A ○ or △ symbol having the following meaning is added to the area used by the related protocol and by setting of QC24(N) control/control method by the user.
A — symbol is added to the system area used by the system or area not used by the relevant protocol.

○ : Area that can be read/written from PLC CPU and external device
△ : Area that can only be read from PLC CPU and external device
— : System area used by the system, or area not used by the relevant protocol

IMPORTANT

Do not write data in the "system area" of the buffer memory.
If data is written in the system area, the PLC system may result in malfunctions.

POINTS

(1) Read/write (default value change, etc.) the buffer memory as described in the description shown in the "Reference Section" column of the table.
(2) The areas of addresses 2EH to 38H and 221H to 23DH in the buffer memory are handled by the QC24N that can use the modem functions shown in Section 1.4.
These areas will become the system area (prohibited to use) with respect to QC24(N)s that do not support modem functions.
(3) The access from PLC CPU is given priority over other special function module processing.
Therefore, if the PLC CPU frequently accesses the buffer memory of a special function module, not only the scan time of the PLC CPU is prolonged but also each processing of the special function module is delayed.
Perform the access to the buffer memory from the PLC CPU using FROM/TO instruction or other means only when it is necessary.
(4) The buffer memory is not backed up by a battery.
When the QC24(N) is started, the QC24(N) default values, or the default values registered to the QC24(N) EEPROM by the user, are written to the special applications area. (See Chapter 15.)

Address and objective I/F		Application	Name		QC24(N) default value	Objective protocol			Reference section
CH1	**CH2**					**Dedicated protocol**	**Non procedure protocol**	**Bidirectional protocol**	
0H(0)		System parameters	LED OFF request (LED No.5 -13)		0	o			Section 19.1.2.
1H(1)			LED OFF request (LED No.16-29)						
2H(2)			EEPROM access	Register/read/delete instruction		o		—	Chapter 16
3H(3)				Frame No. instruction					
4H(4)				Register/read/delete result storage					
5H(5)				Registered data bytes count designation					
6H(6) to 2DH(45)				User-registered frame *40 words					
2EH(46)			Modem functions	Modem connection CH designation	0	o			Chapter 21
2FH(47)				Notification execution designation	0 (Not executed)				
30H(48)				Number of connection retries designation	3				
31H(49)				Connection retries interval designation	180 (sec.)				
32H(50)				Initialization/connection time-out designation	60 (sec.)				
33H(51)				Number of initialization connection retries designation	3				
34H(52)				Data number for initialization designation	2000				
35H(53)				Data number for connection designation	0				
36H(54)				Q6TEL connection designation	0				
37H(55)				No-communication interval time designation	30 (min.)				
38H(56)				RS·CS control/not-control designation	1 (Control)				
39H(57) to 3FH(63)			System area (Prohibited to use)		0	—			—
40H(64)			Y signal·buffer memory timing monitoring designation		0	o			Section 14.12
41H(65) to 7FH(127)			System area (Prohibited to use)		0	—			—
80H(128)			For PLC CPU information clear	PLC CPU information clear request (*2)	0	o	—		Section 19.6
81H(129) to 8FH(143)			System area (Prohibited to use)		0	—			—
90H(144)	130H(304)		Mode Switching	Switching mode No. designation	0 (Switching request disabled)	o			Chapter 18
91H(145)	131H(305)			Switching transmission specifications designation	0				
92H(146)	132H(306)		System area (Prohibited to use)		0	—			—
93H(147)	133H(307)		Transmission control	DTR/DSR, DC control designation	0 (DTR/DSR control)	o			Section 14.3
94H(148)	134H(308)			DC1/DC3 code designation	1311H (11H/13H)				
95H(149)	135H(309)			DC2/DC4 code designation	1412H (12H/14H)				
96H(150)	136H(310)		Word/byte designation (message data length units)		0 (Word units)	o (On-demand	o		Section 14.4
97H(151)	137H(311)		RS-232C CD terminal check designation		1 (No check)	o			Section 4.7.2
98H(152)	138H(312)		RS-232C communication system designation		0 (Full-duplex communications)	o			Section 14.5
99H(153)	139H(313)		Half-duplex communications	Simultaneous transmission priority/ non-priority designation	0 (Priority transmission)	o			
9AH(154)	13AH(314)			Retransmission time transmission method designation	0 (Retransmission disable)				
9BH(155)	13BH(315)		Simultaneously transmission data valid/invalid designation		0 [Send data/receive data valid]	—		o	Section 14.6
9CH(156)	13CH(316)		No-reception monitoring time (timer 0) designation		0H (Unlimited wait)	o			Section 14.7
9DH(157)	13DH(317)		Response monitoring time (timer 1) designation		32h (5 secs)	o	—	o	
9EH(158)	13EH(318)		Transmission monitoring time (timer 2) designation		708h (3 mins)	o	—	o	
9FH(159)	13FH(319)		System area (Prohibited to use)		0	—			—

o: Read/write area △: Read only area —: System area/area not used by relevant protocol.

Address and objective I/F		Application	Name			QC24(N) default value	Objective protocol			Reference section
CH1	CH2						Dedicated protocol	Non procedure protocol	Bidirectional protocol	
A0H(160)	140H(320)	System parameters	On-demand	Buffer memory head address designation		CH1: 400H CH2: 800H	○	—		Section 6.9, Chapter 7
A1H(161)	141H(321)			Data length designation		0				
A2H(162)	142H(322)		Communication parameters	Send buffer memory head address designation		CH1: 400H CH2: 800H	—	○		Section 14.8
A3H(163)	143H(323)			Send buffer memory length designation		200H				
A4H(164)	144H(324)			Received data count designation		1FFH	—	○	—	
A5H(165)	145H(325)			Receive complete code designation		0D0AH (CR, LF)				
A6H(166)	146H(326)			Receive buffer memory head address designation		CH1: 600H CH2: A00H	—	○		
A7H(167)	147H(327)			Receive buffer memory length designation		200H				
A8H(168)	148H(328)			Receive data clear request		0 (Clear request disable)	—	○	—	Section 9.3.4
A9H(169)	149H(329)		On-demand user frame designation	First frame No. designation	(1st)	0 (None)	○	—		Chapter 7
AAH(170)	14AH(330)				(2nd)					
ABH(171)	14BH(331)			Last frame No. designation	(1st)	0 (None)				
ACH(172)	14CH(332)				(2nd)					
ADH(173)	14DH(333)		Receive user frame designation	User frame use enable/disable designation		0 (Use disable)	—	○	—	Section 14.9
AEH(174)	14EH(334)			First frame No. designation	(1st)	0 (None)				
AFH(175)	14FH(335)				(2nd)					
B0H(176)	150H(336)				(3rd)					
B1H(177)	151H(337)				(4th)					
B2H(178)	152H(338)			Last frame No. designation	(1st)	0DH				
B3H(179)	153H(339)				(2nd)	0AH				
B4H(180)	154H(340)				(3rd)	0 (None)				
B5H(181)	155H(341)				(4th)					
B6H(182)	156H(342)		Transmission user frame designation	User frame being transmitted		0 (Transmission disable)	—	○	—	Section 9.6.2 Chapter 11
B7H(183)	157H(343)			Schedule designatilon	CR/LF output designation	0 (Output disable)				
B8H(184)	158H(344)				Output head pointer designation	0 (Output not designated)				
B9H(185)	159H(345)				Output count designation	0 (None)				
BAH(186)	15AH(346)			Output frame No. designation	(1st)	0 (None)				
BBH(187) to 11DH(285)	15BH(347) to 1BDH(445)				(2nd) to (100th)	0 (None)				
11EH(286)	1BEH(446)		Message wait time designation (Used in transmission of other than A compatible frames)			0 (No wait time)	○	—		Section 14.7.4
11FH(287)	1BFH(447)		Send transparent code designation			0 (None)	—	○		Section 14.10
120H(288)	1C0H(448)		Receive transparent code designation			0 (None)				
121H(289)	1C1H(449)		ASCII-BIN conversion designation			0 (Non convert)				Section 14.11
122H(290) to 12FH(303)	1C2H(450) to 1FFH(511)		System area (Prohibited to use)			0	—			—

○: Read/write area △: Read only area —: System area/area not used by relevant protocol

Address and objective I/F		Applica-tion	Name			QC24(N) default value	Objective protocol			Reference section
CH1	CH2						Dedicated protocol	Non proce-dure protocol	Bidirectional protocol	
200H(512)		System data	Station No. setting switch setting status storage			(Switch setting No.)	△			Section 19.4
201H(513)			LED ON status storage (LED No.5-13)			[According to the status of the module]				Section 19.1
202H(514)			LED ON status storage (LED No.16-29)							
203H(515)			Switch setting error, mode switching error storage			0 (No errors)				Section 19.1.3 Section19.4 Section19.5
204H(516)			EEPROM access	Number of registered user registration frames storage		0 [Not registered. However, according to registration status after registration.]	△		—	Chapter 16
205H(517) to 21DH(541)				User registration frame registered status storage (for registration No. check)						
21EH(542)			Number of registered default registration frames storage (OS ROM)			(Actual number of registration)				
21FH(543)			Number of EEPROM writes [*1] 0 to 1000 : Number of writes			0	○			—
220H(544)			EEPROM system parameters write result storage			0	△			Chapter 15
221H(545)		Modem function	Modem function error code storage			0	○			Chapter 21
222H(546)			Modem function sequence status storage			0				
223H(547)			EEPROM access	Number of registered connection data storage		0 (No registration)				
224H(548)				Connection data registration status storage		0				
225H(549)										
226H(550)				Number of registered initial data storage		0 (No registration)				
227H(551)				Initial data registration status storage		0				
228H(552)										
229H(553)			Number of notification execution storage			0	— (Read only)			
22AH(554)			Notification execution data storage	Data 1	Notification execution data No.	0				
22BH(555)					System area (Prohibited to use)	0				
22CH(556)						0				
22DH(557)						0				
22EH(558)				Data 2	Notification execution data No.	0				
22FH(559)					System area (Prohibited to use)	0				
230H(560)						0				
231H(561)						0				
to				to						
23AH(570)				Data 5	Notification execution data No.	0				
23BH(571)					System area (Prohibited to use)	0				
23CH(572)						0				
23DH(573)						0				
23E(574) to 24FH(591)		System data	System area (prochibited to use)			0	—			—
250H(592)	260H(608)		Mode setting switch setting status storage			[According to switch setting]	△			Section 19.4
251H(593)	261H(609)		Transmission specifications switch setting status storage							
252H(594)	262H(610)		Mode setting status storage	Current setting						Section 19.4 Section 19.5
253H(595)	263H(611)		Transmission specifications setting status storage							
254H(596)	264H(612)		RS-232C control signal status storage			(According to signal status)				Section 19.2
255H(597)	265H(613)		Transmission sequence status storage			0 (Send/receive wait)				Section 19.3
256H(598)	266H(614)		On-demand execution result storage			0 (Normal end)	○	—		Section 6.9, Chapter 7
257H(599)	267H(615)		Data transmission result storage			0 (No errors)	○			Section 19.1.3
258H(600)	268H(616)		Data reception result storage							
259H(601)	269H(617)		System area (Prohibited to use)			0	—			
25AH(602)	26AH(618)		Dedicated protocol transmission error code storage			0 (No errors)	○	—		
25BH(603)	26BH(619)		Receive user frame storage (⬚ th)			0 (Not received)	—	△	—	Chapter 11
25CH(604) to 25FH(607)	26CH(620) to 3FFH(1023)		System area (Prohibited to use)			0	—			—

○: Read/write area △: Read only area —: System area/area not used by relevant protocol

Address and objective I/F		Application	Name		QC24(N) default value	Objective protocol			Reference section
CH1	CH2					Dedicated protocol	Non procedure protocol	Bidirectional protocol	
400H(1024)		Default CH1 send/ receive buffer memory	Send area	Send data count designation	0	○ (On-demand)	○		Section 9.3.2 Section 9.4.1 Section 12.3.2 Section12.4.1
401H(1025) to 5FFH(1535)				Send data designation *511 words	0				
600H(1536)			Receive area	Receive data count storage (read data count)	0				
601H(1537) to 7FFH(2047)				Receive data storage *511 words	0				
800H(2048)		Default CH2 send/ receive buffer memory	Send area	Send data count designation	0	○ (On-demand)	○		
801H(2049) to 9FFH(2559)				Send data designation *511 words	0				
A00H(2560)			Receive area	Receive data count storage (read data count)	0				
A01H(2561) to BFFH(3071)				Receive data storage *511 words	0				
C00H(3072) to 1AFFH(6911)		User	User area *3840 words		0	○			Section 6.3 Section 6.9 Section 14.8
1B00H(6912)		User frame registration [Amount registered to buffer memory]	Registration No. 8001H	Registered data bytes count designation	0	○		—	Chapter 16 Section 21.4.5 Section 21.4.6
1B01H(6913) to 1B28H(6952)				User frame designation *40 words	0				
1B29H(6953)			Registration No. 8002H	Registered data bytes count designation	0				
1B2AH(6954) to 1B51H(6993)				User frame designation *40 words	0				
1B52H(6994) to 1FCDH(8141)			⋮						
1FCEH(8142)			Registration No. 801FH	Registered data bytes count designation	0				
1FCFH(8143) to 1FF6H(8182)				User frame designation *40 words	0				
1FF7H(8183) to 1FFFH(8191)		—	System area (Prohibited to use)		0	—			—

○: Read/write area △: Read only area —: System area/area not used by relevant protocol

*1 Available with A1SJ71QC24N1(-R2) only. (system area (prohibited to use) for other modules)

*2 Available only for the A1SJ71QC24N1(-R2) of software version B or later.
(Assigned to System area (Prohibited to use) for other modules)

4. SETTINGS AND PROCEDURES BEFORE OPERATION

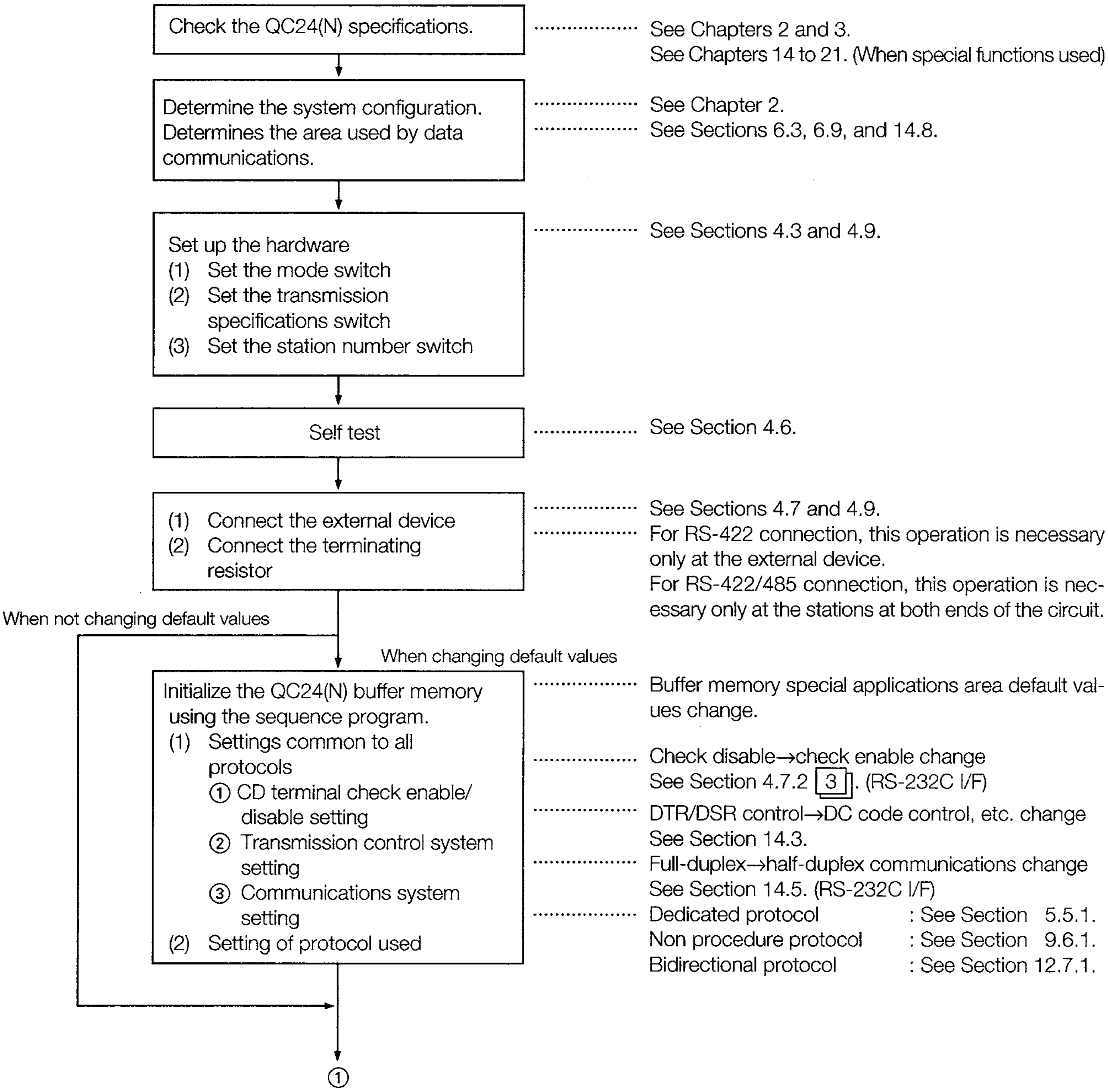
4.1 Procedures Before Operation

The following describes the settings and procedures that must be carried out before a system using the QC24(N) can be started.

POINT

(1) For the procedure summary up to operation when the QC24N modem functions (see Section 1.4 for the QC24N models that support the modem functions) are used, refer to Section 21.4.

(2) Be sure to read through the Safety Precautions in the beginning of this manual prior to QC24(N) startup.



Check the QC24(N) specifications. ………… See Chapters 2 and 3.
See Chapters 14 to 21. (When special functions used)

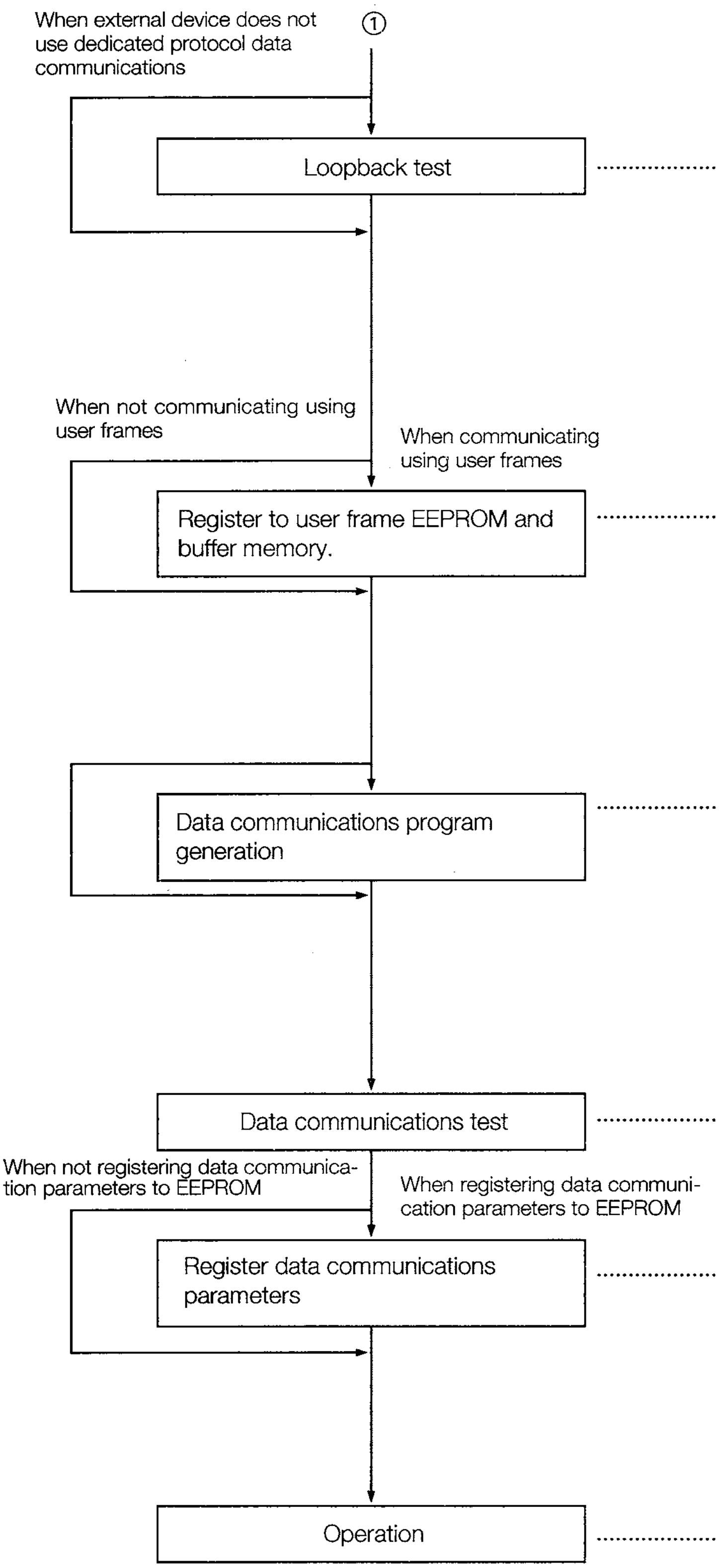
Determine the system configuration. ………… See Chapter 2.
Determines the area used by data communications. ………… See Sections 6.3, 6.9, and 14.8.

Set up the hardware ………… See Sections 4.3 and 4.9.
(1) Set the mode switch
(2) Set the transmission specifications switch
(3) Set the station number switch

Self test ………… See Section 4.6.

(1) Connect the external device ………… See Sections 4.7 and 4.9.
(2) Connect the terminating resistor ………… For RS-422 connection, this operation is necessary only at the external device.
For RS-422/485 connection, this operation is necessary only at the stations at both ends of the circuit.

Initialize the QC24(N) buffer memory using the sequence program. ………… Buffer memory special applications area default values change.
(1) Settings common to all protocols
① CD terminal check enable/disable setting ………… Check disable→check enable change
See Section 4.7.2 [3]. (RS-232C I/F)
② Transmission control system setting ………… DTR/DSR control→DC code control, etc. change
See Section 14.3.
③ Communications system setting ………… Full-duplex→half-duplex communications change
See Section 14.5. (RS-232C I/F)
(2) Setting of protocol used ………… Dedicated protocol : See Section 5.5.1.
Non procedure protocol : See Section 9.6.1.
Bidirectional protocol : See Section 12.7.1.



If dedicated protocol data communications is possible, carry out this test.
See Section 4.8.1.
See the next page for a detailed description of the commands.

- ASCII mode command (TT)
  See Section 5.16 of the Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function).
- Binary mode command (0619)
  See Section 6.13 of this manual.

Register when using the following functions:

- On-demand data transmission (dedicated protocol)....See Chapter 7.
- User data send/receive (non procedure protocol) ... See Chapter 11.

See Chapter 16 for a description of the user frame registration method.

A communications sequence program is necessary when the following functions are used. (PLC CPU side)

- Non procedure protocol/bidirectional protocol data communications
- Data transmission using dedicated protocol on-demand function
- Signal input using dedicated protocol global function

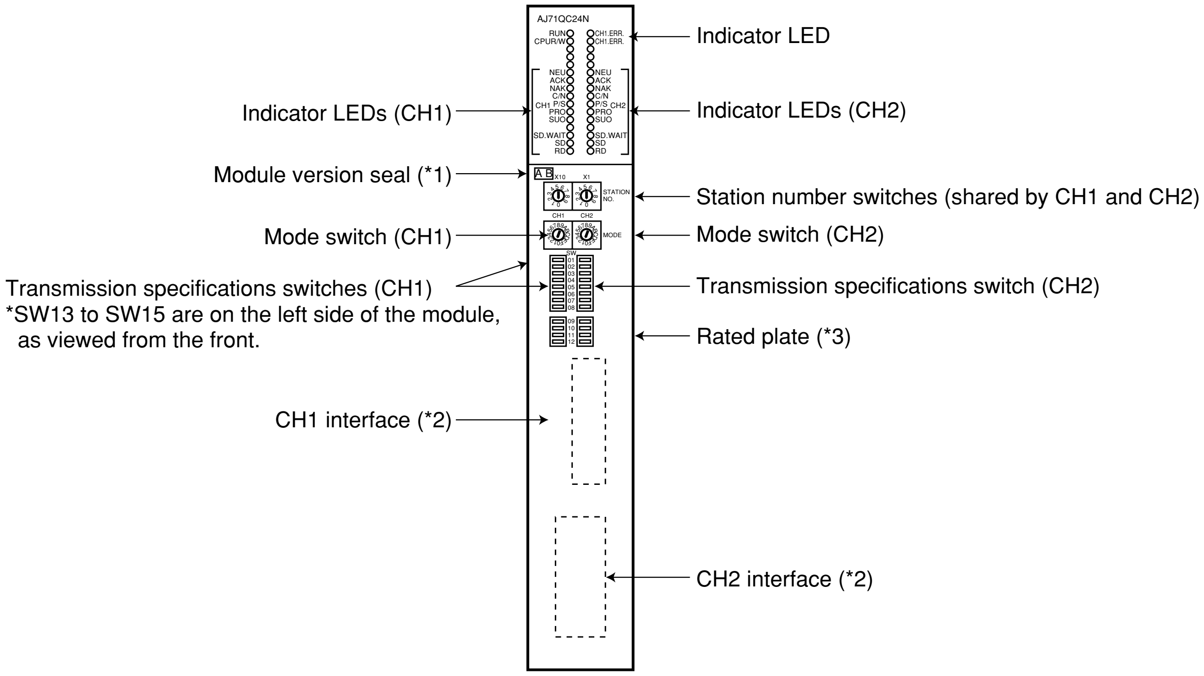
When data cannot be sent and received normally, review the set and registered values and programs.
See Chapter 22.

By registering the data communications parameters to EEPROM, the parameters can be used as the default value during QC24(N) starting. Do this when the results of the data communications test above were normal.
(When the default value are not changed, this operation is unnecessary.)
See Chapter 15.

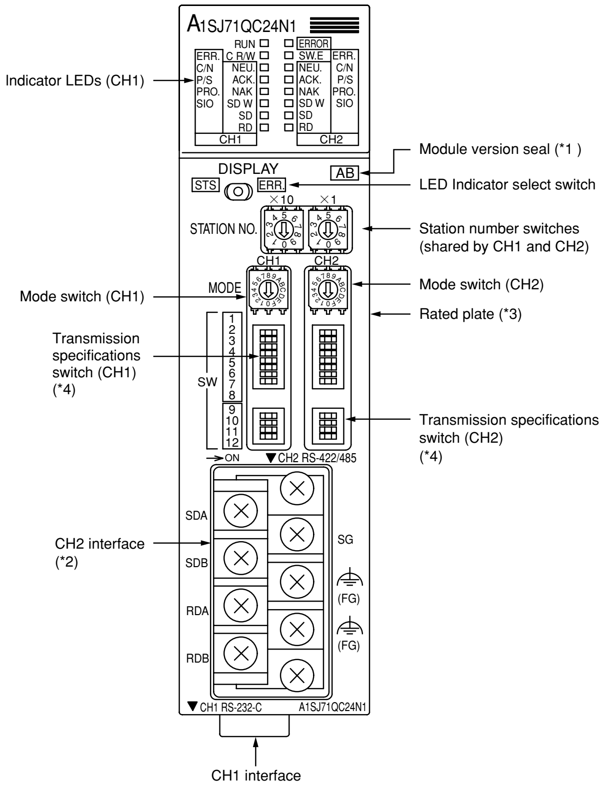
See the dedicated protocol, non procedure protocol, or bidirectional protocol section.
When switching the mode of each interface after starting operation, see Chapter 18.

4.2 Names of Parts

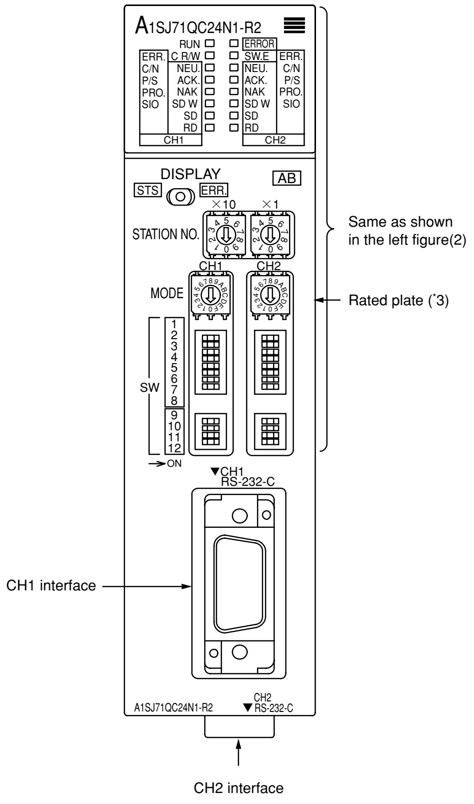
(1) AJ71QC24, AJ71QC24-R2, AJ71QC24-R4
AJ71QC24N, AJ71QC24N-R2, AJ71QC24N-R4



(2) A1SJ71QC24, A1SJ71QC24N, A1SJ71QC24N1

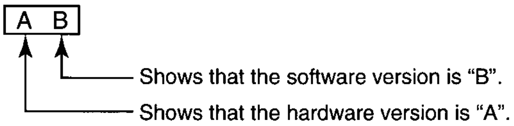


(3) A1SJ71QC24-R2, A1SJ71QC24N-R2, A1SJ71QC24N1-R2



*1 Seal showing the module hardware version and software version.

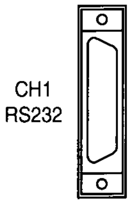
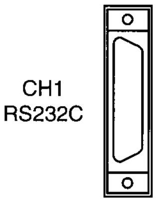
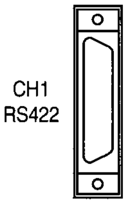
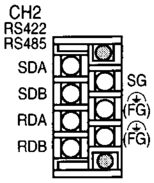
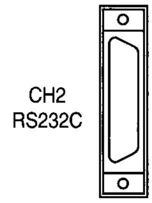
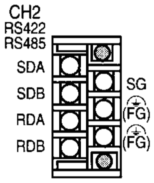
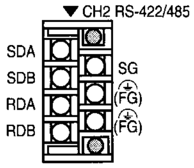
(Example)



Shows that the software version is "B".

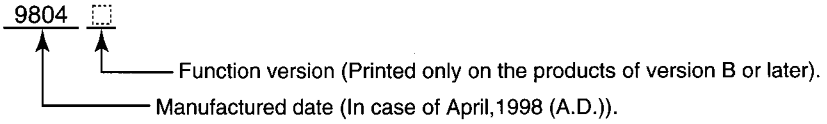
Shows that the hardware version is "A".

*2 The interfaces of each QC24(N) are shown below.

Objective CH	AJ71QC24 AJ71QC24N	AJ71QC24-R2 AJ71QC24N-R2	AJ71QC24-R4 AJ71QC24N-R4	A1SJ71QC24 A1SJ71QC24N A1SJ71QC24N1	A1SJ71QC24-R2 A1SJ71QC24N-R2 A1SJ71QC24N1-R2
CH1	(RS-232C)  (D-sub 25-pin)	(RS-232C)  (D-sub 25-pin)	(RS-422)  (D-sub 25-pin)	(RS-232C)  (D-sub 9-pin)	(RS-232C)  (D-sub 9-pin)
CH2	(RS-422/485)  (2 peaces terminal block)	(RS-232C)  (D-sub 25-pin)	(RS-422/485)  (2 peaces terminal block)	(RS-422/485)  (2 peaces terminal block)	(RS-232C)  (D-sub 9-pin)

- All connectors are D sub (female) screw fastening type.
- The two-piece terminal block in the above diagram is for QC24N.
  In the case of QC24, the FG marking on the two-piece terminal block will be FG on the top and NC at the bottom.

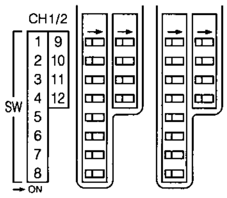
*3 The date column in the rated plate displays the manufactured date and function version of the module.



Function version (Printed only on the products of version B or later).

Manufactured date (In case of April,1998 (A.D.)).

*4 Below is the switch of modules with the following hardware versions.
The switch layout differs from the conventional module, but the setting function of each switch and direction of ON/OFF remain the same.



Applicable module	Hardware version
A1SJ71QC24	Version E or earlier
A1SJ71QC24-R2	Version D or earlier
A1SJ71QC24N	Version A
A1SJ71QC24N-R2	Version A

4.3 Switch Settings

This section describes the QC24(N) switch settings needed to ex-change data with external devices. Set the switches according to the interface and functions of the QC24(N) used.

POINTS

(1) When the setting of the switches described in this section have been changed, turn the PLC CPU power OFF→ON, or reset the PLC CPU.

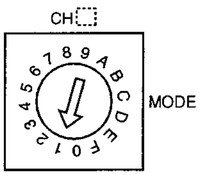
(2) When a QnACPU GPP function peripheral device is connected to the QC24(N) CH1 interface (RS-232C/RS-422) and GPP operation is performed, set the switches as described in Section 4.9.

(3) This section describes all the switches of all serial communication modules.
Ignore the description of settings that do not depend on the module used.

(4) When there is a switch setting error both of the interfaces can no longer be used. In addition, an error code will be stored in the QC24(N) buffer memory (address 203H) and the display LED SW ERR. and the applicable interface CH□ ERR. will light up.
See Section 19.1.3 for a description of how to read the error code and Section 22.1 for the description of the error codes.

4.3.1 Mode switch setting

Set the mode of each interface according to the data communications function with the external device used. Set the mode switch of interfaces without external device connected to any number from [1] through [7].

Mode switch details	Mode switch No.	Setting contents			Notes
 *1	0	When CH1 and CH2 operation is linked: Mode No. set at CH1 When CH1 and CH2 operate indepen-dently: Setting impossible.			Set to CH1 side when linking CH1 and CH2. Data can be exchanged using the CH2 mode setting number function. (Mode No.1=6) When CH1 and CH2 operate independently, setting is impossible.
	1	Dedicated protocol	ASCII mode	Format 1	ASCII mode A compatible frame, QnA frame, QnA extension frame, and QnA simplified frame messages can be transferred. When the system configuration is m:n, format 3 cannot be set.
	2			Format 2	
	3			Format 3	
	4			Format 4	
	5		Binary mode	Format 5	Binary mode QnA extension frame messages can be transferred. When the system configuration is m:n, format 5 cannot be set.
	6	Non procedure protocol			Data communications with user frames is also possible.
	7	Bidirectional protocol			————————
	8 to D	Setting impossible			————————
	E	ROM/RAM switch test			Set when checking the QC24(N) memory and switch settings.
	F	Self loopback test			Set when checking the QC24(N) communica-tions function.

(Factory setting: "1")

*1 The mode switch setting status can be checked with the QC24(N) buffer memory (addresses 250H, 260H). See Section 19.4.

Note

The following shows the relationship between the mode number set with the mode switch and the available QC24(N) functions.

1 **RS-232C, RS-422 interface**

○: Available ×: Unavailable

Function		Dedicated protocol		Non procedure protocol	Bidirectional protocol	Self test
		ASCII	Binary			
		1 to 4	5	6	7	E to F
Dedicated protocol	Communications using ASCII mode frames	○	×	×	×	×
	Communications using binary mode frames	×	○	×	×	×
	On-demand transmission using user frames	○	○	×	×	×
	Access to another station through the QC24(N) using QnACPU link dedicated instruction	○	○	×	×	×
	Access through the QC24(N) using the QnACPU GPP function	×	○	×	×	×
Non procedure protocol	Transmission from PLC CPU to external device	×	×	○	×	×
	Reception from external device to PLC CPU	×	×	○	×	×
	Communication using user frames	×	×	○	×	×
Bidirectional protocol	Transmission from PLC CPU to external device	×	×	×	○	×
	Reception from external device to PLC CPU	×	×	×	○	×
EEPROM access	Registration of buffer memory user special applications area parameters	○	○	○*	○*	×
	Registration of user frames for each protocol	○	○	○*	○*	×
Transmission control		○	○	○	○	×
Half-duplex communications setting (RS-232C only) Communications with the modem function (RS-232C only)		○	○	○	○	×
Data communications when external device and PLC CPU configuration is m:n		×	×	×	×	×
Mode switching		○	○	○*	○*	×
QC24(N) operation check (self test)		×	×	×	×	○

*: Available only from PLC CPU

2 **RS-422/485 interface**

○: Available ×: Unavailable

Function		Dedicated protocol		Non procedure protocol	Bidirectional protocol	Self test
		ASCII	Binary			
		1 to 4	5	6	7	E to F
Dedicated protocol	Communications using ASCII mode frames	○	×	×	×	×
	Communications using binary mode frames	×	○	×	×	×
	On-demand transmission using user frames	○	○	×	×	×
	Access to another station through the QC24(N) using QnACPU link dedicated instruction	○	○	×	×	×
	Access through the QC24(N) using the QnACPU GPP function	×	○	×	×	×
Non procedure protocol	Transmission from PLC CPU to external device	×	×	○	×	×
	Reception from external device to PLC CPU	×	×	○	×	×
	Communication using user frames	×	×	○	×	×
Bidirectional protocol	Transmission from PLC CPU to external device	×	×	×	○	×
	Reception from external device to PLC CPU	×	×	×	○	×
EEPROM access	Registration of buffer memory user special applications area parameters	○	○	○*	○*	×
	Registration of user frames for each protocol	○	○	○*	○*	×
Transmission control		○	○	○	○	×
Half-duplex communications setting Communications with the modem function		×	×	×	×	×
Data communications when external device and PLC CPU configuration is m:n		○	×	×	×	×
Mode switching		○	○	○*	○*	×
QC24(N) operation check (self test)		×	×	×	×	○

*: Available only from PLC CPU

*2 The following shows the linked operation settings and data flow.

(1) Mode switch number [0] is the number that is set in the CH1 mode switch when the two QC24(N) interfaces are linked.

Since the two QC24(N) interfaces cannot be linked in the following cases, do not set [0].

① When the module is the AJ71QC24(N)-R2, A1SJ71QC24(N)-R2.

② When an external device is connected to one of the QC24(N) interfaces.

③ When transferring data using the bidirectional protocol. (CH2 mode switch set to [7].)

④ When the two QC24(N) interfaces are not related and data is transferred with an external device connected to each interface using the function (dedicated protocol/non procedure protocol) set in the mode switches.

⑤ When communicating data using the modem function.

(2) When linking the two QC24(N) interfaces, set the related switches as shown below.

Switch name	CH1	CH2	Notes
Mode switch	0	1 to 6	Set the number of the function used with CH2.
Operation switch	SW01=OFF	SW01=ON	—
Data bits setting to Transmission rate setting	SW02=□ to SW12=□	SW02=□ to SW12=□	Set CH1 and CH2 to the same specifications. Set SW13 to SW15 to OFF.
Station number switch	X10=□ X1=□		Set according to Section 4.3.3.

* Set the data bit setting~write during RUN enable/disable switches to match the specifications of the opposite device.

POINTS

(1) There is no linked operation setting to the QC24(N) buffer memory special applications area. Write the parameters to the interface (CH□) according to the description of the function used.

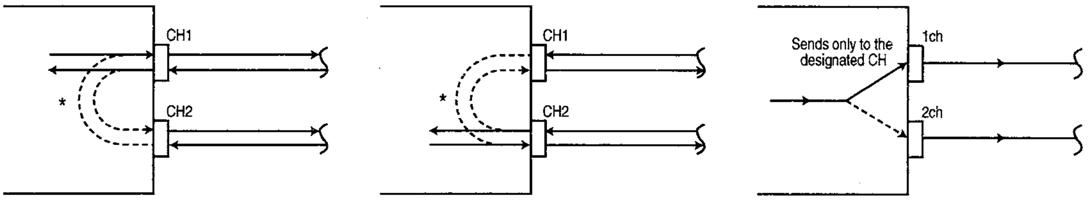
(2) When the following QC24(N) is used and the two interfaces are linked (see Section 4.3.1 *2), the one-character transmission time becomes the QC24(N) H/W gate OFF time.

- AJ71QC24 AJ71QC24N
- AJ71QC24-R4 AJ71QC24N-R4
- A1SJ71QC24 A1SJ71QC24N A1SJ71QC24N1

(3) The following describes the linked operation data flow.

The two linked interfaces operate using the function set in the CH2 mode switch (dedicated protocol (same format) or non procedure protocol) and transmission specifications (CH1 and CH2 must be set as the same specification) set in the transmission specifications switch.

QC24(N) (linked operation data flow)



* A QC24(N) set for linked operation sends all the data received from one interface from the other interface.

In this case, when data communications uses the non procedure protocol, all the connected QC24(N)s receive the data and exclusive control of the receive data is necessary. When data communications uses a dedicated protocol, only the QC24(N) of the station number designated in the message performs the processing designated by command. For data communication using a dedicated protocol QnA (extension) frame, or QnA simplified frame linked operation header data (shown below) is added to messages addressed to other multidrop stations.

① Processing of QC24(N) of station connected to external device
- Adds header data to command messages addressed to another station received from an external device and sends the message from the other interface.
- Deletes the hardware data from the response message received from the other station and sends a response message to the external device through the other interface. (m:n connection: Also sends the header data)

② Operation of accessed station
- Processes the request contents of the command message and adds header data to the response message and sends the response message from the interface that received the command message.

Notes

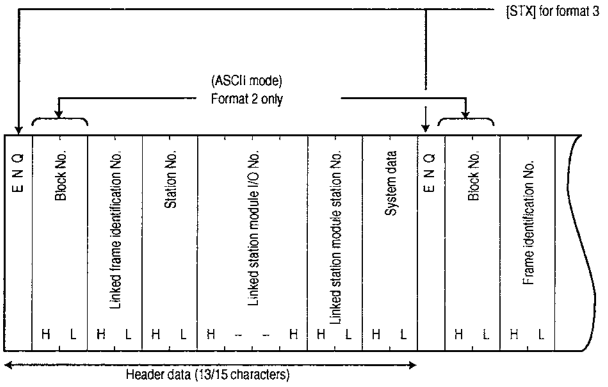
The QC24(N) adds the following linked operation header data to a message.

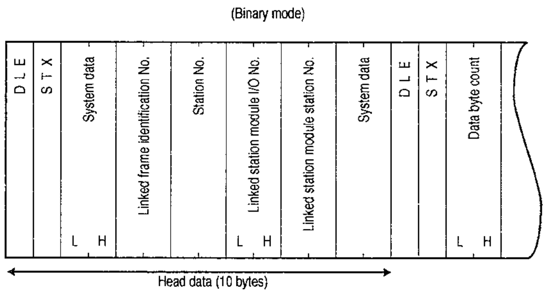
① Communications in ASCII mode (Formats 1 to 4)

The QC24 adds the following 13/15 characters header data immediately before the control code (ENQ/STX/ACK/NAK) at the head of each message. (Format 1· 3 to 4: 13 characters, format 2: 15 characters)

② Communications in binary mode (Format 5)

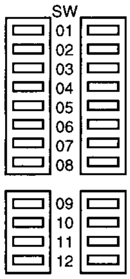
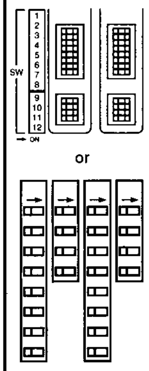
The QC24 adds the following 10 bytes of header data immediately before the control code (DLE+STX) at the head of each message.





4.3.2 Transmission specifications switch setting

Set the switches that depend on the QC24(N) used as described below.

<table>
<tr><th rowspan="2">Switch details</th><th colspan="2">Switch</th><th rowspan="2">Setting item</th><th colspan="2">Switch state (*1)</th><th rowspan="2">Notes</th></tr>
<tr><th>CH1</th><th>CH2</th><th>OFF</th><th>ON</th></tr>
<tr><td rowspan="10">Large-type QC24(N)

Small-type QC24(N)

See Section 4.2 *4</td><td colspan="2">SW01</td><td>Operation setting</td><td>Independent operation</td><td>Linked operation</td><td>Always set CH1 to OFF. Set only CH2 to ON/OFF.</td></tr>
<tr><td colspan="2">SW02</td><td>Data bits setting</td><td>7 bits</td><td>8 bits</td><td>Parity bit not included.</td></tr>
<tr><td colspan="2">SW03</td><td>Parity bit enable/ disable setting</td><td>Disable</td><td>Enable</td><td>When set to Enable, the setting of SW04 is effective.</td></tr>
<tr><td colspan="2">SW04</td><td>Even parity/ odd parity setting</td><td>Odd</td><td>Even</td><td>Effective only when Parity Bit Enable is selected.</td></tr>
<tr><td colspan="2">SW05</td><td>Stop bit setting</td><td>1 bit</td><td>2 bits</td><td>—</td></tr>
<tr><td colspan="2">SW06</td><td>Sum check enable/ disable setting</td><td>Disable</td><td>Enable</td><td>Dedicated protocol, bidirectional protocol</td></tr>
<tr><td colspan="2">SW07</td><td>Write during RUN enable/disable setting</td><td>Disable</td><td>Enable</td><td>Dedicated protocol</td></tr>
<tr><td colspan="2">SW08</td><td>Setting change enable/disable</td><td>Disable (prohibit)</td><td>Enable (allow)</td><td>Sets mode switching and EEPROM write allow/prohibit.</td></tr>
<tr><td colspan="2">SW09
to
SW12</td><td colspan="3"><table>
<tr><th>Transmission rate (bps)</th><th>300</th><th>600</th><th>1200</th><th>2400</th><th>4800</th><th>9600</th><th>19200</th></tr>
<tr><td>SW09</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td></tr>
<tr><td>SW10</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>ON</td></tr>
<tr><td>SW11</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>ON</td></tr>
<tr><td>SW12</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
</table>Transmission rate setting (*2)</td><td>The settings to the left is for QC24. QC24N should be set as *2 indicated below. Settings other than indicated are not possible.</td></tr>
<tr><td colspan="2">SW13
to
SW15</td><td>—</td><td colspan="2">(Set to all OFF.)</td><td>These switches are on the left side of the module, as viewed from the front. (Large-type QC24 Only)</td></tr>
</table>

(Factory settings are all OFF.)

*1 The QC24 buffer memory (address 251H, 261H) can be used to check the setting status of transmission specifications switches SW01 to SW12. See Section 19.4.

*2 For QC24N, either of the following settings should be made. (When two interfaces are used, the total of CH1 and CH2 should be within 115,200 bps. (For A1SJ71QC24N1(-R2), the transmission rate is within 230400 bps))

<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="12">Transmission speed (Units : bps)</th></tr>
<tr><th>300</th><th>600</th><th>1200</th><th>2400</th><th>4800</th><th>9600</th><th>19200</th><th>38400</th><th>14400</th><th>28800</th><th>57600</th><th>115200</th></tr>
<tr><td rowspan="4">Switch</td><td>SW09</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td></tr>
<tr><td>SW10</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td></tr>
<tr><td>SW11</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td>SW12</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>ON</td></tr>
</table>

POINT

The names of the CH1 and CH2 transmission specifications switches (SW n1 n2) are the same. Check the objective interface before setting the switches.

1 Operation setting

① Set if the QC24(N) interfaces are linked or are operated independently when an external device is connected to the two QC24(N) interfaces.

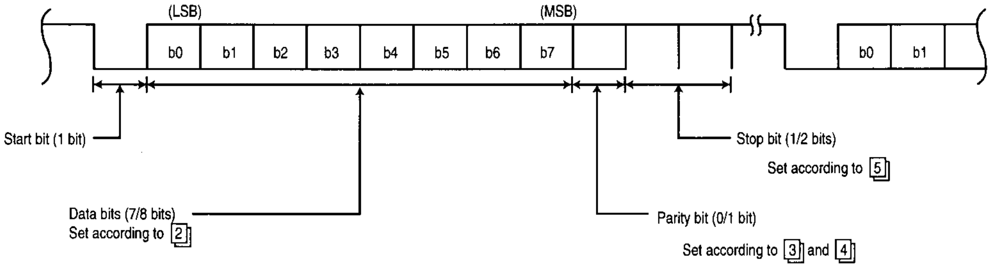
② To link the two interfaces, set the two QC24(N) interfaces to the same transmission specifications by setting the switches as described in Section 4.3.1 *2. (Only set the CH2 operation switch to ON.)

2 Data bits setting

① Set the bit length of one byte of data transferred with the opposite device to match the specifications of the opposite device. (When data is transferred in the dedicated protocol binary mode and when the sum check code is handled in the bidirectional mode, 8 bits must be set.)

② If 7 bits are set, the data is communicated by ignoring the most significant bit (8th bit).

③ The parity bit is not included.



3 Parity bit enable/disable setting

① Set whether or not a parity bit (vertical parity) is added to each byte of data transferred with the opposite device to match the specifications of the opposite device.

② When parity bit is enabled, the QC24(N) adds the parity bit to the data sent from the QC24(N). The QC24(N) checks and removes the parity bit from the received data.

4 Odd parity/even parity setting

Set whether the parity is made odd parity or even parity to match the specifications of the opposite device when a parity bit is added by the parity bit enable/disable setting of 3 above.

5 Stop bit setting

Set the bit length that delimits each byte of data transferred with the opposite device to match the specifications of the opposite station.

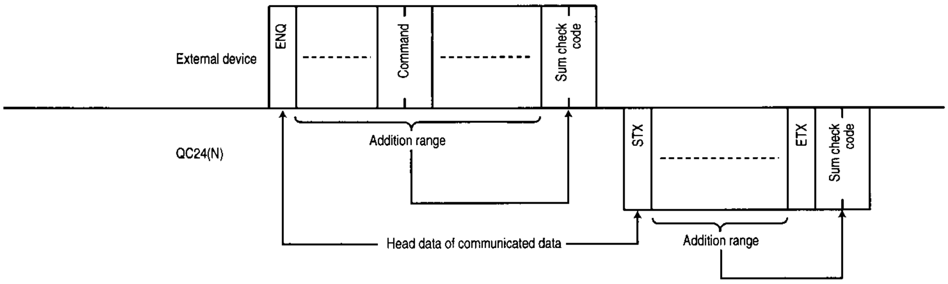
6 Sum check enable/disable setting

① Set whether or not a sum check code is added to the send message and receive message of each frame and each format during dedicated protocol and bidirectional protocol data communications to match the specifications of the opposite device. (This setting is ignored during communications using a user frame that handles the trailer frame.)

② The sum check code is generated by converting the value of the lower byte of the result (sum) of adding a fixed range of messages to a 2-digit hexadecimal ASCII code to increase message reliability.

③ Sections 6.1 and 13.1 describe the system configuration and sum check code when a sum check code is added.

(Dedicated protocol QnA frame (format 1) communications)



7 Write during RUN enable/disable setting

① Set whether or not the write operation is executed even while the PLC CPU is running to match the system specifications when data is written to the PLC CPU from an external device using a dedicated protocol.

② When write during RUN is enabled, when an external device requests writing of data to the PLC CPU while the PLC CPU is running, the PLC CPU returns an NAK message without writing the data.

③ Check the [Write enable setting] and [Write disable setting] columns of the table shown in Section 5.4 for the QC24(N) functions that can be used by this setting.

8 Setting change enable/disable setting

Set whether or not the following processing performed from the PLC CPU and external device is allowed after the QC24(N) starts. To perform the following processing from an external device, set SW08 of the connected interface to ON. To perform the following processing from the PLC CPU, set SW08 of the CH1 and CH2 inter-faces to ON.

- QC24(N) interfaces data communications function, transmission specifications change (mode switching)
- Writing of data (parameters, user frame at QC24(N) restarting) to the EEPROM in the QC24(N)

9 Transmission rate setting

① Set the data transmission rate when transferring data with the opposite device.

② Set maximum transmission rate shown in the table below according to the type and communications system of the QC24(N) used.

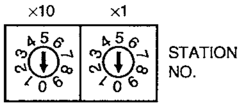
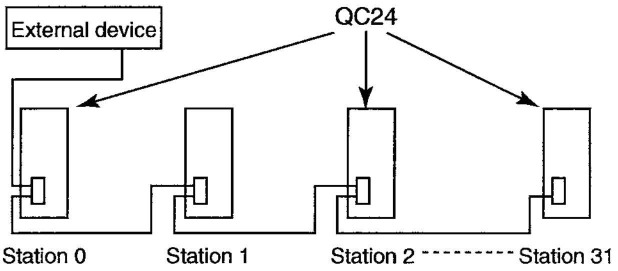
Model	——	Settable maximum transmission rate (Units: bps)	
		Full-duplex	**Half-duplex**
AJ71QC24(N)	CH1	QC24 : 300 to 19,200 for each of CH1 and CH2 (*1) QC24N : 300 to 115200 (*2)	
	CH2		
AJ71QC24(N)-R2	CH1		
	CH2		
A1SJ71QC24(N)	CH1	QC24 : 300 to 19,200 for each of CH1 and CH2 QC24N : 300 to 115200 (*2)	
	CH2		
A1SJ71QC24(N)-R2	CH1		
	CH2		
AJ71QC24(N)-R4	CH1	QC24 : 300 to 19,200 for each of CH1 and CH2 (*1) QC24N : 300 to 115200 (*2)	Half-duplex communications is not available.
	CH2		

*1 When using the QC24 software version of "Version L" or earlier and connecting an external device to each of the two interfaces, set the total transmission speed of the two interfaces to within 19200bps. When an external device is connected to either interface only, the transmission speed of the connected interface can be set to a maximum of 19200bps. In this case, set the transmission speed of the interface, to which an external device is not connected, to 300bps.

*2 When external devices are connected to both of QC24N's interfaces, the total transmission speed for both interfaces must be set no faster than 115,200 bps. (For A1SJ71QC24N1(-R2), the transmission rate is within 230400 bps)
When the external device is connected to only one interface, set the connected interface at no more than of 115,200 bps. Set the unconnected interface at 300 bps.

4.3.3 Station number switch setting

The "station number" is a number for determining the QC24(N) an external device can access during dedicated protocols data communications.

Station switch details	Description
 (Large-type QC24(N))	(1) Station number is set from 0 to 31. (Do not set a station number over 31.) (2) ×10 sets the station number + digit. (3) ×1 sets the station number - digit. (4) Set this switch so that the station numbers are not duplicated within the 0 to 31 range. Not necessary to set the station numbers in connect order. Station numbers can also be skipped. (5) Station number setting example 

(The factory setting is [00].)

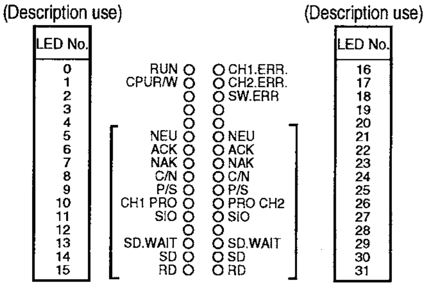
*1 The QC24(N) buffer memory (address 200H) can be used to check the status of the station number switch. See Section 19.4.

POINT

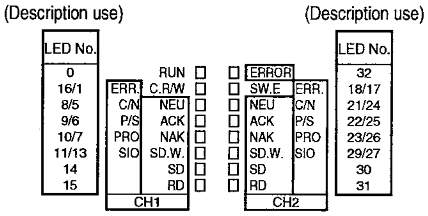
Set the station number switch so that the same number is not set at two or more places. Such setting will destroy the communication data and generate an error.

4.4 LED Display

Large-type QC24 (N)



Small-type QC24 (N)



LED No.		LED name	Meaning of LED display	LED ON (ON/BLINK)	LED OFF (OFF)	Initial status of LED	Related protocol		
CH1	CH2						Dedicated	Non procedure	Bidirectional
0		RUN	Normal operation	Normal	Abnormal	ON	○		
1		CPUR/W	Communicating with PLC	Blinks during PLC communications (when not communicating is OFF)		OFF			
2 to 4	19 to 20	—	(Not used during data communications.)	—	—	OFF	—		
5	21	NEU.	CH□ neutral status	Transmission sequence initial status (Waiting to receive command messages)	Command message receive completed	*1	○	—	
6	22	ACK.	CH□ [normal end] transmission	After [Normal End] transmitted	After [Abnormal End] transmitted	OFF			
7	23	NAK	CH□ [Abnormal End] transmission	After [Abnormal End] transmitted	After [Normal End] transmitted	OFF			
8	24	C/N	CH□ and PLC CPU communications result	See *2.	Normal	OFF			
9	25	P/S	CH□ parity/sum check error	Parity/sum check error	Normal	OFF	○		
10	26	PRO.	CH□ protocol error	Communications protocol error	Normal	OFF	○	—	
11	27	SIO	CH□SIO error	Overrun, framing error	Normal	OFF	○		
				When receive data purged because OS area is full.	Normal	OFF	—	○	
12	28	—	(Unavailable)	—	—	OFF	—		
13	29	SD WAIT	Send wait status	When data send wait state generated	After start of transmission	OFF	○		
14	30	SD	CH□ send status	Blinks during data transmission	Not sent	OFF			
15	31	RD	CH□ receive status	Blinks during data reception	Not received	OFF			
16	—	CH1 ERR.	CH1 error Occurrence	Switch setting error, mode switching error, send error, receive error, on-demand error	Normal	OFF			
—	17	CH2 ERR.	CH2 error Occurrence		Normal	OFF			
18		SW ERR.	Switch setting error	Switch setting error	Normal	OFF			
32		ERROR	Error batch	Any of CH□. ERR. error, C/N error, P/S error, PRO error, SIO error occur	Normal	OFF			

*1 The NEU. LED (LED No. 5, 21) come on when the objective interface is set to a dedicated protocol. When the objective interface is set to a protocol other than a dedicated protocol, these LEDs go off.

*2 The C/N LED (LED No. 8, 24) come on in the following cases:

- When an external device issued a data write request to the PLC CPU when Write During RUN Disable is set in SW07 described in Section 4.3.2. (See the [Write disable setting] column of the table in Section 5.4 for the functions that cannot be used when Write During RUN Disable is set.)
- When access between the QC24(N) and PLC CPU generated an error.

Notes

- The LED Nos. shown in the illustration are for description purposes. They are not printed on the actual module.
- The explanation in this manual is uniform for the large-type QC24(N) LED names shown in the above table except when specially classified.

(1) When an error or abnormality is displayed, take action according to the troubleshooting description.

(2) The LED initial status is the status during starting of the QC24(N) by power ON and PLC CPU reset.

(3) The C/N to SIO (LED No.5 to 11, 21 to 27), CH1 ERR., and CH2 ERR. (LED No. 16 to 17) LEDs come on when an error was generated and remain on until the error is reset.

The ON/OFF status of the LED in the illustration can be checked and LED that are ON can be turned off.

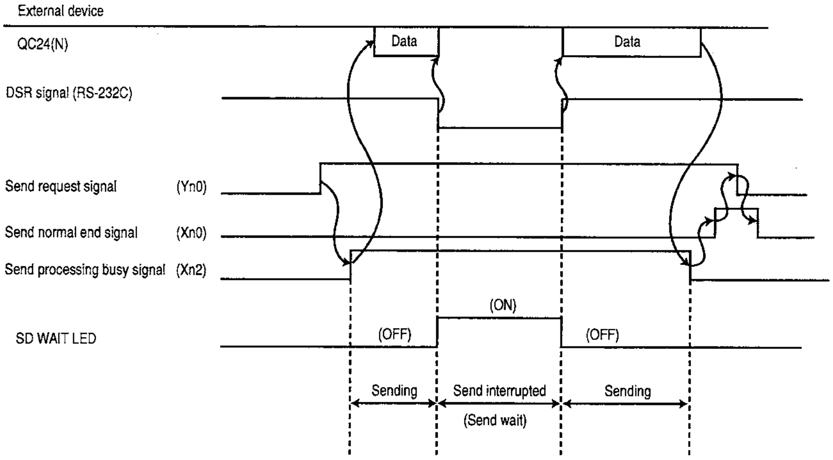
Turn OFF the LED according to Section 19.1.2.

(4) The RUN to NAK (LED No. 0 to 7, 21 to 23), and SD to RD (LED No. 14 to 15, 30 to 31) turn on/blink/turn off according to the QC24(N) status and status of communications with the PLC CPU at the time.

(5) The SD WAIT LED (LED No.13, 29) come on when QC24(N) transmission control cannot send data from the QC24(N) to an external device.

- When transmission cannot be started.
- When a transmission pause request is received from the external device while data is being received. (DSR signal OFF, DC3 receive)
  When transmission becomes possible, the LED goes OFF when data transmission is started/resumed.

(Example) When data is sent using non procedure protocol through the RS-232C interface



(6) The SW ERR. LED (LED No. 18) lights up in the following cases.

- When there is a setting error with a QC24(N) switch.
- When a PLC station that cannot be installed is installed in the QC24(N).

When this LED is turned on the QC24(N)'s two interfaces cannot be used, so remove the cause that turned on the LED and then restart the station installed in the QC24(N).

* For large-type QC24s, the "SW ERR." LED (LED No. 18) is available with module hardware version D and later (See Section 4.2).

(7) To check the LED display states of the CH□.E, C/N, P/S, PRO., and SIO in the small-type QC24(N), turn the LED display select switch to ERR.

Display select switch state	Valid display LED
ERR.	ERR., C/N, P/S, PRO., SIO
STS	C R/W, SW.E., NEU., ACK., NAK, SD W

4.5 Mounting and Installation

This section describes the handling precautions and installation environment common to all the modules when handling the QC24(N) from unpacking to installation.

Refer to the User's Manual of the PLC CPU module used for a detailed description of mounting and installation of the module.

4.5.1 Handling precautions

This section the describes the module handling precautions.

(1) The module case is made of plastic. Be sure not to drop it or subject it to strong vibration.

(2) Tighten the module mounting screws within the following tightening torque range.

Screw	Tightening torque range
RS-422/485 terminal block screws (M3.5 screws)	59 to 88 N·cm
Module mounting screws (M4 screws)	78 to 118 N·cm
RS-422/485 terminal block mounting screws (M3 screws)	39 to 59 N·cm
RS-232C, RS-422 connector mounting screw (M2.6 screws)	19 to 24 N·cm

POINT

Be sure to read through the Safety Precautions in the beginning of this manual for handling of the QC24(N).

4.5.2 Installation environment

Do not install the QnA Series PLC in the following environments.

(1) Where the ambient temperature exceeds the 0 to 55°C range.

(2) Where the ambient humidity exceeds the 10 to 90%RH range.

(3) Where condensation is produced by sudden temperature changes

(4) Where corrosive or combustible gas is present

(5) Where dust, iron powder and other conductive powder, oil mist, salt, or organic solvents are prevalent

(6) In direct sunlight

(7) Where a strong electric or magnetic field is generated

(8) Where vibration and shock may be transmitted directly to the module

⚠CAUTION

- Use the PLC in an environment that meets the general specifications contained in this manual. Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.

4.6 Individual Tests

After mounting the QC24(N) to the QnACPU base unit or MELSECNET/10 remote station, first carry out the module test described below to check the QC24(N) switch settings and operation.

POINTS

(1) Perform this module test when checking if operation of the QC24(N) is the problem when trouble occurs during data communications with an external device.
(2) To avoid system trouble, set the PLC CPU to the STOP state during the module test.
(3) Test the two QC24(N) interfaces simultaneously.
However, the self loopback test can test only one of the two interfaces.
In this case, ignore the LED display of the untested interface.
(4) Perform the switch setting and cable connections for the QC24(N) for individual test after the power to the QC24(N) installed station is turned off.
(5) If an error occurs during an individual test, report the error contents to your nearest Mitsubishi Electric System & Service Co., Ltd., dealer, or branch office.
(6) When an individual test is completed and data communication is to be started, first turn off the power of the QC24(N) installed station, then perform switch setting and cable connections.
(7) When an individual test is completed and data communication is to be started, set the mode setting switches and transmission specification setting switches for the interfaces not performing data communication, as follows:
· Mode setting switch : Set to one of 1 to 7.
· Transmission specification setting switch : Set all to off.

4.6.1 ROM/RAM/switch test

ROM/RAM/switch test procedure

Perform the ROM/RAM/switch test as follows:

(Step 1) Mode switch and transmission specifications switch setting

① Set the CH2 mode switch to “E” (ROM/RAM/switch test).
Set the CH1 mode switch to the mode number (0 to 9) used when exchanging data with an external device after the end of the test. (See Section 4.3.1.)

② Set the transmission switch of the two interfaces to match the transmission specifications when exchanging data with an external device. (See Section 4.3.2.)

(Step 2) ROM/RAM/switch test execution

① Set the PLC CPU to the STOP state.

② About one second after the PLC CPU/remote station power is turned on, or the CPU is reset, the QC24(N) automatically starts the test.

③ The QC24(N) performs the following tests one time.

ⓐ ROM check
Reads the ROM data and performs a sum check.

ⓑ RAM check
Writes test data to the QC24(N) RAM and reads the written data and performs a sum check.

ⓒ Switch check
Checks if station number switch, mode switch, and transmission specification switches SW09 to SW12 are set within the allowable range and if CH1 SW01 is OFF.

ⓓ Linked operation setting check (Performed when CH2 SW01 is ON.)
Checks the following:
- If the CH1 mode switch is set to “0”.
- If the transmission rate is within the allowable range.

(Step 3) End of ROM/RAM/switch test

① The SD WAIT LED (No. 13/29) come on and testing ends. (For about 2 seconds)

Large-type QC24(N)

Use the following LED to check if the tested interface is normal or abnormal.
The LED Nos. in the table correspond to the description use LED Nos. given in Section 4.4.

Test item		LED to be checked	LED No.		Status when normal	Status when abnormal
			CH1	CH2		
(Test end)		SD WAIT	No.13	No.29	● (ON)	
ROM check		CH1 ERR.	No.16		○ (OFF)	● (ON)
RAM check		CH2 ERR.	No.17		○ (OFF)	● (ON)
Switch check	Station No. setting.	SW ERR.	No.18		○ (OFF)	● (ON)
	Mode setting	C/N	No.8	No.24	○ (OFF)	● (ON)
	Transmission specifications setting	P/S	No.9	No.25	○ (OFF)	● (ON)
Linked operation setting check	Mode setting	PRO.	No.10		○ (OFF)	● (ON)
	Transmission specifications setting	SIO	No.11		○ (OFF)	● (ON)

Small-type QC24(N)

ⓐ After the test is completed turn the LED display select switch to STS and check whether the next LED display status is normal/error.

Test item	LED to be checked	LED No.		Status when normal	Status when abnormal
		CH1	CH2		
(Test end)	SD W	No.13	No.29	● (ON)	
Switch check (Station NO. setting)	SW.E.	No.18		○ (OFF)	● (ON)
Batch check	ERROR	No.32		○ (OFF)	● (ON)

When the ERROR LED turns off (normal end) after checking, the ⓑ procedure is not necessary.

ⓑ Turn the LED display select switch from STS to ERR. and check whether the next LED display state is normal/error. (After checking return the LED display select switch from ERR. to STS.)

Test item		LED to be checked	LED No.		Status when normal	Status when abnormal
			CH1	CH2		
ROM check		ERR. (CH1 side)	No.16		○ (OFF)	● (ON)
RAM check		ERR. (CH2 side)	No.17		○ (OFF)	● (ON)
Switch check	Mode setting	C/N	No.8	No.24	○ (OFF)	● (ON)
	Transmission specifications setting	P/S	No.9	No.25	○ (OFF)	● (ON)
Linked operation setting check	Mode setting	PRO.	No.10		○ (OFF)	● (ON)
	Transmission specifications setting	SIO	No.11		○ (OFF)	● (ON)

② After checking if the QC24(N) is normal/abnormal, perform the following processing.

When normal................. Perform ③ to end the test.
When abnormal............. When switch check or linked operation check generated an error, correct the setting and repeat the test.
When ROM check or RAM check generated an error, check the mounting state of the module and repeat the test.
If the module is mounted correctly, consult your nearest Mitsubishi Electric System & Service Co., Ltd., dealer, or branch office.

③ Operation at end of test

ⓐ Turn off the power.

ⓑ Check the mode switch setting.

- To perform the self loopback test, set the mode switch to “F”.
- When beginning data communication with external equipment after the test is completed, set the mode No. to “1” to “7” when communicating data between both CH1 and CH2 and the external equipment.

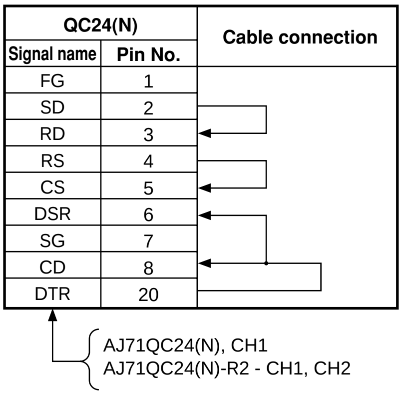
4.6.2 Individual loopback test

Individual loopback test operation procedure

(Step 1) Cable connection

Connect the cables to the two interfaces as shown below.
Install the RS-232C and RS-422 interfaces to the objective interfaces by connecting the cable inside the connector.
Connect the RS-422/485 interface by connecting the cable on the terminal board.

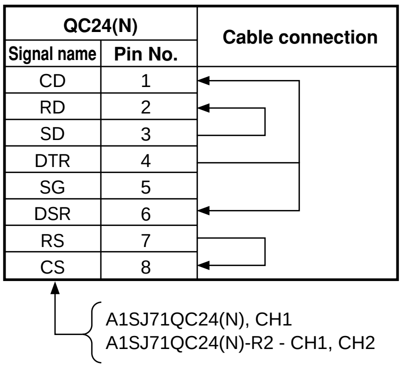
RS-232C interface (25-pin)



QC24(N)		Cable connection
Signal name	Pin No.	
FG	1	
SD	2	
RD	3	
RS	4	
CS	5	
DSR	6	
SG	7	
CD	8	
DTR	20	

AJ71QC24(N), CH1
AJ71QC24(N)-R2 - CH1, CH2

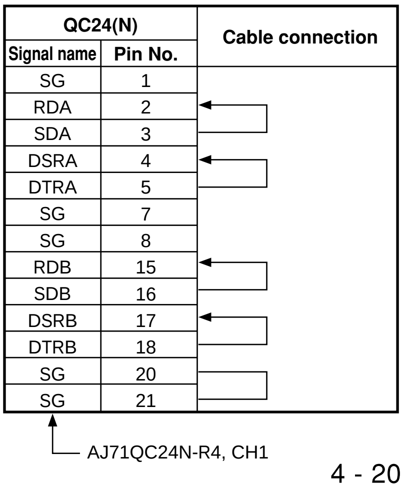
RS-232C interface (9-pin)



QC24(N)		Cable connection
Signal name	Pin No.	
CD	1	
RD	2	
SD	3	
DTR	4	
SG	5	
DSR	6	
RS	7	
CS	8	

A1SJ71QC24(N), CH1
A1SJ71QC24(N)-R2 - CH1, CH2

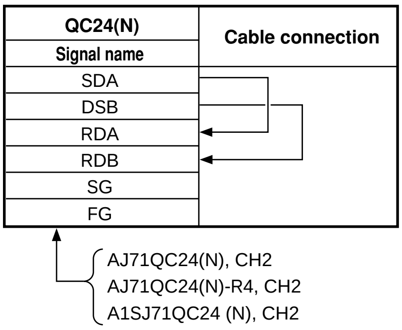
RS-422 interface



QC24(N)		Cable connection
Signal name	Pin No.	
SG	1	
RDA	2	
SDA	3	
DSRA	4	
DTRA	5	
SG	7	
SG	8	
RDB	15	
SDB	16	
DSRB	17	
DTRB	18	
SG	20	
SG	21	

AJ71QC24N-R4, CH1

RS-422/485 interface



QC24(N)	Cable connection
Signal name	
SDA	
DSB	
RDA	
RDB	
SG	
FG	

AJ71QC24(N), CH2
AJ71QC24(N)-R4, CH2
A1SJ71QC24 (N), CH2

(Step 2) Mode switch and transmission specifications switch setting

① Set the mode switch of the two interfaces (CH1, CH2) to "F" (self loopback test). (See Section 4.3.1.)

② Set the transmission specification switch of the two interfaces to match the transmission specifications when exchanging data with an external device. (See Section 4.3.2.)

(Step 3) Individual loopback test execution

① Set the PLC CPU to the STOP state.

② About one second after the PLC CPU/remote station power is turned on, or the CPU is reset, the QC24(N) automatically begins the test.

③ The QC24(N) sequentially performs the following tests repeatedly.
When the test results are all abnormal, the test ends.
(One test cycle takes about one second.)

ⓐ Check of communications with PLC CPU
Reads and checks the PLC CPU model name.

ⓑ Interface send and receive functions check
Sends and receives data through the connection cable while changing the data.

④ When testing starts, the LED of the relevant interface turn on and off as shown below.
The LED Nos. shown in the table, including (Step 4), correspond to the description use LED Nos. given in Section 4.4.

Test item	**LED to be checked**	**LED No.**		**Display during check**
		CH1	**CH2**	
Communications with PLC CPU check	NEU., ACK., NAK, CPU R/W (C R/W)	No.1, 5 to 7		NEU to NAK sequentially light. (CPU R/W: Light dimly)
CH1 interface communications check	SD, RD	No.14,15	—	Blink dimly
CH2 interface communications check	SD, RD	—	No.30, 31	Blink dimly

(Step 4) End of individual loopback test

① Check the test results.

Lage-type QC24(N)

Check whether the lower LED display state used for the interface being tested is normal/error.

Test item	**LED to be checked**	**LED No.**		**Status when normal**	**Status when abnormal**
		CH1	**CH2**		
Communications with PLC CPU check	C/N (CH1 side)	No.8		○ (OFF)	● (ON)
CH1 interface communications check	CH1 ERR.	No.16	—	○ (OFF)	● (ON)
CH2 interface communications check	CH2 ERR.	—	No.17	○ (OFF)	● (ON)

Small-type QC24(N)

Check the ERROR LED (No. 32) display state.

- Off (normal end): ..... Checking if the lower LED is lit is unnecessary.
- Lit (fault end): .... Turn the LED display's select switch from STS to ERR. and check the next LED display state. (After checking return the LED display select switch from ERR. to STS.)

Test item	**LED to be checked**	**LED No.**		**Status when normal**	**Status when abnormal**
		CH1	**CH2**		
Communications with PLC CPU check	C/N (CH1 side)	No.8		(OFF)	●(ON)
CH1 interface communications check	ERR. (CH1 side)	No.16	—	(OFF)	●(ON)
CH2 interface communications check	ERR. (CH2 side)	—	No.17	(OFF)	●(ON)

② After checking if the QC24(N) is normal/abnormal, perform the following processing.

When normal .... Perform ③ to end the test.
When abnormal .... Perform the following checks and after correcting setting/connection/mounting, repeat the test.

- Cable connection method and connection state check
- PLC CPU error check
- Module mounting state check

When an error is detected again by checking and retesting, consult your nearest Mitsubishi Electric System & Service Co., Ltd., dealer, or branch office.

③ Operation at end of test

ⓐ Turn off the power.

ⓑ Change the mode switch setting.

- When beginning data communication with the external equipment after the test is completed, set the mode No. "1" to "7" when communicating data between both CH1 and CH2 and the external equipment.
- To perform the ROM/RAM/switch test, set CH1 to "1" to "7" and CH2 to "E".

ⓒ To start data communications with an external device, connect the data communications cable. (See Section 4.7.)

POINT

When two or more QC24(N) are installed to the base unit, perform a self loopback test on each QC24(N).
Performing the self loopback test simultaneously on two or more QC24(N) will generate a communication with PLC CPU check error.

4.7 External Wiring

This section describes the wiring between the QC24(N) and external device.

4.7.1 Precautions during wiring

External wiring which is resistant to the effects of external noise is a prerequisite for reliable system operation (full use of the QC24(N) functions).

The following describes the precautions that must be taken when connecting the external wiring.

- Ground the shield of shielded wires and cables at only one point.
- The RS-422/485 interface terminal block uses M3.5 screws.
  Fasten suitable sized crimped terminals to the ends of the cables before connecting the cables to the terminals.
- Connect the external device according to its specifications.
- Make the bend radius of cable some distance away from the connectors and terminal block at least "cable outside diameter × 10".
  See Appendix 5 (Outline Dimensions) for the bend radius of cable near the connectors and terminal block.

POINT

Be sure to read through the Safety Precautions in the beginning of this manual prior to making QC24(N) connections to external devices.

4.7.2 Connecting the RS-232C interface (full-duplex communications)

The following describes the connection precautions and standard connection examples when using the QC24(N) RS-232C interface for full-duplex communications.

When setting up full-duplex communications, interconnect the connectors as described in Section 14.5.

POINT

(1) Cautionary items for RS-232C line connection when using the modem function of the QC24(N) are shown below:
  - When connecting the QC24N and a modem/TA, use the RS-232C cable supplied with the modem/TA, or cables designated for the modem/TA.
  - For modems and TA's that can be connected to the RS-232C interface of the QC24N, see Section 21.3.
    In the case of AJ71QC24N-R2, A1SJ71QC24N-R2 or A1SJ71QC24N1-R2, data communications using the modem function may only be performed on either CH1 or CH2.

1 **Connection precautions**

(a) Make one of the connections shown on the next page 2 . Operation of the QC24(N) relative to the CD signal when the QC24(N) CD signal (pin 1/8) is connected to the external device is shown in 3 .

(b) Do not connect an RS-422 device to the RS-232C interface.
Such a connection may damage the hardware of the RS-422 interface of the connected device and cause a loss of communications.

(c) The connection cable FG signal and shield are connected as follows.

	When the QC24(N) is a 25-pin connector	When the QC24(N) is a 9-pin connector	Notes
Connection cable FG signal	Connect to the QC24(N) FG signal	Connect to the QC24(N) connector housing	• Do not short the communication cable FG signal and the SG signal. • When the FG signal and the SG signal are connected inside the external equipment, do not connect the QC24(N) FG signal to the external equipment.
Connection cable shield	Connect to the QC24 FG signal (do not connect with external equipment)	Connect to the external equipment FG terminal or the QC24(N) connector housing	

When normal data communication is not obtained due to external noise even if the wiring has been made as described above, perform the wiring as follows:

① Connect the FG terminals on the external device and QC24(N) using the shield of the connection cable as follows.

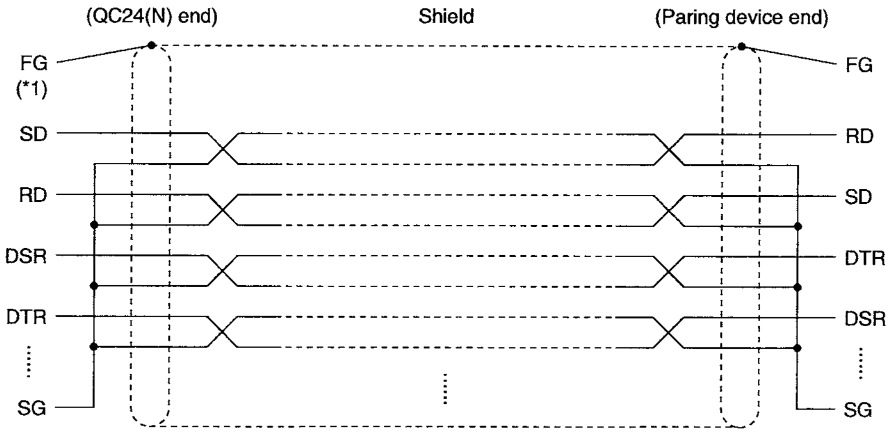
Large-type QC24(N) : Connect to the FG signal (No. 1 pin) of the RS-232C interface.

Small-type QC24(N) : Connect to the connector enclosure area of the RS-232C interface.

* Since the small-type QC24(N) do not use FG signals, the shield of the connection cable is connected to the connector enclosure area of the RS-232C interface.

However, the external devices should be wired according to the manual of the specific device.

② Signals other than SG of the connection cable should be connected in combination with SG signals.



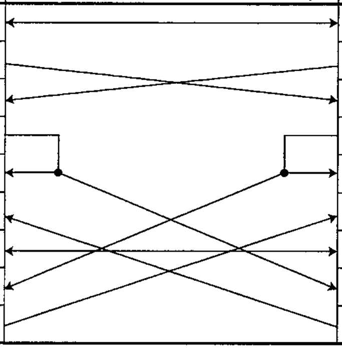
*1 FG of the QC24(N) is connected to the nut used to fasten the connector, thus it is the FG of the module itself.

> **POINT**
>
> When using an RS-232C–RS-422 converter to connect the external device and QC24(N), use a converter that is compatible with the external device and PLC CPU system configuration (1:1). Recommended converters and connection examples are shown in Appendix 6.

2 Connection examples

(a) Large-type QC24(N)

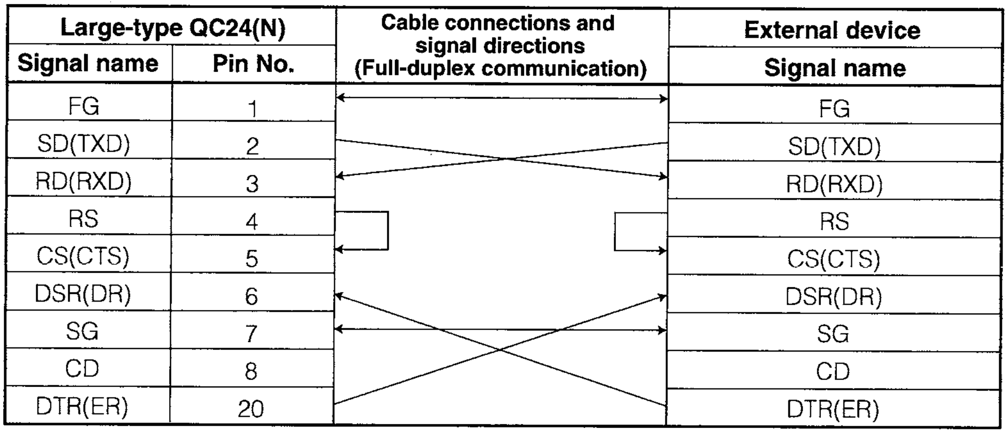
① Connection example with an external device capable of turning on and off the CD signal (No. 8 pin)

Large-type QC24(N)		Cable connections and signal directions (Full-duplex /half-duplex communication)	External device
Signal name	Pin No.		Signal name
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

* The "CD terminal check setting" shown in 3 is set according to the specification of the specific external device. When wiring using this method, DC code control or DTR/DSR control may be performed as the QC24(N) transmission control.

② Connection example with an external device not capable of turning on and off the CD signal (No. 8 pin)

(Connection example 1)

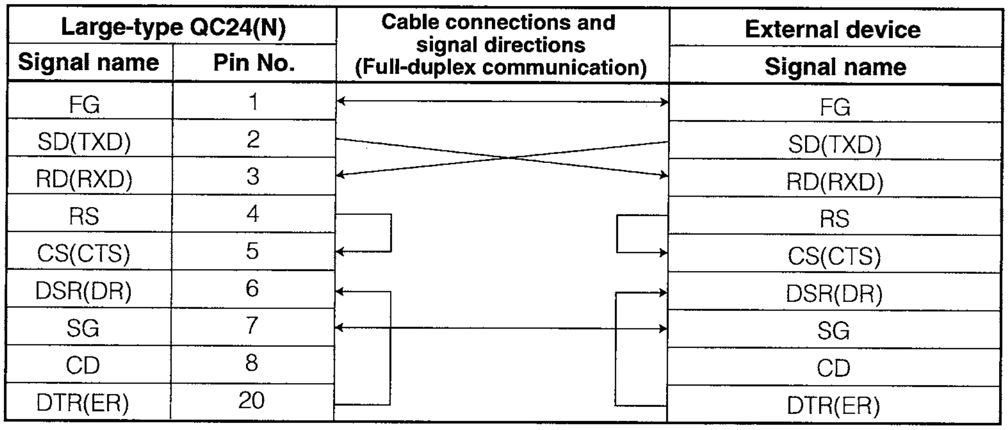


Large-type QC24(N)		**Cable connections and signal directions (Full-duplex communication)**	**External device**
Signal name	**Pin No.**		**Signal name**
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

* Set “Do not check” as the “CD terminal check setting” shown in $\boxed{3}$.

When wiring using this method, DC code control or DTR/DSR control may be performed as the QC24(N) transmission control.

(Connection example 2)



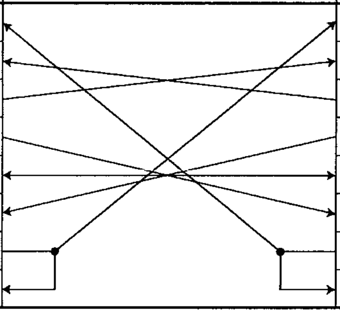
Large-type QC24(N)		**Cable connections and signal directions (Full-duplex communication)**	**External device**
Signal name	**Pin No.**		**Signal name**
FG	1		FG
SD(TXD)	2		SD(TXD)
RD(RXD)	3		RD(RXD)
RS	4		RS
CS(CTS)	5		CS(CTS)
DSR(DR)	6		DSR(DR)
SG	7		SG
CD	8		CD
DTR(ER)	20		DTR(ER)

* Set “Do not check” as the “CD terminal check setting” shown in $\boxed{3}$.

When wiring using this method, DC code control may be performed as the QC24(N) transmission control.

(b) Small-type QC24(N)

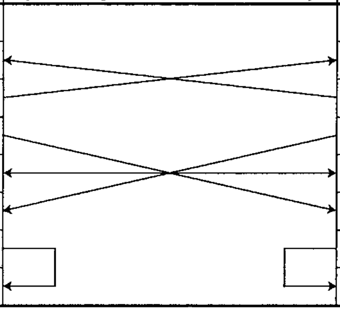
① Connection example with an external device capable of turning on and off the CD signal (No. 1 pin)

Small-type QC24(N)		**Cable connections and signal directions (Full-duplex /half-duplex communication)**	**External device**
Signal name	**Pin No.**		**Signal name**
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

* The "CD terminal check setting" shown in 3 is set according to the specification of the specific external device. When wiring using this method, DC code control or DTR/DSR control may be performed as the QC24(N) transmission control.

② Connection example with an external device not capable of turning on and off the CD signal (No. 1 pin)

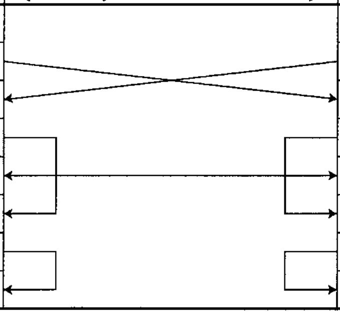
(Connection example 1)

Small-type QC24(N)		**Cable connections and signal directions (Full-duplex communication)**	**External device**
Signal name	**Pin No.**		**Signal name**
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

* Set "Do not check" as the "CD terminal check setting" shown in 3.

When wiring using this method, DC code control may be performed as the QC24(N) transmission control.

(Connection example 2)

Small-type QC24(N)		**Cable connections and signal directions (Full-duplex communication)**	**External device**
Signal name	**Pin No.**		**Signal name**
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

* Set "Do not check" as the "CD terminal check setting" shown in 3.

When wiring using this method, DC code control may be performed as the QC24(N) transmission control.

3 RS-232C CD terminal check setting

When the QC24(N) RS-232C interface is used, RS-232C CD terminal check setting may be necessary, depending on whether a signal line is connected to the QC24(N) CD terminal and if CD signal ON/OFF control by external device is enabled or disabled.
The following describes the RS-232C CD terminal check setting.

(a) RS-232C CD terminal check setting and operation of QC24(N) relative to CD signal RS-232C CD terminal check setting causes the QC24(N) to operate as shown below according to the status of the CD signal.

	Check CD terminal	Do not check CD terminal
Full-duplex	When the CD signal (receive carrier detection) is ON, send/receive processing is performed. When the CD signal is turned off during data communications, the QC24(N) transmission sequence is initialized.	Full-duplex communications send/receive processing is performed regardless of whether the CD signal is ON or OFF. (CD signal ON/OFF check is not performed and the same processing as when the CD signal is ON is performed.) Data communications with external devices whose CD signal is not turned ON/OFF is possible.

① In the following cases, set CD terminal check to [Do Not Check].

- When nothing is connected to the QC24(N) CD terminal
- When the external device cannot turn on the signal connected to the QC24(N) CD terminal.

② When the external device turns on the signal connected to the QC24(N) CD terminal as shown above, set CD terminal check to [Check].

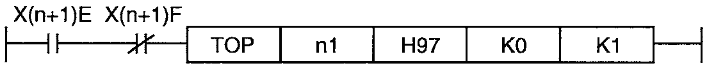
(b) RS-232C CD terminal check setting method

Perform CD terminal check setting according to (a) above.
(Also set buffer memory at addresses 97H (CH1) and 137H (CH2).)

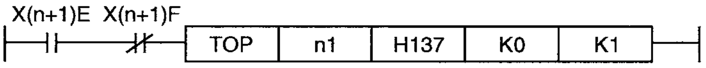
① Setting [Check]

Assemble the sequence program shown below.

(CH1 end)



(CH2 end)



② Setting [Do Not Check]

Since the QC24(N) default value is [Do Not Check], an RS-232C CD terminal check setting sequence program is unnecessary.

Note

When setting [Check], write [0] to the buffer memory of the address shown in the program above.

POINTS

(1) When the CD terminal was set to [Check], during full-duplex communications, turn ON the QC24(N) CD signal.
When the CD signal is turned OFF when sending data to the external device using the non procedure protocol, the QC24(N) stops sending and turns ON the send ended normally signal (Xn0/Xn7).
When the CD signal is turned OFF when transmission starts, the QC24(N) does not send any data, but turns ON the send ended normally signal (Xn0/Xn7).

(2) RS-232C CD terminal check setting is unnecessary except for the QC24(N) RS-232C interface.

4.7.3 Connecting the RS-422 interface (AJ71QC24(N)-R4 CH1)

The following describes the connection precautions and standard connection examples when the QC24(N) RS-422 interface is used.

1 **Connection precautions**

(a) Connect the QC24(N) DTR☐ terminal and DSR☐ terminal as shown below.

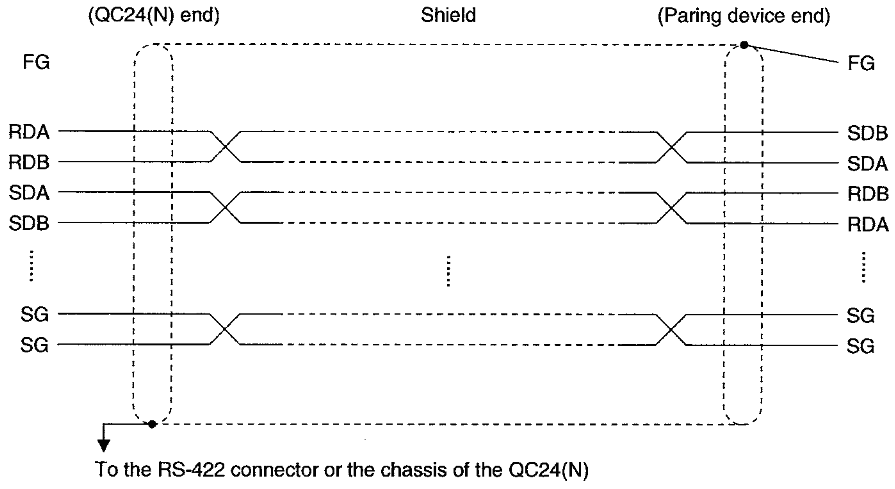
(b) Connect the shield of the connection cable on either of the connected devices.
When connecting to the QC24(N) side, connect to the FG signal.
If normal data communication is not obtained due to external noise even if wiring is made as shown above, perform wiring as follows:

① Connect the shield of the connection cable to both stations.

QC24(N) end : Connect the shield to the connector or to the chassis.
(Example) Connect to the (FG) terminal of the RS-422/485 interface.

External device end : Connect according to the instruction manual of the external device.
(Example) Connection to the FG terminal, etc.

② Connect nnA and nnB of each signal in the connection cable as a pair.



(c) The QC24(N) connector signal list is shown in Section 3.3.1.
Be sure that the signal list is correct.

(d) A terminating resistor must be connected, or set, at the external device.
Connect, or set, the terminating resistor according to the instruction manual of the external device.
Since the QC24(N) has a built-in terminating resistor across RDA and RDB, it is not necessary to connect a terminating resistor.

(e) Make the connections according to the QC24(N) RS-422 interface and connected device signal polarity specifications.
(Connection of the ☐ A and ☐ B signals to the QC24(N) may be the opposite of those shown in the illustration.)

(f) Do not input RS-232C signals to the RS-422 interface.
If RS-232C signals are input, the hardware of the RS-422 interface may be damaged and communications may be lost.

(g) For the countermeasures against false data reception on the external device side, see Section 3.3.3.

(h) If the external device does not operate the SG signal, short-circuit all of the QC24(N)'s RS-422 interface SG signals (pin numbers 7, 8, 20, 21). Short-circuiting the SG signals sometimes makes data communication possible.

POINT

When using an RS-232C–RS-422 converter to connect the external device and QC24(N), use a converter that is compatible with the external device and PLC CPU system configuration (1:1).

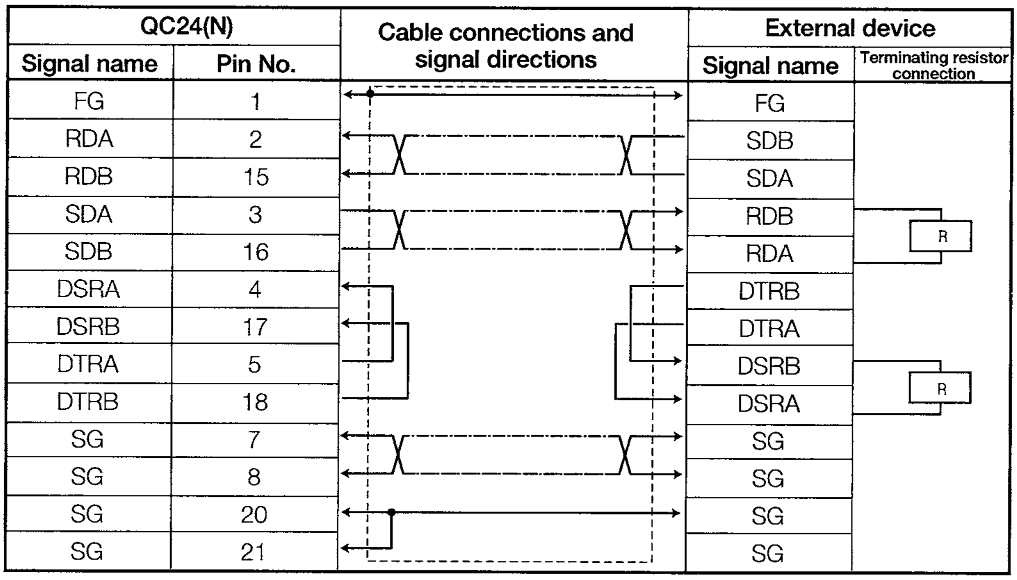
⚠ CAUTION

- When connecting a external device to the AJ71QC24(N)-R4 RS-422 interface, do not connect a device that must receive power from the AJ71QC24(N)-R4.

  The module or external device may be damaged.

2 Connection examples

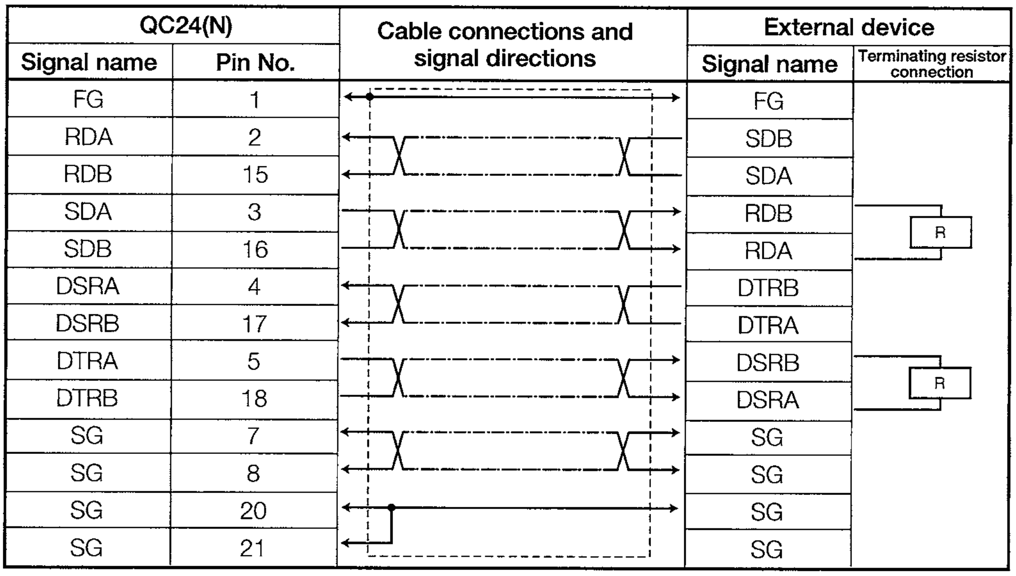
(a) Connection example 1



QC24(N)		Cable connections and signal directions	External device	
Signal name	Pin No.		Signal name	Terminating resistor connection
FG	1		FG	
RDA	2		SDB	
RDB	15		SDA	
SDA	3		RDB	
SDB	16		RDA	
DSRA	4		DTRB	
DSRB	17		DTRA	
DTRA	5		DSRB	
DTRB	18		DSRA	
SG	7		SG	
SG	8		SG	
SG	20		SG	
SG	21		SG	

* When the QC24(N) DTR□ and DSR□ signals are not connected to the external device as shown above, the QC24(N) can control transmission by DC code control. DTR/DSR control cannot be used.

(b) Connection example 2



QC24(N)		Cable connections and signal directions	External device	
Signal name	Pin No.		Signal name	Terminating resistor connection
FG	1		FG	
RDA	2		SDB	
RDB	15		SDA	
SDA	3		RDB	
SDB	16		RDA	
DSRA	4		DTRB	
DSRB	17		DTRA	
DTRA	5		DSRB	
DTRB	18		DSRA	
SG	7		SG	
SG	8		SG	
SG	20		SG	
SG	21		SG	

* By connecting the QC24(N) DTR□ and DSR□ signals to the external device as shown above, the QC24(N) can use DC code control or DTR/DSR control to control transmission.

4.7.4 Connecting the RS-422/485 interface

The following describes the connection precautions and standard connection examples when using the QC24(N) RS-422/485 interface.

1 Connection precautions

(a) When connecting the QC24(N) SG and FG signals to the external device, connect them according to the specifications of the external device.

(b) In the case of QC24N, connect the shield of the connection cable on either of the connected devices.

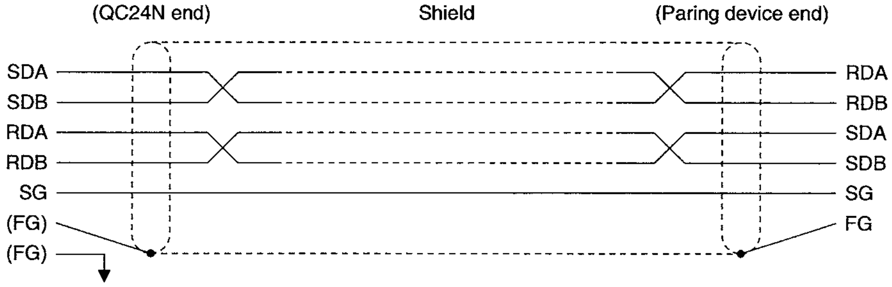
If normal data communication is not obtained due to external noise even if wiring is made as shown above, perform wiring as follows:

① Connect between the FG of both stations with the shield of the connection cable.

On the external device end, however, follow the instruction manual of the external device.

② Connect the (FG) of the QC24N end to the FG terminal at the power supply module of the station which has a QC24N PLC is installed, or to the FG terminal of the control panel on which the QC24N PLC is installed.

③ Connect nnA and nnB of each signal in the connection cable as a pair.



To the FG terminal at the power supply module of the station loaded with a QC24N, or to the FG terminal of the control panel

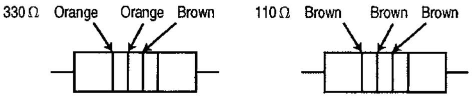
(c) The QC24(N) terminal block signal list is shown in Section 3.3.1.
Be sure that the signal list is correct.

(d) Make the connections by also referring to the QC24(N)specifications and precautions given in Section 3.3.3.

(e) At terminating resistor must be set (or connected) at the station at both ends of the circuit. Match the QC24(N) to the specifications of the external device and connect a terminating resistor according to this section and the User's Manual (Hardware) of the QC24(N) used. Connect, or set. a terminating resistor at the external device according to the instruction manual of the external device.
The terminating resistors (packed with the QC24(N)) to be connected to the QC24(N) are shown below.

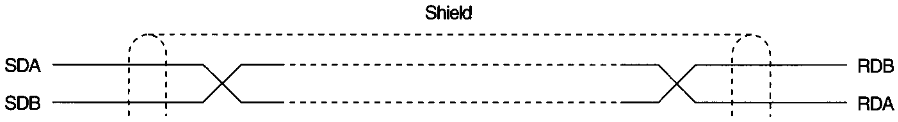
- When communications performed using RS-422: "330Ω 1/4W" resistor
- When communications performed using RS-485: "110Ω 1/2W" resistor

* How to discriminate between the terminating resistors



(f) If data communication with the external device fails, reverse □A and □B of each signal at one of the devices and connect again after comfirming the specifications of the target device. Reversing □A and □B of the signals sometimes makes data communication possible.

(For SDA ·SDB)
Connect SDA to RDB of the target device and SDB to RDA of the target device.

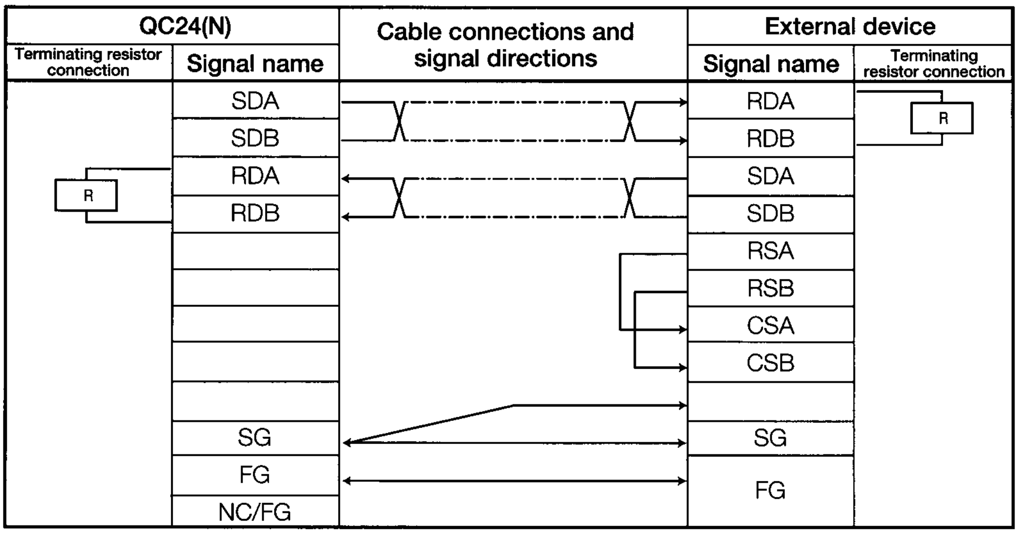


POINT

(1) For terminating resistor setting/connection described in this section, when an RS-232C-RS-422 converter or similar device is used at the external device at both ends of the circuit, a terminating resistor must be set, or connected, at the converter.
(2) When using an RS-232C — RS-422 converter to connect the external devices and the QC24(N), use a converter that is compatible with the external device and PLC CPU system configuration (1:1, 1:n, m:n).
(3) Device connected to the QC24(N) RS-422/485 interface must be standardized as RS-422 or RS-485, including 1:n, n:1 and m:n connections.

2 Connection examples

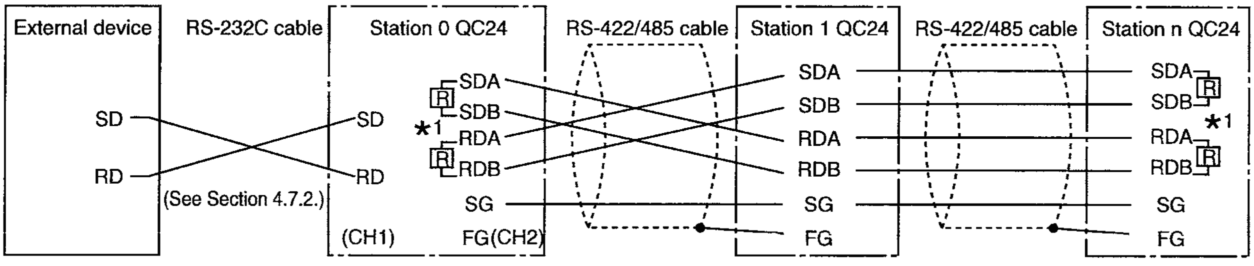
(a) When external device and QC24(N) connected in a 1:1 configuration



QC24(N)		Cable connections and signal directions	External device	
Terminating resistor connection	Signal name		Signal name	Terminating resistor connection
	SDA	→	RDA	R
	SDB	→	RDB	
R	RDA	←	SDA	
	RDB	←	SDB	
			RSA	
			RSB	
			CSA	
			CSB	
	SG	↔	SG	
	FG	↔	FG	
	NC/FG			

(b) When external device and QC24(N) connected in a 1:n configuration (multidrop connection)

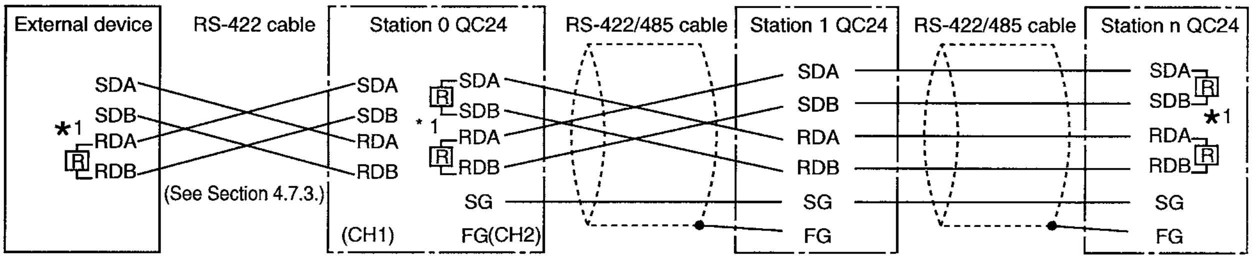
① When external device and station 0 QC24(N) connected through RS232C interface



*1 indicates terminating resistor connection.
*2 indicates linked operation station. (See Section 4.3.1.)

(QC24: QC24, QC24N)

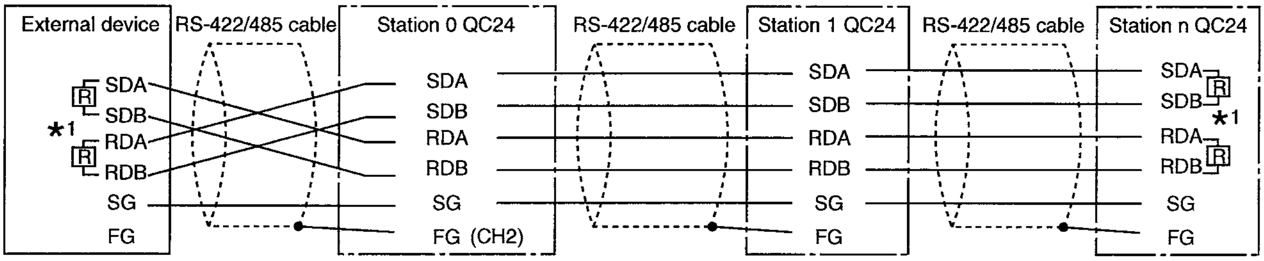
② When external device and station 0 QC24(N) connected through RS-422 interface



*1 indicates terminating resistor connection/setting.
*2 indicates linked operation station. (See Section 4.3.1.)

(QC24: QC24, QC24N)

③ When external device and QC24(N) are all connected through RS-422/485 interface

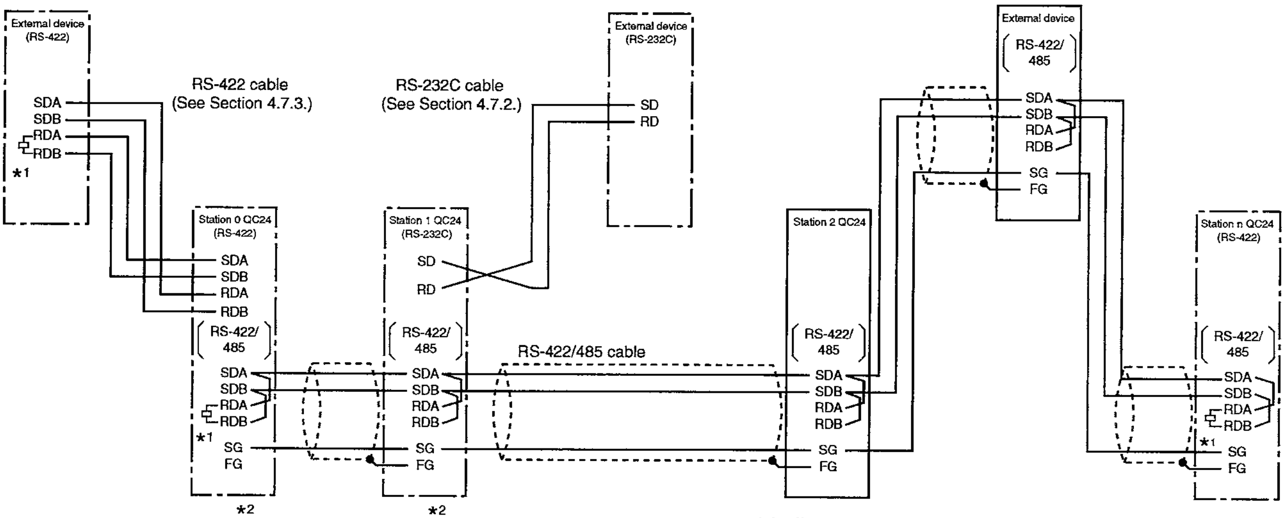


*1 indicates terminating resistor connection/setting.

(QC24: QC24, QC24N)

(c) When external devices and QC24(N) connected in an m:n configuration (multidrop connection)

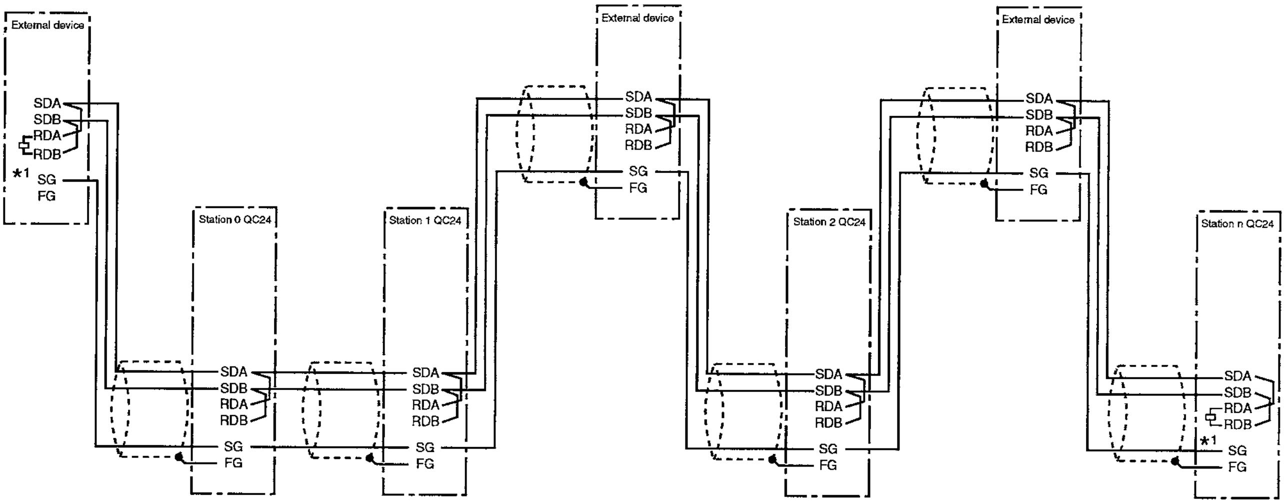
① When external devices and QC24(N) connected through RS-232C, RS-422, and RS-422/485 interfaces and QC24(N)s are interconnected through RS-422/485 interface



★1 indicates terminating resistor connection/setting.
★2 indicates linked operation station. (See Section 4.3.1.)

(QC24: QC24, QC24N)

② When external devices and QC24(N) are all connected through RS-422/485 interface



★1 indicates terminating resistor connection/setting.

(QC24: QC24, QC24N)

4.8 Setting the Mode and Starting Operation

After checking that the QC24(N) is operating normally and the connections to the external devices are completed, data can be transferred with the external devices.

This section describes processing from completion of each job described in Sections 4.3 to 4.7 to the start of data communications.

4.8.1 Loopback test

"Loopback test" is a function that uses dedicated protocol loopback test commands (ASCII mode: TT, binary mode: 0619) to check the external device and QC24(N) connections and communications functions.

If data communications using a dedicated protocol is possible at the external device, carry out the loopback test as described below.

(Step 1) External device and QC24(N) connection

Connect the cable and terminating resistor to match the regular system configuration according to Section 4.7.

(Step 2) Mode switch setting

Set the mode switch to "1" to "5" so that the interface to be loopback tested is for dedicated protocol.
(See Section 4.3.1 for a detailed description of the setting method.)

(Step 3) PLC CPU starting

When the PLC CPU is placed into the STOP state and the power is turned on, or the CPU is reset, the QC24(N) ready signal (X (n+1) E) is turned ON and the loopback test is enabled.

(Step 4) Loopback test command execution (*1)

① Generate a loopback test program at the external device and send commands and data to the QC24(N).
See to Section 5.16 of the Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function) for a detailed description of the formats 1 to 4 message structure and loopback test command (TT).
See Sections 6.1.3 and 6.13 of this manual for a detailed description of the format 5 message structure and loopback test command (0619).

② The QC24(N) sends the receive data to the external device unchanged.

(Step 5) Data check at external device

① Check if the data sent from the external device and the data returned from the QC24(N) match at the external device.
If the data match, communications between external device and QC24(N) is normal.
If the data do not match, the transmission specification settings do not match or the CD terminal is turned ON/OFF repeatedly.
Locate and correct the cause of the trouble according to troubleshooting of Chapter 22 and repeat the loopback test.

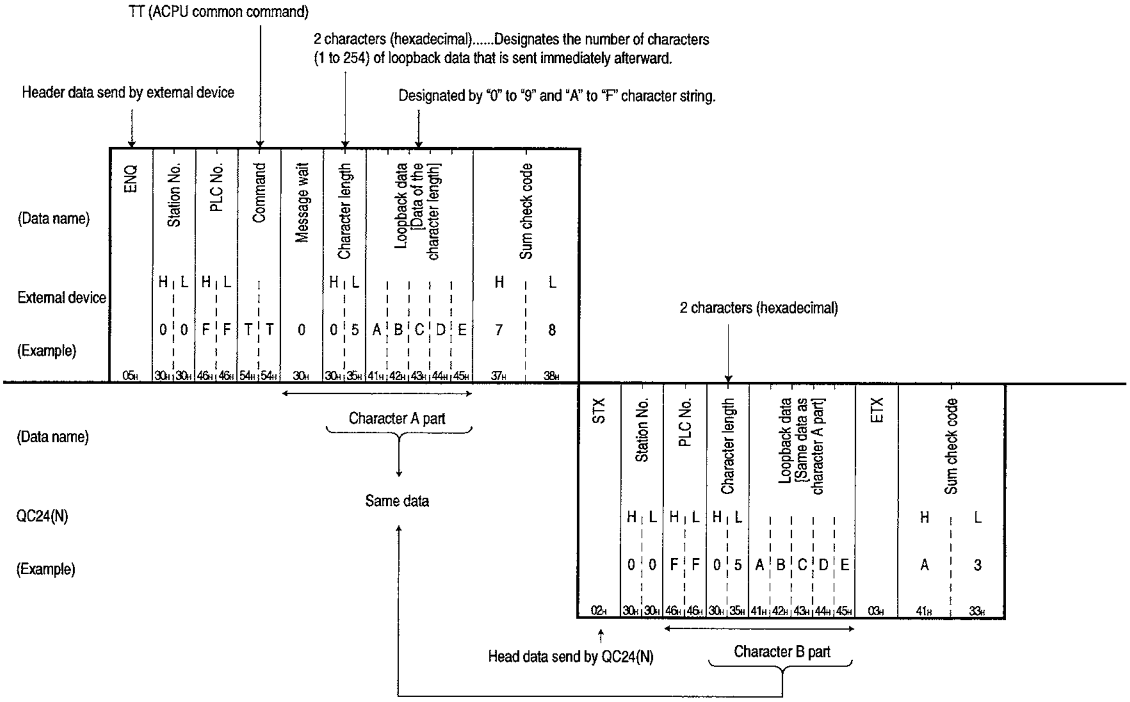
② When communications are impossible
Hardware setting, cable connection, etc. were not performed correctly.
Locate and correct the cause of the trouble according to troubleshooting of Chapter 22 and repeat the loopback test.

③ After the end of the loopback test, data communications using dedicated protocol set format is possible.
When exchanging data by changing the format or the protocol (non procedure protocol/ bidirectional protocol), start data communications according to Section 4.8.2.

*1 An example when the following QC24(N) switch settings are performed and the loopback test is carried out using a format 1 message is shown below.

- Mode switch set to [1]. .... Selects ASCII mode format 1 as the dedicated protocol data communications message format.
- Station number switch set to [00] ...... QC24(N) station No. [00]
- Transmission specifications .... Selects sum check code addition switch SW06 set to [ON].

See Section 5.4 of the Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function) for the message and control procedure basics.



4.8.2 Setting the mode and starting operation

1 **Mode setting**

① After checking of the external device connections and communication functions using with the loopback test are complete, set the mode switch so that the interface connecting the external device becomes the data communication function used.

② The set mode and mode number correspondence is shown in Section 4.3.1. Two setting methods are available: setting by mode switch and setting by mode switching function. See Section 4.3.1 for a detailed description of the mode switch.

③ After setting the mode, reset the PLC CPU power or the PLC CPU and restart the QC24(N). When using the mode switching function to set the mode, set the mode according to Section 18 and restart the QC24(N).

2 **Starting operation**

After QC24(N) mode setting and restarting are complete, the set function data communications are performed. Carry out data communications according to the description of the following manuals which describe the set mode.

(a) Dedicated protocol data communications

① Data communications using A compatible frame
Chapter 5 of this manual and Chapter 5 of the Computer
Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function)

② Data communications using QnA frame and QnA extension frame
Chapter 5 to 7 of this manual

③ Data communications using QnA simplified frame
Chapter 5 and 8 of this manual

(b) Non procedure protocol data communications
Chapters 9 to 11 of this manual

(c) Bidirectional protocol data communications
Chapters 12 and 13 of this manual

When changing (writing) the parameters of the QC24(N) buffer memory special applications area, do so according to the pertinent description of the function used.

IMPORTANT

When using the module while values, such as buffer memory set values, are registered in the EEPROM, do not turn off the power supply for the module loading station nor reset the PLC CPU. If the power supply for the module loading station is turned off or the PLC CPU is reset while any values are registered, the data contents in the EEPROM become inconsistent and as a result the values must be set again in the buffer memory, etc. and reregistered to the EEPROM. Also, this may cause failure and malfunctions of the module.

4.9 Connecting Peripheral Device and GOT for GPP Function

4.9.1 Connecting peripheral device for GPP function

By connecting a peripheral device for QnACPU compatible GPP function (SWn☐-GPPQ) to the QC24(N) CH1 interface, the QnACPU of the connected station can be accessed from the GPP function.

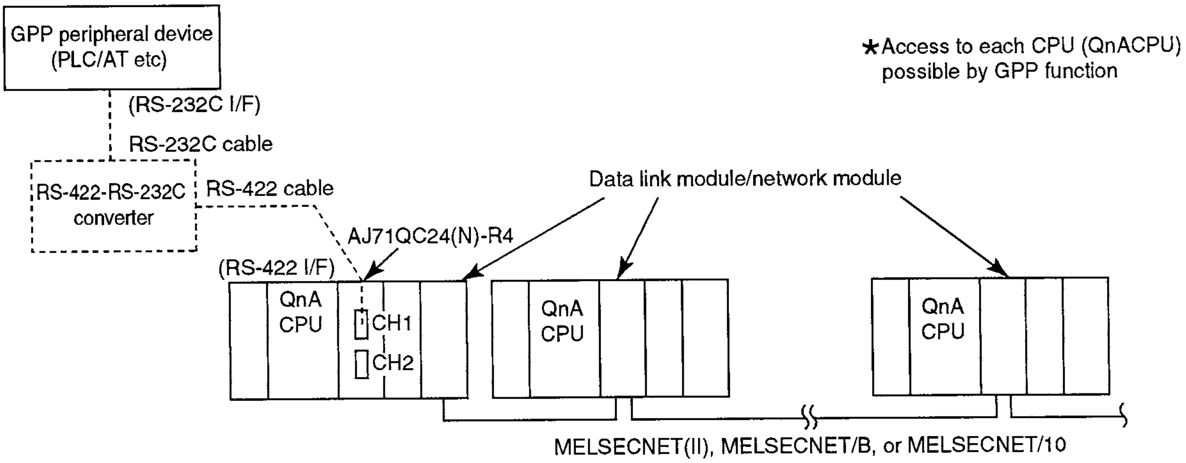
This section describes wiring examples and the QC24(N) switch setting for connecting a GPP function peripheral device described above to the QC24(N) CH1 interface and performing the GPP function.

See the QnACPU compatible GPP function Operating Manual for a detailed description of the wiring, how to use the GPP function, and the operating instructions.

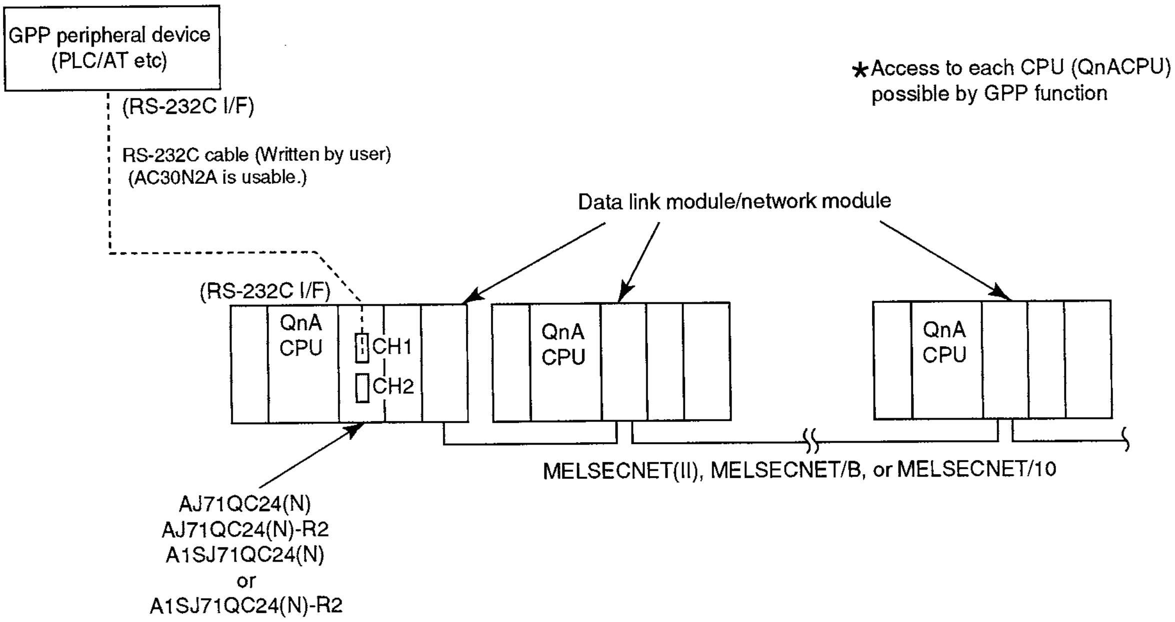
* See the operating manual of the software for the connection of the peripheral device for GPP function software for Windows.

1 Wiring example

① Connection to RS-422 interface



② Connection to RS-232C interface



2 QC24(N) settings

① Switch settings (CH1: RS-232C/RS-422)

<table>
<tr><th colspan="2">Switch (CH1)</th><th>Setting item</th><th>Set value (Setting contents)</th><th>Notes</th></tr>
<tr><td colspan="2">Mode switch</td><td>Mode</td><td>5 (binary mode)</td><td>Dedicated protocol (format 5)</td></tr>
<tr><td colspan="2">Station number switch</td><td>Station number</td><td>00 to 31</td><td>When CH2 is a multidrop connection, the station number must not be duplicated.</td></tr>
<tr><td colspan="2">Transmission specifications switch</td><td></td><td></td><td>—</td></tr>
<tr><td rowspan="12"></td><td>SW01</td><td>Operation setting</td><td>OFF (independent operation)</td><td rowspan="6">—</td></tr>
<tr><td>SW02</td><td>Data bits setting</td><td>ON (8 bit)</td></tr>
<tr><td>SW03</td><td>Parity bit enable/disable setting</td><td>ON (Enable)</td></tr>
<tr><td>SW04</td><td>Even parity/odd parity setting</td><td>OFF (odd parity)</td></tr>
<tr><td>SW05</td><td>Stop bit setting</td><td>OFF (1 bit)</td></tr>
<tr><td>SW06</td><td>Sum check enable/disable setting</td><td>ON (enable)</td></tr>
<tr><td>SW07</td><td>Write during RUN enable/disable setting</td><td>ON (enable)</td><td>The GPP function uses PLC CPU setting to judge if write during run is enabled or disabled.</td></tr>
<tr><td>SW08</td><td>Setting change enable/disable setting</td><td>ON/OFF</td><td>Setting can be made at either setting.</td></tr>
<tr><td>SW09</td><td rowspan="4">Transmission rate setting</td><td rowspan="4"><table><tr><td>Transmission rate (BPS)</td><td>9600</td><td>19200</td></tr><tr><td>SW09</td><td>ON</td><td>OFF</td></tr><tr><td>SW10</td><td>OFF</td><td>ON</td></tr><tr><td>SW11</td><td>ON</td><td>ON</td></tr><tr><td>SW12</td><td>OFF</td><td>OFF</td></tr></table></td><td rowspan="4">Set to match the GPP function set rate.</td></tr>
<tr><td>SW10</td></tr>
<tr><td>SW11</td></tr>
<tr><td>SW12</td></tr>
<tr><td></td><td>SW13
to
SW15</td><td>—</td><td>All OFF</td><td>These switches are on the left side of the module, as viewed from the front.
(Large-type QC24 only)</td></tr>
</table>

② Buffer memory (special applications area) setting (CH1)

- Make CH1 interface addresses 90H to 12FH in the buffer memory special applications area the QC24(N) default value. (See the table in Section 3.5.)

3 Restrictions when using the GPP function

The following describes the restrictions when a peripheral device is connected to the QC24(N) and the GPP function is used.
Restrictions other than those given below are the same as when a QnACPU compatible GPP function peripheral device is connected to a QnACPU.

① GPP function setting

- See the GPP function operating manual for a description of the GPP function setting when a GPP function peripheral device is connected to the QC24(N).

② Accessible PLC CPU

- QnACPU station connecting the GPP function peripheral device.
- QnACPU station above and QnACPU accessed over a MELSECNET/10, MELSECNET (II), or MELSECNET/B.

③ When the two QC24(N) interfaces are linked and the CH2 interface system configuration is 1:n or m:m, only one GPP function peripheral device can be connected to the system. At this time, the devices connected to each circuit cannot transfer data at the same time.

POINTS

(1) A GPP function peripheral device can be connected only to the QC24(N) CH1 interface (RS-232C/RS-422).

(2) When connecting a GPP function peripheral device to the QC24(N) RS-232C interface, always connect the QC24(N) SD, RD, DTR, DSR, and SG signals to the GPP function peripheral device.

④ Access time restriction

- Access to the QnACPU is somewhat slower than when a GPP function peripheral device is connected to the QnACPU.
- When a special function module (another QC24(N), computer link module, etc.) that accesses the QnACPU is used, access becomes still slower.
  In this case, make the number of general data processing settings by QnACPU parameter [PLC System Setting] large. The QnACPU END processing time increases, but the QnACPU processes all communication requests accepted in one scan during END processing of that scan.

⑤ Restrictions during monitoring

A special function module and a GPP function peripheral device cannot conditionally monitor the same QnACPU device memory at the same time.
(Unconditional monitoring or conditional monitoring and unconditional monitoring can be carried out simultaneously.)

For instance, when another special function module and GPP function peripheral device conditionally monitor the same QnACPU, conditional monitoring using the dedicated protocol command shown below cannot be performed.
(If the external device sends a command message with a monitoring condition, the QC24(N) will return a NAK message.)

Command	Function	Description of function
0403	Word units random read	Section 6.2.6.
0802	Registered device memory monitoring	Section 6.2.9.

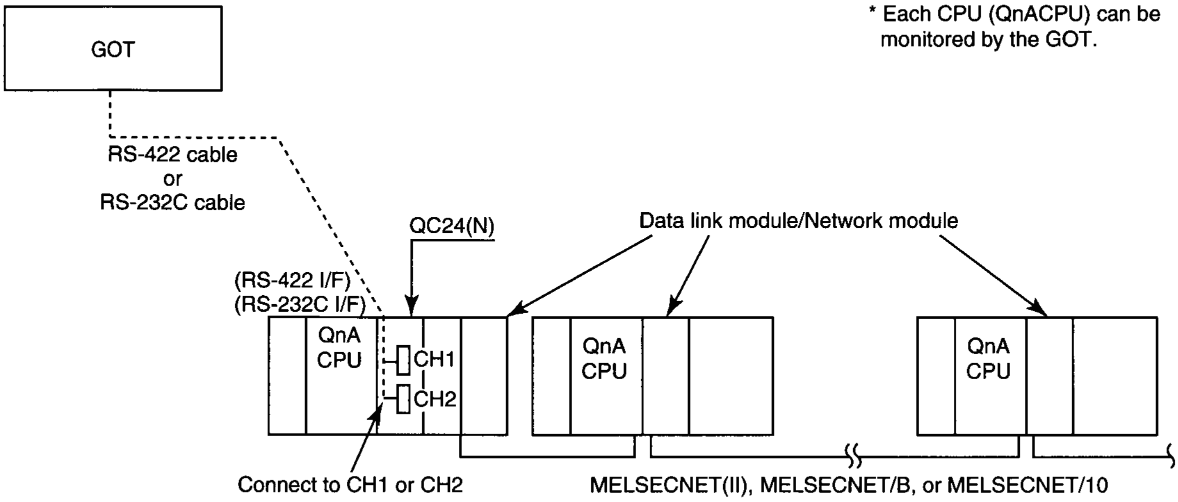
4.9.2 GOT connection

Connecting a GOT to the CH1 or CH2 interface of the QC24(N) allows the users to monitor the connected stations such as the QnACPU on the GOT screen.

This item explains the QC24(N) switch setting for monitoring the PLC using the GOT when the GOT is connected to the QC24(N).

For information regarding wiring details and GOT usage method, restriction details or operation method, see the GOT operating manual.

1 Example wiring



2 **QC24(N) setting**

① Switch setting

Switch (CH1)		Setting item	Set value (Setting contents)	Notes
Mode switch		Mode	5 (binary mode)	Dedicated protocol (format 5)
Station number switch		Station number	00	——
Transmission specifications switch				
	SW01	Operation setting	OFF (independent operation)	
	SW02	Data bits setting	ON (8 bit)	
	SW03	Parity bit enable/disable setting	ON (Enable)	
	SW04	Even parity/odd parity setting	OFF (odd parity)	
	SW05	Stop bit setting	OFF (1 bit)	
	SW06	Sum check enable/disable setting	ON (enable)	
	SW07	Write during RUN enable/disable setting	ON (enable)	
	SW08	Setting change enable/disable setting	OFF (disable)	
	SW09	Transmission rate setting	OFF	Set to 19,200 BPS
	SW10		ON	
	SW11		ON	
	SW12		OFF	
	SW13 to SW15	——	All OFF	These switches are on the left side of the module, as viewed from the front. (Large-type QC24 only)

② Buffer memory (special applications area) setting

- Leave the default values of the QC24(N) (See the table in Section 3.5) in the buffer memory special applications area for the channel used for GOT connection (CH1: 90H to 12FH, CH2: 130H to 1FFH).

3 **GOT usage limitations**

Following are the limitations when the GOT is connected to the QC24(N) and monitored.

① Connection possible QC24(N) interface

- Connectable to either of CH1 or CH2 interface. (Concurrent connection to both channels is not allowed.)
- A GOT and a peripheral for the GPP function cannot be connected at the same time. (If connected, data communication may not function properly.)

② Connection possible GOT

- See the manual of GOT used.

③ Usage possible GOT monitor functions

		Monitor function from user screen		System monitor function		Special module monitor function		Circuit monitor function	
		ACPU	QnACPU (Note 1)	ACPU	QnACPU (Note 2)	ACPU	QnACPU	ACPU	QnACPU
Computer link connection	Local station	——	o	——	o	——	×	——	×
	Remote station	o	o	o*1	o	×	×	×	

o: Usage possible ×: Usage not possible

*1 Usage T/C setting value could not be monitored or written. V/Z also cannot be written.

Note 1

- Depending on the device to be monitored, monitoring and writing cannot be done. (For details see the GOT Operating Manual (Monitor Screen Creation Edition) and the operating manual (Extension Function Edition).)

Note 2

- Depending on the device to be monitoring, monitoring and writing cannot be conducted. (For details see the GOT Operating Manual (Monitor Screen Creation Edition) and the operating manual (Extension Function Edition).)
- Device comments cannot be displayed for the registration monitor, batch monitor, or T/C monitor.

4.10 Maintenance and Inspection

The QC24(N) has no special inspection items other than below.

For items other than listed below, perform inspection according to the inspection items listed in the User's Manual of the PLC CPU module in order to always use the system in the optimal condition.

(QC24(N) inspection items)

① Check if the terminal resistors and cables are connected securely.

② Verify that the module installation screws and the terminal block installation screws are securely tightened.

POINT

Be sure to read through the Safety Precautions in the beginning of this manual regarding QC24(N) inspection and maintenance.

MEMO

DEDICATED PROTOCOLS

This section gives a general description of the various functions for using the dedicated protocols control procedures to transfer data between external devices and PLC CPU through serial communications. It also describes the contents of the command messages and the data communications procedure for each mode and format.

Chapter 5 describes the common items when the dedicated protocols are used in data communications. Read them first.

When using QnA frame and QnA extension frame format messages to transfer data, read Chapters 5 and 6.

When using QnA simplified frame format messages to transfer data, read Chapters 5 and 8.

When using A compatible frame format messages to transfer data, read Chapter 5 of this manual and Chapter 5 of the following manual.

- Computer Link/Multidrop Link Module User's Manual (Computer Link Function, Printer Function) SH-3511

When using the on-demand function, which transmits data from PLC CPU to external device, during dedicated protocol data communications, when transmitting data by user frame, read Chapter 5, Section 6.9, and Chapter 7.

(1) Some restrictions apply to the following functions that are described in the Dedicated Protocols. Read Section 1.4 before using these functions.

	Function name	**Section/Chapter**
1	Multiple block batch read/write	Section 6.2.10
2	Communication using QnA simplified frame	Chapter 8

(2) For communications via the dedicated protocol, be sure to read through the Safety Precautions in the beginning of this manual.

5. DATA COMMUNICATIONS USING DEDICATED PROTOCOLS

The dedicated protocols are data communications functions for sending command messages from external devices and reading and writing device data to and from the PLC and controlling the operation of the PLC.

These controls can be implemented by sending and receiving fixed format messages according to a fixed procedure.

To send data from the PLC CPU to external devices, a data communications sequence program is necessary.

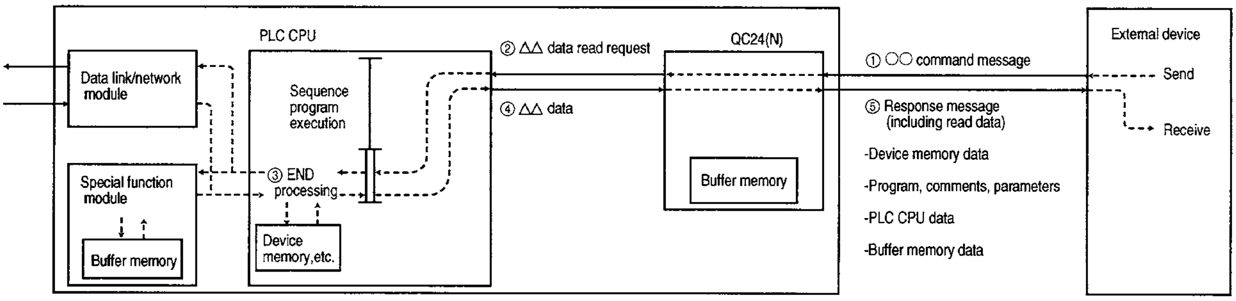
5.1 Dedicated Protocols PLC Access Timing

The following shows the PLC access timing when data read, write, status control, and other operations are performed from external device to PLC. (N) in the illustration shows the access processing flow order.

1 When an external device accesses the PLC CPU

- The PLC CPU accepts and processes the access request from the external device during END processing.
- Appendix 3 shows the number of scans of the PLC CPU required to process the request.

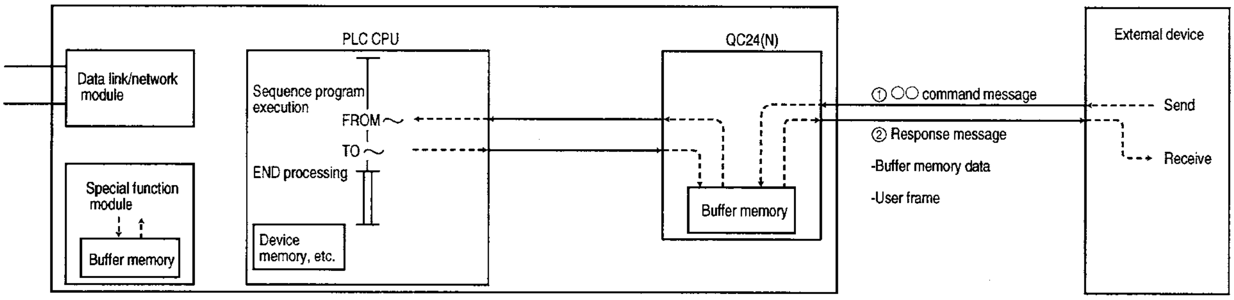
(Processing flow when an external device reads data)



2 When an external device accesses a QC24(N)

- The QC24 immediately accepts and processes the access request from the external device.
- This had no effect on the PLC CPU scan time.

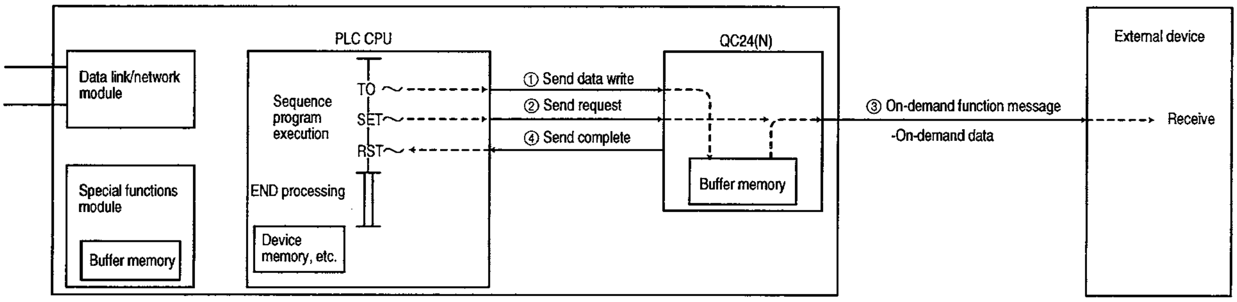
(Processing flow when an external device reads data)



3 When the PLC CPU uses the on-demand function to send data to an external device

The QC24(N) immediately accepts and processes the send request from the PLC CPU.

(Processing flow when on-demand data is sent to an external device)



5.2 Kinds of Modes and Data Communications Frames and Relationship of Accessible PLCs

The dedicated protocols have an ASCII mode, which transfers ASCII code data, and a binary mode, which transfers binary code data.

This section describes the data communications frames and commands of each mode.

1 Modes and data communications frames

① Four kinds of frames are available as data communications messages. Five formats are also available, depending on the contents of the data in the message and the message format.

② The frames and formats that can be used in each mode are shown below.

	Mode	Frame	Set mode number (*1)				
			Format 1	Format 2	Format 3	Format 4	Format 5
Dedicated protocol	ASCII mode	QnA frame	1	2	3	4	Un-available
		QnA extension frame					
		QnA simplified frame					
		A compatible frame					
	Binary mode	QnA extension frame	Unavailable				5

* 1 to 5 are the numbers set in the mode switch.

③ The PLC can be controlled by transferring messages of the frame matched to the external device specifications and communicating PLC CPU in the message format set in the mode switch.
For instance, if mode number 1 was set, an external device can send command messages in format 1 of any of the ASCII mode frames shown above.

④ There is no switch setting and setting to buffer memory for selecting the frame.
The QC24(N) judges the frame of the command message received from the external device and generates the response message to be sent to the external device in response to the command message.

⑤ Since the amount of data of binary mode QnA extension frame messages is about one half that of ASCII mode QnA extension frames, the transmission time is also shorter.

2 Commands

① There are three kinds of commands: QnA frames and QnA extension frames, QnA simplified fames, and A compatible frames.

② QnA extension frame commands are the same in the ASCII mode and binary mode. However, in the ASCII mode, commands are sent and received as ASCII code and in the binary mode, commands are sent and received as binary code.

③ Some A compatible frames cannot be used, depending on the PLC to be accessed.

POINT

1. This sections describes the format, commands and their functions, and accessible PLC of the QnA frame, QnA extension frame and QnA simplified frame.
   This manual and the following manuals describe the A compatible frame.

	Mode	Frame	Reference section	
			Frame	Commands and functions
Dedicated protocol	ASCII mode	QnA frame, QnA extension frame	Section 6.1.1, 6.1.2	Section 5.4.1, Chapter 6
		QnA simplified frame	Chapter 8	Section 5.4.2, Chapter 8
		A compatible frame		Section 5.4.3
			Computer Link/Multidrop Link Module User's Manual (Computer Function, Printer Function)	
	Binary mode	QnA extension frame	Section 6.1.3	Section 5.4.1, Chapter 6

2. To access another station's A series PLC with QC24(N), refer to section 5.10 for an overview of the method.

5.3 Application and Accessible Range of Each Frame

This section describes the applications of each frame that can be used during access between external device and PLC CPU using a dedicated protocol and the range of stations that can be accessed when an external device accesses a station other than a QC24(N) connection station.

5.3.1 Application and accessible range of QnA (extension) frame

1 **Application of QnA(extersion) frame**

① The main purpose of the QnA frame is to access all the devices and all the files of the QnACPU from an external device. Devices of PLC CPU other than the QnACPU can also be accessed.

② The QnA frame construction allows access to the PLC of other stations on a data link system and the PLC of other stations on a specific network system.

③ With the QnA extension frame, the PLC CPU connected via multi-drop can be accessed from the PLC CPU of another station through the network system. (Extended from the QnA frame.)

2 **Accessible range during QnA (extension) frame data communications**

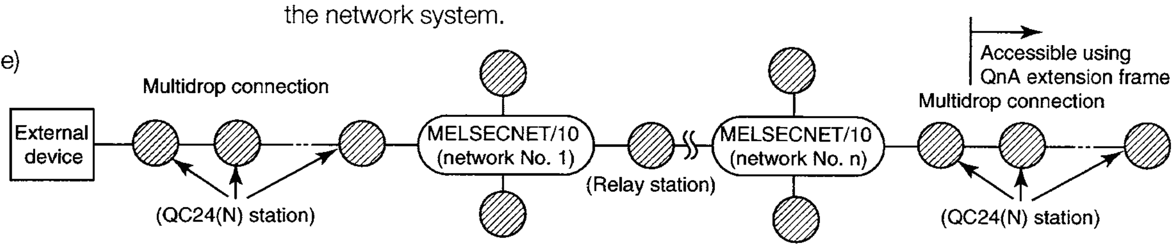
This section describes the basics of the stations that can be accessed when an external station accesses a station other than a QC24(N) station during QnA (extension) frame use.
The PLC of stations other than those shown below cannot be accessed.
See Section 5.3.4 for specific examples for each system.

▨ the illustrations indicates stations that can be accessed and ○ indicates stations that cannot be accessed.

① Access to PLC on MELSECNET/10

- All the PCs on an MELSECNET/10 containing QC24(N) stations connected to external devices.
- A MELSECNET/10 can access the PCs on another user-designated MELSECNET/10 using routing parameters setting to a relay station within the range of specifications of the network system.

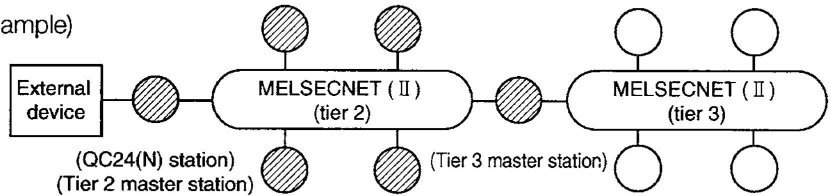
(Example)



② Access to PCs on MELSECNET(II) and MELSECNET/B

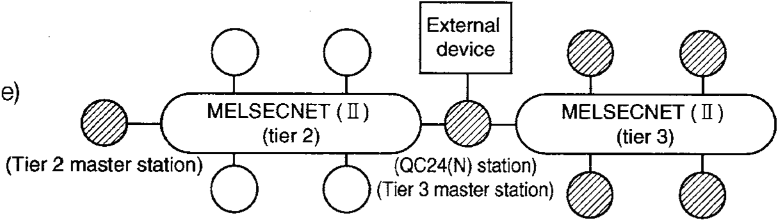
- The PCs on a MELSECNET(II) or MELSECNET/B containing QC24(N) stations connected to external devices can be accessed within the range of specifications of the data link system.

(Example)



* • When the external device connection station is the master station, the master station and each local station/remote station can be accessed.
• When the external device connection station is a local station, the connection station and master station can be accessed.
• The accessible range is also the same for the MELSECNET/B.

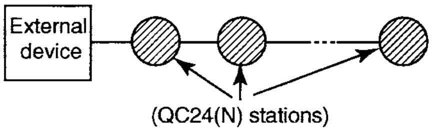
(Example)



③ Access to PLC CPU on multidrop connection

- A QC24(N) connected to an external device can use a multidrop connection to access the PLC CPU.

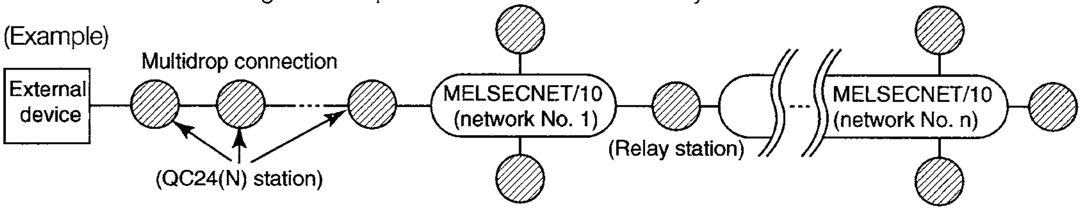
(Example)



④ Access to PLC CPU on designated MELSECNET/10 through multidrop connection station

- The PLC CPU on the user-designated MELSECNET/10 can be accessed through a multidrop connection station using routing parameter setting to a relay station within the range of the specifications of the network system.

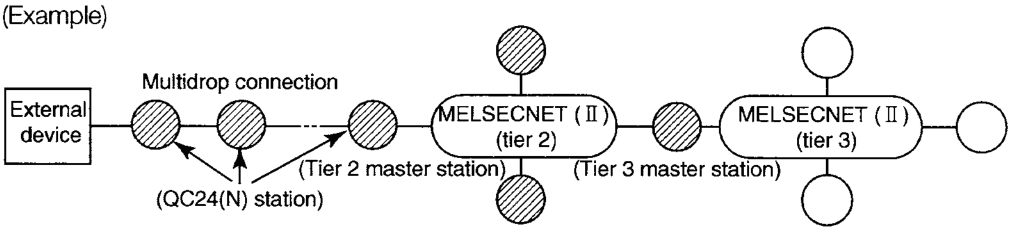
(Example)



⑤ Access to PLC on MELSECNET(II) or MELSECNET/B through multidrop connection station

- The PLC on a MELSECNET (II) or MELSECNET/B can be accessed within the range of specifications of the data link system through a multidrop connection station.

(Example)



- * When the multidrop connection station incorporated in the MELSECNET is the master station, the master station and each local station/remote station can be accessed.
- When the multidrop connection station incorporated in the MELSECNET is a local station, the connection station and master station/remote station can be accessed.
- The accessible range is also the same for the MELSECNET/B.

POINTS

(1) When accessing another station a QC24(N) (or computer link module) station on a data link system or network system, use the GPP function to preset the following parameters in the PLC CPU of the QC24(N) (or computer link module) station.

Setting module enabled for access from other stations...

Set during number of modules setting. Sets the modules that are to be passed through during access to another station.

(2) When the multidrop connection includes a computer link module, use the ASCII mode frames to access another station.

The binary mode QnA extension frame cannot be used to access another station through the included multidrop connection when accessing an external device connection station.

(3) External devices cannot access AOJ2CPU23/R23 and AOJ2P25/R25 stations on a data link system.

(4) Refer to the reference manual of each system for a detailed description of the range of access to another stations's PLC on a data link system or network system.

Applicable module	AJ71QC24			A1SJ71QC24		AJ71QC24N			A1SJ71QC24N	
	–	-R2	-R4	–	-R2	–	-R2	-R4	–	-R2
Function availability	×	×	×	×	×	○	○	○	○	○
Remark	–					–			–	

5.3.2 Application and accessible range of QnA simplified frame

1 Application of QnA simplified frame

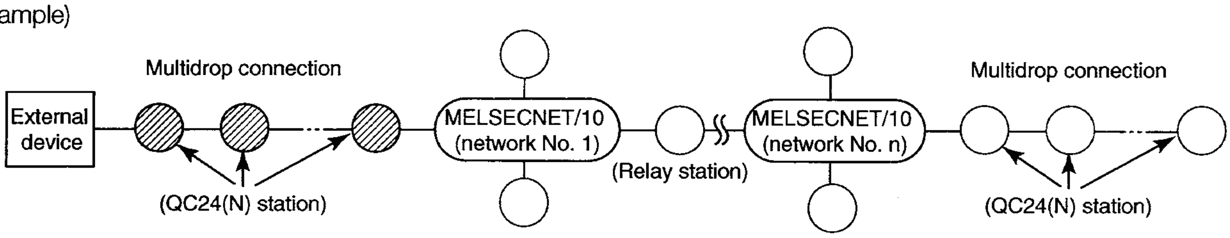
① In order to shorten the transfer time from external devices to the device memory of the QC24N installed station's QnACPU (local station), the message format is simplified in comparison with that of the QnA (extension) frame.

② Since the amount of transmission data is reduced, message processing on the external device side is made easier and the message transmission time is reduced.

2 Accessible range during communications using QnA simplified frame

This enables access to the QC24N installed station (local station) as well as other stations with QC24N installed via multi-drop connection.
The QnA simplified frame cannot access any terminals other than above.
The details will be explained in Chapter 8.

(Example)



5.3.3 Application and accessible range of A compatible frame

1 Application of A compatible frame

① The message construction is the same as that of the computer link module dedicated protocol.

② The external device data communications program written for the A Series PLC can be used. The same frame can be used to access multidrop connection, data link connection, and network connection QnACPU and PLC CPU other than the QnACPU.

However, there are the following restrictions.

- The QnACPU can access only devices with the same name as devices at the AnCPU, AnNCPU, AnACPU, and AnUCPU.
  Devices added to the QnACPU cannot be accessed.
- Since the device is designated by an ASCII code 5-digit/7-digit character string in each command (see Section 5.4.3), access is possible only within the range that can be designated.

2 Accessible range during communications using A compatible frame

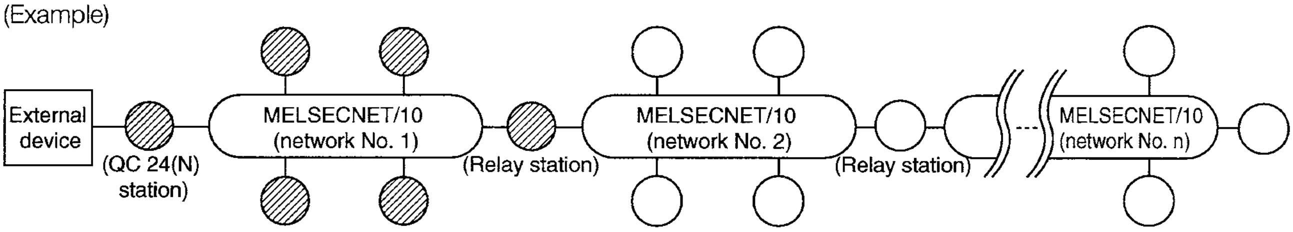
The following describes the basic approach to stations that can be accessed when an external device accesses a station other than a QC24(N) connection station.
Stations other than those shown below cannot be accessed.
See Section 5.3.4 for specific examples for each system.

▨ in the illustrations indicates stations that can be accessed and ○ indicates stations that cannot be accessed.

① Access to PLC on MELSECNET/10

- All the PLCs on an MELSECNET/10 containing QC24(N) stations connected to an external device can be accessed.

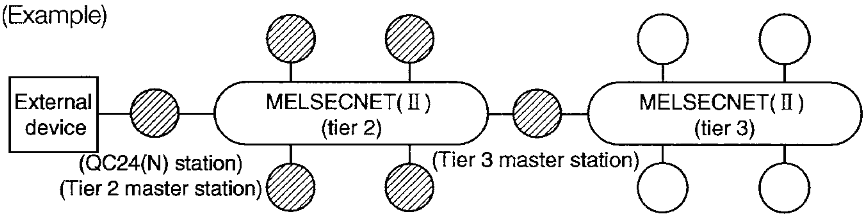
(Example)



② Access to PLC on MELSECNET (II) and MELSECNET/B

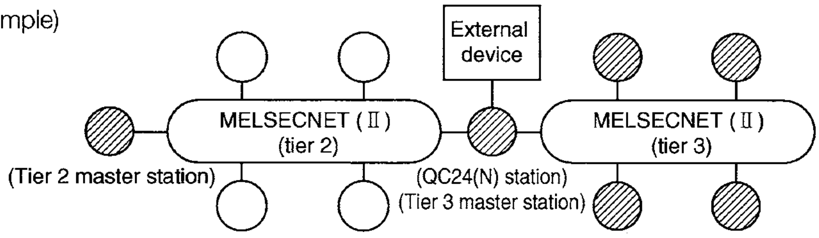
- Each PLC on an MELSECNET(II) or MELSECNET/B containing QC24(N) stations connected to an external device can be accessed within the range of the specifications of the data link system.

(Example)



* • When the station connected to the external device is the master station, the master station and each local station/remote station can be accessed.
- When the station connected to the external device is a local station, the connected station and the master station can be accessed.
- The accessible range is also the same for the MELSECNET/B.

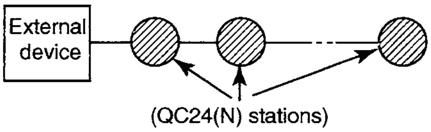
(Example)



③ Access to PLC CPU on multidrop connection

- A QC24(N) connected to an external device can access a multidrop connection PLC CPU.

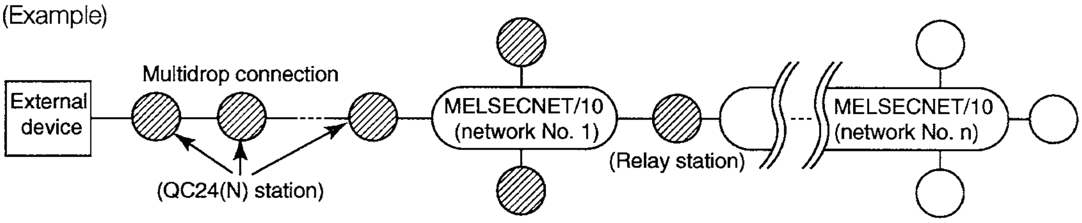
(Example)



④ Access to PLC on MELSECNET/10 through multidrop connection

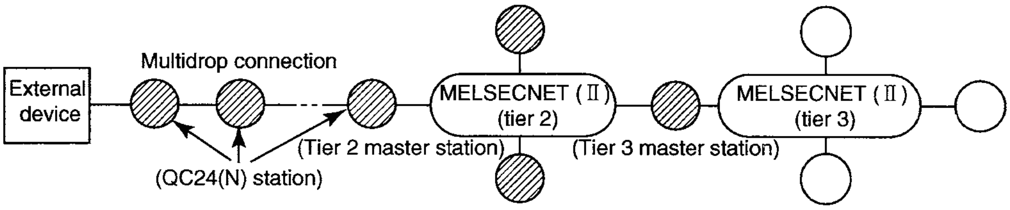
- A PLC on a MELSECNET/10 can be accessed through a multidrop connection within the range of specifications of the network system.

(Example)



⑤ Access to PLC on MELSECNET(II) or MELSECNET/B through a multidrop connection station

- A PLC on a MELSECNET(II) or MELSECNET/B can be accessed through a multidrop connection station within the range of specifications of the data link system.



- * When the multidrop connection station on the MELSECNET is the master station, the master station and each local station/remote station can be accessed.
- When the multidrop connection station on the MELSECNET is a local station, the connection station and master station can be accessed.
- The accessible range is also the same for the MELSECNET/B.

POINTS

(1) When accessing another station through a QC24(N) (or computer link module) station in a data link system or network system, preset the following parameter to the PLC CPU of the QC24(N) (or computer link module) station.

Setting module enabled for access from other stations...

Set during number of modules setting. Sets the modules to be passed through when accessing another station.

(2) External devices cannot access AOJ2CPUP23/R23 and AOJ2P25/R25 stations on a data link system.

(3) See the reference manual of each system for a detailed description of the range of access to the PLC of other stations on a data link system or network system.

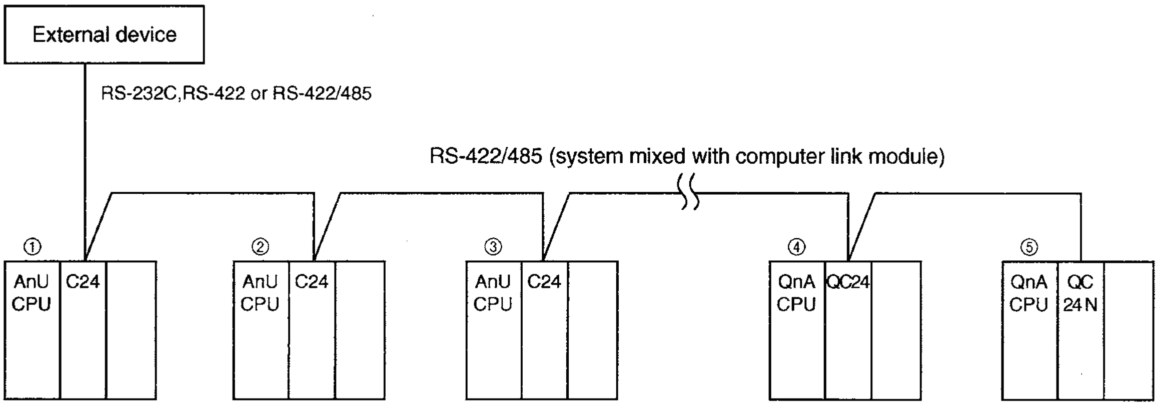
5.3.4 Examples of accessible range when each frame used

This section describes specific examples of the descriptions of Sections 5.3.1 to 5.3.3, including a computer link module, using multidrop connection, data link connection, and network connection.

(Example 1) Multidrop connection

The frames that can be used when the external device and PLC CPU system configuration is 1:n or m:n and the PLC CPU is multidrop connected through an RS-422/485 interface.

* The illustration below is for a 1:n connection.



Mode	Frame	Stations Accessible from External Devices				
		①	②	③	④	⑤
ASCII mode	QnA frame	×	×	×	○	○
	QnA extension frame	×	×	×	○	○
	QnA simplified frame	×	×	×	×	○
	A compatible frame	○	○	○	○	○
Binary mode	QnA extension frame	×	×	×	×	×

(Meaning of symbols in table)
○: Accessible
× : Unaccessible

POINTS

(1) For multidrop connection at QC24(N) only, each frame in the ASCII and binary modes can be used to access the PLC CPU.

(2) When the multidrop connection contains a computer link module, each frame in the ASCII mode can be used to access the PLC CPU. The binary mode QnA extension frame cannot be used to access the PLC CPU.

① Each frame of the ASCII mode can be used to access the QC24(N) PLC CPU.

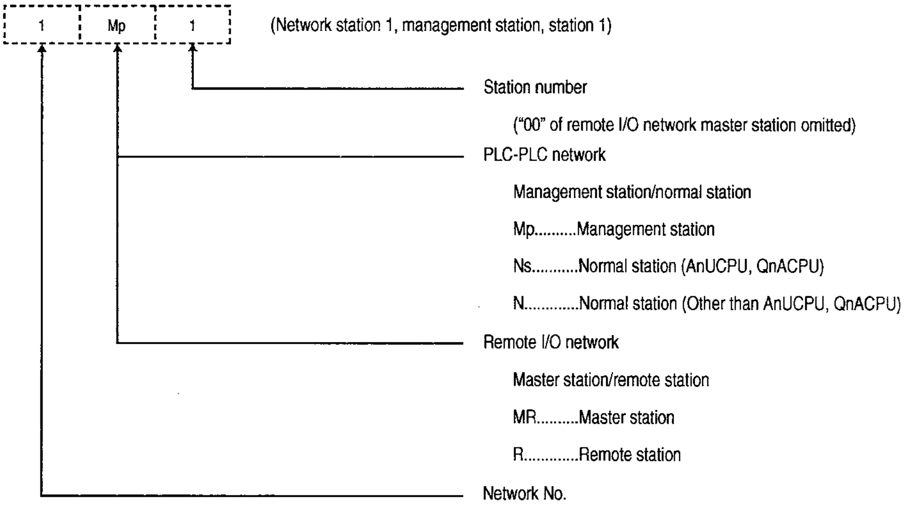
② The ASCII mode A compatible frame can be used to access a computer link module PLC CPU.
However, the commands that can be used differ with the computer link module installed in the accessed station. See Section 5.4.3.

(Example 2) Data link system connection and network system

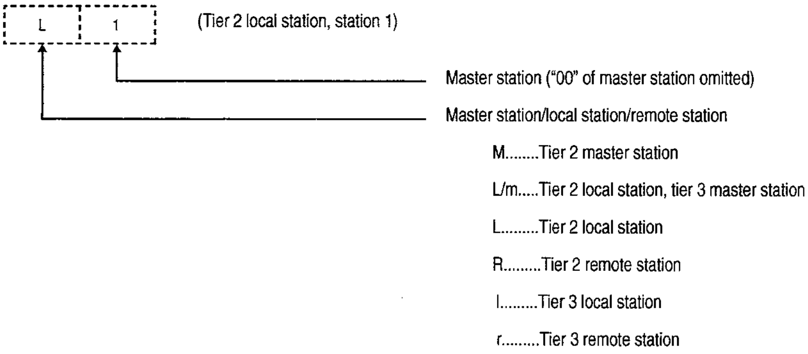
The following shows the frames that can be used when PLC CPU are connected by a data link system or network system.

The symbols of each station in the illustration are defined below.

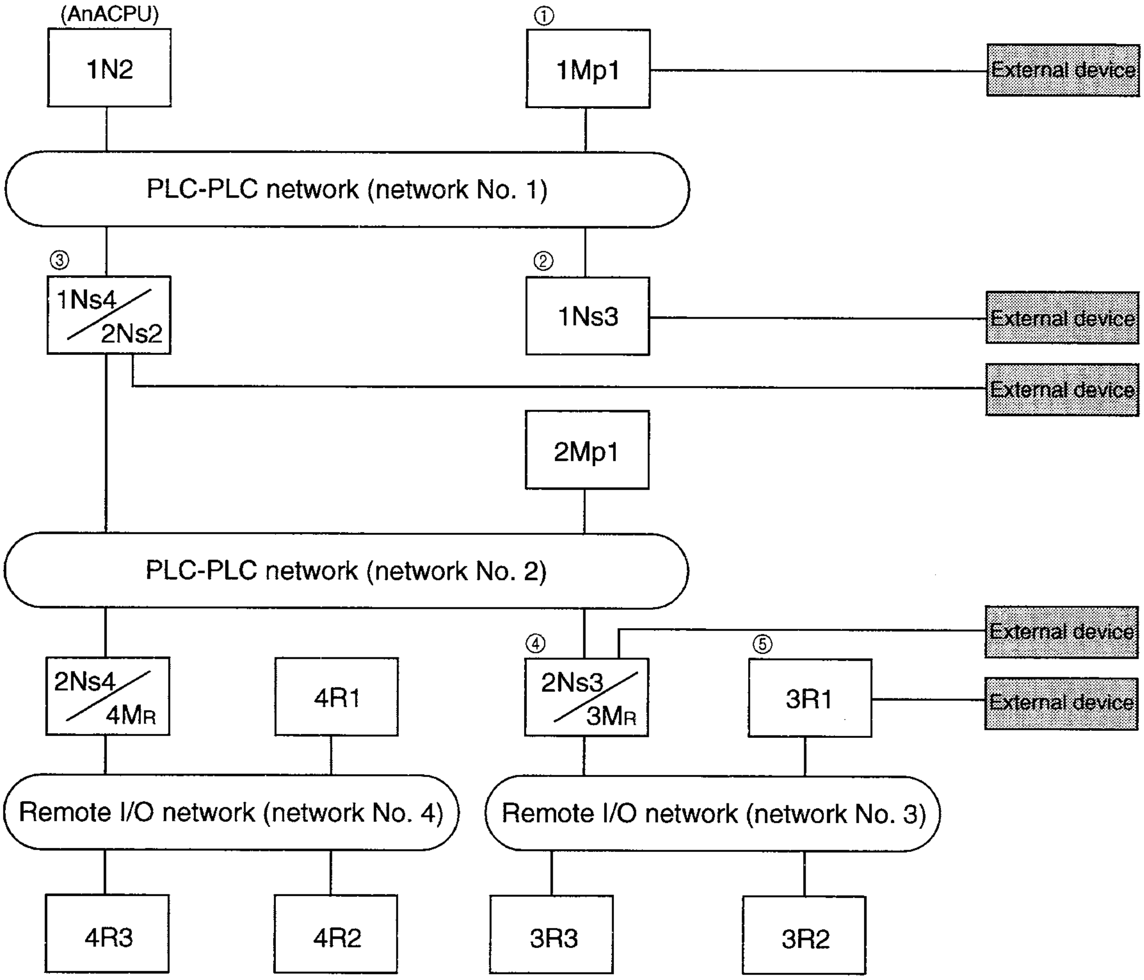
- MELSECNET/10



- MELSECNET(Ⅱ), MELSECNET/B



(a) When management stations/normal stations connected to external devices are all QnACPU



External device connection station	**Stations accessible from external device**												
	1Mp1	**1N2**	**1Ns3**	**1Ns4/2Ns2**	**2Mp1**	**2Ns3/3MR**	**2Ns4/4MR**	**3R1**	**3R2**	**3R3**	**4R1**	**4R2**	**4R3**
①	★	★	★	★	☆	☆	☆	☆	☆	☆	☆	☆	☆
②	★	★	★	★	☆	☆	☆	☆	☆	☆	☆	☆	☆
③	★	★	★	★	★	★	★	☆	☆	☆	☆	☆	☆
④	☆	☆	☆	★	★	★	★	★	★	★	☆	☆	☆
⑤	☆	☆	☆	☆	☆	★	☆	★	×	×	×	×	×

(Meaning of symbols in table)

★: Access using ASCII mode and binary mode QnA frame, QnA extension frame, and A compatible frame is possible.

☆: Access using ASCII mode and binary mode QnA frame and QnA extension frame is possible.

× : Unaccessible

(b) When QnACPU used as intermediate station of network system + data link system

**: Multidrop connection

QC24: QC24, QC24N

External device connection station	Stations accessible from external device															
	1Mp1	1Ns2	1Ns3 M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	⑤	⑦	⑨
①	△	△	△	△	×	×	×	×	×	×	×	○	×	×	×	×
②	△	△	△	△	×	×	×	×	×	×	×	×	○	×	×	×
③	★	★	★	★	☆	☆	☆	★	★	★	★	×	×	◇	×	◇
④	★	★	★	★	★	★	★	×	×	×	×	×	×	★	×	◇
⑤	★	★	★	★	★	★	★	×	×	×	×	×	×	★	×	◇
⑥	×	×	★	×	×	×	×	×	×	★	×	×	×	×	★	×
⑦	×	×	★	×	×	×	×	×	×	★	×	×	×	×	★	×
⑧	☆	☆	☆	★	×	×	★	×	×	×	×	×	×	◇	×	★
⑨	☆	☆	☆	★	×	×	★	×	×	×	×	×	×	◇	×	★

(Meaning of symbols in table)

★ : Access using ASCII mode and binary mode QnA frame, QnA extension frame, and A compatible frame is possible.

○ : Access using ASCII mode QnA frame, QnA extension frame, and A compatible frame is possible.

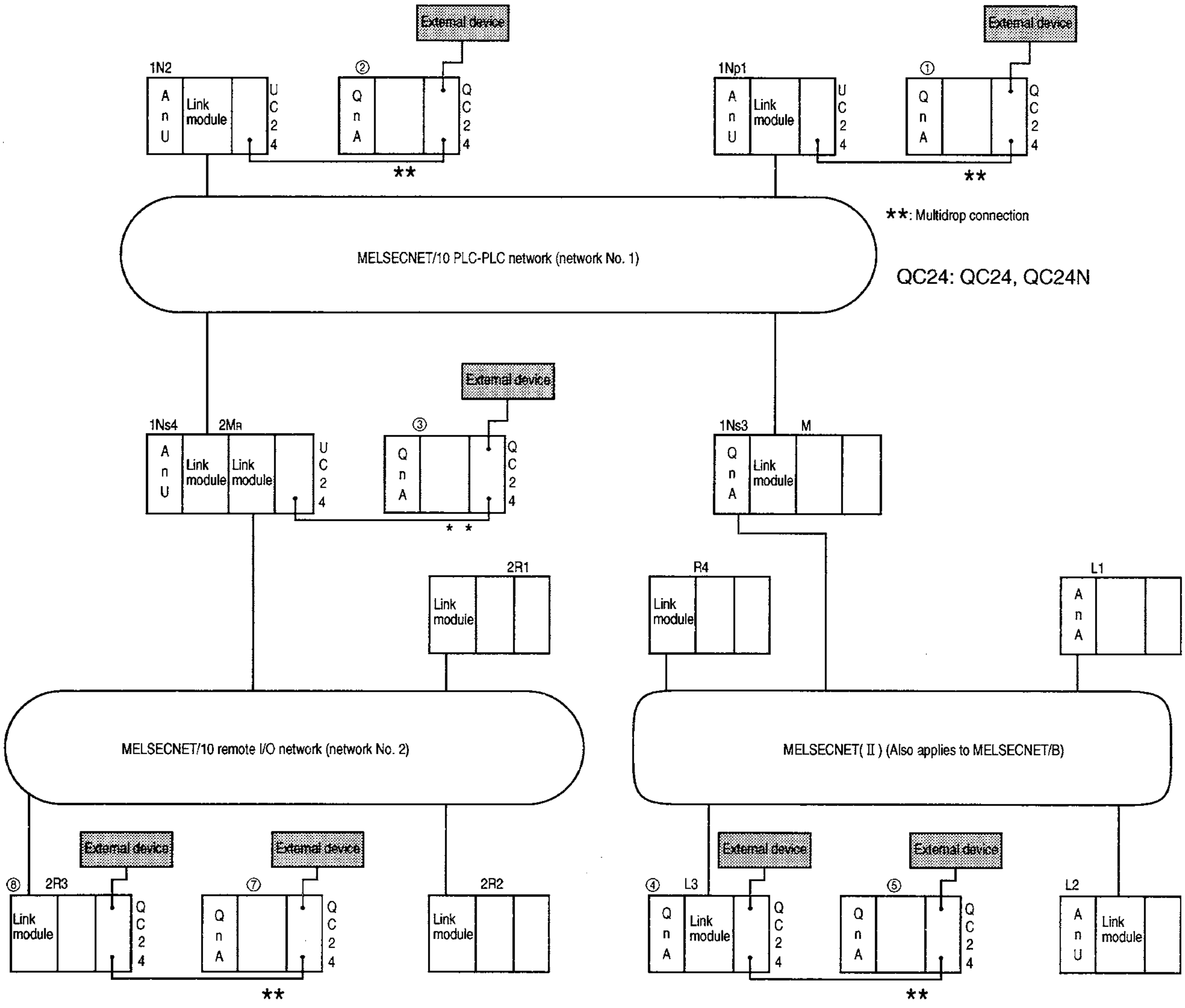
☆ : Access using ASCII mode and binary mode QnA frame and QnA extension frame is possible.

◇ : Access using ASCII mode and binary mode QnA extension frame is possible.

△ : Access using ASCII mode A compatible frame is possible.

× : Unaccessible

(c) When a PLC CPU other than a QnACPU is used as an intermediate station in a network system + data link system



**: Multidrop connection

QC24: QC24, QC24N

External device connection station	Stations accessible from external device															
	1Mp1	1Ns2	1Ns3 M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	③	⑤	⑦
①	△	△	△	△	×	×	×	×	×	×	×	○	×	×	×	×
②	△	△	×	×	×	×	×	×	×	×	×	×	○	×	×	×
③	△	△	△	△	△	△	△	×	×	×	×	×	×	○	×	×
④	×	×	△	×	×	×	×	×	×	★	×	×	×	×	★	×
⑤	×	×	△	×	×	×	×	×	×	★	×	×	×	×	★	×
⑥	×	×	×	△	×	×	★	×	×	×	×	×	×	×	×	★
⑦	×	×	×	△	×	×	★	×	×	×	×	×	×	×	×	★

(Meaning of symbols used in table)

★ : Access using ASCII mode and binary mode QnA frame, QnA extension frame, and A compatible frame is possible.

○ : Access using ASCII mode QnA frame, QnA extension frame, and A compatible frame is possible.

△ : Access using ASCII mode A compatible frame is possible.

× : Unaccessible

5.4 Dedicated Protocol Commands and Functions Tables

The following uses tables to show the commands and functions for an external device to access the PLC by dedicated protocol.

5.4.1 QnA frame and QnA extension frame commands

The following describes the commands and functions when an external device uses the QnA frame or QnA extension frame to access the PLC.

The □ part of [Subcommand] in the table depends on the designated device and how the command function is used. Regarding the □ part, see the description of the relevant command of Section 6.

Of these commands, the commands for access to device memory can also be used to access PLC CPU other than the QnACPU. (Except multiple block batch read/write command)

Function			Command (Subcommand) * ASCII-mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal number.	Processing contents	Number of points processed per communication	
					Access station-1*7	Access station-2*8
Device memory	Batch read	Bit units	0401 (00□1)	Reads bit devices (X, Y, M, etc.) in units of points.	3952 points	256 points
		Word units	0401 (00□0)	Reads bit devices (X, Y, M, etc.) in units of 16 points.	480 words (7680 points)	32 words (512 points)
				Reads word devices (D, R, T, C, etc.) in units of points.	480 points	64 points
	Batch write	Bit units	1401 (00□1)	Writes to bit devices (X, Y, M, etc.) in units of points.	3952 points	160 points
		Word units	1401 (00□0)	Writes to bit devices (X, Y, M, etc.) in units of 16 points.	480 words (7680 points)	10 words (160 points)
				Writes to word devices (D, R, T, C, etc.) in units of points.	480 points	64 points
	Random read	Word units	0403 (00□0)	Reads bit devices (X, Y, M, etc.) in units of 16 bits and 32 bits by designating the devices and device numbers.	96 points	10 words (160 points)
				Reads word devices (D, R, T, C, etc.) in units of points and 2 points by designating the devices and device numbers.		10 points
	Test [Random write]	Bit units	1402 (00□1)	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	94 points	20 points
		Word units	1402 (00□0)	Sets/resets sbit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at random.	960 points	10 words (160 points)
				Writes word devices (D, R, T, C, etc.) in units of points and 2 points by designating the devices and device numbers at random. However, only units of points is possible for other than the QnACPU.		10 points
	Monitor data registration	Word units	0801 (00□0)	Registers bit devices (X, Y, M, etc.) to be monitored in units of 16 points.*2	96 points	20 words (320 points)
				Registers word devices (D, R, T, C, etc.) to be monitored in units of points or 2 points. However, only units of points is possible for other than QnACPU.		20 points
	Monitor	Word units	0802 (0000)	Monitors the devices with monitor data registered.	(Number of registered points)	
	Multiple block batch read	Word units	0406 (00□0)	Read and write data by treating n points of word devices or bit devices (one points is equivalent to 16 bits) as one block, or by designating multiple blocks randomly.	480 points	(Unavailable)
	Multiple block batch write	Word units	1406 (00□0)		480 points	(Unavailable)
Buffer memory*3	Batch read		0613 (0000)	Reads the buffer memory of the QC24(N) connected to an external device. Can also be used for data communications between PLC CPU and external devices.	480 words (960 bytes)	(Unavailable)
	Batch write		1613 (0000)	Writes data to the buffer memory of QC24(N) connected to an external device.		
Special function module	Batch read		0601 (0000)	Reads the Special Function Module buffer memory data.	960 bytes (See Section 6.3 for information regarding the access station.)	
	Batch write		1601 (0000)	Writes the data to the Special Function Module buffer memory.		

	PLC CPU that can execute commands															PLC CPU status*1			Reference section
	A0J2	A0J2 H	A1, A1N	An(N) (Other than written left), AnS	A3H, A3M	A2C, A52G A2CJ	AnA	AnU	AJ72 P25/ R25	AJ72 (Q)LP 25/ (Q)BR 15	Q2A, Q2AS, Q2ASH (S1)	Q3A	Q4A, Q4AR	A73	A7L MS-F	During STOP	During RUN		
																	Write enable set	Write disable set	
	○								×		○			○		○	○	○	Section 6.2.1 Section 6.2.2 Section 6.2.3
	○								×		○			○					
	○								×		○			○					
	○								×		○*4			○		○	○	×	Section 6.2.1 Section 6.2.4 Section 6.2.5
	○								×		○*4			○					
	○								×		○*4			○					
	×								×		○			×		○	○	○	Section 6.2.1 Section 6.2.6
	×								×		○			×					
	○								×		○*4			○		○	○	×	Section 6.2.1 Section 6.2.7 Section 6.2.8
	○								×		○*4			○					
	○								×		○*4			○					
	×								×		○			×		○	○	○	Section 6.2.1 Section 6.2.9
	×								×		○			×					
	×								×		○			×		○	○	○	
	×								×		○*9			×		○	○	○	Section 6.2.1 Section 6.2.10
	×								×		○*9			×		○	○	×	
	——															○	○	○	Section 6.3
	——															○	○	○	
	×										○			×		○	○	○	
	×										○			×		○	○	×	

Function			Command (Subcommand) * ASCII-mode: Designated by ASCII code. Binary mode: Each is designated as a hexa-decimal number.	Processing contents	Number of points processed per communication	
					Access station-1*7	Access station-2*8
PLC CPU	Remote RUN		1001(0000)	Issues a remote RUN request to the PLC CPU	(1 station)	(Unavailable)
	Remote STOP		1002(0000)	Issues a remote STOP request to the PLC CPU.	(1 station)	
	Remote PAUSE		1003(0000)	Issues a remote PAUSE request to the PLC CPU.	(1 station)	
	Remote latch clear		1005(0000)	Issues a remote latch clear request to the PLC CPU when the PLC CPU is in the STOP state.	(1 station)	
	Remote RESET		1006(0000)	Issues a remote RESET request to the PLC CPU to clear the state that stopped the PLC CPU due to an error.	(1 station)	
Drive memory	Memory usage status read		0205(0000)	Reads the drive cluster usage status.	[256 clusters]	
	Memory defragmentation		1207(0000)	Defragments the drive memory and increases the contiguous vacant area. (File storage location defragmentation)	(1 station)	
File	File information table read	No header statement	0201(0000)	Reads the file table (filename, date of last updating, file size).	(36 files)	
		Header statement	0202(0000)	Reads the file table (file header statement, filename, date of last updating, file size).	(16 files)	
		File No. usage status	0204(0000)	Reads the file No. usage status.	(256 files)	
	File information modification	Date and time file last updated	1204(0000)	Changes the date and time the file was last up-dated.	(1 file)	
		Filename, size modification	1204(0001)	Changes the filename and file size.	(1 file)	
		Batch modification	1204(0002)	Changes the filename, file size, and data and time the file was last updated.	(1 file)	
	File search		0203(0000)	Reads whether or not the designated file exits, the file No., and the file size.	(1 file)	
	File contents read		0206(0000)	Reads the file contents.	960 bytes	
	New registration (filename registration)		1202(0000)	Reserves a file area with the designated filename.	(1 file)	
	File contents write	Arbitrary data	1203(0000)	Writes the designated data (n bytes) to a file.	960 bytes	
		Same data (FILL)	1203(0001)	Writes n bytes of the designated data (1 word) to a file.	[File size]	

	PLC CPU that can execute commands															PLC CPU status*1			Reference section
	A0J2	A0J2 H	A1, A1N	An(N) (Other than written left), AnS	A3H, A3M	A2C, A52G, A2CJ	AnA	AnU	AJ72 P25/ R25	AJ72 (Q)LP 25/ (Q)BR 15	Q2A, Q2AS, Q2ASH (S1)	Q3A	Q4A, Q4AR	A73	A7L MS-F	During STOP	During RUN		
																	Write enable set	Write disable set	
	×										○*4			×		○	○	○	Section 6.4
	×										○*4			×					
	×										○*4			×					
	×										○*4			×		○	×	×	
	×										○*4			×		○	×	×	
	×										○			×		○	○	○	Section 6.5
	×										○*4,5			×		○	×	×	
	×										○			×		○	○	○	Section 6.6.1 to Section 6.6.4
	×										○			×					
	×										○			×					
	×										○*4,6			×		○	○	×	Section 6.6.1 to Section 6.6.3 Section 6.6.5
	×										○*4,6			×					
	×										○*4,6			×					
	×										○			×		○	○	○	Section 6.6.1 to Section 6.6.3 Section 6.6.6
	×										○*6			×		○	○	○	Section 6.6.1 to Section 6.6.3 Section 6.6.7
	×										○*4,6			×		○	○	×	Section 6.6.1 to Section 6.6.3 Section 6.6.8
	×										○*4,6			×		○	○	×	Section 6.6.1 to Section 6.6.3 Section 6.6.9
	×										○*4,6			×					

Function		Command (Subcommand) * ASCII-mode: Designated by ASCII code. Binary mode: Each is designated as a hexa-decimal number.	Processing contents	Number of points processed per communication	
				Access station-1*7	Access station-2*8
File	File lock registration/clear	0808 (000□)	Registers file lock so that the contents cannot be changed while the designated file is being accessed. Or clears the registration.	(1 file)	(Unavailable)
	File copy	1206 (0000)	Writes (copies) the contents of an existing file to a newly registered file.	480 bytes	
	File delete	1205 (0000)	Deletes a file.	(1 file)	
User frame *3	Registered data read	0610 (0000)	Reads the registered data of the designated frame.	80 bytes	(Unavailable)
	Data registration	1610 (0000)	Registers (writes) the data list of the first frame/last frame when data is transferred in user format message format.		
	Registered data delete	1610 (0001)	Deletes the registered data of the designated frame No.	(1 data)	
Global*3		1618 (000□)	Turns the global signals (X1A/X1B) to the QC24 (N)QnACPU ON/OFF.	(1 station/ all stations)	(Unavailable)
On-Demand		2101 (—)	Reads send requests from the PLC CPU and sends data to an external device. Data of the maximum area size of the contiguous vacant area in the user area of the QC24(N) buffer memory can be sent. (When system configuration is 1:1)	(Item at the left.)	
Transmission sequence initialize (Binary mode only)*3		1615 (0000)	Terminates the current processing request and places the QC24(N) into the command receive wait state.	(1 station)	
Mode switching *3		1612 (0000)	Switches the operation mode and transmission specifications of the designated interface.	(1 station)	
LED OFF, Error code initialize *3		1617 (000□)	Turns off the display error LED and initializes the error code.	(1 station)	
Loopback test *3		0619 (0000)	Checks if data communications between QC24(N) and external devices is normal. (For connection status and communications functions check)	960 bytes (Only connected stations can communicate)	

	PLC CPU that can execute commands														PLC CPU status*1			Reference section
	A0J2	A0J2H	A1, A1N	An(N) (Other than written left), AnS	A3H, A3M	A2C, A52G, A2CJ	AnA	AnU	AJ72P25/R25	AJ72(Q)LP25/(Q)BR15	Q2A, Q2AS, Q2ASH (S1)	Q3A	Q4A, Q4AR	A73	A7LMS-F	During STOP	During RUN		
																	Write enable set	Write disable set	
	×										○			×		○	○	○	Section 6.6.1 to Section 6.6.3 Section 6.6.10
	×										○*4,6			×		○	○	○	Section 6.6.1 to Section 6.6.3 Section 6.6.11
	×										○*4,6			×		○	○	×	Section 6.6.1 to Section 6.6.3 Section 6.6.12
	–															○	○	○	Section 6.7, Chapter 16
	–															○	○	○	
	–															○	○	○	
	×										○			×		○	○	○	SEction 6.8
	×										○			×		○	○	○	Section 6.9, Chapter 7
	–															○	○	○	Section 6.10
	–															○	○	○	Section 6.11, Chapter 18
	–															○	○	○	Section 6.12
	–															○	○	○	Section 6.13

○: Command executable △: Command executable with conditions ×: Command not executable –: Access to QC24(N)

*1 QC24(N) DIP switch SW07 sets Write During RUN Enable/Disable to the PLC CPU.

SW07=ON......Enable Write During RUN, SW07=OFF......Disable Write During RUN

*2 For PLC CPU other than the A3HCPU, AnA/AnU/QnACPU, device X (input) is two processing points per point.
When the designated device includes X, make the number of points processed per communication ≤ ((X designated points X 2) + other device designated points).
When only X is designated, the number of points processed per communication becomes one half the value given in the table.

*3 Commands can be executed only for QC24(N) connected to an external device (including multidrop connected station) or other QnACPU of other QC24(N) stations.
Commands cannot be executed for the PLC of other stations over a data link system or network system.

*4 If system protect (system protect switch SW05: ON) is applied to an QnACPU that executes commands, the QC24(N) will recognize an error and return a NAK message to the external device.

*5 When registering data write/read keywords to a QnACPU that executes commands, designate the same keywords in the command message.
If the keywords do not match, the QC24(N) will recognize and return a NAK message to the external device.

*6 When registering data write/read keywords to the relevant QnACPU when executing commands for program files and parameter files, designate the same keywords in the command message.
If the keywords do not match, the QC24(N) will recognize an error and an return a NAK message.

*7 [Access Station-1] indicates the number of processing points when accessing any of the following stations.

① QC24(N) QnACPU station connected to an external device/MELSECNET/10 remote I/O station
② QnACPU station multidrop-connected to the QC24(N) of ① above
③ QnACPU of ① and ② above and QnACPU/remote I/O station connected over a MELSECNET/10

*8 [Access Station-2] indicates the number of processing points when stations other than those of *7 above are accessed.

(Examples)

① PLC CPU station other than QnACPU
② PLC CPU station/remote I/O station connected over an MELSECNET(II) or MELSECNET/B

*9 Multiple block batch read and write may be performed on the QnACPU explained in Section 1.4.

Applicable module	AJ71QC24			A1SJ71QC24		AJ71QC24N			A1SJ71QC24N	
	–	-R2	-R4	–	-R2	–	-R2	-R4	–	-R2
Function availability	×	×	×	×	×	○	○	○	○	○
Remark	–					–			–	

5.4.2 QnA simplified frame commands

The following describes the commands and functions when an external device uses QnA simplified frame to access the QnACPU.

All of the commands are used for reading and writing data from/to the device memory of the QC24N installed station's QnACPU (local station) using the dedicated protocol.

Function		Command	Processing contents	Number of points processed per communication	PLC CPU status*1		
					During STOP	During RUN	
						Write enable set	Write disable set
Batch read	Bit units	1	Reads bit devices in units of points. (1 point = 1 bit)	3952 points	○	○	○
	Word units	2	Reads bit devices in units of points. (1 point = 16 bits)	480 points			
			Reads word devices in units of points.				
Batch write (*2)	Bit units	3	Writes to bit devices in units of points. (1 point = 1 bit)	3952 points	○	○	×
	Word units	4	Writes to bit devices in units of points. (1 point = 16 bits)	480 points			
			Writes to word devices in units of points.				
Random read	Word units	5	Reads bit devices in units of points by designating the devices and device numbers at random. (1 point = 16 bits)	96 points	○	○	○
			Reads word devices in units of points by designating the devices and device numbers at random.				
Test [Random write] (*2)	Bit units	6	Writes to bit devices in units of points by designating the devices and device numbers at random. (1 point = 1 bit)	94 points	○	○	×
	Word units	7	Writes to bit devices in units of points by designating the devices and device numbers at random. (1 point = 16 bits)	960 points			
			Writes to word devices in units of points by designating the devices and device numbers at random.				
Monitor data registration (*3)	Word units	8	Registers bit devices to be monitored in units of points. (1 point = 16 bits)	96 points	○	○	○
			Registers word devices to be monitored in units of points.				
Monitor (*3)	Word units	9	Monitors the devices with monitor data registered.	(Number of registered points)			

*1 QC24N transmission specification switch SW07 sets Write During RUN Enable/Disable to the PLC CPU.

SW07 = ON .... Write enable during RUN

SW07 = OFF ...... Write disable during RUN

*2 When the system protect is active (system protect switch SW05=ON) for the QnACPU which executes the command, an error occurs and a NAK message is returned.

*3 The procedure for monitoring is the same as that for monitoring the exchange by the QnA (extension) frame.

5.4.3 A compatible frame commands, accessible devices, and reference manuals

The following describes the commands and functions when an external device uses an A compatible frame to access the PLC.

The A compatible frame commands are the same as the commands supported by the computer link module.

1 Usable commands

Function			Command		Processing contents	Number of points processed per communications
			Symbol	ASCII Code		
Device memory	Batch read	Bit units	BR JR	42H, 52H 4AH, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points
		Word units	WR	57H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)
			QR	51H, 52H	Reads word devices (D, R, T, C, etc.) in units of points.	64 points
	Batch write	Bit units	BW JW	42H, 57H 4AH, 57H	Writes to bit devices (X, Y, M, etc.) in units of points.	160 points
		Word units	WW	57H, 57H	Writes to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)
			QW	51H, 57H	Writes to word devices (D, R, T, C, etc.) in units of points.	64 points
	Test [Rwdom write]	Bit units	BT JT	42H, 54H 4AH, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of bits.	20 points
		Word units	WT	57H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers.	10 words (160 points)
			QT	51H, 54H	Writes to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers.	10 points
	Monitoring data registration *4	Bit units	BM JM	42H, 4DH 4AH, 4DH	Registers the bit devices (X, Y, M, etc.) to be monitored in units of points. *2	40 points
		Word units	WM	57H, 4DH	Registers bit devices (X, Y, M, etc.) to be monitored in units of 16 points.*2	20 words (320 points)
			QM	51H, 4DH	Registers word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points
	Monitoring	Bit units	MB MJ	4DH, 42H 4DH, 4AH	Monitors devices with monitoring data registered.	—
		Word units	MN MQ	4DH, 4EH 4DH, 51H		
Special function module	Batch read		TR	54H, 52H	Reads the Special Function Module buffer memory data.	128byte
	Batch write		TW	54H, 57H	Writes the data to the Special Function Module buffer memory.	
Extension file register	Batch read		ER	45H, 52H	Reads extension file registers (R) in units of points.	64 points
	Batch write		EW	45H, 57H	Writes to extension file registers (R) in units of points.	64 points
	Test (Random write)		ET	45H, 54H	Writes to extension file registers (R) in units of points.	10 points
	Monitor data registration *4		EM	45H, 4DH	Registers extension file registers (R) to be monitored in units of points.	20 points
	Monitor		ME	4DH, 45H	Monitors extension file registers (R) with monitor data registered.	—
	Direct read	Word units	NR	4EH, 52H	Reads extension file registers (R) in units of points by designating the device No. by serial number without being aware of the extension file register block No.	64 points
	Direct write	Word units	NW	4EH, 57H	Writes to extension file registers (R) by designating the device No. by serial number without being aware of the extension file register block No.	64 points

	PLC CPU that can execute commands															PLC CPU status*1			Reference section*3
	A0J2	A0J2 H	A1, A1N	An(N) (Other than written left), AnS	A3H, A3M	A2C, A52G, A2CJ	AnA	A2U	AJ72 P25/ R25	AJ72 (Q)LP 25/ (Q)BR 15	Q2A, Q2AS, Q2ASH (S1)	Q3A	Q4A, Q4AR	A73	A7L MS-F	During STOP	During RUN		
																	Write enable set	Write disable set	
	○								×		○			○		○	○	○	Section 5.7.2
	○								×		○			○		○	○	○	Section 5.7.3
	○								×		○			○		○	○	×	Section 5.7.4
	○								×		○			○		○	○	×	Section 5.7.5
	○								×		○			○		○	○	×	Section 5.7.6
	○								×		○			○		○	○	○	Section 5.7.7
	○								×		○			○		○	○	○	Section 5.7.8 2
	○								×		○			○		○	○	○	
	○								×		○			○		○	○	○	Section 5.7.8 3
	○								○		×			○		○	○	○	Section 5.10.3
	○								○		×			○		○	○	×	Section 5.10.4
	×	○	×	○					×					○		○	○	○	Section 5.8.4
	×	○	×	○					×					○		○	○	×	Section 5.8.5
	×	○	×	○					×					○		○	○	×	Section 5.8.8
	×	○	×	○					×					○		○	○	○	Section 5.8.9 2
	×	○	×	○					×					○		○	○	○	Section 5.8.9 3
	×	○	×	○					×					○		○	○	○	Section 5.8.6
	×	○	×	○					×					○		○	○	×	Section 5.8.7

*1 QC24(N) DIP switch SW07 sets Write During RUN Enable/Disable to the PLC CPU.
SW07=ON......Write During RUN Enable, SW07=OFF......Write During RUN Disable

*2 For PLC CPU other than the A3HCPU, AnA/AnU/QnACPU, device X (input) becomes the number of two points processed per one point. When the designated device includes X, set the following:
((X designated points) + other device designated points) ≤ number of points processed per communication
When only X is designated, the number of points processed per communication is one half the value shown in the table.

*3 The Reference Section in the table is the number of the description section of the following manual:
Computer Link Module/Multidrop Link Module User's Manual (Computer Link Function, Printer Link Function)......SH-3511

*4 The devices that can be registered to the QC24(N) is 1 command for each interface.

2 Devices that can be accessed

① Only devices present among AnCPU, AnNCPU, AnACPU, and AnUCPU, and devices with the same name can access QnACPU (exceptions are below).
The devices listed below can not be accessed from an external device.

- Devices that were added by QnACPU
- Latch relay (L) or Step relay (S)
  * In the case of QnACPU, the latch relay (L) and step relay (S) are separate from the internal relay (M). However, you can designate either one to access the internal relay.
- File register (R)

② Since the device to be accessed is designated in each command by an ASCII code 5-digit/7-digit character string, PLC CPU can only be accessed within the range that can be designated.

<table>
<tr><th colspan="9">QnACPU accessible devices (Access using a compatible command)......When parameters setting is default</th></tr>
<tr><th>Class</th><th>Device</th><th>Device Number (Designation range)</th><th>Decimal/ hexadecimal expression</th><th>Class</th><th colspan="2">Device</th><th>Device number (Designation range)</th><th>Decimal/ hexadecimal expression</th></tr>
<tr><td rowspan="9">Internal User Device</td><td>Input relay</td><td>X0 to X1FFF</td><td rowspan="2">Hexadecimal</td><td rowspan="7">Internal User Device</td><td rowspan="3">Timer</td><td>Contacts</td><td>TS0 to TS2047</td><td rowspan="9">Decimal</td></tr>
<tr><td>Output relay</td><td>Y0 to Y1FFF</td><td>Coil</td><td>TC0 to TC2047</td></tr>
<tr><td rowspan="3">Internal relay</td><td rowspan="3">M0 to M8191</td><td rowspan="3">Decimal</td><td>Current value</td><td>TN0 to TN2047</td></tr>
<tr><td rowspan="4">Counter</td><td>Contacts</td><td>CS0 to CS1023</td></tr>
<tr><td>Coil</td><td>CC0 to CC1023</td></tr>
<tr><td>Link relay</td><td>B0 to B1FFF</td><td>Hexadecimal</td><td rowspan="2">Current value</td><td rowspan="2">CN0 to CN1023</td></tr>
<tr><td>Annunciator</td><td>F0 to F2047</td><td rowspan="2">Decimal</td></tr>
<tr><td>Data register</td><td>D0 to D12287</td><td rowspan="2">Internal System Device</td><td colspan="2">Special relay *1</td><td>M9000 to M9255</td></tr>
<tr><td>Link register</td><td>W0 to W1FFF</td><td>Hexadecimal</td><td colspan="2">Special register *2</td><td>D9000 to D9255</td></tr>
</table>

*1 M9000 to M9255 designations access SM1000 to SM1255.
*2 D9000 to D9255 designations access SD1000 to SD1255.

3 Reference manuals

① This manual only describes the QnA (extension) frame and QnA simplified frame commands from among the commands that can be used by the QC24(N).

② When using A compatible frame commands, see Section 5 of this manual and to the following manual:

Computer Link/Multidrop Link Module User's Manual (Computer Function, Printer Function). ... SH-3511
Section 5.4... Describes the control procedure and message designation items when communicating between external device and QC24(N).
Section 5.7 ... Describe the device memory read and write methods.

* When seeing the Computer Link/Multidrop Link Module User's Manual, reread the description terms as follows:
Computer .... External device, Computer link module...............QC24(N)

5.5 Buffer Memory Read/Write

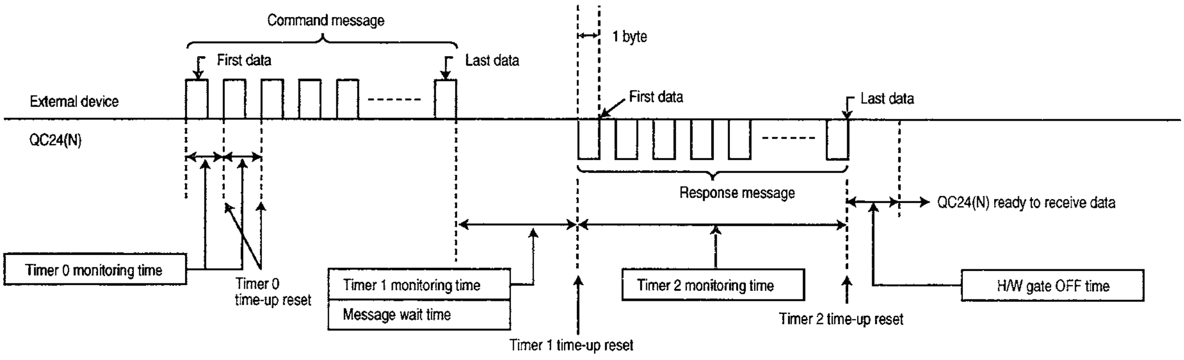
This section describes reading and writing of the QC24(N) buffer memory when using a dedicated protocol to communicate data.
Write the sequence program of the necessary part.

5.5.1 Initializing buffer memory special applications area

During QC24(N) starting, the QC24(N) default values, or the default values registered to the EEPROM by the user, are written to the special applications area of the buffer memory.
The QC24(N) default values can be used to transfer data with an external device, but the default value may have to be changed, depending on the specifications of the external device.
The following describes the setting items, description section, and examples of initialization when the default values of the QC24(N) buffer memory special applications area must be changed (initialized).

	Contents of read/write required by program generation	QC24(N) default value	Reference section
①	When QC24(N) CD terminal check performed during data communications through RS-232C interface.	Not checked	Section 4.7.2 3
②	When transmission control to external device implemented using DC code.	DTR/DSR control	Section 14.3
③	When data length units of on-demand data to be sent by ondemand function is made byte units.	Word units	Section 14.4
④	When data communications through RS-232C performed using half-duplex communications system.	Full-duplex communications	Section 14.5
⑤	When receive interval (timer 0) monitored by QC24(N) during reception of data from external device.	0 (Unlimited wait)	Section 14.7
⑥	When the QC24(N) monitors the PLC processing time (timer 1) from reception of command message from external device to transmission of result response message.	5 secs	
⑦	When the QC24(N) monitors the time (timer 2) from the start of transmission to the end of transmission is monitored when data is transmitted to an external device.	3 mins	
⑧	When a QC24(N) response message transmissions wait time (message wait time) is necessary during data communications using QnA (extension) frame.	0 ms	

(Example)



POINTS

(1) When changing the default values, write the new values during QC24(N) starting (when QC24 (N) ready signal X (n+1) E is ON).

(2) It is recommended that when the buffer memory special applications area parameters were changed, the parameters to be registered to the QC24(N) EEPROM after checking that data is sent and received normally thereafter and the registered values be used as the default values during QC24(N) starting.

* The use of the values registered to the EEPROM as the default values eliminates the need for a sequence program of the part whose parameters were changed.

(3) See Sections 14.1 and 15 for a description of the contents of the following:
- Area that can be registered to the EEPROM
- EEPROM registration method
- Initialization of parameters to buffer memory (return to QC24(N) default values)

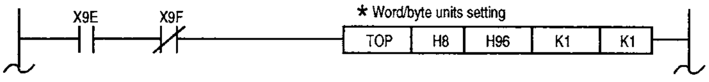
(Example of initialization of buffer memory special applications area)

The following is a sample program when the default values of the QC24(N) buffer memory special applications area are changed.
Write the program of the necessary part.
This example shows the CH1 interface settings when the QC24(N) I/O signals seen from the PLC CPU are 80H to 9FH.

Designation Example

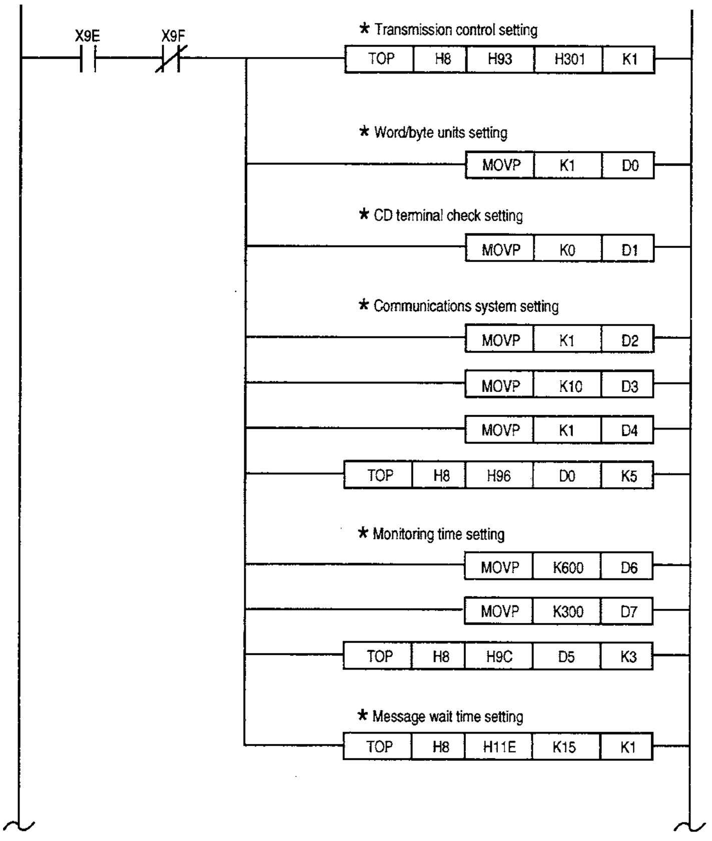
(QC24(N) I/O signals 80H to 9FH)

① When only [Word/Byte Units Setting] changed



Designation that handles on-demand data in units of bytes.
See Section 14.4.

② When the following 6 parameters are changed



Setting that implements transmission control by DC code and enables all DC control. The DC code uses the default value.
See Section 14.3.

Setting that handles on-demand data in units of bytes.
See Section 14.4.

Sets the Check CD Terminal.
See Section 4.7.2 3.

Sets the S-232 I/F communications system to half-duplex communications.
Sets non-priority during simultaneous communications. (Send wait time 1000 mS)

Sets retransmission during transmission restarting.
See Section 14.5.

Sets the response monitoring time (timer 1) to 1 minute.

Sets the send monitoring time (timer 2) to 30 seconds.
See Section 14.7.

Sets the QnA (extension) frame message wait time to 150 ms.
See Section 14.7.

5.5.2 Buffer memory read/write during data communications

This section shows the contents and reference sections when reading and writing the QC24(N) buffer memory after the start of dedicated protocol data communications.

	Read/write contents required by program generation	Reference section
①	When external device uses the QC24(N) buffer memory read/write functions.	Section 6.3
②	When the on-demand function is used to transmit data from PLC CPU to an external device.	Section 6.9
③	When data is sent to an external device by user frame when the on-demand function is used.	Chapter 7
④	When the QC24(N) interface used with a dedicated protocol is switched to another protocol.	Chapter 18
⑤	When the QC24(N) LED ON status is read and the LED turned OFF.	Section 19.1
⑥	When the QC24(N) module status, signal status, and switch setting status are read.	Section 19.2 to Section 19.5
⑦	When the result of data transmission and reception are checked. When the error contents are checked when the CH1.ERR LED or CH2.ERR LED comes on.	Section 19.1.3, Chapter 22
⑧	When the error code is read and the QC24 responded with an abnormal end NAK message to a command message received from an external device.	Section 22.1

POINT

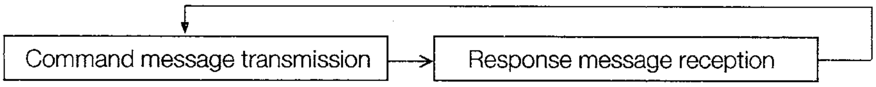
When the operations shown above do not have to be performed, a sequence program that reads and writes the buffer memory is unnecessary.

5.6 Command Transmission from External Device

This section describes procedure for transmitting commands from an external device when a dedicated protocol is used to access the PLC from an external device.

1 **Command message transmission format**

When accessing the PLC from an external device, have the external device send the following message after receiving a response message from the QC24 in response to transmission of the immediately preceding command message.
(See the descriptions of the control procedure formats (Section 6.1, etc.).)



* If the on-demand function is not used, dedicated protocol data communications are performed by half-duplex communications system.
External devices cannot send the following command messages until reception of the response for the sent command message is complete.
(The following command messages cannot be sent until data communications between an external device and PLC is complete, even when the external device and PLC configuration is m:n.)

2 **When a normal end response message cannot be received in response to a command message**

① When abnormal end response message was received
When the external device received an abnormal end response message in response to transmission of a command message, take action according to the error code in the response message. (See Section 22.1.)

② When response message cannot be received
Change the response monitoring time (timer 1, default value: 5 secs) setting. (See Section 14.7.2.)
If the response message cannot be received when the set value was changed, check the mode setting of the relevant interface, QC24(N) indicator LED ON status, and the connection cable.

③ When the first part of the response message cannot be received
Make the message wait time (default value: 0ms) set value longer. (See Section 14.7.4.)
When the response message cannot be received even when the set value is long, the processing time between the end of external device transmit processing to the start of receive processing must be shortened.

3 **When request was canceled by command message transmission**

Perform one of the following, according to the format set in the QC24(N) mode switch.
However, when write was requested, if the data was written already, the request can be cannot be canceled.

① Formats 1 to 4 (ASCII mode) data communications
Send the control code (EOT, CL) given in Section 6.1.4 1 to the QC24(N) to match each format.

② Format 5 (binary mode) data communications
Send the transmission sequence initialize command given in Section 6.10 to the QC24(N).

POINT

(1) The status of the QC24(N) transmission sequence can be checked with the indicator LED and buffer memory (addresses 255H, 265H).

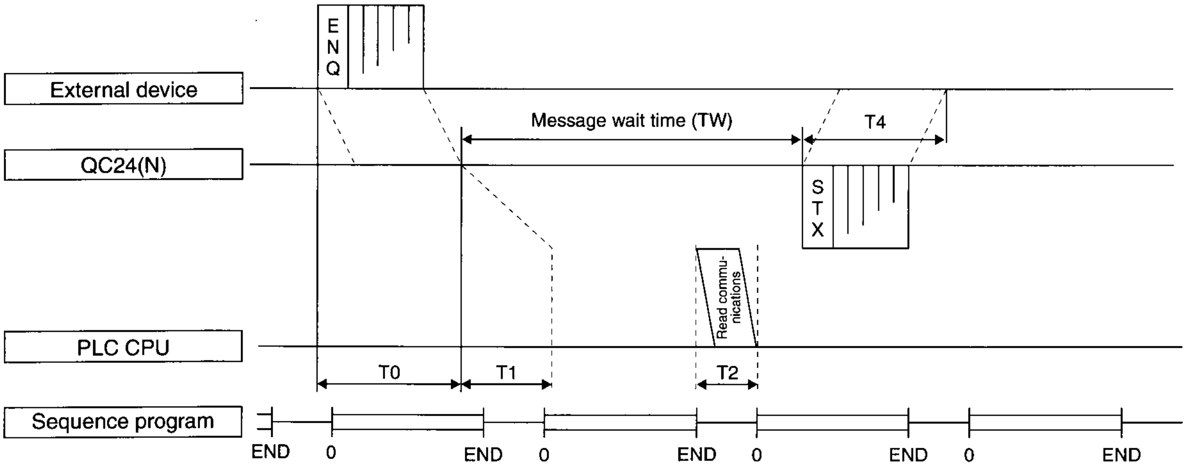
(2) When the QC24(N) detects an error, it stores the error code to the following buffer memory. When the error cord is read and stored, as required, check the error contents and take the action described in Section 22.1.
- Buffer memory addresses 257H, 267H......Data send result
- Buffer memory addresses 258H, 268H......Data receive result
- Buffer memory addresses 25AH, 26AH......Dedicated protocol send error code

5.7 Transmission Sequence Timing Chart and Communications Time

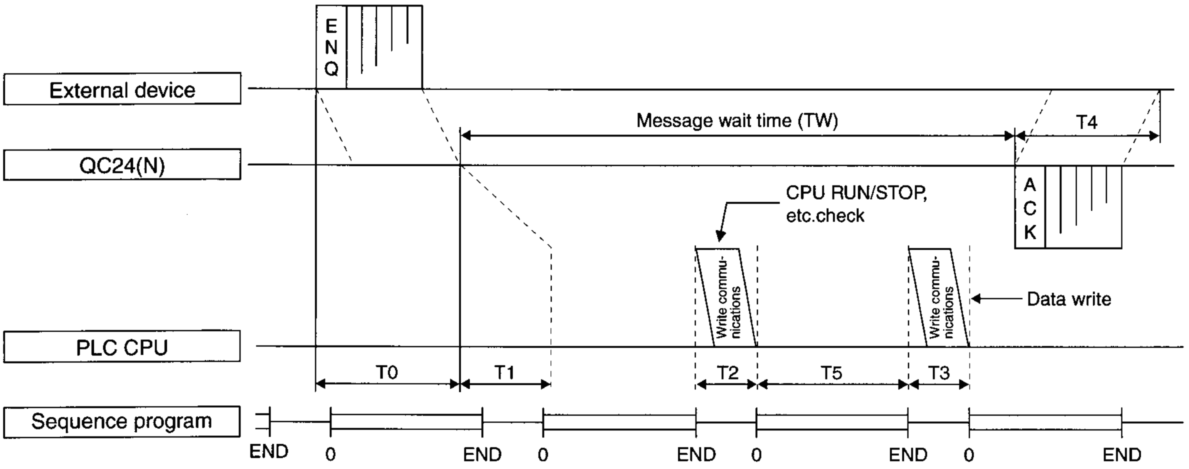
This section describes the external device and PLC communications timing chart.

1 When the external device reads/writes the data of a QC24(N) station PLC CPU

(a) Data read (When message wait time was set.)



(b) Data write (When message wait time was set.)



Notes

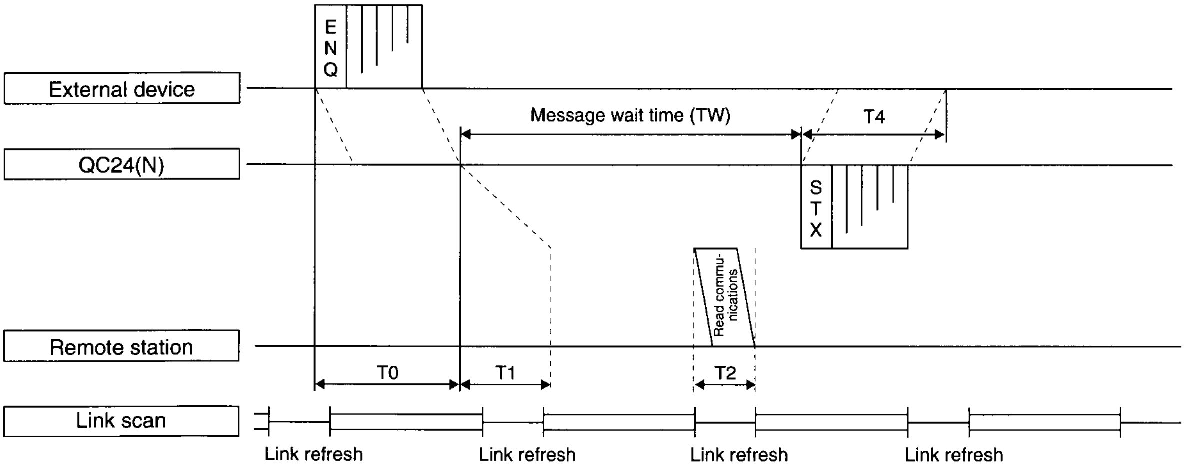
(1) Communications between QC24(N) and PLC CPU is always performed after END processing in accordance with the illustration above. Therefore, the scan time becomes longer by that communications time (intervention time to PLC CPU).

(2) The number of scans required by processing when read/write to the PLC CPU is requested differs with the contents of the request.
For instance, when a read operation that requires two scans was requested, a surplus of 1 scan + T2 time is required.

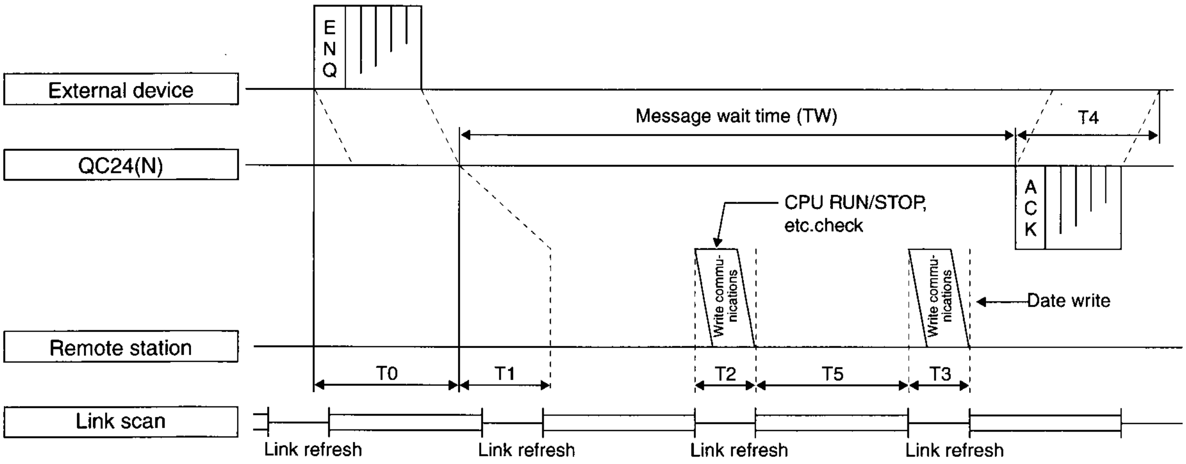
(3) See Appendix 3 for the communications time and number of scans required by read/write request processing.
See Section 5.4 for the number of points processed per communication after END processing.

2 When external device reads/writes the data of a QC24(N) remote station

(a) Data read (When message wait time was set.)



(b) Data write (When message wait time was set.)



Notes

(1) QC24(N) and remote station communications are always performed during link refresh as shown in the illustration above.
Therefore, the link refresh time becomes longer by that communications time (intervention time to remote I/O station).

(2) The number of link scans required by processing by read/write request to remote station depends on the request contents.
For instance, When a read operation requiring two link scans was requested, a surplus of 1 link scan + T2 time is required.

(3) See Appendix 3 for the communication time and number of scans required by read/write request processing. (Replace the number of scans shown in Appendix 3 with number of link scans.)
See Section 5.4 for the number of points processed per communications during link refresh.

3 Transmission sequence transmission time

This section describes the average value of the approximate time from the start of data transmission by an external device to return of the result from the QC24(N).
Use this as a reference for the processing time.

Symbol	Name	Description
T	Communications time	Total time from the start of message transmission by an external device to completion of the receipt of the response message.
T1	Message processing time	Time required for analysis of request data and preparation of the response data.
T2, T3	CPU intervention time*1	Intervention time to the PLC CPU (increase in scan time) (see Appendix 3)
T0	Request message transmission time	Time required to put the request message on the line.
T4	Response message transmission time	Time required to put the response message on the line.
T5	1 scan time/1 link scan time*2	1 scan time/1 link scan time

*1 For functions that can be processed in 1 scan/1 link scan, T3 is 0.
*2 For functions that can be processed in 1 scan/1 link scan, T5 is 0.

(a) Reading data

	Formula
Communications time [ms]	T=T0+{the longer of the T1+T2 or TW time}+T4
Request message transmission time [ms]	T0=request message size [byte] x number of bits of 1 character / transmission rate [bps] x 1000
Response message transmission time [ms]	T4=response message size [byte] x number of bits of 1 character / transmission rate [bps] x 1000
Message processing time [ms]	T1=maximum 1 scan time, 1 link scan time or internal processing time of the QC24(N)*3 • When maximum 1 scan time or 1 link scan time < internal processing time of the QC24(N) T1=internal processing time of the QC24 (N) • When maximum 1 scan time or 1 link scan time ≧ internal processing time of the QC24(N) T1=Max. 1 scan time or 1 link scan time

(b) Writing data

	Formula
Communications time [ms]	T=T0+{the longer of the T1+T2+T3+T5 or TW time}+T4
Request message transmission time [ms]	T0=request message size [byte] x number of bits of 1 character / transmission rate [bps] x 1000
Response message transmission time [ms]	T4=response message size [byte] x number of bits of 1 character / transmission rate [bps] x 1000
Message processing time [ms]	T1=maximum 1 scan time, 1 link scan time or internal processing time of the QC24(N)*3 • When maximum 1 scan time or 1 link scan time < internal processing time of the QC24(N) T1=internal processing time of the QC24 (N) • When maximum 1 scan time or 1 link scan time ≧ internal processing time of the QC24(N) T1=Max. 1 scan time or 1 link scan time

*3 Internal processing time of the QC24 (N)
Time is within the following range depending on the access points (MIN to MAX).
· A1SJ71QC24N1(-R2): 12.5 to 45.0[ms]
· QC24(N) other than the above: approx.100[ms]

4 Transmission time over data link system/network system

(a) Over MELSECNET (Ⅱ) or MELSECNET/B

The transmission time (T1) for data transmission by designating the PLC CPU number to a PLC CPU on MELSECNET (Ⅱ) or MELSECNET/B not equipped with a QC24(N) is shown below.

- **Local station**

  Transmission time (T1) = $(\underset{*1}{\underline{\text{Transmission delay time A}}} + \underset{\text{(When 50 ms is exceeded.)}}{\underline{\text{QC24(N) equipped station scan time}}} \text{ or } \underset{\text{(When 1CH is used.)}}{\underline{\text{50ms}}}) \times (\underset{*2}{\underline{n}}+\underset{*3}{\underline{1}})$

- **Remote I/O station**

  Transmission time (T1) = $(\underset{*1}{\underline{\text{Transmission delay time B}}} + \underset{\text{(When 50 ms is exceeded.)}}{\underline{\text{master station scan time}}} \text{ or } \underset{\text{(When 1CH is used.)}}{\underline{\text{50ms}}}) \times (\underset{*2}{\underline{n}}+\underset{*3}{\underline{1}})$

[*1] See the description of the relevant data link system transmission delay time in the data link reference manual.
Transmission delay time A........... See the LRDP instruction processing time field.
Transmission delay time B........... See the RFRP instruction processing time field.

[*2]
- When communication to the relevant station is performed for the first time when the power is turned on or after the CPU is reset } n=3
- When communicating to stations except the 10 stations that communicated last
- When communicating for the second time when the number of communicating stations is less than 10 } n=1
- When communicating for the second time to the 10 stations that communicated last

[*3] If SW07 of the QC24(N) transmission specification setting switch is in the OFF position (write during RUN disable), addition is performed only when data is written from the external device.

Example)

When QC24(N) installed to MELSECNET master station and local station device memory is read
(Communications for second time when number of communicating stations is less than 10)
(Condition < L < LS < M, M:120ms $\alpha1$: 10ms)
Transmission time (T1) = $(M\times4+\alpha1\times4+M) \times 1 = (120\times4+10\times4+120) \times 1 = 640$
T1 becomes 640ms.

M : MELSECNET master station scan time
$\alpha1$: MELSECNET master station link refresh time
LS : Link scan time
L : MELSECNET local station scan time

- **Causes of transmission time (T1) delay**

  Commands requiring 2 scans for transmission need double the time derived from the equations above.
  See Section 5.8 $\boxed{2}$ for the number of scans required when another QC24(N), GPP function, etc. requested access to the same QnACPU at the same time.

* See the data link reference manual for a detailed description of the data link.

POINT

Under some conditions, data transmission to a PLC CPU of other than the local station on the MELSECNET(II) or MELSECNET/B can cause a considerable delay.
This time delay can be reduced by assuming that only QC24(N) stations communicate between external devices and PLC, and communications with other PLC are carried out by data link (B, W).

(b) Transmission time over MELSECNET/10

The transmission time (T1) for data transmission by designating the PLC number for a PLC equipped with a QC24(N) on a MELSECNET/10 is shown below.

① PLC-PLC network

- $$\text{Transmission time (T1)} = (\underset{*1}{\underline{\text{Transmission delay time}}} + \underset{\text{(When 50 ms is exceeded.)}}{\underline{\text{QC24(N) equipped station scan time}}} \text{ or } \underset{\text{(When 1CH is used.)}}{\underline{\text{50ms}}}) \times (\underset{*2\ *3}{\underline{n+1}})$$

*1 See the description of the transmission delay time related to the ZNRD/ZNWR instructions in the network system reference manual (PLC-PLC network).

*2
- When communicating with the relevant station for the first time after the power is turned on, or the CPU is reset
- When communicating to stations except the 16 stations that communicated last

} n=6

- When communicating for the second time when the number of communicating stations is 16 or less
- When communicating for the second time to the 16 stations that communicated last

} n=1

*3 If SW07 of the QC24(N) transmission specification setting switch is in the OFF position (write during RUN disable), addition is performed only when data is written from the external device.

Example)

When the QC24(N) was installed in a station on the MELSECNET/10 (PLC-PLC network) and the device memory of another station on the same MELSECNET/10 was read. (Communications for the second time when the number of communicating stations is 16 or less)

- S_T: Sending side scan time 120 ms
- α_T: Sending side link refresh time 10 ms
- S_R: Receiving side scan time 100 ms
- α_R: Receiving side link refresh time 5 ms
- L_S: Link scan time 30 ms
- Number of simultaneous transient requests: 3
- Maximum number of transients: 2

$$\text{Transmission time (T1)} = \{\underset{(S_T)}{120\times 2}+\underset{(\alpha_T)}{10\times 2}+\underset{(L_S)}{30\times 6}+\underset{(S_R)}{100\times 2}+\underset{(\alpha_R)}{5\times 2}$$

$$+\left[\underbrace{\frac{\text{3 (number of simultaneous transient requests)}}{\text{2 (max. number of transients)}}}_{\text{Integer value (rounded after the decimal point)}}-1\right]\times \underset{(L_S)}{30}\times 2+\underset{(S_T)}{120}\}\times 1 = 890\text{ms}$$

- **Causes of transmission time (T1) delay**

  Commands requiring 2 scans for transmission need double the time derived from the equations above.

  See Section 5.8 for the number of scans required when another QC24(N), GPP function, etc. requested access to the same QnACPU at the same time.

  * See the network reference manual (PLC-PLC network) for a detailed description of the network system.

POINT

Under some conditions, data transmission to a PLC CPU of other than the local station on the MELSECNET/10 can cause a considerable delay.

This time delay can be reduced assuming that only QC24(N) stations communicate between external devices and PLC, and communications with other PLC are carried out by data link (LB, LW).

② Remote I/O network

- Transmission time (T1) = $(\underset{*1}{\underline{\text{Transmission delay time}}} + \underset{\text{(When 50 ms is exceeded.)}}{\underline{\text{link scan time}}} \text{ or } \underset{\text{(When 1CH is used.)}}{\underline{\text{50ms}}}) \times (\underset{*2}{\underline{n}}+\underset{*3}{\underline{1}})$

*1 See the description of the transmission delay time regarding the ZNFR/ZNTO instructions in the network system reference manual (remote I/O network).

*2
- When communicating to the relevant station for the first time after the link is started
- When communicating to a station other than the 16 stations that communicated last } n=6
- When communicating for the second time when the number of communicating stations is 16 or less
- When communicating for the second time to the 16 stations that communicated last } n=1

*3 If SW07 of the QC24(N) transmission specification setting switch is in the OFF position (write during RUN disable), addition is performed only when data is written from the external device.

Example)
When QC24(N) was installed in a station on the MELSECNET/10 (remote I/O network) and the device memory of another station on the same MELSECNET/10 was read
(When communicating for the second time when the number of communicating stations is 16 or less)

• Sm :	Master station sequence scan time	120 ms
• αm :	Master station link refresh time	10 ms
• αr :	Remote I/O station link refresh time	2 ms
• LS :	Link scan time	30 ms

Since (Sm) > (LS), the above becomes as shown below. (When there is one master station)

Transmission time (T1) = $\{(\underset{(Sm)}{120}+\underset{(\alpha m)}{10}) \times 3+50\} \times 1 = 440$ ms

- **Causes of transmission time (T1) delay**
  Commands requiring 2 scans for transmission (device write when DIP switch SW07 is off, etc.) need double the time derived from the equations above.
  See Section 5.8 for the number of scans required when another QC24(N), GPP function, etc. accessed the same QnACPU at the same time.

* See the network reference manual (remote I/O network) for a detailed description of the network system.

POINT

Under some conditions, data transmission to a PLC CPU of other than the local station on the MELSECNET/10 can cause a considerable delay.
This time delay can be reduced by assuming that only QC24(N) stations communicate between external devices and PLC, and communications with other PLC are carried out by data link (LB, LW).

5.8 Operation of PLC CPU During Data Communications

This section describes the operation of the PLC CPU during dedicated protocol data communications.

1 PLC CPU scan time

When the PLC CPU is RUNNING for requests from the QC24(N), QC24(N) and PLC CPU access is processed only for one request during each END processing.
Therefore, the scan time is extended accordingly.
See Appendix 3 for the intervention time to the PLC CPU required in communications between QC24(N) and PLC CPU.

2 Simultaneous access to QnACPU

Processing during simultaneous access depends on the QnACPU [PLC System Setting] parameter.

① When [PLC System Setting] parameter not set

The QnACPU processes only one request during END processing.
When the same QnACPU was simultaneously accessed from each module and GPP function, the QnACPU waits until the end of other processing and the number of scans required by processing increases.
Entering a COM instruction in the sequence program also increases the scan time by the COM instruction execution time. However, two or more accesses can be processed during one scan.

② When [PLC System Setting] parameter set

If general data processing of the [PLC System Setting] parameter is set, the QnACPU processes requests corresponding to the number of general data processing settings during END processing.
For instance, if the [PLC System Setting] general data processing setting is [4], the QnACPU processes up to four access requests from each module and GPP function during END processing of one scan.
The insertion of a COM instruction also increases the scan time by the COM instruction execution time. However, the QnACPU processes up to four access requests from each module and GPP function up to COM instruction execution during execution of that COM instruction.

5.9 Data Communications Precautions

This section describes the precautions to be taken during dedicated protocol data communications.

1 **Conditions that initialize the QC24(N) transmission sequence**

The following conditions initialize the QC24(N) transmission sequence.

- When the power is turned on, the CPU panel reset switch is operated, or the mode is switched.
- When transmission of the response message for transmission of a command message is complete.
- When a transmission sequence initialize request was received. (See Sections 6.1.4 1 (b) and 6.10.)
- When the CD signal was turned OFF when data is transferred by setting CD Terminal Check Enable (see Section 4.7.2 3) in full duplex communications at the RS-232C.

2 **NAK response from QC24(N)**

The QC24(N) sends a NAK response by dedicated protocol when an error is detected for a request addressed to the local station.
Therefore, during full-duplex communications, a NAK response may be sent even when the external device is transmitting.

3 **Change of another stations PLC CPU that communicates data**

After starting, the QC24(N) fetches and stores the data of the other station PLC CPU.

When the other station PLC CPU that is transferring data is changed after the QC24(N) starts, when the PLC CPU type name changes, restart the QC24(N). (Local PLC power reset/CPU reset)

4 **Framing error generation at external device**

When nothing is sent from the QC24(N) to an external device through the RS-422 or RS-422/485 interface, a framing error may be generated at the external device. (See Section 3.3.3.)
Skip the data at the external device until the QC24(N) sends STX, ACK, or NAK.
Check the QC24(N) interface specifications given in Section 3.3.3 before transmitting data.

5 **Installation of multiple QC24(N)**

When external devices connected to each QC24(N) access the PLC CPU at the same time, the PLC CPU determines the access order.
The user cannot decide the access priority.

6 When connecting a peripheral for the GPP function or a GOT, which is compatible with the QnACPU, to the QC24(N), set the switches for the connected channel side of the QC24(N) according to Section 4.9.

7 Before changing data or program in the PLC during operation, please read the manual carefully and check thoroughly for safety. If an error is made in changing data or program, it can cause faulty operation of the system and breakdown or failure of mechanical units.

8 **Canceling Read/Write Request**

If using the external device to send the command to cancel the read/write request, refer to sections 6.1.4 and 6.10. Following those procedures, send the command that initializes the transmission sequence, from the external device to QC24(N).

5.10 To Access Another Station's A Series PLC

The following is an overview to access another station's A series PLC CPU, using the QC24(N)'s dedicated protocol for data transfer. Section 5.3 shows the range of access possibilities. Use the commands listed in section 5.4 as possible to use to transfer data.

External device access station (other station)		Data transfer overview			
		QnA (enlargement) frame		QnA simplified frame (form 1 to form 4)	A compatible frame (form 1 to form 4)
		Form 1 to Form 4	Form 5		
Via MELSECNET/10	A series PLC CPU	○	○	×	○
Via MELSECNET(II) Via MELSECNET/B	A series PLC CPU	○	○	×	○
Multi-drop connection	A series PLC CPU (*1)	○	×	×	○
	QnA series PLC CPU (*1)	○	×	×	○
	QnA series PLC CPU (*2)	○	○*4	×	○
	QnA series PLC CPU (*3)	○	○*4	○	○
Multi-drop connection via MELSECNET/10	A series PLC CPU (*1)	×	×	×	×
	QnA series PLC CPU (*1)	×	×	×	×
	QnA series PLC CPU (*2)	○	○*4	×	×
	QnA series PLC CPU (*3)	○	○*4	×	×

○ : access is possible × : access is impossible

*1 Shows the computer link module mounting station.

*2 Shows the QC24 mounting station.

*3 Shows the QC24N mounting station.

*4 If the computer link module is included in the multi-drop computer link module, it can not be accessed.

6. DATA COMMUNICATIONS USING QnA FRAME AND QnA EXTENSION FRAME

This section describes the control procedure format of each frame, the method of designating each item in a message, and how to use the commands when an external device uses the dedicated protocol QnA frame and QnA extension frame to transfer data with the PLC.

6.1 Basic Formats

There are five formats as control procedures (command message, response message construction and communication procedure) for an external device to use a dedicated protocol to access the PLC. Data communications in the designated format is possible by setting the mode switch of the objective interface of the QC24(N) to [1] to [5] to match the format used.

① When transferring data by ASCII mode QnA frame, QnA extension frame, and A compatible frame Format 1 to format 4

② When transferring data by binary mode QnA extension frame Format 5

The differences between the four ASCII mode formats when format 1 is made the standard are shown below.

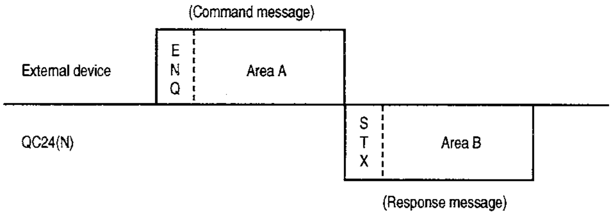
Format 2 .... Format with block number added to each message
Format 3 .... Format with each message enclosed between STX and ETX
Format 4 .... Format with CR, LF added to each message

The following describes the contents of the control procedure and the contents of each section designated by the control procedure of each of the five formats.

1 Basics of dedicated protocol control procedure

This section describes the basics of the send data given in the description of each control procedure beginning from Section 6.1.1.

(a) When external device reads data from PLC

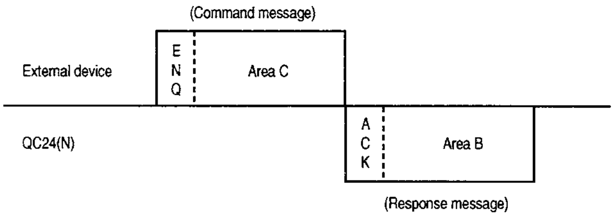


① Area A indicates transmission from external device to QC24(N).
② Area B indicates transmission from QC24(N) to external device.
③ The external device program is generated so that the data are sequentially sent from left to right.
(Example: For Area A, the data is sequentially sent to the right from ENQ.)

POINT

When the QC24(N) receives a command message from an external device, after it completes processing of Area A in the message, the QC24(N) sends a response message and enters the neutral state.
When the QC24(N) is in the neutral state, it waits to receive the next command message and a on-demand data send request from the PLC CPU.

(b) When data is written to PLC from an external device

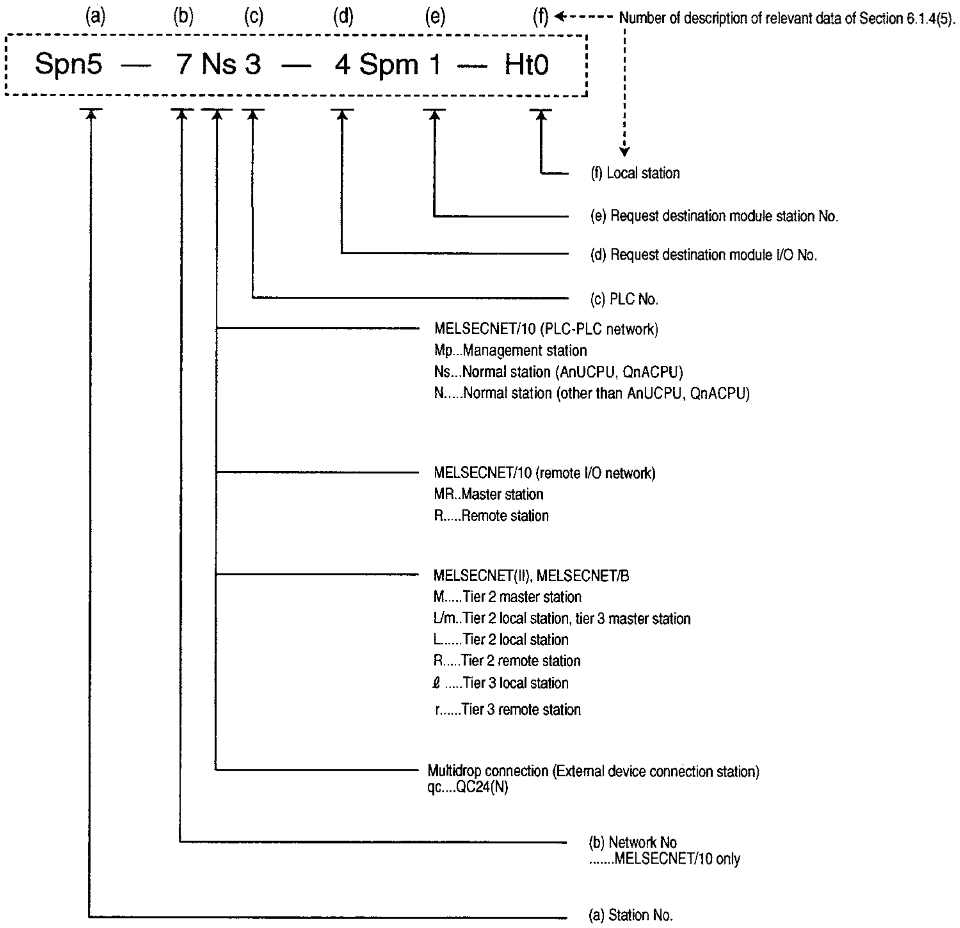


① Area C indicates transmission from external device to QC24(N).
② Area B indicates transmission from QC24(N) to external device.
③ The external device program is generated so that the data are sequentially sent from left to right.
(Example: For Area C, the data is sequentially sent to the right from ENQ.)

2 External device connection stations and access destination

The following show the external connection stations that transmit the send data (example) given in the description of each control procedure format beginning from Section 6.1.1 and the PLC CPU (QnACPU) that is accessed by the external stations.

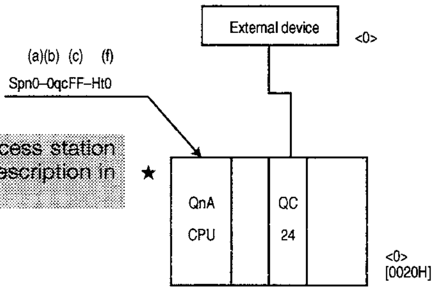
① Meaning of symbols indicated by the arrow to each station in the illustrations
The number before or after the symbol is the contents (value) of the relevant data in the message when an external device accesses the station indicated by the arrow.
See Section 6.1.4 5 for a description of the designation contents of each data.



② QnA frame data communication format description section external device connection station and access destination

This section shows the external device connection stations that transmit the send data (example) given in the description of each control procedure format of Section 6.1.1 and the PLC CPU (QnACPU) that is accessed by the external devices.

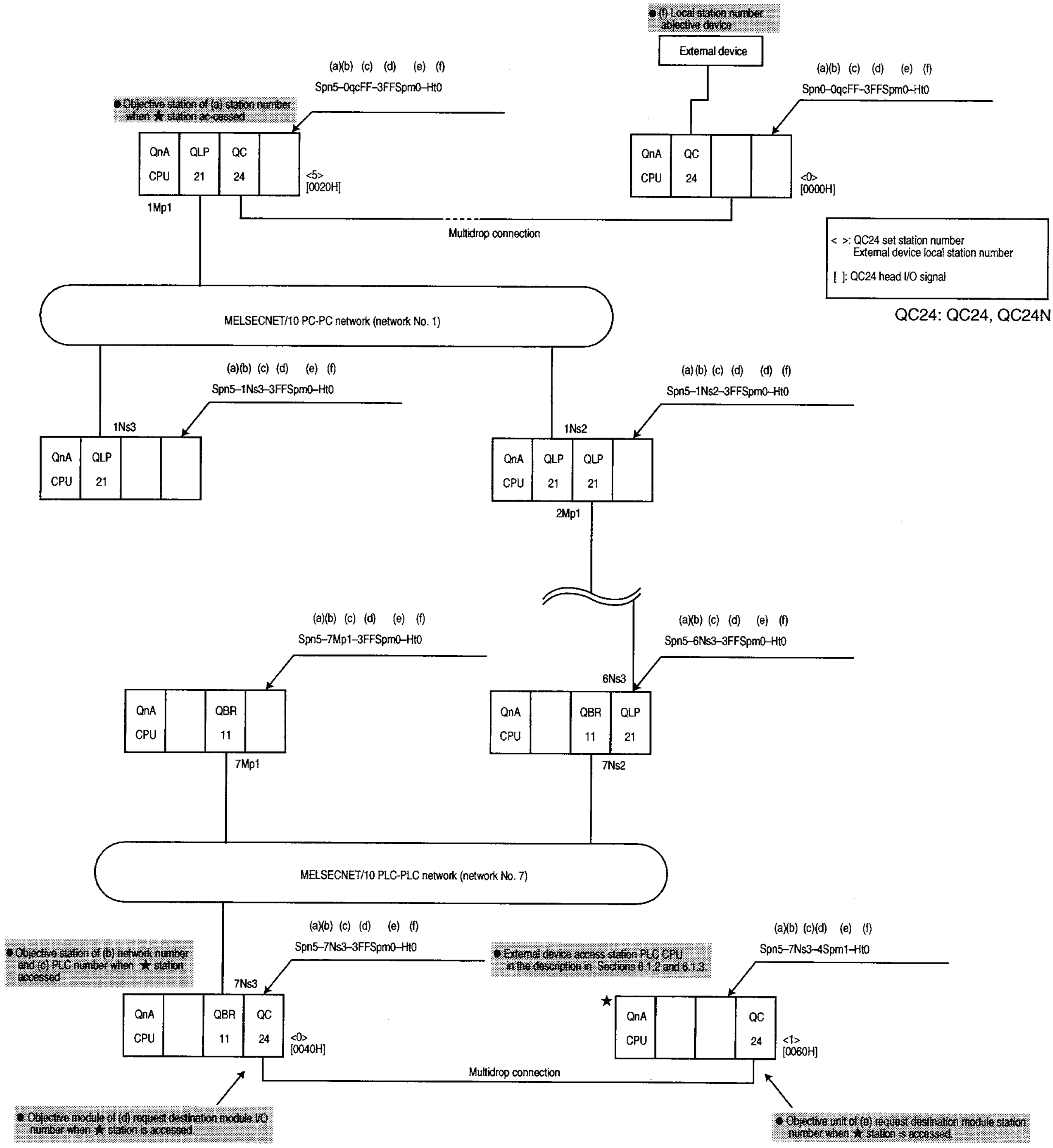
*External device access station PLC CPU in the description in Section 6.1.1.



< >: QC24(N) set station number
External device local station number
[ ]: QC24(N) head I/O signal

QC24: QC24, QC24N

③ QnA extension frame data communications format description section external device connected stations and access destination
This section shows the external device connection stations that transmit the send data (example) given in the description of each control procedure of Sections 6.1.2 and 6.1.3 and the PLC CPU (QnACPU) accessed by the external device connection stations.

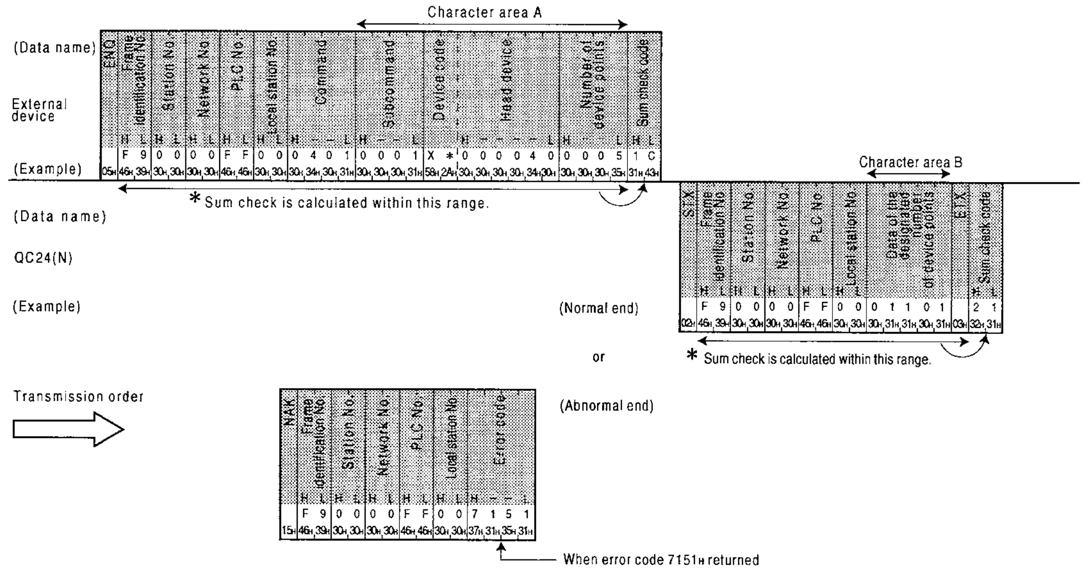


6.1.1 ASCII mode QnA frame data communications format

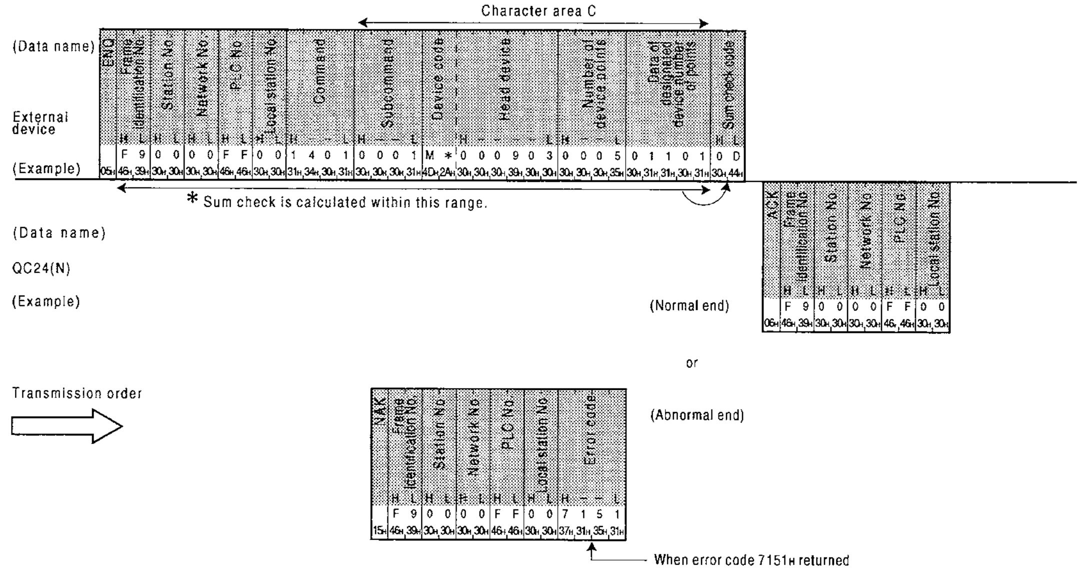
1 Communications using control procedure format 1

(ASCII mode QnA frame format 1)

<table>
<tr><th>Contents</th><th>Control procedure (Protocol)</th></tr>
<tr><td>When external device reads PLC data</td><td>
(Example) Using a 0401 command to read the five points from X40 to X44 of an external device connection station QnACPU
(Section 6.1 2 ② ★ station)



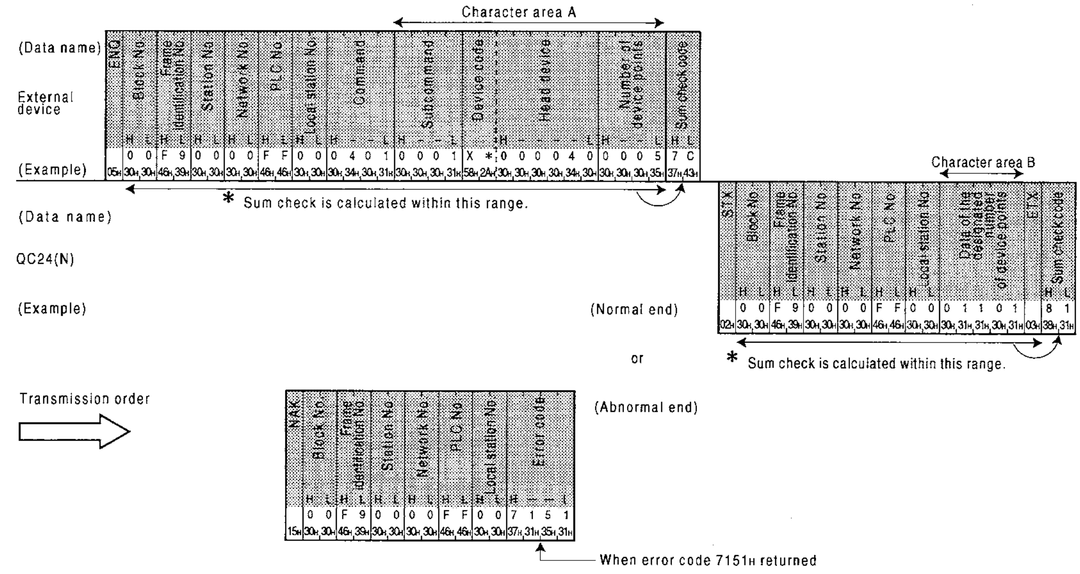
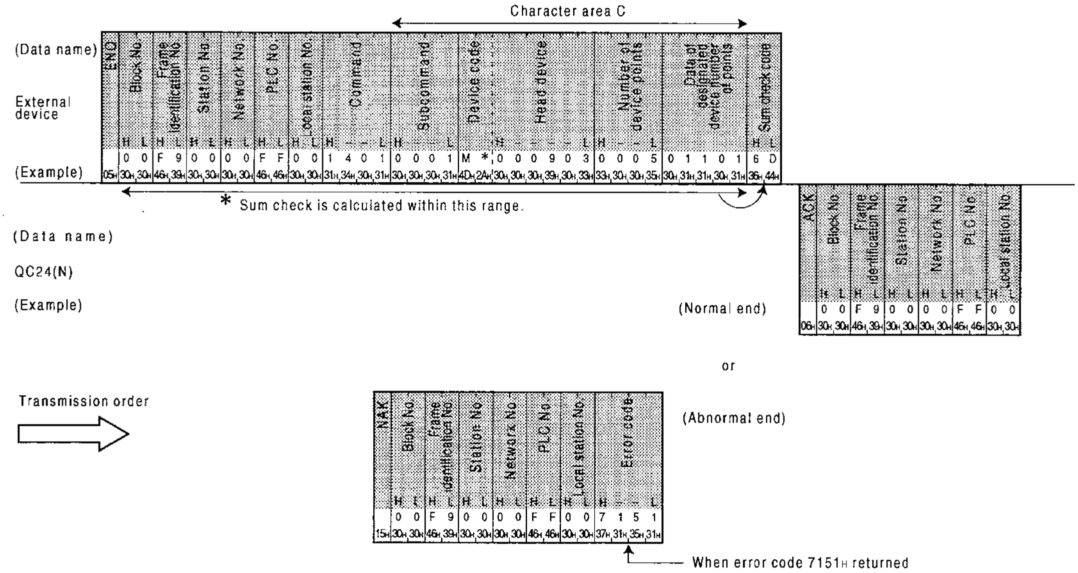
</td></tr>
<tr><td>When external device writes data to PLC</td><td>
(Example) When using a 1401 command to write data to five points from M903 to M907 of an external device connection station (Section 6.1 2 ② ★ station)



</td></tr>
<tr><td>Notes</td><td>
(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added.
(2) When sum check is enabled, the sum check is calculated only for the characters of the * part in the illustrations above.
(3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats.
(4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0ms to 150 ms range. (See Section 14.7.4.)
</td></tr>
</table>

2 Communications using control procedure format 2

(ASCII mode QnA frame format 2)

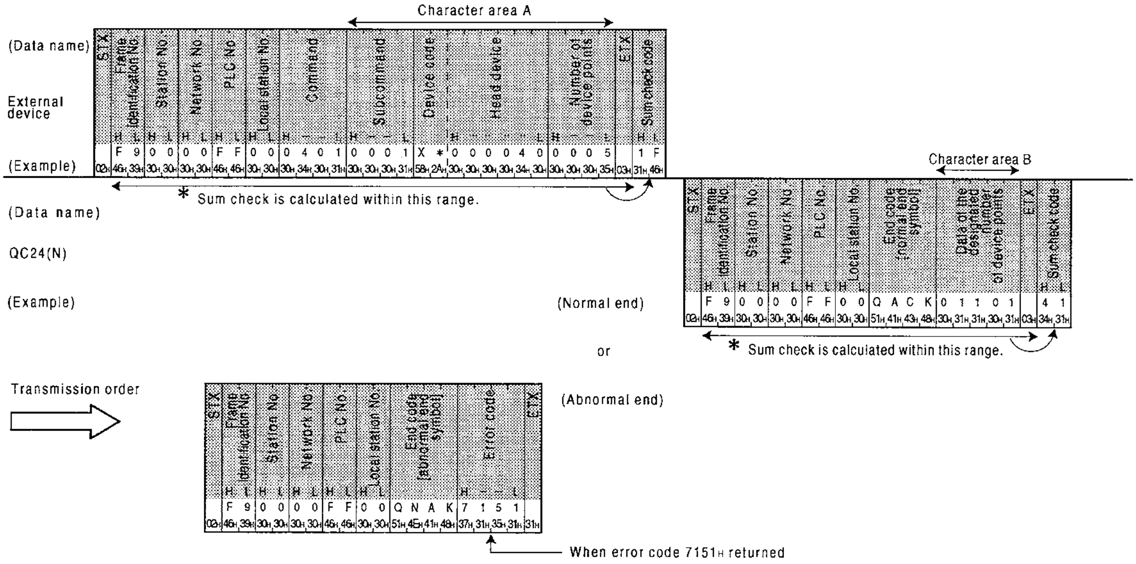
Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the data at five points from X40 to X44 of an external device connection station QnACPU (Section 6.1 2 ② ★ station.) 
When external device writes data to PLC	(Example) When using a 1401 command to write the data of five points from M903 to M907 of an external device connection station QnACPU (Section 6.1 2 ② ★ station) 
Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added. (2) When sum check is enabled, the sum check is calculated only for the characters of the * part in the illustrations above. (3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats. (4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0ms to 150 ms range. (See Section 14.7.4.)

3 Communications using control procedure format 3

(ASCII mode QnA frame format 3)

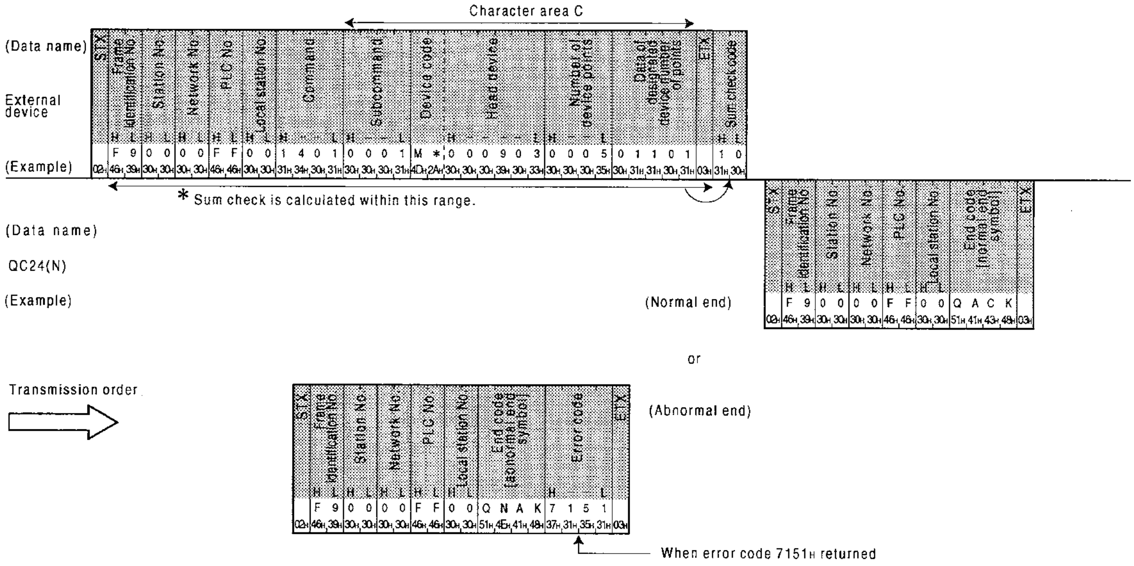
<table>
<tr><th>Contents</th><th>Control procedure (Protocol)</th></tr>
<tr><td>When external device reads PLC data</td><td>

(Example) When using a 0401 command to read the data of five points from X40 to X44 of the external device connection station QnACPU (Section 6.1 2 ② ★ station)



</td></tr>
<tr><td>When external device writes data to PLC</td><td>

(Example) When using a 1401 command to write data to five points from M903 to M907 of an external device connection station QnACPU (Section 6.1 2 ② ★ station)



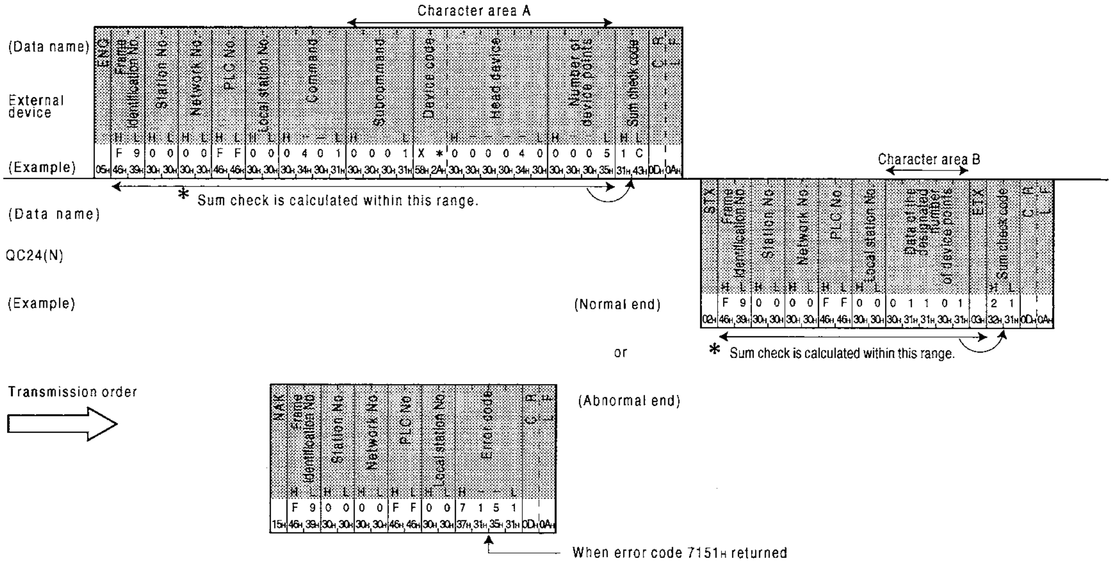
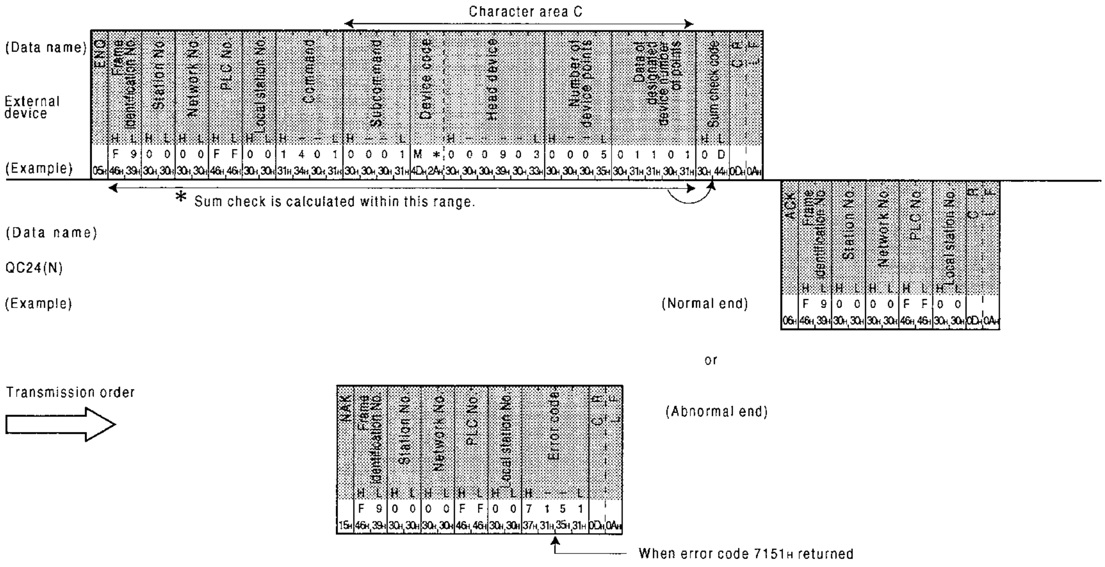
</td></tr>
<tr><td>Notes</td><td>

(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check disabled, the sum check code is not added.
(2) When sum check is enabled, the sum check is calculated only for the characters of the * part in the illustrations above.
(3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area is the same for all four formats.
(4) The time interval from reception of a command message to transmission of a response message by the QC24(N) can be set over the 0ms to 150 ms range. (See Section 14.7.4.)
(5) When the external device and PLC CPU system configuration is m: n, data communications cannot use control procedure format 3.

</td></tr>
</table>

4 Communications using control protocol format 4

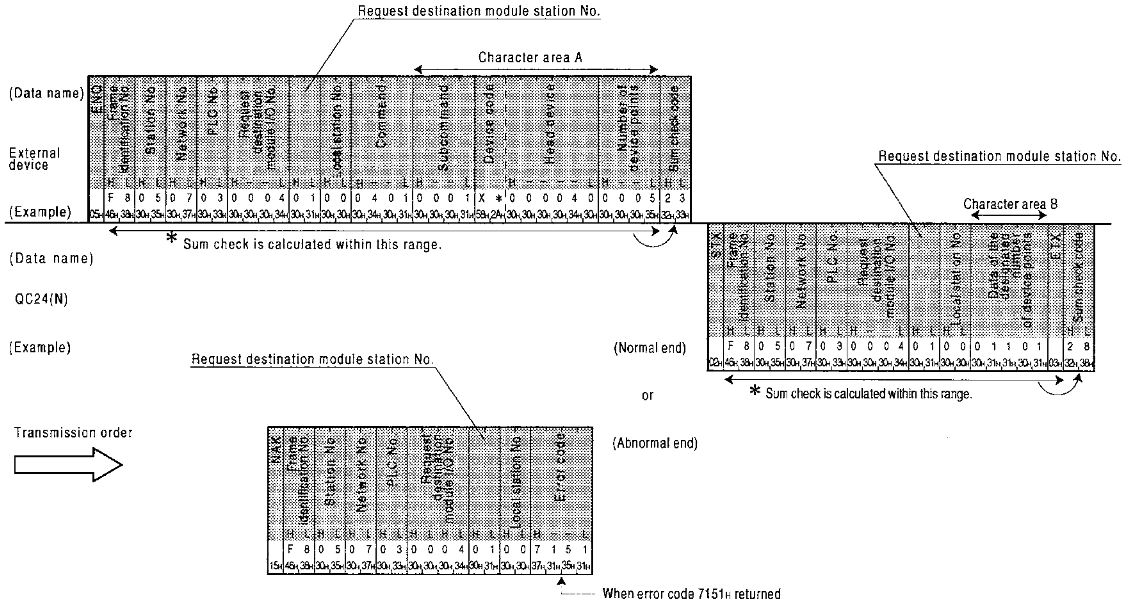
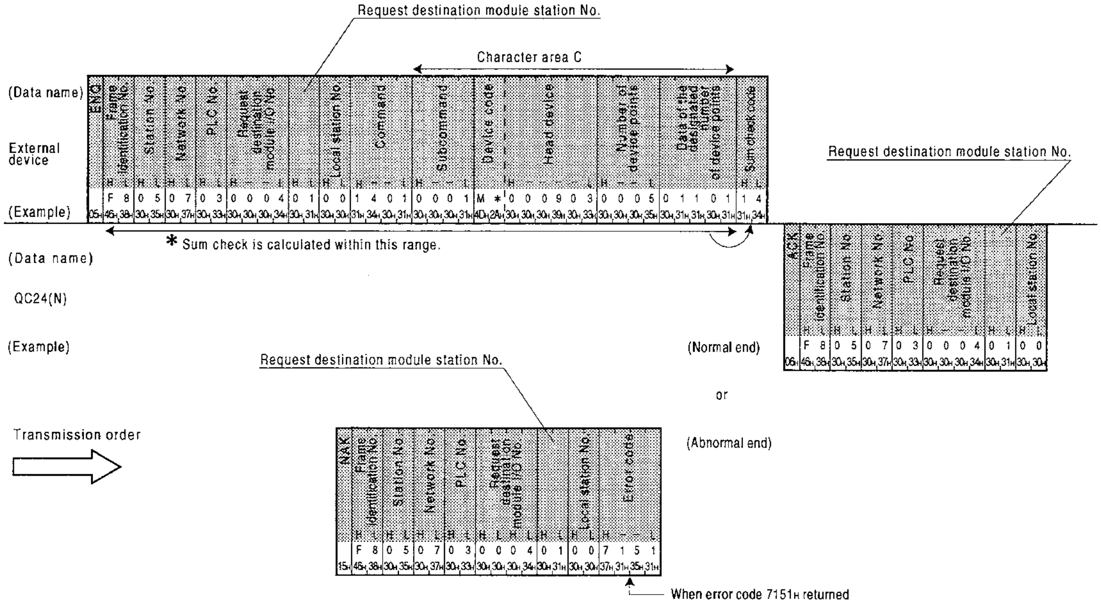
(ASCII mode QnA frame format 4)

Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the data of five points from X40 to X44 of an external device connection station QnACPU (Section 6.1 2 ② ★ station) 
When external device writes data to PLC	(Example) When using a 1401 command to write the data of five points from M903 to M907 of an external device connection station QnACPU (Section 6.1 2 ② ★ station) 
Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added. (2) When sum check is enabled, the sum check is calculated only for the characters of the * part in the illustrations above. (3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area is the same for all four formats. (4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0ms to 150 ms range. (See Section 14.7.4.)

6.1.2 ASCII mode QnA extension frame data communications format

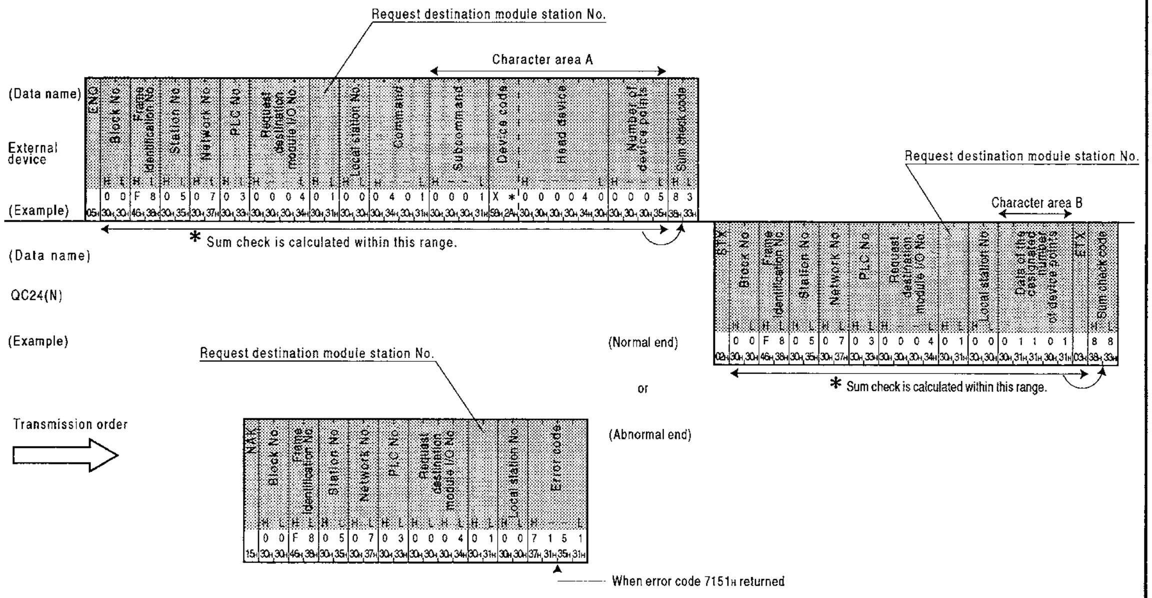
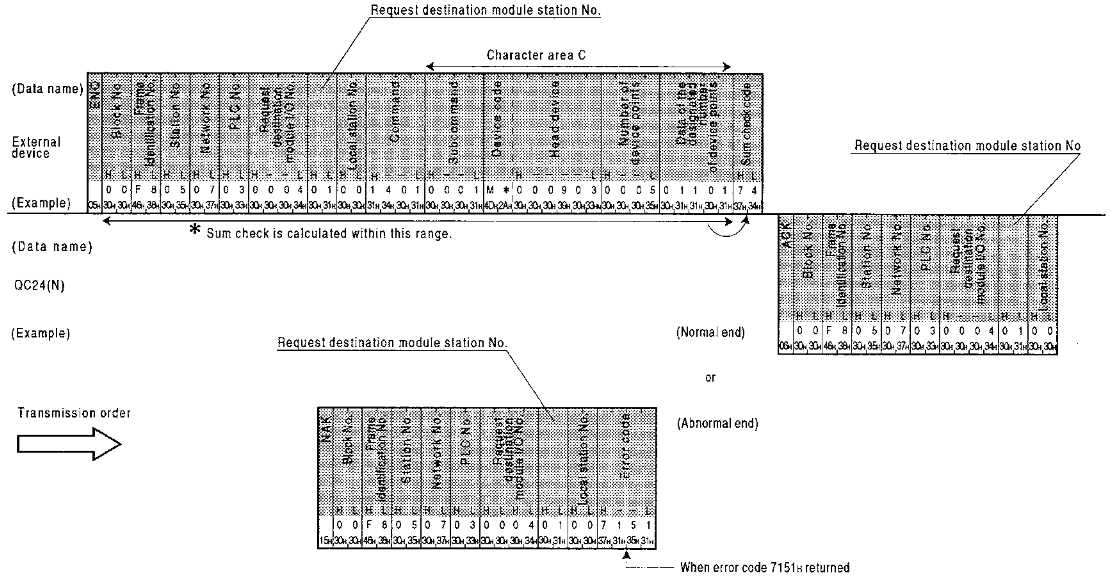
1 When communicating using control format 1

(ASCII mode QnA extension frame format 1)

Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the data at five points from X40 to X44 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
When external device writes data to PLC	(Example) When using a 1401 command to write data to five points from M903 to M907 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added. (2) When sum check is enabled, the sum check of only the characters of the * part in the illustrations above is calculated. (3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats. (4) The time between reception a command message and transmission of the response message by the QC24(N) can be set within the 0ms to 150 ms range. (See Section 14.7.4.)

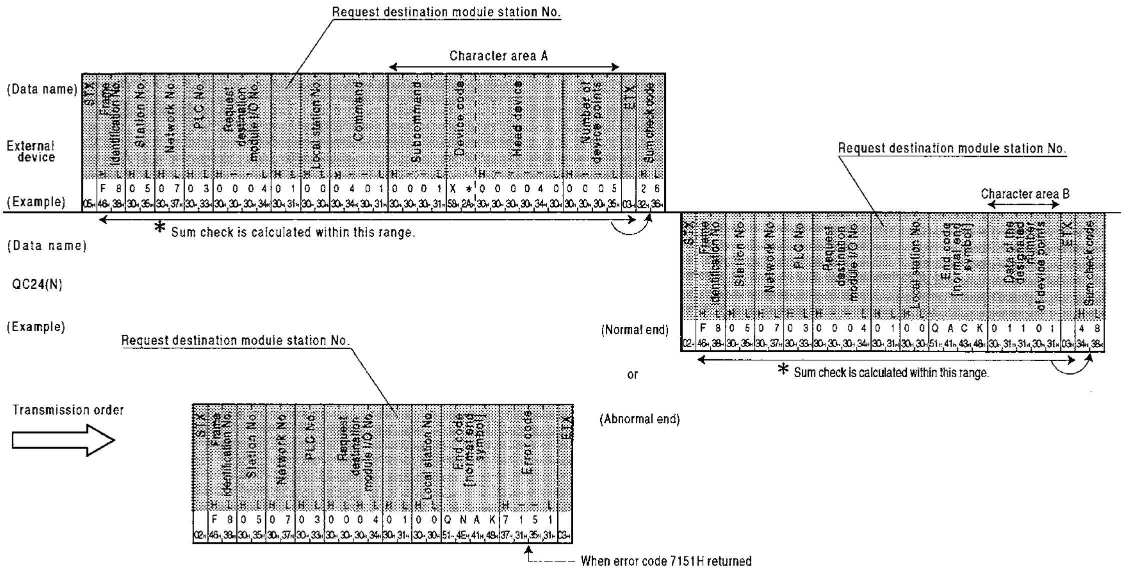
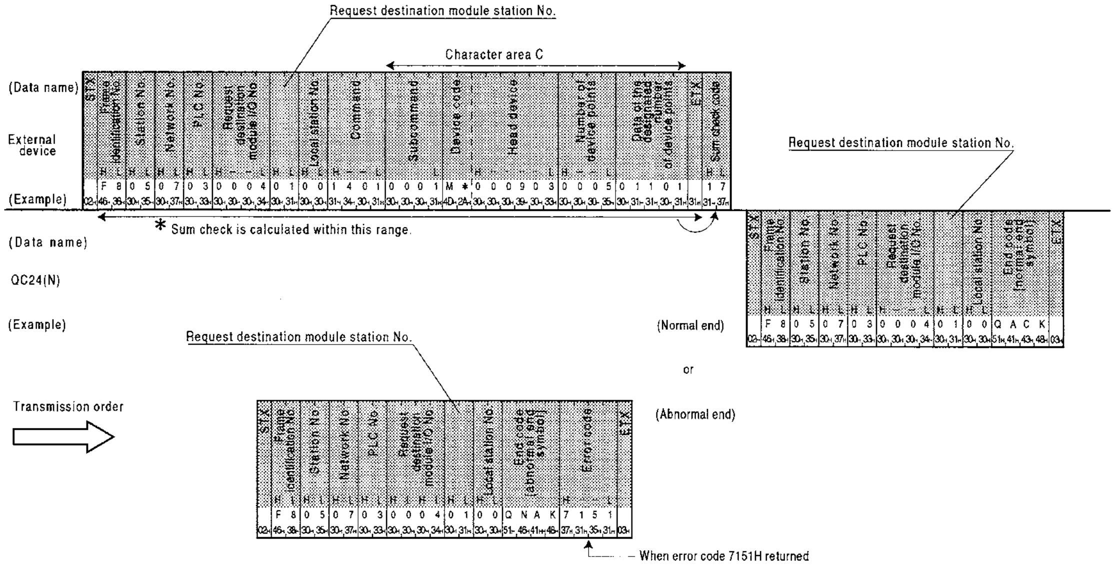
2 Communicating using control procedure format 2

(ASCII mode QnA extension frame format 2)

Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the contents of five points from X40 to X44 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
When external device writes data to PLC	(Example) When using a 1401 command to write data to five points from M903 to M907 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added. (2) When sum check is enabled, the sum check of only the characters of the * part in the illustrations above is calculated. (3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats. (4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0ms to 150 ms range. (See Section 14.7.4.)

3 When communicating using control procedure format 3

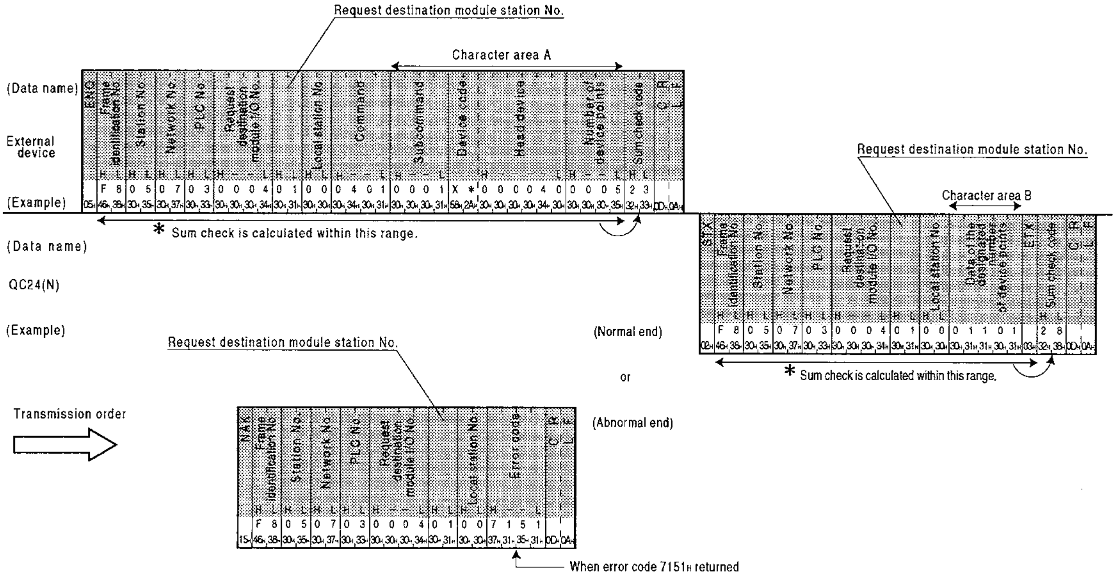
(ASCII mode QnA extension frame format 3)

Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the contents of five points from X40 to X44 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
When external device writes data to PLC	(Example) When a 1401 command is used to write data to five points from M903 to M907 of another station's QnACPU (Section 6.1 2 ③ ★ station) 
Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added. (2) When sum check is enabled, the sum check is calculated only for the * part shown in the illustrations above. (3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats. (4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0 ms to 150 ms range. (See Section 14.7.4.) (5) When the external device and PLC CPU system configuration is m: n, control procedure format 3 is not used during data transfer.

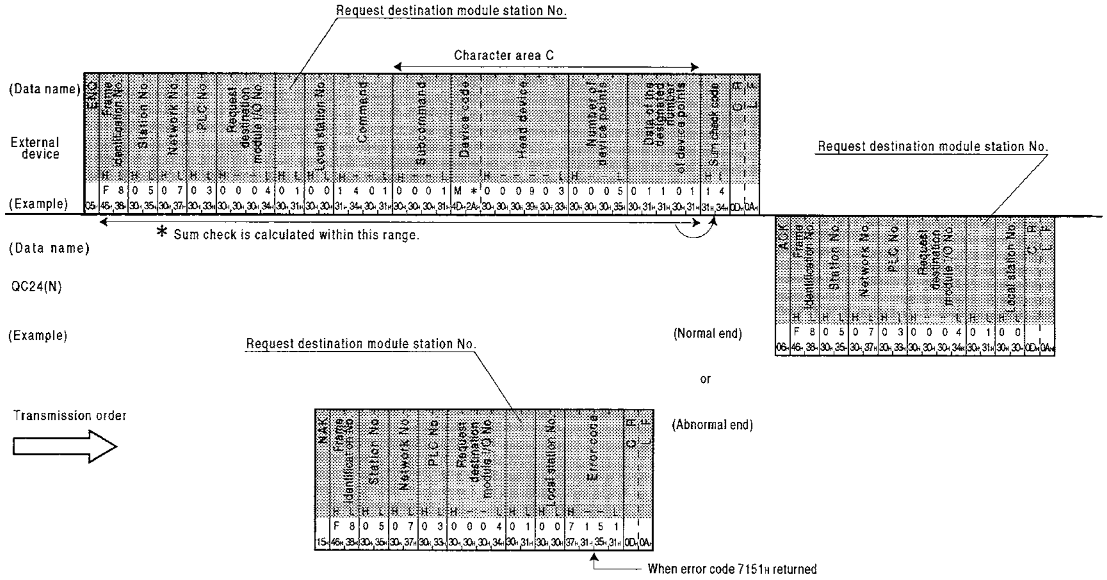
4 When communicating using control procedure format 4

(ASCII mode QnA extension frame format 4)

<table>
<tr><th>Contents</th><th>Control procedure (Protocol)</th></tr>
<tr><td>When external device reads PLC data</td><td>
(Example) When using a 0401 command to read the contents of five points from X40 to X44 of another station's QnACPU
(Section 6.1 2 ③ ★ station)



</td></tr>
<tr><td>When external device writes data to PLC</td><td>
(Example) When a 1401 command is used to write data to five points from M903 to M907 of another station's QnACPU
(Section 6.1 2 ③ ★ station)

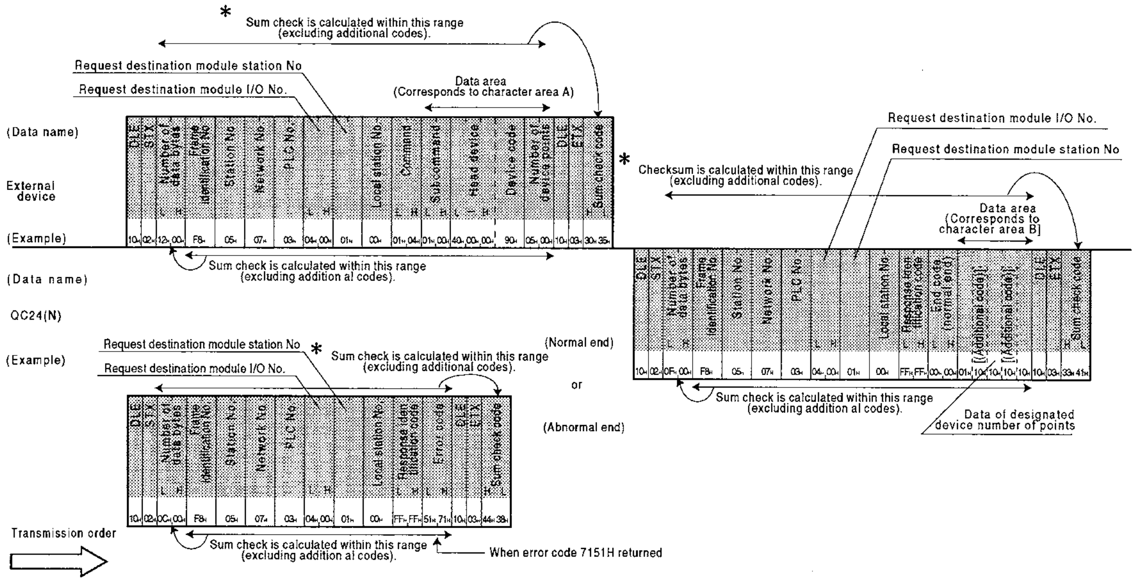
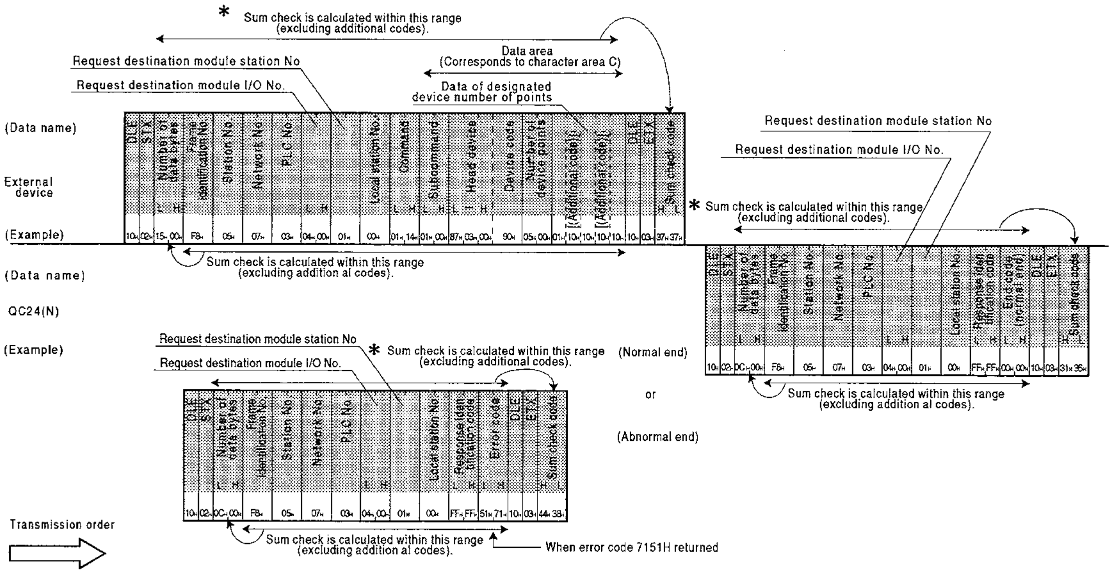


</td></tr>
<tr><td>Notes</td><td>
(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2.) When sum check is disabled, the sum check code is not added.
(2) When sum check is enabled, the sum check is calculated only for the * part shown in the illustrations above.
(3) The contents of [Character area A], [Character area B], and [Character area C] in the illustrations above depend on the processing contents. See the description of each command for more information. The contents of each character area are the same for all four formats.
(4) The time interval from reception of a command message to transmission of a response message by the QC24(N) can be set within the 0 ms to 150 ms range. (See Section 14.7.4.)
</td></tr>
</table>

6.1.3 Binary mode QnA extension frame data communications format

(Control procedure format 5)

(Binary mode QnA extension frame format 5)

Contents	Control procedure (Protocol)
When external device reads PLC data	(Example) When using a 0401 command to read the contents of five points from X40 to X44 of another station's QnACPU (Section 6.1 [2]③ ★ station) 
When external device writes data to PLC	(Example) When using a 1401 command to write data to five points from M903 to M907 of another station's QnACPU (Section 6.1 [2]③ ★ station) 

Notes	(1) The sum check code is added only when sum check is enabled. (See Section 4.3.2). When sum check is set to disabled, the sum check code is not added. (2) When sum check is enabled. the sum check is calculated only for the data of the * part in the illustrations (except [10H] added according to (5) below) and is converted to ASCII code. (3) The contents of the "data area" (areas corresponding to ASCII mode [Character area A], [Character area B], and [Character area C]) in the illustrations depends on the processing contents. See the description of each command for more information. (4) The time from reception of a command message to transmission of the response message by the QC24(N) can be set within the 0 ms to 150 ms range. (See Section 14.7.4.) (5) When the data of the * part in the illustrations includes [10H] data, [10H] (DLE code) is added immediately in front of the data before the data is sent. (The data is sent as [10H] → [10H] + [10H].) However, the added [10H] are not included in the [Number of Data Bytes] to be sent. (6) When the external device and PLC CPU configuration is m: n, control procedure format 5 cannot be used during data transfer.

6.1.4 Contents of data designation items of each format at QnA (extension) frame

This section describes the designation contents of each data name designated in the control procedure of each QnA frame and QnA extension frame format.

1 Control code (ASCII mode, binary mode)

The following shows the codes and contents of the data (message head data, etc.) that have a special meaning for QC24(N) transmission control in each control procedure.
The control codes used by each ASCII mode frame are indicated by a ○ mark in the ASCII mode column in the table.
The control codes used by the binary mode QnA extension frame is indicated by a ○ mark in the binary mode column in the table.
The way the control codes are used in messages is the same.

Symbol	Code (hexadecimal)	Contents	ASCII mode	Binary mode	Symbol	Code (hexadecimal)	Contents	ASCII mode	Binary mode
NUL	00H	Null	○		CL	0CH	Clear	○	
STX	02H	Start of Text	○	○	CR	0DH	Carriage Return	○	
ETX	03H	End of Text	○	○	DLE	10H	Data Link Escape		○
EOT	04H	End of Transmission	○		NAK	15H	Negative Acknowledge	○	
ENQ	05H	Enquiry	○			F6H	(System use)		○
ACK	06H	Acknowledge	○		QnA frame identification No.	F8H	(QnA extension frame identification code)	○	○
LF	0AH	Line Feed	○			F9H	(QnA frame identification code)	○	
—	—	—				FAH	(System use)	○	○

POINT

When [Number of Data Bytes] to [Data Area] in a message includes [10H] user data when binary mode the QnA extension frame is used to transfer data, the [10H] DLE code (represented by additional code in the table) is added immediately before the data and the data is transferred. (Transferred as [10H] → [10H] + [10H].)
The QC24(N) adds the response message.
An example of the message construction is shown in (Example) of Section 6.1.3.

(a) Null codes (00H) are ignored in all messages. Therefore, even if there are Null codes in a message, they are not processed.

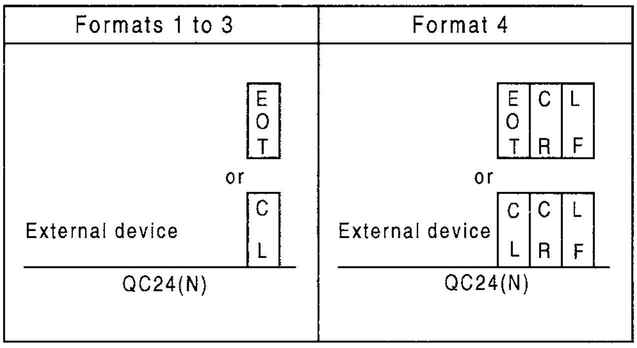
(b) EOT and CL are codes for initializing the transmission sequence for data communications in the dedicated protocol ASCII mode and place the QC24(N) in the state in which it waits to receive commands from an external device.
When performing the following at an external device, send EOT or CL to the QC24(N), depending on the format used.

① A read/write request issued by the immediately preceding command is canceled. (When a write request was issued, and data was already written to the PLC CPU, the write request cannot be canceled.)

② Before commands are sent, the QC24(N) is placed into the command receive wait state.

③ If data communications cannot be carried out normally, the system will enter the same state as when the QC24(N) was started.

The following shows the message construction when sending EOT or CL.



* when EOT or CL is sent, only the data shown at the left is sent.
The station No., PLC No., etc. do not have to be sent.

When the QC24(N) receives EOT or CL, it proceeds as follows:

- Terminates read/write processing performed for the PLC CPU by request from an external device.
  In this case, the QC24 does not send a response message (area B shown in Section 6.1) for the command received last.
- Initializes the dedicated protocol transmission sequence of the interface that received EOT or CL and enters the command receive wait state.
- There is no response message for EOT and CL. (Nothing is sent to the external device.)
- When EOT or CL is received while the on-demand function (function that sends data from the PLC CPU to an external device, see Section 6.10) is executing, the QC24(N) terminates on-demand function data transmission to the external device.

POINT

During data communications in the dedicated protocol binary mode, the transmission sequence can be initialized by using the transmission sequence initialize command.

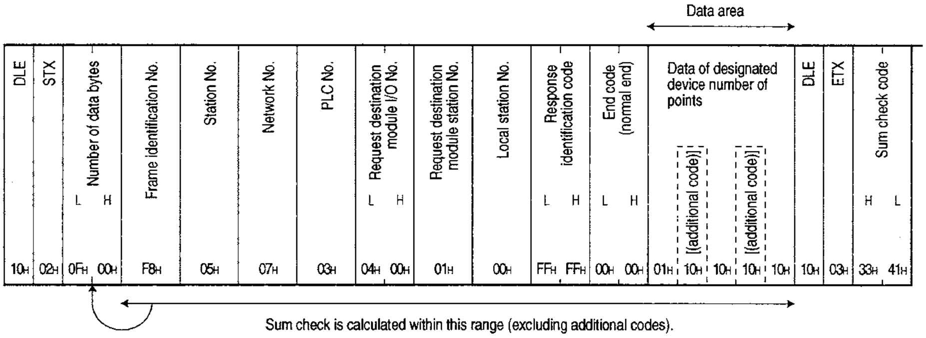
2 Block No. (ASCII mode (format 2))

"Block No." is an arbitrary number that is given a meaning by the relevant message at an external device. It is used in data management No., etc.
The block numbers range is 00H to FFH range. Block numbers are converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.
The QC24(N) only checks if the block number is designated within the correct range.
It does not check if the block numbers sent by command messages are sequential.

3 Number of data bytes (binary mode)

"Number of data bytes" is used to inform the opposite device of the total number of data, excluding additional codes, between the frame identification No. and data area or frame identification No. and end code (error code). (Since the QC24(N) does not check the number of data bytes in command messages received from an external device, it can also be designated by dummy data 00H, 00H.)
Number of data bytes is transmitted as a 2-byte value in Low byte (L: bit0 to 7), High byte (H: bits 8 to 15) order.

(Example) Response message when data was read from PLC CPU



4 Frame identification No. (QnA frame, QnA extension frame)

"Frame identification No." is used to identify if the message to be transferred is QnA frame or QnA extension frame.

The following shows the frame identification numbers that are designated during data communications.

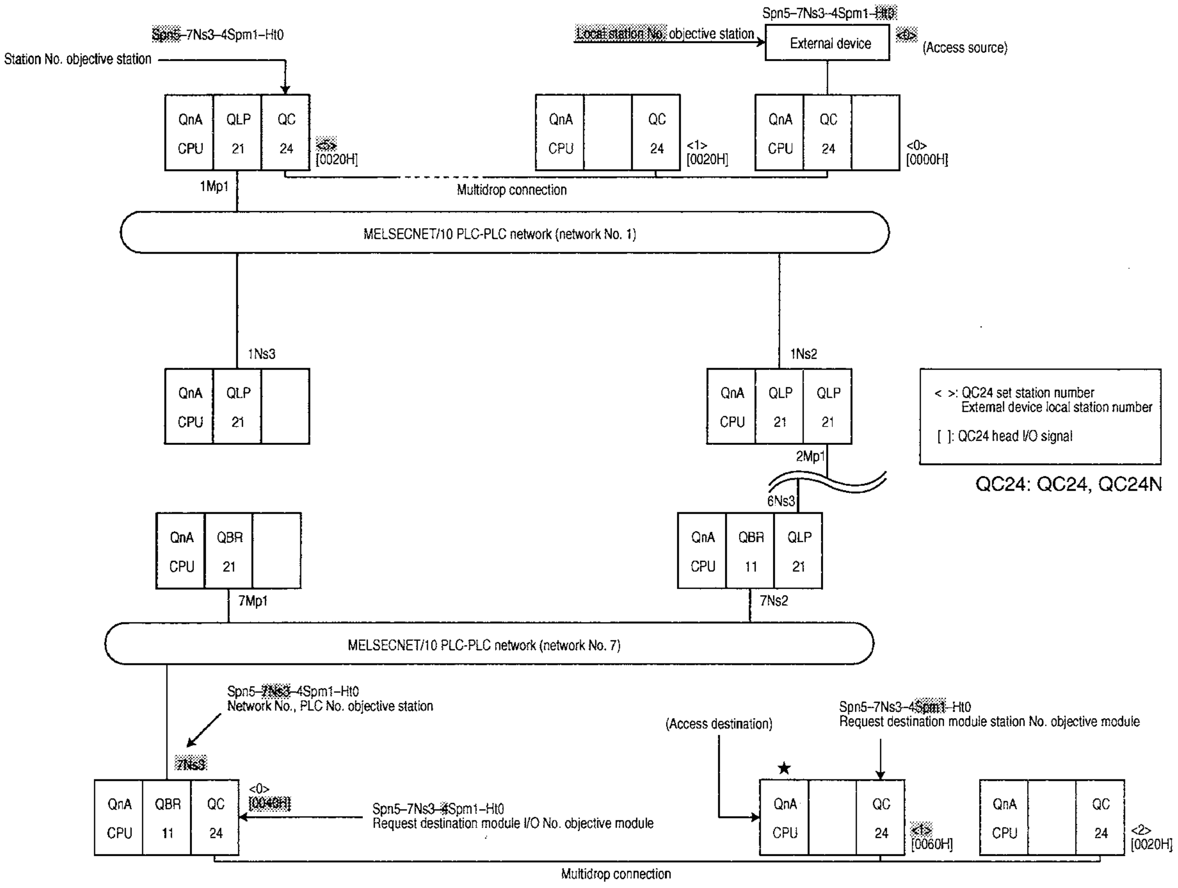
Mode	Frame	Frame identification No.	Note
ASCII mode	QnA frame	"F9"	Two characters sent in "F", "9" order.
	QnA extension frame	"F8"	Two characters send in "F", "8" order.
Binary mode	QnA extension frame	F8H	One bytes of F8H data is sent.

5 Station No. to local station No.

The station No. to local station No. data designate the PLC station to be accessed by an external device. The four sets of data shown below designate the route up to the access destination.

- Station No.
  Designates the QC24(N) (including multidrop QC24(N)) of the external device that is passed through last by QC24(N) set station No. when an external device accesses the PLC.
- Network No., PLC No.
  Designate the number of the network system/data link system that is passed through last and the PLC No. (station No.) on the relevant system by network module, etc. set number when an external device accesses another station's PLC.
- Request destination module I/O No., Request destination module station No.
  Designate the connection source QC24(N) and access destination QC24(N) of the multidrop connection when an external device accesses another station's PLC through a network system and multidrop connection QC24(N).
  The request destination module I/O No. designates the multidrop connection source QC24(N) by I/O signal head No.
  The request destination module station No. designates the access destination QC24(N) by QC24(N) set station No.
- Local station No.
  Designates the external device's station number by the number [0] (fixed value).

(Example) The following shows the station No. to local station No. objective stations and networks when an external device accesses the ★ station QnACPU in the following system configuration.
(See Section 6.1 2 for the meaning of Spn5-7Ns3-4Spm1-Ht0.)



(a) Station No. (QnA frame, QnA extension frame)

① Data communications in ASCII mode
00H to 1FH (0 to 31) range. Converted to 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
A 1-byte value from [00H] to [1FH] (0 to 31) transmitted.

③ A designation example is given at the end of this section.

POINTS

(1) The station No. switch is set as a decimal number. However, the ASCII mode station No. is designated as a hexadecimal number.
Example) Setting switch station No. "10"......Station No. "0A" on protocol

(2) When the global function described in Section 6.8 is used, designation of the station No. on the protocol is "FF"/FFH.
When a number from 0 to 31 (00H to 1FH) is designated, X (n + 1) A/X (n + 1) B of only the designated station is turned ON. Other stations are not turned on. See Section 6.8 for more information.

(3) When the external device and PLC CPU system configuration is m: n, when data is transferred by QnA frame or QnA extension frame, the external device station number must not be the same as the QC24(N) station number.
See Section 17 for a description of the external device station number.

(b) Network number (QnA frame, QnA extension frame)

① Data communications in ASCII mode
A value within the range shown below is converted to 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The network numbers that are designated during data communications are shown below. A designation example is given at the end of this sections.

	External device access station	Network No. designated by external device
1	External device connection station (local station)	00H
2	Multidrop connection station from external device connection station	00H
3	Station on MELSECNET/10 (Except 1 and 2 above.)	01F to EFH (1 to 239) (Access station network No.)
4	Station on MELSECNET(II) (Except 1 and 2 above.)	00H
5	Station on MELSECNET/B (Except 1 and 2 above.)	00H
6	Multidrop connection station through MELSECNET/10 connection station	01H to EFH (1 to 239) (Network No. passed through last)
7	Station through network module set by [Effective Module When Accessing Another Station]	FED (254)

POINTS

(1) The network module network No. switch is set as a decimal number, but the ASCII mode network No. is designated as a hexadecimal number.

Example) Setting switch network No. "10"......Network No. "0A" designated on protocol

(2) The PLC CPU cannot be accessed through a MELSECNET/10 with a network No. from 240 to 255.

(3) When designating network No. FEH and accessing another station through a QC24(N) (or computer link module) incorporated in a data link system or network system, use the CP function to set the following parameters in the QC24(N) (computer link module) station PLC CPU.

Setting module enabled for access from other stations...

Set in the number of modules setting and sets the module through which an external device accesses another station.

(4) Designate the network No. using the No. shown in the table. Sometimes a response will not be returned when a No. other than that shown in the table is designated.

(c) PLC No. (QnA frame, QnA extension frame)

① Data communications in ASCII mode
A value within the range shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The PLC numbers that are designated during data communications are shown below. A designation example is given at the end of this section.

	External device access station	PLC number designated by external device
1	External device connection station (Local station)	FFH*1
2	Multipdrop connection station from external connection station	FFH*1
3	Station on MELSECNET/10 (Except 1 and 2 above and 4 below.)	01H to 40H (1 to 64) (Station No. of access station)
4	Remote I/O network master station on MELSECNET/10 (When the external device is connected to the QC24 of a remote station in a remote I/O network.)	7DH (125)
5	Master station on MELSECNET(II) (Except 1 and 2 above.)	00H
6	Local station/remote station on MELSECNET(II) (Except 1 and 2 above.)	01H to 40H (1 to 64) (Station No. of access station)
7	Station on MELSECNET/B	(Same as 5 and 6 above.)
8	Multidrop connection station via MELSECNET/10 connection station	01H to 40H (1 to 64) (Station No. of last station passed through)

*1 PLC No. FFH can be designated only when (b) Network No. is 00H.

POINTS

(1) The station No. switch is set as a decimal number, but in the ASCII mode, the PLC No. is designated as a hexadecimal number.

Example) Setting switch station No. "16"......Designated PLC No. "10" protocol

(2) When the on-demand function described in Section 6.9 and Chapter 7 is used, the QC24(N) sends "FE"/FEH as the PLC No. on the protocol.
See Section 6.9 and Chapter 7 for more information.

(d) Request destination module I/O No. (QnA extension frame)

① Data communications in ASCII mode
When the I/O signals of the objective QC24(N) are expressed by four digits, the higher 3 digits, or 03FFH, are converted to a 4-digit ASCII (hexadecimal) code and sequentially transmitted from the most significant digit.

(Example) When QC24(N) I/O signals are 0080 to 009FH
The request destination module I/O number "0008" is sequentially transmitted from the first "0".

② Data communications in binary mode
When the I/O signals of the objective QC24(N) are expressed by four digits, the higher 3 digits, or two bytes of 03FFH data, are transmitted in Low byte (L: bits 0 to 7), High byte (H: bits 8 to 15) order.

(Example) When QC24(N) I/O signals are 0080H to 009FH
The request destination module I/O No. 0008H is transmitted in 08H, 00H order.

③ The following shows the request destination module I/O No. that is designated during data communications. A designation example is shown at the end of this section.

	External device access station	**Request destination module I/O No. designated by external device**
1	Station other than the station below.	03FFH
2	Station on multidrop connection (Conforms to the above when the QnACPU of the MELSECNET/10 connection station passed through last is accessed.)	000H to 01FFH

(e) Request destination module station No. (QnA extension frame)

① Data communications in ASCII mode
A value within the range shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The following shows the request destination module station No. that is designated during data communications. A designation example is given at the end of this section.

	External device access station	**Request destination module dtation No. designated by external device**
1	Stations other than the station below.	00H (0)
2	Station on multidrop connection (Conforms to 1 above when the QnACPU of the MELSECNET/10 connection station passed through last is accessed.)	00H to 1FH (0 to 31)

POINT

The station No. switch is set as a decimal number, but ASCII mode station number is designated as a hexadecimal number.
Example) Setting switch station No. "16"......Station number designated on protocol "10"

(f) Local station No. (QnA frame, QnA extension frame)

① During communications in the ASCII mode, "00" is transmitted.

② During communications in the binary mode, the 1-byte value [00H] is transmitted.

③ A designation example is given at the end of this section.

POINT

When the external device and PLC CPU system configuration is m: n, when data is transferred by QnA frame or QnA extension frame, the external device station number must be a number within the 00H to 1FH (0 to 31) range that does not duplicate the QC24(N) station No.
See Chapter 17 for a description of the external device station number.

6 Command

Designates if the PLC accessed from an external device is accessed for read, write, or other operation.

① Data communications in ASCII mode
The commands described in Sections 6.2 to 6.13 are converted to 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Example) Bit units batch read command
Command "0401" is sequentially transmitted from the first "0".

② Data communications in binary mode
The commands described in Sections 6.2 to 6.13 are used as 2-byte values (hexadecimal) and are transmitted in Low byte (L: bits 0 to 7), High byte (H: bits 8 to 15) order.

(Example) Bit units batch read command
Command 0401H is sent in 01H, 04H order.

7 Character area □ (data area)

The following describes the application of each character area.

Character area A .... Data for execution by the PLC CPU of a read request designated by command from the QC24(N).
Character area B .... Data returned to the external device by the QC24(N) in response to a request designated by command.
Character area C .... Data for execution by PLC CPU of a write request designated by command from the QC24(N).

The contents of the character areas (data areas) depends on the command send from the external device. See Sections 6.2 to 6.13 for more information.

① During data communications in the ASCII mode, the character areas are converted to ASCII code and transmitted.

② During data communications in the binary mode, the character areas are transmitted in binary code.

③ See Section 6.1.5 for the approach to the character area send data.

8 Sum check code (QnA frame, QnA extension frame)

The sum check code is the lower byte (8 bits) of the sum of binary addition of the data within the sum check range (see Sections 6.1 to 6.1.3) in a message.

When [Sum Check Enable/Disable Setting] is set to [Enable] by transmission specifications switch SW06 setting (see Section 4.3.2), the sum check code must be added.

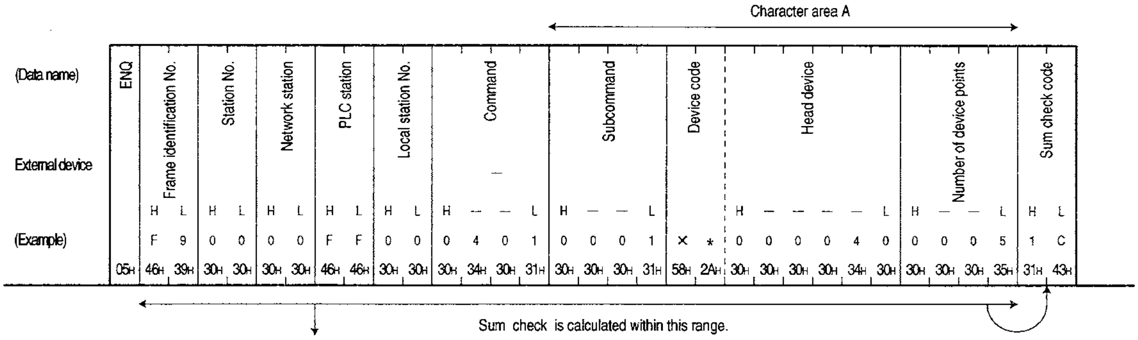
When sum check is enabled, QC24(N) generates the sum check code and adds it to the transmit message. The QC24(N) also checks the sum check code in the receive message. When sum check is disabled, the QC24(N) does not add the sum check code to the transmit message. The QC24(N) processes receive messages as if they did not contain a sum check code.

① During communications in the ASCII and binary modes, the sum check code is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② During data communications in the binary mode, the sum check objective range addi tional code (see Section 6.1.4 1 Point) is removed and the sum check is calculated.

③ The examples below show the contents of the sum check code.

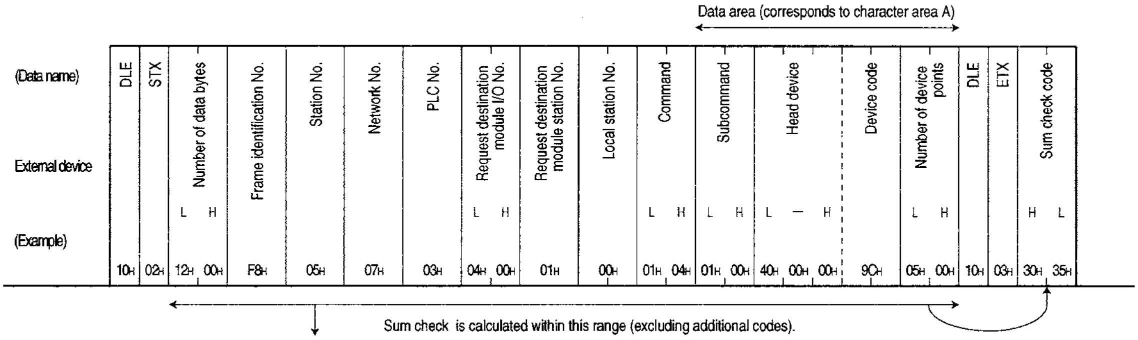
(Example 1) When data read using ASCII mode QnA frame format 1.



46H+39H+30H+30H+30H+30H+46H+46H+30H+30H+30H+34H+30H+31H+30H+30H+
30H+31H+58H+2AH+30H+30H+30H+30H+34H+30H+30H+30H+30H+35H=61CH

The sum check code is "1C" (ASCII code 31H, 43H).

(Example 2) When data read using binary mode QnA extension frame



12H+00H+F8H+05H+07H+03H+04H+00H+01H+00H+01H+04H+01H+00H+40H+00H+
00H+9CH+05H+00H=205H

The sum check code is "05" (ASCII code 30H, 35H).

9 Response identification code (binary mode)

The response identification code tells the external device that a response message was received for a request that it sent. The 2 byte value [FFFFH] is transmitted.

10 End code (binary mode normal end)

The end code tells the external device that the PLC CPU normally processed a request that it sent. The 2-byte value [0000H] is transmitted.

11 Error code (ASCII mode, binary mode)

The error code tells the external device that PLC CPU processing of a request that it sent ended abnormally.

① Data communications in ASCII mode
The error code is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Example) Error code 7151H

The error code sent to the external device is "7151", and is sequentially transmitted from the "7".

② Data communications in binary mode
The error code is used as a 2-byte value and is transmitted in Low byte (L: bits 0 to 7), H byte (H: bits 8 to 15) order.

(Example) Error code 7151H
The error code is sent to the external device in 51H, 71H order.

③ If two or more error codes are generated at the same time, the QC24(N) sends the error code detected first.

④ See Section 22.1 for a detailed description of the error codes.

Notes

(1) [Message wait] time cannot be designated in the QnA frame, QnA extension frame, and QnA simplified frame shown in Chapter 8 control procedures. During QnA frame, QnA extension frame and QnA simplified frame data communications, the QC24 buffer memory [Message Wait Time Designation] area (addresses: 11EH, 1BEH) designates the message wait time.
Transfer data with external devices connected to the QC24(N) RS422/485 interface by designating the external device hardware gate OFF time, or longer, as the message wait time, including A compatible frame data communications.

(2) The following gives designation examples of [Station No.] to [Own Station No.] from among the data that is designated in each control procedure during data communications using QnA frame and QnA extension frame control procedure.

(How to read the figures and tables)

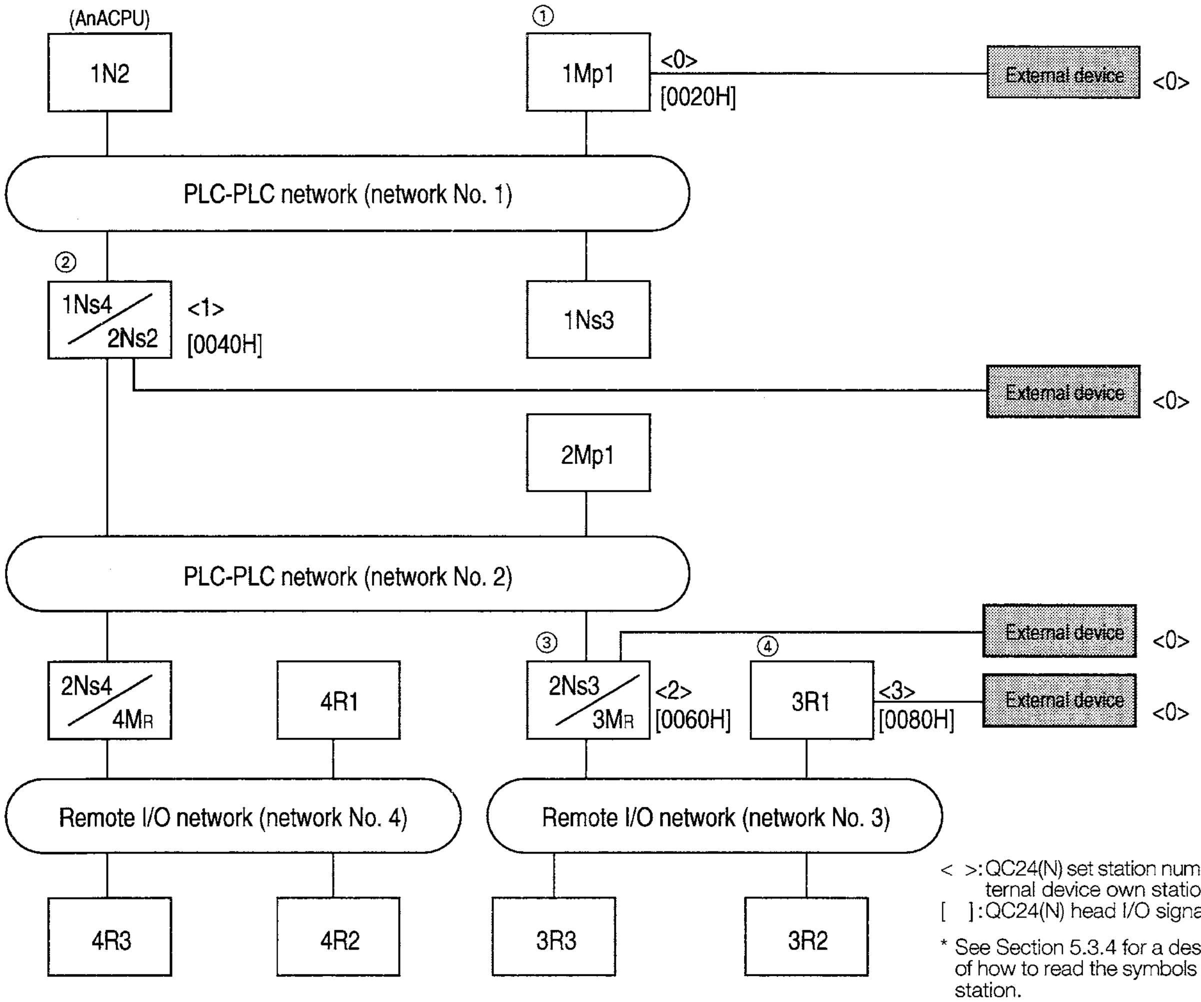
- The contents of the number in the symbols (< >, [ ]) shown at the right side of the station in the figures are given below.

  < > : QC24(N) set station No. of that station
  [ ] : Head I/O signal of QC24(N) of that station

- (n) in the [Data name] column of the tables indicates the description number of the relevant data of Section 6.1.4 5. The description symbols of the relevant data of Section 6.1 2 are indicated by examples.
- The number in the [Designated Value When Accessed From External Device] column in the tables shows the designation value to the data shown at the left side of the table when the relevant station shown at the top of the table is accessed.

MEMO

(Designation example 1) When external device and connection station/normal station are all QnACPU



< >: QC24(N) set station number, external device own station No.
[ ]: QC24(N) head I/O signal
* See Section 5.3.4 for a description of how to read the symbols of each station.

When external device connection station is ①

Data name	Designated value when accessed from external device												
	1Mp1	**1N2**	**1Ns3**	**1Ns4/2Ns2**	**2Mp1**	**2Ns3/3MR**	**2Ns4/4MR**	**3R1**	**3R2**	**3R3**	**4R1**	**4R2**	**4R3**
(a) Station No. Spn□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H
(b) Network No. □Mp	00H	01H	01H	01H	02H	02H	02H	03H	03H	03H	04H	04H	04H
(c) PLC No. Mp□	FFH	02H	03H	04H	01H	03H	04H	01H	02H	03H	01H	02H	03H
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H

When external device connection station is ②

Data name	Designated value when accessed from external device												
	1Mp1	**1N2**	**1Ns3**	**1Ns4/2Ns2**	**2Mp1**	**2Ns3/3MR**	**2Ns4/4MR**	**3R1**	**3R2**	**3R3**	**4R1**	**4R2**	**4R3**
(a) Station No. Spn□	01H	01H	01H	01H	01H	01H	01H	01H	01H	01H	01H	01H	01H
(b) Network No. □Mp	01H	01H	01H	00H	02H	02H	02H	03H	03H	03H	04H	04H	04H
(c) PLC No. Mp□	01H	02H	03H	FFH	01H	03H	04H	01H	02H	03H	01H	02H	03H
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H

When external device connection station is ③

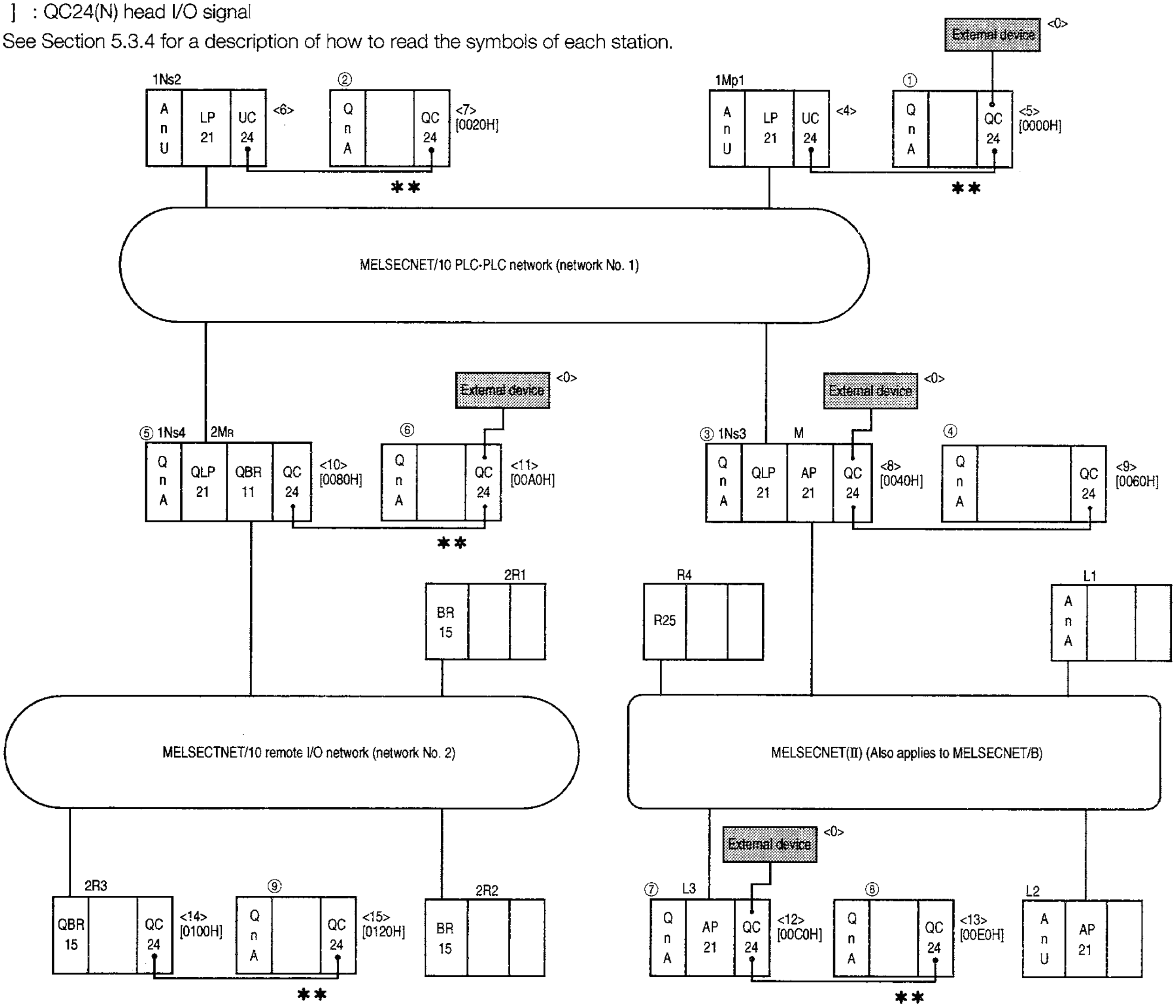
Data name	Designated value when accessed from external device												
	1Mp1	**1N2**	**1Ns3**	**1Ns4/2Ns2**	**2Mp1**	**2Ns3/3MR**	**2Ns4/4MR**	**3R1**	**3R2**	**3R3**	**4R1**	**4R2**	**4R3**
(a) Station No. Spn□	02H	02H	02H	02H	02H	02H	02H	02H	02H	02H	02H	02H	02H
(b) Network No. □Mp	01H	01H	01H	02H	02H	00H	02H	03H	03H	03H	04H	04H	04H
(c) PLC No. Mp□	01H	02H	03H	02H	01H	FFH	04H	01H	02H	03H	01H	02H	03H
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H

When external device connection station is ④

Data name	Designated value when accessed from external device												
	1Mp1	**1N2**	**1Ns3**	**1Ns4/2Ns2**	**2Mp1**	**2Ns3/3MR**	**2Ns4/4MR**	**3R1**	**3R2**	**3R3**	**4R1**	**4R2**	**4R3**
(a) Station No. Spn□	03H	03H	03H	03H	03H	03H	03H	03H	Cannot be accessed				
(b) Network No. □Mp	01H	01H	01H	02H	02H	03H	02H	00H					
(c) PLC No. Mp□	01H	02H	03H	02H	01H	7DH	04H	FFH					
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH					
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H	00H					
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H	00H					

(Designation example 2) When the QnACPU is used as an intermediate station of a network system + data link system

✱✱ : Multidrop connection station
< > : QC24(N), UC24 set station No.
[ ] : QC24(N) head I/O signal
* See Section 5.3.4 for a description of how to read the symbols of each station.



When external device connection station is ①

Data name	Designated value when accessed from external device																
	1Mp1	1Ns2	1Ns3/ M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	④	⑥	⑧	⑨
(a) Station No. Spn□	04H	04H	04H	04H	Cannot be accessed							05H	Cannot be accessed				
(b) Network No. □Mp	01H	01H	01H	01H								00H					
(c) PLC No. Mp□	FFH	02H	03H	04H								FFH					
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH								03FFH					
(e) Request destination module station No. Spm□	00H	00H	00H	00H								00H					
(f) Local station No. Ht□	00H	00H	00H	00H								00H					

When external device connection station is ③

Data name	Designated value when accessed from external device																
	1Mp1	1Ns2	1Ns3/M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	④	⑥	⑧	⑨
(a) Station No. Spn□	08H	08H	08H	08H	08H	08H	08H	08H	08H	08H	08H	Cannot be accessed		09H	08H	Cannot be accessed	08H
(b) Network No. □Mp	01H	01H	00H	01H	02H	02H	02H	00H	00H	00H	00H			00H	01H		02H
(c) PLC No. Mp□	01H	02H	FFH	04H	01H	02H	03H	01H	02H	03H	04H			FFH	04H		03H
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH			03FFH	0008H		0010H
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H			00H	0BH		0FH
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H	00H			00H	00H		00H

When external device connection station is ⑥

Data name	Designated value when accessed from external device																
	1Mp1	1Ns2	1Ns3/M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	④	⑥	⑧	⑨
(a) Station No. Spn□	0AH	0AH	0AH	0AH	0AH	0AH	0AH	Cannot be accessed						0AH	0BH	Cannot be accessed	0AH
(b) Network No. □Mp	01H	01H	01H	00H	02H	02H	02H							01H	00H		02H
(c) PLC No. Mp□	01H	02H	03H	FFH	01H	02H	03H							03H	FFH		03H
(d) Request destination module I/O No. □Spm	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH	03FFH							0004H	03FFH		0010H
(e) Request destination module station No. Spm□	00H	00H	00H	00H	00H	00H	00H							09H	00H		0FH
(f) Local station No. Ht□	00H	00H	00H	00H	00H	00H	00H							00H	00H		00H

When external device connection station is ⑦

Data name	Designated value when accessed from external device																
	1Mp1	1Ns2	1Ns3/M	1Ns4 2MR	2R1	2R2	2R3	L1	L2	L3	R4	①	②	④	⑥	⑧	⑨
(a) Station No. Spn□	Cannot be accessed		0CH	Cannot be accessed								0CH	Cannot be accessed			0DH	Cannot be accessed
(b) Network No. □Mp			00H									00H				00H	
(c) PLC No. Mp□			00H									FFH				FFH	
(d) Request destination module I/O No. □Spm			03FFH									03FFH				03FFH	
(e) Request destination module station No. Spm□			00H									00H				00H	
(f) Local station No. Ht□			00H									00H				00H	

6.1.5 Character area transmission data

This section explains the transmission data handled as character areas when using commands to transfer data between external devices and PLC CPU.

The transmission data shown in the examples is contained in character area B in the case of read and monitor, and in character area C in the case of write, test, and monitor data registration.

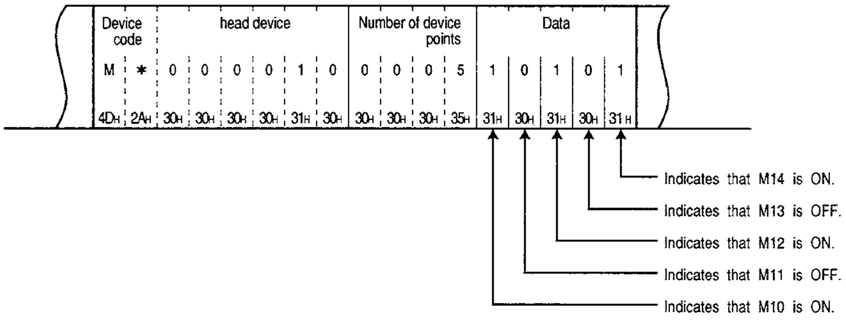
1 Data communications using the ASCII mode QnA frame and QnA extension frame control procedures

(a) Bit device memory read and write

The bit device memory can be read and written in bit units (1 device point) or word units (16 device points).
These units are described below.

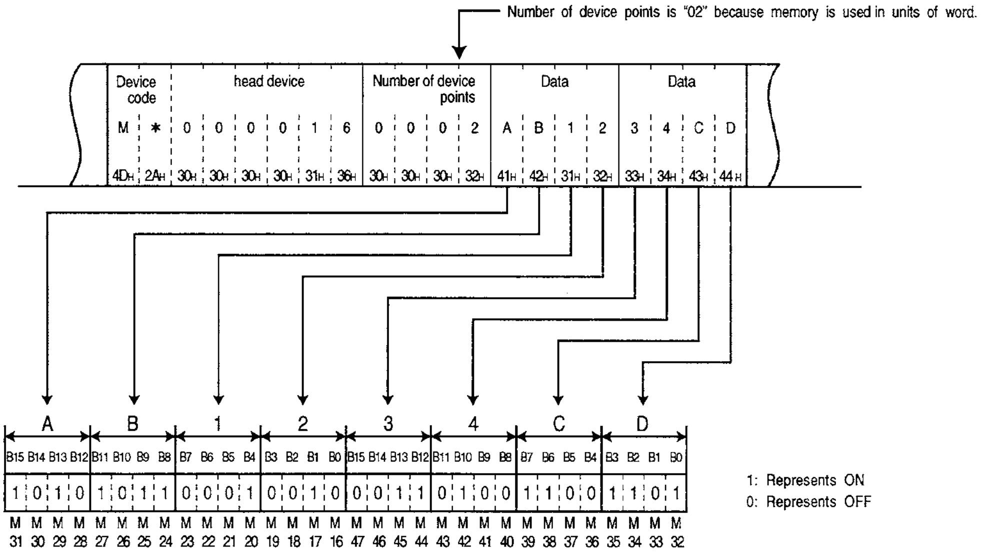
① Bit units (1 point)
When the bit device memory is handled as bit units, the designated number of device points from the designated head device in sequence from the left are represented as "1" (31H) if the device is ON and "0" (30H) if the device is OFF.

Example) Indication of the ON/OFF status of 5 points from M10



② Word units (16 points)
When the bit device memory is handled as word units, each word is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

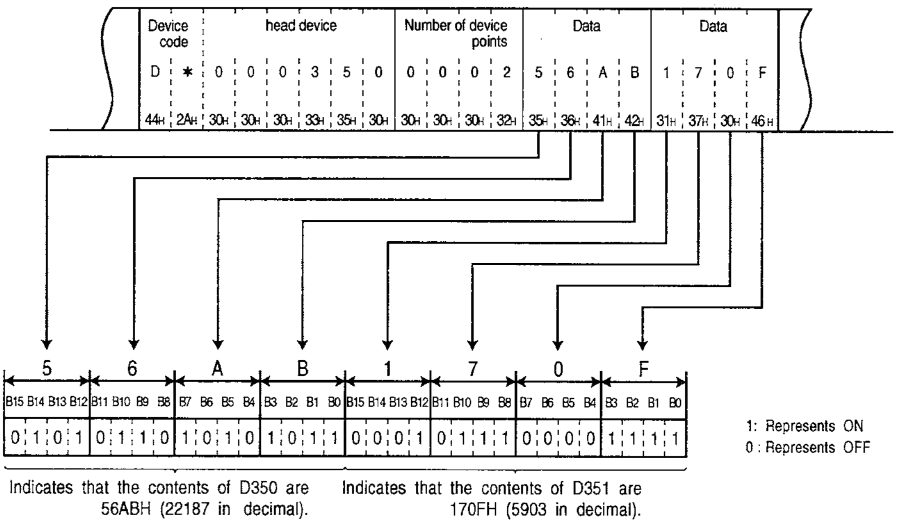
Example) Indication of the ON/OFF status of 32 points from M16



(b) Word device memory read and write

Each word of the word device memory is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

Example) Indication of storage contents of data registers D350 and D351



POINTS

(1) When designating letters in the character field, use upper case code.

(2) When data other than an integer value (real number, character string, etc.) was stored in a word device memory to be read, the QC24(N) reads the stored value as an integer value.

(Example 1) When the real number (0.75) is stored in D0 and D1, it is read as the following integer values:
D0 = 0000H, D1 = 3F40H

(Example 2) When the character string ("12AB") is stored in D2 and D3, it is read as the following integer values:
D2 = 3231H, D3 = 4241H

Note

The same thinking is used in regards to the word unit data and word device memory used by the buffer memory read and write functions, etc.

2 Data communications using binary mode QnA frame control procedure

(a) Bit device memory read and write

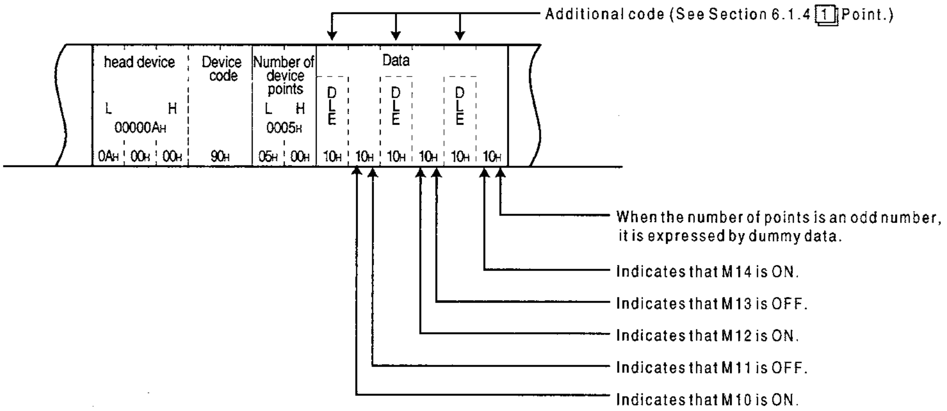
The bit device memory can be handled in bit units (1 device point) or word units (16 device points).

These units are described below.

① Bit units (1 point)

When the bit device memory is handled as bit units, one point is designated by four bits and the designated number of device points from the designated head device in sequence from the higher bit are represented by [1] if the device is ON, or by [0] if the device if OFF.

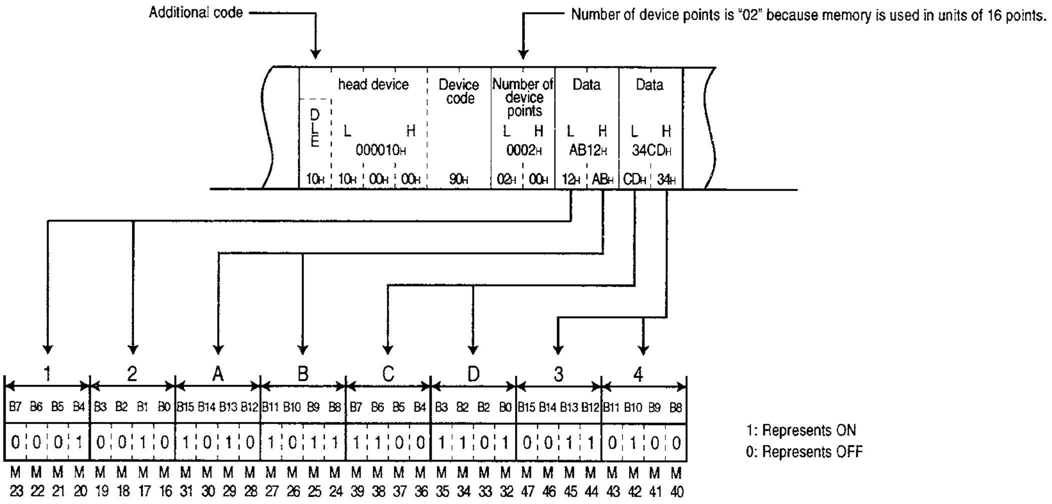
Example) Indication of the ON/OFF status of 5 points from M10



② Word units (16 points)

When the bit device memory is handled as word units, each point is designated by 1 bit and the number of designated device points from the designated head device are sequentially expressed in 16 points units by Low byte (L: bits 0 to 7) and High byte (bits 8 to 15).

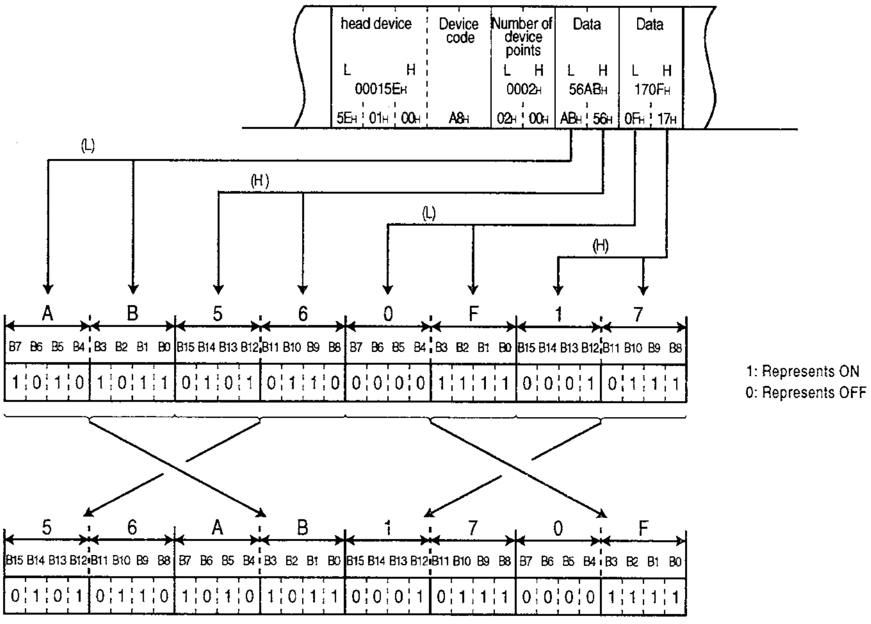
Example) Indication of ON/OFF status of 32 points from M16



(b) Word device memory read and write

Each word is designated by 16 bits and the designated number of points from the designated head device are sequentially expressed in point units by Low byte (L: bits 0 to 7) and High byte (H: bits 8 to 15).

Example) Indication of storage contents of data registers D350 and D351



1: Represents ON
0: Represents OFF

Indicates that the contents of D350 are 56ABH (22187 in decimal).

Indicates that the contents of D351 are 170FH (5903 in decimal).

POINT

When data other than an integer value (real number, character string) are stored to a word device memory to be read, the QC24(N) reads the stored value as an integer value.

(Example 1) When the real number (0.75) is stored in D0 and D1, it is read as the following integer value:
D0 = 0000H, D1 = 3F40H

(Example 2) When the character string ("12AB") is stored in D2 and D3, it is read as the following integer value:
D2 = 3231H, D3 = 4241H

Note

The same thinking is used in regards to the word unit data and word device memory used by the buffer memory read and write functions, etc.

6.2 Device Memory Read/Write

This section describes the control procedure designation contents and designation examples when reading and writing device memory.

6.2.1 Command and character areas contents and device range

The following describes the commands, control procedure character areas (in binary mode, data areas), and the accessible devices range when reading and writing device memory.

1 Commands

Function	——	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Designated as a hexadecimal number.	Processing	Number of points processed per communication		PLC CPU status *1			Reference Section
				Access station - 1 [See Section 5.4.1 *7.]	Access station -2 [See Section 5.4.1 *8.]	During STOP	During RUN		
							Write enable set	Write disable set	
Batch read	Bit units	0 4 0 1 (0 0 □ 1)	Reads bit devices in units of points.	3952 points	256 points	○	○	○	6.2.1 6.2.2 6.2.3
	Word units	0 4 0 1 (0 0 □ 0)	Reads bit devices in units of 16 points.	480 words (7680 points)	32 words (512 points)				
			Reads word devices in units of ponts.	480 points	64 points				
Batch write	Bit units	1 4 0 1 (0 0 □ 1)	Writes data to bit devices in units of points.	3952 points	160 points	○	○	×	6.2.1 6.2.4 6.2.5
	Word units	1 4 0 1 (0 0 □ 0)	Writes to bit devices in units of 16 points .	480 words (7680 points)	10 words (160 points)				
			Writes to word devices in units of points.	480 points	64 points				
Random read	Word units	0 4 0 3 (0 0 □ 0)	Reads bit devices in units of 16 points and 32 points by designating the devices at random. *3	96 points	10 words (160 points)	○	○	○	6.2.1 6.2.6
			Reads word device in units of points and 2 points by designating the devices at random. *3		10 points				
Test (Random write)	Bit units	1 4 0 2 (0 0 □ 1)	Sets/resets bit devices in units of points by designating the devices at random. *3	94 points	20 points	○	○	×	6.2.1 6.2.7 6.2.8
	Word units	1 4 0 2 (0 0 □ 0)	Sets/resets bit devices in units of 16 points and 32 points by designating the units at random. *3	(See Section 6.2.8)	10 words (160 points)				
			Writes data to word devices in units of points and 2 points by designating the devices at random. *3		10 points				
Monitor data registration	Word units	0 8 0 1 (0 0 □ 0)	Registers the bit devices to be monitored in units of 16 points and 32 points. *2, 3	96 points	20 words (320 points)	○	○	○	6.2.1 6.2.9
			Registers the word devices to be monitored in units of points and 2 points. *3		20 points				
Monitor	Word units	0 8 0 2 (0 0 0 0)	Monitors the devices registered for monitoring.	(Number of registered points)		○	○	○	
Multiple block batch read	Word units	0 4 0 6 (0 0 □ 0)	Read data by treating n points of word devices or bit devices (one points is equivalent to 16 bits) as one block, or by specifying multiple blocks randomly.	480 points	(Unavailable)	○	○	○	6.2.1 6.2.10
Multiple block batch write	Word units	1 4 0 6 (0 0 □ 0)	Write data by treating n points of word devices or bit devices (one points is equivalent to 16 bits) as one block, or by specifying multiple blocks randomly.	480 points	(Unavailable)	○	○	×	

○ in the PLC CPU column of the table above, shows the executable state.

*1 Write to PLC CPU during RUN enable/disable is set by QC24(N) DIP switch SW07.
SW07 = ON...Write during RUN enabled, SW07 = OFF...Write during RUN disabled

*2 When a PLC CPU other than the A3HCPU and AnA, AnU, and QnACPU is used, device X (input) is the number of points processed per point. (When only X is designated, the number of processing points that can be transmitted at one time is one half the value given in the table.)
When the designated device includes X, make the number of processing points a number within the following range.
((X designated points × 2) + designated number of points of other device) ≤ number of points processed per communication

*3 The number of processing points other than that for the QnACPU is 1 point unit for a word device and 16 point unit for a bit device.

2 Character areas (data areas in binary mode)

This section describes the common contents of the character areas in each control procedure when an external device reads and writes data from and to the PLC.

POINTS

(1) The character area depends on the command used and other designation contents.
This section describes the data contents common to the character areas when the device memory to be read or written is designated directly.

(2) The character area data handled only by a certain command is described in the description of each command.

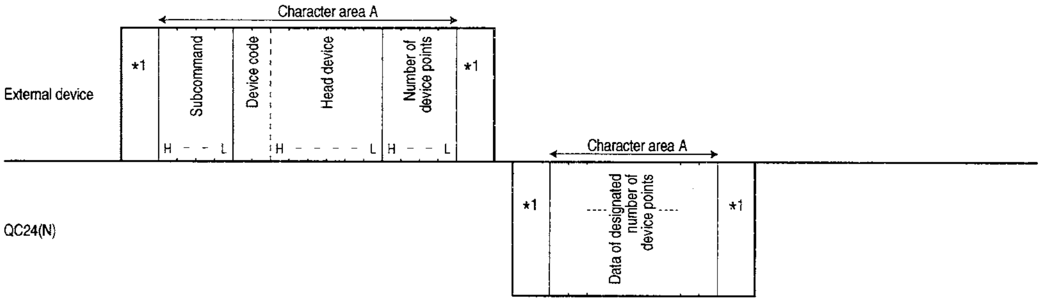
(3) The following sections describe the dedicated data handled by some of the functions and dedicated data handled by special designation.

- Section 6.2.6 .... Dedicated data designated by word units random read (command: 0403) and monitor data registration (command: 0801) functions.
- Section 6.2.11 .... Data used when extending and designating the device memory to be read or written.

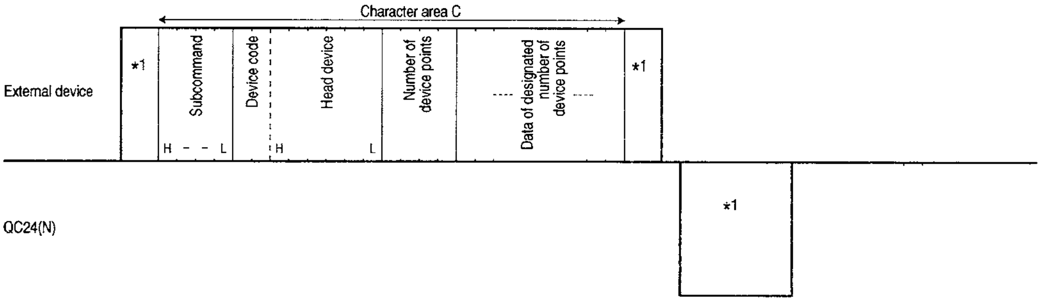
(a) ASCII mode character area data

The data list and contents of character area A, character area B, and character area C when the same command is used under the same conditions using the ASCII mode QnA frame and QnA extension frame format 1 to format 4 control procedures are the same.

(Example) Read



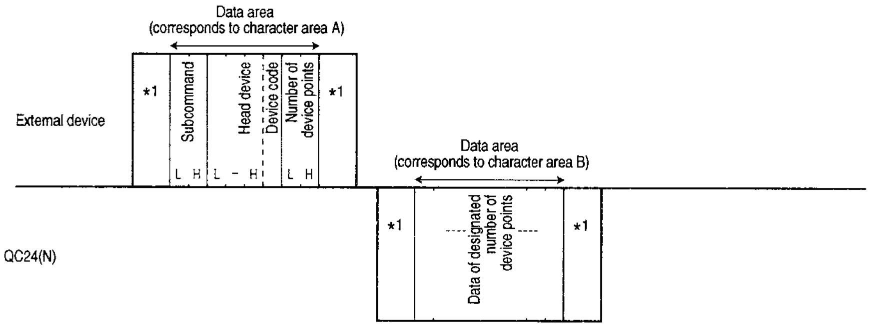
(Example) Write



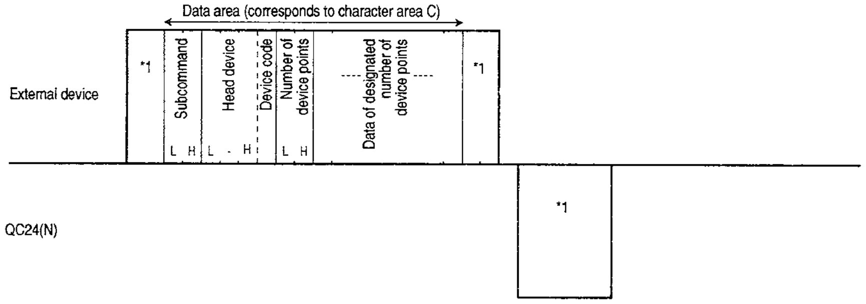
Sections 6.1.1, 6.1.2, and 6.1.4 describe the data list and contents of the *1 part.

(b) Binary mode data area data

(Example) Read



(Example) Write



Sections 6.1.3 and 6.1.4 describe the data list and contents of the *1 part.

(c) Contents of data common to character areas

① Subcommand

This data designates the read/write units, type of designated device, data read/write conditions, etc.

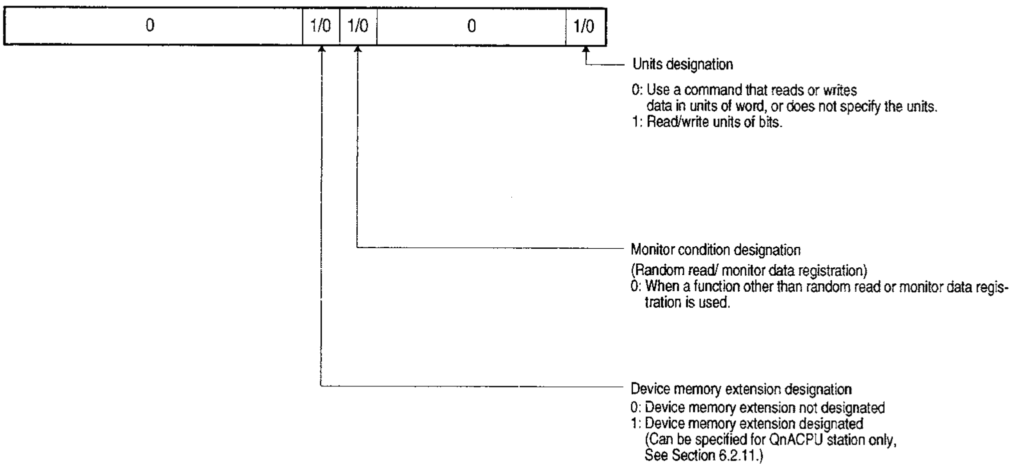
ⓐ Data communications in ASCII mode

The value 0000H (0), or the following value, is converted to a 4 digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

ⓑ Data communications in binary mode

The value 0000H, or the following 2-byte value, is transmitted.

ⓒ The subcommand designation contents are shown below.



ⓓ In the following cases, the subcommand is 0000H/0001H.

- When monitor condition not designated and device memory extension not designated.
- When a command that cannot select monitoring condition designation and device memory extension designation is used.

POINTS

The device memory of the following QC24(N) stations and other QnACPU can be accessed by setting [Device Memory Extension Designation] in subcommand bit 7. See Section 6.2.11. (The PLC CPU cannot be accessed over a data link.)

① QnACPU link direct device memory
② Special function module buffer register (buffer memory)

② Device code

This data identifies the device memory to be read or written.

ⓐ The device codes are shown in the table of $\boxed{3}$.

ⓑ Data communications in ASCII mode
The device code is converted to a 2-digit ASCII code and sequentially transmitted from the most significant digit.

(Example) Input relay
Input relay device code "X*" is sequentially transmitted from "X".

The second character "*" can be designated a blank (code: 20H).

ⓒ Data communications in binary mode
The 1-byte value shown in the table of $\boxed{3}$ is transmitted.

③ Head device (device)

This data designates the number of the device memory to be read or written.
When contiguous device memories are designated, the head number of that device memory range is designated.
The head device No. is designated by the expression method (decimal or hexadecimal) shown in the [Expression] column of the table shown in $\boxed{3}$ according to the objective device memory.

ⓐ Data communications in ASCII mode
The device number shown in the table is converted to a 6-digit ASCII code and sequentially transmitted from the most significant digit.
The "0" row of the most significant digit (indicates the "0" of the first two characters of the example "001234) can also be designated by a blank (code: 20H).

(Example) Internal relay M1234 and link relay B1234
Internal relay M1234 and link relay B1234 become "001234" or "␣␣1234" and are sequentially transmitted from the first "0" or "␣".

ⓑ Data communications in binary mode
The 3-byte value shown in the table is sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) Internal relay M1234 and link relay B1234
Internal relay M1234 becomes 0004D2H and is transmitted in D2H, 04H, 00H order.
Link relay B1234 becomes 001234H and is transmitted in 34H, 12H, 00H order.

④ Number of device points

This data designates the number of points to be read or written by execution of each command. It is designated within the number of points processed per communication shown in the table of $\boxed{1}$.

ⓐ Data communications in ASCII mode
The number of processing points is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Examples)
5 points.....Becomes “0005” and is sequentially transmitted from the first “0”.
20 points...Becomes “0014” and is sequentially transmitted from the first “0”.

ⓑ Data communications in binary mode
A 2-byte value representing the number of processing points is sequentially transmitted from the Low byte (L: bits 0 to 7).

(Examples)
5 points Becomes 0005H and is transmitted in 05H, 00H order.
20 points Becomes 0014 and is transmitted in 14H, 00H order.

⑤ Data of designated number of device points

Shows the contents of the data written to the designated device memory, or the contents of the data read from the designated device memory. The data list depends on the processing units (words/bytes).
See Section 6.1.5 for the data contents and data list (transmission order).

⑥ Number of bit access points

This data designates the number of points to be accessed in units of bits. It is designated within the number of points processed per communication given in Section 6.2.1 $\boxed{1}$.

ⓐ Data communications in ASCII mode

The number of points is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant.

(Example)
5 points....... Converted to “05” and sequentially transmitted from the “0”.
20 points..... Converted to “14” and sequentially transmitted from the “1”.

ⓑ Data communications in binary mode
A 1-byte value representing the number of points is transmitted.

(Example)
5 points....... 05H is transmitted.
20 points..... 14H is transmitted.

⑦ Set/reset

This data designates the data to be written to a bit device. It is designated by the value shown below.

Mode	Write data		Notes
	ON	OFF	
ASCII mode	“01”	“00”	Two characters are sequentially transmitted from the “0”.
Binary mode	01H	00H	The 1-byte value shown at the left is transmitted.

3 Device range

Indicates the device and device numbers of the PLC CPU that can be accessed using the QnA (extension) frame.
It designates the device and device number range at the module to be read or written.

(a) In the case of QnACPU

Table 6.1 Accessible Devices Table (QnACPU) (*1)

Class	Device		Device type		Device code		Device No. range (Default allocation)	Expression		Notes
			Bit	Word	ASCII mode	Binary mode		Decimal	Hexa-decimal	
Internal System	Function input		○		—	—	000000 to 00000F		○	Cannot be accessed
	Function output		○		—	—	000000 to 00000F		○	
	Function register			○	—	—	000000 to 000004	○		
	Special relay		○		SM	91H	000000 to 002047	○		—
	Special register			○	SD	A9H	000000 to 002047	○		
Internal User	Input relay		○		X*	9CH	000000 to 001FFF		○	Total within 28.75K words [1 device: Max. 32k points] When allocation is changed, up to the maximum device number after modification can be accessed. Local device can not be accessed.
	Output relay *2		○		Y*	9DH	000000 to 001FFF		○	
	Internal relay *2		○		M*	90H	000000 to 008191	○		
	Latch relay		○		L*	92H	000000 to 008191	○		
	Annunciator		○		F*	93H	000000 to 002047	○		
	Edge relay		○		V*	94H	000000 to 002047	○		
	Link relay		○		B*	A0H	000000 to 001FFF		○	
	Data register			○	D*	A8H	000000 to 012287	○		
	Link register			○	W*	B4H	000000 to 001FFF		○	
	Timer *3	Contact	○		TS	C1H	000000 to 002047	○		
		Coil	○		TC	C0H		○		
		Current value		○	TN	C2H		○		
	Integrating timer *3	Contact	○		SS	C7H		○		
		Coil	○		SC	C6H		○		
		Current value		○	SN	C8H		○		
	Counter *3	Contact	○		CS	C4H	000000 to 001023	○		
		Coil	○		CC	C3H		○		
		Current value		○	CN	C5H		○		
	Special link relay		○		SB	A1H	000000 to 0007FF		○	
	Special link register			○	SW	B5H	000000 to 0007FF		○	
	Step relay *2		○		S*	98H	000000 to 008191	○		
	Direct input		○		DX	A2H	000000 to 001FFF		○	Same as input relay and output relay (for direct access)
	Direct output		○		DY	A3H	000000 to 001FFF		○	
—	Index register			○	Z*	CCH	000000 to 000015	○		—
	File register *4 *5			○	R*	AFH	000000 to 032767	○		Normal access by block switching.
					ZR	B0H	000000 to 00FE7FF		○	Serial No. access

*1 Access is made to the device memory in the QnACPU.
The device ranges change depending on the version of the QnACPU.
For the device ranges, refer to the user's manual of the used CPU.

*2 For the QnACPU, the internal user's internal relay (M), latch relay (L) and step relay (S) are different devices.

*3 The following table indicates the QnACPU that allows the contacts and coils of the timer, integrating timer and counter to be designated for random read.
Note that the contacts and coils of the timer, integrating timer and counter in the QnACPU of function version A cannot be specified.
In monitor data registration/monitor, the contacts and coils of the timer, integrating timer and counter of the QnACPU cannot be specified.

Function	Command	QnACPU	
		Function version	
		A	B
Random read	0403	×	o
Monitor data registration/Monitor	0801/0802	×	o

o: Can be specified, ×: Cannot be specified.

The 4032H error is returned if any of the contacts and coils of the timer, integrating timer and counter is specified for the QnACPU that does not allows them to be designated.

*4 When making access from the external device to the file register of the PLC CPU, designate the following device code according to the file register configuration of the PLC CPU before making access. However, the program-by-program file register cannot be accessed from the external device.

① When the file register is configured by multiple blocks

- Designate the serial No. access device code “ZR” in the ASCII mode, or “B0H” in the binary mode.

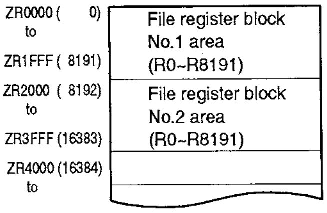
② When the file register is configured by block 0 only

- Designate either the serial No. access or normal access device code “ZR” or “R*” in the ASCII mode, or “B0H” or “AFH” in the binary mode.
- By designating the normal access code “R*” or “AFH”, the device No. can be specified in decimal.
- For access with the serial No. access code, designate the device No. in hexadecimal.

Refer to the following manuals for the concepts of the file register device Nos. for serial No. access and normal access.
QnACPU .... QnACPU Programming Manual (Fundamentals)
Other than QnACPU ..... AnACPU/AnUCPU Programming Manual (Dedicated Instructions)

Note

Example of serial No. access device Nos. (in the case of other than QnACPU)



The serial No. access device Nos. are automatically assigned in ascending order to the devices in the existent block No. 1 to block No. n.

*5 Write of data to the file register set to the EEPROM of the QnACPU can be performed only when the following restrictions have all been cleared.
When all the following restrictions cannot be cleared, an abnormal termination message is returned at the time of data write to the file register.

(Restrictions on write of data to the file register of the EEPROM)

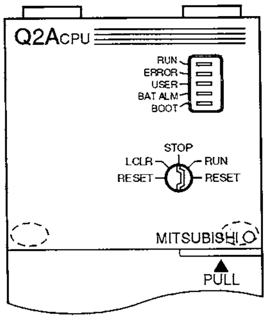
- Write can be performed using the batch write function (command: 1401) only.
- Write can be performed when the operating status of the target QnACPU is during STOP/during PAUSE.
- Write can be performed to the QnACPUs whose year and month of manufacture is January, 1999 or later and to the following QnACPUs.

QnACPU type	Year and month of manufacture	Software version
Q2ACPU (-S1), Q3ACPU, Q4ACPU	September to December, 1998	Version L or later
Q4ARCPU		Version S or later
Q2ASCPU (-S1), Q2ASHCPU (-S1)		Version T or later

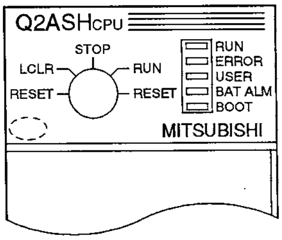
For the other QnACPUs, refer to the manual of the target QnACPU.

* The year and month of manufacture of the module (year (lower 2 digits), month (2 digits)) can be confirmed in the "DATE field of the rating plate" on the module side face.
The software version of the module can be confirmed in the seal on the module front (in either of the positions enclosed by dotted line shown below).

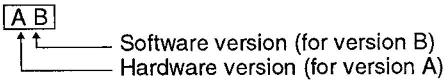
(In the case of Q2ACPU)



(In the case of Q2ASHCPU)



(Example)



(b) In the case of other than QnACPU

Table 6.2 Accessible Devices Table (Other than QnACPU) (*6)

Device		Device type		Device code		Device No. range	Expression		Notes
		Bit	Word	ASCII mode	Binary mode		Decimal	Hexa decimal	
Input X		○		X*	9CH	000000 to 001FFF		○	Extension designation cannot be done. To make access, designate the device and device range existing in the access destination.
Output Y		○		Y*	9DH	000000 to 001FFF		○	
Internal relay M		○		M*	90H	000000 to 008191	○		
Latch relay L		○		L*	92H	000000 to 008191	○		
Step relay S		○		S*	98H	000000 to 008191	○		
Link relay B		○		B*	A0H	000000 to 001FFF		○	
Annunciator F		○		F*	93H	000000 to 002047	○		
Special relay M		○		M*	90H	009000 to 009255	○		
Timer T	Contact	○		TS	C1H	000000 to 002047	○		
	Coil	○		TC	C0H	000000 to 002047	○		
	Current value		○	TN	C2H	000000 to 002047	○		
Counter C	Contact	○		CS	C4H	000000 to 001023	○		
	Coil	○		CC	C3H	000000 to 001023	○		
	Current value		○	CN	C5H	000000 to 001023	○		
Data register D			○	D*	A8H	000000 to 008191	○		
Link register W			○	W*	B4H	000000 to 001FFF		○	
File register *7 R			○	R*	AFH	000000 to 008191	○		Normal access by block switching
				ZR	B0H	000000 to 07FFFF		○	Serial No. access
Special register D			○	D*	A8H	009000 to 009255	○		—

*6 Access is made to the device memory in the designated CPU.

Note the following when making access to the PLC CPU other than the QnACPU.

(1) Make access within the device No. range that can be used by the access target PLC CPU.

(2) When access is made in word unit to the PLC CPU except the QnACPU at the station connected to the external device and the QnACPU via MELSECNET/10, the bit device No. must be a multiple of 16 (0, 16 ... in decimal).
The device No. of special relay M9000 or later can also be designated as (9000 + multiple of 16).

(3) M, L and S are designated in range. However, the same processing is performed if the number range of M is designated by L or S or if that of another device is designated the other way.

(4) The special relay (M9000 to M9255) and special register (D9000 to D9255) are divided into those for read only, write only and system.
If write is performed to those outside the write enabled range, a PLC CPU error may occur.
For details of the special relay and special register, refer to the ACPU Programming Manual.

*7 Refer to (a) *4.

6.2.2 Batch read in bit units (command: 0401)

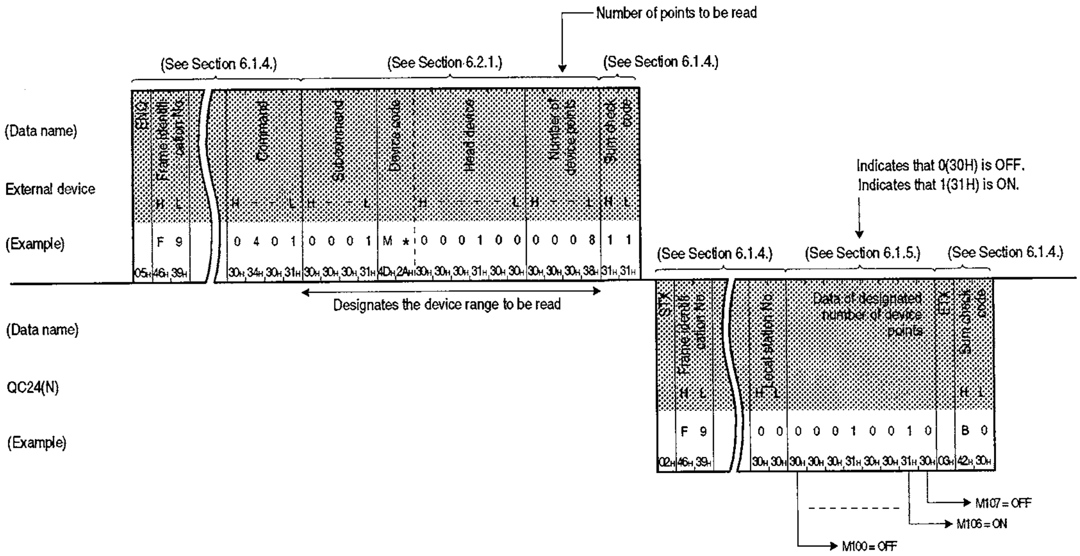
The following uses examples to described the bit device memory batch read control procedure.

[Control Procedure]

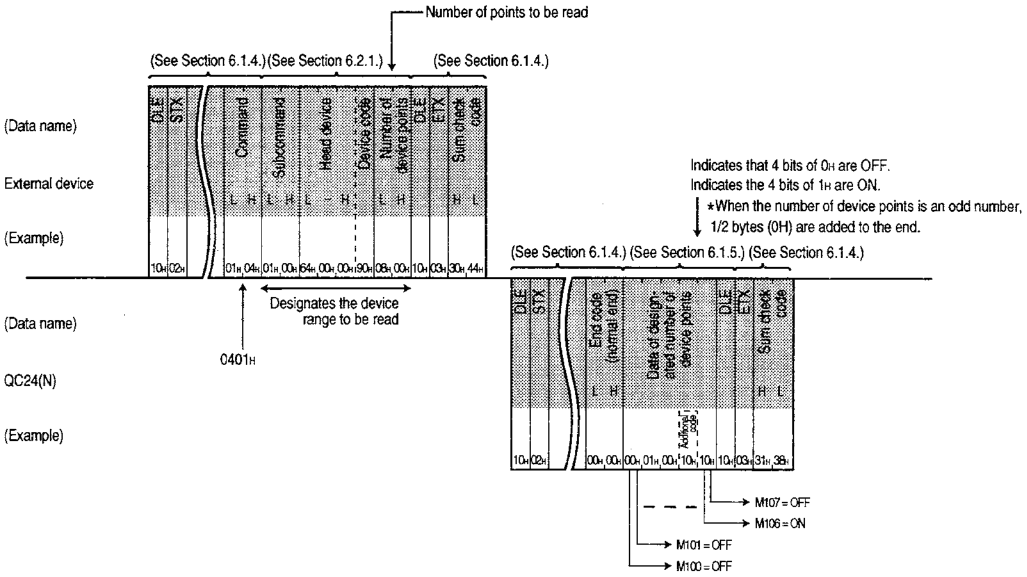
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to read the eight points of internal relays M100 to 107



2 When using binary mode format 5 to read the eight points from internal relays M100 to M107



POINTS

Designate the number of device points within the following range:

① When accessing an external device connection QnACPU or a QnACPU over a MELSECNET/ 10
- Number of device points ..... 1 ≤ number of device points ≤ 3952
- Access range .... (Head device No. + number of device points − 1) ≤ max. device No.

② When accessing a PLC CPU other than ① above
- Number of device points ..... 1 ≤ number of device points ≤ 256
- Access range .... (Head device No. + number of device points − 1) ≤ max. device No.

6.2.3 Batch read in word units (command: 0401)

This section uses examples to describe the bit device memory (16bit units) and word device memory (word units) batch read control procedure.

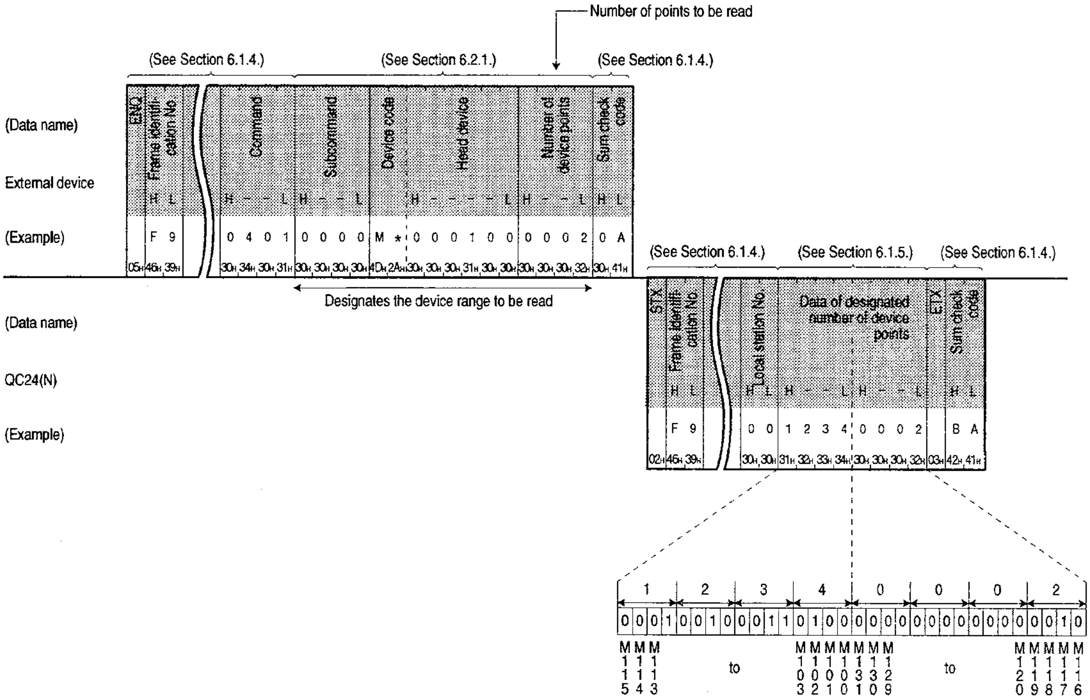
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

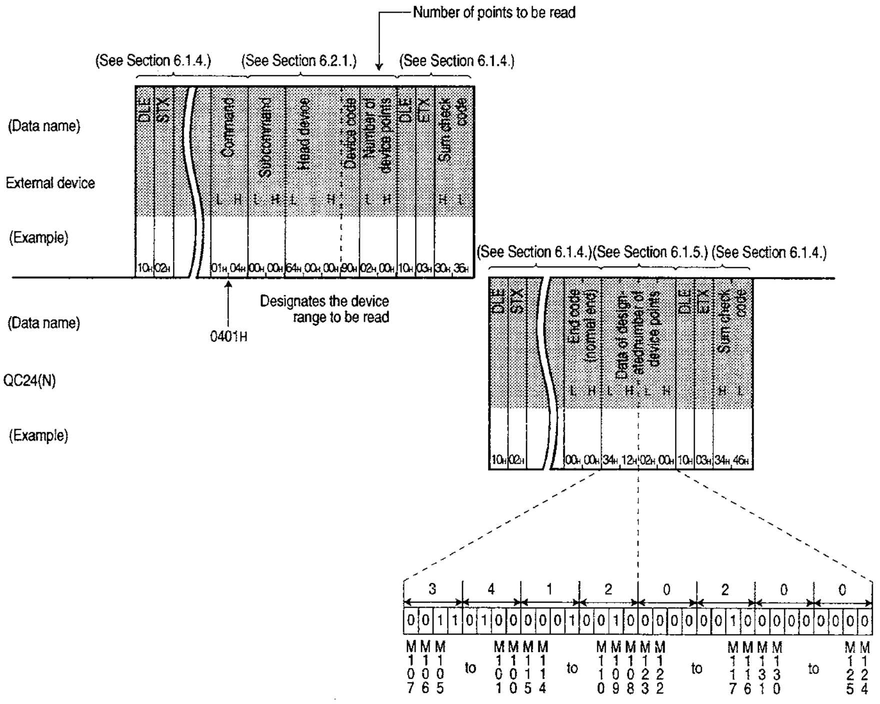
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 Reading bit device memory

(a) Using ASCII mode format 1 to read the two points (32 bits) from internal relays M100 to M131



(b) Using binary mode format 5 to read the two points (32 bits) from internal relay M100 to M131



POINTS

(1) Designate the number of device points within the following range.
For bit devices, 1 point is 16 bits.

① When accessing an external device connection QnACPU or an QnACPU over a MELSECNET/10

- Number of device points ..... 1 ≤number of device points ≤ 480 ····· (480 words = 7680 bits)
- Access range .... (Head device No. + number of device points × 16 – 1) ≤ max. device No.

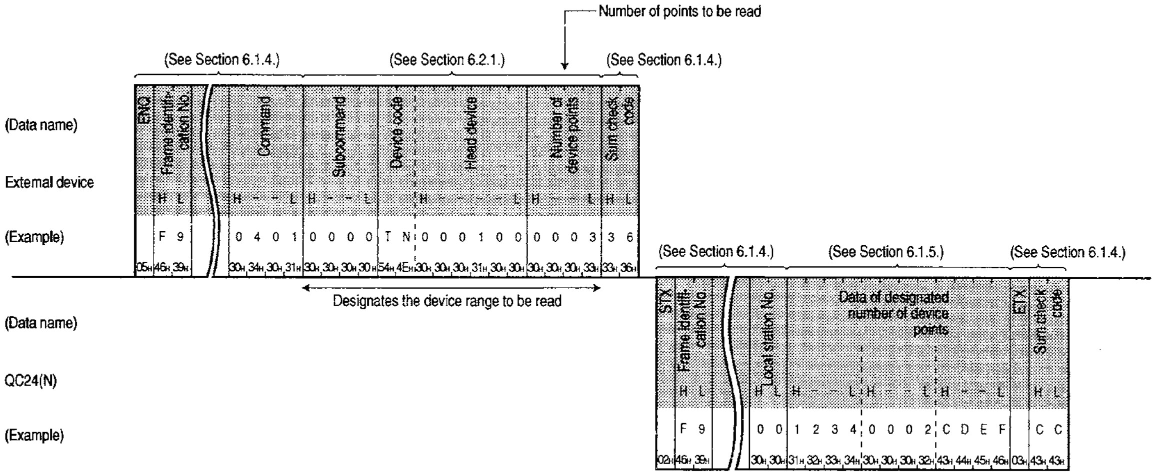
② When accessing a PLC CPU other than ① above

- Number of device points ..... 1 ≤ number of device points ≤ 32...(32 words = 512 bits)
- Access range .... (Head device No. + number of device points × 16 – 1) ≤ max. device No.

(2) When accessing the bit device of a PLC CPU other than ① above, always make the head device No. a multiple of 16 (for decimal, 0, 16....).

2 When reading a word device memory

(a) When using ASCII mode format 1 to read the current value of the three points from timers T100 to T102

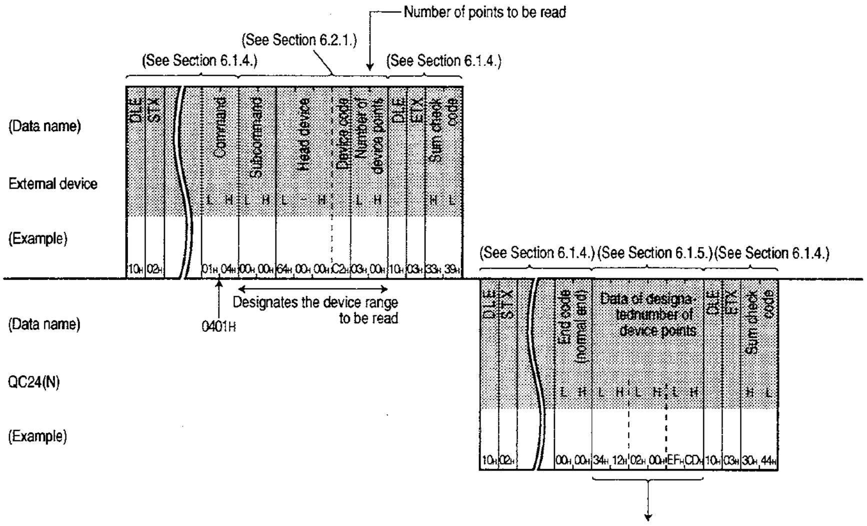


Indicates that the T100 current value 1234H (hexadecimal) is 4660 in decimal.

Indicates that the T101 current value 0002H (hexadecimal) is 2 in decimal.

Indicates that the T102 current value CDEFH (hexadecimal) is -12817 in decimal.

(b) When using binary mode format 5 to read the current value of the three points from timers T100 to T102



Indicates that the T100 current value 1234H (hexadecimal) is 4660 in decimal.

Indicates that the T101 current value 0002H (hexadecimal) is 2 in decimal.

Indicates that the T102 current value CDEFH (hexadecimal) is -12817 in decimal.

POINTS

Designate the number of points within the following range.

① When accessing an external device connection QnACPU or a QnACPU over a MELSECNET/10
- Number of device points ..... 1 ≤ number of device points ≤ 480
- Access range .... (Head device No. + number of device points − 1) ≤ max. device No.

② When accessing a PLC CPU other than ① above
- Number of device points ..... 1 ≤ number of device points ≤ 64
- Access range .... (Head device No. + number of device points − 1) ≤ max. device No.

6.2.4 Batch write in bit units (command: 1401)

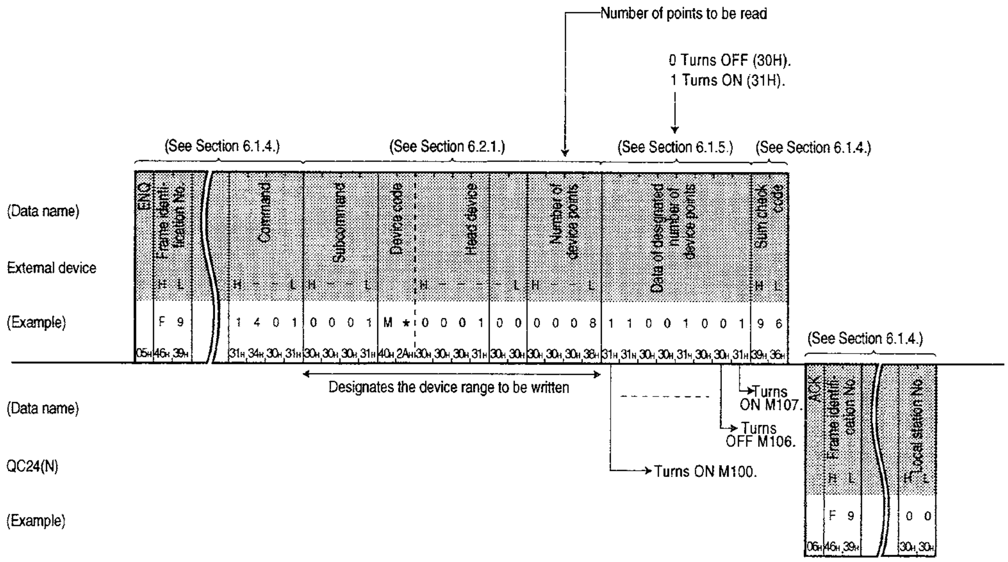
This section uses examples to describe the bit device memory batch write control procedure.

[Control Procedure]

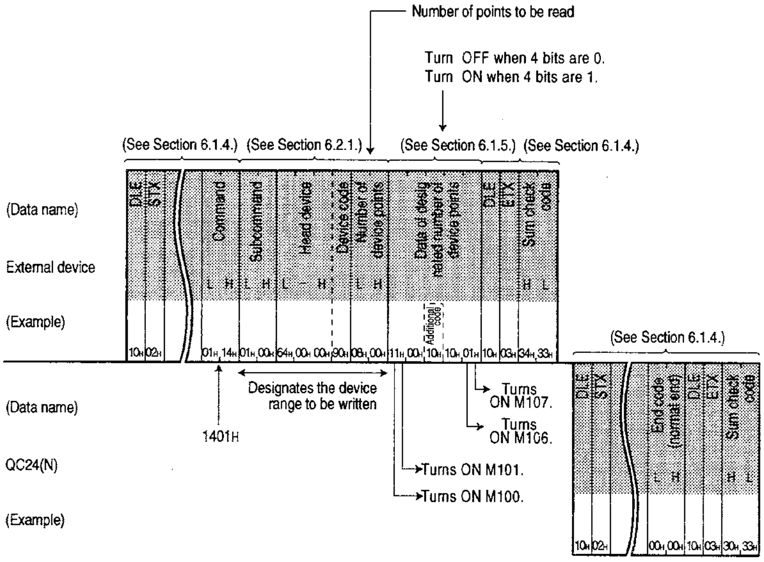
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to write eight points to internal relays M100 to M107



2 When using binary mode format 5 to write eight points to internal relays M100 to M107



POINTS

(1) Designate the number of device points within the following range.

① When accessing an external device connection station QnACPU, or a QnACPU over a MELSECNET/10

- Number of device points ..... 1 ≤ number of device points ≤ 3952
- Access range .... (Head device No. + number of device points – 1) ≤ max. device No.

② When accessing a PLC CPU other than ① above

- Number of device points ..... 1 ≤ number of device points ≤ 160
- Access range .... (Head device No. + number of device points – 1) ≤ max. device No.

(2) When writing to a QnACPU, if system-protect is applied to the QnACPU (system-protect switch SW05: ON), the QC24(N) will recognize an error and return a NAK message to the external device.

6.2.5 Batch write in word units (command: 1401)

This section uses examples to describe the bit device memory (16 bit units) and word device memory (word units) batch write control procedures.

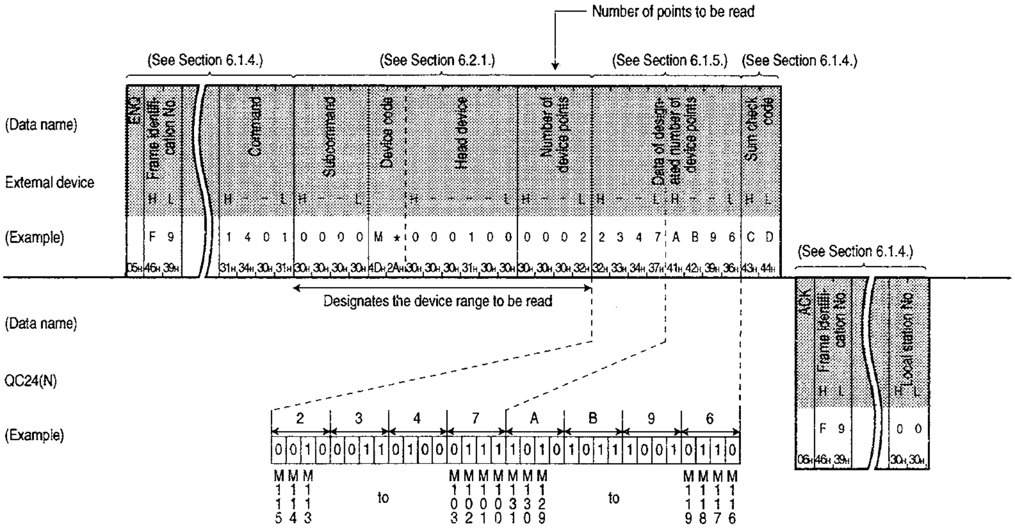
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

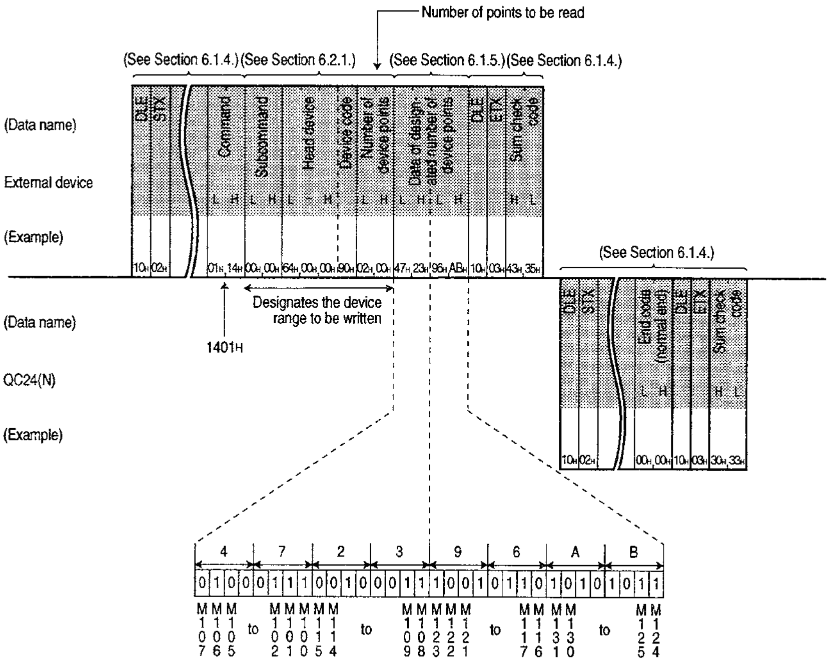
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When writing to bit device memory

(a) When using ASCII mode format 1 to write two points (32 bits) to internal relays M100 to M131



(b) When using binary mode format 5 to write two points (32 bits) to internal relays M100 to M131



POINTS

(1) Designate the number of device points within the following range.
For bit devices, 1 point is 16 bits.
① When accessing an external device connection station QnACPU or a QnACPU over a MELSECNET/10
- Number of device points ..... 1 ≤ number of device points ≤ 480 (480 words = 7680 bits)
- Access range .... (Head device No. + number of device points x 16 – 1) ≤ max. device No.

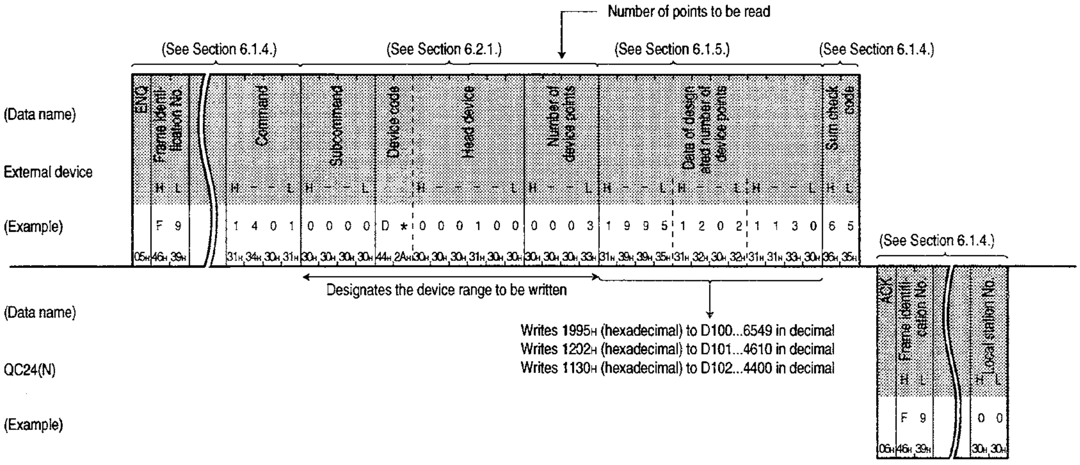
② When accessing a PLC CPU other than ① above
- Number of device points ..... 1 ≤ number of device points ≤ 10....(10 words = 160 bits)
- Access range .... (Head device No. + number of device points x 16 – 1) ≤ max. device No.

(2) When accessing the bit device of a PLC CPU other than ① above, always make the head device No. a multiple of 16 (For decimal, 0, 16...).

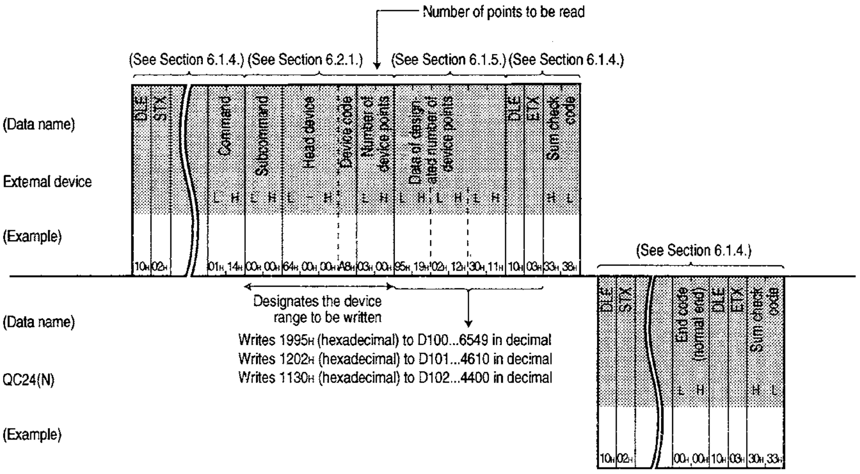
(3) When writing to a QnACPU, if system-protect is applied to the QnACPU (system-protect switch SW05: ON), the QC24(N) will recognize an error and return a NAK message to the external device.

2 When writing to word device memory

(a) When using ASCII mode format 1 to write three points to D100 to D102



(b) When using binary mode format 5 to write three points to D100 to D102



POINTS

(1) Designate the number of device points within the following range.

① When accessing an external device connection QnACPU or a QnACPU over a MELSECNET/10

- Number of device points ..... 1 ≤ number of device points ≤ 480
- Access range .... (Head device No. + number of device points – 1) ≤ max. device No.

② When accessing a PLC CPU other than ① above

- Number of device points ..... 1 ≤ number of device points ≤ 64
- Access range .... (Head device No. + number of device points – 1) ≤ max. device No.

(2) When writing to a QnACPU, if system-protect is applied to the QnACPU (system-protect switch SW05: ON), the QC24(N) will recognize and error and return a NAK message to the external device.

6.2.6 Random read in word units (command: 0403)

This section uses examples to describe the procedure that reads data while designating device memory (16/32 bit units) and word device memory (1/2 word units) at random.

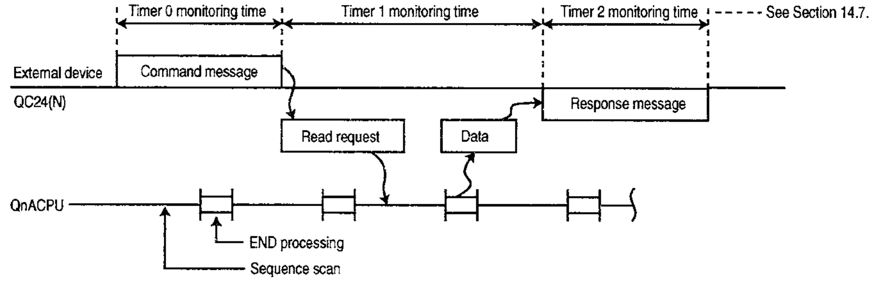
In random read in word units, the following data read timing conditions (hereafter abbreviated "monitoring conditions") can be designated. (Combined designation is also possible.)

- Read the device memory when the designated device was turned ON or OFF during PLC CPU END processing.
- Read the device memory when the value of the designated device memory reached the monitor conditions value during PLC CPU END processing. (A mask value can also be designated as the monitoring condition.)
- Read the device memory when the designated step of the designated file was executed during PLC CPU END processing. (MELSEP3 block No. and step No. can also be designated.)

The following shows the device memory read timing by device condition designation.

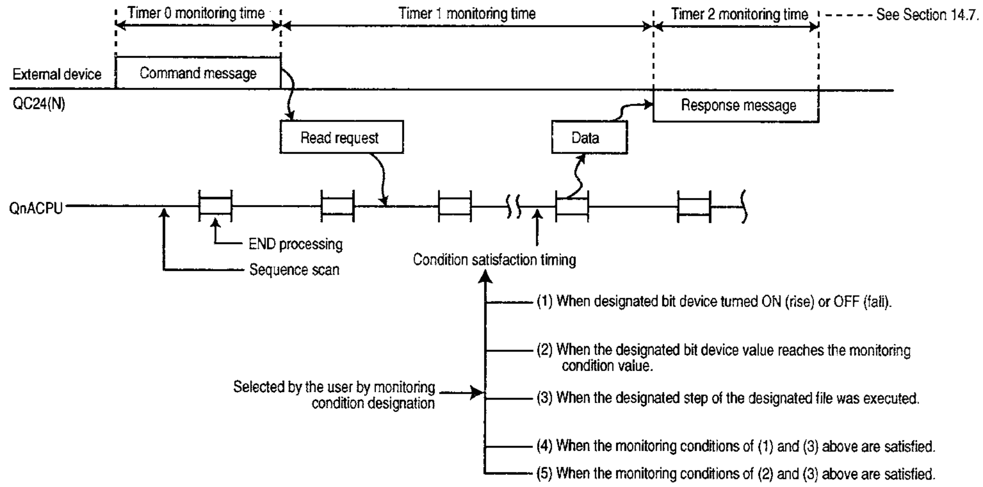
When monitor condition not designated

The device memory is read during END processing when the QC24(N) issued a read request to the PLC CPU.



When monitor condition designated

The device memory is read during END processing when the monitor condition above designated by the user is satisfied after the QC24(N) issued a read request to the PLC CPU.



POINT

A special function module and GP function peripheral device cannot conditionally monitor the same QnACPU device memory at the same time.

When the QC24(N) receives the command message shown below from an external device, if conditional monitoring of the same QnACPU is being performed simultaneously from a special function module and a GPP function peripheral device, the QC24(N) will send a NAK message to the external device. (When unconditional monitoring is being performed, the QC24(N) can perform conditional/unconditional monitoring.)

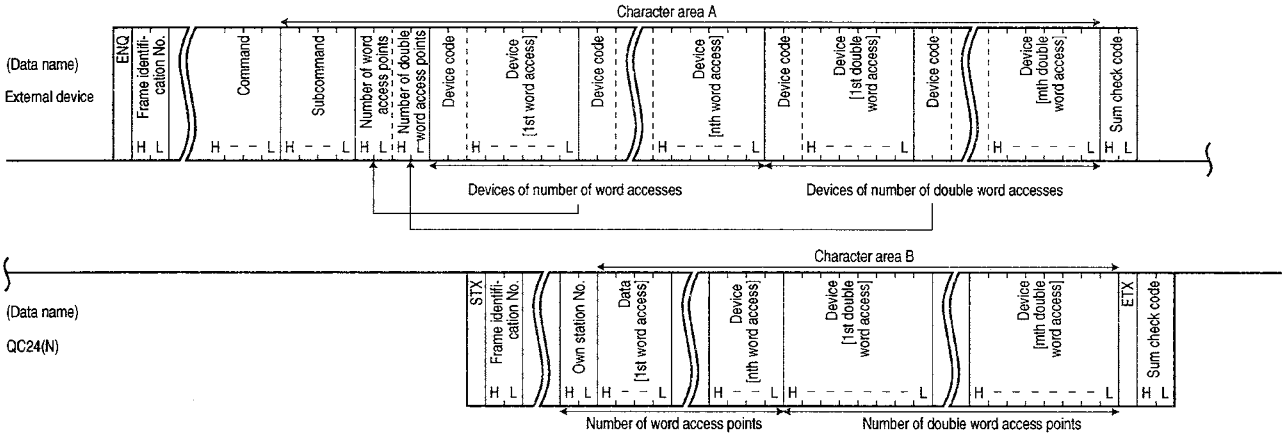
Command	Function	Function description
0403	Word units random read function	This section.
0802	Registered device memory monitor function	Section 6.2.9 4

1 Character area data list and contents during random read

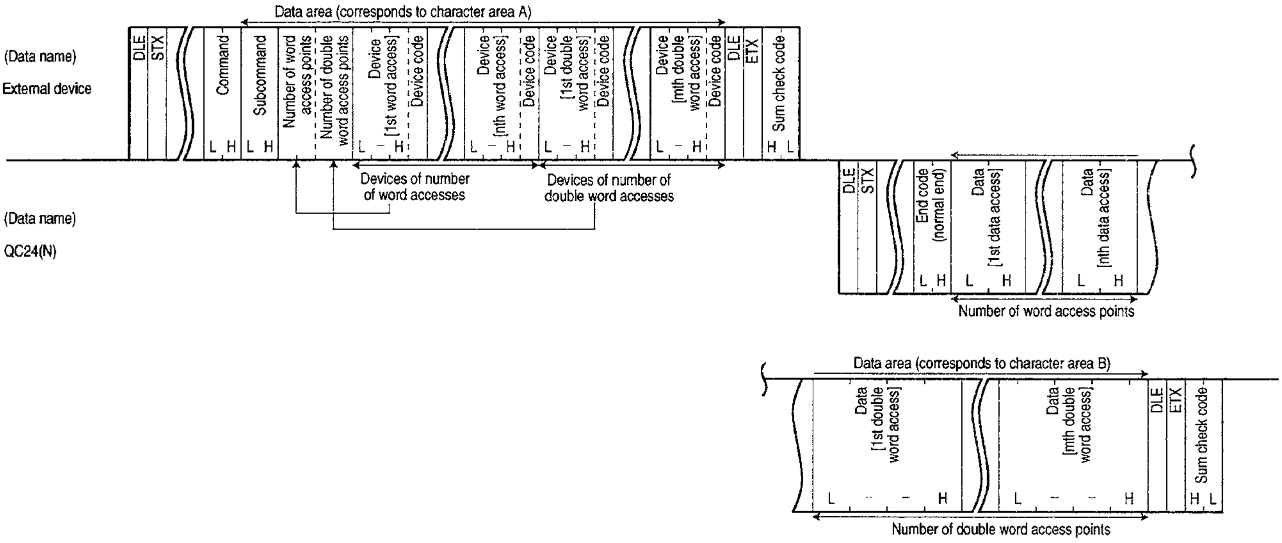
The following describes the character area data list and contents during random read.
The list and part of the character area different when another command is used.

(a) Character area data list when monitor condition not designated

① ASCII mode QnA (extension) frame data list (format 1)

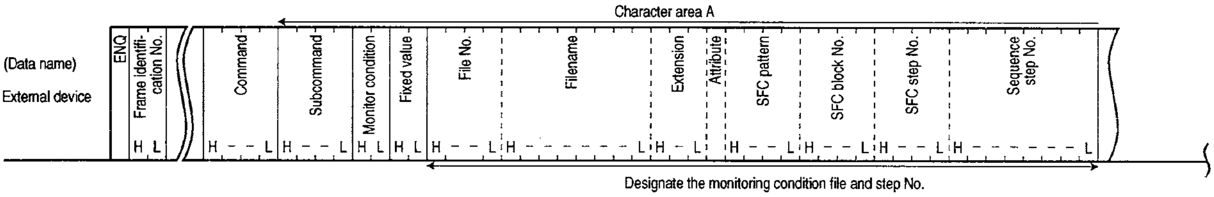


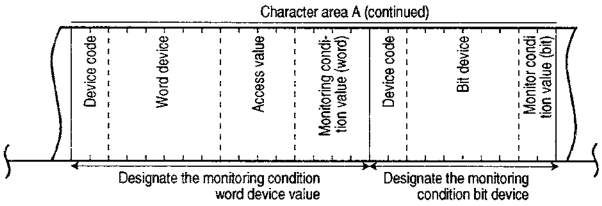
② Binary mode QnA extension frame data list

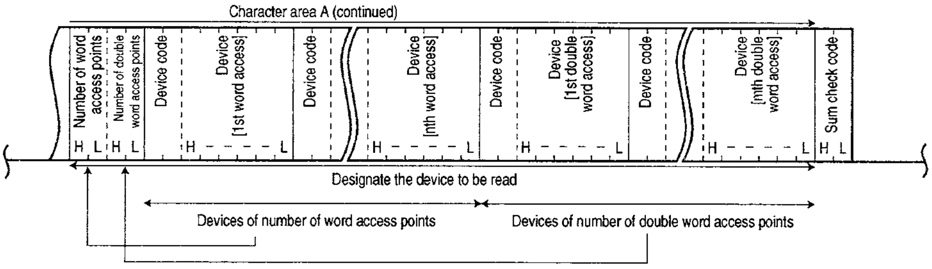


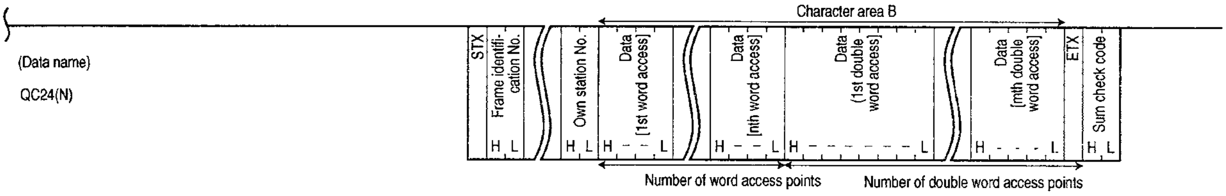
(b) Character area data list when monitoring condition designated

① ASCII mode QnA (extension) frame data list

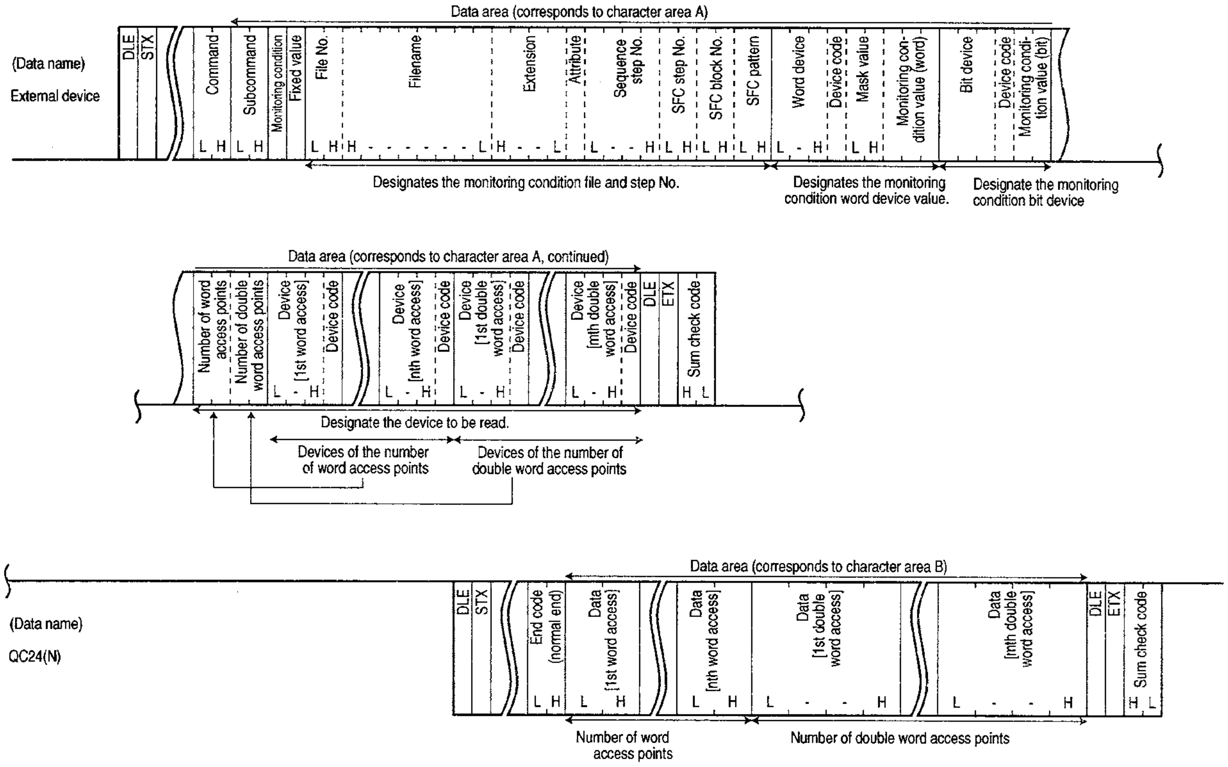








② Binary mode QnA extension frame data list



(c) Contents of character areas

The contents of the character areas are the same as the contents when another command is used, except for the following data:

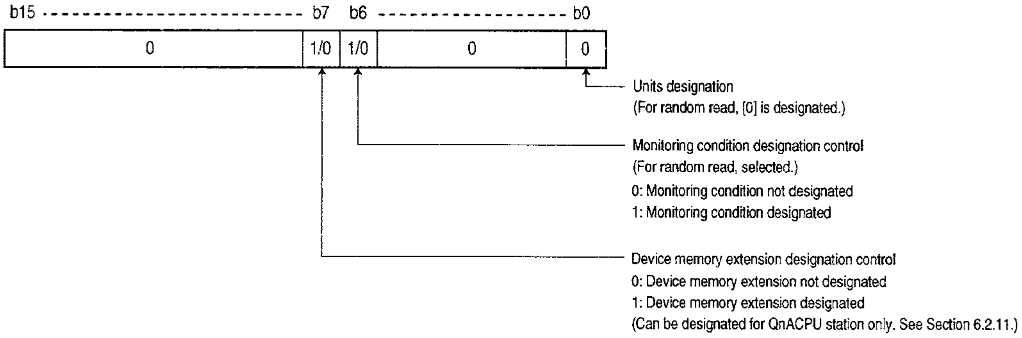
① Subcommand

This data designates the read/write units, kind of device to be designated, data read conditions (timing), etc.

ⓐ Data communications in ASCII mode
The value 0000H (0), or the value shown below, is converted to a4-digit (hexadecimal) ASCII code and transmitted from the most significant digit.

ⓑ Data communications in binary mode
The value 0000H, or the 2-bytes value shown below, is transmitted.

ⓒ The subcommand designation contents are:



ⓓ When monitoring condition not designated and device memory extension designation are selected, the subcommand is [0000H].

Note

The data that must be designated after the character area depending on whether or not the subcommand monitoring condition is designated is shown below.

Condition designation Data name	When monitoring condition not designated	When monitoring condition designated		
	—	When file and step No. designated	When word device value designated	When bit device designated
Number of word access points	●			
Number of double word access points				
(Read device designation)	—	—	—	—
(Word read)				
Device code	●			
Device	(However, when the number of word access points is 0, designation is unnecessary.)			
(Double word read)	—	—	—	—
Device code	●			
Device	(However, when the number of double word access points is 0, designation is unnecessary.)			
Monitoring condition	×	●		
Fixed value				
File No. to Attribute	×	●	△	△
SFC pattern to SFC step No.	×	△	△	△
Sequence step No.	×	●	△	△
(Word device value designation)	—	—	—	—
Device code to Monitoring condition value (word)	×	△	●	△
(Bit device designation)	—	—	—	—
Device code to Monitoring condition value (bit)	×	△	△	●

●: Designation necessary △: Selective (When not designated, a fixed value is designated.) ×: Designation unnecessary

② Number of word access points and number of double word accesspoints

These data designate the number of points read in word units and the number of points read in double word units.

The total number of points of each is designated within the number of points processed per communications shown in Section 6.2.1 $\boxed{1}$.

ⓐ Data communications in ASCII mode

Each number of points is converted to a 2-digit (hexadecimal) ASCII code and transmitted from the most significant digit.

(Example) 5 points......Converted to "05" and transmitted from the"0".
20 points....Converted to "14" and transmitted from the "1".

ⓑ Data communications in binary mode

The 1-byte number indicating the number of points is transmitted.

(Example) 5 points......05H is transmitted.
20 points....14H is transmitted.

ⓒ When the number of access points is 0, the relevant device and device code do not have to be designated.

③ Monitoring condition

This data designates the data read condition. It can be designated for the QnACPU only.
The monitoring condition combinations that can be designated are shown below. (Three conditions cannot be designated at the same time.)

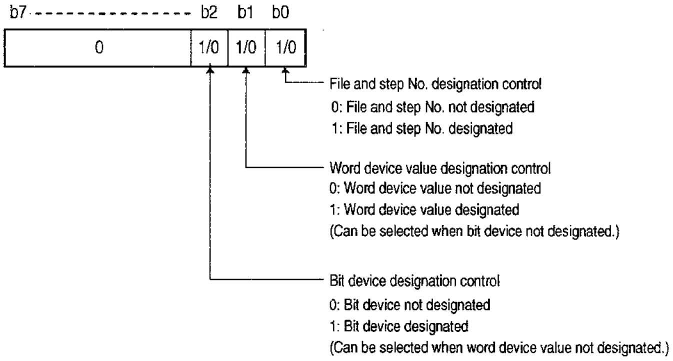
Combination / Monitoring condition	File and step No. designation	Word device value designation	Bit device designation
Single designation	○	○	○
Combined designation	○	○	
	○		○

○: Can be designated

ⓐ Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and transmitted from the most significant digit.

ⓑ Data communications in binary mode
The 1-byte value shown below is transmitted.

ⓒ The monitoring condition designation contents are shown below.



ⓓ When "monitoring condition designated" was selected by subcommand, the monitoring conditions are [01H] to [05H].
[00H] cannot be used.

ⓔ When "monitoring condition not designated" was selected by subcommand, the monitoring condition does not have to be designated.

④ Fixed value

ⓐ Data communications in ASCII mode
The value "0F" is transmitted from the most significant digit ("0").

ⓑ Data communications in binary mode
The 1-byte value [0FH] is transmitted.

ⓒ When "monitoring condition not designated" was selected by subcommand, "fixed value" does not have to be designated.

⑤ File No.

This data designates the registration No. when a file designated by the following filename and extension is written to the PLC CPU. One of the following can be designated.

File No.	Contents	Designation contents
00H	Filename not designated	Designated when "file and step No. not designated" was selected as the monitoring conditions.
0001H to 0100H	File No.	Designated when file No. is known.
FFFFH	File No. unknown	Designated when file No. retrieved by QC24(N). (Random read requests from QC24(N) to PLC CPU are delayed by one sequence scan, or longer.)

ⓐ Data communications in ASCII mode
The file No. shown above is converted to a 4-digit (hexadecimal) ASCII code and transmitted from the most significant digit.
(Example)
File No. 1FH....Converted to "001F" and sequentially transmitted from the first "0".

ⓑ Data communications in binary mode
The 2-byte value shown above is transmitted from the Low byte (L: bits 0 to 7).
(Example)

File No. 1FH....Becomes 001FH and is transmitted in1FH, 00H order.

ⓒ When "file and step No. not designated" are selected (02H, 04H) as the monitoring condition, the file No. becomes 0000H even if "monitor condition designated" is selected by subcommand.

ⓓ When "monitor condition not designated" is selected by subcommand, the file No. does not have to be designated.

ⓔ The file No. can be checked using the file search function described in Section 6.6.6.

⑥ Filename, extension, attribute

Data ⑨ Sequence No. objective file. This data designates the filename, extension, and attribute when the objective file was registered (written) to the PLC CPU.
The initial user file attribute is 20H (disk file). This attribute can be changed by the user. (See Section 6.6.5.)

ⓐ Data communications in ASCII mode
The filename, extension, and attribute used during registration are sequentially transmitted from the first character of each.
Blank (code: 20H) is transmitted as the attribute.
When the filename is less than 8 characters, blanks (code: 20H) are added.
(Example) When the filename during registration was "ABCD12""ABCD12__" is sequentially transmitted from the "A".

ⓑ Data communications in binary mode
The filename and extension use the character codes used during registration as binary values, and are sequentially transmitted from the first character.
The 1-byte value [20H] is transmitted as the attribute.
When the filename is less than 8 characters, 20H is added.
(Example) When the filename during registration was "ABCD12"
The filename becomes 41H, 42H, 43H, 44H, 31H, 32H, 20H, 20H and is sequentially transmitted from 41H.

ⓒ When "file and step No. not designated" was selected (02H, 20H used) as the monitoring condition, the filename and extension are replaced by a string of blanks or 20H codes.
The attribute is made a blank or 20H code.

ⓓ When "monitoring condition not designated" was selected by subcommand, the filename, extension, and attribute do not have to be designated.

ⓔ The attribute can be checked using the file search function described in Section 6.6.6.

⑦ SFC pattern

This is one of the data for making the execution time of the designated sequence No. of the MELSAP3 program (SFC) the timing that reads the data.

ⓐ When "monitoring condition designated" was selected by a subcommand and "file and step No. designated" was selected by ③ monitoring condition control, the data shown below designates the SFC pattern.
Other patterns can not be designated.

Mode	Write data		Notes
ASCII mode	When SFC designated	"0003"	4 characters are sequentially transmitted from the first character ("0").
	When SFC not designated	"0000"	
Binary mode	When SFC designated	0003H	Transmits the 2-byte value shown at the left from the Lowbyte (L: bits 0 to 7).
	When SFC not designated	0000H	

ⓑ When "monitoring condition designated" was selected by subcommand and "file and step No. not designated" was selected by monitoring condition control, the SFC pattern is "0000"/[0000H].

ⓒ When the SFC pattern is specified by "0003"/0003H, the designated device memory data is read during PLC CPU END processing when the sequence step No. designated by ⑨ of the block No. and step No. designated by ⑧ was executed.

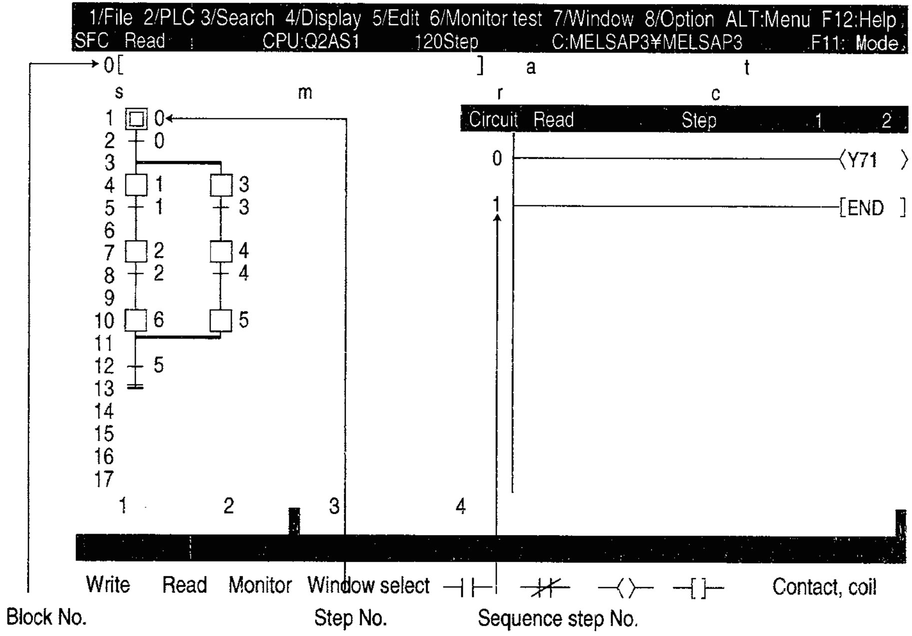
ⓓ When "monitoring condition not designated" was selected by subcommand, the SFC pattern does not have to be designated.

POINTS

(1) See the MELSAP3 programming manual and operating manual for a detailed description of the MELSAP3.

(2) When the relevant step (operation output) is displayed in the ZOOM state during MELSAP3 program editing, the operation SFCblock No. and SFC step No. designated using ⑧ and the sequence step No. designated using ⑨ correspond to the following display.

(Example)



⑧ SFC block No. and SFC step No.

These data designate the SFC block No. and SFC step No. that include the data read timing (at designated step execution) sequence step.
This data can be designated when "monitoring condition designated" was selected by subcommand, "file and step No. designated" was selected by monitoring condition control, and "SFC block designated" was selected by the SFC pattern designation.

ⓐ Data communications in ASCII mode
The following values are converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

- SFC block No .. 0000H to 013FH (0 to 319)
- SFC step No .... 0000H to 01FFH (0 to 511)

ⓑ The 2-byte values shown above are sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) 0005H....Transmitted in 05H, 00H order.

ⓒ In the following cases, the SFC block No. and SFC step No. become [000H].

- When "file and step No. not designated" was selected by monitoring condition control even when "monitoring condition designated" was selected by subcommand.
- When "SFC block No. not designated" was selected by SFC pattern.

ⓓ When "monitoring condition not designated" was selected by subcommand, the SFC block No. and SFC step No. do not have to be designated.

⑨ Sequence step No.

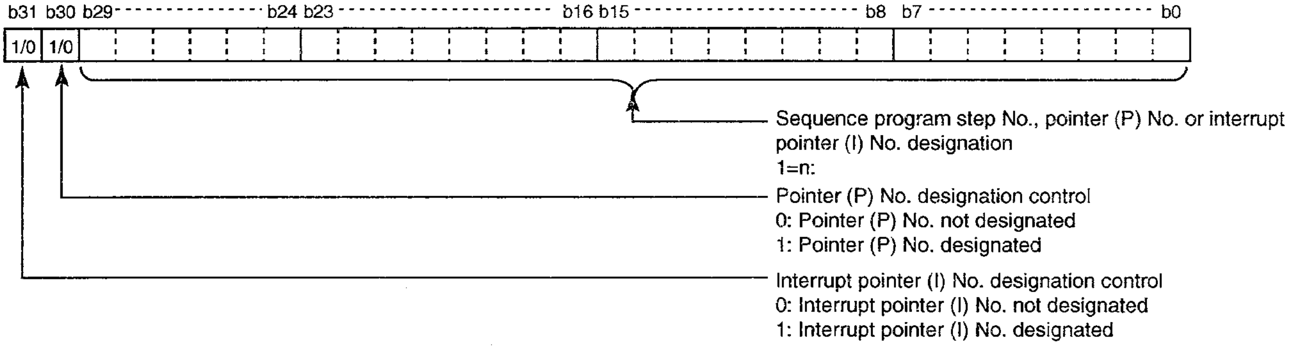
This data designates the step No. and pointer (P) No., or interrupt pointer (I) No., of the data read timing (when designated sequence step executed) sequence program. When "monitoring condition designated" was selected by subcommand and "designate file and step No." was selected by monitoring condition control, the sequence step No. can be designated.

ⓐ Data communications in ASCII mode
The value shown below within the range depending on the objective file is converted to an 8-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

ⓑ Data communications in binary mode
The 4-byte value below within the range depending on the objective file is sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) 00000005H....Sequentially transmitted from 05H.

ⓒ The sequence step No. designation contents are shown below.



(Example) When designated, sequence program No. 28 is 00000001H. When designated, interrupt pointer 128 is 80000001H.

ⓓ When "file No. and step No. not designated" was selected by monitoring condition control, even when "monitoring condition designated" was selected by subcommand, the sequence step No. is [00000000H].

ⓔ When "monitoring condition not designated" was selected by subcommand, the sequence step No. does not have to be designated.

⑩ Mask value and monitoring condition value (word)

These data designate the data read timing (when designated word device was the monitoring condition) word device value, etc.

- Mask value
  This data extracts the values of an arbitrary range of bits of the monitoring condition word device.
  (Operation is the same as that of the sequence program [WAND] instruction.)
- Monitoring condition value (word)
  This data designates the data read timing value (monitoring condition word device value and mask value logical operation (same as [WAND] instruction) result).

(Example) When the result of extraction of bits 0 to 14 of monitoring condition D0 was 3E8H (1000) and this was made the dataread timing, the following is designated:
Mask value : 7FFFH
Monitoring condition value (word) : 03E8H

When "monitoring condition designated" was selected by subcommand and "word device value designated" was selected by monitoring condition control, the mask value and monitoring condition value (word) can be designated.

ⓐ Data communications in ASCII mode
The mask value and monitoring condition value above are converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

ⓑ Data communications in binary mode
Two-byte values indicating the mask value and monitoring condition value above are sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) 0005H...Sequentially transmitted from 05H.

ⓒ When "monitoring condition designated" was selected by subcommand and "word device value not designated" was selected by monitoring condition, the mask value and monitoring condition value are replaced by blanks or [0000H].
In this case, word device and device code for designating the monitoring condition word device value designate an arbitrary word device memory and its device code.

ⓓ When "monitoring condition not designated" was selected by subcommand, the mask value and monitoring condition value do not have to be designated.
(Word device and device code for designating the monitoring condition word device value do not have to be designated either.)

⑪ Monitoring condition value (bit)

This data designates the data read timing conditions (rise, fall).
When "monitoring condition designated" was selected by subcommand and "bit device designated" was selected by monitoring condition, monitoring condition value (bit) can be designated.

ⓐ Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

ⓑ Data communications in binary mode
The 1-byte value shown below is transmitted.

ⓒ The monitoring condition value (bit) designation contents are shown below.

Designated value	Read timing
02H	During PLC CPU END processing when designated bit device raised
04H	During PLC CPU END processing when designated bit device dropped

ⓓ When "bit device not designated" was selected by monitor condition even through "monitoring condition designated" was selected by subcommand, the monitoring condition value is "00" or [00H].
In this case, the bit device and device code for designating the monitoring condition bit device designate an arbitrary bit device memory and its device code.

ⓔ When "monitoring condition not designated" was selected by subcommand, the monitoring condition value does not have to be designated.
(The bit device code for designating the monitoring condition bit device does not have to be designated either.)

2 Word units random read (when monitoring condition not designated)

The following uses examples to describes the control procedure that reads data by designating bit device memories (16 bit units) and word device memories (word units) at random, without designating a monitoring condition (read condition).

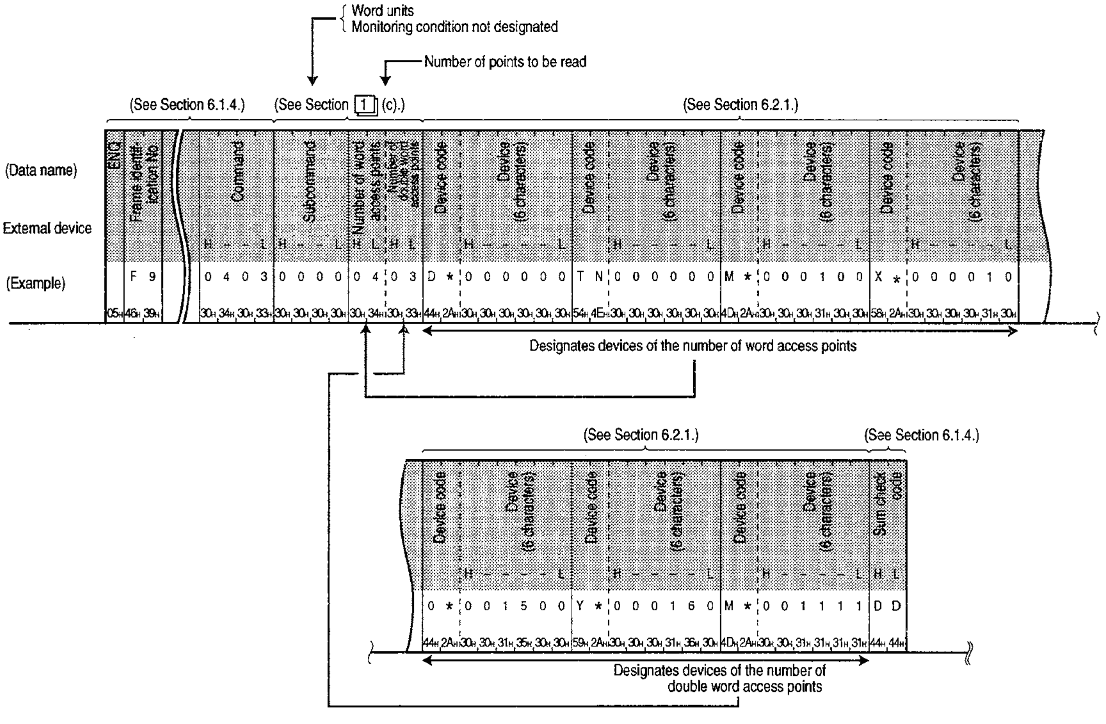
[Control Procedure]

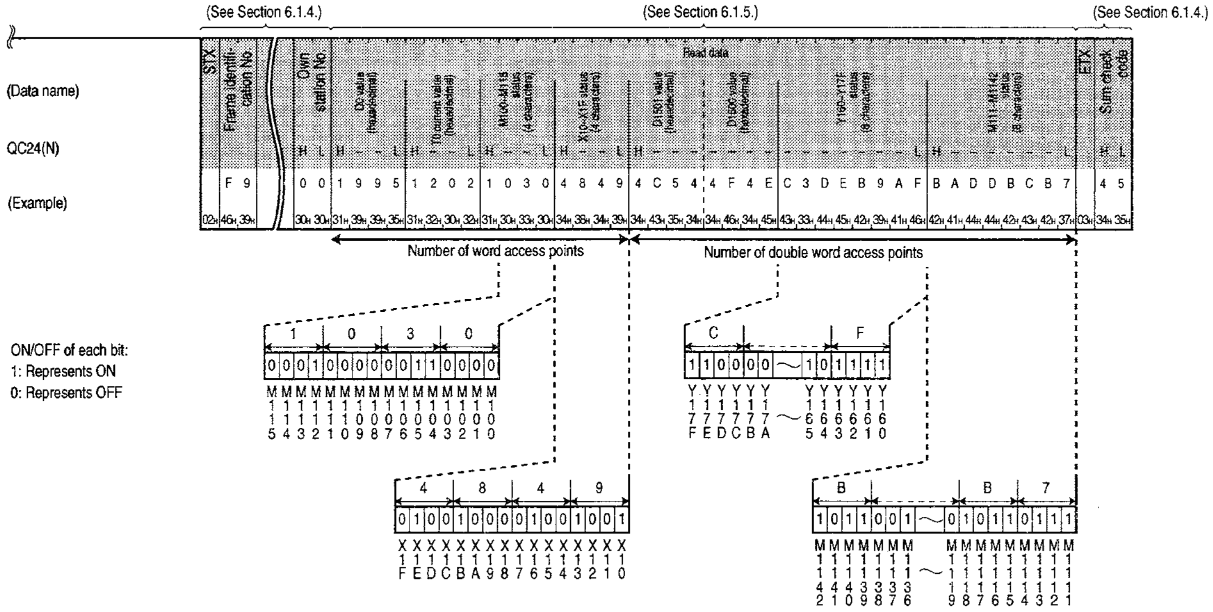
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to read the following device memories

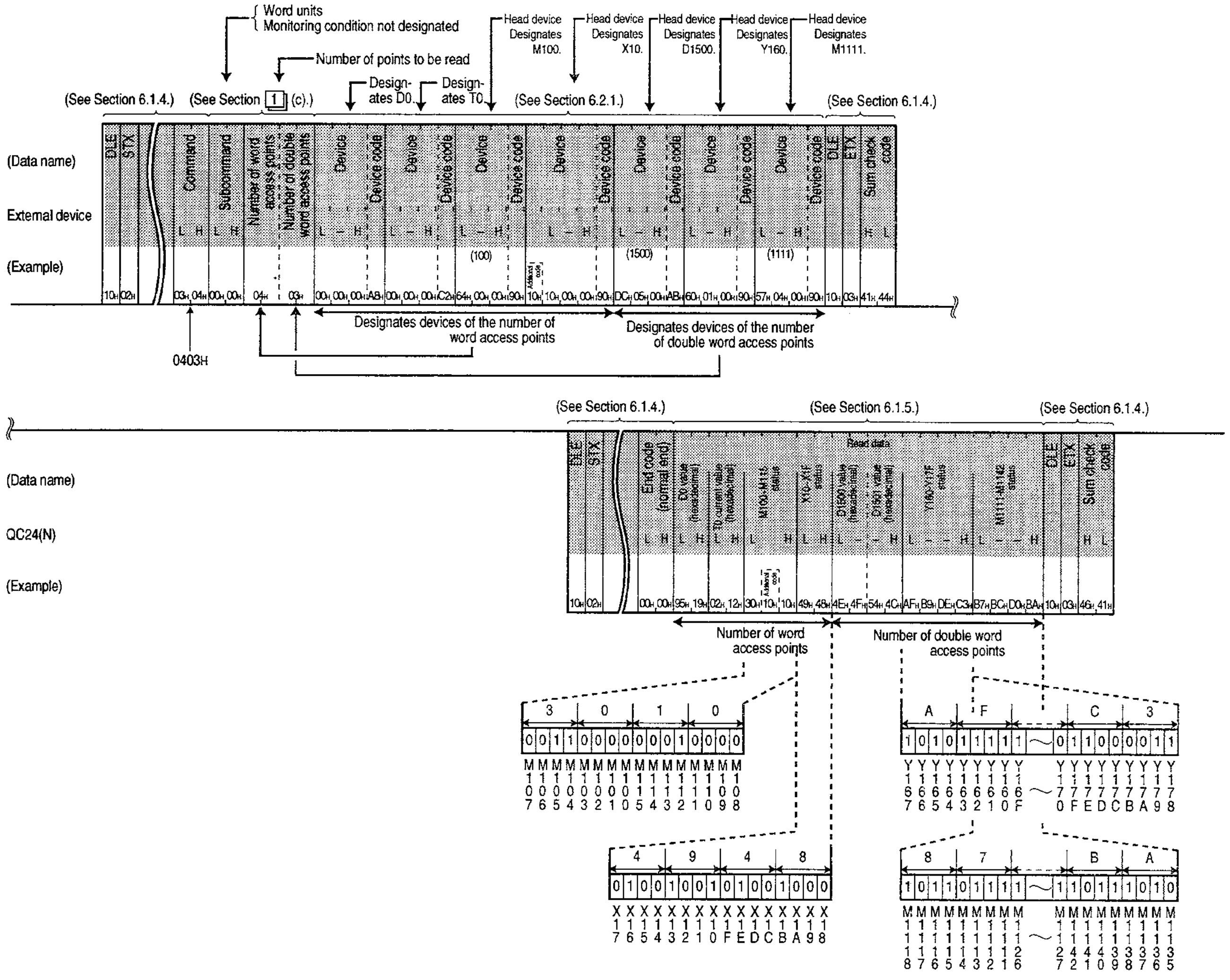
- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142





(b) When using binary mode format 5 to read the following devicememories

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



POINTS

(1) Designate the number of access points within the following range. (This also applies when a monitoring condition is designated.)
For bit device, one word access point is 16 bits and one double word access point is 32 bits.
For word device, one word access point is 1 word and one double word access point is 2 words.

① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10
- Number of access points ... 1 ≤ (number of word access points + number of double word access points) ≤ 96

② When accessing a PLC CPU other than ① above
- Number of access points .... 1 ≤ (number of word accesses) ≤10

(2) When accessing the bit device of a PLC CPU other than ① above, always make the device No. a multiple of 16 (for decimal, 0, 16...).

3 Word units random read (when monitoring condition designated)

The following uses examples to describe the control procedure that reads data by designating the monitoring condition (read condition) and designating bit device memories (16 bit units) and word device memories (word units) at random.

[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

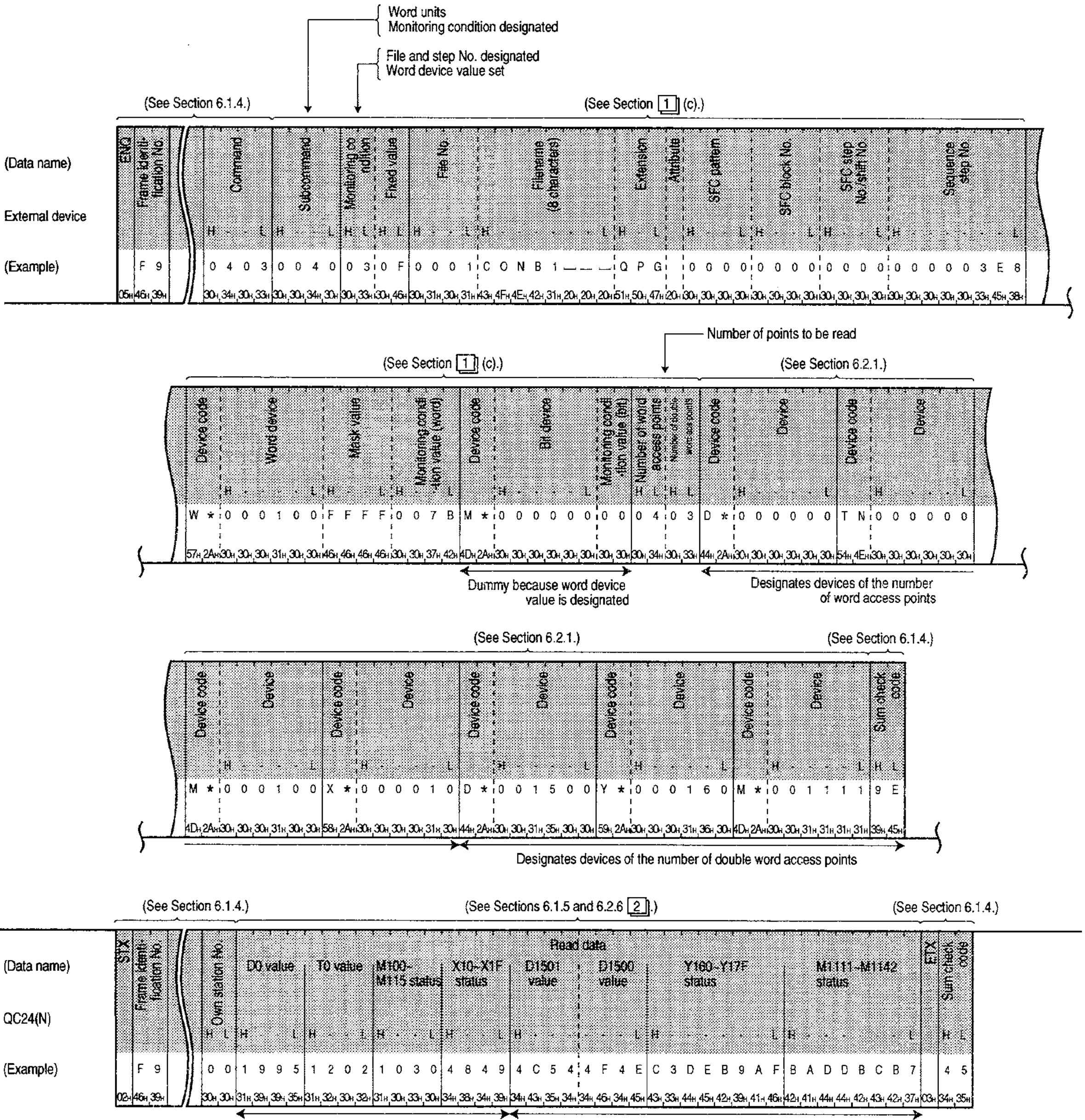
(a) When using ASCII mode format 1 to read the following contentsat random

① Monitoring condition

When the value of link register W100 reaches [7BH] (123) during program file CONB1.QPG step No. 1000 execution

② Read device memories

- Word access D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



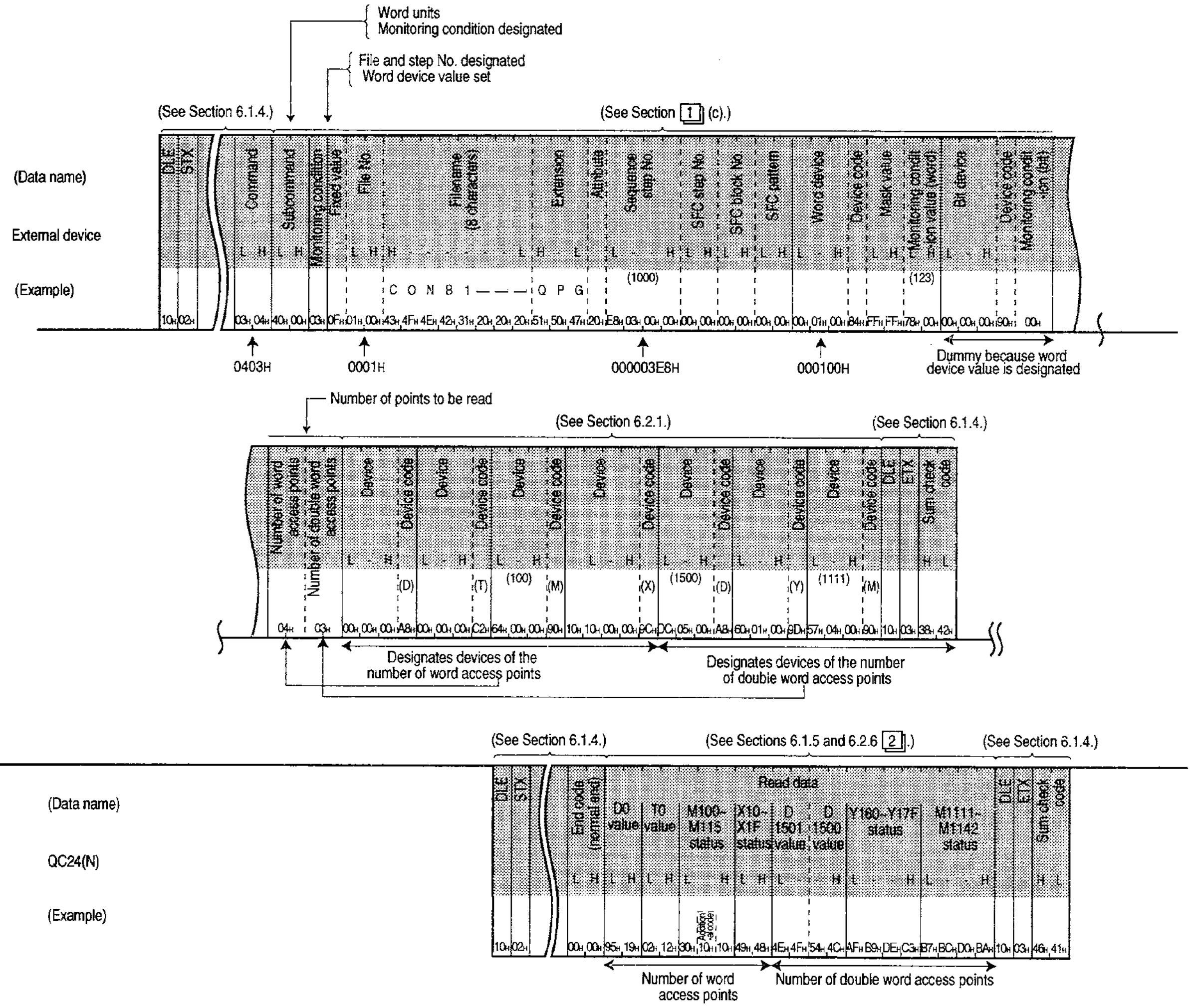
(b) When using binary mode format 5 to read the following contents at random

① Monitoring condition

When the value of link register W100 reaches [7BH] (123) during program file CONB1.QPG step No. 1000 execution

② Read data memories

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F M1111 to M1142



POINTS

(1) Designate the number of access points within the following range. (This also applies when a monitoring condition is not designated.)
For bit device, one word access point is 16 bits and one double word access point is 32 bits.
For word device, one word access point is 1 word and double word access point is 2 words.

① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10

- Number of access points ... 1 ≤ (number of word access points +number of double word access points) ≤ 96

② When accessing a PLC CPU other than ① above

- Number of access points ... 1 ≤ (number of word access points) ≤ 10

(2) When accessing the bit device of a PLC CPU other than ① above, always make the device No. a multiple of 16 (for decimal, 0,16...).

6.2.7 Random write in bit units (test) (command: 1402)

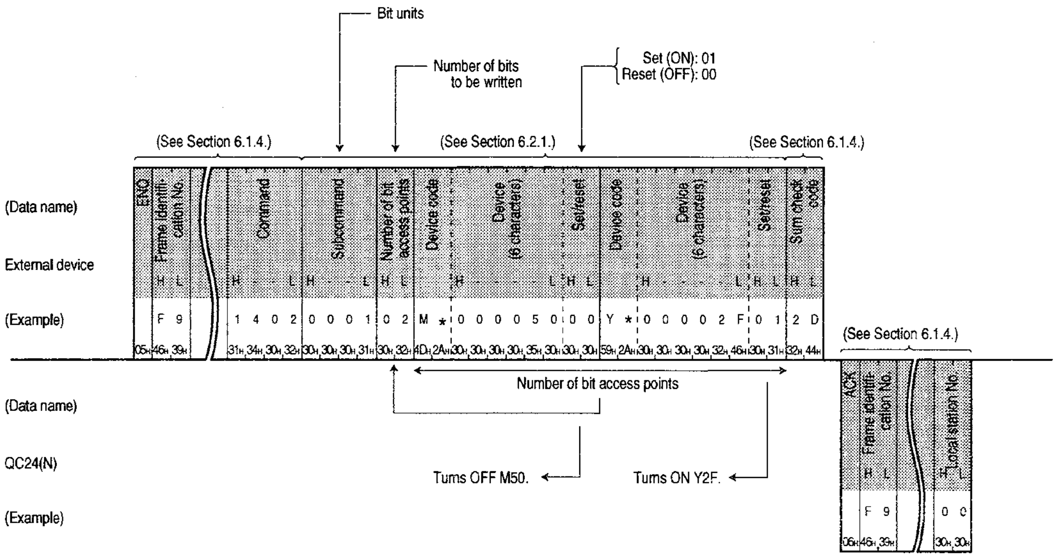
This section uses examples to describe the control procedure that writes data while designating bit device memories at random.

[Control Procedure]

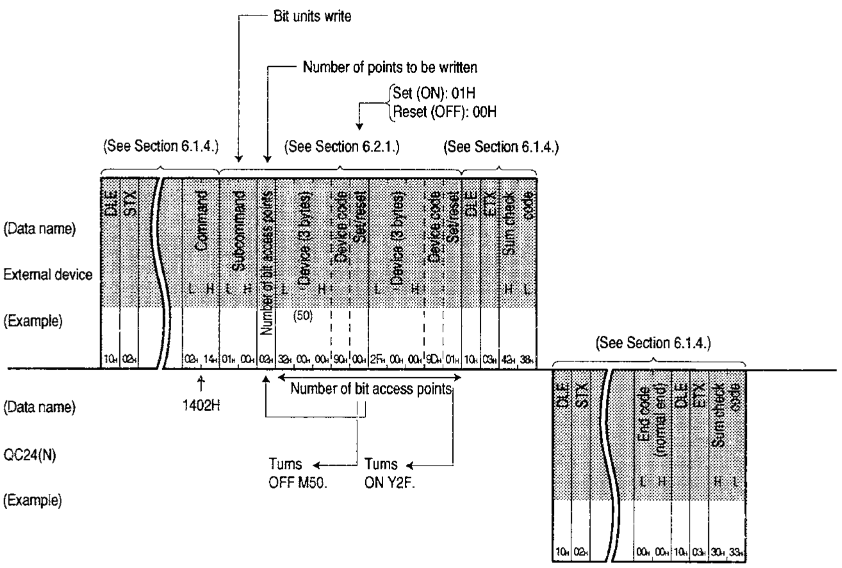
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to turn OFF internal relay M50 and turn ON output relay Y2F



(b) When using binary mode format 5 to turn OFF internal relay M50 and turn ON output relay Y2F



POINTS

(1) Designate the number of access points within the following range.
   ① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10
      - Number of access points ... 1 ≤ number of access points ≤ 94
   ② When accessing a PLC CPU other than ① above
      - Number of access points ... 1 ≤ number of access points ≤ 20

(2) When writing to a QnACPU, if system-protect (system-protect SW5: ON) is applied to the QnACPU, the QC24(N) will recognize an error and return a NAK message to the external device.

6.2.8 Random write in word units (test) (command: 1402)

This section uses examples to describe the control procedure that writes data while designating bit device memories (16/32 bit units) and word device memories (1/2 word units) at random.

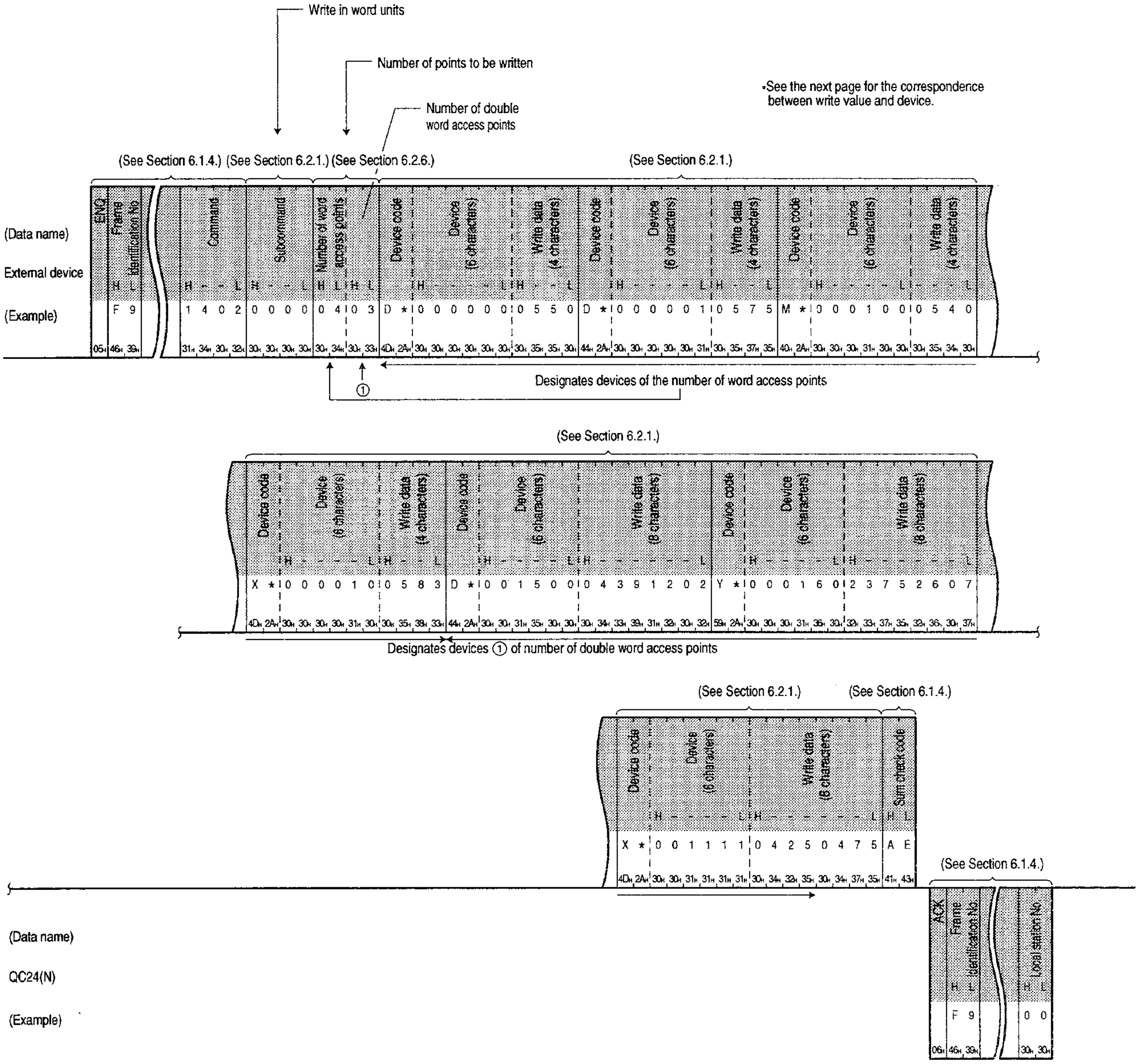
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

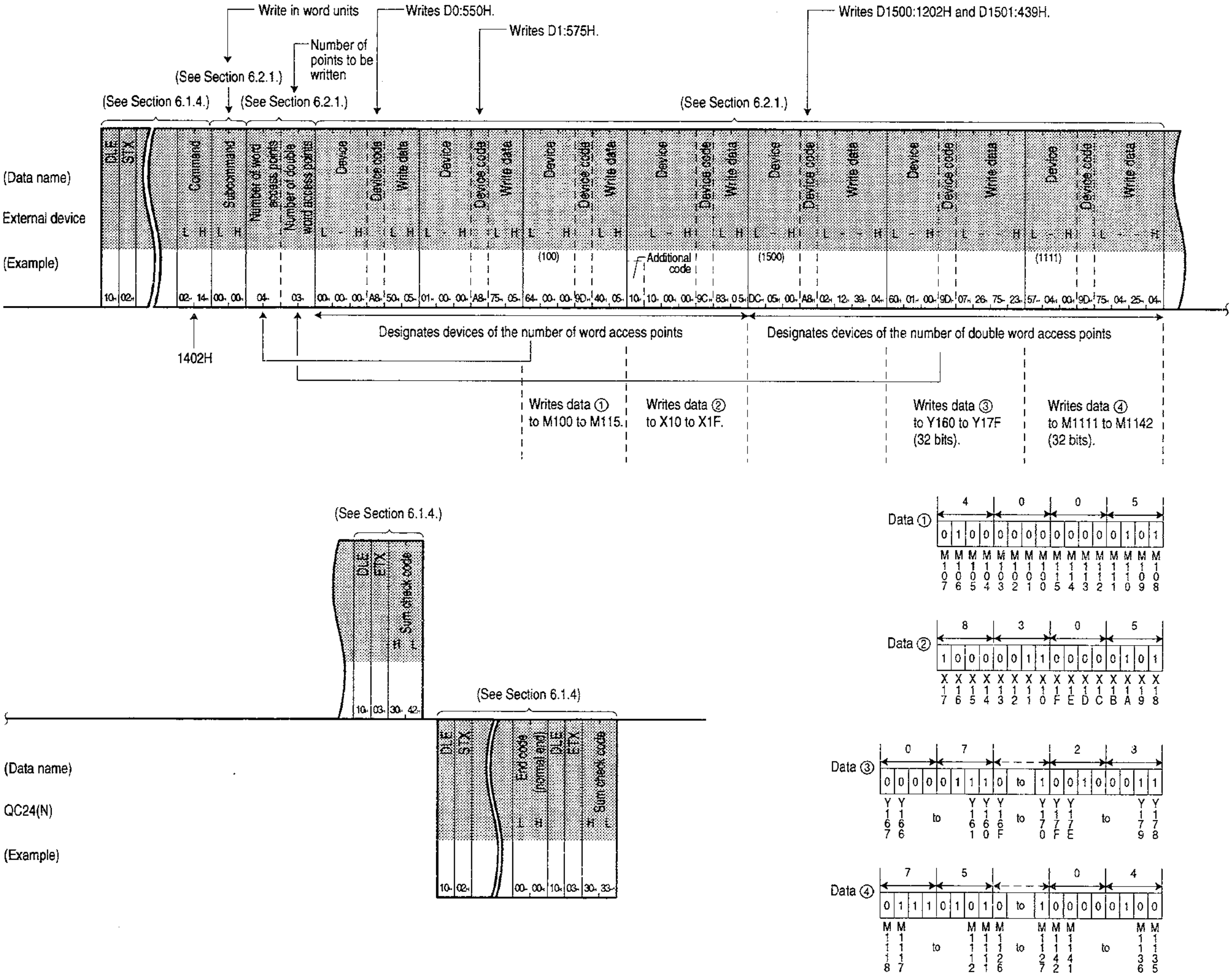
(a) When using ASCII mode format 1 to write to the following device memories

- Word access: D0, D1 M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



(b) When using binary mode format 5 to write to the following device memories

- Word access: D0, D1, M100 to M115 X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



POINTS

(1) Designate the number of access points within the following range.
For bit device, one word access point is 16 bits and one double word access point is 32 bits.
For word device, one word access point is 1 word and double word access point is 2 words.

① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10
Number of access points .... 1 ≤ (number of word access points x 12 + number of double word access points x 14) ≤ 960

② When accessing a PLC CPU other than ① above
Number of access points .... 1 ≤ (number of word access points) ≤10

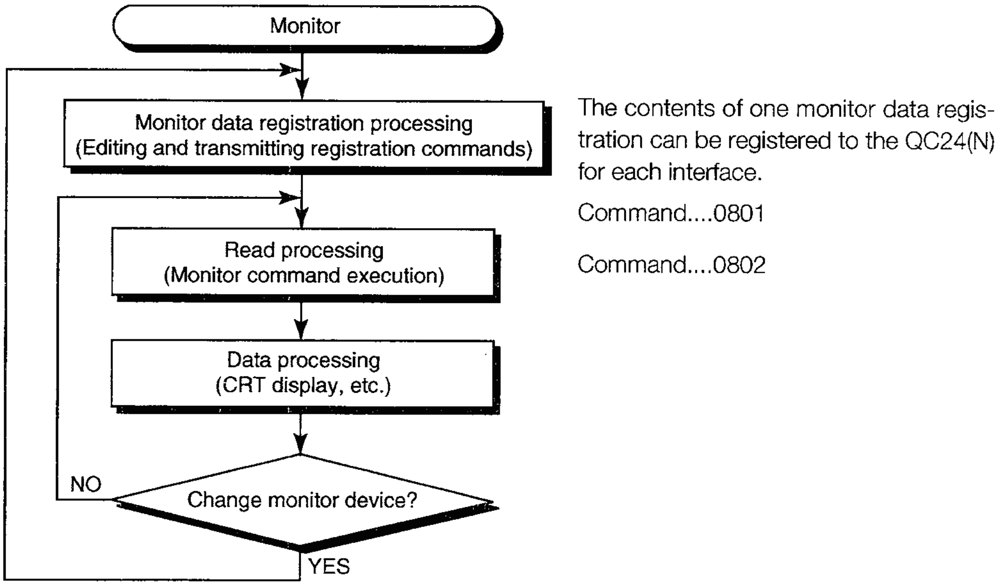
(2) When accessing the bit device of a PLC CPU other than ① above, always make the device No. a multiple of 16 (for decimal, 0,16...).

(3) When writing to a QnACPU, if system-protect (system-protect switch SW05: ON) is applied to the QnACPU, the QC24(N) will recognize an error and return a NAK message to the external device.

6.2.9 Device memory monitoring

The monitor data registration function registers the name and number of the devices to be monitored from an external device to the QC24(N).
The monitor function reads the data content of the registered device from the PLC CPU and processes it in the external device.
When the batch read function (see Section 6.2.3) is used to read the devices, the device numbers must be consecutive. However, by using the monitor data registration function, devices can be monitored by designating the device numbers at random.
The following uses examples to describe the control procedure to monitor and to registers the monitoring control procedure and the name and number of the devices to be monitored to the QC24(N).

1 Monitoring procedure



POINTS

(1) The device memory monitor function can read data as follows.
The designation method and control procedure character field data contents and the data monitoring (read) timing are the same as when the word units random read function is used. See Section 6.2.6 for more information.
① Bit device memory and word device memory designated together.
② Bit device memory can be read in 16/32 bit units and word device memory can be read in 1/2 word units.
③ The data monitoring (read) timing monitoring condition can be designated by monitoring data registration. (Multiple conditions can be combined and designated.)

(2) One QnACPU device memory cannot be conditionally monitored from a special function module and GPP function peripheral device at the same time.
When an external device sent the following command message to the QC24(N), if another special function module and GPP function peripheral device conditionally monitor the same QnACPU, the QC24(N) will send an NAK message to the external device. (When unconditional monitoring is performed, conditional/unconditional monitoring can be performed from the QC24(N).)

Command	Function	Function description
0403	Word units random read	Section 6.2.6
0802	Registered device memory monitoring	This Section 4

(3) When monitoring is executed as shown above, monitoring data must always be registered. If monitoring is performed without registering the monitoring data, a protocol error will be generated.

2 Monitoring data registration (command: 0801) (When not designating the monitoring condition)

This section uses an example to describe the monitoring data registration control procedure for monitoring the device memories without monitoring condition (read condition) by designating the bit device memories (16/32 bit units) and word device memories (1/2 word units) at random.

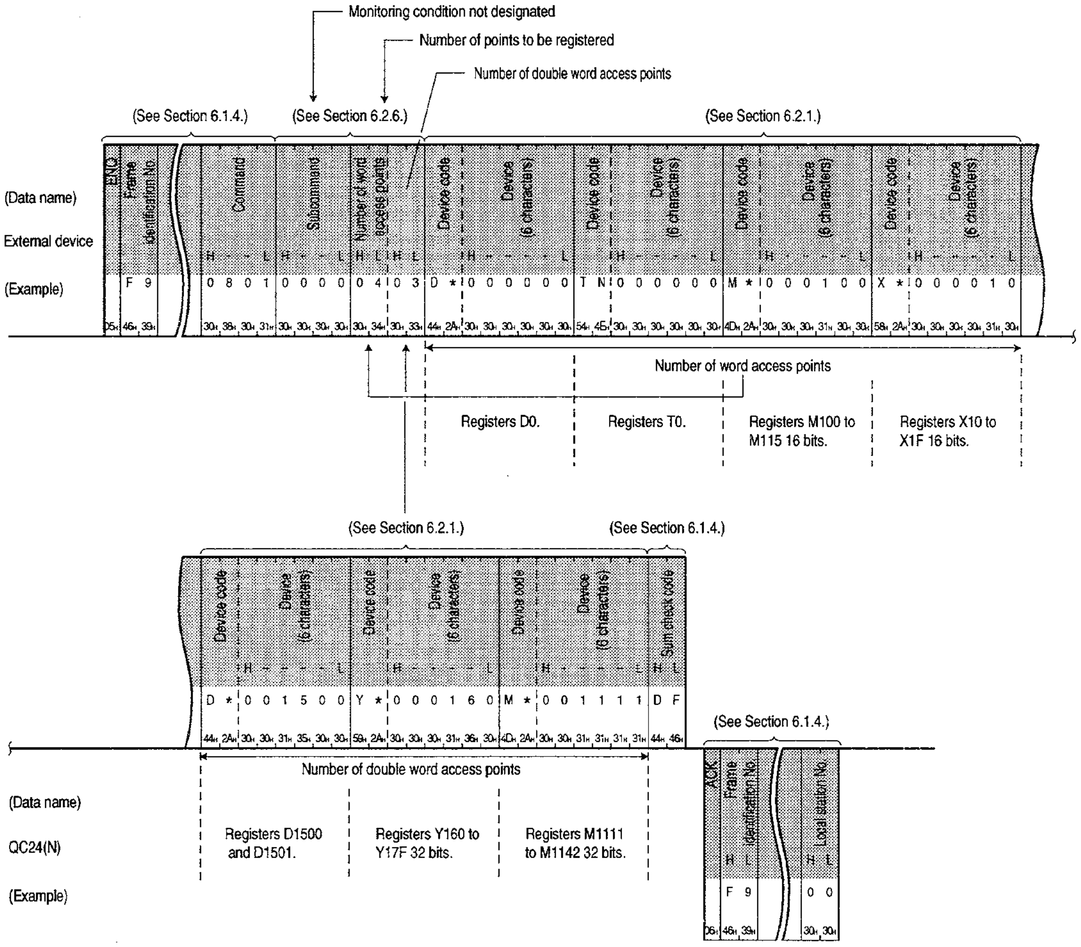
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

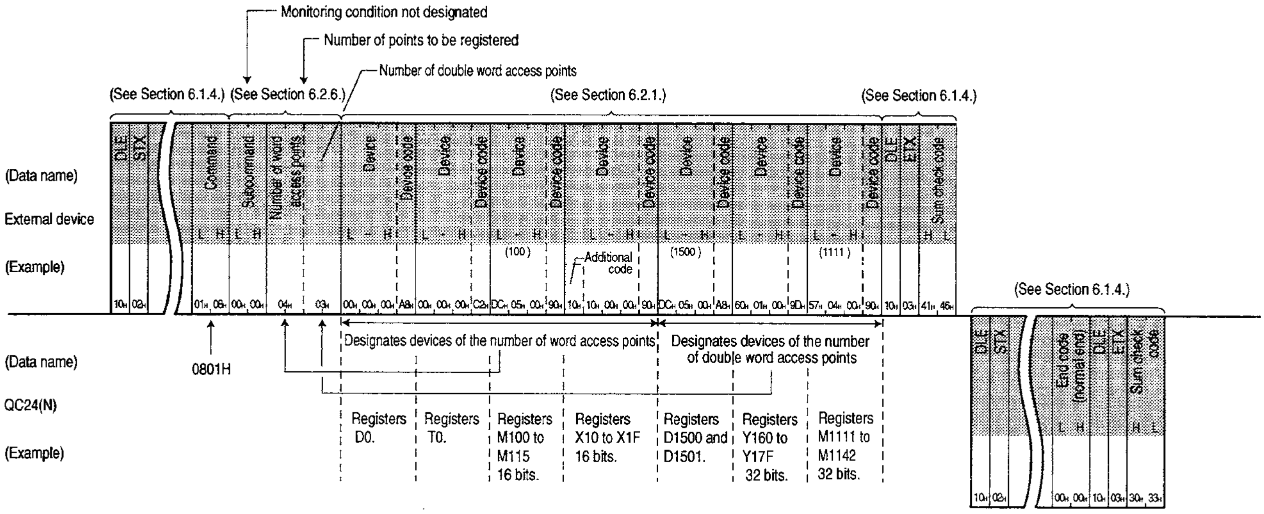
(a) When using ASCII mode format to register the monitoring data for the following device memories

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



(b) When using binary mode format 5 to register monitor data for the following device memories

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



POINTS

(1) Designate the number of access points within the following range. (This also applies when a monitoring condition is designated.)
For bit device, one word access point is 16 bits and one double word access point is 32 bits.
For word device, one word access point is 1 word and one double word access point is 2 words.
① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10
- Number of access points ... 1 ≤ (number of word access points + number of double word access points) ≤ 96

② When accessing a PLC CPU other than ① above
- PLC CPU other than ① above cannot be accessed.

(2) When accessing the bit device of a PLC CPU other than ① above, always make the device No. a multiple of 16 (for decimal, 0,16...).

3 Monitoring data registration (command: 0801) (When designating the monitoring condition)

The following uses examples to describe the monitoring data registration control procedure for monitoring device memories by designating the monitoring condition and designating bit device memories (16/32 bit units) and word device memories (1/2 word units) at random.

[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

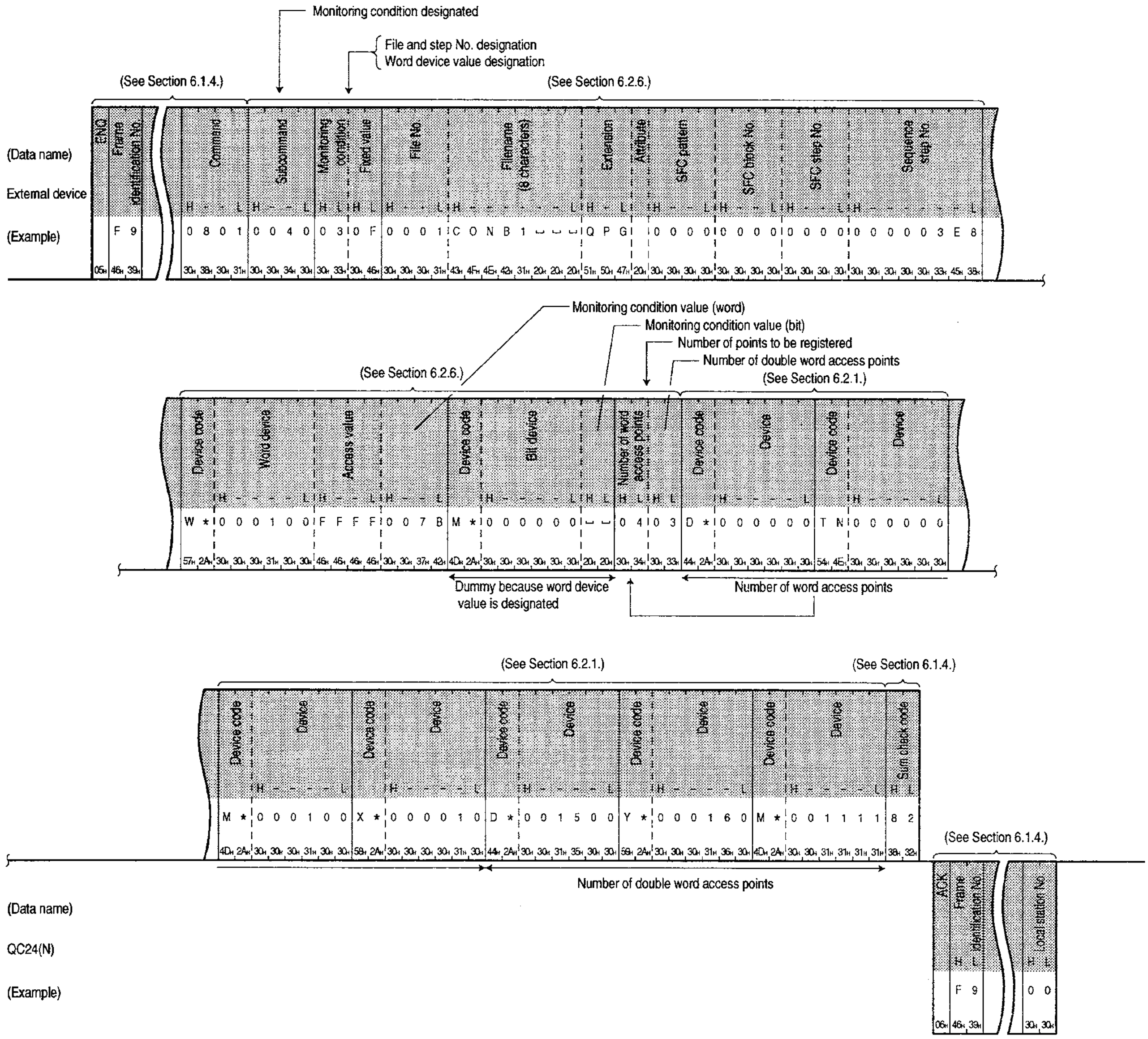
(a) When using ASCII mode format 1 to monitor the following monitoring data

① Monitoring condition

When the value of link register W100 reaches [78H] (123) while step No. 1000 of the program file CONB1. QPG sequence program is executing

② Device memories to be monitored (read)

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D15010, Y160 to Y17F, M1111 to M1142



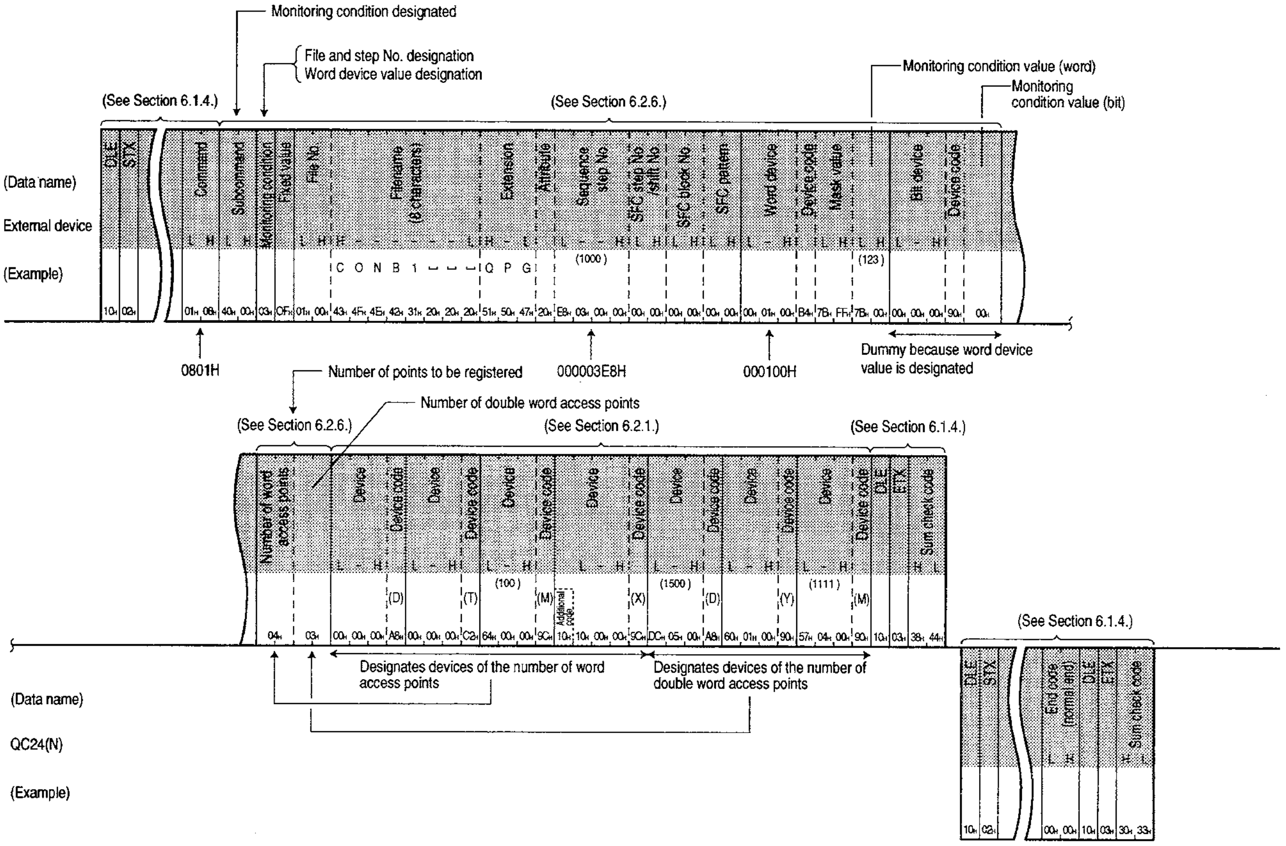
(b) When using binary mode format 5 to register the following monitoring data

① Monitoring condition

When the value of link register W100 reaches [7BH] (123) while step No. 1000 of the program file CONB1. QPG is executing

② Device memories to be monitored (read)

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



POINTS

(1) Designate the number of access points within the following range. (This also applies when a monitoring condition is not designated.)
For bit device, one word access point is 16 bits and one double word access point is 32 bits.
For word device, one word access points is 1 word and one double word access point is 2 words.

① When accessing an external device connection station QnACPU and a QnACPU over a MELSECNET/10

- Number of access points ... 1 ≤ (number of word access points +number of double word access points) ≤ 96

② When accessing a PLC CPU other than ① above

- PLC CPU other than ① above cannot be accessed.

(2) When accessing the bit device of a PLC CPU other than ① above, always make the device No. a multiple of 16 (for decimal, 0, 16....).

4 Monitoring registered device memories (command: 0802)

The following uses examples to describe the control procedure that monitors a device memory registered using monitor data registration (command: 0801).
The monitoring control procedure is the same regardless of whether or not a monitoring condition is designated during monitoring data registration.

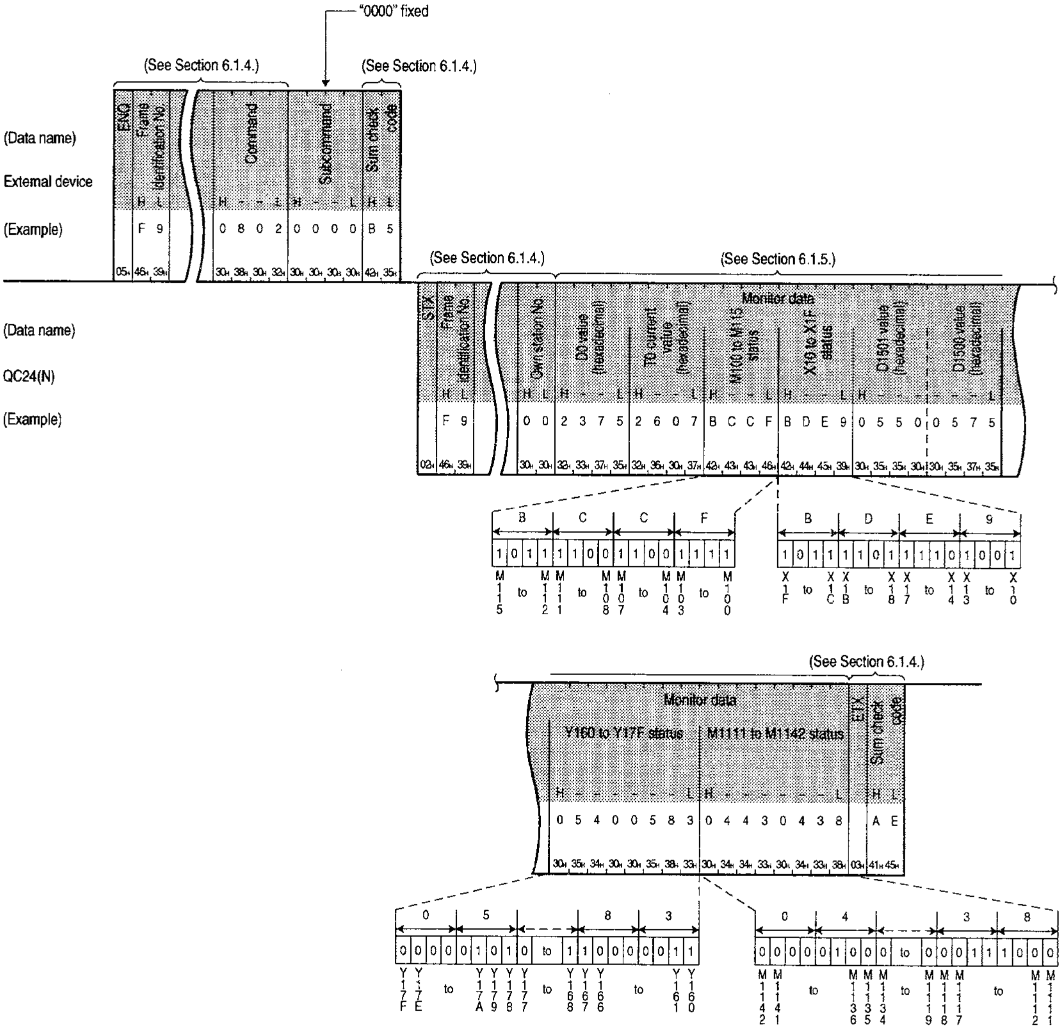
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

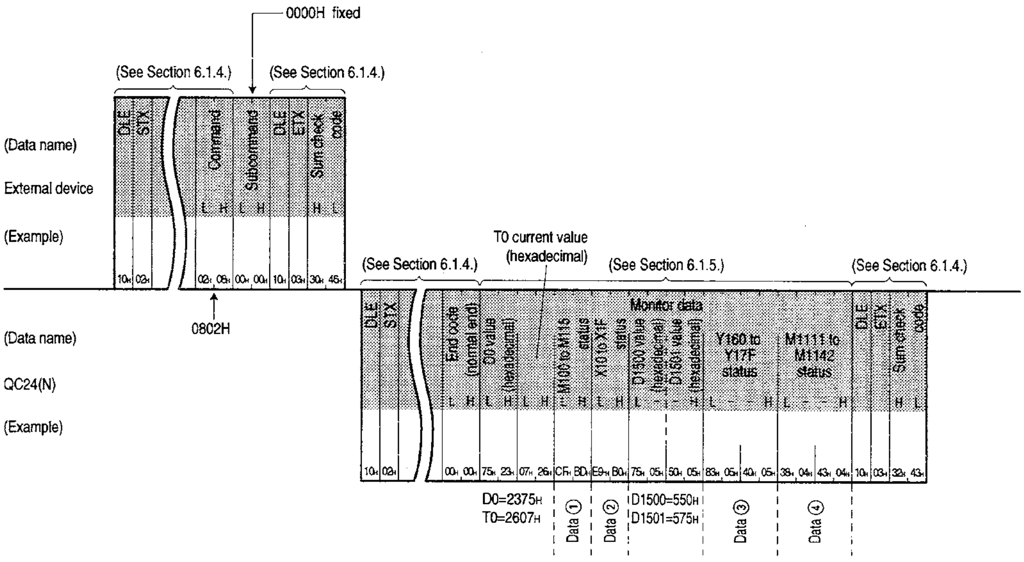
(a) When using ASCII mode format 1 to monitor the following device memories with monitoring data registered
(Device memories with monitoring data registered)

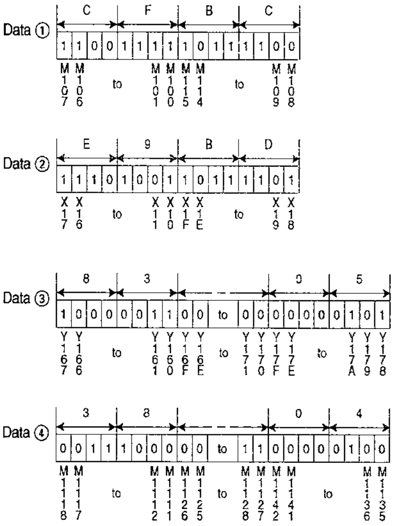
- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142



(b) When using binary mode format 5 to monitor a the following device memories with monitoring data registered
(Device memories with monitor data registered)

- Word access: D0, T0, M100 to M115, X10 to X1F
- Double word access: D1500 to D1501, Y160 to Y17F, M1111 to M1142





Applicable module	AJ71QC24			A1SJ71QC24		AJ71QC24N			A1SJ71QC24N	
	–	-R2	-R4	–	-R2	–	-R2	-R4	–	-R2
Function availability	×	×	×	×	×	△	△	△	△	△
Remark	–					See Section 1.4				

6.2.10 Multiple block batch read and batch write (command : 0406, 1406)

The control procedure and other items related to executing data read and data write from the external device to the device memory of the QnACPU using the multiple block batch read and batch write are described.

1 Overview of the function

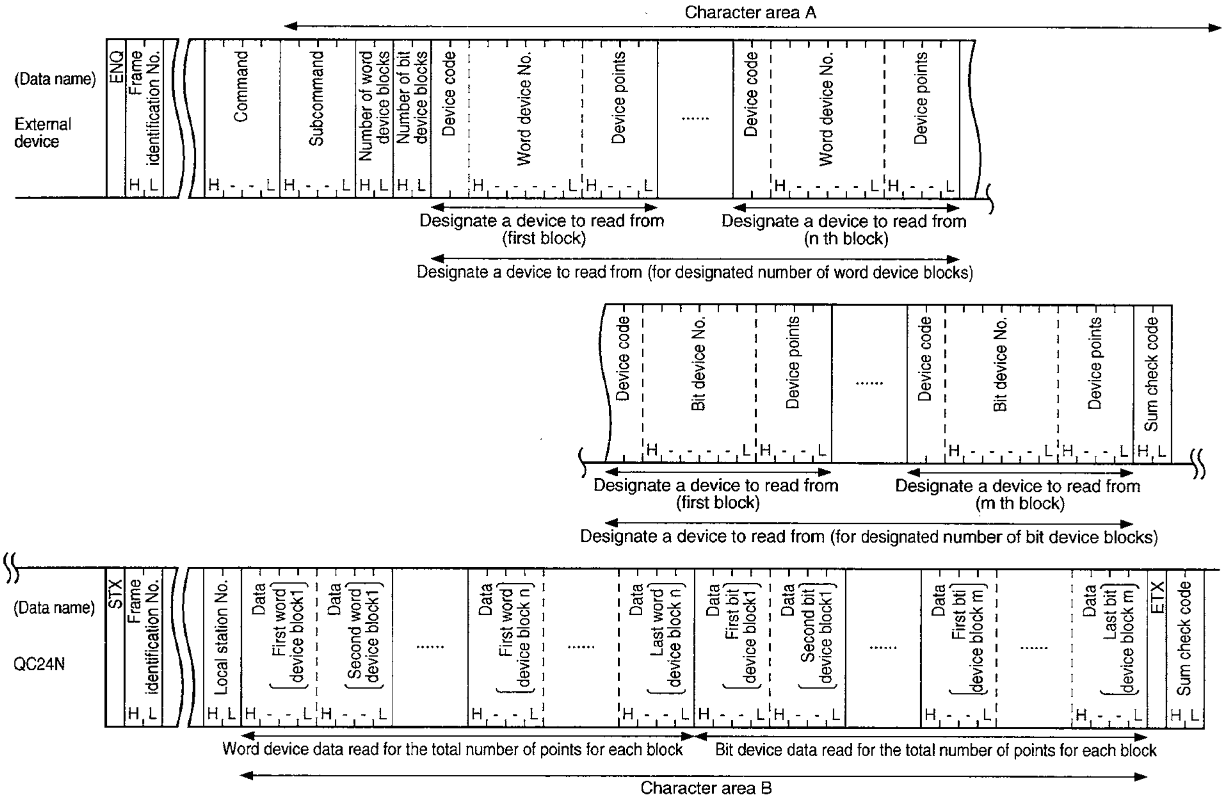
Using the multiple block batch read and batch write, by defining n points of QnACPU's word device and bit device (one point occupies 16 bits) as one block, the external device can randomly designate multiple blocks to execute a batch read and a batch write of the data.

2 PLCs for which the multiple block batch read and batch write are allowed

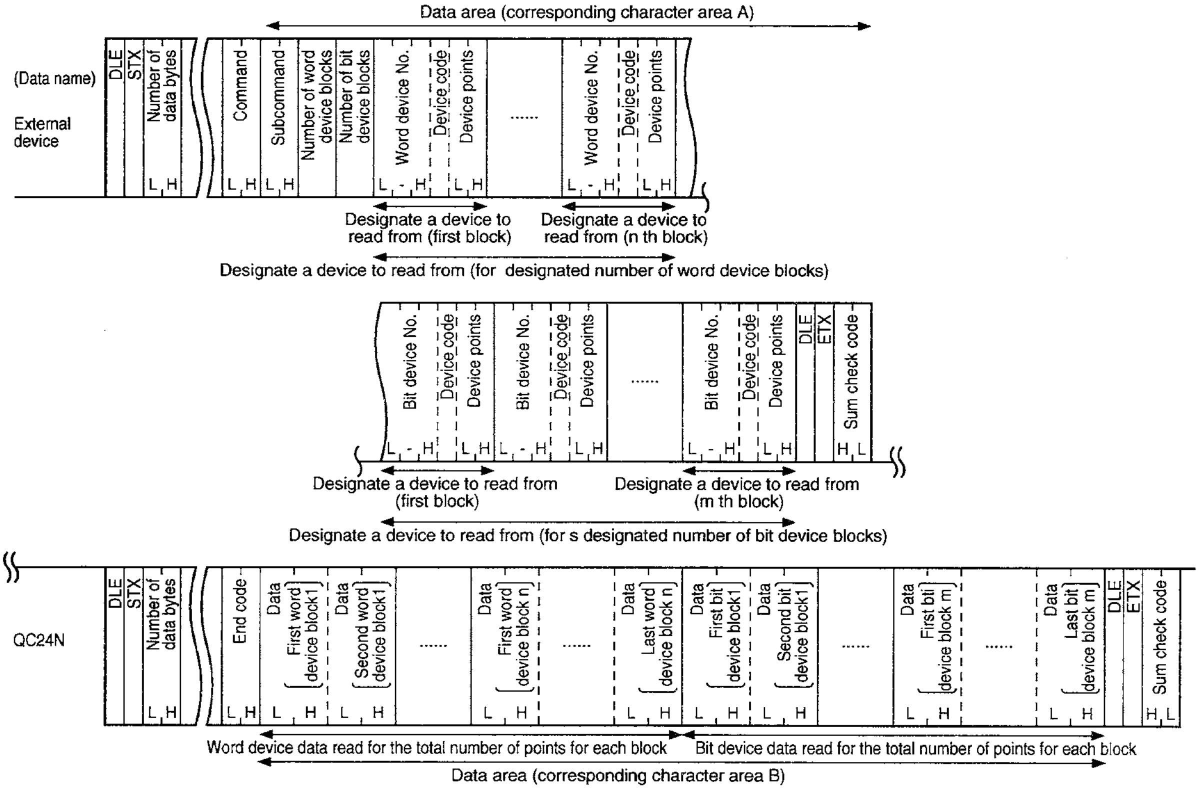
The data communication is allowed with the local station with the QC24N, QnACPU (QnACPU shown in Section 1.4) of remote station via MELSECNET/10 installed.

3 Data order in the character area during the multiple block batch read

① QnA (extension) frame data order for ASCII mode (format 1)

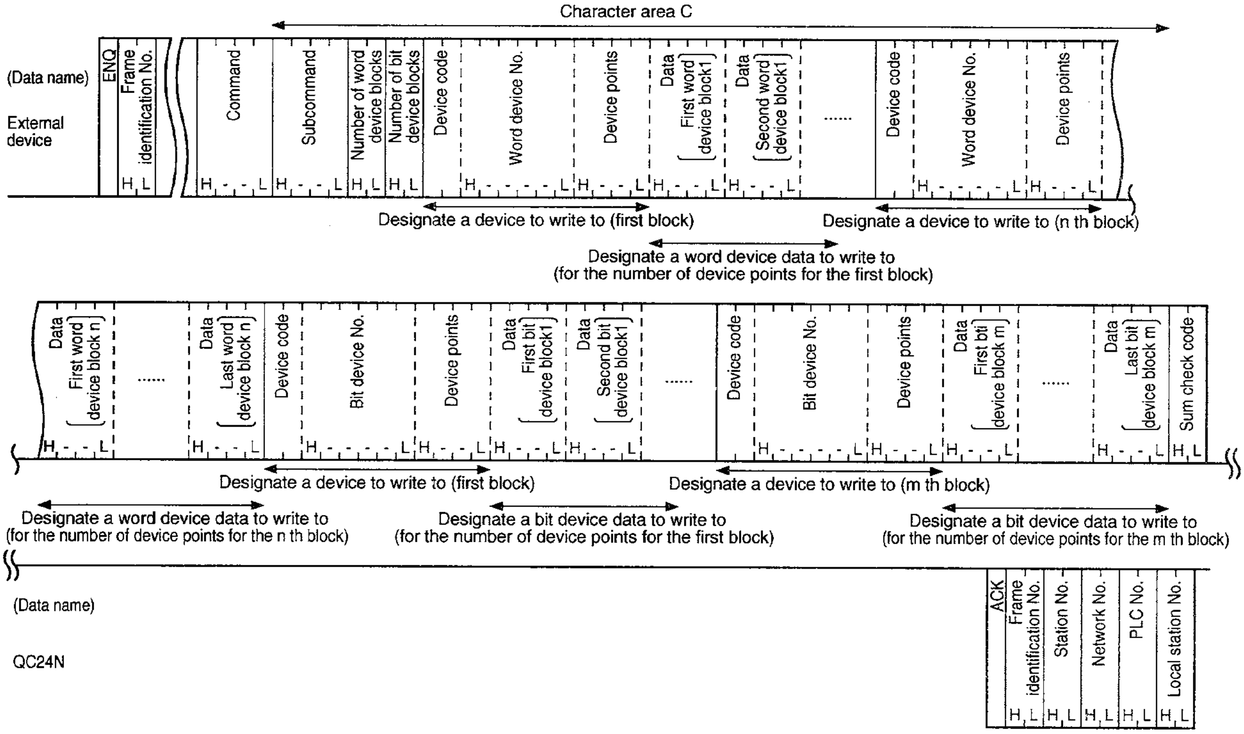


② QnA extension frame data order for binary mode

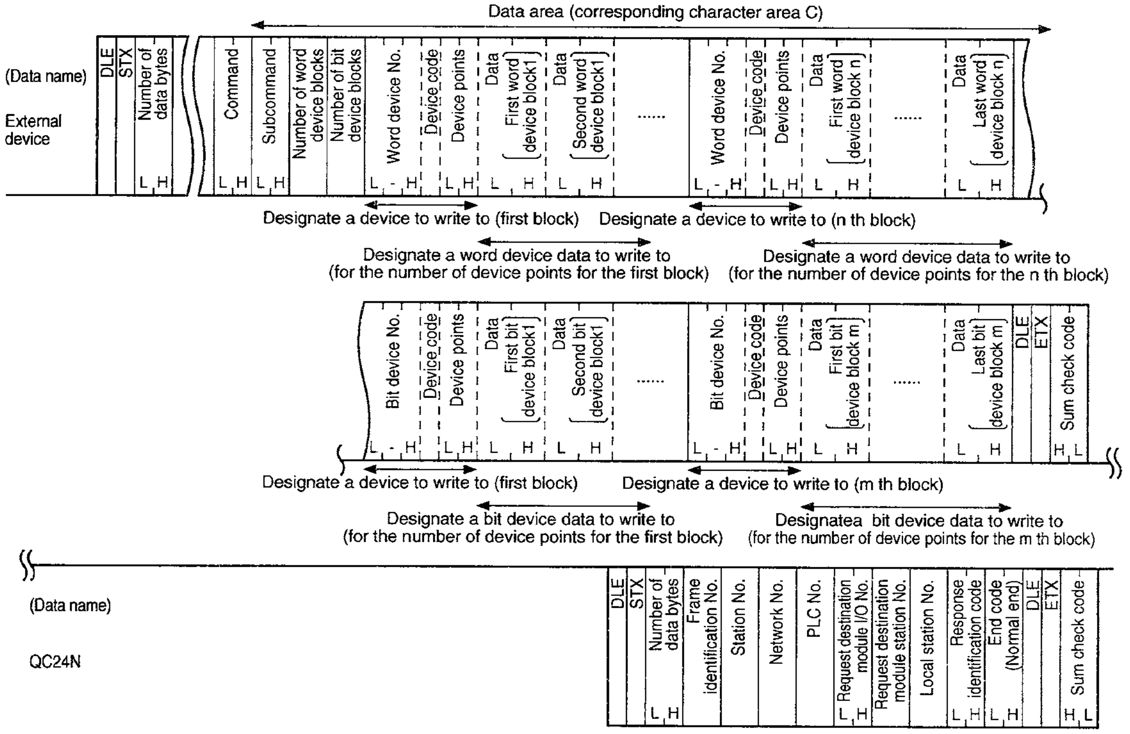


4 Data order in the character area during the multiple block batch write

① QnA (extension) frame data order for ASCII mode (format 1)



② QnA extension frame data order for binary mode



5 **Details of the multiple block batch read and batch write**

Details of the multiple block batch read and batch write are described.

Besides the data shown below, the details are the same as when using the other commands.

(a) Number of word device blocks and number of bit device blocks

Designates each of the number of word device blocks or bit device blocks to be sent directly after this data in the batch read or batch write to the word device and bit device.

① Data exchange in ASCII mode

Each number of blocks are converted to 2-digit ASCII code (hexadecimal) and transmitted.

(Example) For 5 blocks .... Becomes "05", and transmitted starting from "0".

For 20 blocks ..... Becomes "14", and transmitted starting from "1".

② Data communication in binary mode

Transmits 1-byte numeric value indicating each number of blocks.

(Example) For 5 blocks .... 05H is transmitted.

For 20 blocks ..... 14H is transmitted.

③ Designate each number of blocks so the following is satisfied:

120 ≥ number of word device blocks + number of bit device blocks

④ When setting one of the number of blocks to 0, the corresponding device number, device code, device points, and data designations are not necessary.

(b) Word device number and bit device number

Designates the head word device or bit device for each block to which batch read or batch write is performed, when continuous word/bit devices are used as one block.

① Data communication in ASCII mode

The head device number of each block is converted to 6-digit ASCII code and transmitted.

(Example) For internal relay M1234 and link register W1234:

The internal relay M1234 is converted to "001234" or "␣␣1234" and the link register W1234 "001234" or "␣␣1234". The transmission starts from "0" or "␣".

② Data communication in binary mode

The head device number of each block is indicated in a 3-byte numeric value and transmitted.

(Example) For internal relay M1234 and link register W1234:

The internal relay M1234 is converted to 0004D2H and transmitted in the order, D2H, 04H, and 00H.

The link register W1234 is converted to 001234H and transmitted in the order 34H, 12H, and 00H.

(c) Device code

Identifies the head device memory for each block for batch read and batch write.

The device code for each device is shown in Section 6.2.1 3 .

① Data communication in ASCII mode

Each device code is converted to 2-digit ASCII code (hexadecimal) and transmitted.

(Example) For internal relay (M) and link register (W):

The internal relay (M) is converted to "M*" and link register (W) to "W*", and transmitted in the order "M" to "W".

② Data communication in binary mode

1-byte numeric value indicating each device code is transmitted.

(Example) For internal relay (M) and link register (W):

The internal relay (M) is transmitted as 90H, and link register (W) is transmitted as B4H.

(d) Device points

This is used when the continuous word devices or bit devices are used as one block.

It designates the number of points in the continuous device range of each block for batch read or batch write (1 point=16 bits for bit device memory and 1 point=1 word for word device memory).

① Data communication in ASCII mode

The number of points for each block is converted to a 4-digit ASCII code (hexadecimal) and transmitted.

(Example) For 5 points........ Converted to "0005" and transmitted starting from "0".

For 20 points...... Converted to "0014" and transmitted starting from "0".

② Data communication in binary mode

2-byte numeric value indicating the number of points for each block is transmitted.

(Example) For 5 points........ Converted to 0005H and transmitted starting from 05H.

For 20 points...... Converted to 0014H and transmitted starting from 14H.

③ Each device points must be designated in the following range:

- For multiple block batch read

  480 ≥ total number of points for all word device blocks + total number of points for all bit device blocks

- For multiple block batch write

  480 ≥ 4 x (number of word device blocks + number of bit device blocks) + total number of points for all word device blocks + total number of points for all bit device blocks

POINT

The extension designation is allowed to the device memory to which a read or write is performed by the multiple block batch read and batch write function.

See the explanation in Section 6.2.11 to make an extension designation to the device memory.

6 Multiple block batch read (command: 0406)

This section uses an example to explain the control procedure for reading by designating multiple blocks randomly, when n-points of continuous bit device memory (1 point = 16 bits) and word device memory is considered as one block.

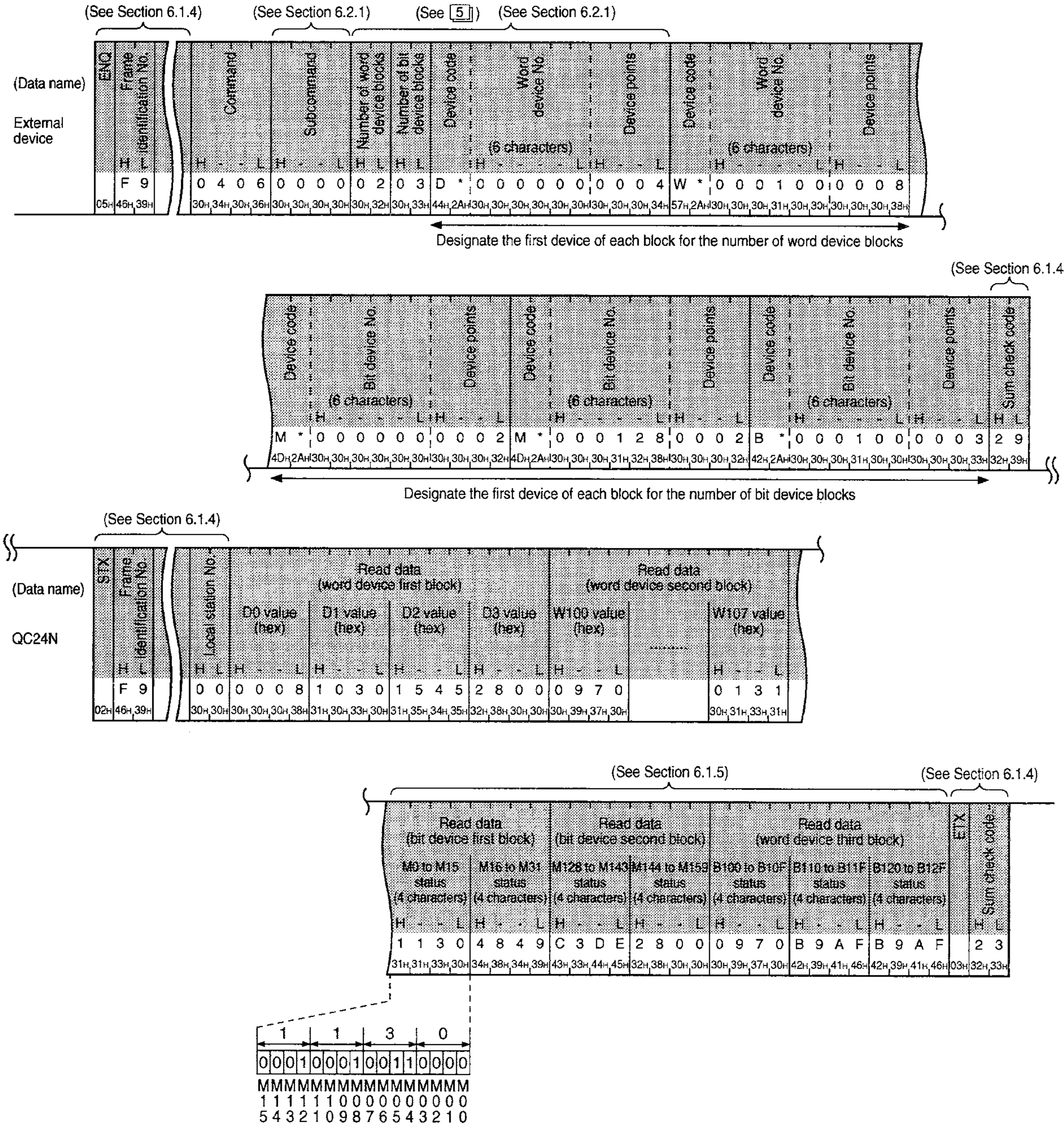
[Control procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Sections 6.1.1 and 6.1.2 after seeing this description.

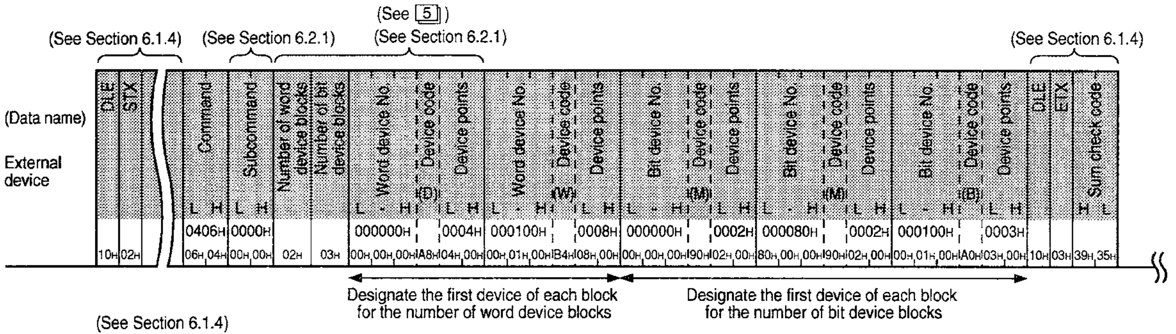
(a) When the following device memory is read in ASCII mode format 1:

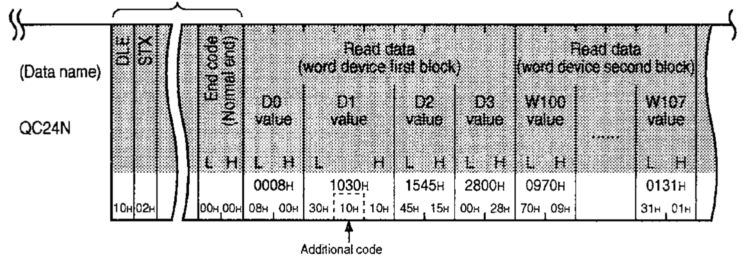
- Word device memory : 2 blocks ; D0 to D3 (4 points), W100 to W107 (8 points)
- Bit device memory : 3 blocks ; M0 to M31 (2 points), M128 to M159 (2 points), B100 to B12F (3 points)

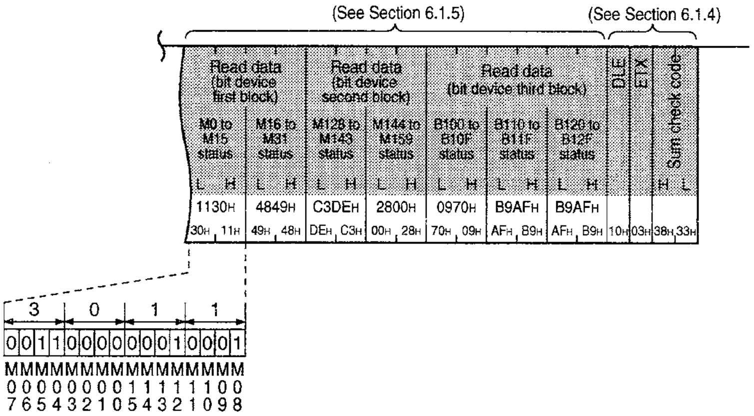


(b) **When the following device memory is read in binary mode format 5:**

- Word device memory : 2 blocks ; D0 to D3 (4 points), W100 to W107 (8 points)
- Bit device memory : 3 blocks ; M0 to M31 (2 points), M128 to M159 (2 points), B100 to B12F (3 points)







POINT

(1) Designate the number of blocks so that the following is satisfied:
120 ≥ number of word device blocks + number of bit device blocks

(2) Designate each device points so that the following is satisfied:
480 ≥ total number of points for all word device blocks + total number of points for all bit device blocks

7 Multiple block batch write (command:1406)

This section uses an example to explain the control procedure for writing by designating multiple blocks randomly, when n-points of continuous bit device memory (1 point = 16 bits) and word device memory is considered as one block.

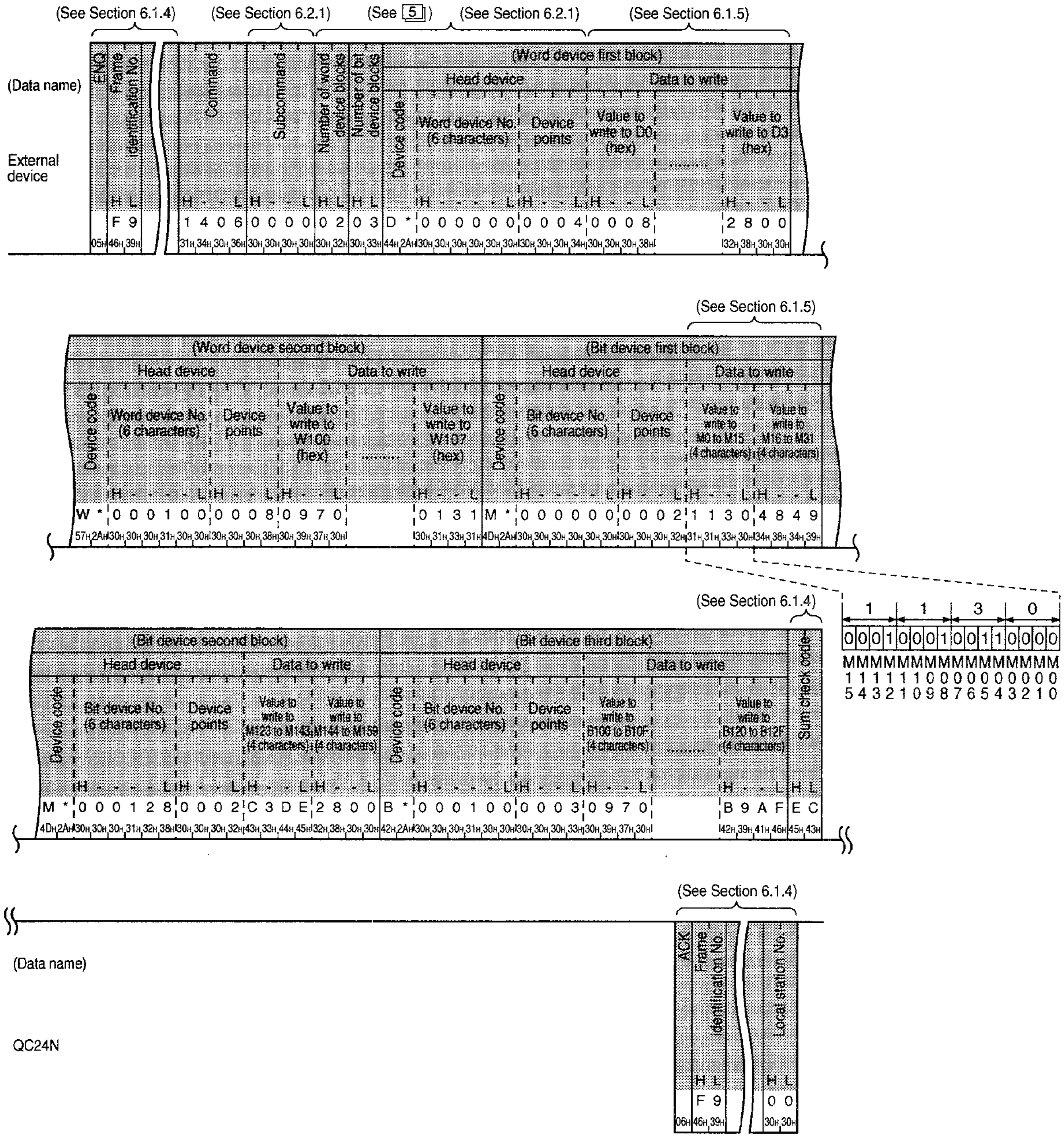
[Control procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Sections 6.1.1 and 6.1.2 after seeing this description.

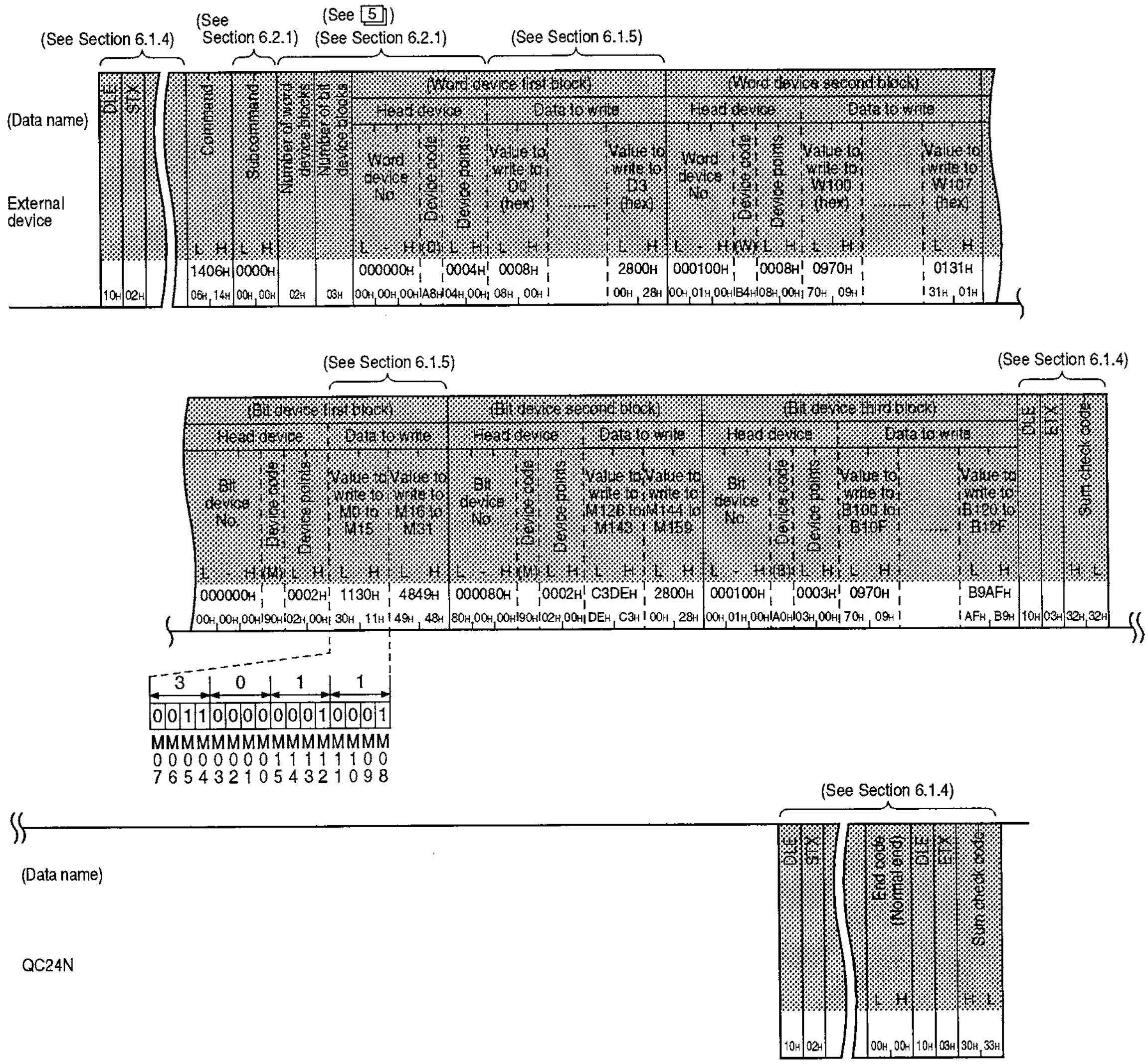
(a) When the following device memory is written in ASCII mode format 1:

- Word device memory : 2 blocks ; D0 to D3 (4 points), W100 to W107 (8 points)
- Bit device memory : 3 blocks ; M0 to M31 (2 points), M128 to M159 (2 points), B100 to B12F (3 points)



(b) When the following device memory is written in binary mode format 5:

- Word device memory : 2 blocks ; D0 to D3 (4 points), W100 to W107 (8 points)
- Bit device memory : 3 blocks ; M0 to M31 (2 points), M128 to M159 (2 points), B100 to B12F (3 points)



POINT

Designate each device points so that the following is satisfied:
$480 \geq 4 \times$ (number of word device blocks + number of bit device blocks) + total number of points for all word device blocks + total number of points for all bit device blocks

6.2.11 Device memory read/write by extension designation

Device memory extension designation designates external devices other than the devices given in Section 6.2.1 $\boxed{3}$ and qualifies and designates the device No., network No., etc. of the device memory to be accessed. The following gives a general description of device memory extension designation.
In the descriptions following this section, these designation expressions are shown as [Designation-1] to [Designation-2].

[Designation-1]

Designation for accessing a MELSECNET/10 link direct device. (Link input, link output, link special relay, etc. (See Table $\boxed{2}$).)

[Designation-2]

Designation for accessing a QnACPU station or MELSECNET/10 remote station special function module special direct device. (Buffer register. See Table $\boxed{2}$ and Appendix 4.)

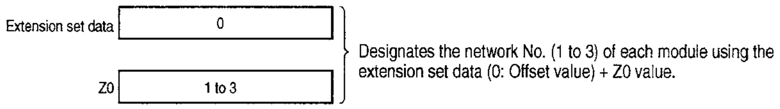
[Designation-3]

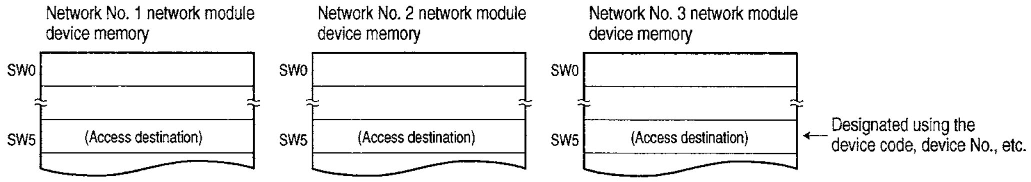
Designation of objective module using network No. and I/O signal extension setting qualification according to ① and ② below.

① Designation of objective module of [Designation-1] above
(Arbitrary network No.) + (network No. designated by index register) network module

② Designation of objective module of [Designation-2] above
(Arbitrary I/o signal No.) + (I/O signal No. designated by index register) special function module

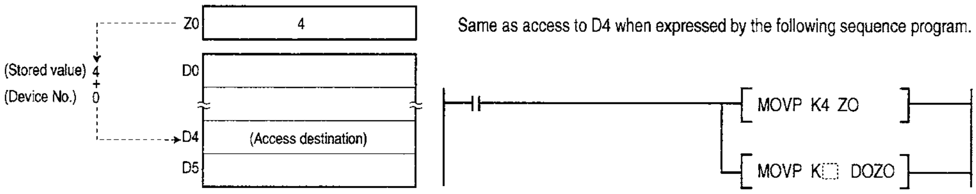
For instance, when two or more network modules are installed in the access station, an external device can access the same device (SW5) of each module by designating the extension set data inthe illustration shown below and index register [Z0].



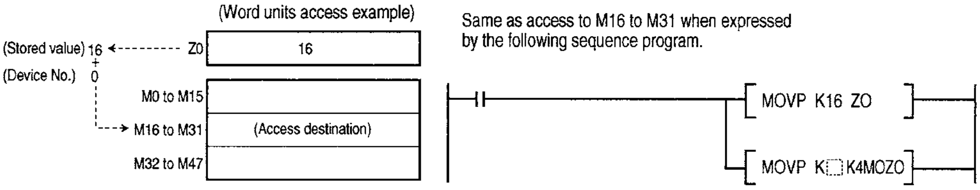


[Designation-4]

Designation of object module for [Designation-1], [Designation2], and Section 6.2.1 [3] devices using device No. and indexregister device qualification.
For instance, device memory (D4) can be accessed by D0 and Z0 designation.

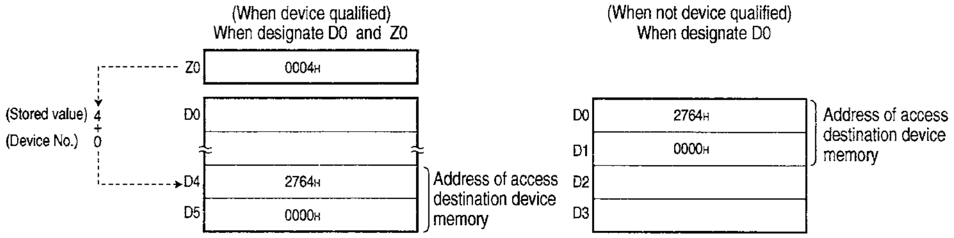


Device memories (M16 or M16 to M31, etc.) can also be accessed by M0 and Z0 designation.



[Designation-5]

Indirect designation of word device at which the stored value of the designated word device becomes the address of the access destination device memory.
In this case, the device memory allocated to device memory address 00002764H is accessed.



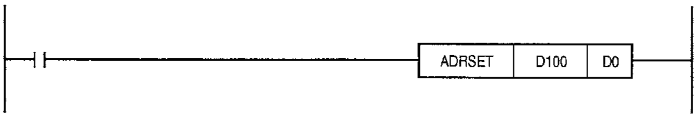
POINT

When an external device uses indirect designation to access adevice memory, do the following by agreement with the PLC CPU before carrying out the access.

① Use the PLC CPU ADRSET instruction to check the address on the memory allocated by the device memory to be accessed.

② Store the address checked at ① above to the device memory designated by indirect designation.

(Example) Sample sequence program that stores the address of D100 to D0, D1 when an external device accesses device memory D100.
(An external device can access D100 by indirectly designating D0.)



1 Character area data list and contents in device memory extension designation

The following describes the designation contents of the part added for extension designation during extension designation ofthe device memory to be read and written.

See Section 6.2.1 2 3 for the data items that are the same as when device memory is not extended.

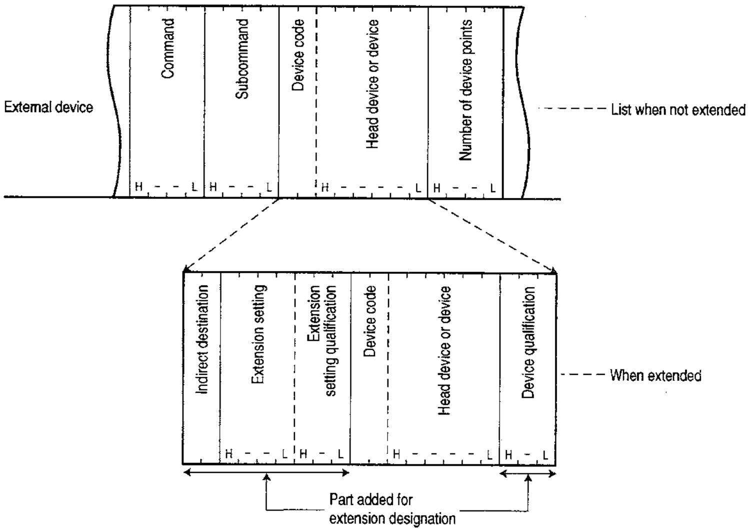
POINTS

(1) Extension designation replaces the device memory designation part when the device memory is not extended.

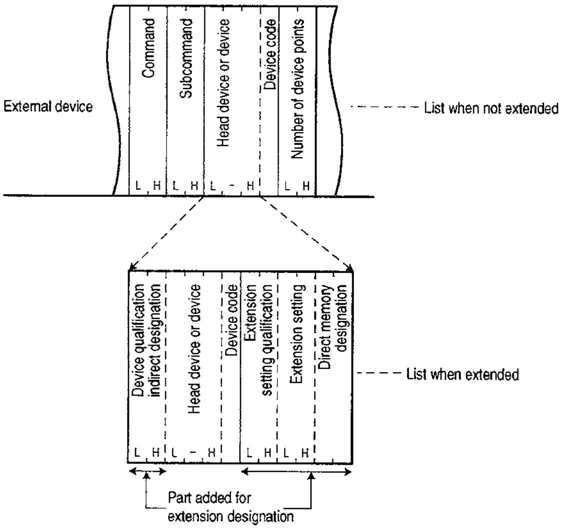
(2) When designating two or more device memories, use extension designation.

(a) Data list of device memory designation part when device memory extended

① ASCII mode QnA (extension) frame data list



② Binary mode QnA extension frame data list



(b) Contents of data area when device memory extended

The following shows the values assigned to the character area when dèvice memory is extended.

(ASCII mode)

		Value designated by external device					Number of designation characters
		[Designation-1]	[Designation-2]	[Designation-3]	[Designation-4]	[Designation-5]	
Sub-command	No monitoring condition	"0080"/"0081" (See ①.)					4
	Monitoring condition	"00C0"/"00C1" (See ①.)					
Indirect designation		"00"				"0@"	2
Extension designation		"J□" (See ②.)	"U□" (See ②.)	One of the designations at the left/ "0000" (See ②.)		"0000"	4
Extension setting qualification		"000"		"Z□" (See ③.)	One of the designations at the left (See ③.)	"000"	3
Device code		(See (2) (a) and Section 6.2.1 (3).)					2
Head device or device							6
Device qualification		"000"			"Z□" (See ④.)	One of the designations at the left (See ④.)	3

(Binary mode)

		Value designated by external device					Number of designation bytes
		[Designation-1]	[Designation-2]	[Designation-3]	[Designation-4]	[Designation-5]	
Sub-command	No monitoring condition	0080H/0081H (See ①.)					2
	Monitor condition	00C0H/00C1H (See ①.)					
Device qualification indirect designation		0000H			40□ H (See ④.)	0800H/□8□H (See ④.)	2
Head device or device		(See (2) (a) and Section 6.2.1 (3).)					3
Device code							1
Extension setting qualification		0000H		40□H (See ③.)	One of the designations at the left (See ③.)	0000H	2
Extension setting		□H (See ②.)				0000H	2
Direct memory designation		F9H	F8H	One of the designations at the left/00H (See ②.)		00H	1

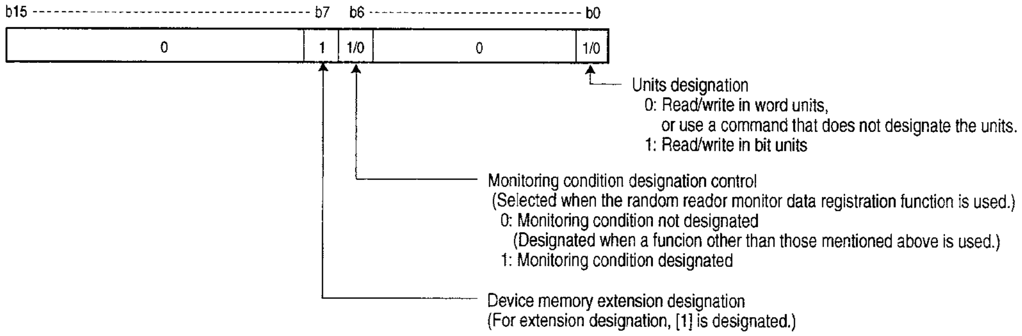
① Subcommand

This data designates the read/write units, kind of device to be designated, data read conditions, etc.

ⓐ Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

ⓑ Data communications in binary mode
The 2-byte value shown below is transmitted.

ⓒ The subcommand designation contents are shown below.



ⓓ Section 6.2.6 describes monitoring condition control (random read, monitor data registration) and the device memory read timing by monitoring condition designation.

ⓔ For device memory extension designation, the subcommand becomes 0080H, 0081H, 00C0H, or 00C1H, depending on the monitoring condition designation and units designation.

② Extension setting and direct memory designation

These data designate the device memory for an external device to access the device memories listed below.

- Link direct device [Designation-1]
- Special function module direct device [Designation-2]

ⓐ During data communications in the ASCII mode
Only the extension set data is designated and the following value is sequentially transmitted from the most significant digit.

Designated value	Objective device memory	Notes
"0000"	(No extension setting)	—
"J□"	Link direct device	Converts the network No. to be accessed to a 3-digit (hexadecimal) ASCII code and designates it at the □ part.
"U□"	Special function module direct device	Designated at the □ part using the higher 3 digits when the head I/O signal of the special function module to be accessed was converted to a 4-digit (hexadecimal) ASCII code.

ⓑ During data communications in the binary mode
The extension setting and direct memory designation data are designated and the following value is transmitted. (The extension set data is sequentially transmitted from the Low byte (L: bits 0 to 7).

Designated value		Objective device memory	Notes
Extension setting	Direct memory designation		
0000H	00H	(No extension setting)	—
□H	F9H	Link direct device	Designates (hexadecimal) the network No. to be accessed in the □ part.
□H	F8H	Special function module direct device	Designated in the □part using the higher 3 digits when the head I/O signal (hexadecimal) of the special function module to be accessed was expressed by 4 digits.

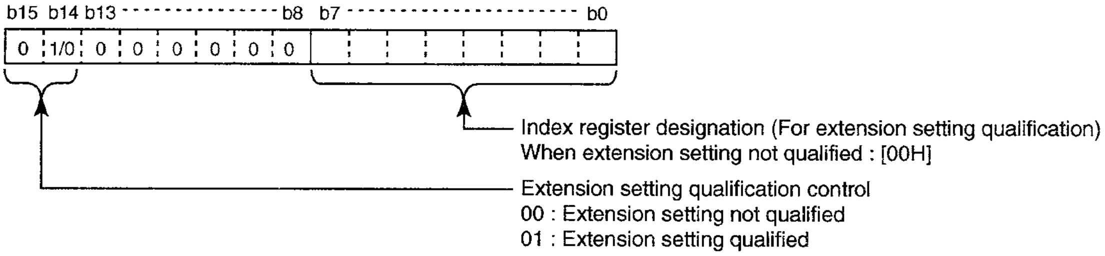
③ Extension setting qualification ([Designation-3] used)

This data assumes that the value designated by extension setting is the network No./ I/O signal offset and uses an index register to designate an arbitrary network No./I/O signal module.

ⓐ During data communications in the ASCII mode
The following value is sequentially transmitted from the most significant digit.

Designated value	Contents	Notes
"000"	(No extension setting qualification)	—
"Z□"	Index register for extension setting qualification	Designated in the □ part by converting the No. of the indexregister to be used to a 2-digit (hexadecimal) ASCII code.

ⓑ During data communications in the binary mode, the following value is sequentially transmitted from the Low byte (L: bits 0 to 7).



Index register designation (For extension setting qualification)
When extension setting not qualified : [00H]

Extension setting qualification control
00 : Extension setting not qualified
01 : Extension setting qualified

ⓒ Index registers (Z0 to Z15) can be used for extension setting qualification.

ⓓ When the I/O signals are stored to an index register forextension setting qualification, they are designated the following subtraction value.

(Value of higher 3 digits when head I/O signal of module to be accessed was expressed by 4 digits) — (extension setting designated value) = (Value stored to index register for extension qualification)

④ Device qualification and indirect designation

(Device qualification.....[Designation-4] used)
This data assumes that the value designated by head device (ordevice) is the device No. offset value and uses an index registerto designate an arbitrary device No. of the same device.

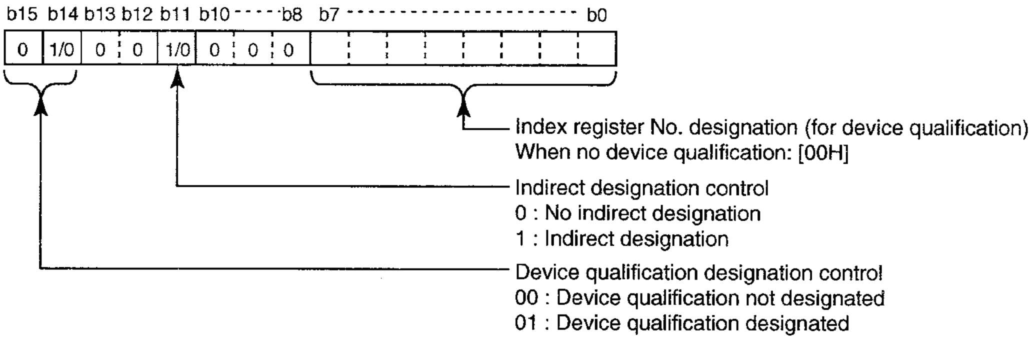
(Indirect designation......[Designation-5] used)
This data makes the value stored in the device memory designated by head device (or device) and the following device memory the address of the device memory to be accessed by the externaldevice.

For access to a word device, indirect designation is possible.

ⓐ During data communications in the ASCII mode
Only the device qualification data is designated and the following value is sequentially transmitted from the most significant digit.

Designated value	Contents	Notes
"000"	(No device qualification)	—
"Z□"	Index register for device qualification	Designated in the □ part by converting the No. of the index register to be used to a 2-digit (hexadecimal) ASCII code.

ⓑ During data communications in the binary mode
The device qualification and indirect designation data are designated and the following value is sequentially transmitted from the Low byte (L: bits 0 to 7).



ⓒ Index registers (Z0 to Z15) can be used for extension setting qualification.

2 Extension designation device memories and designation examples

(a) Extension designation device memories

The following device memories of a station equipped with a QC24(N) and QnACPU stations over a MELSECNET/10 can be extended.

① QnACPU device memory (See Section 6.2.1 3.)

② Network module link direct device and special function module special direct link device (See the table below and Appendix 4.)

Clas	Device	Type of device		Extension setting		Device code		Device No. range	Expression		Notes
		Bit	Word	ASCII mode	Binary mode	ASCII mode	Binary mode		Decimal	Hexa-decimal	
Link Direct Device	Link input	○		J□	F9H	X*	9CH	000000 to 001FFF		○	Network No. is designated in the extension setting □ part.
	Link output	○				Y*	9DH	000000 to 001FFF		○	
	Link relay	○				B*	A0H	000000 to 001FFF		○	
	Link special relay	○				SB	A1H	000000 to 0001FF		○	
	Link register		○			W*	B4H	000000 to 001FFF		○	
	Link special register		○			S*	85H	000000 to 0001FF		○	
Special Direct Device	Buffer register (buffer memory)		○	U□	F8H	G*	ABH	000000 to 016383	○		The I/O signals of the objective module are designated in the extension setting □ part.

1 "" of the device code designation and "00...0" of the headdevice (or device) designation can be designated using blanks (code: 20H) as described in Section 6.2.1 2 (c) ② and ③.

(b) Device memory extension designation example

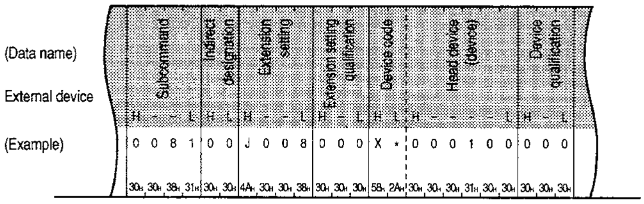
The following is a designation example when device memory is extended. (When subcommand does not designate a monitoring condition.)

[Designation-1]

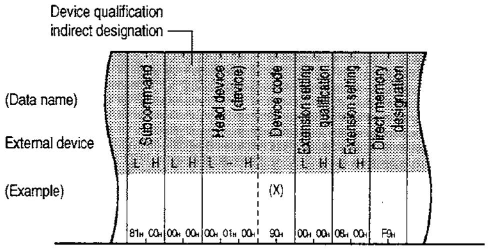
ⓐ When accessing the following devices

- Objective module : Network No. 8 (008H) network module
- Device No. : X100....Access in bit units

(ASCII mode designation method)



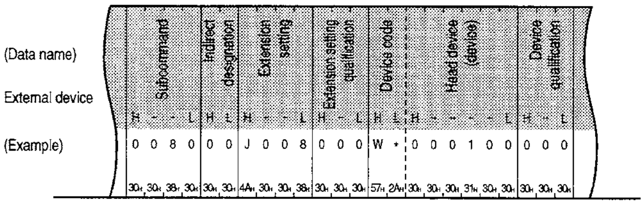
(Binary mode designation method)



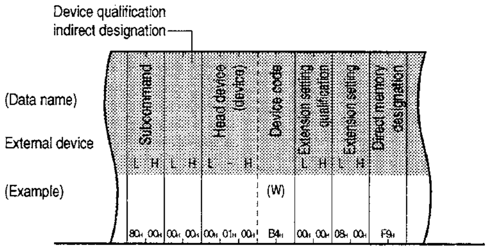
ⓑ When accessing the following devices

- Objective module : Network No. 8 (008H) network module
- Device No. : W100....Access in word units

(ASCII mode designation method)



(Binary mode designation method)

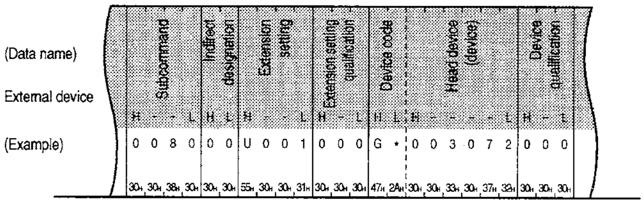


[Designation-2]

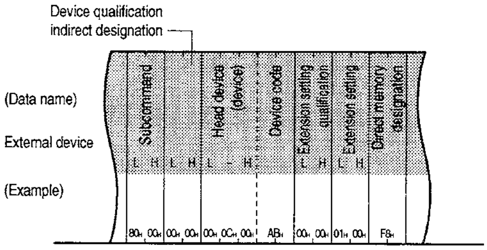
ⓐ When accessing the following buffer memories

- Objective special function module : Head I/O signal No. 010H special function module
- Head address : 3072(C00H)

(ASCII mode designation method)



(Binary mode designation method)

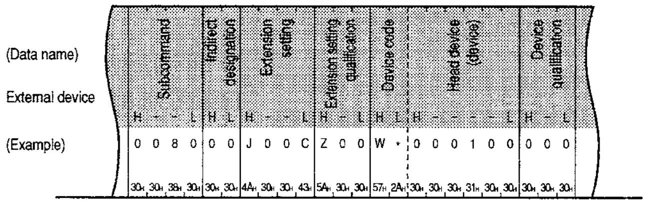


[Designation-3]

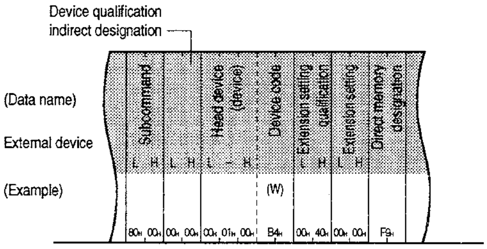
ⓐ When accessing the following device memories

- Objective module : Network No. 12(0CH) +Z0 network module
- Head address : W100

(ASCII mode designation method)



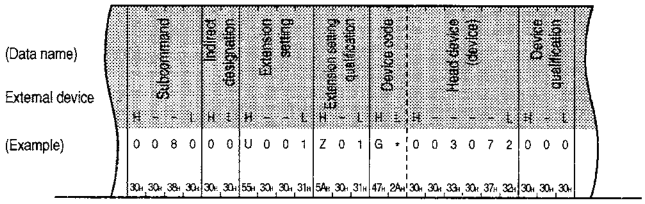
(Binary mode designation method)



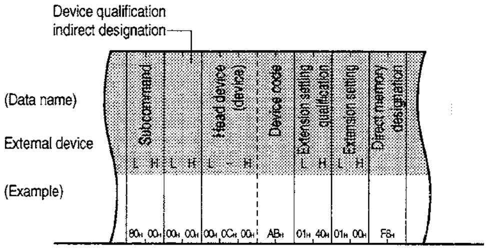
ⓑ When accessing the following buffer memories

- Objective special function module : Special function module whose head I/O signal is indicated by 010H+Z1
- Head address : 3072(C00H)

(ASCII mode designation method)



(Binary mode designation method)

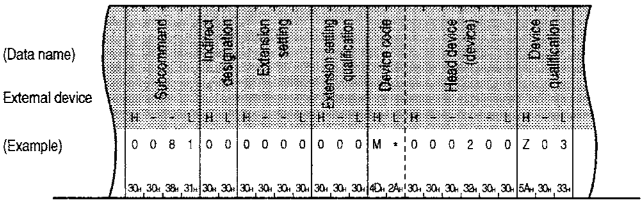


[Designation-4]

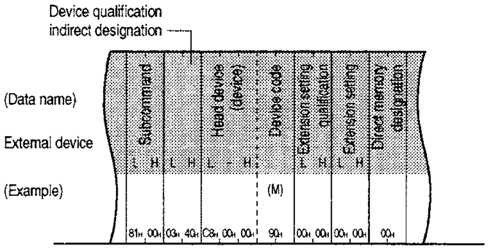
ⓐ When accessing the following device memories

- Device No. : Internal relay (M) designated using M200+Z3....Access in bit units

(ASCII mode designation method)



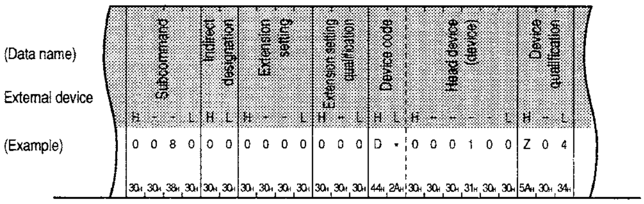
(Binary mode designation method)



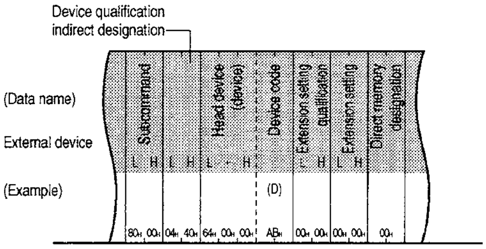
ⓑ When accessing the following device memories

- Device No. : Data register (D) designated using D100+Z4....Access in word units

(ASCII mode designation method)



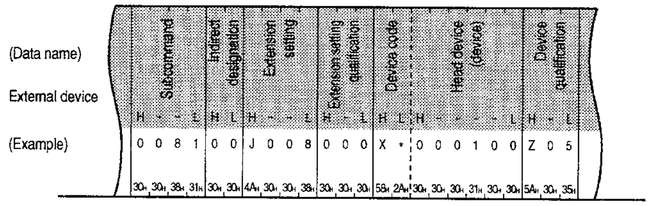
(Binary mode designation method)



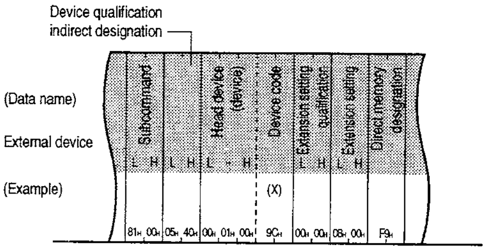
ⓒ When accessing the following device memories

- Object module : Network No. 8(008H) network module
- Device No. : Link input (X) indicated using X100+Z5....Access in bit units

(ASCII mode designation method)



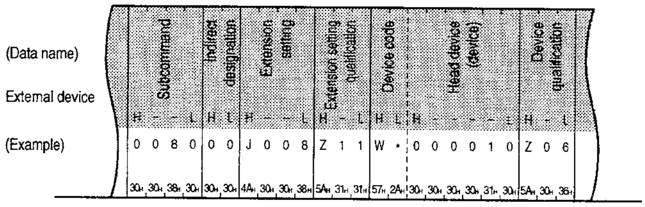
(Binary mode designation method)



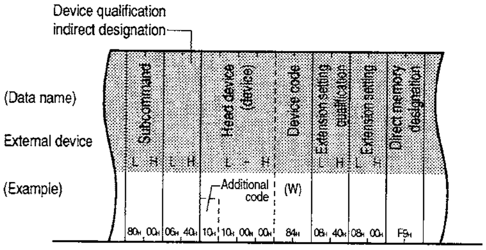
ⓓ When accessing the following device memories

- Object module : Network module whose network No. is indicated using 8(008H)+Z11
- Device No. : Link register (W) indicated using W10+Z6....Access in word units

(ASCII mode designation method)



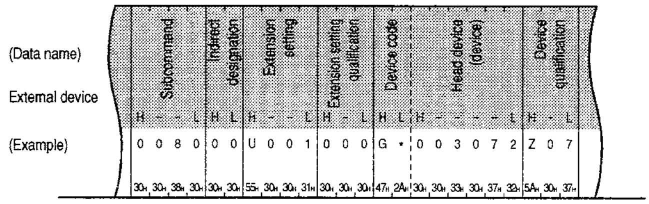
(Binary mode designation method)



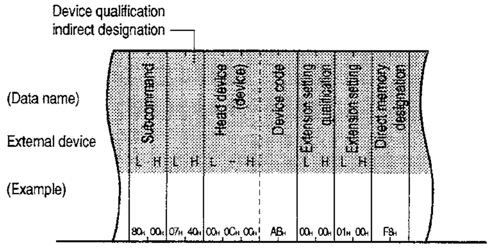
ⓔ When accessing the following buffer memories

- Objective special function module : Head I/O signal 010H special function module
- Head address : Address indicated using 3072(C00H)+Z7

(ASCII mode designation method)



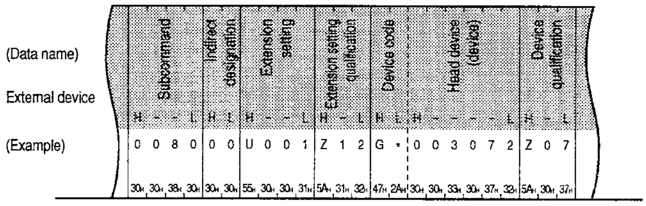
(Binary mode designation method)



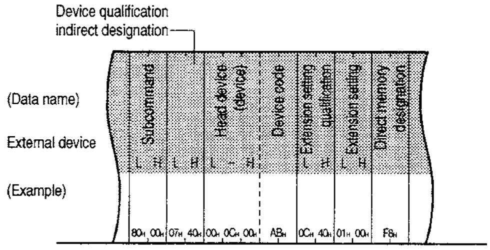
ⓕ When accessing the following buffer memories

- Objective special function module : Head I/O signal 010H+Z12 special function module
- Head address : Address indicated using 3072(C00H)+Z7

(ASCII mode designation method)



(Binary mode designation method)

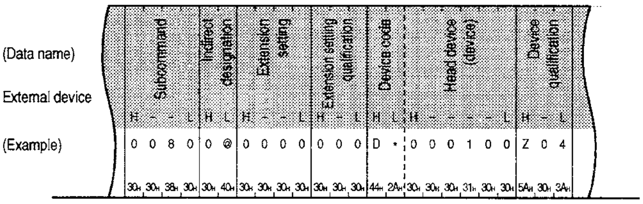


[Designation-5]

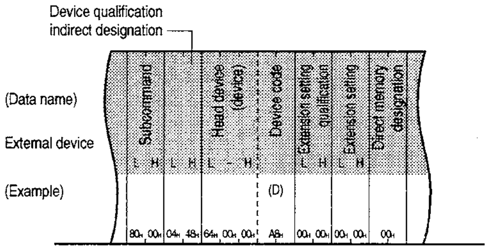
When accessing the following device memories

- Device No. : Device memory of address stored in the data register (D) indicated using D100+Z4....Access in word units

(ASCII mode designation method)



(Binary mode designation method)



3 Device memory extension designation restrictions

The following describes the device memory extension designation restrictions.

(a) Device memory extension designation commands

The following describes the device memory extension designation contents for each QnA (extension) frame device memory read and write command.

Function		Access device	Command	Device memory extension designation item					Designation expression				
				Indirect designation	Extension setting	Extension setting qualification	device qualification	Direct memory designation	Designation-1	Designation-2	Designation-3	Designation-4	Designation-5
Batch read Batch write	Bit units	Bit	0401 1401	×	○	×	×	○	○	○	×	×	×
	Word units	Bit											
		Word											
Random read	Word units	Bit	0403	×	○	○	○	○	○	○	○	○	○
		Word		○									
Test [Random write]	Bit units	Bit	1402	×	○	○	○	○	○	○	○	○	○
	Word units	Bit		×									
		Word		○									
Monitor data registration	Word units	Bit	0801	×	○	○	○	○	○	○	○	○	○
		Word		○									
Monitor	Word units	—	0802	×	×	×	×	×	—	—	—	—	—
Multiple block batch read Multiple block batch write	Word units	Bit	0406 1406	×	○	×	×	○	○	○	×	×	×
		Word											

Bit: Bit device
Word: Word device

○: Can be designated ×: Cannot be designated

(b) Device memory extension designation control mixed designation

When using the following functions, two or more device names can be designated in a command message.
In this case, when device memory is extended, extension-designate all the devices designated in the command message.
Device memory [Extension designated] and [Not extension designated] cannot be mixed.

- Random read function .... (Command: 0403)
- Test (random write) function .... (Command: 1402)
- Monitor data registration function .... (Command: 0801)
- Multipul block batch read/write function .... (Command: 0406, 1406)

(c) Access to special function module

① The read/write of the special function module buffer memory using the device memory extension designation can be conducted for the special function modules installed in the following stations using the above QnA frame and QnA extension frame commands.

- The QnACPU + QC24(N) station connected to the external equipment and the QnACPU + QC24(N) station multi-drop connected to that QC24(N).
- QnACPU station in the MELSECNET/10 and the stations corresponding to the QnA multi-drop connected to that QC24(N) via the QnACPU station.

② For information regarding reading to and writing from special function modules installed in stations other than those listed above refer to Section 6.3.

6.3 Buffer Memory Read/Write

This section explains the functions for reading data from and writing data to external equipment for the buffer memory of the Special Function Module installed in the PLC station (Remote station) in the data link system or network system not installed in the QC24(N) or in the QnA PLC station (Local station) installed in the QC24(N). The PLC stations in which reading/writing of the special function module buffer memory are possible, the functions used, and the commands are as follows.

The applicable stations and modules for access 1 to access 6 and the applicable functions and commands for the reading/writing method are shown in the table below.

	Read applicable read/write				Read/write method			
	No.	Applicable station		Applicable Module	QnA extension designation (Section 6.2.11)	Command used by QnA frame and QnA extension frame		Commands "TR," and "TW" used by the A compatible frame
						"0601", "1601"	"0613", "1613"	
Access 1 (Local station)	①	External equipment connection station	QnACPU station	QC24(N)	×	×	○	×
			Remote station					
Access 2 (Local station)	②	External equipment connection station	QnACPU station	Special Function Module (Except QC24(N))	○	○	×	×
	③		QnA supporting remote station		×	○	×	×
Access 3 (Remote station)	④	Station in the MELSECNET/10	QnACPU station	Special Function Module (Including QC24(N))	○	○	×	×
	⑤		QnA supporting remote station		×	○	×	×
Access 4 (Remote station)	⑥		PLC CPU station other than the QnACPU		×	×	×	×
	⑦		AnU supporting remote station		×	×	×	×
Access 5 (Remote station)	⑧	Station in the MELSECNET (Ⅱ), /B	QnACPU station		×	×	×	×
Access 6 (Remote station)	⑨		PLC CPU station other than the QnACPU		×	×	×	Local station : ○ Master station : ×
	⑩		Remote station		×	×	×	○

○: Read/write possible ×: Read/write not possible

(1) Stations and modules that correspond to the access 1 to access 6 shown in the table

- Access 1 (Local station)
  ① QC24(N) connected to the external equipment and the QC24(N) multi-drop connected to that QC24(N).
- Access 2 (Local station)
  ② QC24(N) station connected to the external equipment and the Special Function Module that is installed in the QC24(N) station that is multi-drop connected to that QC24(N).
  ③ Special Function Module installed in the MELSECNET/10 remote station that is installed in the QC24(N) connected to the external equipment.
- Access 3 (Remote station)
  ④ Special Function Module installed in the QnACPU station in the MELSECNET/10.
  ⑤ Special Function Module installed in the remote station for the QnA in the MELSECNET/10.
- Access 4 (Remote station)
  ⑥ Special Function Module installed in the station other than the QnACPU in the MELSECNET/10.
  ⑦ Special Function Module installed in the remote station for the AnU in the MELSECNET/10.
- Access 5 (Remote station)
  ⑧ Special Function Module installed in the QnACPU station in the MELSECNET (Ⅱ) or MELSECNET/B.
- Access 6 (Remote station)
  ⑨ Special Function Module installed in a station other than the QnACPU in the MELSECNET (Ⅱ) or MELSECNET/B.
  ⑩ Special Function Module installed in the remote station for the AnA/AnU in the MELSECNET (Ⅱ) or MELSECNET/B.

(2) Functions and commands for the read/write method shown in the table

- QnA extension designation: Conduct read/write using the device memory extension designation shown in Section 6.2.11.
- QnA frame and QnA extension frame commands
  0613, 1613 : Read/write the commands 0613 and 1613 for the QnA frame and QnA extension frame shown in Section 6.3.1.
  0601, 1601 : Read/write the 0601 and 1601 commands for the QnA frame shown in Section 6.3.2.
- A compatible frame command
  TR, TW : Read/write the TR and TW commands for the A compatible frame shown in Section 5.4.2.
  For details regarding commands see the Computer Link/Multi-Drop Link Module User's Manual (Computer Link and Printer Function Edition).

POINT

The special function module buffer memory, also including QC24(N), has read/write possible areas, read only areas, write only areas, and OS user usage not possible areas in each module. Execute this function following the explanations in the manuals for each module. Conducting an incorrect read or write will cause an error to occur in the PLC CPU and the special function modules.

6.3.1 Serial communication module buffer memory read/write

This function is used to read from, and write to, the buffer memory of a QC24(N) (including multidrop connection) connected to anexternal device.

Since communications bet ween external device and QC24(N) by this function is performed without waiting for PLC CPU END processing when the external device issues a read or write request, transmission time T1 described in Section 5.7 becomes "0".

The PLC CPU uses the FROM or TO instruction to write or read the buffer memory data (data exchanged with external device).

This section uses examples to describe the control procedure of this function.

6.3.1.1 Commands and buffer memory

This section describes the commands used and the buffer memory address designated by the control procedure when reading from, and writing to, the QC24(N) buffer memory.

1 Commands

Function	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication (See Section 6.3.)	PLC CPU state			Reference section
				During STOP	During RUN		
					Write enable set	Write disable set	
Batch read	0 6 1 3 (0 0 0 0)	Reads from buffer memory.	480 words (960 bytes)	○	○	○	6.3.1.2
Batch write	1 6 1 3 (0 0 0 0)	Writes to buffer memory.		○	○	○	6.3.1.3

○ in the PLC CPU state column in the table above indicatesthat execution is possible.

2 Buffer memory and access units

The buffer address designated by this function uses the user area of the buffer memory table shown in Section 3.5.

One address is made up of 1 word (16 bits).

This function reads and writes data in word units without regard to the word/byte designation (designated by buffer memory address96H/136H).

POINTS

(1) Buffer memory addresses 0H to 3FFH and 1B00H to 1FFFH are the special applications area. The QC24(N) will not operate correctly if operations other than those described in this manual are performed.

(2) When using the following functions at the same time, be sure that allocation of the buffer memory user area storing the send data and receive data handled by the function used is not duplicated.
If an area is duplicated, the data will be rewritten and communications will not be performed correctly.
- Dedicated protocol buffer memory read/write functions (Commands: 0613, 1613)
- Dedicated protocol on-demand function
- Non precedure protocol transmit/receive functions
- Bidirectional protocol transmit/receive functions

3 Contents of character area

The following describes the contents of the character area when an external device reads and writes the QC24(N) buffer memory.

(a) Head address

This data designates the address of the head area of the data read (or write) range.

① Data communications in ASCII mode

Head area addresses 0H to 1FFFH (0 to 8191) are converted to 8-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

(Example) When head area address is 1E1H....
Converted to"000001E1" and sequentially transmitted from the first "0".

② Data communications in binary mode

A 4-bit value indicating head area addresses 0H to 1FFFH (0 to 8191) is sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) When head area address is 1E1H....
The value 000001E1H is sequentially transmitted from E1H.

(b) Word length

This data designates the number of addresses (number of words) ofthe data read (or write) range.

① Data communications in ASCII mode

Number of addresses 1H to 1E0H (1 to 480) is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from themost significant digit ("0").

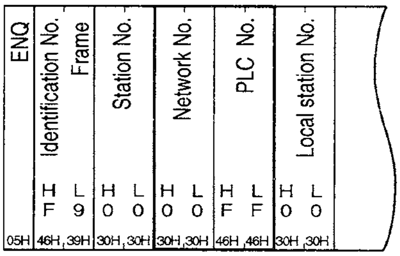
② Data communications in binary mode

A 2-byte value indicating the number of addresses 1H to 1E0H (1 to 480) is sequentially transmitted from the Low byte (L: bits 0 to 7).

Note

Designate the following data for the local stations for the data designation item network No. and PLC No. in the text.
Network No. : 00H PLC No. : FFH

(For QnA frame format 1)



6.3.1.2 Reading buffer memory (command: 0613)

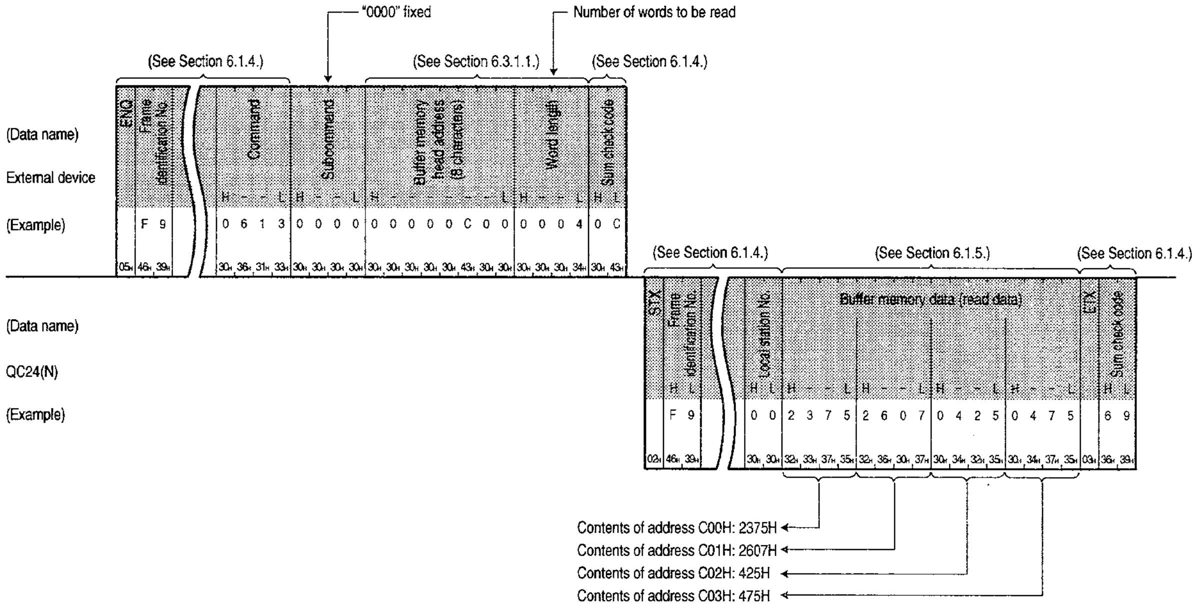
The following uses an example to describe the QC24(N) buffer memory batch read control procedure.

[Control Procedure]

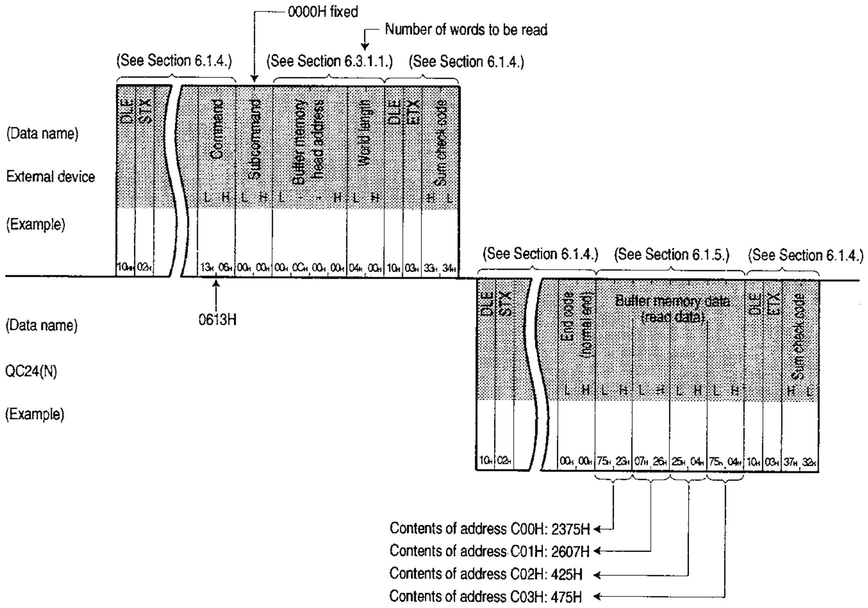
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to read 4 words from the contents of buffer memory addresses C00H to C03H (3072 to 3075).



2 When using binary mode format 5 to read 4 words from the contents of buffer memory addresses C00H to C03H (3072 to 3075).



POINT

Designate the head address and word length within the following range.

- Head address .... 0H ≤ head address ≤ 1FFFH(8191)
- Word length .... 1H ≤ word length ≤ 1E0H(480)
- Access range............. (Head address + word length − 1) ≤ 1FFFH

6.3.1.3 Writing to buffer memory (command: 1613)

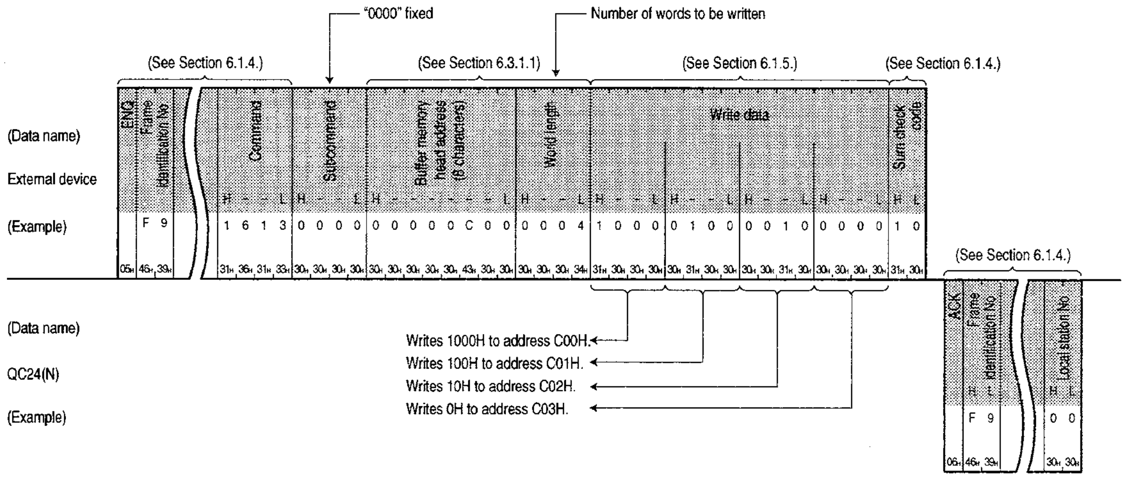
The following uses examples to describe the QC24(N) buffer memory batch write control procedure.

[Control Procedure]

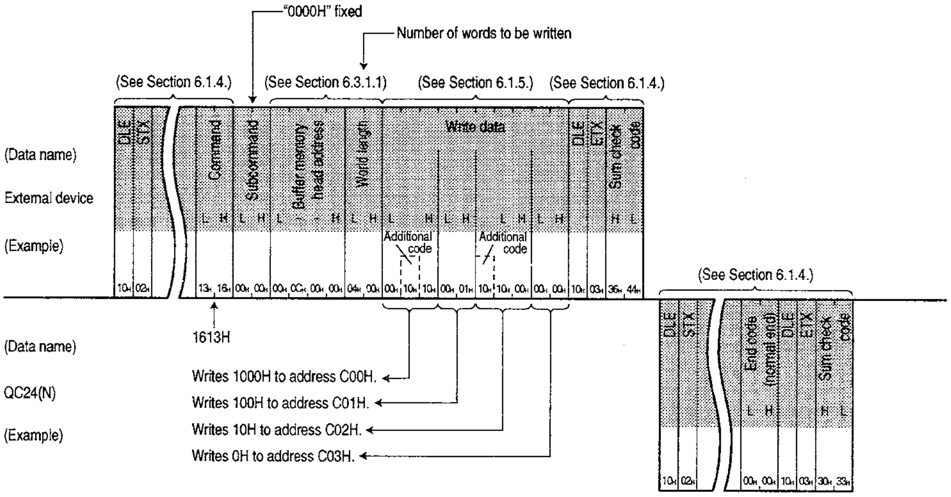
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to write 4 words of data to buffer memory addresses C00H to C03H (3072 to 3075)**



2 When using binary mode format 5 to write 4 words of data to buffer memory addresses C00H to C03H (3072 to 3075)



POINT

Designate the head address and word length within the following range.

- Head address .... 0H ≤ head address ≤ 1FFFH(8191)
- Word length .... 1H ≤ word length ≤ 1E0H(480)
- Access range............. (Head address + word length – 1) ≤ 1FFFH

6.3.2 Special functions module buffer memory read/write

This section explains the control procedure and uses examples for reading and writing data to the buffer memory special function module (Including QC24(N)).

This command accesses the special function module buffer memory using byte units.

6.3.2.1 Commands and buffer memory

This section explains about the buffer memory addresses, etc., set for the commands and control procedure when reading from or writing to the special function module buffer memory.

1 Commands

Function	Command (subcommand) *ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication (See Section 6.3.)	PLC CPU state			Reference section
				During STOP	During RUN		
					Write enable set	Write disable set	
Batch read	0 6 0 1 (0 0 0 0)	Reads from buffer memory.	960 bytes (480 words)	○	○	○	6.3.2.3
Batch write	1 6 0 1 (0 0 0 0)	Writes to buffer memory.		○	○	×	6.3.2.4

In the PLC CPU status column in the above table the "○" means execute possible and the "×" means execute not possible.

2 Buffer memory and access units

The buffer memory addresses designated using this function are designated using the method explained in Section 6.3.2.2. One address is configure of one word (16 bits), but with this function the byte unit can be read/written regardless of the word/byte setting (Set by a buffer memory address 96H/136H).

3 Character section contents

This section explains the character portion contents when the external equipment reads from or writes to the special function module buffer memory.

(a) Head address

This data is used to designate the head area address of the data read range (or write range).

The head address designation method is as shown in ③. The access possible modules and buffer memory head addresses are shown in Section 6.3.2.2.

① When communicating in the ASCII mode
The head area address is converted to ASCII code 8 digits (hexadecimal), used, and transmitted from the first digit ("0").
(Example) When the head area address is 1E1H....
Becomes "000001E1" and is transmitted in the order from "0."

② When communicating data in the binary mode

The head area address shown in the 4-byte number is used and is transmitted in order from the low byte (L: Bit 0 to 7).

(Example) When the head area address is 1E1H....

Becomes 000001E1H and is transmitted in order from E1H.

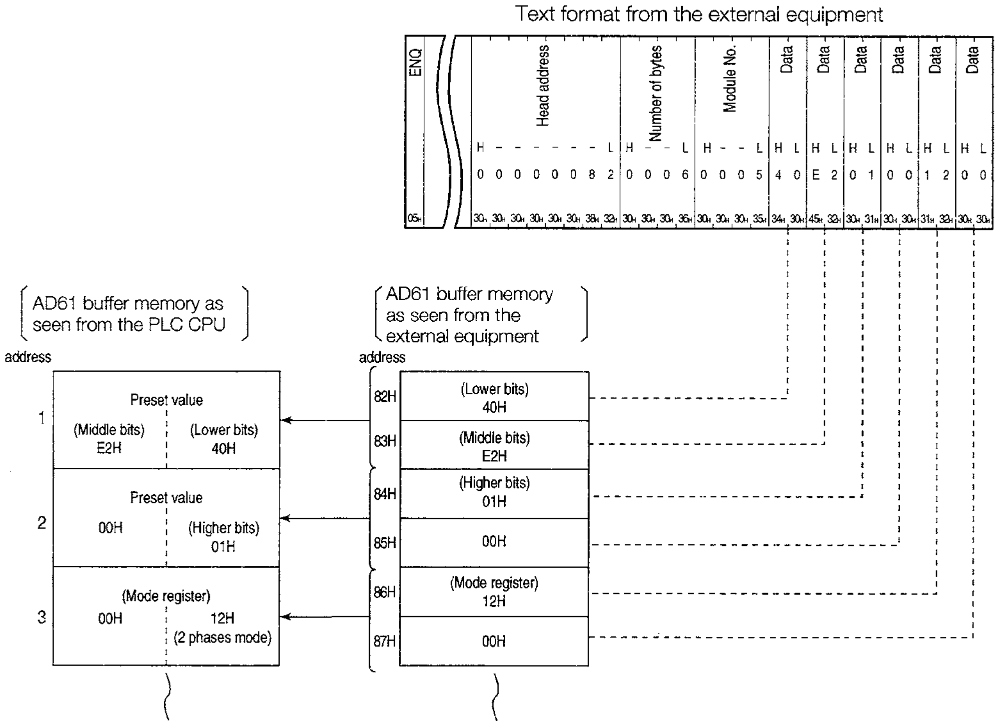
③ This shows the header address designation method when reading from or writing to the special function module buffer memory. The special function module buffer memory is configured of one address 16 bits (1 word) and reading/writing from the PLC CPU and the special function module is conducted using FROM/TO instructions. When the commands shown in Section 6.3.2 are used to read from or write to the Special Function Module buffer memory via the QC24(N) from the external equipment, it is conducted with one address equaling 8 bits (1 byte). The address designated by the external equipment (hexadecimal) is designated by the address which conducts the following conversion from the FROM /TO instruction address.

Head address (hexadecimal) = [(FROM/TO instruction address × 2)] becomes the hexadecimal number + buffer memory head address

This section explains the data format when the special function module buffer memory is accessed from the external equipment using AD61 as an example.

(Example) When model AD61 high-speed counter module FROM/TO instruction address 1 (CH.1 preset value) is designated

Head address	=	FROM/TO instruction address 1 × 2	+	buffer memory head address
82H	=	2H	+	80H



POINT

The special function module buffer memory head addresses (80H for the above AD61) when "head address" is designated in the text is shown in Section 6.3.2.2.

(b) Number of bytes

An even number of bytes is designated for the data used to designate the data read range (or write range) number of addresses × 2 (number of bytes).

① When data is communicated in the ASCII mode

The number of addresses × 2 (2 to 960) is converted to 4 digit ASCII code (hexadecimal), used, and transmitted from the first digit ("0").

② When communicating in the binary mode

The 2-byte number that shows the number of addresses × 2 (2 to 960) is used and transmitted from the low byte (L: Bit 0 to 7).

(c) Module No.

This data is used to designate the special function module that will read, or write, the data. The module No. designation method is as shown in ③. The module No. when the access possible module and buffer memory head address are installed in slot 0 is shown in Section 6.3.2.2.

① When communicating in the ASCII mode

When the applicable special function module I/O signal is expressed in 4 digits, the first 3 digits are converted to ASCII code 4 digits (hexadecimal), used, and transmitted from the first digit.

(Example) When the special function module I/O signal is 0080H to 009FH....

The head I/O signal becomes "0008" and is transmitted in order from "0."

② When communicating data in binary mode

When the applicable special function module I/O is expressed in 4 digits, the first 3 digits are used as a 2-byte number and transmitted in order from the low byte (L: Bit 0 to 7) and high byte (H: Bit 8 to 15).

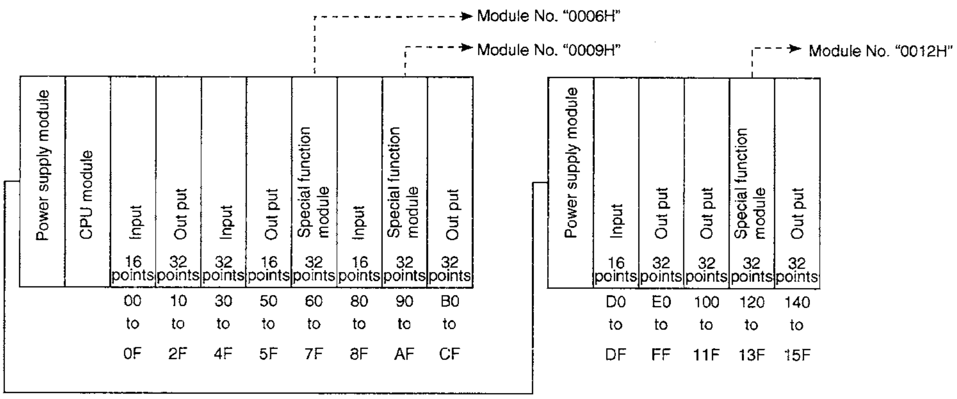
(Example) When the special function module I/O signal is 0080H to 009FH....

The head I/O No. becomes 0008H and is transmitted in order from 08H, 00H.

③ This shows the module No. designation method when reading from or writing to the special function module buffer memory.

- The module No. is designated by the head I/O signal allocated to the special function module corresponding to the installed station.
- For the special function module occupying slot 2 this is designated by the special function module slot's head I/O signal.

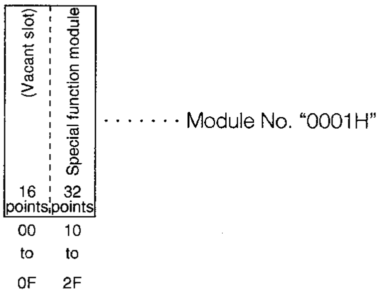
(When the special function module occupies slot 1)



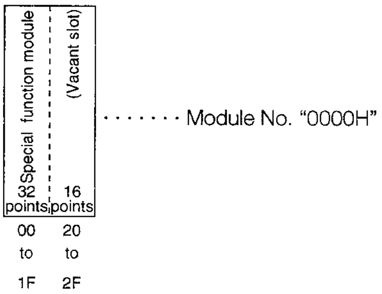
(When the special function module occupies slot 2)

For the special function module occupying slot 2 the number of points occupied by each slot is determined for each module. The Module No. is the first 3 digits from the 4 digits that express the head address of the slot allocated as a special function module. For information regarding the allocation for each module slot see the corresponding special function module users manual.

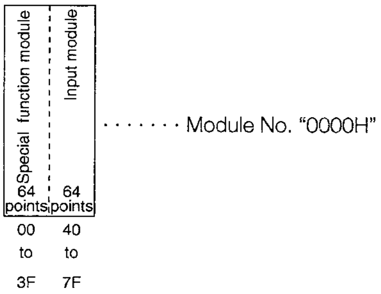
ⓐ For modules allocated with the front-half slots being vacant slots. (AD72, A84AD, etc.)



ⓑ For modules allocated with the last-half slots as empty slots. (A61LS, etc.)



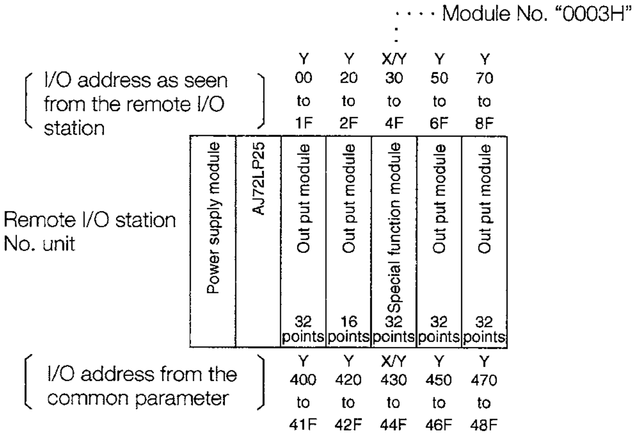
ⓒ For modules mixed as special function module allocated and I/O allocated. (A81CPU, etc.)



(For a network system remote I/O station special function modules)

For the MELSECNET/10 remote I/O station special function module's module Nos. the first 3 digits of the 4 digits that express the head address of all the following "I/O addresses as seen from the remote I/O station."

Designate to the "I/O address as seen from the remote I/O station" regardless of the common parameter contents set by the MELSECNET/10 remote I/O network master station.



The model number of the special function module occupying slot 2 is designated using the method shown on the previous page (for special function modules occupying slot 2).

(d) Reading data and writing data

The read data and write data for the special function module is the same as the number of bytes data shown in (b) above (maximum 960 bytes).

① When communicating using ASCII mode

Each data code is converted into ASCII code 2 digits (hexadecimal), used, and transmitted from the first digit.

(Example) When the read data/written data is 12H....

The read data/written data becomes "12" and is transmitted from "1."

② When communicating using binary mode

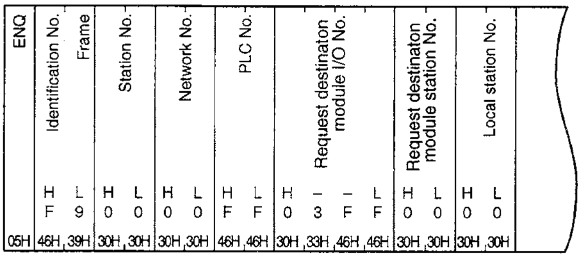
The data code is transmitted from the header.

POINT

When using this QnA frame and QnA extension frame commands 0601 and 1601, designate the following data in the data designation item request destination module I/O No. and request destination module station No. in the text data when communicating using the QnA extension frame.

Request destination module I/O No.: 03FFH Request destination module station No.: 00H

(For QnA extension frame format 1)



6.3.2.2 Access possible special function modules

Following is shown the special function modules for which reading/writing to the buffer memory using the dedicated protocol QnA frame and QnA extension frame commands 0601 and 1601 and the header address module No. designated in the text.

Notes

The buffer memory header addresses and module No. when installed in slot 0 shown in the table are used to designate the head address and module No. in the text.

1 **Access possible special function module model names**

Special function module model name	Buffer memory header address (Hexadecimal)	Module No. when installed in slot 0
Model AD61 (S1) High-Speed Counter Module	80H	0000H
Model A616AD Analog - Digital Conversion Module	10H	
Model A616DAI/DAV Digital - Analog Conversion Module	10H	
Model A616TD Temperature - Digital Conversion Module	10H	
Model A62DA (S1) Digital - Analog Conversion Module	10H	
Model A68AD (S2) Analog - Digital Conversion Module	80H	
Model A68ADN Analog - Digital Conversion Module	80H	
Model A68DAV/DAI Digital - Analog Conversion Module	10H	
Model A68RD3/4 Temperature - Digital Conversion Module	10H	
Model A84AD Analog - Digital Conversion Module	10H	0001H
Model A81CPU PID Control Module	200H	0000H
Model A61LS Position Detection Module	80H	
Model A62LS (S5) Position Detection Module	80H	0001H
Model AJ71PT32 (S3), AJ71T32 - S3 MELSECNET/MINI Master Module	20H	0000H
Model AJ61BT11 CC-Link System Master · Local Module	2000H (*2)	
Model AJ71C22 (S1) Multi Drop Link Module	1000H	
Model AJ71C24 (S3, S6, S8) Computer Link Module	1000H	
Model AJ71UC24 Computer Link Module	400H	
Model AD51 (S3) Intelligent Communication Module	800H	0001H
Model AD51H (S3) Intelligent Communication Module	800H	
Model AJ71C21 (S1) Terminal Interface Module	400H	0000H
Model AJ71B62 B/NET Interface Module	20H	
Model AJ71P41 SUMINET Interface Module	400H	
Model AJ71E71 (S3) Ethernet Interface Module	400H	
Model AD51FD (S3) External Problem Diagnostic Module	280H	0001H
Model AD57G (S3) Graphic Controller Module	280H	
Model AS25VS Vision Sensor Module	100H	0001H
Model AS50VS Vision Sensor Module	100H	
Model AS50VS-GN Vision Sensor Module	80H	
Model AD59 (S1) Memory Card Interface Module	1800H (*1)	0000H
Model AJ71ID1 (2)-R4 ID Interface Module	280H	
Model AD70 (D) (S2) Positioning Module	80H	0000H
Model AD71 (S1/S2/S7) Positioning Module	200H	0001H
Model AD72 Positioning Module	200H	

Special function module model name	Buffer memory header address (Hexadecimal)	Module No. when installed in slot 0
Model AD75P1/ P2/ P3 (S3), AD75M1/M2/M3 Positioning Module	800H	0000H
Model AJ61QBT11 CC-Link System Master · Local Module	2000H	
Model AJ71QC24(N) (R2, R4) Serial Communication Module	4000H	
Model AJ71QE71 (B5) Ethernet Interface Module	4000H	
Model A1SD61, A1SD62 (E/D (S1)) High-Speed Counter Module	10H	
Model A1S62DA Digital-Analog Conversion Module	10H	
Model A1S62RD3/4 Temperature-Digital Conversion Module	10H	
Model A1S64AD Analog-Digital Conversion Module	10H	
Model A1SJ71 (U) C24-R2 Computer Link Module	400H	
Model A1SJ71 (U) C24-PRF Computer Link Module	400H	
Model A1SJ71 (U) C24-R4 Computer Link Module	400H	
Model A1SJ71E71-B2/B5 (S3) Ethernet Interface Module	400H	
Model A1SD51S Intelligent Communication Module	800H	
Model A1SJ71ID1(2)-R4 ID Interface Module	280H	
Model A1SD70 Single Axis Positioning Module	80H	
Model A1SD71-S2/S7 Positioning Module	200H	0001H
Model A1SD75P1/P2/P3 (S3), A1SD75M1/M2/M3 Positioning Module	800H	0000H
Model A1S63ADA Analog I/O Module	10H	
Model A1S64TCTT (BW)-S1 Temperature Adjustment Module	20H	
Model A1S64TCRT (BW)-S1 Temperature Adjustment Module	20H	
Model A1S62TCTT (BW)-S2 Temperature Adjustment Module	20H	
Model A1S62TCRT (BW)-S2 Temperature Adjustment Module	20H	
Model A1S68DAV/A1S68DAI Digital-Analog Conversion Module	20H	
Model A1S68AD Analog-Digital Conversion Module	20H	
Model A1S68TD Thermocouple Input Module	20H	
Model A1SJ71PT32-S3 MELSECNET/MINI Master Module	20H	
Model A1SJ61BT11 CC-Link System Master · Local Module	2000H (*2)	
Model A1SJ71QC24(N) (R2) Serial Communication Module	4000H	
Model A1SJ71QE71-B2/B5 Ethernet Interface Module	4000H	
Model A1SJ61QBT11 CC-Link System Master · Local Module	2000H	

*1 Changing the memory card bank using the I/O signal Y10, Y11 between the PLC CPU and the AD59 (S1) makes it possible to read/write from the memory card access memory area only.

*2 Changing the buffer memory bank using the I/O signal Y1C/Y1D between the PLC CPU and the AJ61BT11/A1SJ61BT11 makes it possible to read/write the buffer memory of the corresponding bank.

2 Example when the external equipment designates the special function module head address

The head address designated by the external equipment using the model AD61 High-Speed Counter Module is shown below.

Buffer memory contents	Head address		Address from FROM/TO instruction	
	Channel 1	Channel 2	CH1	CH2
Unused area (Prohibited to use)	80H	C0H	0	32
	81H	C1H		
Pre-set value write (Lower bits)	82H	C2H	1	33
Pre-set value write (Middle bits)	83H	C3H		
Pre-set value write (Higher bits)	84H	C4H	2	34
	85H	C5H		
Mode register	86H	C6H	3	35
	87H	C7H		
⋮				

6.3.2.3 Special function module buffer memory read (command: 0601)

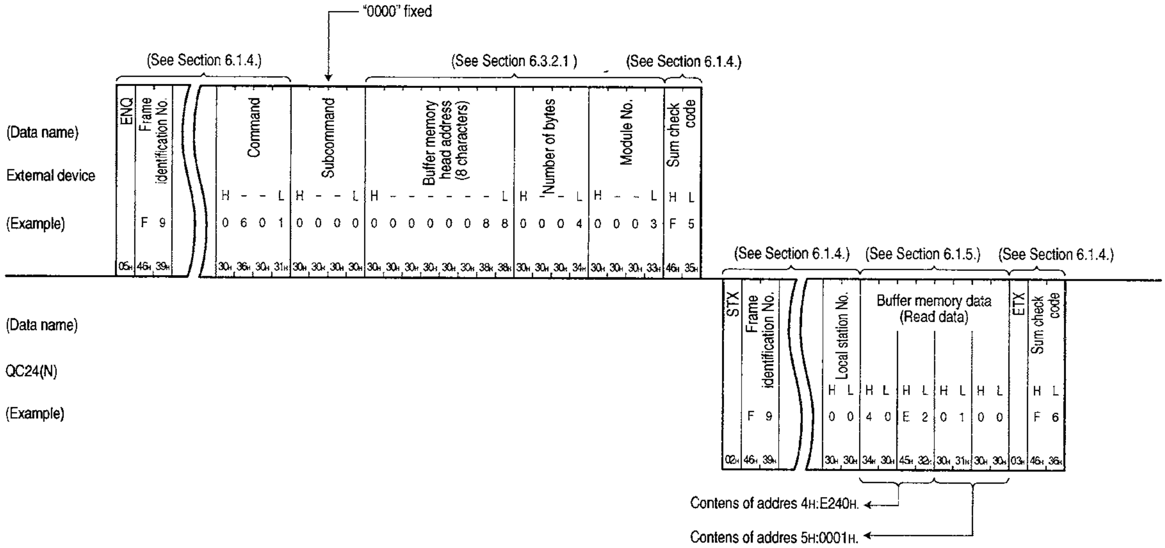
The following explains the special function module buffer memory read control procedure using an example.

[Control procedure]

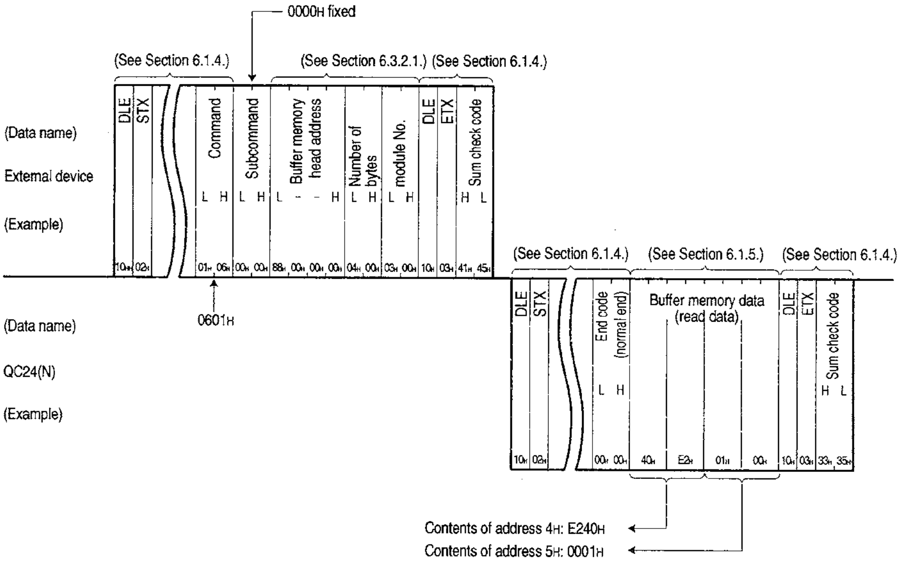
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When reading 4 bytes portion from 4H to 5H of the AD61 high-speed counter buffer memory address which I/O number is 30H to 4 FH(module No.:03H), by using ASCII mode format 1**



2 **When reading 4 bytes portion from 4H to 5H of the AD61 high-speed counter buffer memory address which I/O number is 30H to 4 FH(module No.:03H), by using binary mode format 5**



POINTS

(1) Designate the head address and number of bytes within the following ranges.
- Head address .... Applicable Special Function Module address range
- Number of bytes .... 2 (2H) ≤ number of bytes ≤ 960 (3C0H)

(2) Because the contents of one data varies between 2 and 3 bytes depending on the Special Function Module refer to the manual of each module when designating the number of bytes and the write data.

(3) When communicating using a QnA extension frame specify the data designation item Request Destination Module I/O No. in the text to [03FFH] and the Request Destination Module station No. in the text to [00H].

6.3.2.4 Special function module buffer memory write (command: 1601)

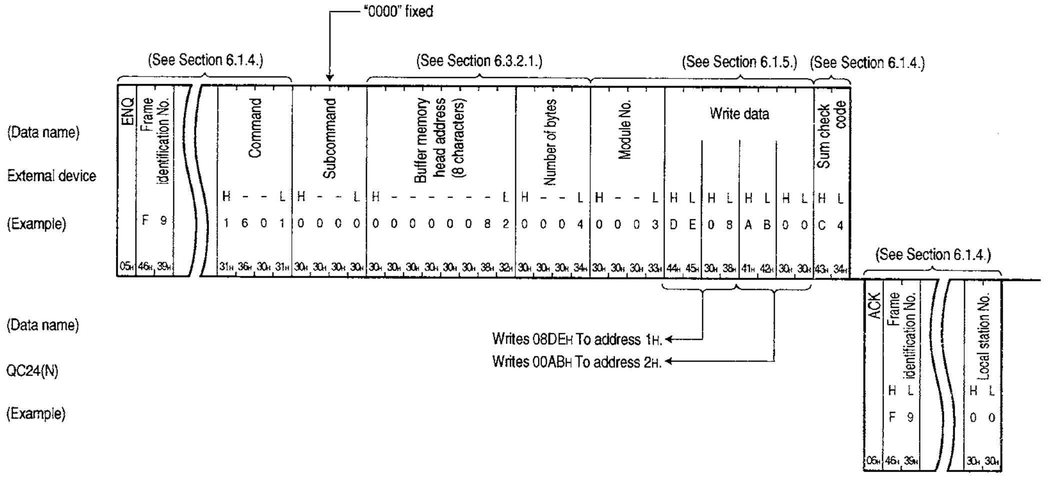
The following explains the Special Function Module buffer memory write control procedure using an example.

[Control procedure]

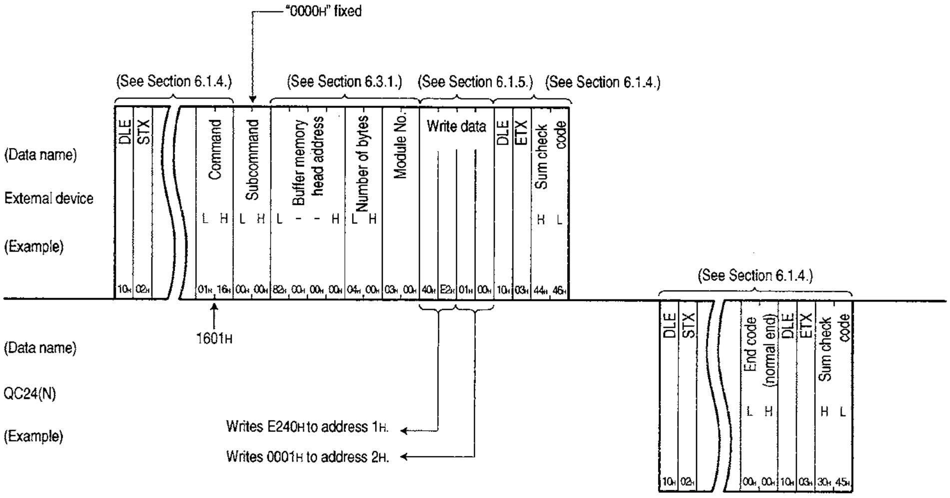
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When writing 4 bytes portion of data to 1H to 2H of the AD61 high-speed counter buffer memory address which I/O number is 30H to 4 FH(module No.:03H), by using ASCII mode format 1**



2 When writing 4 bytes portion of data to 1H to 2H of the AD61 high-speed counter buffer memory address which I/O number is 30H to 4 FH(module No.:03H), by using binary mode format 5



POINTS

(1) Designate the head address and number of bytes within the following ranges.
- Head address: .... Applicable Special Function Module address range
- Number of bytes: .... 2 (2H) ≤ number of bytes ≤ 960 (3C0H)

(2) Because the contents of one data varies between 2 and 3 bytes depending on the Special Function Module refer to the manual of each module when designating the number of bytes and the write data.

(3) When communicating using a QnA extension frame designate the data designation item Request Destination Module I/O No. in the text to [03FFH] and the Request Destination Module station No. in the text to [00H].

6.4 PLC CPU State Control

This function sets the QnACPU to the remote RUN/STOP/PAUSE/RESETstate, or clears the QnACPU device memory, from an external device.
The following uses examples to describe the control procedure of this function.

6.4.1 Commands, control contents, and character area contents

This section describes the commands, control contents, and the character area (data area in binary mode) in the control procedure when controlling the state of the PLC CPU.

1 Commands

— Function	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
Remote RUN	1001 (0000)	Requests remote RUN (operation execution).	(1 station)	(Un-available)	○	○	○	6.4.2
Remote STOP	1002 (0000)	Requests remote STOP (operation stop).						6.4.3
Remote PAUSE	1003 (0000)	Requests remote PAUSE (operation stop). (Output state is held)						6.4.4
Remote latch clear	1005 (0000)	Request remote clear (device memory clear) when the PLC CPU isin the STOP state.			○	×	×	6.4.5
Remote RESET	1006 (0000)	Request remote RESET (operation execution start) when the PCCPU is in the STOP state.			○	×	×	6.4.6

○ in the PLC CPU state column above indicates that execution is possible.

2 Control contents

(a) The following table shows the QnACPU state by state control from the external device and the state of the RUN/STOP key switch on the QnACPU panel.

		State of QnACPU panel key switch	
		RUN	STOP
Contents of request from external device	Remote RUN	RUN	STOP
	Remote STOP	STOP	STOP
	Remote PAUSE	PAUSE	STOP
	Remote latch clear	[Executable when the QnACPU is in the STOP (operation stopped) state regardless of the state of the key switch.]	
	Remote RESET		

POINTS

(1) When the QnACPU power is turned OFF→ON, or the QnACPU is reset, after remote RUN/STOP/PAUSE was executed from an external device, the remote data is cleared.

(2) When system-protect (system-protect switch SW5: ON) is applied to the QnACPU, its state cannot be controlled from an external device. The QC24(N) returns an NAK message in response to each request.

3 Contents of character area

The following describes the contents of the character area when an external device controls the state of the QnACPU.

(a) Mode

This data forcefully executes remote RUN/remote PAUSE.
Forced execution is used when forcefully executing remote RUN/remote PAUSE from another external device when the controlled QnACPU could not execute remote RUN/ remote PAUSE because of trouble in the QC24(N) station or external device that requested QnACPU remote STOP/PAUSE.

① Data communications in ASCII mode
The designated value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The mode designation contents are shown below.

Designated value	Processing
0001H	Not forcefully executed. When the QnACPU executed remote STOP/PAUSE from another device, remote RUN/remote PAUSE is not executed.
0003H	Forcefully executed. Remote RUN/remote PAUSE is executed even if the QnACPU executed remote STOP/PAUSE from another device. (Can only be designated in the remote RUN or remote PAUSE state.)

④ When state control other than remote RUN and remote PAUSE is executed, "0001" or [0001H] is transmitted.

(b) Clear mode

This data designates QnACPU buffer memory clear (initialize) processing at the start of QnACPU operation by remote RUN.
After the designated buffer memory is cleared, the QnACPU runs according to the parameters settings (PLC file setting → device initial value).

① Data communications in ASCII mode
The designated value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The clear mode designation contents are shown below.

Designated value	Processing
00H	Device memory is not cleared.
01H	Clears the device memories outside the latch range.
02H	Clears all the device memories, including those in the latchrange.

④ When state control other than remote RUN is executed, the clear mode designation is unnecessary.

(c) Fixed value

① During data communications in the ASCII mode, "00" is transmitted.

② During data communications in the binary mode, the 1-byte value [00H] is transmitted.

③ When state control other than remote RUN is executed, fixed value designation is unnecessary.

6.4.2 Remote RUN (command: 1001)

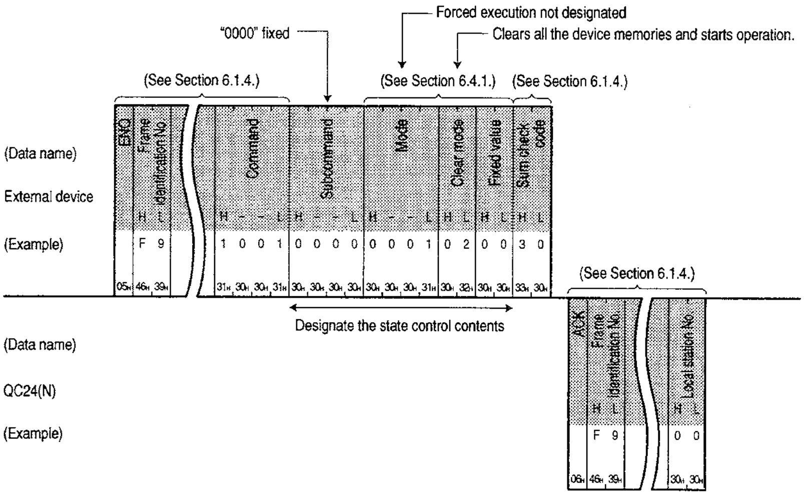
This section uses examples to describe the remote RUN control procedure.

[Control Procedure]

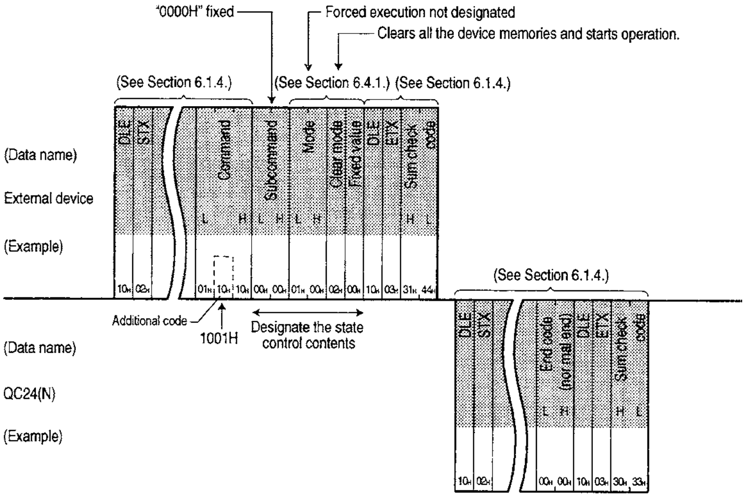
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to execute remote RUN**



2 **When using binary mode format 5 to execute remote RUN**



POINT

If forced execution is not designated by [Mode], and the objective QnACPU has already executed remote STOP/PAUSE from another external device, it will not enter the RUN state even if its own station external device executes remote RUN.

6.4.3 Remote STOP (command: 1002)

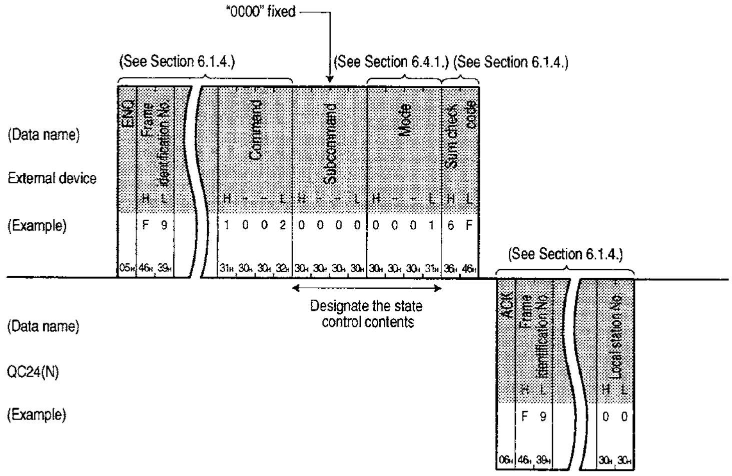
The following uses examples to describe the remote STOP control procedure.

[Control Procedure]

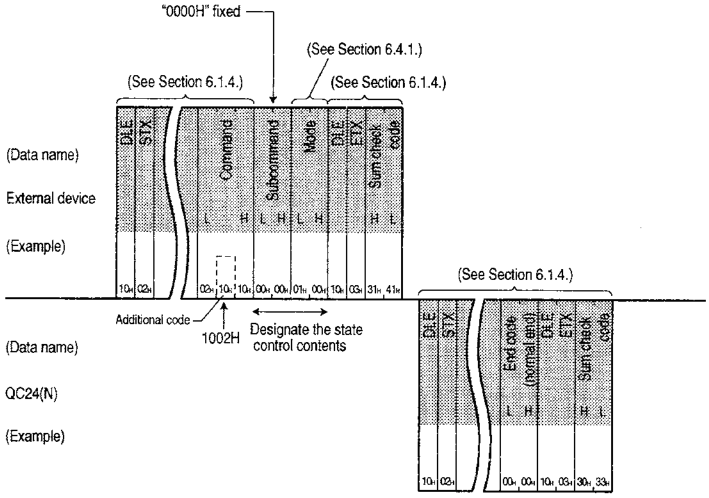
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to execute remote STOP**



2 **When using binary mode format 5 to execute remote STOP**



6.4.4 Remote PAUSE (command: 1003)

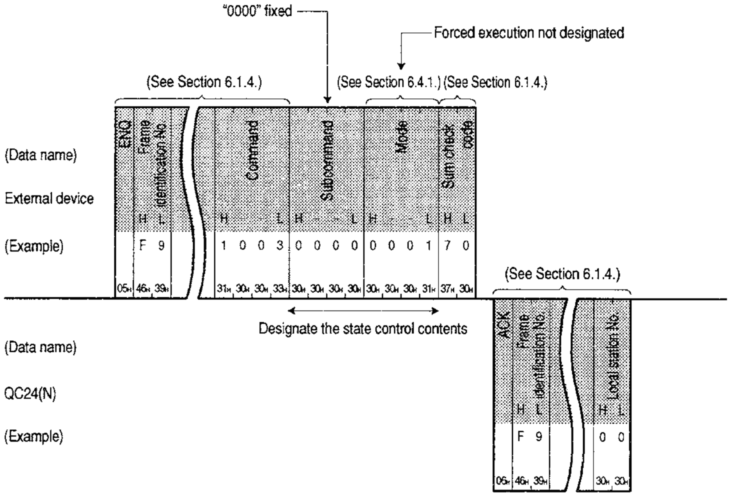
The following uses examples to describe the remote PAUSE controlprocedure.

[Control Procedure]

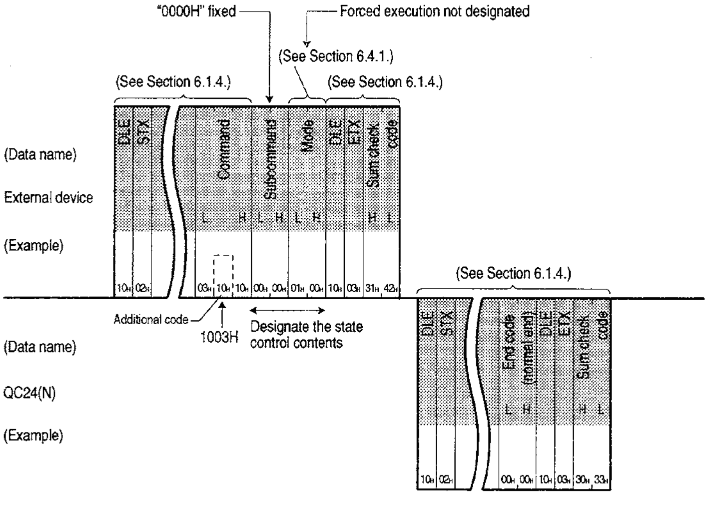
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to execute remote PAUSE**



2 **When using binary mode format 5 to execute remote PAUSE**



6.4.5 Remote latch clear (command: 1005)

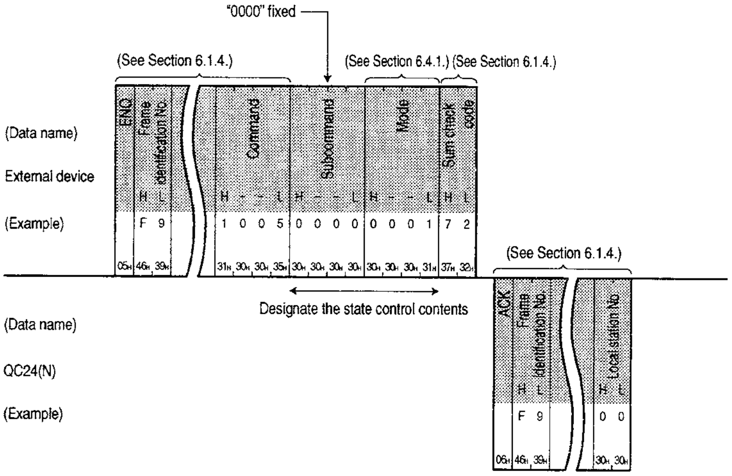
The following uses examples to describe the remote latch clear control procedure.

[Control Procedure]

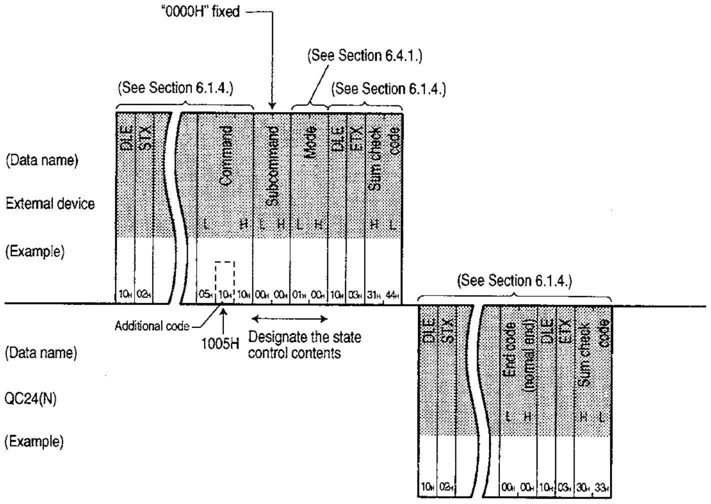
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to execute remote latch clear



2 When using binary mode format 5 to execute remote latch clear



POINTS

(1) Execute remote latch clear after putting the objective QnACPU into the STOP state.

(2) If the objective QnACPU was put into the remote STOP/PAUSE state by request from another external device, remote latch clear cannot be executed. The QC24(N) returns an NAK message to the external device.

6.4.6 Remote RESET (command: 1006)

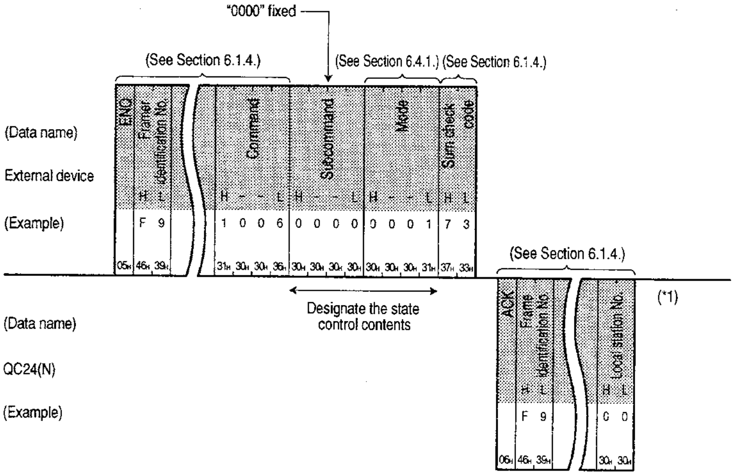
The following uses examples to describe the remote RESET control procedure.

[Control Procedure]

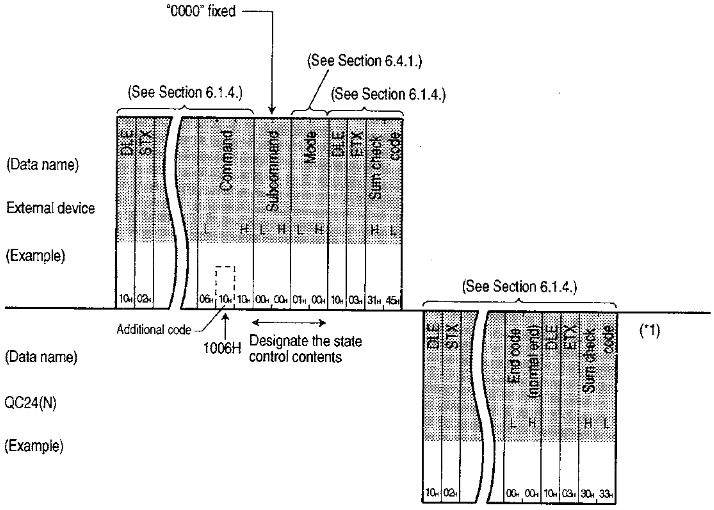
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to execute remote RESET



2 When using binary mode format 5 to execute remote RESET



*1 Before sending a response message from the QC24(N), if the QnACPU has been reset due to a request from the QC24(N), the response message is not sent from the QC24(N).

POINTS

(1) Execute remote RESET when the objective QnACPU was set to the STOP state by an generation of an error.

(2) Remote RESET can be executed when the QnACPU is operating normally. When remote RESET is executed, the QC24(N) is also resetand is restarted in the same state as when the power is turned on.

6.5 Drive Memory Defragmentation

An external device uses this function to carry out the following operations on the QnACPU drive that stores the program file containing the parameters and sequence program, etc.

1 **Drive memory status read**

Checks the usage status (cluster usage status) of the drive memory of the designated drive.

2 **Drive memory defragmentation**

Increases the continuous vacant area by defragmenting the drive memory in cluster units when the memories containing valid data are scattered over the drive memory.

The following uses an example to describe the drive memory defragmentation function control procedure.

POINT

"Cluster" is the minimum unit when files are stored to drive memory (memory card, etc.) and the memories containing data are managed by FAT(*1). The size of one cluster of each QnACPU drive is shown below.

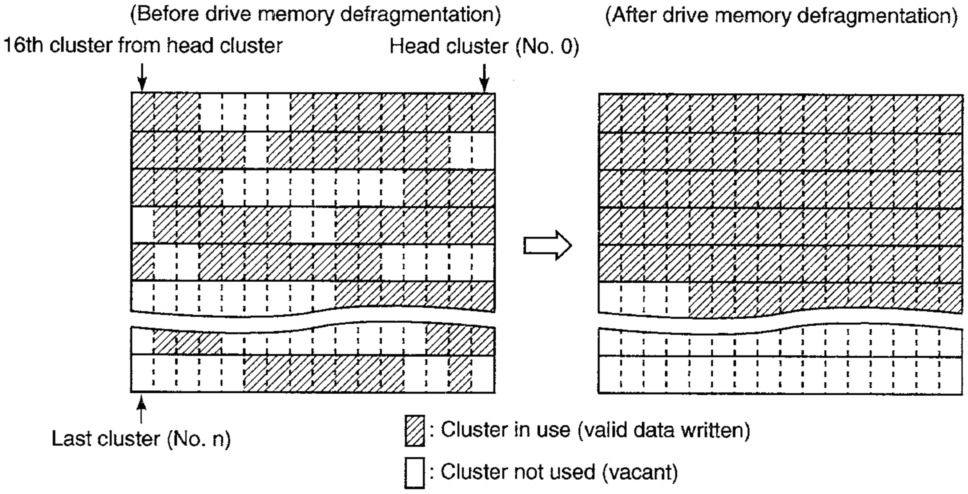
- Internal memory: 4096 bytes
- Other memory: 512 bytes

For example, if the following 512 bytes of data are written to memory card, drive memory of 1 cluster is used to write the data.

If 513 to 1024 bytes of data are written, drive memory of two clusters is used to write the data.

*1 FAT (File Allocation Table)
Table used by the OS to manage the location of files on drive memory.

(Drive memory defragmentation image)



6.5.1 Commands and contents of character area

This section describes the commands used and the character area (for binary mode, data area) in the control procedure used to defragment drive memory.

1 Commands

Function	Command (subcommand) *ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
Memory usage status read	0 2 0 5 (0 0 0 0)	Reads the drive cluster usage status.	[256 cluster]	(Un-available)	○	○	○	6.5.2
Memory defragmentation	1 2 0 7 (0 0 0 0)	Increases the continuous vacant area by defragmenting the drive memory.	(1 station)		○	×	×	6.5.3

○ in the PLC CPU state column above indicates that execution is possible.

2 Contents of character area

The following describes the contents of the character area when an external device defragments the QnACPU drive memory.

(a) Keyword

Character string (maximum 6 characters) registered to the designated drive by the user. This data enables/disables access to that drive.

When a keyword is registered, designate the same keyword.

① Data communications in ASCII mode
The keyword registered in the designated drive is transmitted.

② Data communications in binary mode
The keyword registered in the designated drive is converted to a 3-byte binary code and sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example)

Registered keyword	Before conversion to binary code	Transmission order	Notes
"012345"	01H, 23H, 45H	45H, 23H, 01H	Sequentially transmitted from 45H.
"012300"	01H, 23H, 00H	00H, 23H, 01H	Sequentially transmitted from 00H.

③ The character area keyword when a keyword is not registered in the designated drive is shown below.

- ASCII mode .... "000000"
- Binary mode 00H, 00H, 00H

(b) Set flag

This data indicates whether or not the keyword registered in the designated drive by the user is designated at the keyword of (a) above.

① Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal)ASCII code and sequentially transmitted from the most significantdigit ("0").

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The set flag designation contents are shown below.

Designated value	Designation contents
00H	Keyword is invalid (designated by a dummy).
01H	Keyword is valid (keyword registered in designated drive is designated).

(c) Drive name

This data reads the drive memory usage status and designates the QnACPU drive that is to be defragmented.

① Data communications in ASCII mode
The value shown below, which indicates the drive to be accessed, is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communication in binary mode
The 2-byte value shown below, which indicates the drive to be accessed, is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The drive name designation contents are shown below. Othervalues cannot be designated.

Designated value	Objective drive
0000H	Internal memory (internal RAM)
0001H	Memory card A RAM area
0002H	Memory card A ROM area
0003H	Memory card B RAM area
0004H	Memory card B ROM area
000FH	Drive (designated by QnACPU DIP switch) storing the parameter files currently in use.

(d) Cluster No.

This data designates the head cluster No. of the range over which the drive memory usage status is to be read. It is designated inmultiples of 16 (for hexadecimal, 00H, 10H, 20H...).

① Data communications in ASCII mode
Cluster No. 00H, or higher, is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 2-byte value that indicates cluster No. 00H, or higher, is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ When drive memory is defragmented, cluster No. does not have to be designated.

(e) Number of reads

This data designates the number of clusters within the drive memory range whose usage status is to be read. It is designated in multiples of 16 (for hexadecimal, 10H, 20H...).

① Data communications in ASCII mode
Number of clusters 10H to 100H (16 to 256) are converted to a 4digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Communications in binary mode
The 2-byte value that indicates number of clusters 10H to 100H (16 to 256) is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ When the drive memory is defragmented, the number of reads does not have to be designated.

POINT

Designate the number of reads according to the usable memory size after the drive whose usage status is to be read is formatted.
Number of clusters = Usable memory size ÷ number of bytes of 1cluster (4096 or 512)...See Section 6.5.

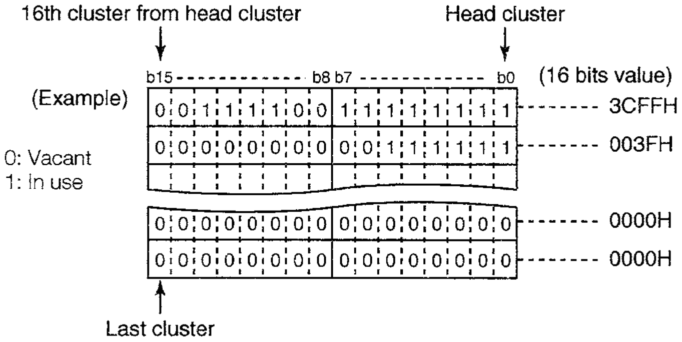
(f) Vacant cluster table

This data (indicates the cluster usage status) is returned to the external device when the drive memory usage status is read.

① Data communications in ASCII mode
The value shown below, which indicates the usage status, is converted to an n-digit (hexadecimal) ASCII code and transmitted to the external device. (16 clusters/4 digits)

② Data communications in binary mode
An m-byte value that indicates the usage state is transmitted to the external device. (16 clusters/2 bytes)

③ The contents of the vacant cluster table are shown below.
This table shows the usage status of each cluster as 1 cluster/1bit.



The contents of the vacant cluster table returned to the external device for the usage status shown above are given below.

- When 32 clusters are returned during communications in the ASCII mode
  The value "3CFF003F" is returned, and is sequentially transmitted from the first "3".
- When 32 clusters are returned during communications in the binary mode
  The values FFH, 3CH, 3FH, 00H are returned, and are sequentially transmitted from FFH.

④ When the device memory is defragmented, the vacant clustertable is not returned.

6.5.2 Drive memory usage status read (command: 0205)

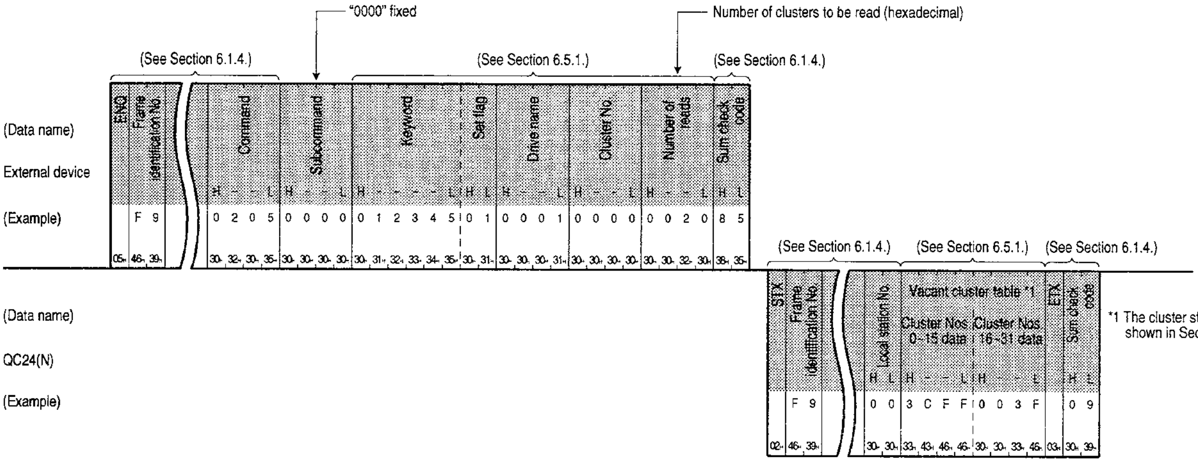
The following uses examples to describe the drive memory usage status read control procedure.

[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

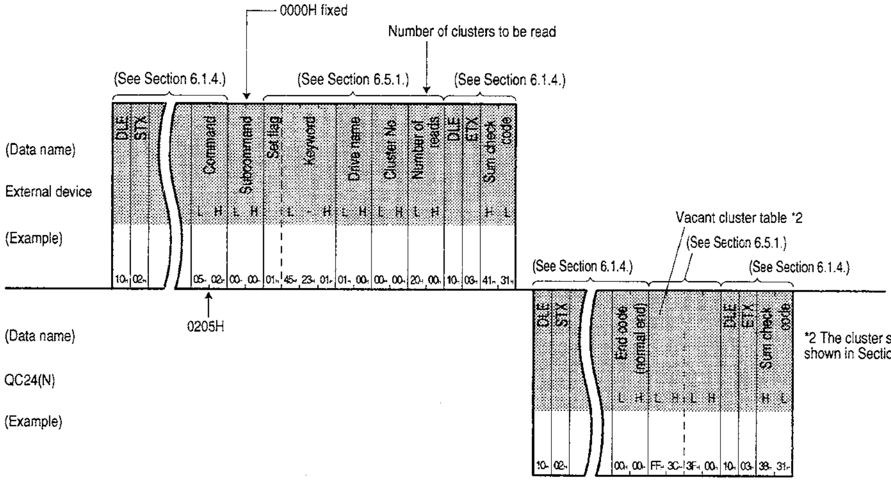
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode 1 to read the usage status of 32 clusters of the memory card A RAM area (drive name: 01H) drive memory



*1 The cluster statuses are shown in Section 6.5.1 2 (f).

2 When using binary mode format 5 to read the usage status of 32 clusters of the memory card A RAM area (drive name: 01H) drive memory



*2 The cluster statuses are shown in Section 6.5.1 2 (f).

POINTS

(1) Designate the number of reads in multiples of 16 (for hexadecimal, 10H, 20H...) within the 10H to 100H (16 to 256) range.

(2) When a new file is created (new registration), a continuous vacant area of the size of the file to be created is necessary.
To find the size of the continuous vacant area of the designated drive, check the number of continuous vacant clusters (number of OFF bits list) by reading the usage status of that drive memory.
Size of continuous vacant area = number of continuous vacant clusters × 4096 or 512 (bytes)
If the continuous vacant area is insufficient, defragment the memory as described in Section 6.5.3.

6.5.3 Drive memory defragmentation (command: 1207)

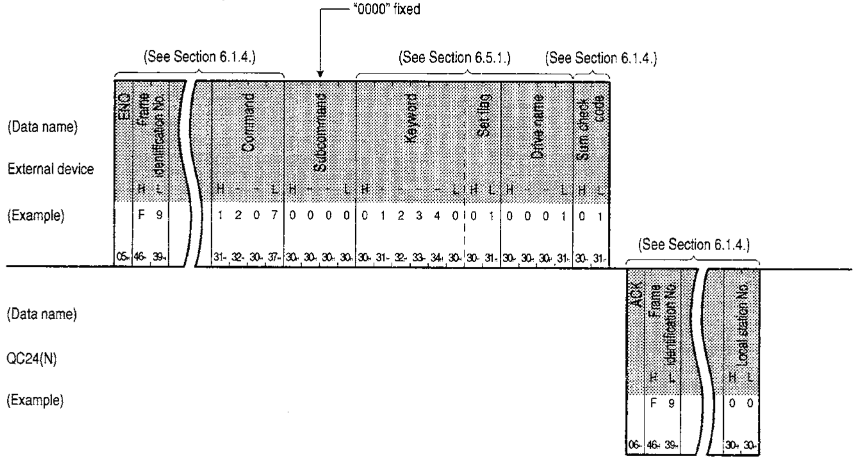
The following uses examples to describe the control procedure that defragments drive memory.

[Control Procedure]

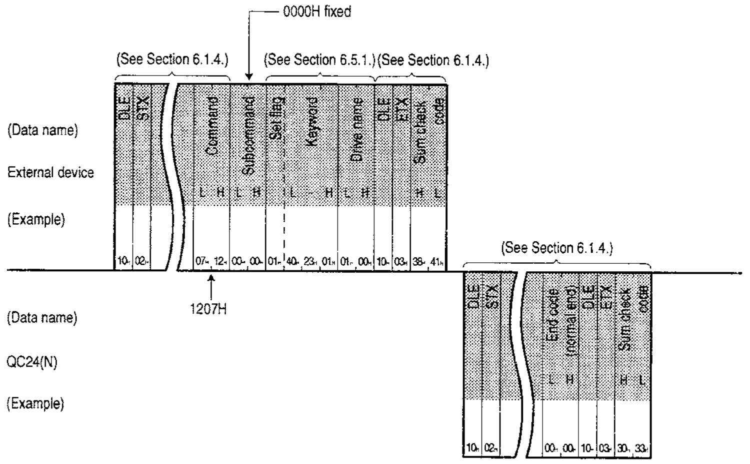
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to defragment the memory cardA RAM area (drive name: 01H) drive memory**



2 **When using binary mode format 5 to defragment the memory cardA RAM area (drive name: 01H) drive memory**



POINTS

(1) Defragment the drive memory at the following times.
  - When the designated station QnACPU is in the STOP state
  - When storing files when the drive memory usage status (checkedby command 0205) is scattered

(2) In the following cases, the QC24 will recognize an error and return a NAK message to the external device.
  ① When system-protect (system-protect switch SW5: ON) is applied to the QnACPU
  ② When the keyword registered in the designated drive was not designated.
  ③ When the drive memory is abnormal. (Defective cluster, etc.)
  ④ When the following operations are performed using an IC memory card read/writer.
    - Subdirectory is created
    - One file is stored to the continuous area of one location

6.6 File Control

This function reads the file registration status, registers newfiles, and reads, writes, and deletes data for the QnACPU designated drive.

This function is used when an external device reads and stores parameters and programs from the QnACPU or writes parameters and programs to the QnACPU according to the control contents.

6.6.1 Commands and contents of character area

The following describes the file control procedure commands and character area (in binary mode, data area) contents.

1 Commands

File		Command (subcommand) *ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
				Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
							Write enable set	Write disable set	
File information table read	No header statement	0201 (0000)	Reads the file table (filename, size and time of last updating, file size).	(36 files)	(Unavailable)	○	○	○	6.6.4 1
	Header statement	0202 (0000)	Reads the file table by file header statement.	(16 files)					6.6.4 2
	File No. usage status	0204 (0000)	Reads the file No. usage status.	(256 files)					6.6.4 3
File information modification	Date and time of last updating modification	1204 (0000)	Changes the date and time the file was last updated.	(1 file)		○	○	×	6.6.5 1
	Filename, file size modification	1204 (0001)	Changes the filename or file size.						6.6.5 2
	Batch modification	1204 (0002)	Changes the filename, file size, and date and time of last updating.						6.6.5 3
File search		0203 (0000)	Reads the file No. and file size of the designated file.	(1 file)		○	○	○	6.6.6
File contents read (batch read)		0206 (0000)	Reads the contents of a file.	960 bytes		○	○	○	6.6.7
New registration (filename registration)		1202 (0000)	Reserves an area of the designated filename.	(1 file)		○	○	×	6.6.8
File contents write	Arbitrary data (batch write)	1203 (0000)	Writes the designated data (n bytes) to a file.	960 bytes		○	○	×	6.6.9 1
	Same data (FILL)	1203 (0001)	Writes n bytes of the designated data (1 word) to a file.	(File size)					6.6.9 2
File lock	Register	0808 (0001)	Registers file lock so that the contents cannot be modified from another device. Or clears registration.	(1 file)		○	○	○	6.6.10
	Clear	0808 (0000)							
File copy		1206 (0000)	Write the contents of an existing file to a new file.	480 bytes		○	○	○	6.6.11
File delete		1205 (0000)	Deletes a file.	(1 file)		○	○	×	6.6.12

○ in the PLC CPU column in the table above indicates that execution is possible.

2 Contents of character area

The following describes the contents of the character area of the messages described beginning from Section 6.6.4 when an external device controls the QnACPU files.

(a) Keyword

Character string (maximum 6 characters) registered to the designated drive by the user. This data enables/disables access to that drive.
When a keyword is registered, designated the same keyword.
See Section 6.5.1 2 (a) for a description of the contents of the character area.

(b) Set flag

This data indicates whether or not the keyword registered in the designated drive by the user is designated at (a) Keyword above.
See Section 6.5.1 2 (b) for a description of the contents of the character area.

(c) Drive name

This data designates the QnACPU whose files are to be controlled.
See Section 6.5.1 1 (c) for a description of the character area.

(d) File No.

This data designates the registration No. when a file designated by filename and extension described below was registered (written) to the PLC CPU, or the registration No. when registering to the PLC CPU.

① Data communications in ASCII mode
The file No. shown below is converted to a 4-digit (hexadecimal)ASCII code and sequentially transmitted from the most significant digit.

(Example) 1FH....Converted to "001F" and sequentially transmitted from the first "0".

② Data communications in binary mode
A 2-byte value indicating the file No. shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

(Example) 1FH....The value 001F is transmitted in 1FH, 00H order.

③ The file Nos. shown below can be designated.

Designated value	Contents	Designation contents
01H to 100H	File No.	Designated when the file No. is known.
FFFFH	File No. unknown	Designated when searching the QC24(N) for the file No. [Read/write requests from QC24(N) to PLC CPU are delayed by 1 sequence scan time, or longer.]

④ The file No. of a registered file can be checked using the file search function described in Section 6.6.6.
When registering a new file, the unused file Nos. can be checked using the file No. usage status read function described in Section 6.6.4.

(e) Number of file requests, total number of registered files, number of file information

These data indicate the number of files requested by the user, number of files registered in the designated drive, and number offiles that return file information during file information read.

① Data communications in ASCII mode
The value given in the description of the relevant function isconverted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 2-byte value given in the description of the relevant function is sequentially transmitted from the Low byte (L: bits 0 to 7).

(f) Filename, extension, attribute

This data designates the file to be read, written, registered, etc.
When designating an existing file, designate the filename, extension, and attribute designated when the file was registered (written) to the PLC CPU.
When registering a new file, designate the filename (maximum 8 encharacters) and extension (maximum 3 en characters) according to the rules for naming files by QnACPU compatible GPP function.

* Alphanumeric characters and kana characters and characters (shift JIS kanji code) can be used.
See the GPP function operating manual (online) for more information.

The attribute of files created by the user is initially 20H (diskfile), but can be changed by the user. (See Section 6.6.5.)

① Data communications in ASCII mode
The filename, extension, and attribute are sequentially transmitted from the first character.
A blank (code: 20H) is transmitted as the attribute of a new file and for dummy attribute designation.

When the filename is less than 8 characters, blanks (code: 20H)are added.

(Example) When the filename designated during registration was "ABCD12"
The filename "ABCD12␣␣" is sequentially transmitted from the "A".

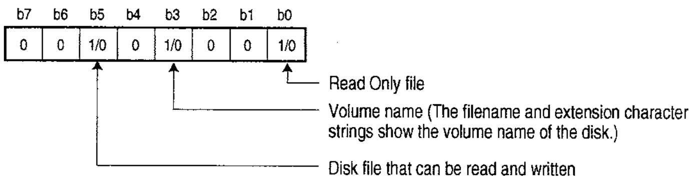
② Data communications in the binary mode
The character code of each character of the filename and extension is used as a binary value and is sequentially transmitted from the first character.
The 1-byte value [20H] is transmitted as the attribute of a new file and for dummy attribute designation.
When the filename is less than 8 characters, 20H are added tomake it 8 characters.

(Example) When the filename designated during registration was "ABCD12"
The filename becomes 41H, 42H, 43H, 44H, 31H, 32, 20H, 20H and issequentially transmitted from 41H.

③ The attribute of an existing file can be checked using the file read function described in Section 6.6.6.

Note

The following outlines the basics of the attribute of the files stored on each disk of the QnACPU.
Each bit of the value indicating the attribute is meaningful.
The applicable attribute is fixed according to the relevant bit turns ON(1).



* User files whose attribute does not change are given the read/write disk file attribute. The attribute of a user file can be changed between 01H (Read Only file) ↔ 20H (read/write disk file). (See Section 6.6.5.)

(g) Time of last updating, date of last updating

This data indicates the date and time the current contents were registered.

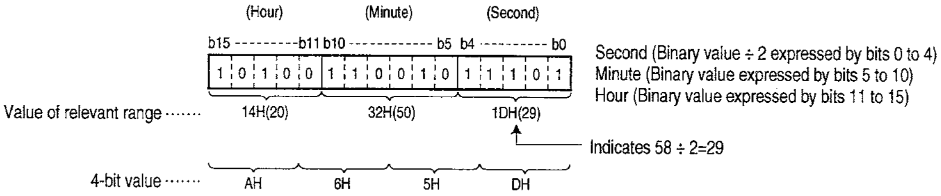
① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit (time, year). Transmits "0000" when dummy is designated.

② Data communications in binary mode
The 2-byte values shown below are sequentially transmitted from the Low byte (L: bits 0 to 7). Transmits 0000H when dummy is designated.

③ The contents of the values that indicate the time and date and the order in which they are transmitted are shown below.

- Time (hour, minute, second)

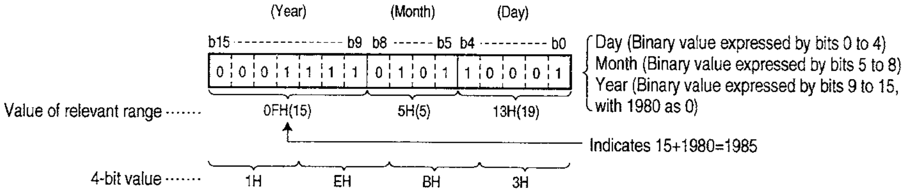
(Example) 20 hours 50 minutes 58 seconds



Binary mode data······A65DH (Transmitted in 5DH, A6H order.)
ASCII mode data ······"A65D" (Sequentially transmitted from the "A".)

- Date (Year, month, day)

(Example) May 19, 1995



Binary mode data······1EB3H (Transmitted in B3H, 1EH order.)
ASCII mode data ······"1EB3" (Sequentially transmitted from the "1".)

(h) File size

This data indicates the current file size in number of byte.

① Data communications in ASCII mode
The 2-word value is converted to an 8-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Example) When the file size is 7168 bytes
Converted to "00001C00" and sequentially transmitted from the head "0".
Head ⅃

② Data communications in binary mode

The 2-word value is sequentially transmitted from the Low byte (L:bits 0 to 7).

(Example) When the file size is 7168 bytes
The file size becomes 00001C00H and is transmitted in 00H, 1CH,00H, 00H order.

(i) Header statement

This is the header statement given to the designated file by the QnACPU compatible GPP function. (Maximum 32 en characters)

① Data communications in ASCII mode
The header statement is sequentially transmitted from the head character.
When the header statement is less than 32 characters, blanks (code: 20H) are added to make it 32 characters.

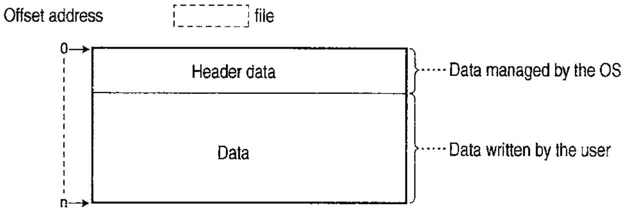
(Example) When the header statement designated during registration was "1 line-PC5"
The header statement "1 line-PC5..." is sequentially transmitted from the "1".

② Data communications in binary mode
The character code of each character of the header statement is used as a binary value and is sequentially transmitted from the head character.
When the header statement is less than 32 characters, 20H codes are added to make it 32 characters.

(Example) When the header statement designated during registration was "1 line-PC5"
The header statement becomes 31H D7H, B2H, DDH, 2DH, 50H, 43H,35H, 20H, 20H, ... and is sequentially transmitted from 31H.

(j) Offset address

This data designates the head address of the area of the range within which data is to be read from, or written to, the file.
The head address (1 address/1 byte) from the head (offset address: 0H) of each file is designated as an even address.



① Data communications in ASCII mode
The address given in the description of the relevant function is converted to an 8-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 4-byte value that indicates the address given in the description of the relevant function is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ For the offset address that can be designated, check the filesize (number of bytes) using the file information table read function described in Section 6.6.4 and find the offset address (0H to nH) from this size.

(k) Number of read bytes, number of write bytes

These data designate the number of bytes of the range within which data is to be read from, or written to, the file. It is designated as 1 address/1 byte.

① Data communications in ASCII mode
The value given in the description of the relevant function is converted to a 4-digit (hexadecimal) ASCII code and transmitted from the most significant digit ("0").

② Data communications in binary mode
The 2-byte value given in the description of the relevant function is sequentially transmitted from the Low byte (L: bit 0 to 7).

(l) Read data, write data (batch read, batch write functions)

These are the data read from, or written to, the QnACPU file.
They are listed from the offset address.

① Data communications in ASCII mode
One byte (1 address) is converted to a 2-digit (hexadecimal) ASCII code and the designated number of bytes are sequentially transmitted from the most significant digit.

② Data communications in binary mode
The designated number of bytes is transmitted with 1 address as 1byte.

③ Read stores unchanged the list read from the QnACPU to the external device.
Write designates unchanged the list read from the QnACPU.

(m) Write data (same data write function)

This data is for the same data write function when the same datais written to an existing QnACPU file.

① Data communications in ASCII mode
The value of 1 word is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The value of 1 word is sequentially transmitted from the Low byte (L: bits 0 to 7).

(n) Size

This data reserves the file area on the designated disk during new file registration. It is designated in number of bytes.

① Data communications in ASCII mode
The value when the area for the designated file to be reserved is expressed as 2 words is converted to an 8-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant byte.

② Data communications in binary mode
The value when the area for the designated file to be reserved is expressed as 2 words is sequentially transmitted from the Lowbyte (L: bits 0 to 7).

③ An external device can register a new file with the same contents as an existing file. The size of the objective existing file must be reserved using the file information table read function described in Section 6.6.4.

(o) Fixed value

① During data communications in the ASCII mode, "0000" is transmitted.

② During data communications in the binary mode, the 2-byte value [0000H] is transmitted.

(p) Modification pattern (for filename and file size modification)

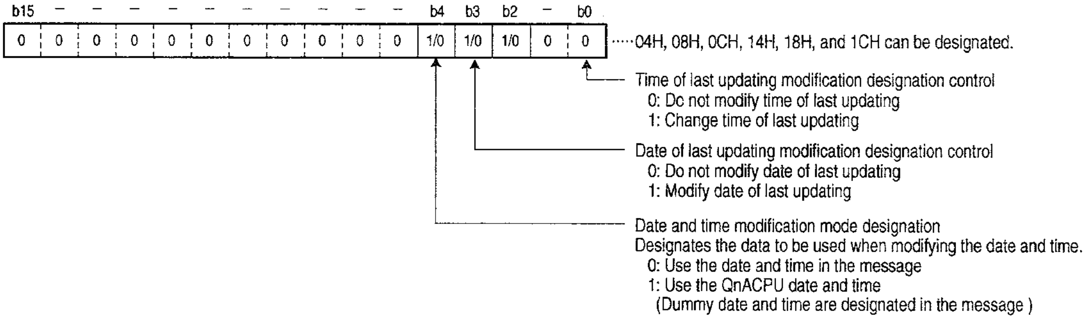
This data designates what data is to be modified when the data (filename, size, date and time created) of an existing file is to be modified.

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

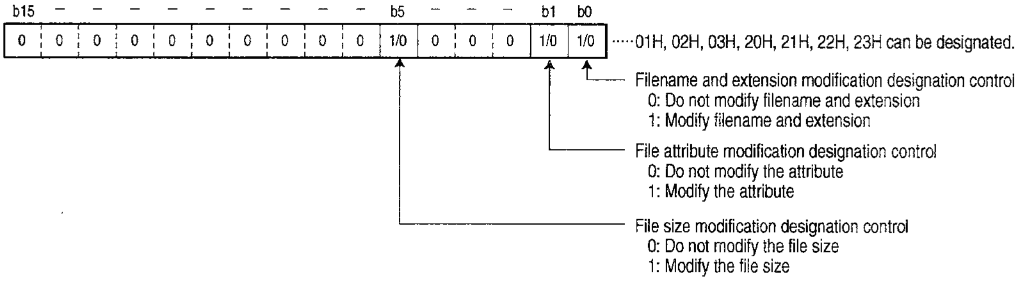
② Data communications in binary mode
The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The modification pattern designated value and contents are shown below.

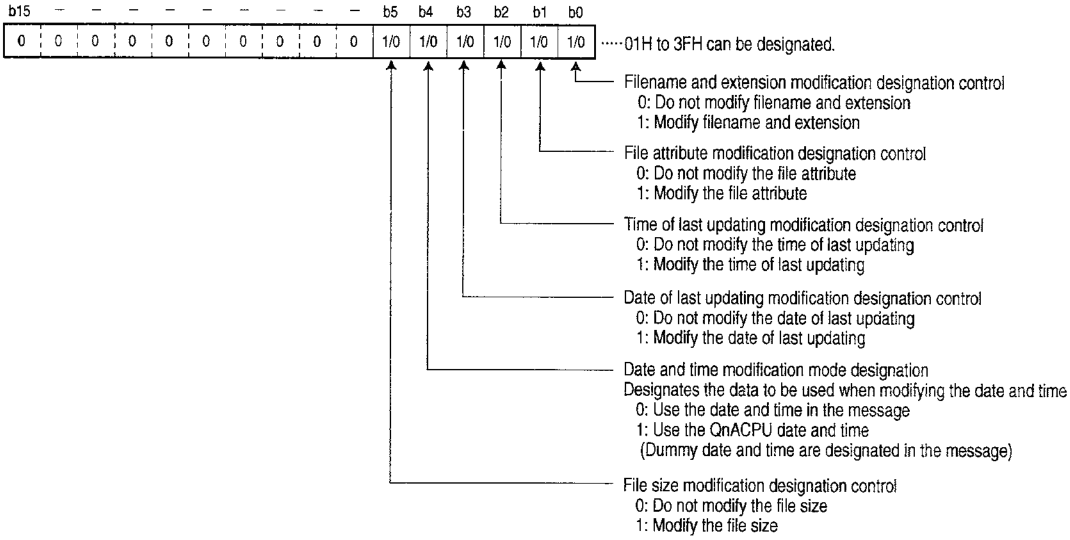
- When modifying the date and time the file was created
  (command:1204, subcommand: 0000)



- When modifying the filename and file size
  (Command: 1204, subcommand: 0001)



- When batch modifying the file information (command: 1204, subcommand: 0002)



·····01H to 3FH can be designated.

Filename and extension modification designation control
0: Do not modify filename and extension
1: Modify filename and extension

File attribute modification designation control
0: Do not modify the file attribute
1: Modify the file attribute

Time of last updating modification designation control
0: Do not modify the time of last updating
1: Modify the time of last updating

Date of last updating modification designation control
0: Do not modify the date of last updating
1: Modify the date of last updating

Date and time modification mode designation
Designates the data to be used when modifying the date and time
0: Use the date and time in the message
1: Use the QnACPU date and time
(Dummy date and time are designated in the message)

File size modification designation control
0: Do not modify the file size
1: Modify the file size

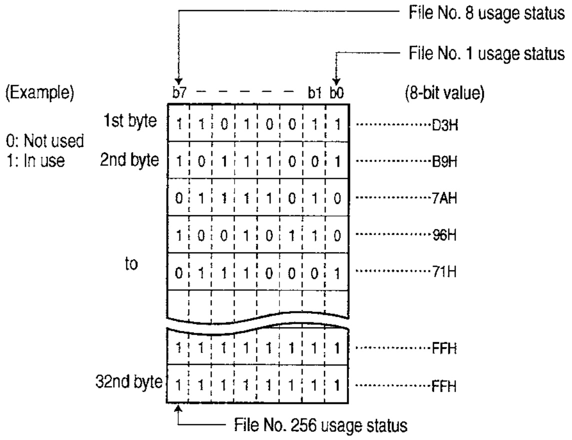
(q) File No. usage status

This data shows the usage status of the 256 file Nos. returned to the external device by the file No. usage status read function. It is listed from the 1st byte shown below, which indicates the file No. usage status.

① Data communications in ASCII mode
The value shown below is converted to a 64-digit (hexadecimal) ASCII code and transmitted to the external device.
(Eight file Nos.: 2 digits)

② Data communications in binary mode
The following 32-byte value indicating the usage state is sequentially transmitted to the external device from the Low byte (L:bits 0 to 7). (Eight file Nos.: 1 byte)

③ The contents of the file No. usage status are shown below.
The usage status of each file No. is shown as 1 file No./1 bit.



The contents of the file No. usage status returned to the external device for the usage status shown above are shown below.

- During data communications in the ASCII mode, "D3B97A...FFFF" are returned, and are sequentially transmitted from the "D".
- During data communications in the binary mode, D3H, B9H, 7AH...FFH, FFH are returned, and are sequentially transmitted from D3H.

(r) File lock mode

This data designates whether or not file lock is to be forcefully cleared when access to the designated file from another device is enabled.

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The following 2-byte numbers are used and transmitted from the low byte (L: Bit 0 to 7).

③ The file lock mode designated values and designation contents are shown below. Other values cannot be designated.

Designated value	Designation contents
0000H	Normally execute file lock clear.
0002H	Forcefully execute file lock clear.

④ The difference between normal execution and forced execution when file lock clear is executed for the designated file is described below.

- Normal execution

  When another device registers file lock, file lock cannot be cleared.

  When a clear request is issued, the QC24(N) recognizes an error and returns a NAK message.

- Forced execution

  File lock is forcefully cleared even if another device registered file lock.

  Use the forced execution function when file lock cannot be cleared because of trouble in the device that registered the file lock.

(s) Copy mode

This data designates the file to which the date and time the source file was updated is to be copied upon completion of copying by the file copy function.
When the date and time are not copied, the QnACPU management time when the file was created remains unchanged.

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and is sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The copy mode designated values and contents are shown below.

Designated value	Designation contents
0000H	Do not copy the date and time the source file was last updatedat the end of copying.
0001H	Copy the date and time the source file was last updated at the end of copying.

6.6.2 File control precautions

The following describes the precautions that should be taken when using the functions described in Section 6.6 to control QnACPU files.

(1) The files read from the QnACPU are for storage by an external device.

The external device cannot edit (revise, modify) the contents of a file read from the QnACPU.

(2) The maximum number of bytes when data is read and written is fixed.

When reading data from a file to an external device, read all the data by dividing the data to be written to the QnACPU into two or more parts.
When writing data from an external device, write all the data by dividing the read data into two or more parts.
The file size can be checked using the following functions.

- File information table read function .... See Section 6.6.4.
- File search function .... See Section 6.6.6.

(3) If system-protect (system-protect SW5: ON) is applied to the QnACPU when using the following functions, the QC24(N) will recognize an error and will return a NAK message to the external device.

- File information modification function...... See Section 6.6.5.
- New file registration function .... See Section 6.6.8.
- File contents write function..................... See Section 6.6.9.
- File copy function .... See Section 6.6.11.
- File delete function .... See Section 6.6.12.

(4) When registering a keyword to the file control objective disk, memorize the keyword.

When accessing the following files, always designate the registered keyword.

- Parameters file
- Program file
- Data write file (when command: 1203, subcommand: 0001 designated)

(5) The file attribute data is valid only when using the following functions.

The attribute of files handled by other functions is treated as adummy.

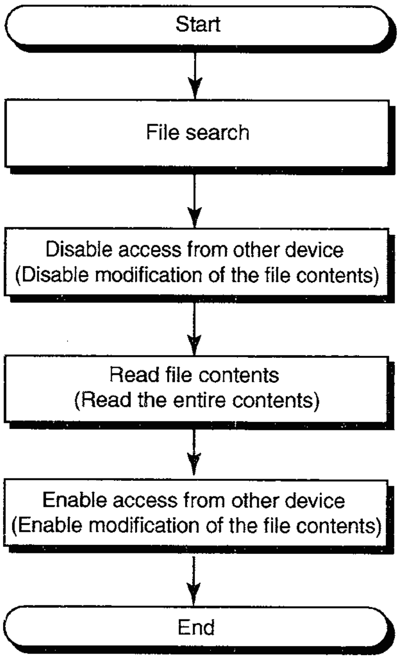
- File information read function .... See Section 6.6.4.
- File information modification function...... See Section 6.6.5.
- New file registration function .... See Section 6.6.8.

(6) See POINT of the description of each function for other precautions.

6.6.3 File control execution procedure

The following uses flowcharts to show the file control procedures.

1 Procedure when reading the contents of a file



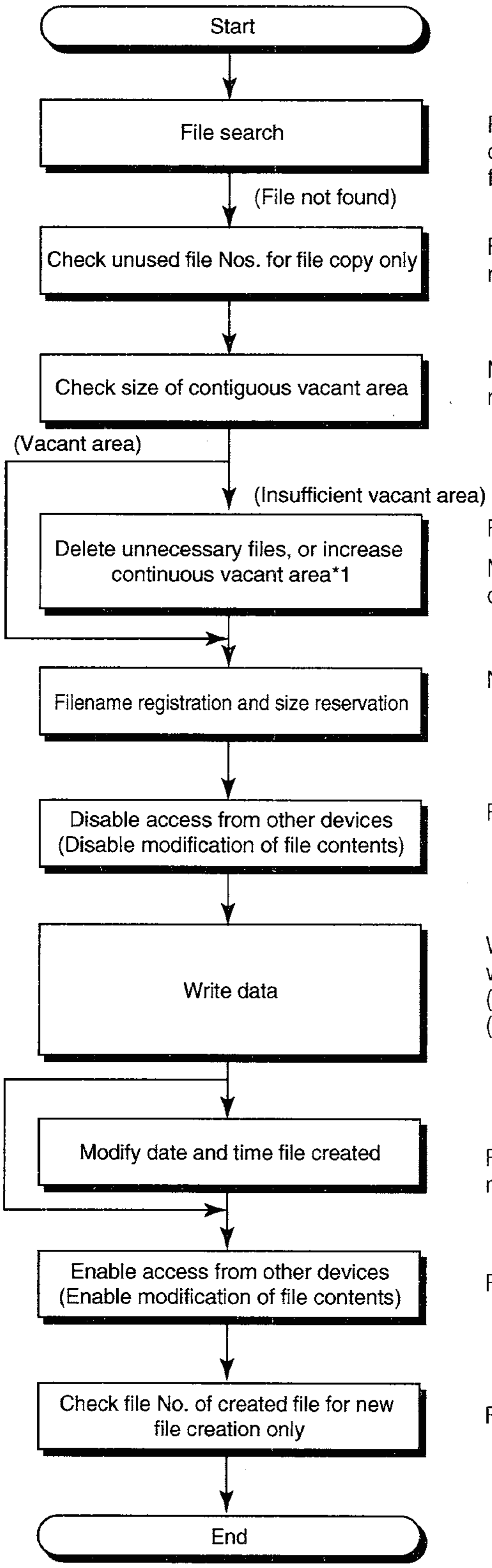
(Function name)	(Command)	(Reference section)
File search	0203	6.6.6
or		
file information read	0201 0202	6.6.4
File lock registration	0808	6.6.10
File contents read (batch read)	0206	6.6.7
File lock clear	0808	6.6.10

POINT

Store the following file information of the file (storage use) read to an external device in advance.

- File No.
- Filename and attribute
- File size

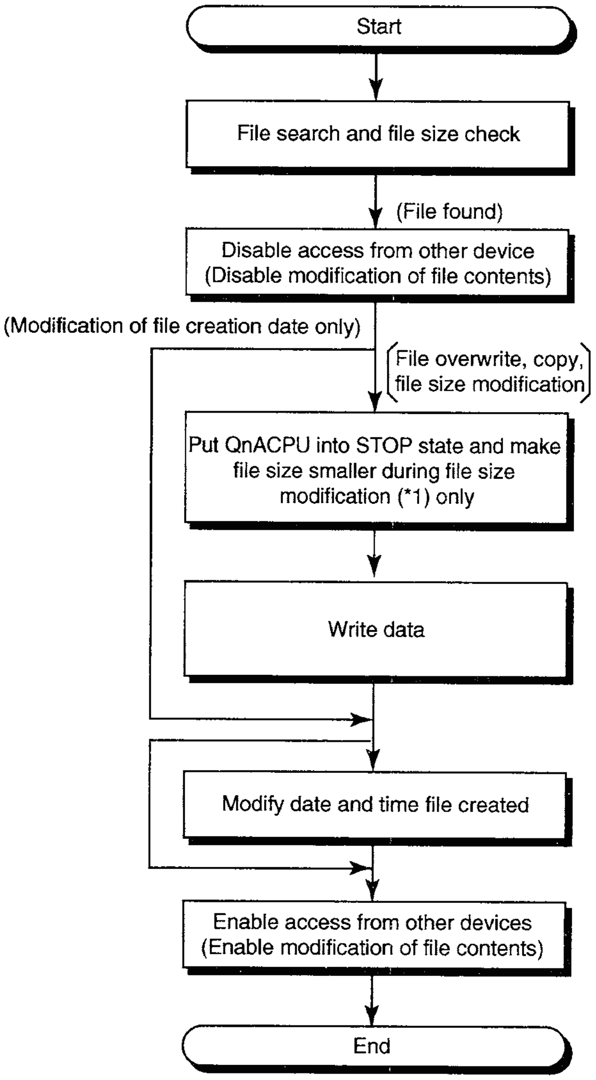
2 Procedure when creating a new file and writing data to that file
Procedure when copying the data of an existing file to a new file



(Function name)	(Command)	(Reference section)
File search or file information read	0203 0201 0202	6.6.4
File No. usage status read	0204	6.6.4
Memory usage status read	0205	6.5.2
File delete		4 of this section
Memory defragmentation	1207	6.5.3
New file creation	1202	6.6.8
File lock registration	0808	6.6.10
Write to file (Batch write)	1203	6.6.9
(Write same data)	1203	6.6.9
(File copy)	1206	6.6.11
File information modification	1204	6.6.5
File lock clear	0808	6.6.10
File search	0203	6.6.4

*1 Use the remote STOP (command: 1002) function described in Section 6.4.3 to put the QnACPU into the STOP state before defragmenting memory.
After completion of processing of this section, the remote RUN (command: 1001) function described in Section 6.4.2 can be used to put the QnACPU into the RUN state.

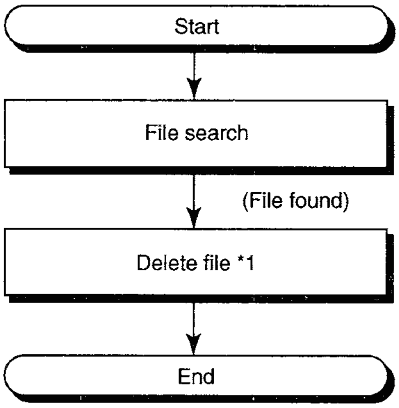
3 Procedure when overwriting data to an existing file
Procedure when modifying the file information



(Function name)	(Command)	(Reference section)
File search	0203	
or		
file information read	0201 0202	6.6.4
File lock registration	0808	6.6.10
Write to file		
(Batch write)	1203	6.6.9
(Same data write)	1203	6.6.9
File information modification	1204	6.6.5
File lock clear	0808	6.6.10

*1 The file information modification (command: 1204) function described in Section 6.6.5 can modify the file size only when making the file size smaller.
When the file size must be made larger, use the procedure described in 2 of this section to create a new file and write the data.

4 Procedure when deleting a file



(Function name)	(Command)	(Reference section)
File search	0203	6.6.4
or		
file information read	0201 0202	
File delete	1205	6.6.12

*1 Determine the file deletion timing for the entire system, including the QnACPU and related devices.

6.6.4 File information table read

1 Reading file information table without header statement (command: 0201)

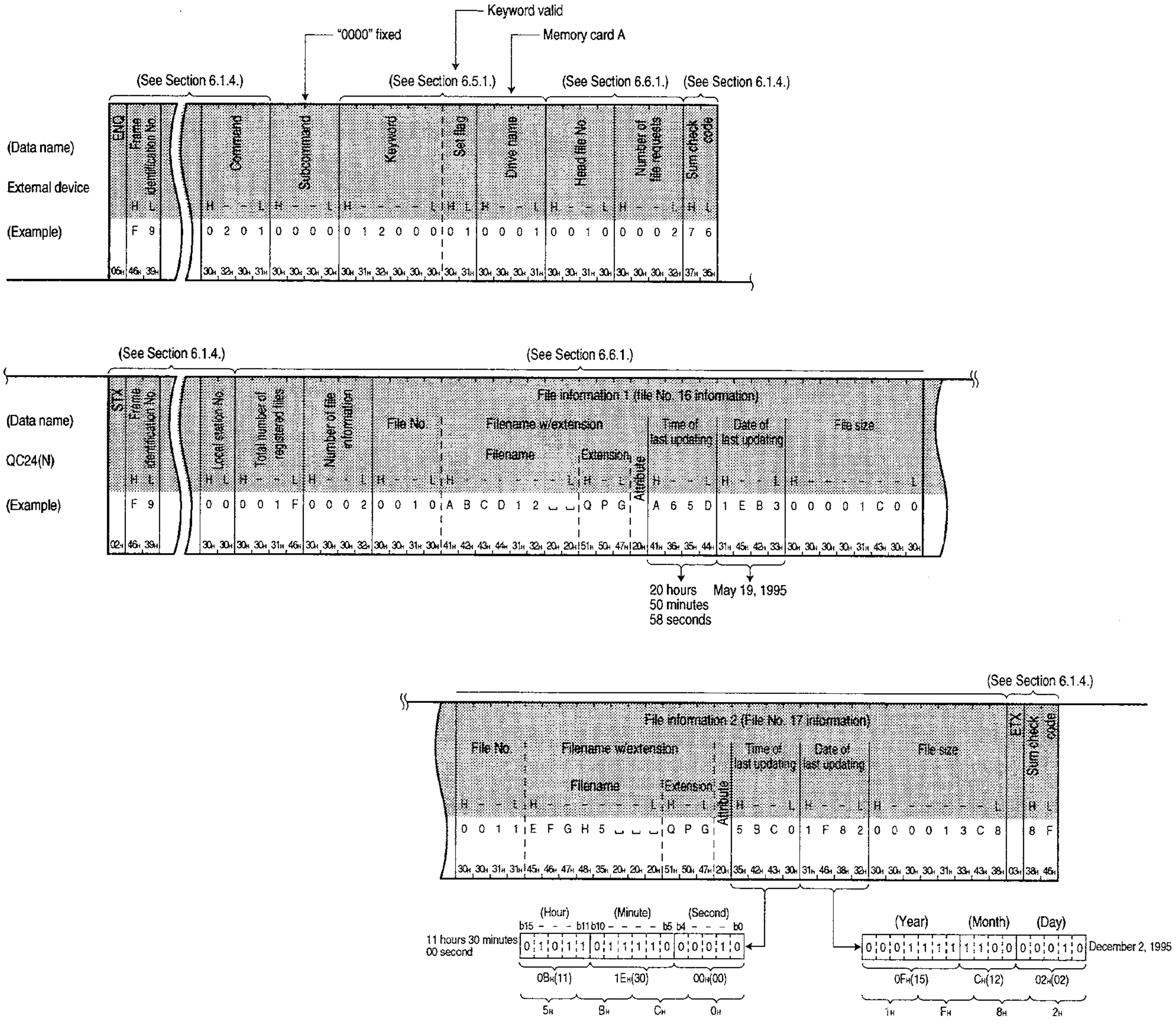
The following uses examples to describe the control procedure that reads the file information within the designated file No.range.

[Control Procedure]

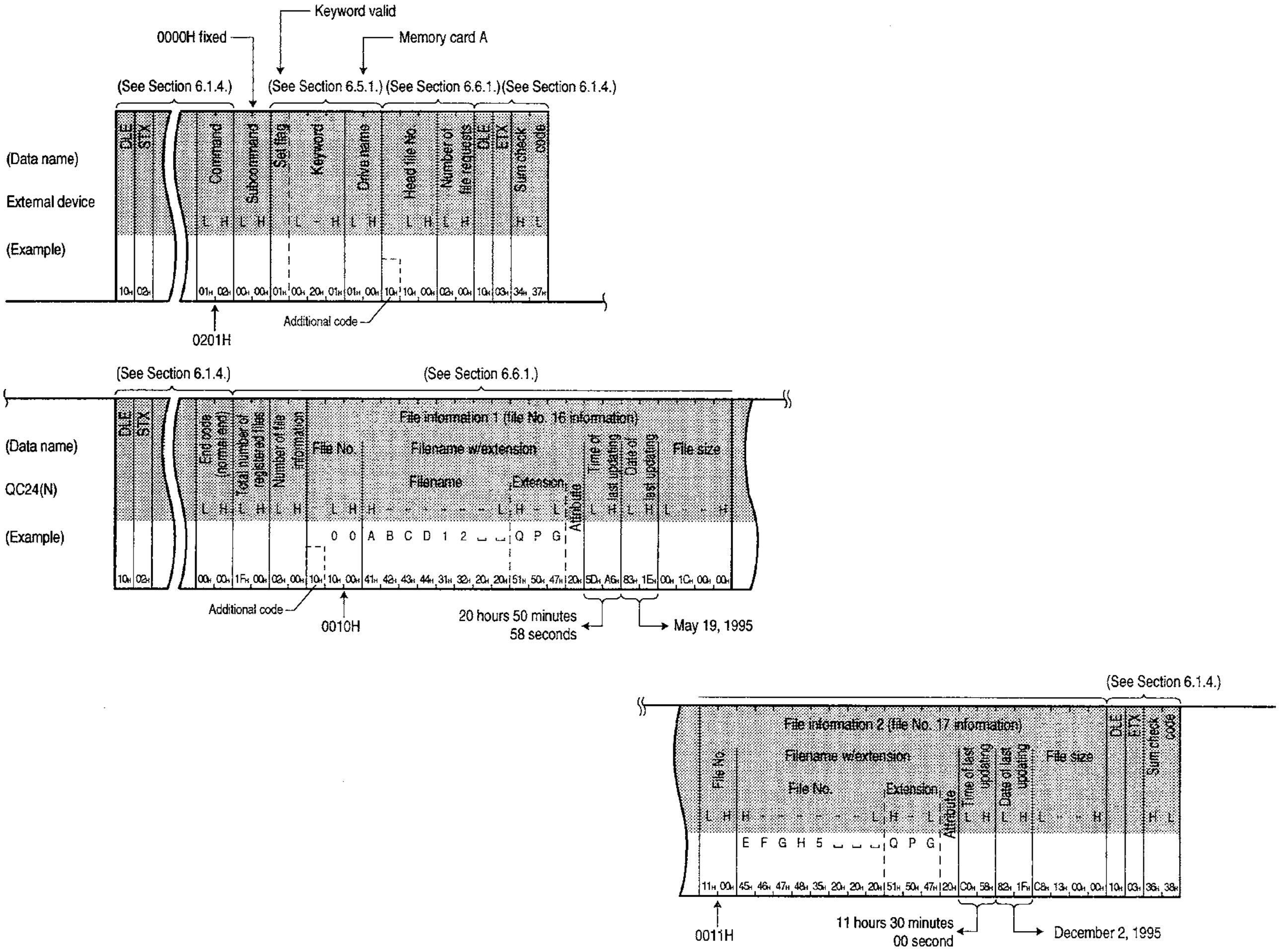
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to read the file information of two files from memory card A (RAM area, drive name:01H) file No. 16 (10H).



(b) When using binary mode format 5 to read the file information of two files, beginning from memory card A (RAM area, drive name:01H) file No. 16 (10H)



POINTS

(1) Designate, or return, the designated values within the following range.

- Head file No .... 1 ≤ file No. ≤ 256
- Number of file requests .... 1 ≤ file No. ≤ 36
- Total number of registered files ... 1 ≤ number of files ≤ 256
- Number of file information......... 0 ≤ file count ≤ number of file requests (0: No registered files from the designated head file No.)

(2) The total number of registered files is the current total number of files registered at the designated drive.

(3) When all the files are not registered within the designated file No. range, the number of file information becomes the number of files registered in the designated range (Return number of file information).

2 Reading file information table with header statement (command: 0202)

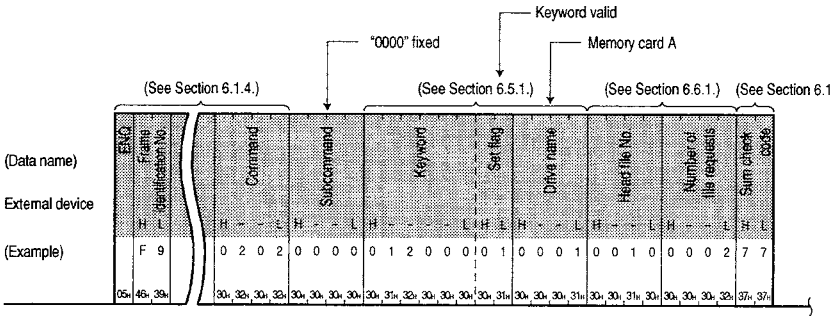
The following uses examples to describe the control procedure that reads, with header statement, the file information over the designated file No. range.

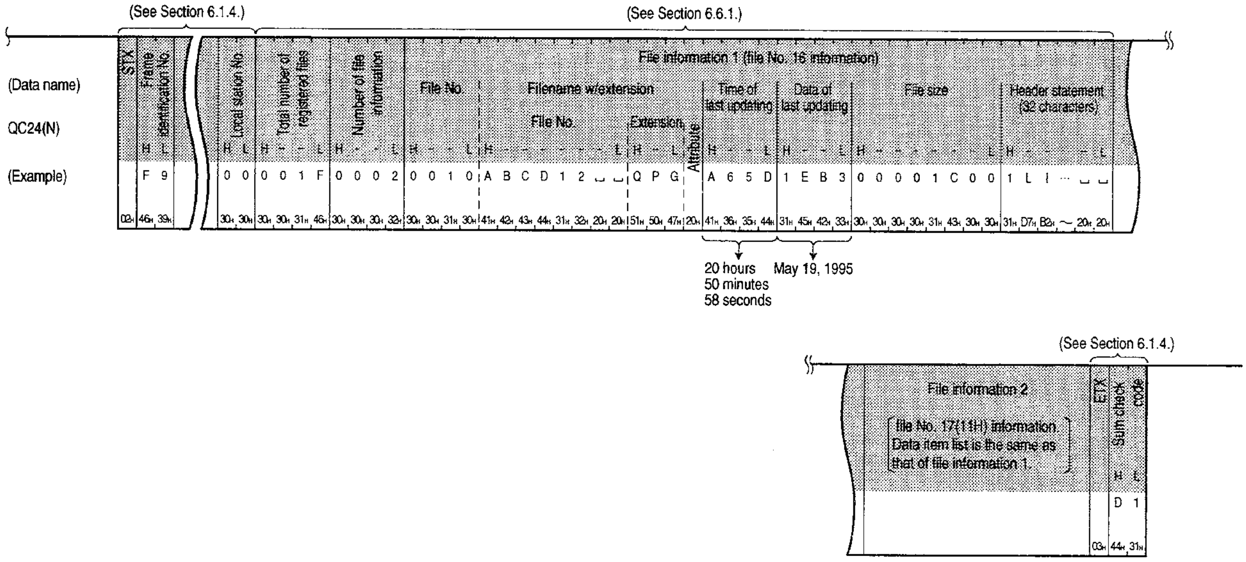
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

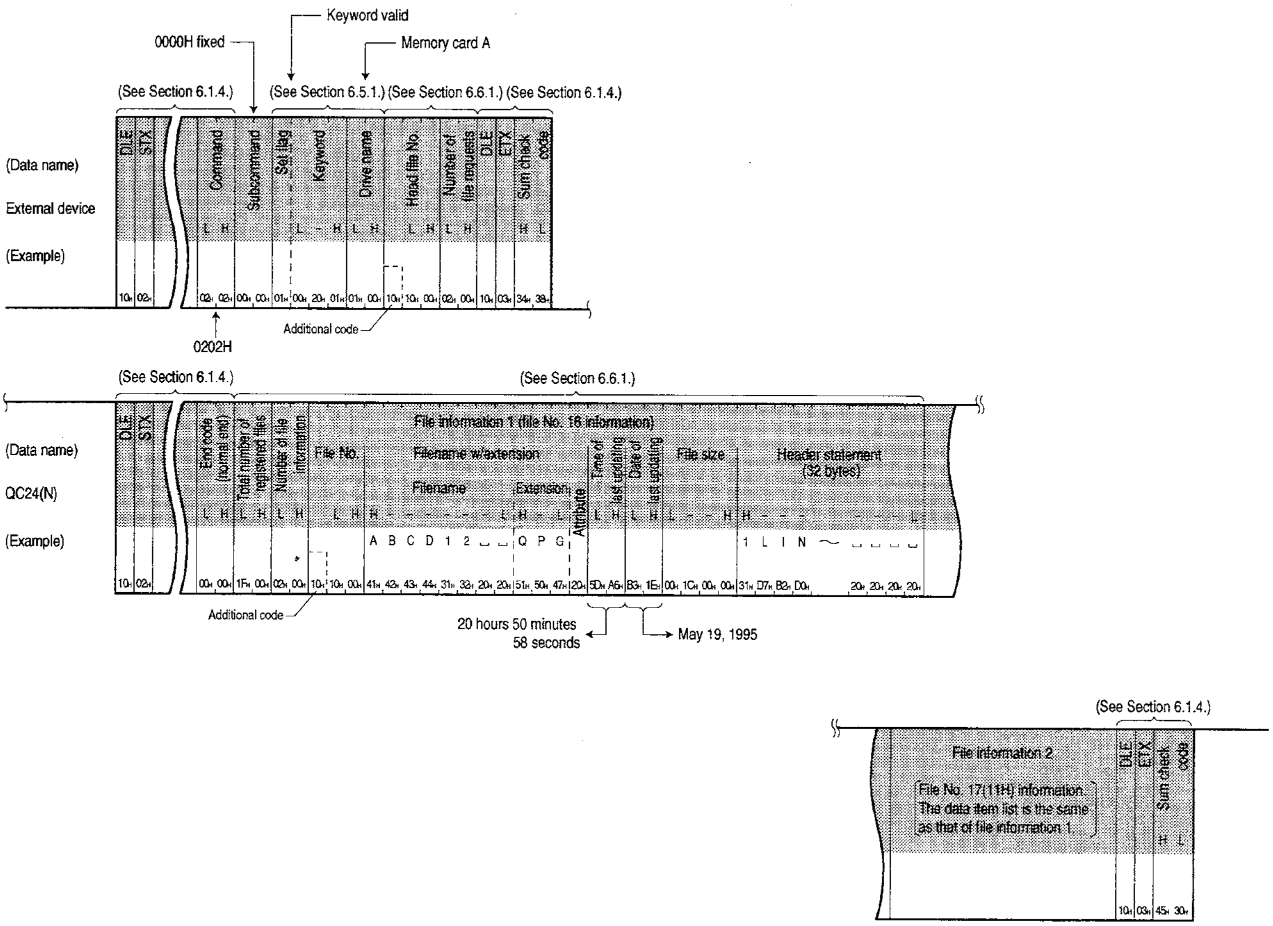
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to read the file information of two files, beginning from memory card A (RAM area drive name:01H) file No. 16 (10H)





(b) When using binary mode format 5 to read the file information of two files, beginning from memory card A (RAM area, drive name:01H) file No. 16 (10H)



POINTS

(1) Designate, or return, the designated values within the following range.
- Head file No. .... 1 ≤ file No. ≤ 256
- Number of file requests .... 1 ≤ file No. ≤ 16
- Total number of registered files ... 1 ≤ number of files ≤ 256
- Number of file information......... 0 ≤ number of files ≤ number ofregistered files

(0: No registered files from the designated head file No.)

(2) The total number of registered files is the total number offiles currently registered in the designated drive.

(3) When all the files are not registered within the designated file No. range, the number of file information becomes the number of files registered in the designated range (Return number of file information).

3 File No. usage status read (command: 0204)

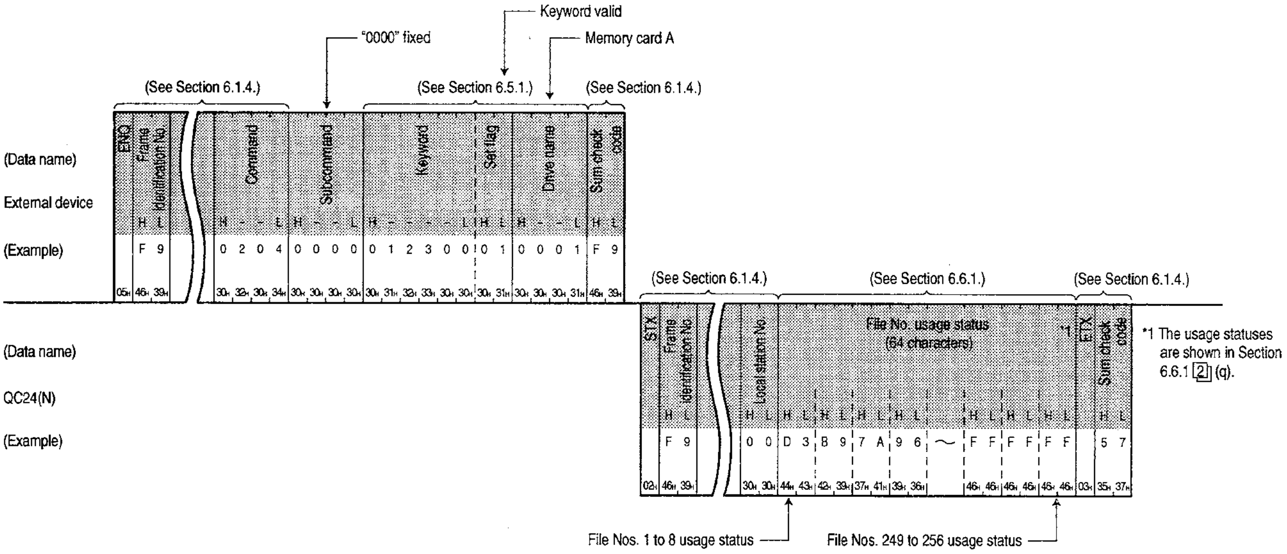
The following uses examples to describe the control procedure that reads the file No. usage status.

[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

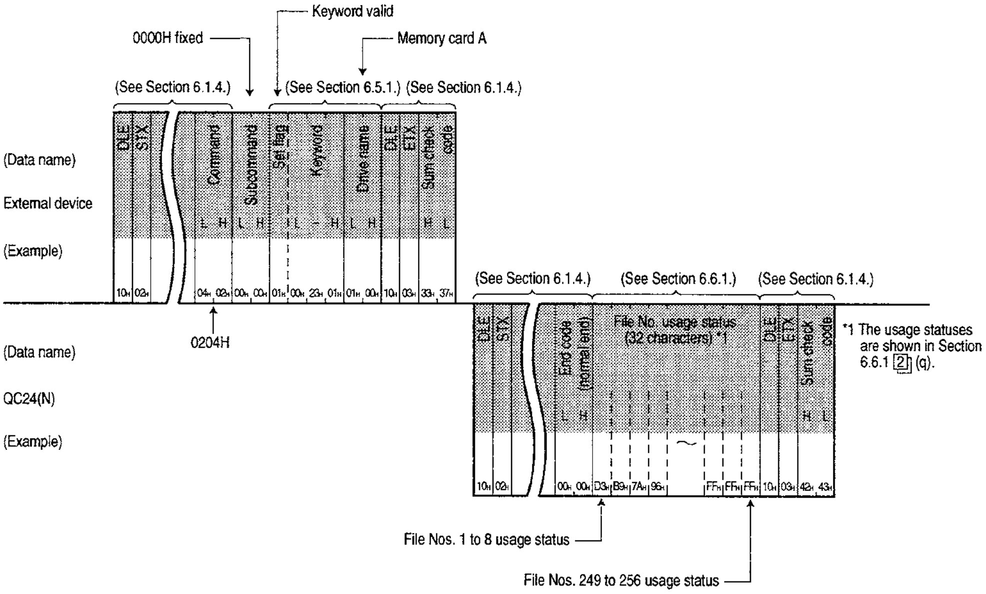
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to read the memory card A (RAM area, drive name: 01H) file No. usage status



*1 The usage statuses are shown in Section 6.6.1 [2] (q).

(b) When using binary mode format 5 to read the memory card A (RAM area, drive name: 01H) file No. usage status



POINT

When a drive memory that cannot store up to 256 files is designated, the status of file Nos. that cannot store files (insufficient portion) is made “in use” (relevant bit: 1).

6.6.5 Modifying the file information (command: 1204)

1 Modifying the file creation date (command: 1204, subcommand: 0000)

The following uses examples to describe the control procedure that modifies the date and time the designated file was last updated.

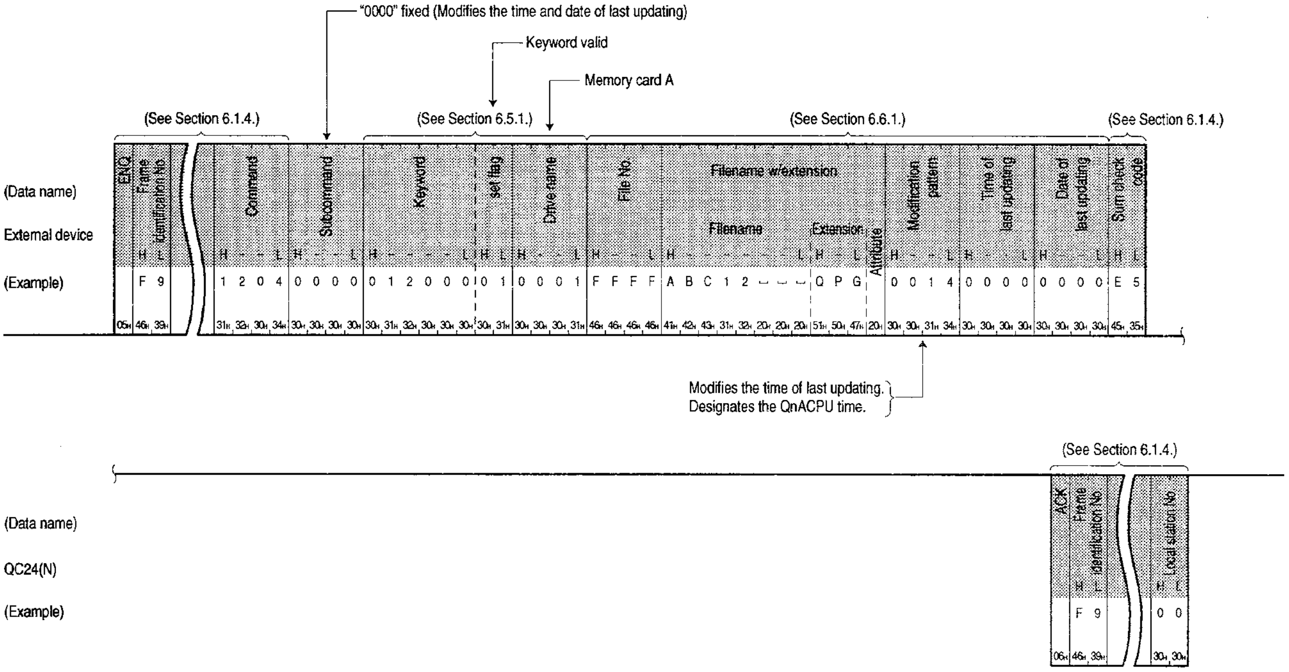
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

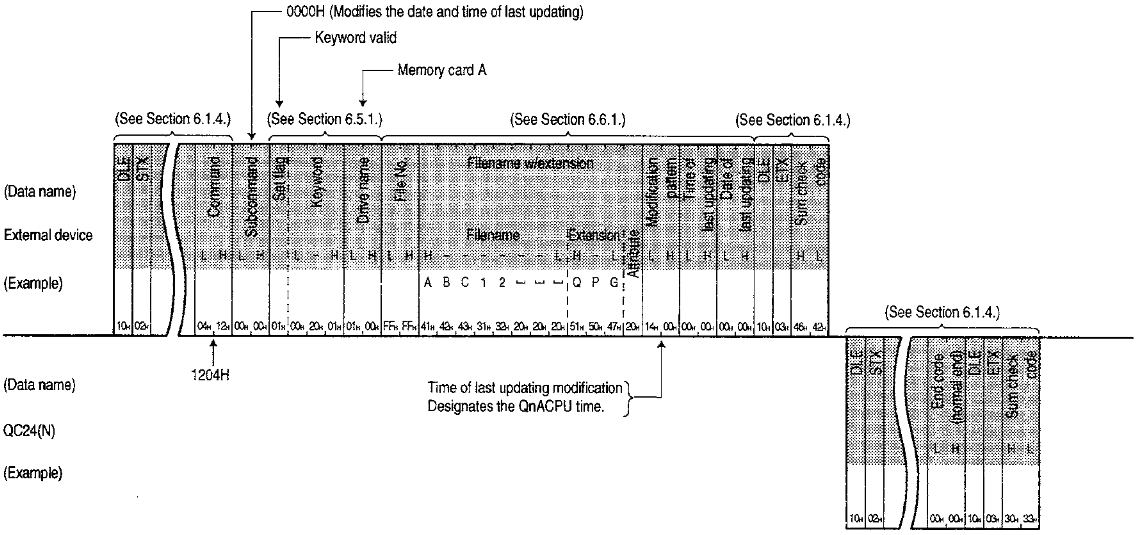
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to modify the time memory card A (RAM area, drive name: 01H) file name "ABC12.QPG" was last updated

(The file No. is unknown and the time of last updating is the QnACPU time.)



(b) When using binary mode format 5 to modify the time memory card A (RAM area, drive name: 01H) filename "ABC12.QPG" was last updated
(The file No. is unknown and the time of last updating is the QnACPU time.)



POINTS

(1) Designate, or return, the designated values within the following range.
- File No .... 1 ≤ file No. ≤ 256
- Modification pattern .... 04H, 08H, 0CH, 14H, 18H or 1CH

(2) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize an error and return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing

2 Modifying filename, attribute, and file size (command: 1204, subcommand: 0001)

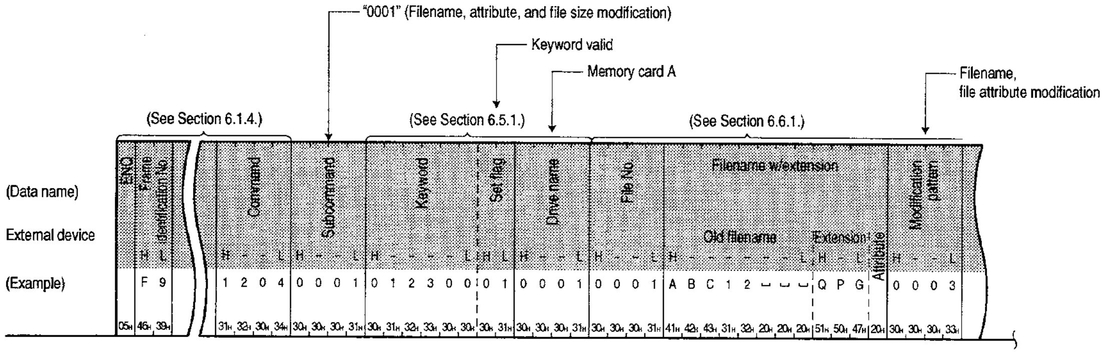
The following uses examples to describe the control procedure that modifies the filename, attribute, and file size of the designated file.

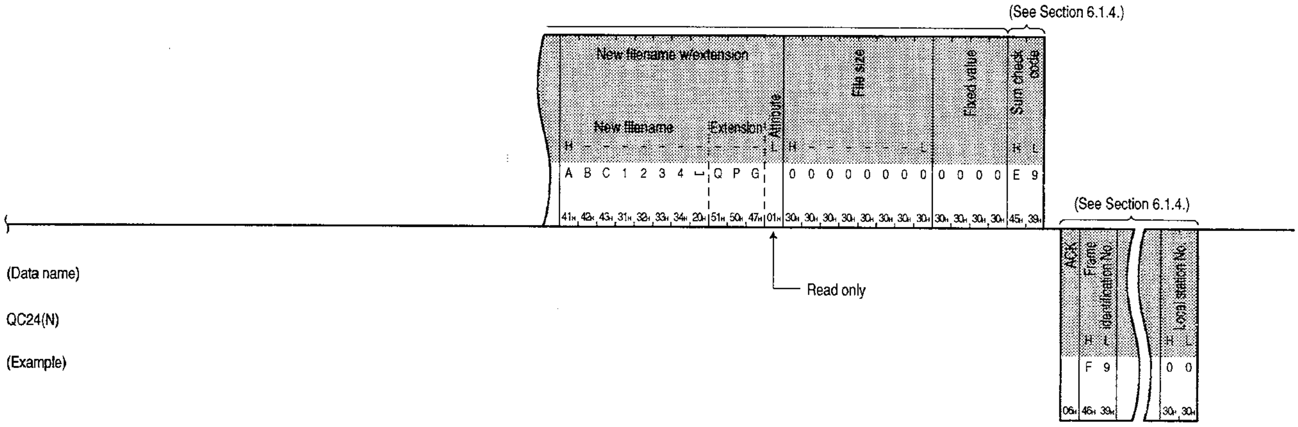
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

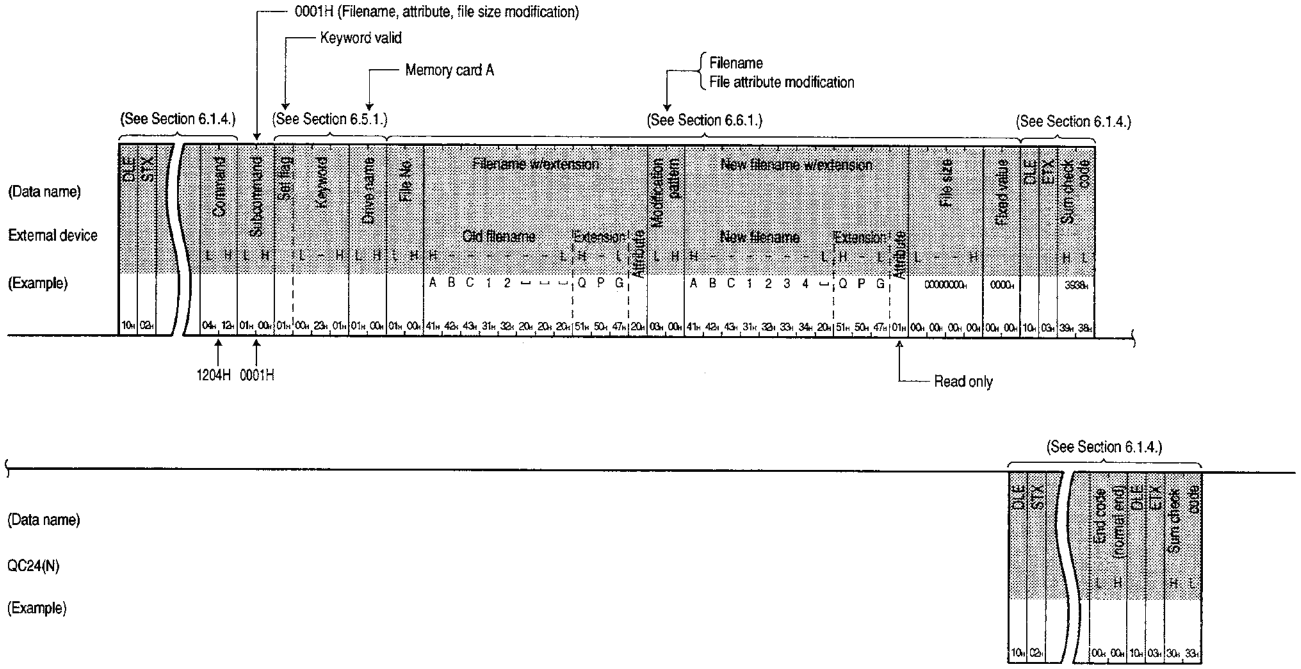
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to modify the filename and attribute of memory card A (RAM area, device name: 01H) file No.1/filename "ABC12.QPG.
(Changes the filename to "ABC1234.QPG" and the attribute to "read only".)





(b) When using binary format 5 to modify the filename and attribute of memory card A (RAM area, drive name: 01H) file No.1/filename "ABC12.QPG"
(Changes the filename to "ABC1234.QPG" and the attribute to "read only".)



POINTS

(1) Designate, or return, the designated values within the following range.
- File No .... 1 ≤ file No. ≤ 256
- Modification pattern .... 01H, 02H, 03H, 20H, 21H, 22H or 23H

(2) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize an error and return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing

(3) The attribute can only be modified between 01H (read only file) ↔ 20H (read/write disk file)

(4) The size can be modified only while the QnACPU is in the STOP state. A continuous vacant area of the designated size is necessary on the designated drive.
The vacant area can be checked using the memory usage status read function described in Section 6.5.2.

3 Batch modification of file information (command: 1204, subcommand: 0002)

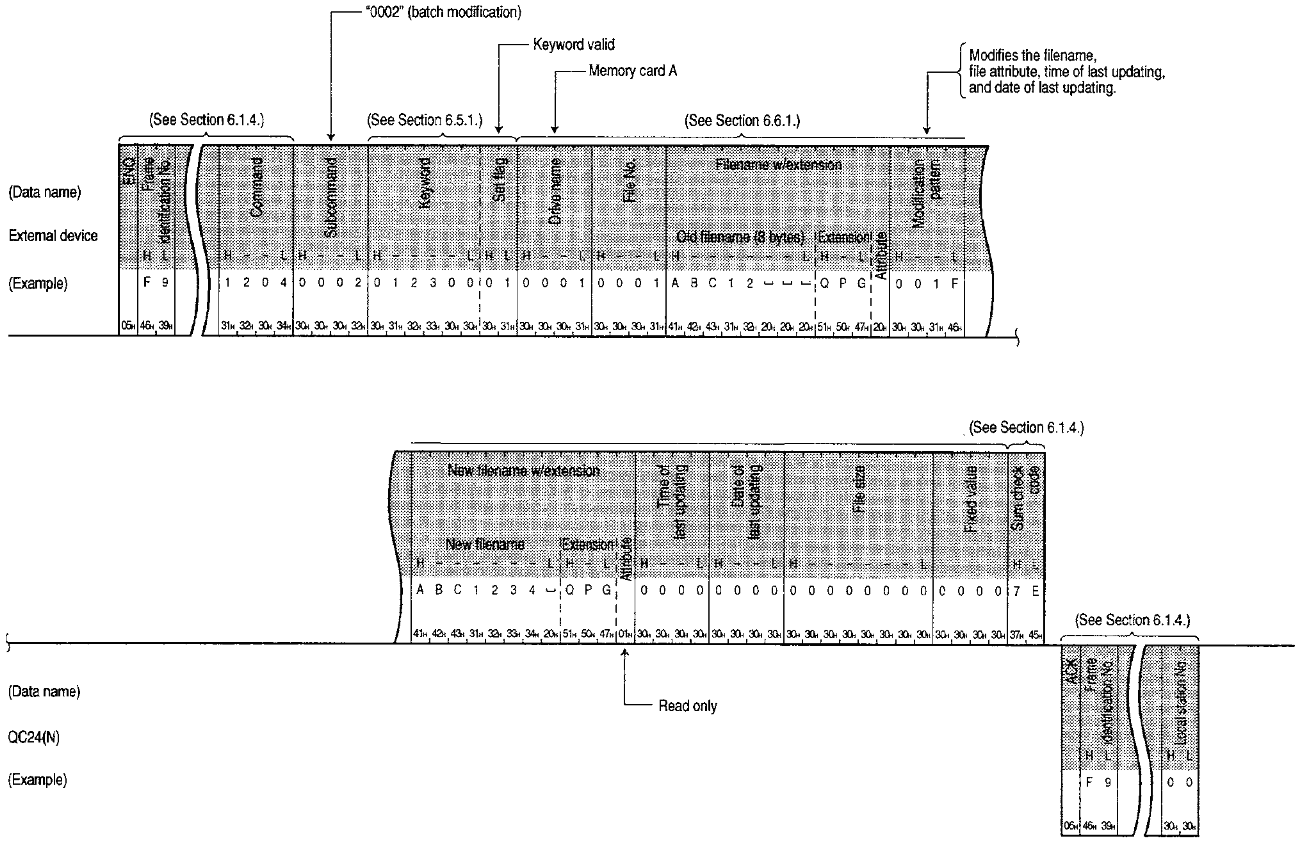
The following uses examples to describe the control procedure that batch-modifies the file information of the designated file.

[Control Procedure]

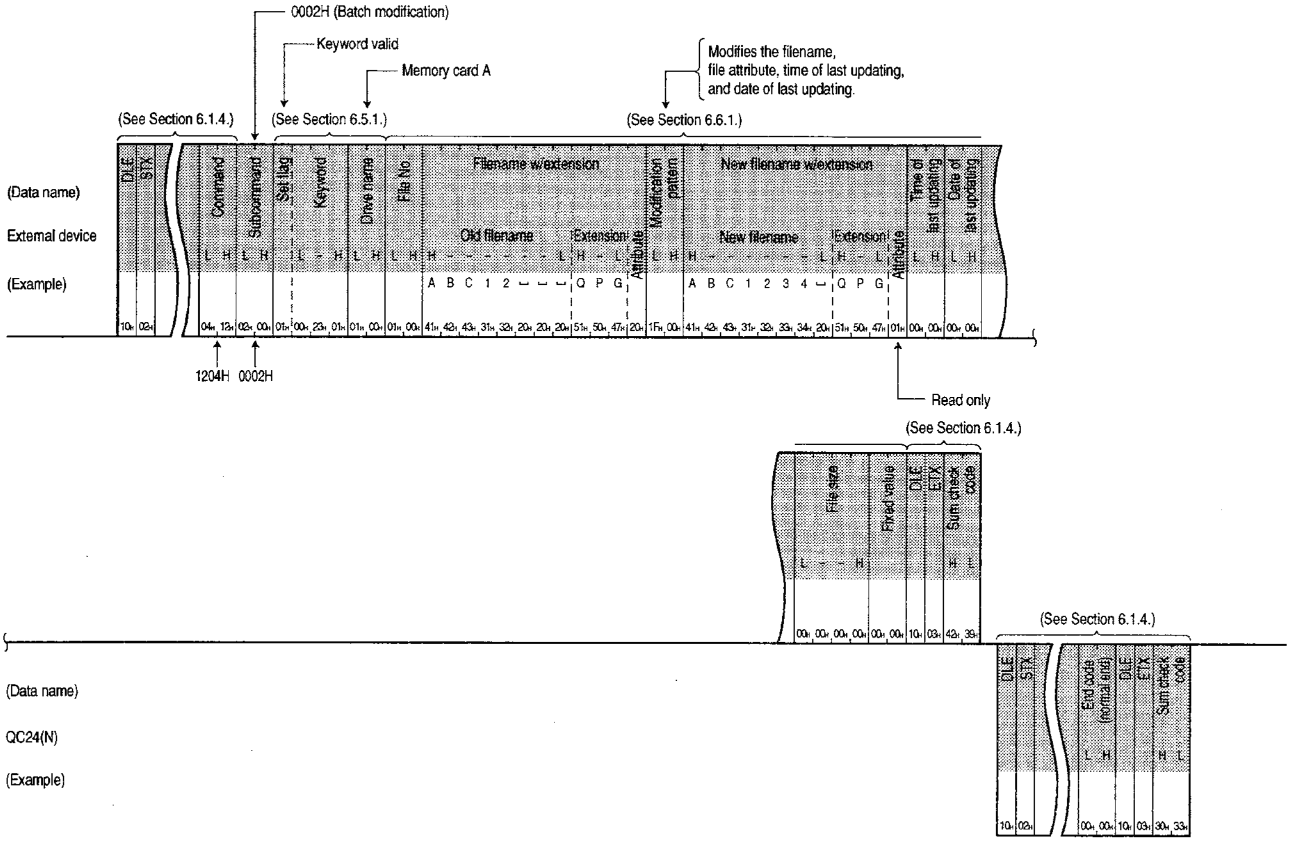
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to modify the filename, attribute, and date and time of last updating of memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG"
(The date and time of last updating use the QnACPU date and time. The file attribute is changed to "read only".)



(b) When using binary mode format 5 to modify the filename, attribute, and date and time of last updating of memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG"
(The date and time of last updating use the QnACPU date and time. The file attribute is changed to "read only".)



POINTS

(1) Designate, or return, the designated values within the following range.
- File No .... 1 ≤ file No. ≤ 256
- Modification pattern .... 01H ≤ modification pattern ≤ 3FH

(2) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize and error and will return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing

(3) The attribute can only be changed between 01H (read only file) ↔ 20H (read/write disk file).

(4) The file size can be changed only while the QnACPU is in the STOP state. A continnous vacant area of the designated size is necessary on the designated drive.
The vacant area can be checked using the memory usage status read function described in Section 6.5.2.

6.6.6 File search (command: 0203)

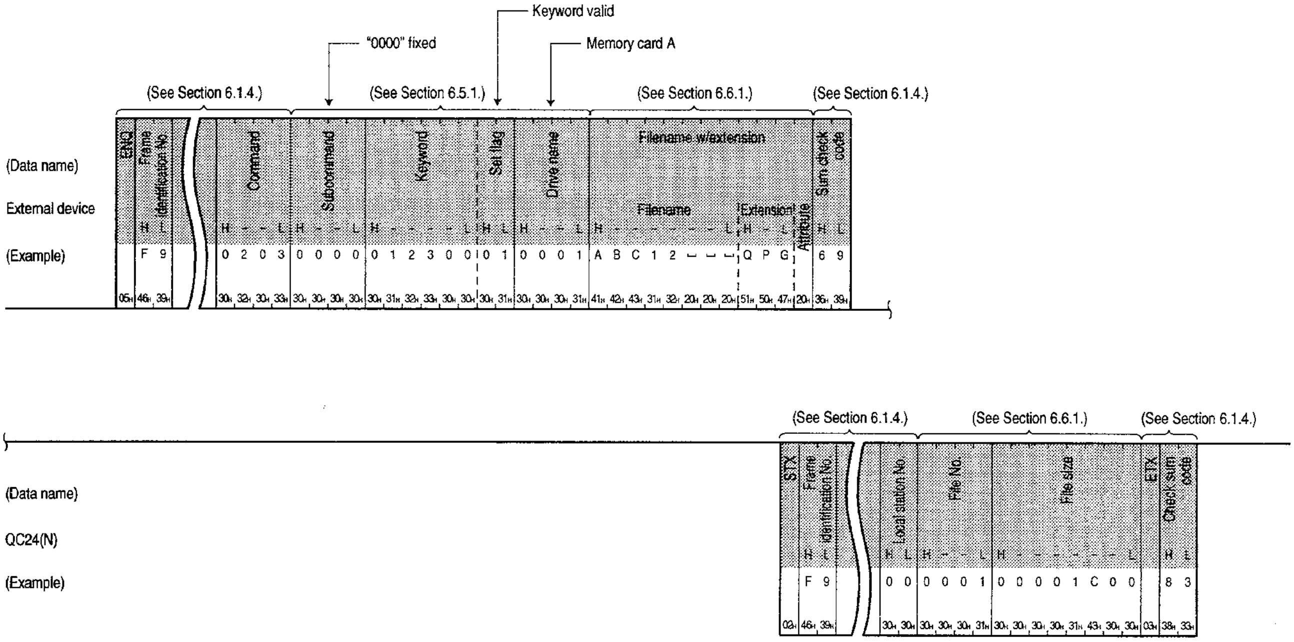
The following uses examples to describe the control function that searches for the designated files and reads the file No. and filesize if the file is found.

[Control Procedure]

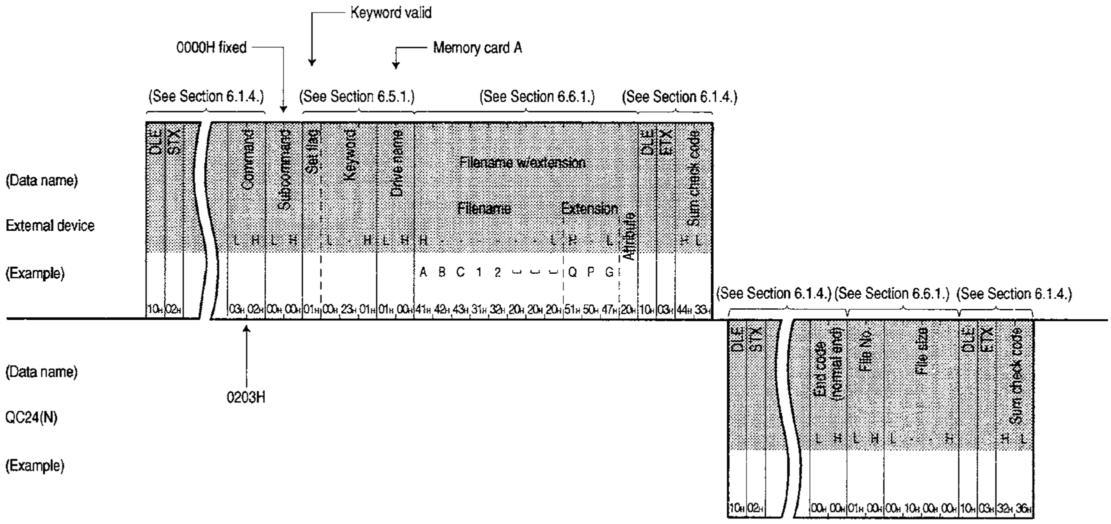
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to search for memory card A (RAM area, drive name: 01H) file name "ABC12.QPG".



2 When using binary mode format 5 to search for memory card A (RAM area, drive name: 01H) file name “ABC12.QPG”



POINT

(1) The file attributes to be read are handled as dummy data.

(2) When the designated file does not exist an error occurs and NAK text is returned.

6.6.7 Reading the contents of a file (command: 0206)

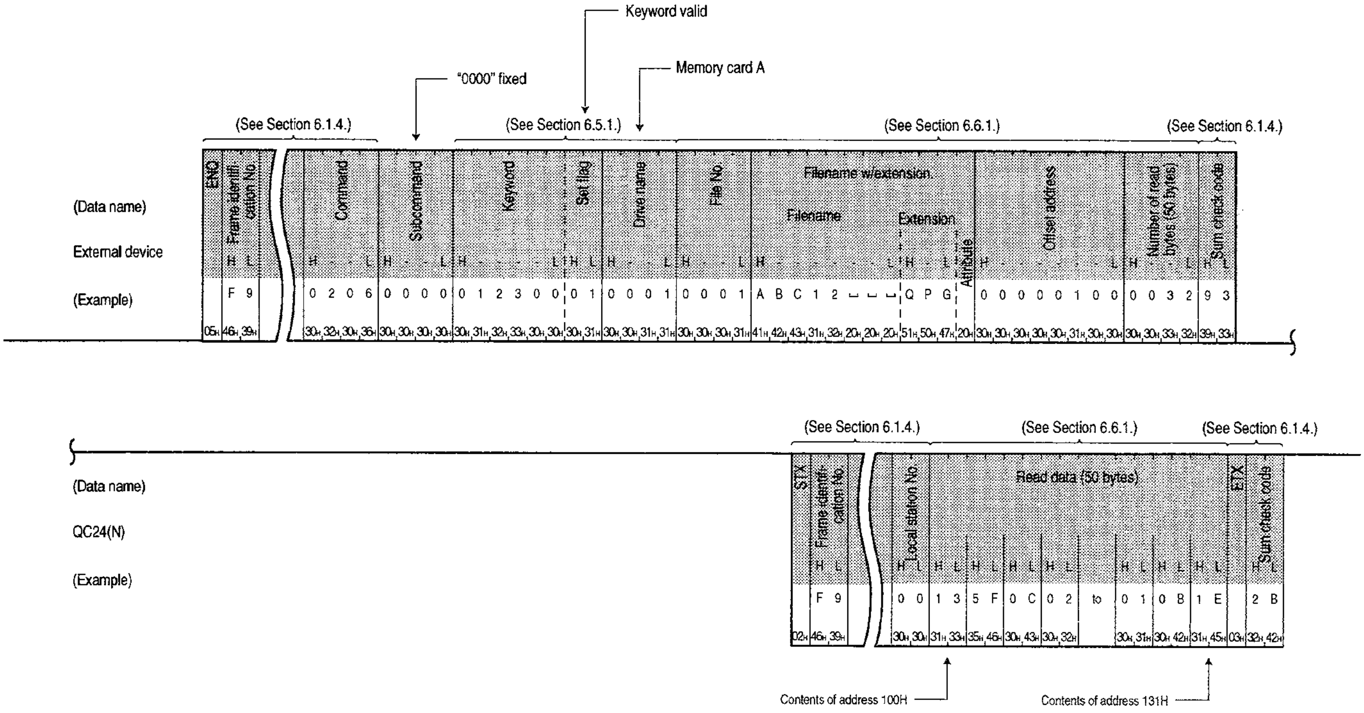
The following uses examples to describe the control procedure that reads the data written to the designated file.

[Control Procedure]

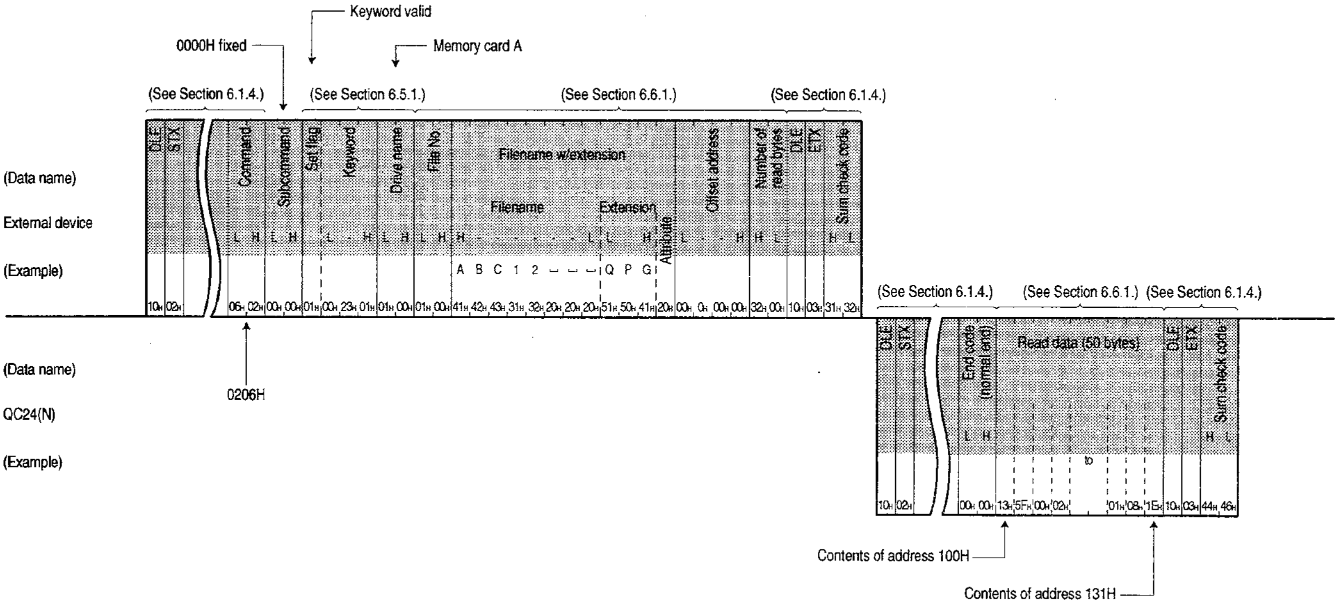
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to read the contents of the 50 bytes beginning from offset address 100H of the memory card A (RAM area drive name: 01H) file No. 1/filename "ABC12.QPG" file**



2 **When using binary mode format 5 to read the contents of 50 bytes beginning from offset address 100H of the memory card A (RAM area, drive name: 01H) file No. 1/ filename "ABC12.QPG" file**



POINTS

(1) The maximum number of bytes per read operation time when datais read is fixed. Adjust the offset address and number of read bytes and read all the data written to the designated file in two or more parts.
Also store the data read to the external device unchanged.
The file size can be checked using the following functions.
- File information table read function ...... See Section 6.6.4.
- File search function .... See Section 6.6.6.

(2) The file attributes to be read are handled as dummy data.

(3) Designate the designated values within the following range.
- File No .... 1 ≤ file No. ≤ 256
- Offset address .... Designate within the following range by even number address.
  0 ≤ address ≤ (file size – 1)
- Number of read bytes.............. 0 ≤ number of bytes ≤ 960

6.6.8 Creating a new file (filename registration) (command: 1202)

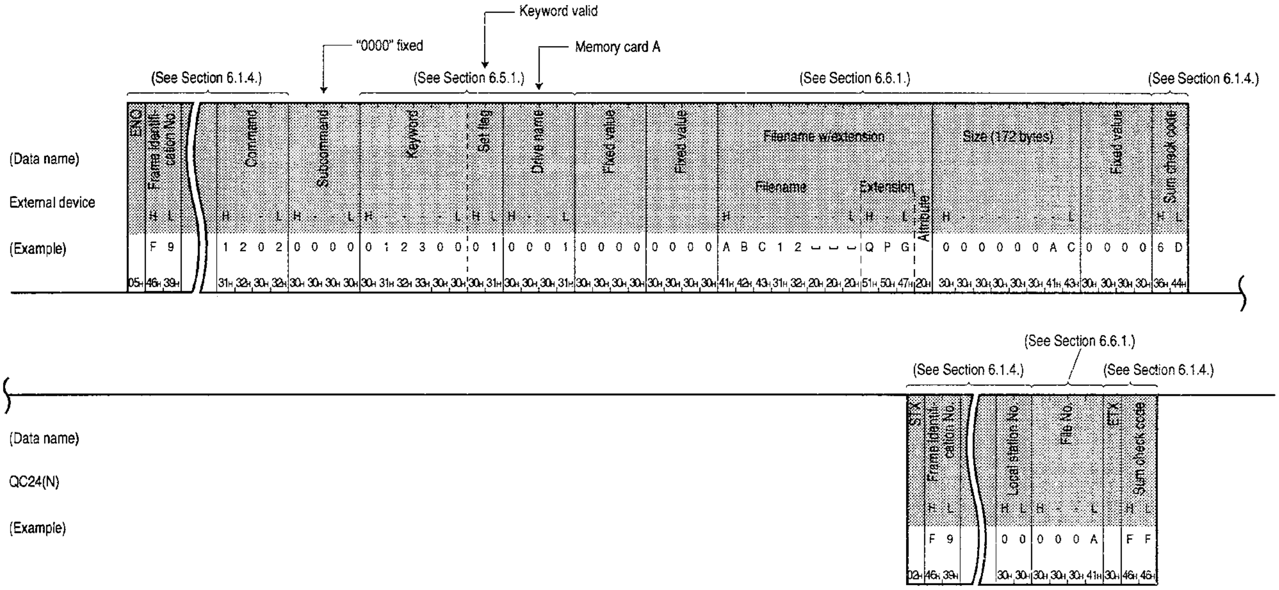
The following uses examples to describe the control function that registers a new file to, and reserves a file area on, the designated disk.

[Control Procedure]

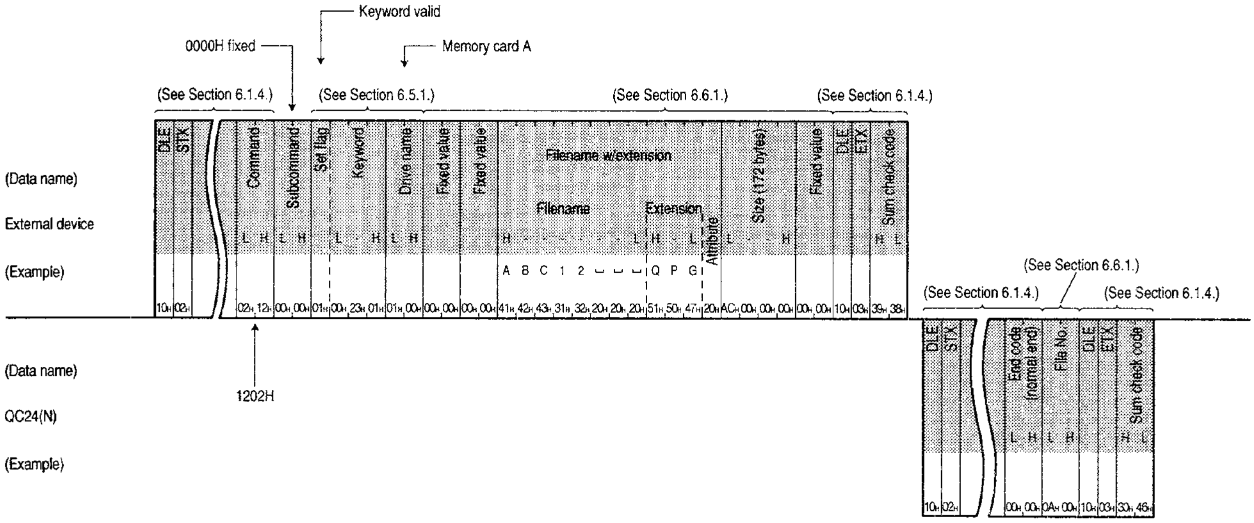
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **When using ASCII mode format 1 to register a new 172-byte file to, and reserve a file area on, memory card A (RAM area, drive name: 01H) under the filename "ABC12.QPG"**



2 When using binary mode format 5 to register a new 172-byte file to, and reserve a file area on, memory card A (RAM area, device name: 01H) under the filename "ABC12.QPG"



POINTS

(1) A new file can be created within a size that links unused clusters (see Section 6.5) on the designated drive memory.
When creating a new file, it is recommended that the addition of data later be taken into account when deciding the file size.

(2) Designate [20H] (read/write disk file) as the attribute of the new file.

(3) Use the "write to file" function (command: 1203) described in Section 6.6.9 to write data to a new file created using this function.
The contents of a file to which data was not written cannot be read.

(4) The QnACPU management time is registered as the date and time of last updating to a new file created using this function.

6.6.9 Writing to a file (command: 1203)

1 Batch write

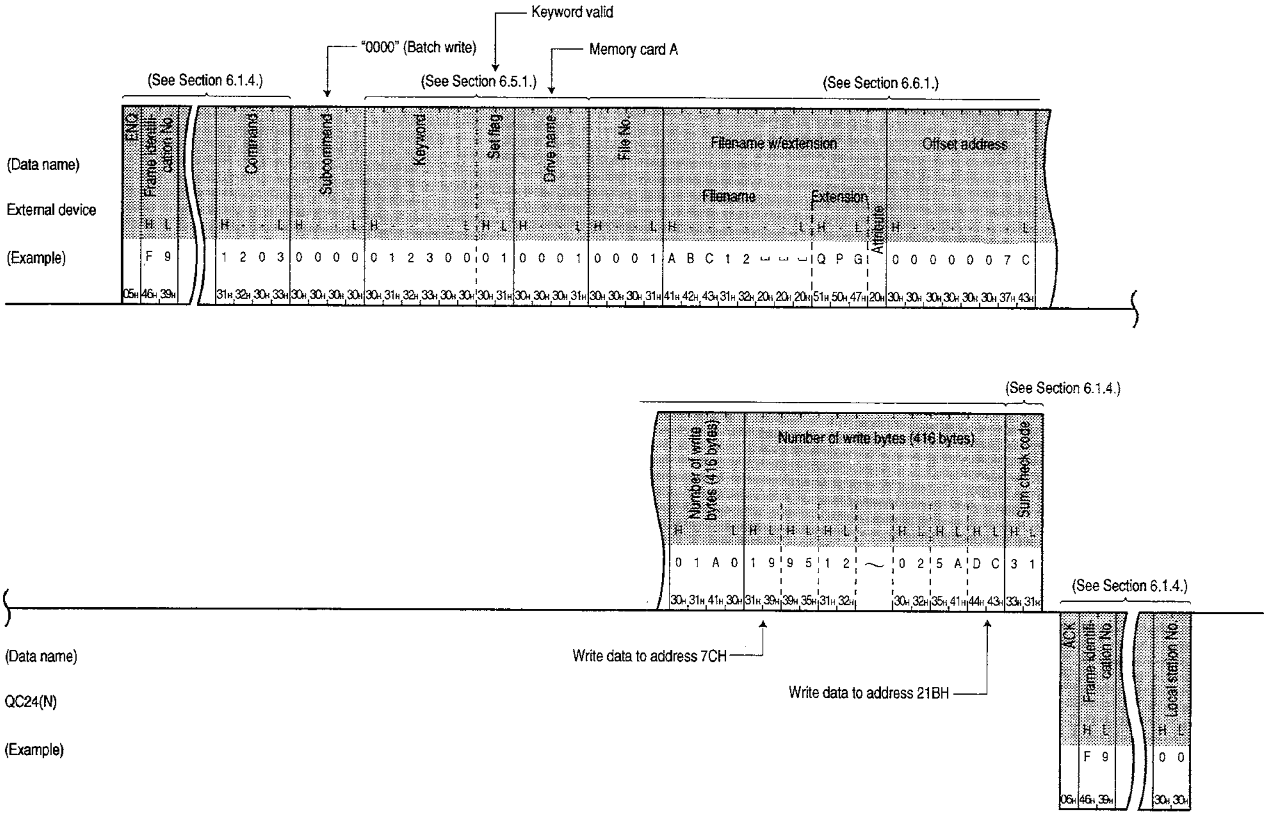
The following uses examples to describe the control procedure that writes the data of the file stored in the external device read from the QnACPU to the designated file.

[Control Procedure]

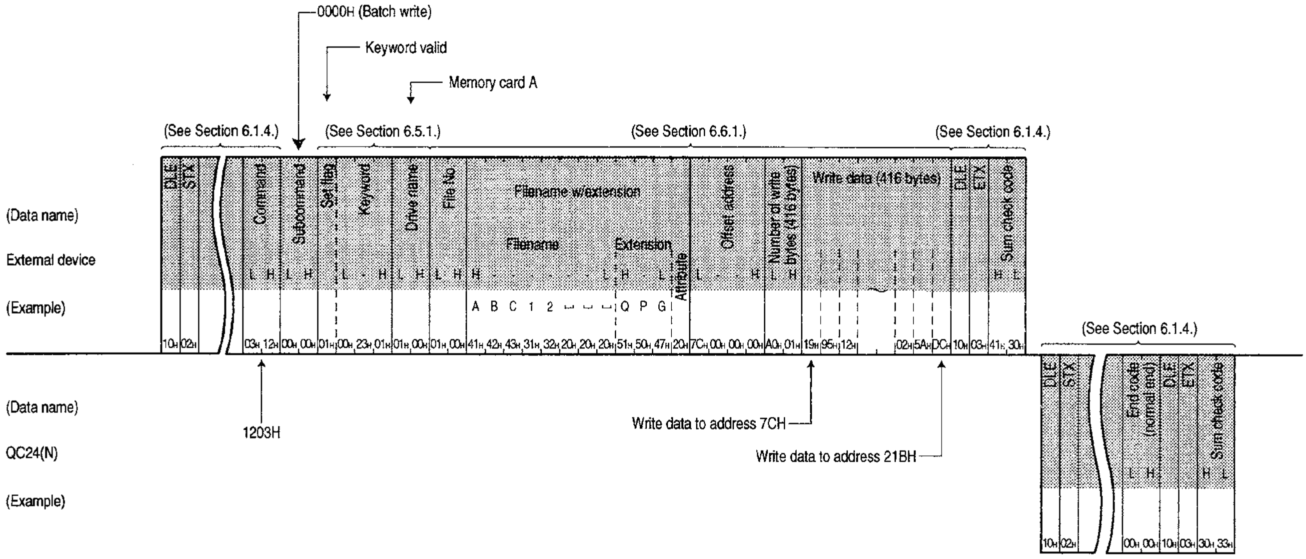
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode format 1 to write 416 bytes of data, beginning from the offset address, to the memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG" file



(b) When using binary mode format 5 to write 416 bytes of data, beginning from the offset address, to the memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG" file



POINTS

(1) The maximum number of bytes per write operation when writing data is fixed.
Adjust the offset address and number of write bytes and write all the data stored in the external device read from the QnACPU to the designated file in two or more parts.

(2) The attribute designated during file creation, etc. is valid as the attribute of the file to which the data is written.
When writing data, treat the attribute as a dummy.

(3) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize an error and will return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing.

(4) Designate the designated values within the following range.
- Offset address .... 0 ≤ address ≤ (file size – 1)
  When writing data to a drive name [00H] (internal memory) file, designate the address in multiples of 4 (for decimal, 0, 4,8....) within the range above.
  When writing data to a file other than a drive name [00H] file, designate the addresses in even number addresses (for decimal, 0,2, 4, 6, 8....) within the range above.
- Number of write bytes .... 0 ≤ number of bytes ≤ 960

2 Writing the same data (FILL)

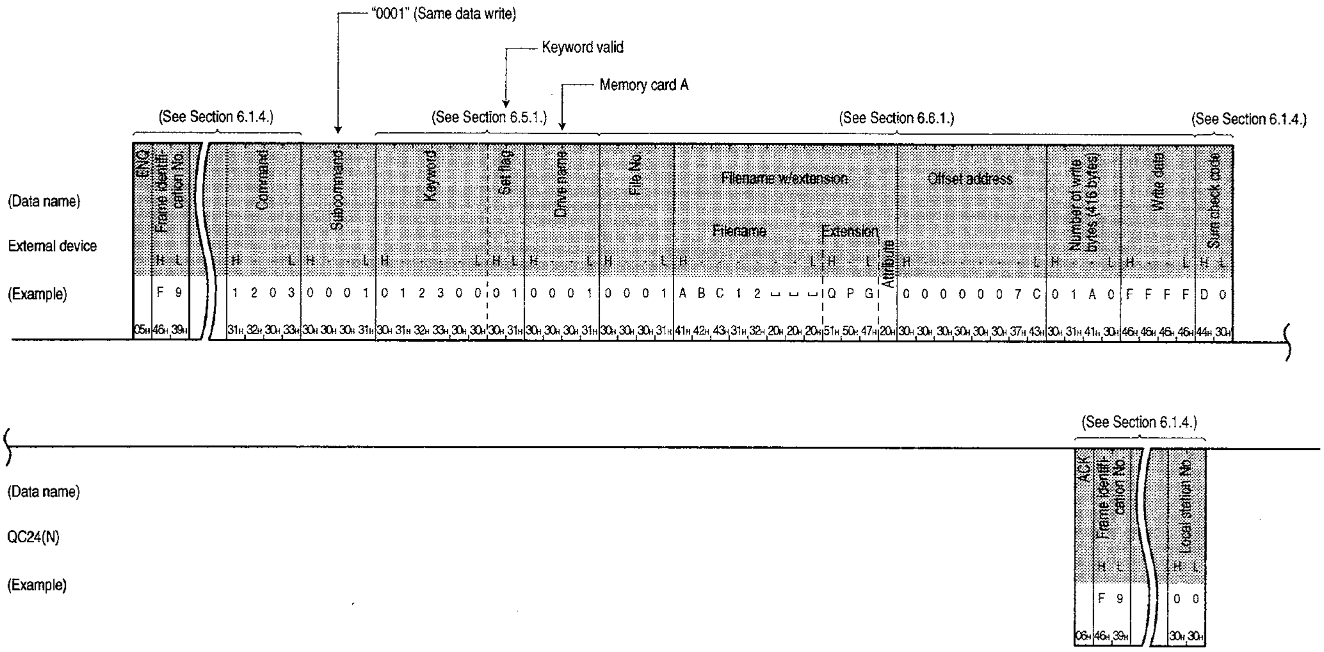
The following uses examples to describe the control procedure that write n bytes of arbitrary 1 word data to the designated file.

[Control Procedure]

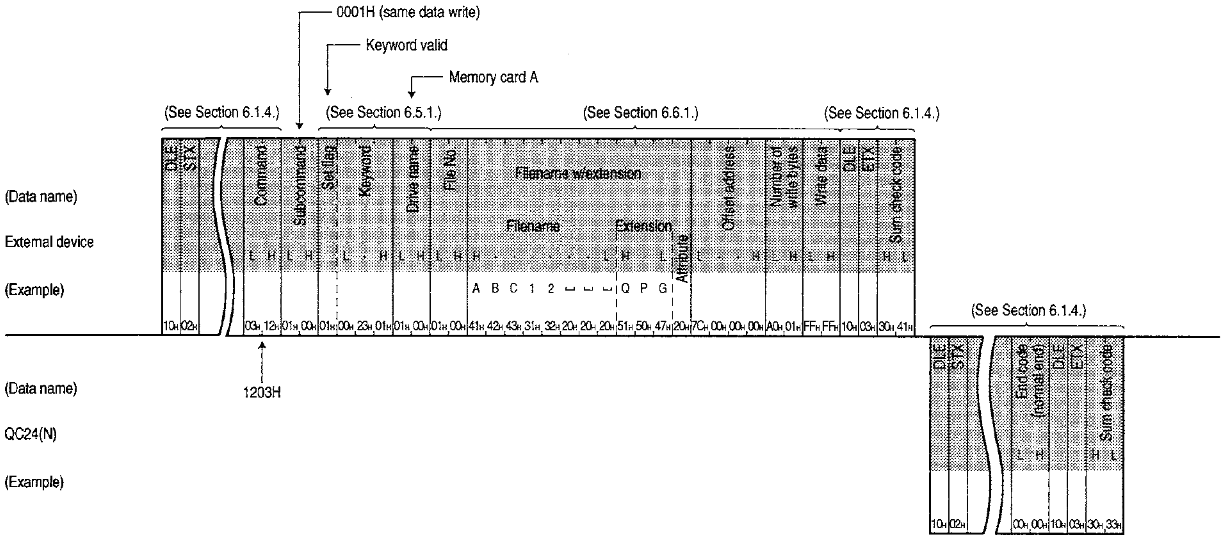
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

(a) When using ASCII mode 1 to write 416 bytes of [FFFFH], beginning from offset address 7CH, to the memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG" file



(b) When using binary mode format 5 to write 416 bytes of [FFFFH], beginning from offset address 7CH, to the memory card A (RAM area drive No.: 01H) file No. 1/filename "ABC12.QPG" file



POINTS

(1) The maximum number of bytes per write operation when writing data is fixed.
Adjust the offset address and number of write bytes and write arbitrary 1 word data within the size of the designated file in two or more parts.
Since data is written in byte units, when the size of the remaining data is 1 byte, the value of the higher byte (bits 8 to 15) of the 1 word data will not be written.

(2) The file attribute designated during file creation, etc. is valid as the attribute of the file to which the data is written.
When writing data, treat the attribute as a dummy.

(3) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize an error and return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing

(4) Designate the designated values within the following range.
- Offset address .... 0 ≤ address ≤ (file size – 1)
When writing to a file on drive name [00H] (internal memory), designate the addresses in multiples of 4 (for decimal, 0, 4,8....) within the range above.
When writing data to a file on a drive other than drive name [00H], designate the addresses in even number addresses (for decimal, 0, 2, 4, 6, 8....0) within the range above.
- Number of write bytes .... 0 ≤ number of bytes ≤ 960

6.6.10 Registering and clearing file lock (command: 0808)

The following uses examples to describe the control procedures for controlling the following processing from the QC24(N).

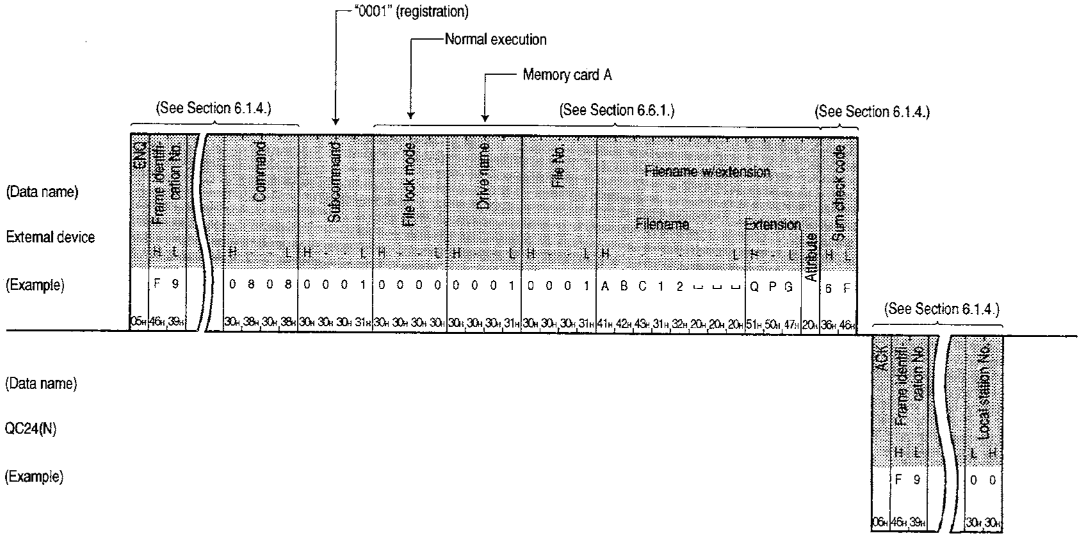
- File lock registration (Disable access from other devices)
  Registers file lock so that the contents of the file cannot be changed from another device and the same file cannot be accessed from another device while the designated file is being accessed.
- File lock clear (Enable access from other devices)
  Clears file lock of a file that was file-locked so that the same file can be accessed from other devices.

[Control Procedure]

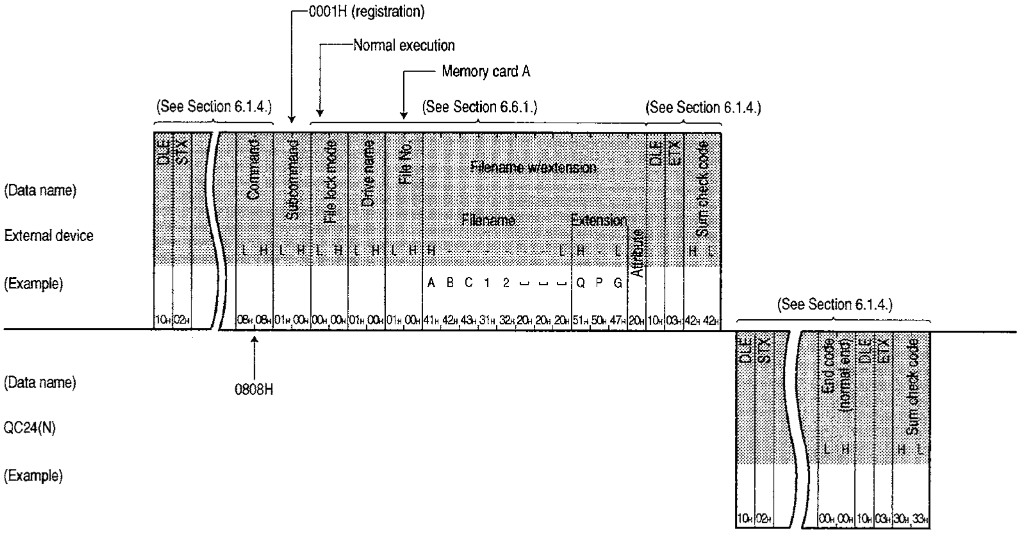
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to normally execute file lock registration for the memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG" file



2 When using binary mode format 5 to normally execute file lock registration for the memory card A (RAM area, drive name: 01H) file No. 1/filename "ABC12.QPG" file



POINTS

(1) The attribute designated during file creation, etc. is valid as the attribute of the file that is locked and cleared.
When registering and clearing file lock, treat the attribute as a dummy.

(2) When file lock is registered, the file lock registration is cleared when the QnACPU is restarted (CPU reset, etc.).

6.6.11 Copying files (command: 1206)

The following uses examples to describe the control procedure that writes (overwrites) the data written in an existing file to a new file.

[Control Procedure]

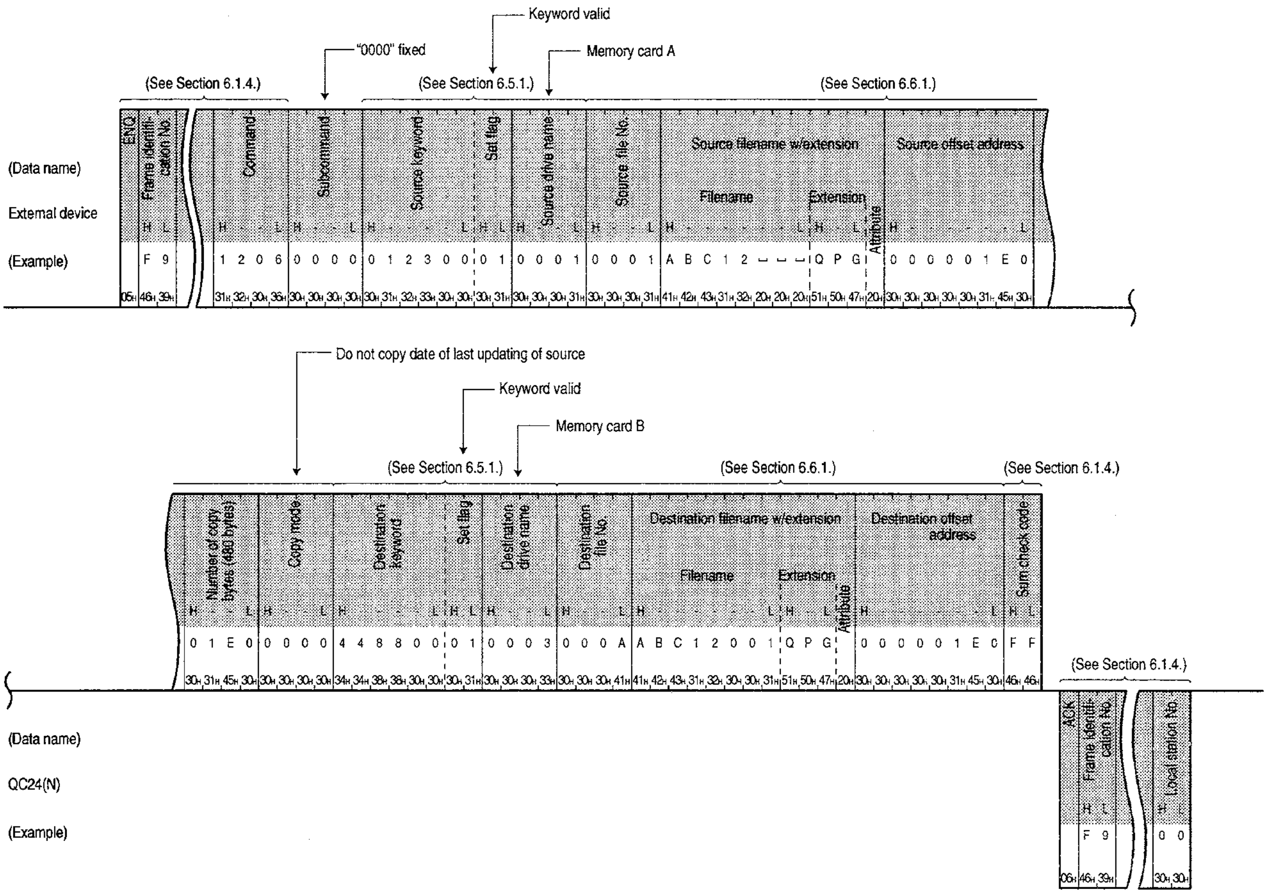
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to copy the contents of an existing file in memory card A (RAM area drive name: 01H) to anew file

Designate offset address 1E0H for both files and copy 480 bytes.

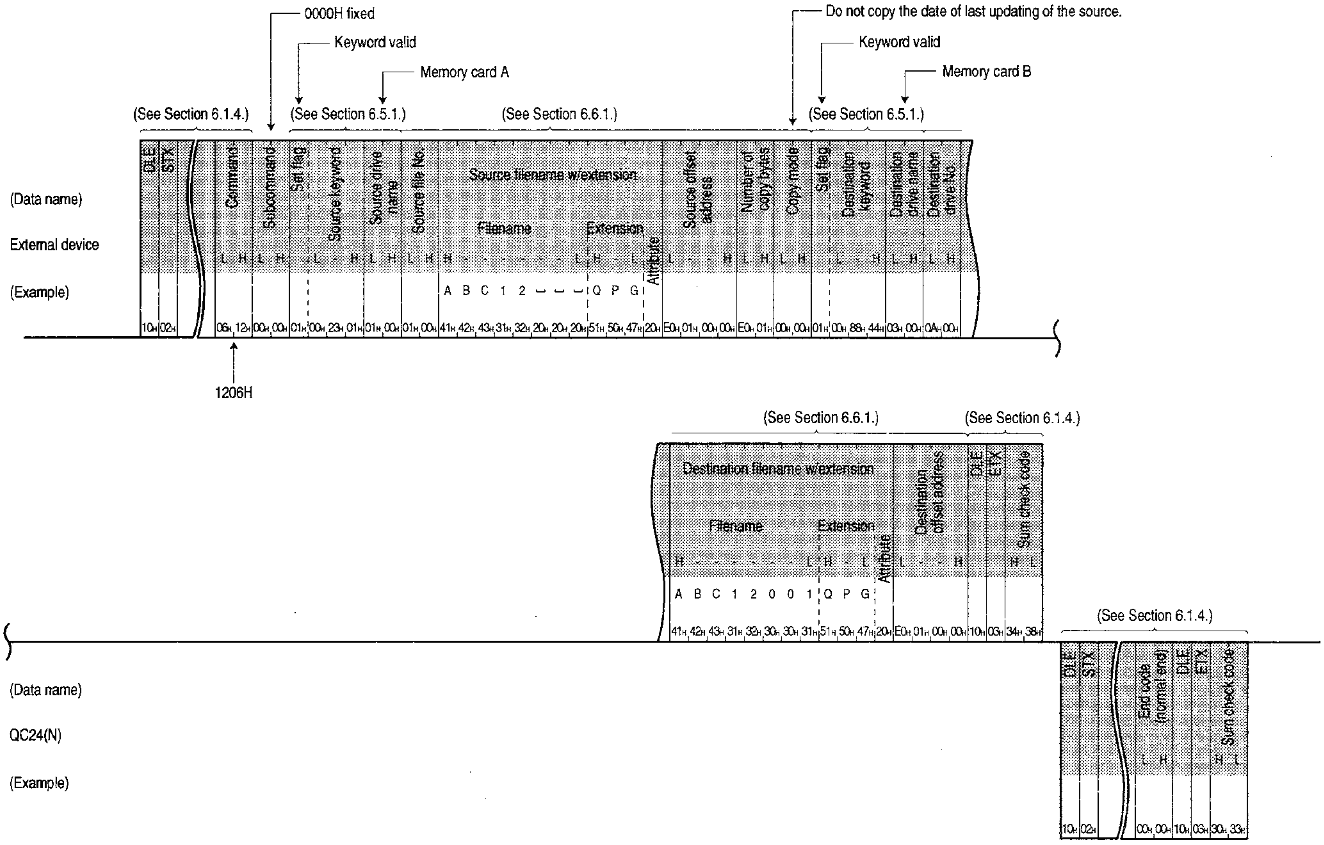
Existing file .... File No.:0001H (1), filename: "ABC12.QPG"
New file .... File No.:000AH (10), filename: "ABC12001.QPG"
(Do not copy the date of last updating of the source file.)



2 When using binary mode format 5 to copy the contents of an existing file in memory card A (RAM area, drive name: 01H) to anew file

Designate offset address 1E0H for both files and copy 480 bytes.

Existing file .... File No.: 0001H (1), filename: "ABC12.QPG"
New file .... File No.: 000AH (10), filename: "ABC12001.QPG"



POINTS

(1) The maximum number of bytes per copy operation when copying is fixed.
Adjust the offset address and copy number of bytes and write all the data written in the existing file to the new file in two or more parts.

(2) The attribute designated during file creation, etc. is valid as the attribute of the source and destination files.
When copying, treat the attribute as a dummy.

(3) If the following files are designated while the QnACPU is in the RUN state, the QC24(N) will recognize and error and return a NAK message to the external device.
- Parameters file
- Internal memory (drive name: 00H) file currently executing

(4) Designate the designated values within the following range.
- Offset address .... 0 ≤ address ≤ (file size – 1)
  When designating a drive name [00H] (internal memory) file, use addresses of a multiple of 4 (for decimal, 0, 4, 8....)
  When designating a file of a drive name other than [00H], use even number addresses (for decimal, 0, 2, 4, 6, 8....)
- Copy number of bytes .... 0 ≤ number of bytes ≤ 480

6.6.12 Deleting files (command: 1205)

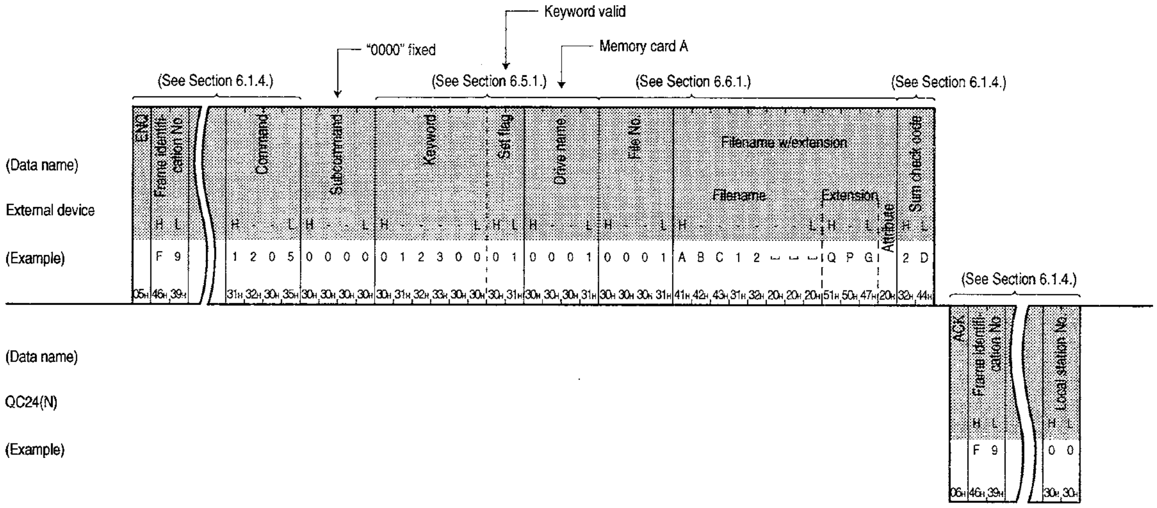
The following uses examples to describe the control procedure that deletes an existing file.

[Control Procedure]

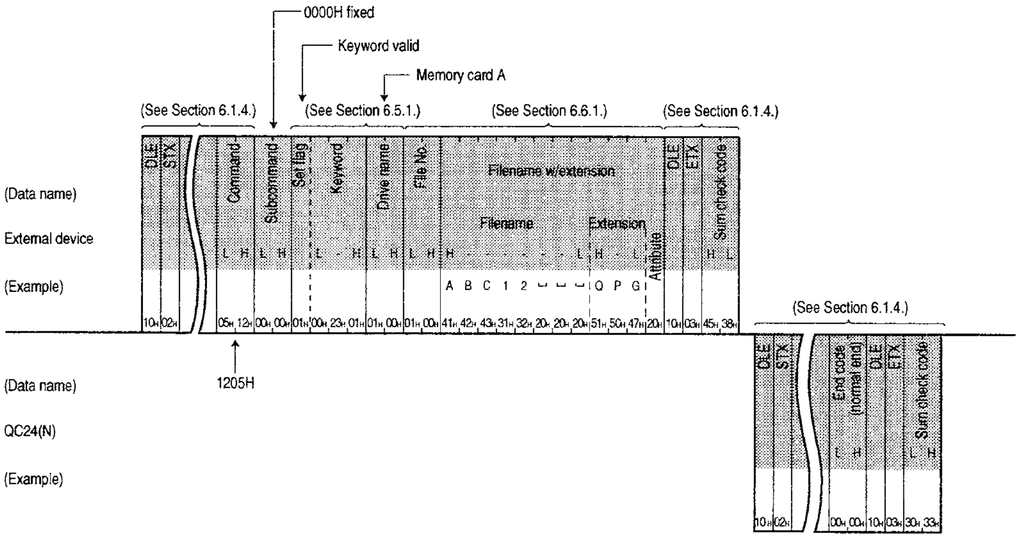
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 When using ASCII mode format 1 to delete existing memory card A (RAM area, drive name: 01H) file "ABC12.QPG"



2 When using binary mode format 5 to delete the existing memory card A (RAM area, drive name: 01H) file with the file name "ABC12.QPG"



POINTS

(1) The attribute designated during file creation, etc. is valid as the attribute of the file to be deleted.
When deleting a file, treat the attribute as a dummy.

(2) Select the file deletion timing for the entire system, including the QnACPU and related device.

(3) File-locked files cannot be deleted.
When the QnACPU is in the [RUN] state, the following files cannot be deleted.
- Program file (☐.QPG)
- Parameter file (☐.QPA)
- Boot setting file (☐.QBT)

6.7 User Frame Registration, Deletion, and Read

An external device uses this function to register (write), delete, and read user frames at the QC24(N). User frames are used to transfer data by making the beginning and end of the messages exchanged between external device and QC24(N) a data list of the format selected by the user.
This section describes how to use the commands that register, delete, and read user frames from an external device.

POINTS

(1) See Chapter 16 and the description of user file data communications functions listed below for a description of the user frame.
  - Dedicated protocol on-demand function (See Chapter 7.)
  - Non protocol data communications function (See Chapter 11.)

(2) Chapter 16 describes how to register and read user frames from the PLC CPU.

(3) This function can only be used with QC24(N) connected to an external device (including multidrop link station).
It cannot be used with other station QC24(N) connected over a data link system or network system.

(4) When an external device issues a register, delete, or read request, the data communications described in this section is carried out without waiting for PLC CPU END processing.
Transmission time T1 given in Section 5.7 remains "0" during communications using this function.

6.7.1 Commands and contents of character area

The following describes the commands and the contents of the character area (in binary mode, data area) in the control procedure when an external device registers a user frame, etc. to the QC24(N).

1 Commands

Function		Command (subcommand) *ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
				Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
							Write enable set	Write disable set	
User frame	Data registration	1610 (0000)	Registers the user frame. (data string)	80 bytes	(Unavailable)	○	○	○	6.7.2
	Registered frame deletion	1610 (0001)	Deletes the user frame of the designated frame No.	(1 frame)					
	Registered frame read	0610 (0000)	Reads the registered frame of the designated frame No.	80 bytes					6.7.3

○ in the PLC CPU state column in the table above indicates that execution is possible.

2 **Contents of character area**

The following describes the contents of the character area when an external device registers, deletes, or reads a user frame at the QC24(N).

(a) Frame No.

This data specifies the user frame number to be registered, deleted, or read.

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Example) When the user frame number is 3E8H (frame registered by the user)
The user frame number is converted to "03E8" and sequentially transmitted from "0".

② Data communications in binary mode
The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The frame No. designated value and designation contents are shown below. Values other than these cannot be designated.

Designated value	Contents	Registration destination
1H to 3E7H	Default registration frame	QC24(N) OS ROM (Can only be read)
3E8H to 4AFH	User frame	QC24(N) EEPROM (Can be read, written, and deleted)
8001H to 801FH	User frame	QC24(N) buffer memory (addresses 1800H to 1FF6H) (Can be read, written, and deleted)

(b) Registration data byte count

This data specifies the number of bytes of the registration data.
When the user frame contains variable data (control data for replacing part of the user frame with a sum check code, etc.), this data is different from the frame byte count described below.
See Chapter 16 for the data list and byte count during registration and the frame byte count during communications.

① Data communications in ASCII mode
The value 0H (value designated during deletion) or 1H to 50H (1 to 80) is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

(Example) When the byte count is 10
The 10 is converted to "000A" and sequentially transmitted from the first "0".

② Data communications in binary mode
A 2-byte value indicating the byte count 0H (when designated during deletion) or 1H to 50H (1 to 80) is sequentially transmitted from the Low byte (L: bits 0 to 7).

(c) Frame byte count

This data designates the number of bytes of the frame to be registered or read.
The variable data part is calculated with the 2-bytes of FFH + ☐H as 1 byte.

① Data communications in ASCII mode
The value 0H (value designated during deletion) or 1H to 50H (1 to 80) is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
A 2-byte value indicating byte count 0H (when designated during deletion) or 1H to 50H (1 to 80) is sequentially transmitted from the Low byte (L: bits 0 to 7).

(d) Registration data

This data designates the data list of the frame to be registered to the QC24(N). It is a list of data (maximum 80 bytes) corresponding to the read/write byte counts described in item (b) above.
When deleting a registered user frame, you do not have to designate the registration data.

① Data communications in ASCII mode
The data codes making up the frame are converted to 2-digit (hexadecimal) ASCII codes and transmitted from the most significant digit.

(Example) Designating a frame to transmit/receive ENQ + module station No. + blank (space)
The registration data is converted to "05FF0120" and sequentially transmitted from the first "0".

② Data communications in binary mode

The data codes making up the frame are sequentially transmitted from the head data.

(Example) Designating a frame to transmit/receive END + module station No. + blank (space)
The registration data becomes 05H, FFH, 01H, and 20H and is sequentially transmitted from 05H.

6.7.2 Registering and deleting user frames (command: 1610)

The following uses examples to describe the control procedure when registering a user frame to the QC24(N).

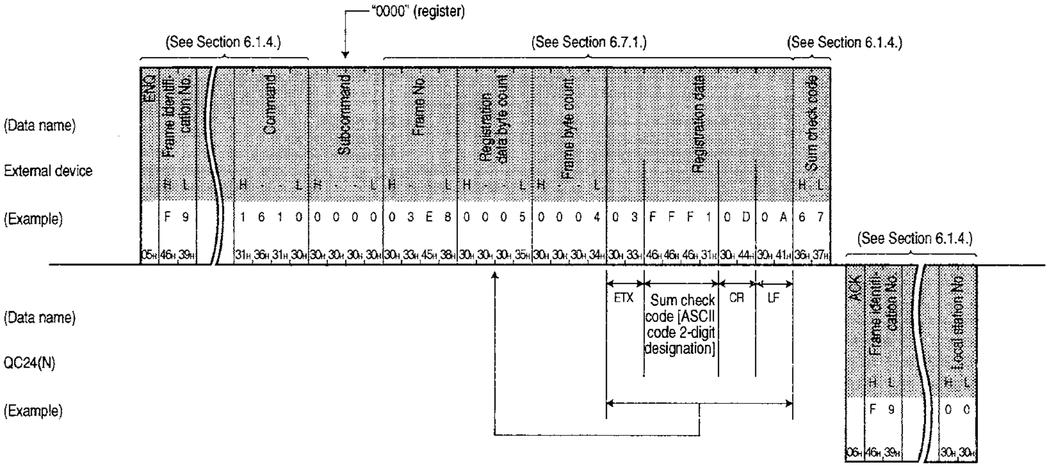
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

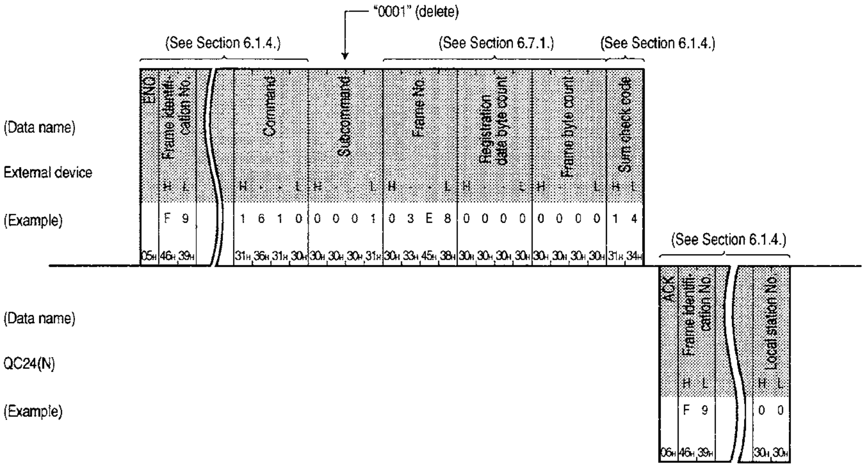
To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **Using ASCII mode format 1 to register and delete a user frame**

(a) Registering a frame to transmit/receive ETX + sum check code + CR + LF with frame No. 3E8H (codes and list after registration: 03H, FFH, F1H, 0DH, 0AH)
When the sum check code is made a character string created by converting the value of the lower byte (8 bits) of the sum to a 2-digit (hexadecimal) ASCII code with the data of the part with the header frame removed as binary data.

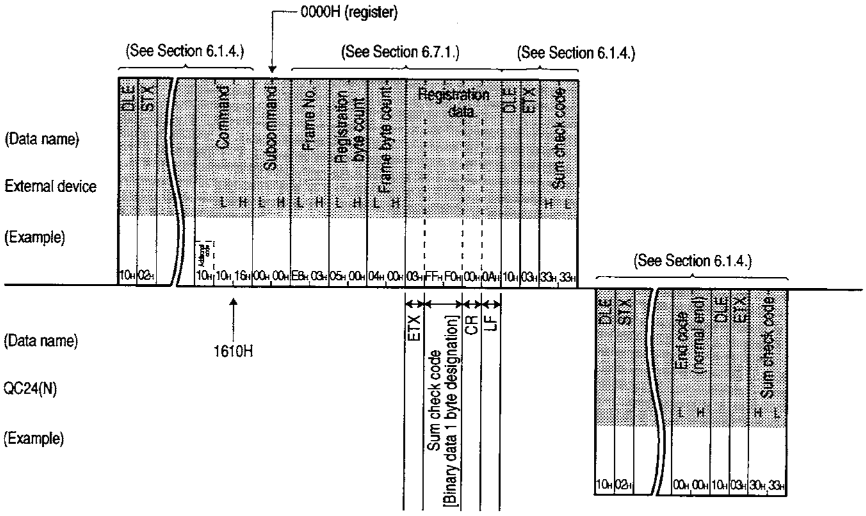


(b) Deleting register user frame No. 3E8H

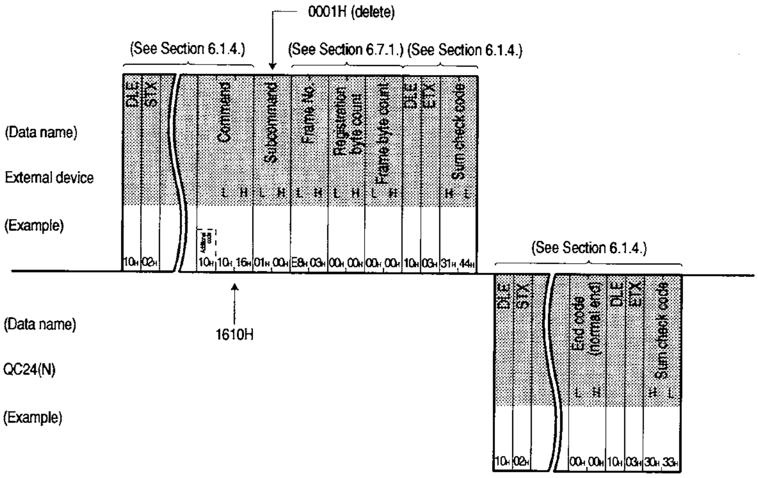


2 Using binary mode format 5 to register and delete user frames

(a) Deleting frame No. 3E8H to transmit/receive ETX + sum check code + CR + LF (Code and list after registration: 03H, FFH, F0H, 0DH, 0AH)
When the value of the lower byte (8 bits) of the sum, with the data of the part with the header frame removed as binary data, is used unchanged as the sum check code.



(b) Deleting registered user frame No. 3E8H



POINTS

(1) If a frame No. which was registered as a user frame is designated during registration, the old registered contents are invalid and the new registered contents are valid.
If a frame No. without a user frame registered is designated during deletion, the QC24(N) will recognize and error and return a NAK message to the external device.

(2) Designate the designated values within the following range.
- When registering to QC24(N) EEPROM........... 3E8H ≤ frame No. ≤ 4AFH
- When registering to QC24(N) buffer memory... 8001H ≤ frame No. ≤ 801FH

6.7.3 Reading user frames (command: 0610)

The following uses examples to describe the control procedure that reads the registered contents (registered data list) of a user frame from the QC24(N).

[Control Procedure]

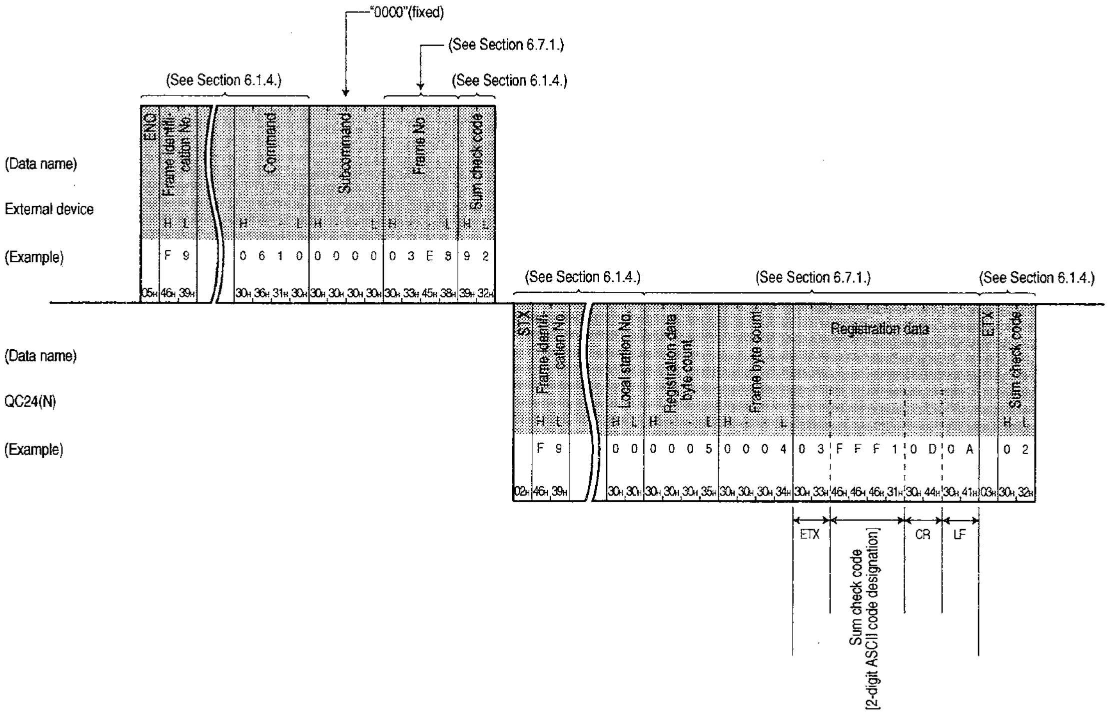
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **Using ASCII mode frame 1 to read the contents registered using frame No. 3E8H**

The registered contents are frames for transmitting and receiving ETX + sum check code + CR + LF.

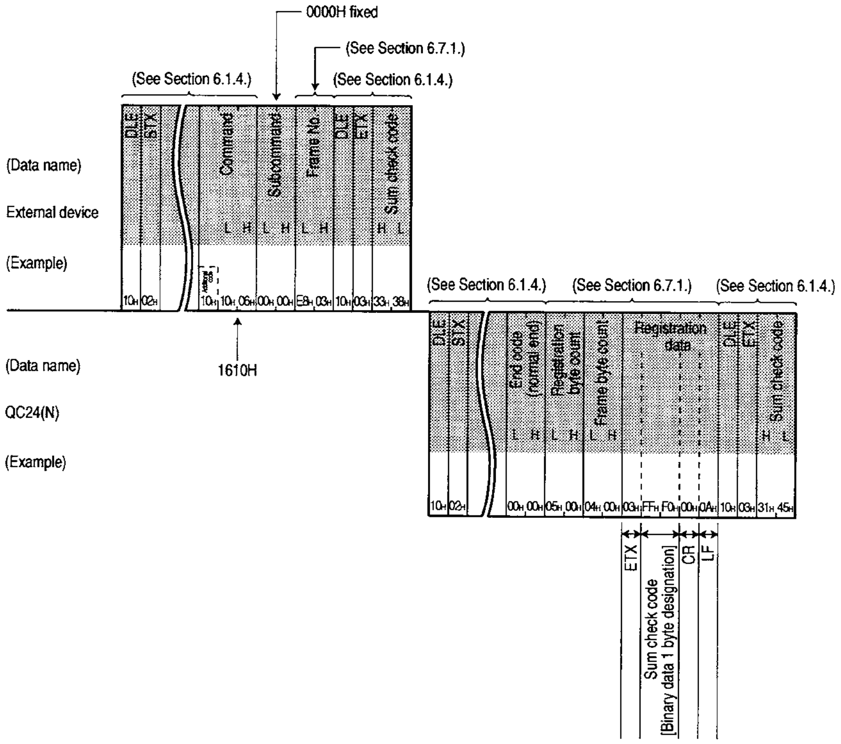
When designated so that the sum check code is made a character string generated by converting the value of the lower byte (8bits) of the result of addition with the data of the part with the header frame removed as binary data to a 2-digit (hexadecimal) ASCII code.



2 Using binary mode format 5 to read the contents registered using frame No. 3E8H

The registered contents are frames for transmitting and receiving ETX + sum check code + CR + LF.

The value of the lower byte (8 bits) of the result of addition with the data of the part with the header frame removed as binary data is used unchanged to designate the sum check code.



POINTS

(1) If a frame No. without a user frame registered is designated, the QC24(N) will recognize an error and return a NAK message to the external device.

(2) Designate the designated values within the following range.
- Default registration frame registered in QC24(N) OS ROM.... 1H ≤ frame No. ≤ 3E7H
- User frame registered in QC24(N) EEPROM .... 3E8H ≤ frame No. ≤ 4AFH
- User frame registered in QC24(N) buffer memory .... 8001H ≤ frame No. ≤ 801FH

6.8 Global Function

The "global function" turns global signals X (n+1) A/X (n+1) B (see Section 3.4) of a QC24(N) equipped station PLC CPU connected to an external device over a multidrop link ON/OFF.
This function is used by emergency instructions, simultaneous starting, data communications enable/disable interlock signal, etc. for the PLC CPU.
The following uses examples to describe the control procedure when using the global function.

POINTS

(1) When the A compatible frame GW command was used, the global signal (input signal) X (n+1) A or X (n+1) B of the QnACPU+QC24(N) station interface that received the GW command is turned ON/OFF.
(Example) When a GW command was received from the QC24(N) CH1 interface, the QC24(N) turns X (n+1) A ON/OFF.

(2) When the global function is used with an ACPU + QC24(N) station connected over a multidrop link, the ACPU Xn2 signal is turned ON/OFF.

(3) When the PLC CPU is restarted after the global signal was turned ON/OFF, the global signal is turned OFF.

(4) The function can only be used with QnACPU + QC24(N) stations (including multidrop link stations) connected to an external device.
Other QnACPU + QC24(N) stations connected over a data link system or network system cannot use this function.

6.8.1 Commands and contents of character area

The following describes the commands and the contents of the character area (in binary mode, data area) in the control procedure when an external device turns the global signals to a QC24(N) equipped PLC CPU ON/OFF.

1 Commands

Function		Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
				Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
							Write enable set	Write disable set	
Global	Global signal OFF	1 6 1 8 (0 0 0 0)	Turns off the global signal to the QnACPU of the designated QC24(N) equipped station.	(1 station/ all stations)	(Unavailable)	○	○	○	6.8.2
	Global signal ON	1 6 1 8 (0 0 0 1)	Turns on the global signal to the QnACPU of the designated QC24(N) equipped station.						

○ in the PLC CPU State column in the table above indicates that execution is possible.

2 Contents of character area

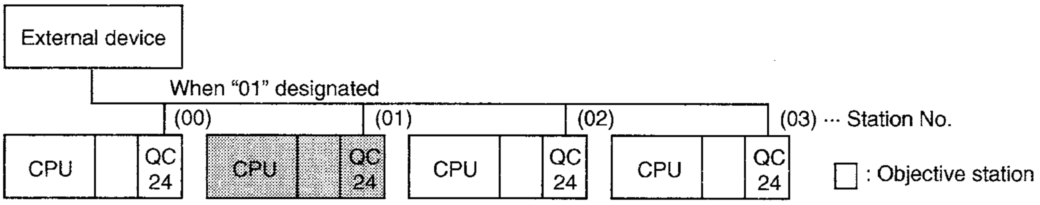
The following describes the contents of the global signal designation data of the character area when an external device turns the global signal ON and OFF.

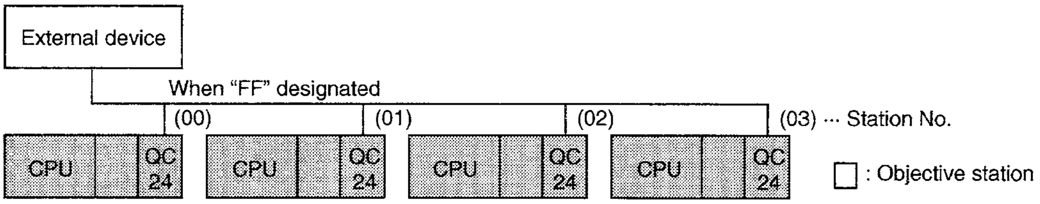
(a) Station No.

Designates the station No. of the station whose global signal is to be turned ON or OFF by the external station.
Designate one of the following.

Designated value		Global function processing
ASCII mode	Binary mode	
"00" to "1F"	00H to 1FH	Turns the global signal of only the designated station in a multidrop link ON/OFF.
"FF"	FFH	Turns the global signal of all the stations in a multidrop link ON/OFF

(Example)





QC24: QC24, QC24N

(b) Global signal designation

This data tells the QnACPU which global signal to turn ON/OFF.

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The global signal designation designated values and designation contents are shown below. Other values cannot be designated.

Designated value	Designation contents
0000H	Turns the global signal of the interface that received the global function command ON/OFF • When the command was received from the CH1 interface, X (n+1) A is turned ON/OFF • When the command was received from the CH2 interface, X (n+1) B is turned ON/OFF
0001H	Turns X (n+1) A ON/OFF without regard to the interface that received the global function command.
0002H	Turns X (n+1) B ON/OFF without regard to the interface that received the global function command.

6.8.2 Global function control procedure (command: 1618)

The following uses examples to describe the control procedure that turns the global signals to the PLC CPU ON/OFF from an external device.

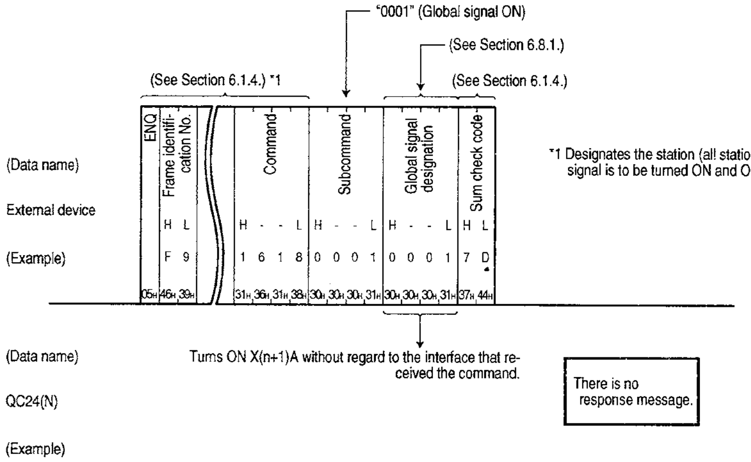
[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

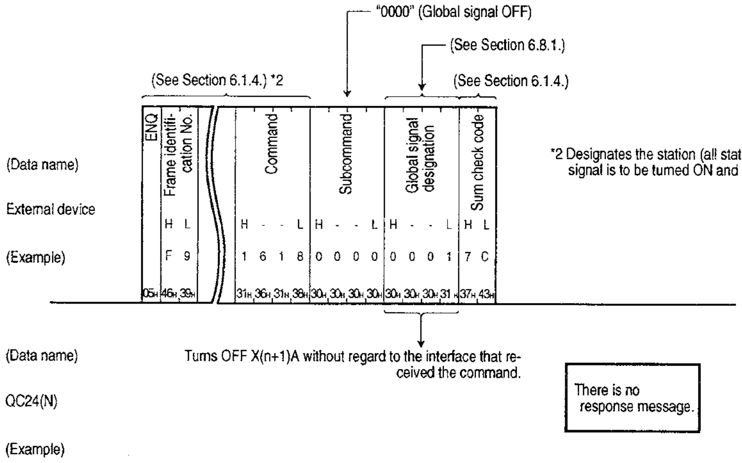
1 Using ASCII mode format 1 to turn the global signals ON and OFF

(a) Turning ON global signal X (n+1) A of all the stations in a multidrop link



*1 Designates the station (all stations/designated station only) whose global signal is to be turned ON and OFF by station No. (See Section 6.8.1 2 .)

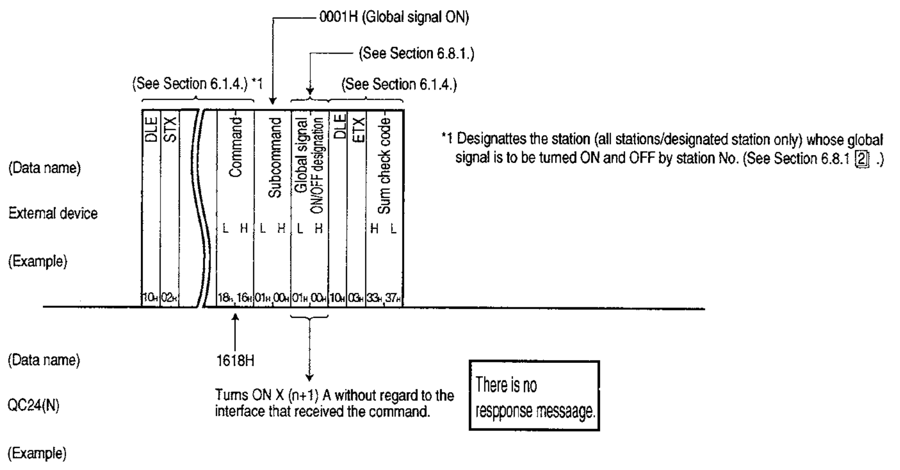
(b) Turning OFF global signal X (n+1) A of all the stations in a multidrop link



*2 Designates the station (all stations/designated station only) whose global signal is to be turned ON and OFF by station No. (See Section 6.8.1 2 .)

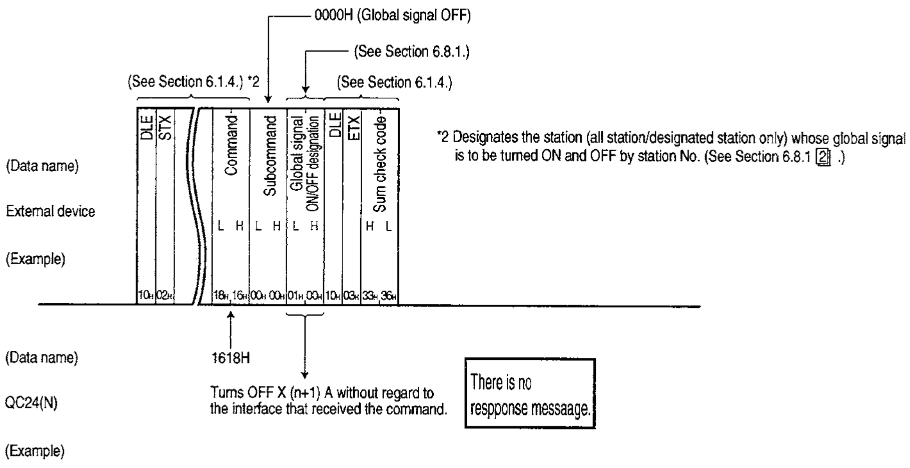
2 Using binary mode format 5 to turn global signal ON/OFF

(a) Turning ON global signal X (n+1) A of all the stations in a multidrop link



*1 Designattes the station (all stations/designated station only) whose global signal is to be turned ON and OFF by station No. (See Section 6.8.1 2 .)

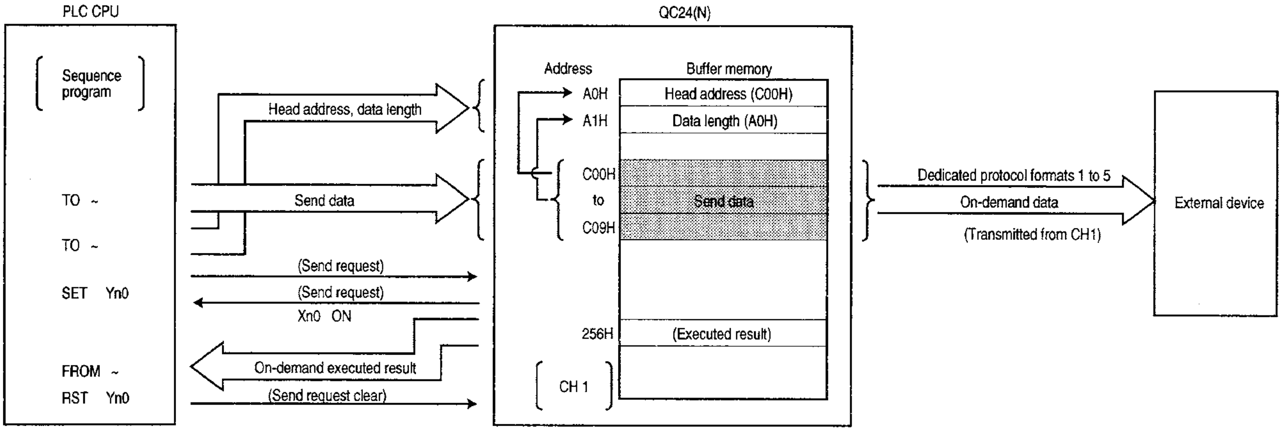
(b) Turning OFF global signal X (n+1) A of all the stations in a multidrop link



*2 Designates the station (all station/designated station only) whose global signal is to be turned ON and OFF by station No. (See Section 6.8.1 2 .)

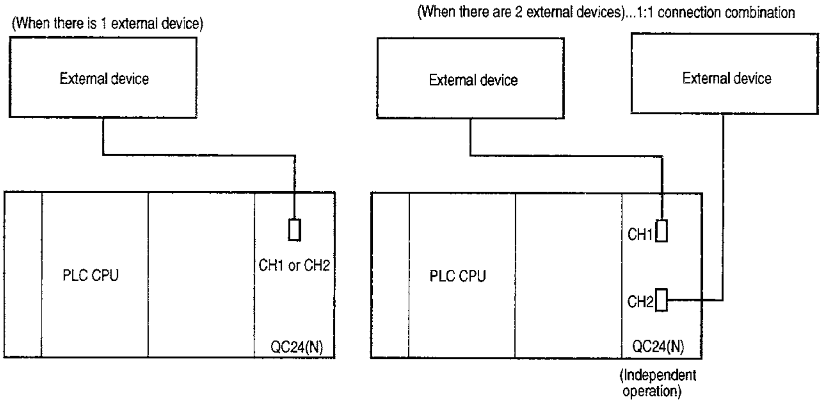
6.9 On-Demand Function

The on-demand function allows the PLC CPU to designate the buffer memory area in which the transmitted data is to be stored and start transmission when the PLC CPU has data to be transmitted to an external device.
Data transmission between external device and PLC CPU using a dedicated protocol is normally initiated by the external device.
When the PLC CPU has emergency data to be transmitted to an external device, the on-demand function is used to transmit the on-demand data to the external device by starting transmission from the PLC CPU.



POINT

The on-demand function can be used when the external device and PLC CPU system are connected in a 1:1 configuration.



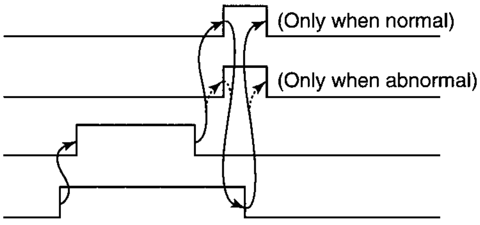
Do not use the on-demand function when the system configuration is not 1:1.
If you use the on-demand function when the external device and PLC CPU are connected by an m:n multidrop link, the control procedure formats 1 to 5 communication data and on-demand data will be destroyed and data will not be transmitted correctly.

6.9.1 On-demand function handshake I/O signals and buffer memory

The following describes the handshake I/O signals and buffer memory used by the on-demand function.

1 **On-demand function handshake I/O signals**

"Handshake I/O signals" are I/O signals exchanged between the PLC CPU and QC24(N) used when the on-demand function is used to transmit on-demand data from the PLC CPU to an external device.
They are used as an interlock to prevent on-demand requests from being issued simultaneously.

	I/O signal		Signal name	Device turned ON/OFF		Timing
	CH1	CH2		CPU	QC24(N)	
Input signal	Xn0	Xn7	Transmission normal end		○	
	Xn1	Xn8	Transmission abnormal end		○	
	Xn2	Xn9	Transmitting		○	
Output Signal	Yn0	Yn7	Send request	○		

2 **Buffer memories used by on-demand function**

The on-demand function uses the following buffer memories to transmit on-demand data.

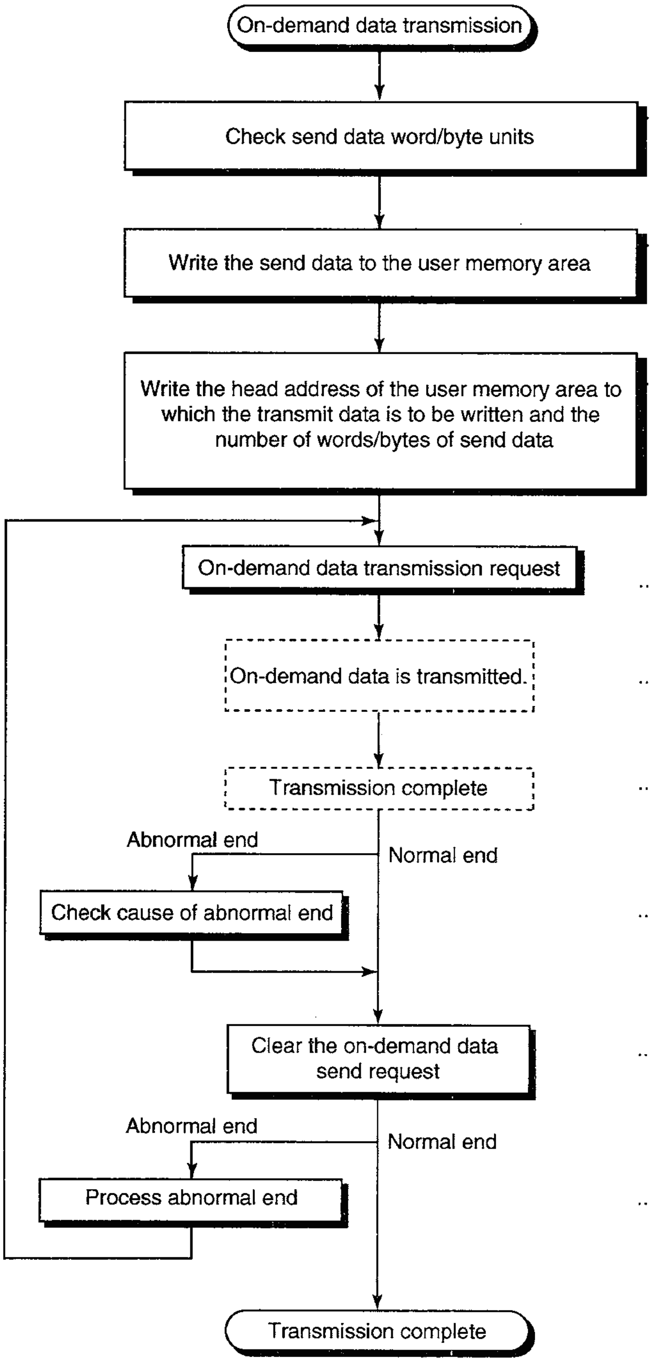
Address		Name	Device to which data is to be set		Description
CH1	CH2		CPU	QC24(N)	
96H (150)	136H (310)	Word/byte designation	○		Designates the data length units of the send data when the QC24(N) is started.
A0H (160)	140H (320)	On-demand buffer memory head address designation	○		Designates the head address of the user memory area to which the send data is to be written.
A1H (161)	141H (321)	On-demand data length designation	○		Designates the number of bytes/words of send data to be written to the user memory area. The data length units conform to [Word/byte designation] above.
256H (598)	266H (614)	On-demand executed result		○	Stores the result of transmission of the on-demand data. (Normal end: 0, abnormal end: nonzero) When nonzero is stored, see Section 22.2.
			○		Clears the result of on-demand data transmission.
400H (1024) to 1AFFH (6911)		User memory area	○		Designates the user data to be transmitted to the external device. (Write) *1

*1 When using this function with the following functions, be sure that duplicate areas are not allocated.

- Dedicated protocol .... Buffer memory read and write functions (See Section 6.3.)
- Non procedure protocol ..... Transmit and receive functions (See Chapters 9 to 11.)
- Bidirectional protocol .... Transmit and receive functions (See Chapters 12 and 13.)

6.9.2 On-demand function execution procedure

1 PLC CPU execution procedure



Check the contents of buffer memory addresses 96H/136H. See Section 6.9.4 for the transmission data formats when word or byte units are selected.

Write to buffer memory addresses 400H to 1AFFH. (See Section 6.9.1 2 *1.)
The buffer memory special applications area cannot be used.

Write the head address where the send data is to be written to buffer memory addresses A0H/140H and write the send data to buffer memory addresses A1H/141H.

Turn ON send request signal Yn0/Yn7.

Turn ON transmitting signal Xn2/Xn9.

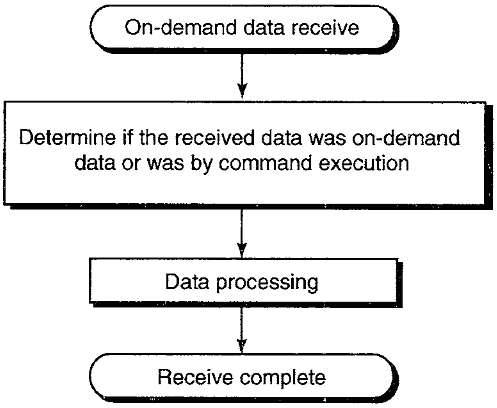
Turn OFF transmitting signal Xn2/Xn9.
For normal end, turn ON Xn0/Xn7.
For abnormal end, turn ON Xn1/Xn8.

Check the contents of buffer memory addresses 256H/266H. See Section 22.1 for the stored value (error code) and contents.

Turn OFF send request signal Yn0/Yn7.

When a nonzero value is written to buffer memory addresses 256H/266H, the data was not transmitted normally.

2 External device execution procedure



.... For on-demand data transmission, the QC24(N) sends "FE"/FEH as the PLC No.

- ASCII mode...."FE"
- Binary mode....FEH

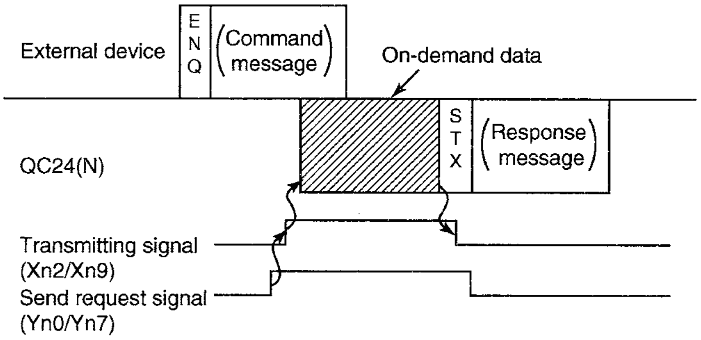
When the PLC No. of the received data is only "FE"/FEH, process it as on-demand data.

3 The following describes the timing charts when an on-demand send request was issued.

(a) Full-duplex communications

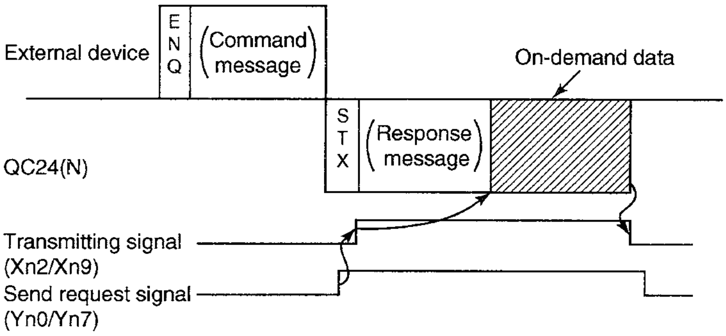
When QC24(N) is receiving data

The QC24(N) waits until the transmission of the on-demand data is complete before transmitting a response message (STX~) in reply to the command message (ENQ~).



When QC24(N) is transmitting data

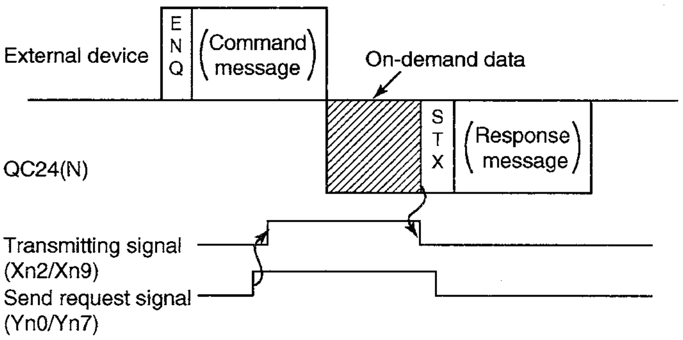
Transmission of the on-demand data waits until transmission of the response message (STX~) in reply to a command message (ENQ~) from the external device is complete.



(b) Half-duplex communications......See Section 14.5.

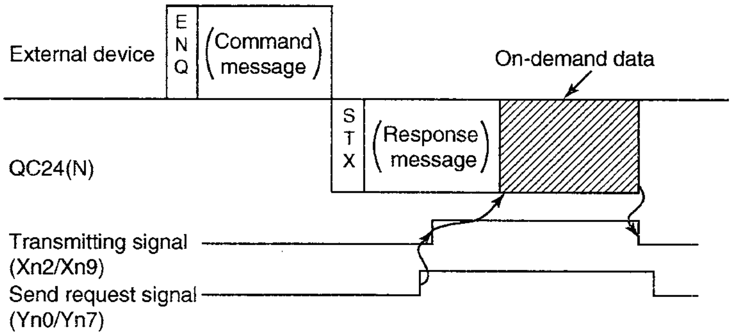
When QC24(N) is receiving data

On-demand data transmission waits until reception of the command message (ENQ~) from the external device is complete.



When QC24(N) is transmitting data

On-demand data transmission waits until transmission of the response message (STX~) in reply to the command message (ENQ~) from the external device is complete.



Note

During transmission of on-demand data and response data, time-out of the transmit watchdog timer (timer 2) described in Section 14.7.3 is checked.

If a time-out error was generated, reset the transmit watchdog timer so that transmission is normally completed within the set time.

(When transmitting on-demand data)

Transmitting signal ON time ≤ transmit watchdog timer (timer 2) setting

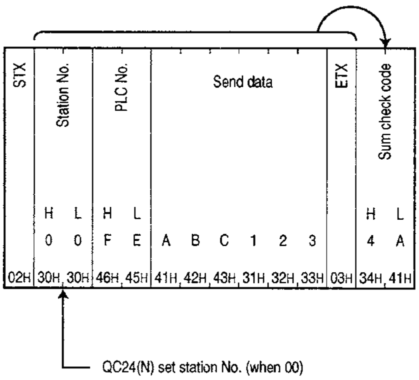
6.9.3 On-demand function data transmission format

The number set in the QC24(N) mode switch determines the on-demand function on-demand data list. The on-demand data is transmitted in the frame format shown below.

- When [1] to [4] set: ASCII mode A compatible frame [format 1] to [format 4] list
- When [5] set: Binary mode QnA extension frame [format 5] list

The following uses examples to describe the A compatible frame and QnA extension frame on-demand data lists and contents.
Data other than the send data, data byte count, and sum check code in the on-demand data are transmitted as the ASCII data or binary data shown in the illustration.
("Station No." is the QC24(N) set station No.)

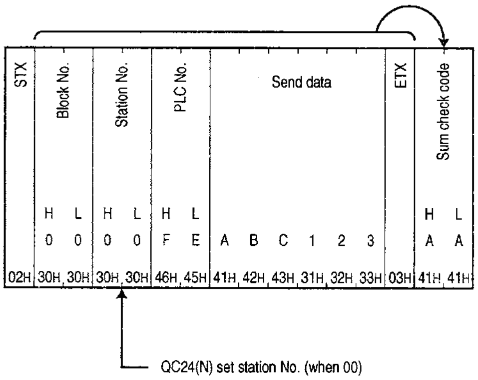
1 **ASCII mode A compatible frame formats 1 and 3 on-demand data transmission format**



QC24(N) set station No. (when 00)

*The QC24(N) adds and transmits data other than the send data.

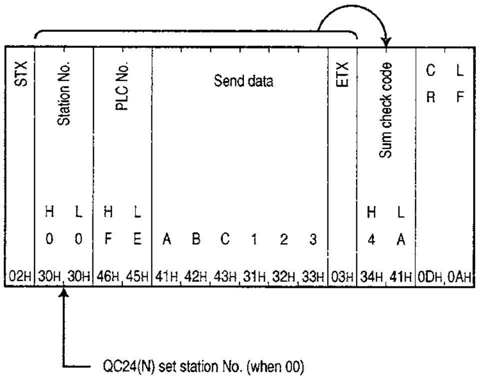
2 **ASCII mode A compatible frame format 2 on-demand data transmission format**



QC24(N) set station No. (when 00)

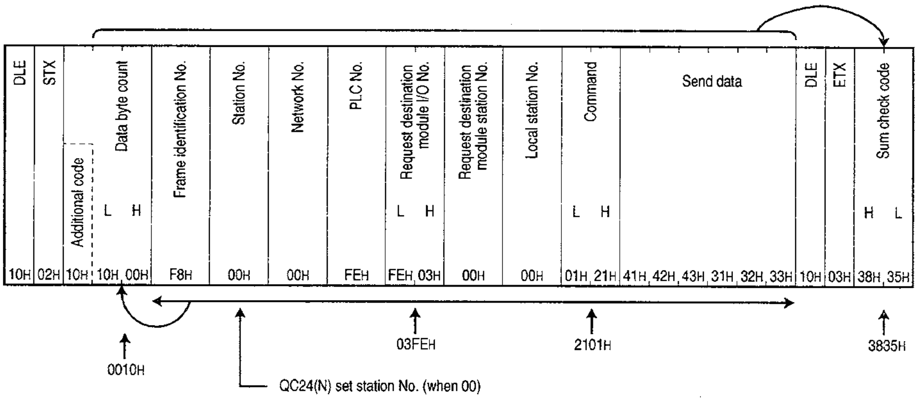
*The QC24(N) adds and transmits data other than the send data.

3 ASCII mode A compatible format 4 on-demand data transmission format



*The QC24(N) adds and transmits data other than the send data.

4 Binary mode A compatible frame format 5 on-demand data transmission format



POINT

When you want to transmit data in QnA (extension) frame user format or another format other than the above, use the user frame data communications function described in Chapter 7.

6.9.4 On-demand function control procedure (command: 2101)

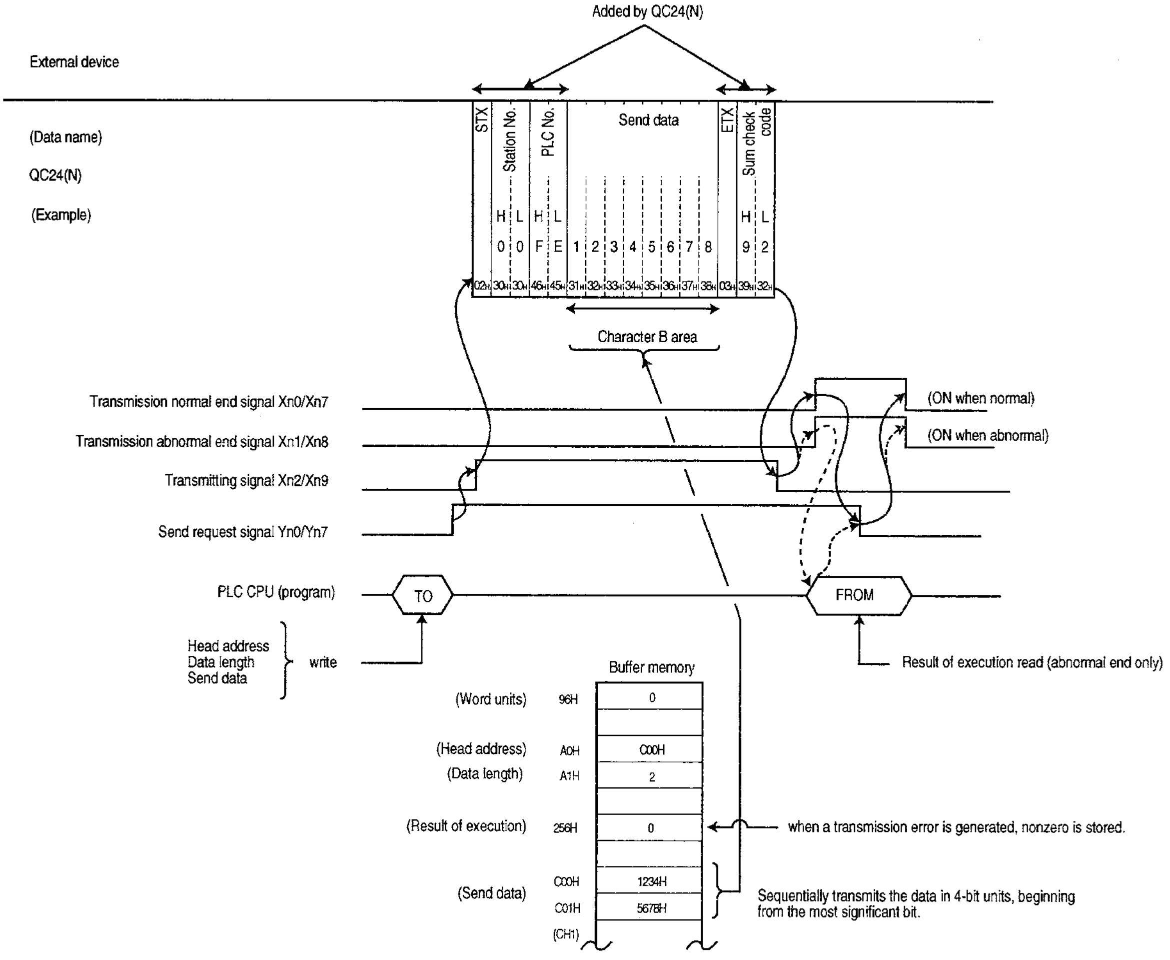
The following uses examples to describe the control procedure that uses the on-demand function to transmit on-demand data to an external device.

[Control Procedure]

The following describes the control procedure in A compatible frame format 1 and QnA extension frame format 5.

1 ASCII mode format 1

(a) When the value set to the "word/byte designation" area of QC24(N) buffer memory addresses 96H/136H is [0] (word units)
The illustration below shows the control procedure used to write 2 words of send data to buffer memory addresses C00H to C01H.

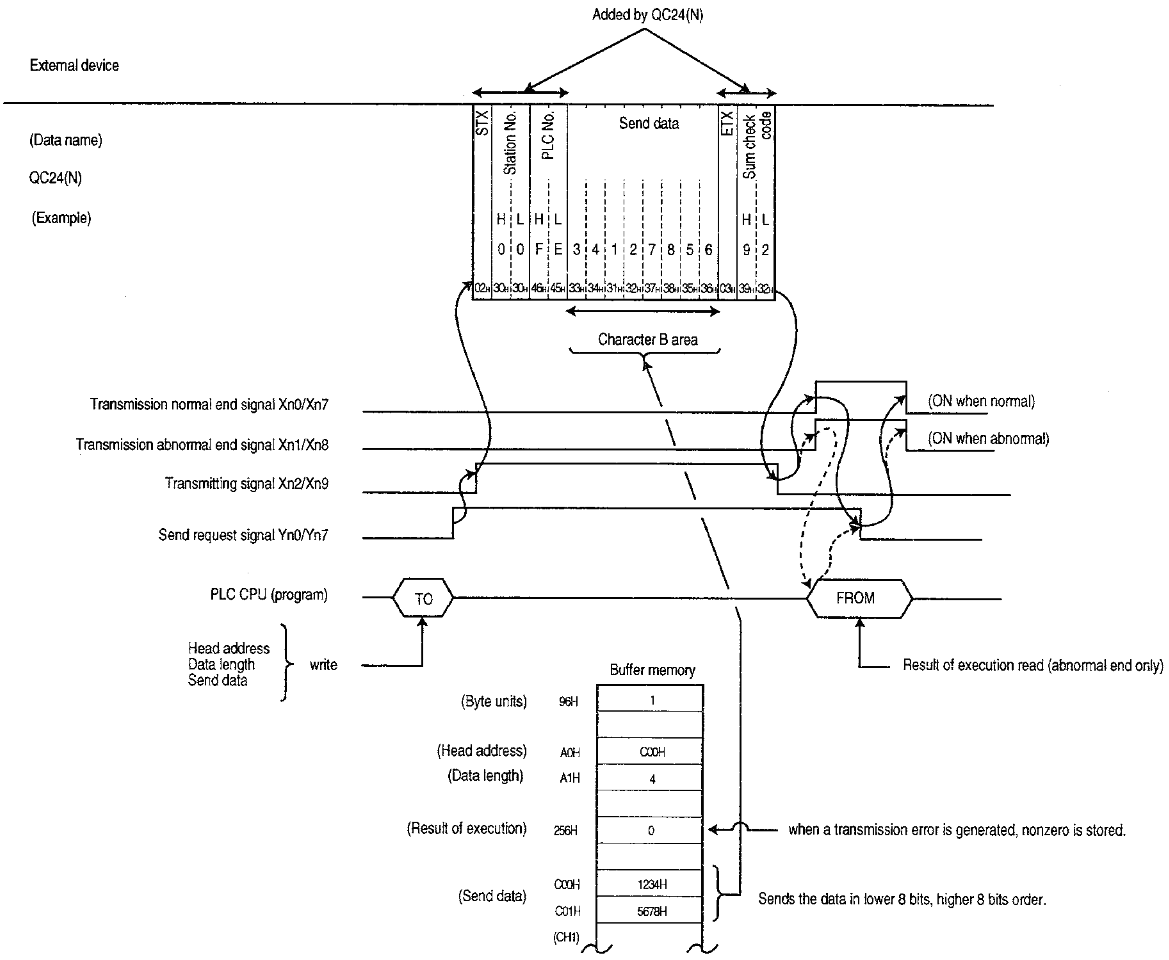


POINTS

(1) When control procedure format 2 is used, the block No. is "00".

(2) The number of characters of the send data area of the on-demand data is data length × 4.
[One byte of data uses 4 characters. Therefore, one byte of data is expressed by 4 digits (hexadecimal).]

(b) When the value set to the QC24(N) buffer addresses 96H/136H "word/byte designation" area is [1] (byte)
The illustration below shows the control procedure used to write 2 words (4 bytes) of send data to buffer memory addresses C00H to C01H.

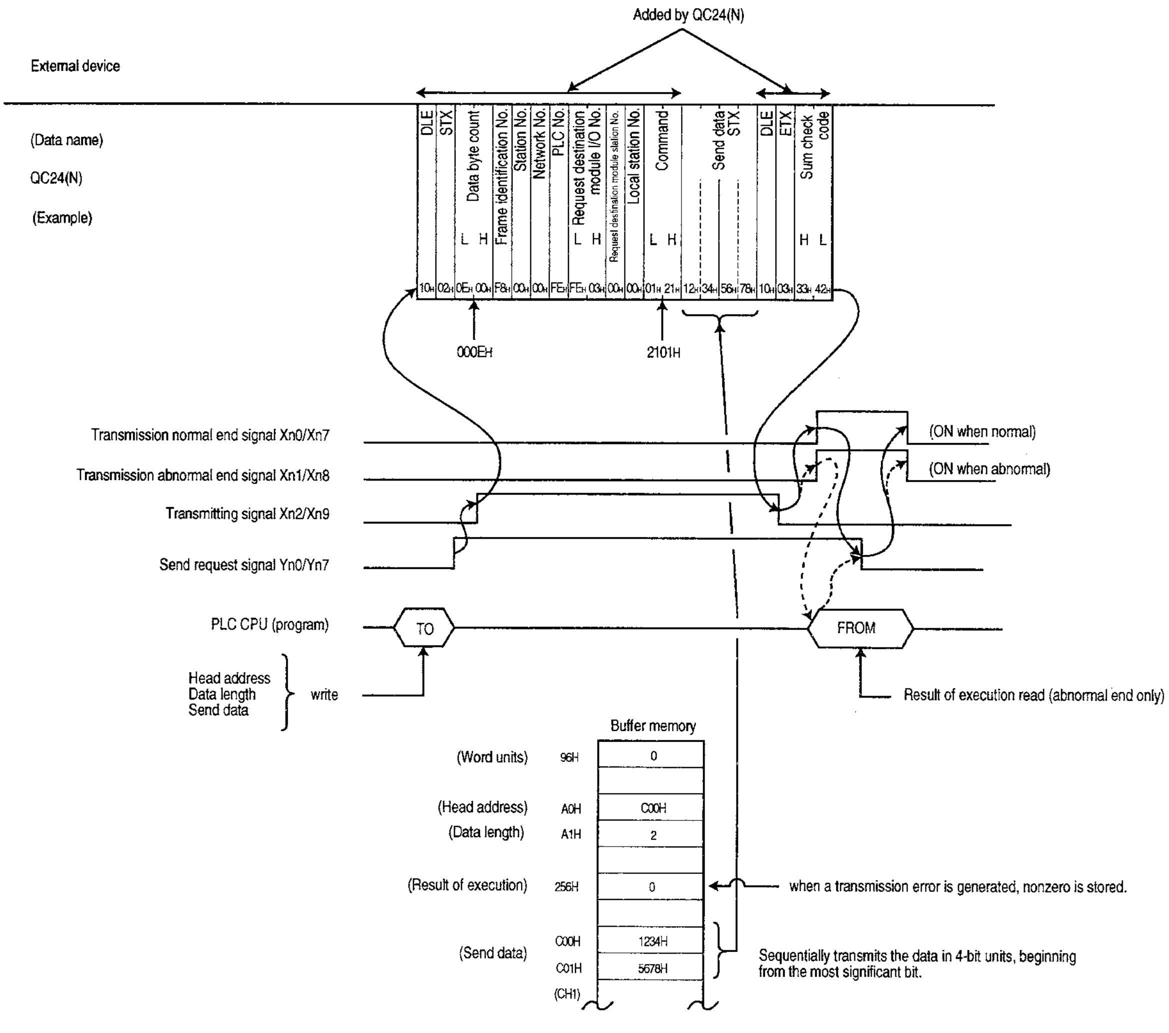


POINTS

(1) When control procedure format 2 is used, the block No. is "00".
(2) The number of characters of the send data area of the on-demand data is data length × 2.
[One byte of data uses 2 characters. Therefore, one byte of data is expressed by 2 digits (hexadecimal).]
(3) When the data length is an odd number, the data of the lower byte (bits 0 to 7) of the last data storage area of the buffer memory are transmitted.

2 **Binary mode format 5**

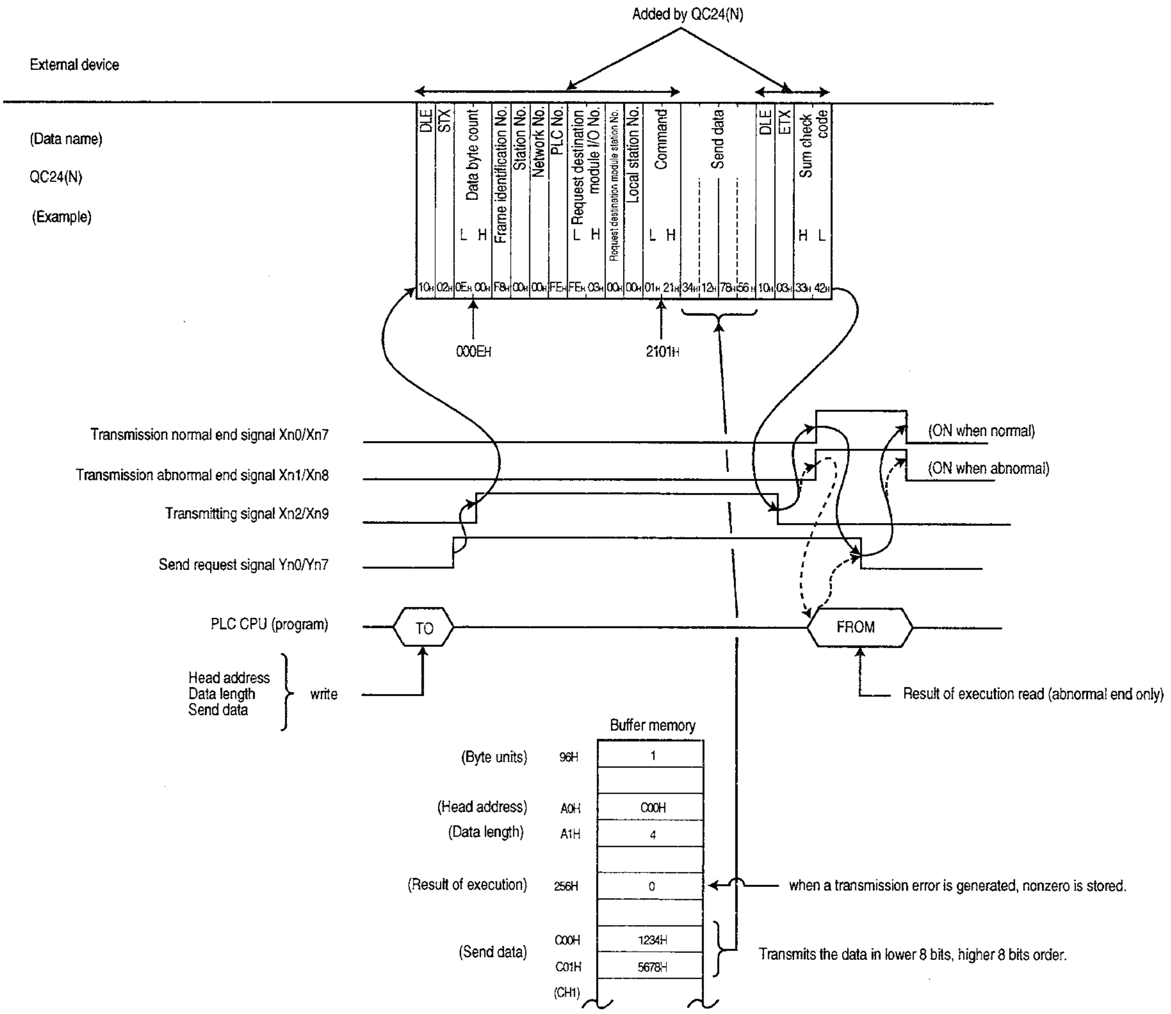
(a) When the value set to the QC24(N) buffer memory addresses 96H/136H "word/byte designation" area is [0] (word units)
The illustration below shows the control procedure used to write 2 words of send data to buffer memory addresses C00H to C01H.



POINT

The number of bytes of the send data area of the on-demand data is data length × 2. (One word of data uses 2 bytes.)

(b) When the value set to the QC24(N) buffer memory address 96H/136H "word/byte designation" area is [1] (byte units)
The illustration below shows the control procedure used to write 2 words (4 bytes) of send data to buffer memory addresses C00H to C01H.



POINTS

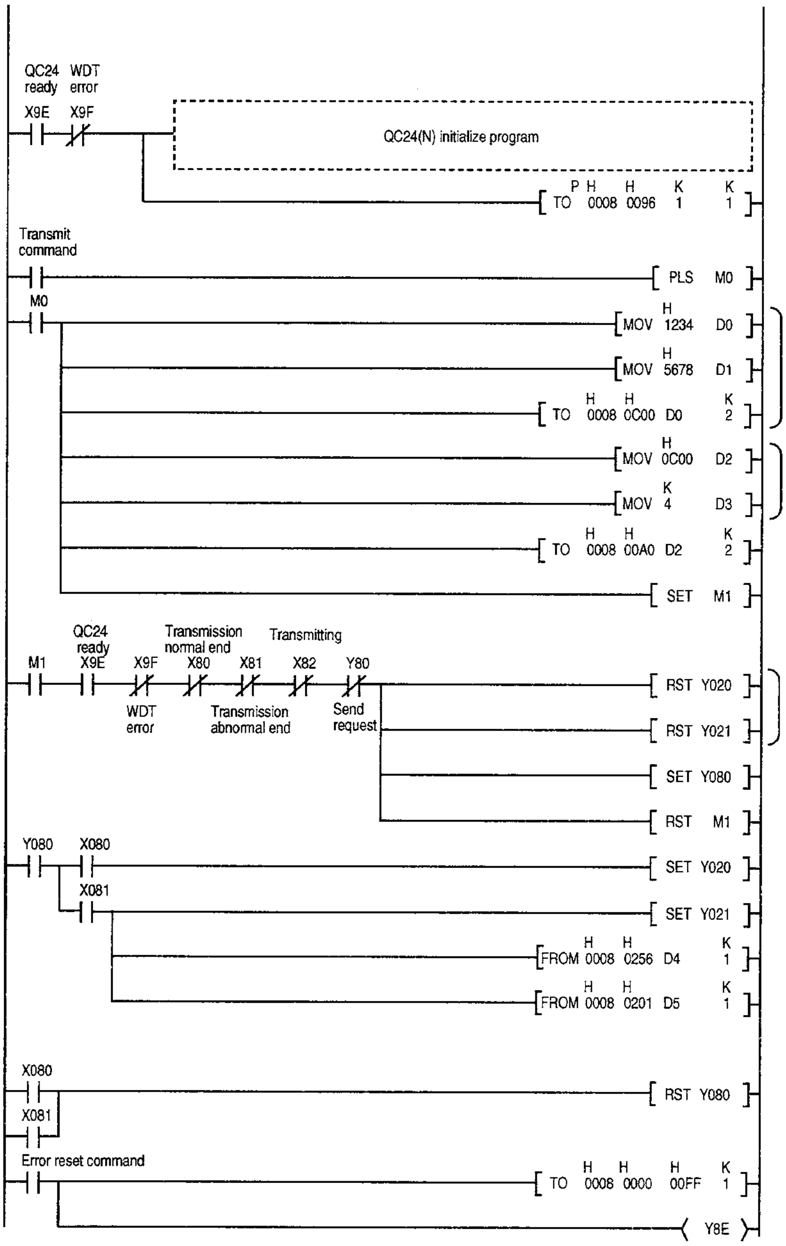
(1) The number of bytes of the send data area of the on-demand data is the same as the data length. (One byte of data uses 1 byte.)

(2) When the data length is an odd number, the data of the lower byte (bits 0 to 7) of the buffer memory last data storage area are transmitted.

3 Sample sequence programs when on-demand function used

The sample programs shown below use the control procedures described in 1 and 2 above as an example.
(QC24(N) I/O signals 80H to 9FH, transmission from CH1)

(a) Program when application instructions used (TO, TOP, DTO, DTOP instructions)
See the programming manual (common instructions) for more information.



Generates the program as described in Chapter 14. (The set contents can be registered to the QC24 EEPROM as described in Chapter 15.)

Sets the send data to word units.
Does not have to be written if the send data is in word units.

Converts the transmit command to PLS.

Sets the send data.

Sets the head address of the buffer memory storing the send data and the data length.
When the send data units are word units, this is made $-[\text{MOV}\ \overset{K}{2}\ \text{D3}]-$.

Resets the output signal for operator confirmation.

On-demand start. (Send request)

Normal end

Abnormal end
Determines the cause of the abnormal end by reading the result of on-demand execution and the LED ON status.

Address 256H — 0: Transmitted normally
Non zero: Data was not transmitted correctly due to an error.

Clears the send request.

Error LED OFF request.

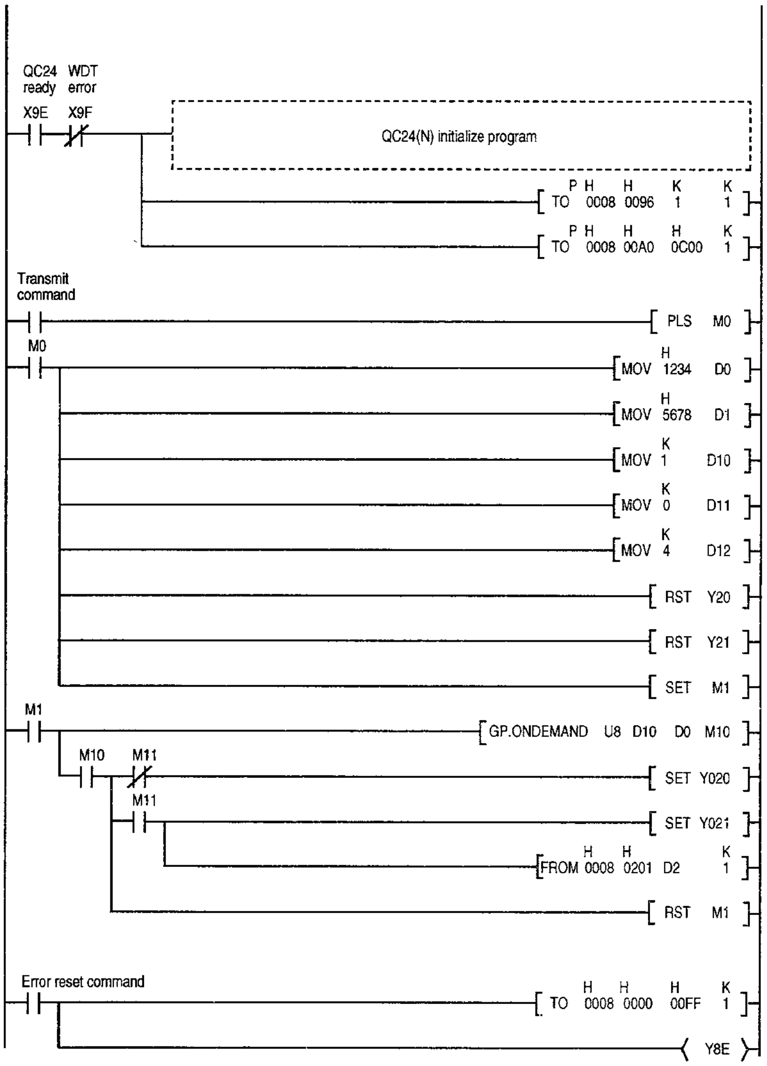
Resets the on-demand executed result stored value.

POINT

Designate so that the send data storage range and data length designation range do not exceed the following addresses.

- Word units .... 400H ≤ (Head address + designated data length – 1) ≤ 1AFFH
- Byte units ..... 400H ≤ (head address + (designated data length x 2) – 1) ≤ 1AFFH

(b) Program when dedicated instruction used (On-demand instruction)
See the programming manual (special function module) for more information.



Generates the program as described in Chapter 14. (The set contents can be registered to the QC24 EEPROM as described in Chapter 15.)

Sets the send data to byte units.
Does not have to be written if the send data is in word units.

Sets the on-demand buffer memory head address.

Converts the transmit command to PLS.

Sets the send data.

Designates the No. (CH□) of the interface that is to transmit the data.

Clears to 0 the device that stores the result of transmission.

When the send data units is word units, this is made $-[\text{MOV} \overset{K}{2}\ \text{D12}]-$.

Sets the Ready To Send flag.

On-demand starting. (Send request)

Normal end
Abnormal end [Output signal for operator confirmation]

Determines the cause of the abnormal end by reading D11 storing the result of on-demand transmission and the state of LED D2.

D11 — 0: Transmitted normally
Non zero: Data could not be transmitted due to an error.

Error LED OFF request.

Resets the on-demand executed result stored value.

POINTS

(1) When the QC24(N) dedicated instruction is used, model name registration by I/O allocation of the parameters written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and module model name (AJ71QC24) of the slot into which the QC24(N) is installed are set.)

(2) The status of communications by dedicated command can be read using the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of (1) and (2) above.

(4) Designate so that the send data storage size (stored in D0 and D1 of the sample program above) and data length (stored in D12 of the example program above) do not exceed the buffer memory range allocated to the on-demand function by the user.

6.10 Transmission Sequence Initialization

This function initializes the dedicated protocol binary mode data communication transmission sequence, and puts the QC24(N) into the state in which it is ready to receive commands from an external device.
To initialize the QC24(N) transmission sequence from the external device during data communications in the binary mode, transmit the command message described in this section to the QC24(N).
The function described in this section is the same as the ASCII mode data communications EOT, CL function.
See the description of EOT and CL in Section 6.1.4 1 (b) for the following contents:

- When the QC24(N) transmission sequence is initialized from an external device
- Processing and operation when the QC24(N) initializes the transmission sequence
- Transmission sequence initialization during data communications in the ASCII mode

POINT

This function can be used only when the QC24(N) (including a multidrop link station) is connected to an external device.
It cannot be used with the QC24(N) of another station connected over a data link system or network system.

6.10.1 Command

The following describes the command used when an external device initializes the QC24(N) transmission sequence.

Function	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
Transmission sequence initialize	1 6 1 5 (0 0 0 0)	Terminates the currently processing request and puts the QC24 into the command wait state.	(1 station)	(Unavailable)	○	○	○	6.10.2

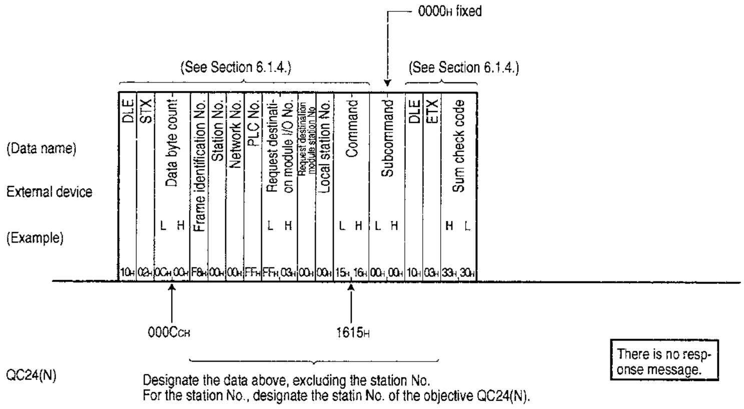
○ in the PLC CPU State column in the table above indicates that execution is possible.

6.10.2 Transmission sequence initialization (command: 1615)

The following uses an example to describe the transmission sequence initialization control procedure.

[Control Procedure]

QnA extension frame format 5 is used to describe the control procedure.



6.11 Mode Switching

This function forcefully switches the current operation mode (protocol) and transmission specifications of the designated interface from an external device after the QC24(N) starts.
It is used when continuing data communications by changing the mode and transmission specifications of each interface to match the data communications application without restarting the QnACPU.
This section only explains how to use the command that switches the QC24(N) mode from an external device.

POINTS

(1) Read Chapter 18 before switching the mode.
Chapter 18 explains how to switch the QC24(N) mode from the PLC CPU.

(2) This function, which switches the QC24(N) mode from an external device, can be used only with QC24(N) (including multidrop link stations) connected to an external device.
This function cannot be used with other station QC24(N) connected over a data link system or network system.

(3) Switching of the QC24(N) mode starts as soon as the mode switching request is issued.
If the QC24(N) was processing a request when a mode switching request was issued, it terminates that processing.

6.11.1 Command and contents of character area

The following describes the command and the contents of the character area (in binary mode, data area) when the QC24(N) mode is switched from an external device.

1 Command

Function	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
Mode switching	1 6 1 2 (0 0 0 0)	Switches the operation mode and transmission specifications of the designated interface.	(1 station)	(Unavailable)	○	○	○	6.11.2

○ in the PLC CPU State column in the table above indicates that execution is possible.

2 Contents of character area

The following describes the contents of the character area when the QC24(N) mode is switched from an external device.

(a) Channel No.

This data designates the interface (CH□) whose mode is to be switched.

① Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The channel No. designated values and objective interfaces are shown below.

Designated value	Objective interface
1H	QC24(H) CH1 interface
2H	QC24(H) CH2 interface

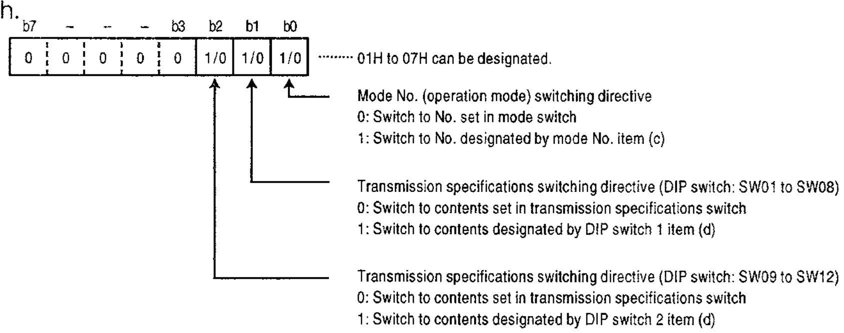
(b) Switching directive

This data designates the mode switching contents.

① Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The switching directive designated values and designation contents are shown below.
When a bit is 0 (OFF), the mode is switched according to the setting of the QC24(N) switch.



(c) Mode No.

This data designates the switching destination mode No.

① Data communications in ASCII mode
A value of [1] to [7] is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
A 1-byte value of [1] to [7] is transmitted.

③ The modes corresponding to the numbers and the mode No. that can be designated for each interface are the same as for setting by mode switch. (See Section 4.3.1.)

④ When "mode No. (operation mode) switching directive" of item (b) "Switching directive" is [0], this item uses a dummy to designate [1] to [7]. Do not designate [0].

(d) DIP switch 1, DIP switch 2

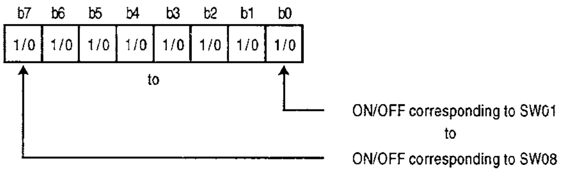
These data designate the switching transmission specifications during mode switching.

① Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

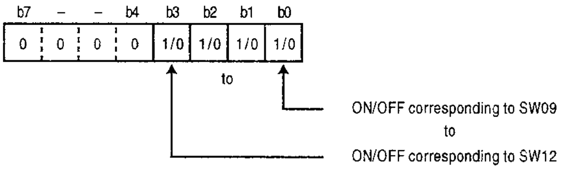
② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The DIP switch 1 and DIP switch 2 designated values and designation contents are shown below.
Relevant bit 1 (ON)/0 (OFF) is designated the same as ON/OFF setting of the corresponding transmission specifications switch of the QC24(N). (See Sections 4.3.1 and 4.3.2.)

- DIP switch 1 (Designation corresponding to SW01 to SW08)



- DIP switch 2 (Designation corresponding to SW09 to SW12)



④ When the objective "transmission specifications switching directive" of item (b) "Switching directive" above is [0], the corresponding DIP switch 1, DIP switch 2 item is made [00H].

6.11.2 Mode switching (command: 1612)

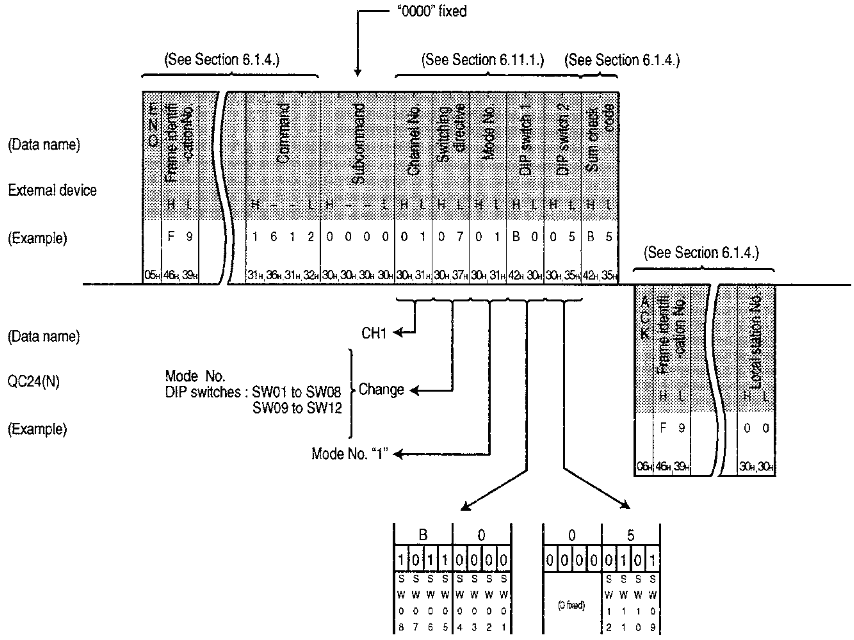
The following uses an example to describe the control procedure that switches the QC24(N) mode from an external device.

[Control Procedure]

Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

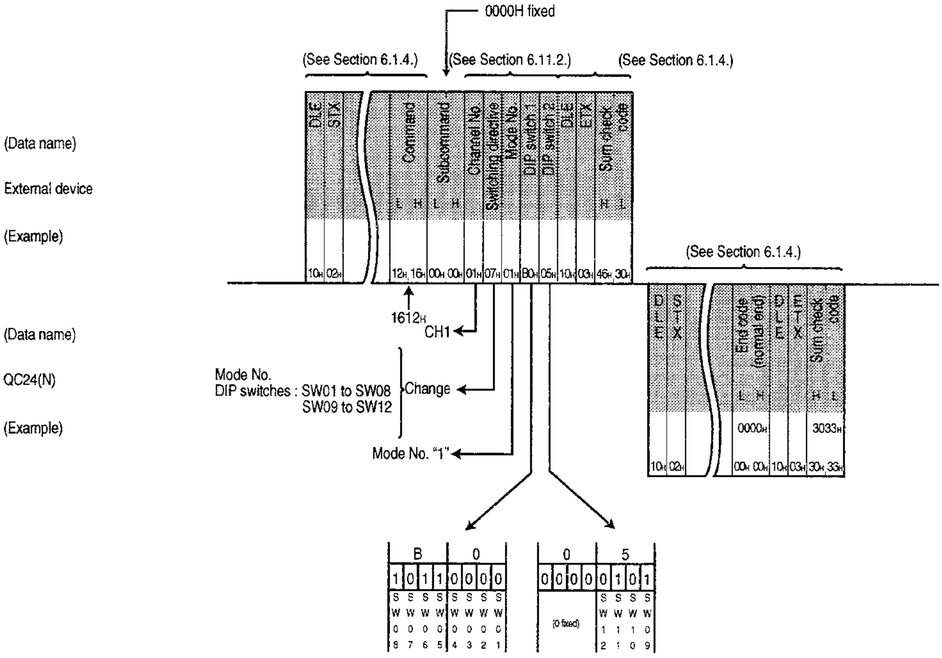
1 Using ASCII mode format 1 to switch the CH1 interface mode



* Mode switching contents of the illustration above

Designation item	Designation contents	Corresponding switch (Set value)
Operation mode	Dedicated protocol format 1	Mode switch (1)
Operation setting	Independent operation	SW01 (OFF)
Data bits setting	7 bits	SW02 (OFF)
Parity bit setting	Disabled	SW03 (OFF)
Even parity/odd parity setting	Odd	SW04 (OFF)
Stop bit setting	2 bits	SW05 (ON)
Sum check setting	Enabled	SW06 (ON)
Write during RUN enable/disable setting	Disable write during RUN	SW07 (OFF)
Setting modification enable/disable setting	Modification enabled	SW08 (ON)
Transmission speed	9600BPS	SW09 (ON)
		SW10 (OFF)
		SW11 (ON)
		SW12 (OFF)

2 Using binary mode format 5 to switch the CH1 interface mode



* The mode switching contents of the illustration above are the same as those of 1 .

6.12 LED OFF and Error Code Clearing

This function turns off the QC24(N) LED that can be turned off from an external device, or clears the error code stored in the buffer memory.

It is used to return the LEDs currently turned on by a NAK response to a command message to the normal state, or to clear the buffer memory error code area.

The QC24(N) processed this function the same as processing by the output signals and buffer memory shown below.

Processing corresponding to ON and OFF of bits 0 to 3 of the value indicated by subcommand described in Section 6.12.1 2 (a) is performed. Read the following description before using this function.

(Section 19.1.3 describes how this processing is performed from the PLC CPU.)

This section only describes how the commands are used.

Memory bit status representing the subcommand designated value	Output No. and buffer memory that perform the same processing	Processing	Reference section
When bit 0 is 1 (ON)	CH1.ERR LED OFF request signal (YnE)	Turns off the CH1.ERR LED and input signal XnE and clears the buffer memory CH1 error code.	19.1.3
When bit 1 is 1 (ON)	CH2.ERR LED OFF request signal (YnF)	Turns off the CH2.ERR LED and input signal XnF and clears the buffer memory CH2 error code.	
When bit 2 is 1 (ON)	LED OFF request area (Buffer memory address 0H)	Turns off the LED (LED Nos. 5 to 13 for description use)	19.1.1 19.1.2
When bit 3 is 1 (ON)	LED OFF request area (Buffer memory address 1H)	Turns OFF the LED (LED Nos. 16 to 21 for description use)	

POINTS

(1) Check QC24(N) processing according to whether bits 0 to 3 indicated by subcommand are ON/OFF before turning off the objective LED and clearing the error code.
It is recommended that the LED be turned off and the error code be cleared for each interface, or for both interfaces simultaneously.
(Subcommand designated by a value of 0005H, 000AH, or 000F.)

(2) This function can only be used with QC24(N) (including multidrop link stations) that are connected to an external device.
It cannot be used with other station QC24(N) that are connected over a data link system or network system.

6.12.1 Command and contents of character area

The following describes the command and the contents of the character area (for binary mode, data area) in the control procedure when the QC24(N) LEDs are turned OFF and the error code is cleared from an external device.

1 Command

Function	Command (subcommand) *ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
LED OFF and error code clear	1617 (000C)	Turns off the LED and clears the error code.	(1 station)	(Unavailable)	○	○	○	6.12.2

○ in the PLC CPU State column of the table above indicates that execution is possible.

2 Contents of character area

The following describes the contents of the character area when the QC24(N) LEDs are turned off and the error code is cleared from an external device.

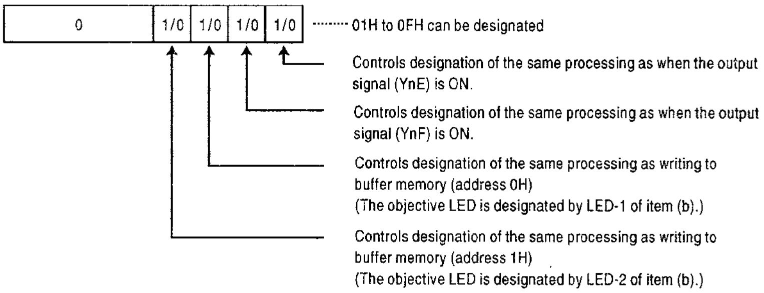
(a) Subcommand

This data designates if an LED is to be turned off or an error code is to be cleared.

① Data communications in ASCII mode
The value shown below is converted to a 2-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The 1-byte value shown below is transmitted.

③ The subcommand designated values and designation contents are shown below.
The corresponding processing can be performed by setting the relevant bit to 1 (ON).



(b) LED-1, LED-2

These data designate the LED to be turned off.

- LED-1 (Designated for description use LED Nos. 5 to 13)
- LED-2 (Designated for description use LED Nos. 16 to 21)

① Data communications in ASCII mode
The value shown below is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit.

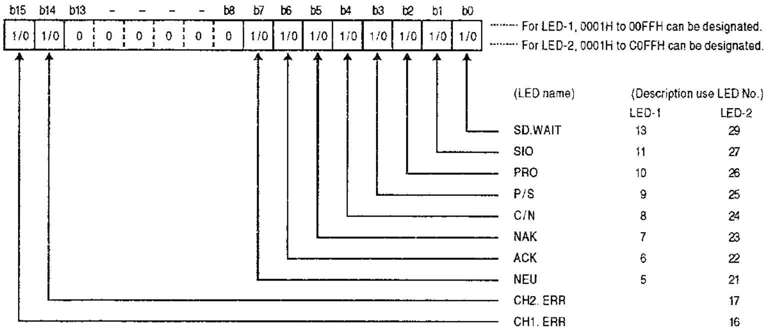
(Example) To make description use LED Nos. 16 to 21 (LED-2) the objective, the value shown below is converted to "C0FF" and sequentially transmitted from the "C".

② Data communications in binary mode

The 2-byte value shown below is sequentially transmitted from the Low byte (L: bits 0 to 7).

③ The LED-1 and LED-2 designated values and designation contents are shown below.
The LED to be turned off can be designated by setting the relevant bit to 1 (ON).

Subcommand	LED-1	LED-2	Notes
0001H to 0003H	00H	00H	Values other than 00H are designates as shown below.
0004H to 0007H	0001H to 00FFH	00H	
0008H to 000BH	00H	0001H to C0FFH	
000CH to 000FH	0001H to 00FFH	0001H to C0FFH	



6.12.2 LED OFF and error code clearing (command: 1617)

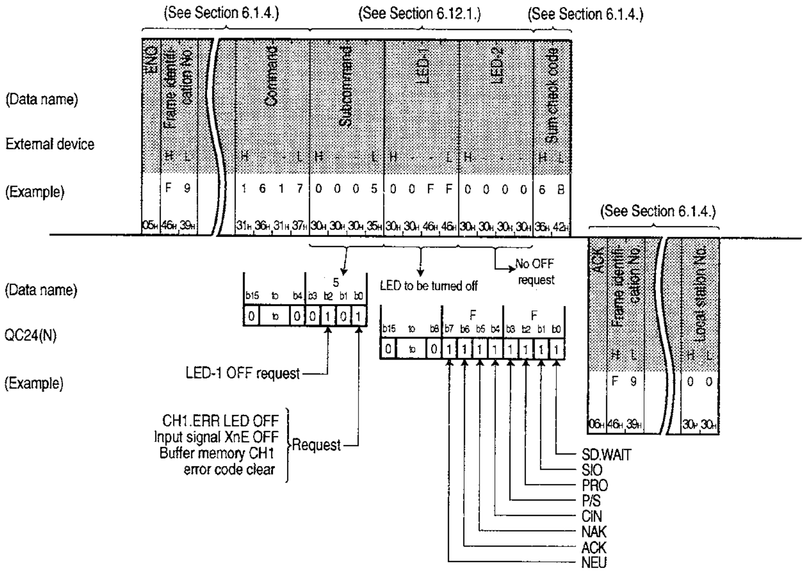
The following uses examples to describe the control procedure when the QC24(N) LEDs are turned off and the error code is cleared from an external device.

[Control Procedure]

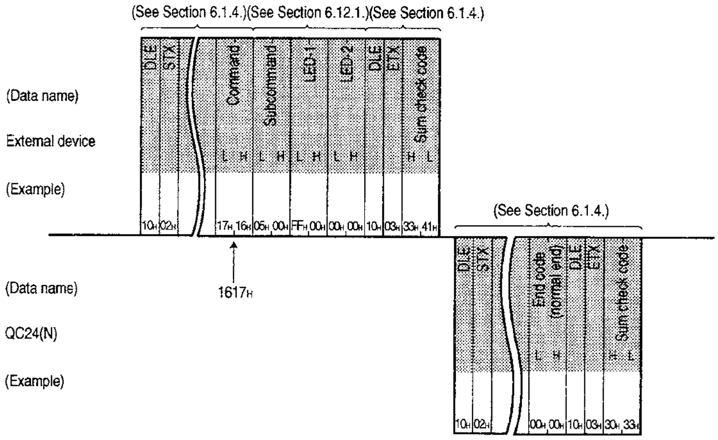
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 **Using ASCII mode format 1 to turn off the ACH1 interface CH1.ERR LED and input signal XnE and to clear the buffer memory CH1 error code and turn off the LED designated by the LED-1 item**



2 **Using binary mode format 5 to turn off the CH1 interface CH1.ERR LED and input signal XnE and clear the buffer memory CH1 error code and turn off the LED designated by the LED-1 item**



6.13 Loopback Test

"Loopback test" is a function that tests if the external device and QC24(N) communication function is operating normally. An example is used to describe the control procedure when this function is used.

POINTS

(1) When the QC24(N) is started, or when trouble occurs in the QC24(N), whether or not the external device and QC24(N) connection and data communication functions are operating normally can be checked using the loopback test function.

(2) This function can be used only with QC24(N) (including multidrop link stations) that are connected to an external device.
It cannot be used with other station QC24(N) connected over a data link system or network system.

6.13.1 Command and contents of character area

The following describes the command and the contents of the character area (for binary mode, data area) in the control procedure when performing a loopback test on the QC24(N) from an external device.

1 Command

Function	Command (subcommand) * ASCII mode: Designated by ASCII code. Binary mode: Each is designated as a hexadecimal value.	Processing	Number of points processed per communication		PLC CPU state			Reference section
			Access station-1 (See Section 5.4.1 *7.)	Access station-2 (See Section 5.4.1 *8.)	During STOP	During RUN		
						Write enable set	Write disable set	
Loopback test	0 6 1 9 (0 0 0 0)	Checks if data communication is performed normally.	960 bytes	(Unavailable)	○	○	○	6.13.2

○ in the PLC CPU State column of the table above indicates that execution is possible.

2 Contents of character area

The following describes the contents of the character area when the loopback test is performed on the QC24(N) from an external device.

(a) Loopback data count

This data designates the number of bytes of the loopback data area.

① Data communications in ASCII mode
The byte count is converted to a 4-digit (hexadecimal) ASCII code and sequentially transmitted from the most significant digit ("0").

② Data communications in binary mode
The byte count is sequentially transmitted as a 2-byte value, beginning from the Low byte (L: bits 0 to 7).

(b) Loopback data

This data designates the user data of the message that is transmitted and received using the loopback test function.

① Data communications in ASCII mode
The maximum 960 character portion half-width character string ("0" to "9," "A" to "F") order is transmitted from the header.

② Data communications in binary mode
The half-width character ("0" to "9," "A" to "F") order for each character code is transmitted as a 1 byte number and the maximum 960 byte portion is transmitted from the header character code.

6.13.2 Loopback test (command: 0619)

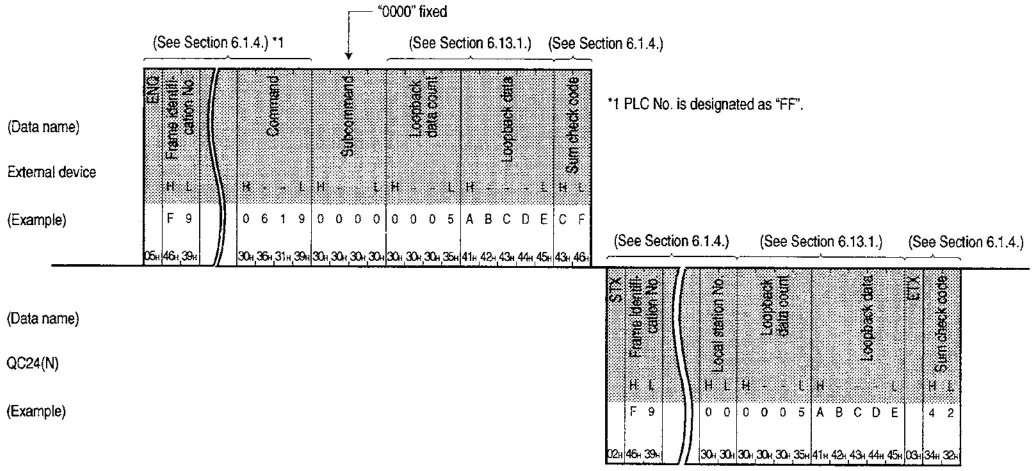
The following uses examples to describe the control procedure when loopback test is performed on the QC24(N) from an external device.

[Control Procedure]

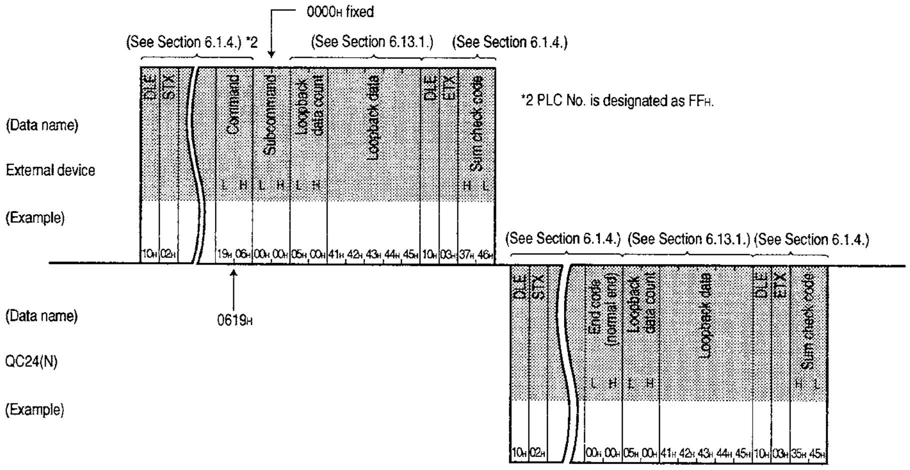
Format 1 and format 5 of the QnA (extension) frame are shown, focusing mainly on the designations to the character area.

To access by format 2 to format 4 of the QnA (extension) frame, follow the procedure described in Section 6.1.1 and 6.1.2 after seeing this description.

1 Using ASCII mode format 1 to perform the loopback test (loopback data: "ABCDE")



2 Using binary mode format 5 to perform the loopback test (loopback data: "ABCDE" code)



POINT

The loopback data count and loopback data transmitted by the external device are echoed back to the external device.

7. DATA COMMUNICATIONS USING USER FRAMES

During communications between external device and PLC CPU using a dedicated protocol, on-command data can be transmitted from the PLC CPU to the external device by on-demand function using user frames.

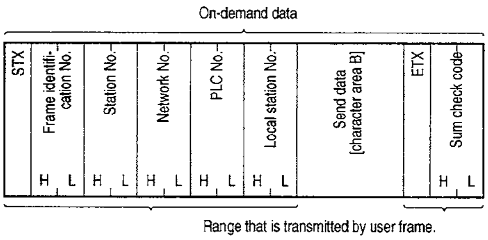
This section describes the transmission of designated send data by the PLC CPU using a message format other than the message formats (A compatible formats 1 to 4, QnA extension frame format 5) described in Section 6.9.3.

7.1 User Frame Data Communications Function

The user frame data communications function transmits and receives the message header and trailer parts in the format selected by the user during data communications between PLC CPU and external device via the QC24(N).

By using the function described in this section, on-demand data listed as shown below can be transmitted from the QC24(N) to an external device.

(Transmitting in QnA frame format 1)



Lists other than the "send data" part of the message format described in Section 6.9.3 are selected by the user as shown at the left. The "send data" part is the same as the list given in Section 6.9.3.

*1 User frame data communications can be carried out by registering the message format to be transmitted by the external device and the message format to be received by the external device according to the specifications of the external device to the QC24(N) as user frames.
For the illustration above, the QC24(N) transmits the on-demand data as described below.

- User frame sum check code
  Calculates the sum check code according to the contents registered in advance by the user and transmits the result as ASCII code or binary code data.
- Other than user frame sum check code
  Transmits data of the code registered in advance by the user. (No conversion)
- Send data (character area B)
  This is the data that the sequence program requested the QC24(N) to write to buffer memory.
  The same contents and list as when transmitted without using a user frame described in Section 6.9.4 by ASCII mode/binary mode and word/byte designation.

7.2 User Frame Types and Registration

Data communications using user frames can be performed by registering the user frames to the QC24(N) from an external device and the PLC CPU.
Chapter 16 describes the types of user frames and the data that can be used.
To register a user frame from the PLC CPU, see Chapter 16.
To register a user frame from an external device, first see Chapter 16 and check the precautions, etc., then register the user frame using the function described in Section 6.7.

7.3. User Frame On-Demand Data Transmission and Buffer Memory Used

This section describes user frame on-demand data transmission processing and the on-demand data list by user frame setting to QC24(N) buffer memory.

1 Transmission of on-demand data using user frames

The following describes the transmission of on-demand data using user frame.

① PLC CPU processing

- Before issuing a transmission request to the QC24(N), set the No. of the user frame registered in the QC24(N) to the buffer memory shown below.
- Except for the above, the PLC CPU execution procedure and control procedure are the same as when transmitting on-demand data without user frames described in Section 6.9.

② External device processing

- When the external device receives the user frame transmitted by the QC24(N) as the header frame, have it receive it as on-demand data.

2 Buffer memory used and on-demand data list

① Buffer memory used

During on-demand data transmission by user frame, the user frame to be transmitted is designated by the buffer memories shown below.

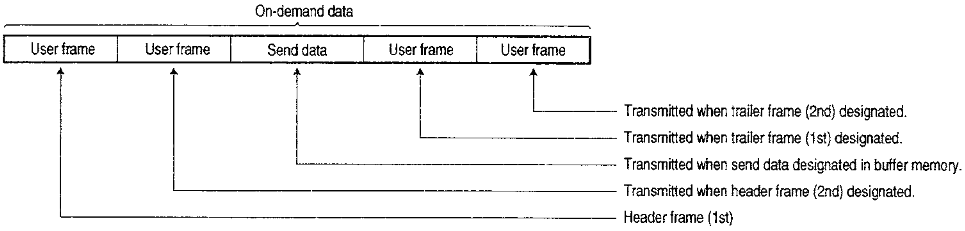
Address		Name			Description
CH1	CH2				
A9H(169)	149H(329)	On-demand user frame designation	Header frame No. designation	(1st)	Designates the No. of the user frame that is transmitted as the header frame. 0H : Do not transmit Others : Transmit (*1) * Other than 0H is always designated for the 1st frame. When designating the 1st frame, the 2nd frame can also be designated.
AAH(170)	14AH(330)			(2nd)	
ABH(171)	14BH(331)		Trailer frame No. designation	(1st)	Designates the No. of the user frame to be transmitted as the trailer frame. 0H : Do not transmit Others : Transmit (*1) * When designating the 1st frame, the 2nd frame can also be designated.
ACH(172)	14CH(332)			(2nd)	

*1 Designates the registration No. (shown below) of the user frame to be transmitted from among the user frames registered in the QC24(N).

1H to 3E7H (1 to 999) : Default frame
3E8H to 4AFH (1000 to 1199) : User frame (registered in EEPROM)
8001H to 801FH (-32767 to -32737) : User frame (registered in buffer memory)

② On-demand data list

The following shows the user frame designation on-demand data list.



POINTS

(1) Only the on-demand data list combinations shown below can be used.

○: Designation data

Data name / Combination	Header frame (1st)	Header frame (2nd)	Send data	Trailer frame (1st)	Trailer frame (2nd)
①	○	○	○	○	○
②	○	○	○	○	
③	○	○	○		
④	○	○			
⑤	○		○	○	○
⑥	○		○	○	
⑦	○		○		
⑧	○				

(2) The send data for on-demand data transmission by user frame is outlined below.
(See Chapter 16 for a detailed description of user frame.)

Contents of send data		ASCII mode	Binary mode
User frame Header frame (1st) Trailer frame (Trailer frame)	Codes registered from 00H to FEH	Transmit the data of the code registered in the QC24(N). (No conversion)	
	Combination of codes registered in FFH and 00H to FFH	Transmit the data according to the user-designated contents, code, and byte count.	
User frame Header frame (2nd) Trailer frame (Other than trailer frame)	Codes registered from 00H to FEH	Converts the data code registered in the QC24(N) to ASCII data and transmits the ASCII data.	Transmits data code registered in the QC24(N). For 10H data, transmits 10H + 10H.
	Combination of codes registered in FFH and 00H to FFH	Converts data of the contents, code, and byte count designated by the user to ASCII data and transmits the ASCII data.	Transmits the data of the contents, code, and byte count designated by the user. For 10H data, transmits 10H + 10H.
Send data (See Section 6.9.4 for details.)	—	Converts the designated send data to ASCII data and transmits the ASCII data.	Transmits the designated data unchanged. (No conversion) For 10H data, transmits 10H + 10H.

7.4 On-Demand Function Control Procedure During User Frame Use

The following uses examples to describe the control procedure when using the on-demand function to frame to transmit on-demand data to an external device by user frame.

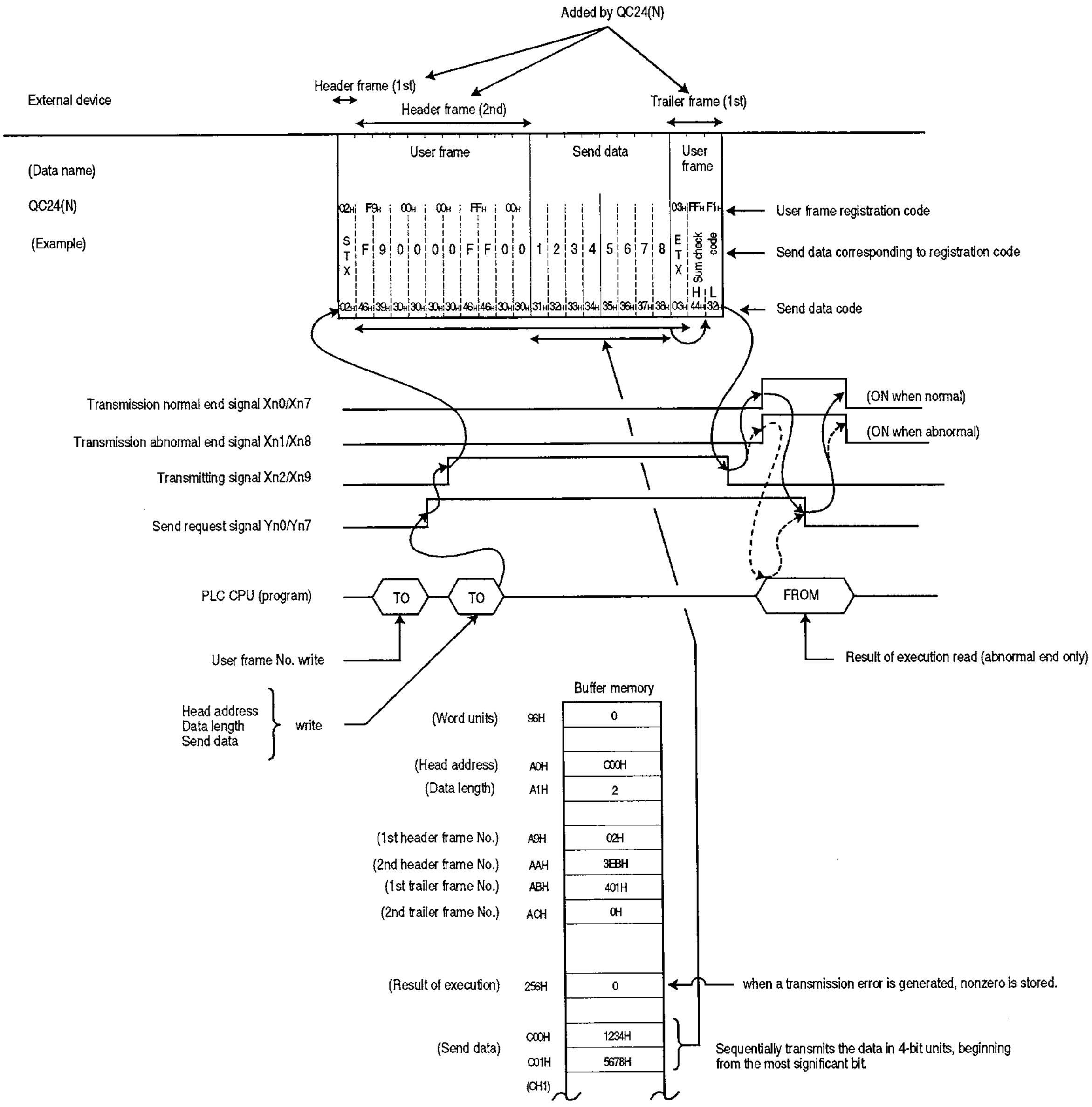
7.4.1 Data communications in ASCII mode

[Control Procedure]

1 **Transmitting data by user frame, user arbitrary send data, and user frame combination**

- Writing 2 words of send data to buffer memory addresses C00H to C01H
- The value set to the buffer memory address 96H/136H “word/byte designation” area is [0] (word units).
- The QC24(N) set station No. is [0].
- The registered user frame contents are shown below.

User frame No.	User frame (Registration code)	Contents of user frame registration
02H	02H	STX to local station No. data code matched to ASCII mode QnA frame format 1
3EBH(1003)	F9H, 00H, 00H, FFH, FFH, 00H	
401H(1025)	03H, FFH, F1H	ASCII mode QnA frame format 1 corresponding ETX, sum check code data code


Added by QC24(N)
Header frame (1st)
Header frame (2nd)
Trailer frame (1st)
External device
(Data name)
QC24(N)
(Example)
User frame
Send data
User frame
02H F9H 00H 00H FFH 00H 03H FFH F1H
STX F 9 0 0 0 0 F F 0 0 1 2 3 4 5 6 7 8 ETX Sum check code H L
02H 46H 39H 30H 30H 30H 30H 46H 46H 30H 30H 31H 32H 33H 34H 35H 36H 37H 38H 03H 44H 32H
User frame registration code
Send data corresponding to registration code
Send data code
Transmission normal end signal Xn0/Xn7
Transmission abnormal end signal Xn1/Xn8
Transmitting signal Xn2/Xn9
Send request signal Yn0/Yn7
(ON when normal)
(ON when abnormal)
PLC CPU (program)
TO
TO
FROM
User frame No. write
Head address
Data length
Send data
write
Result of execution read (abnormal end only)
Buffer memory
(Word units) 96H 0
(Head address) A0H C00H
(Data length) A1H 2
(1st header frame No.) A9H 02H
(2nd header frame No.) AAH 3EBH
(1st trailer frame No.) ABH 401H
(2nd trailer frame No.) ACH 0H
(Result of execution) 256H 0
(Send data) C00H 1234H
C01H 5678H
(CH1)
when a transmission error is generated, nonzero is stored.
Sequentially transmits the data in 4-bit units, beginning from the most significant bit.

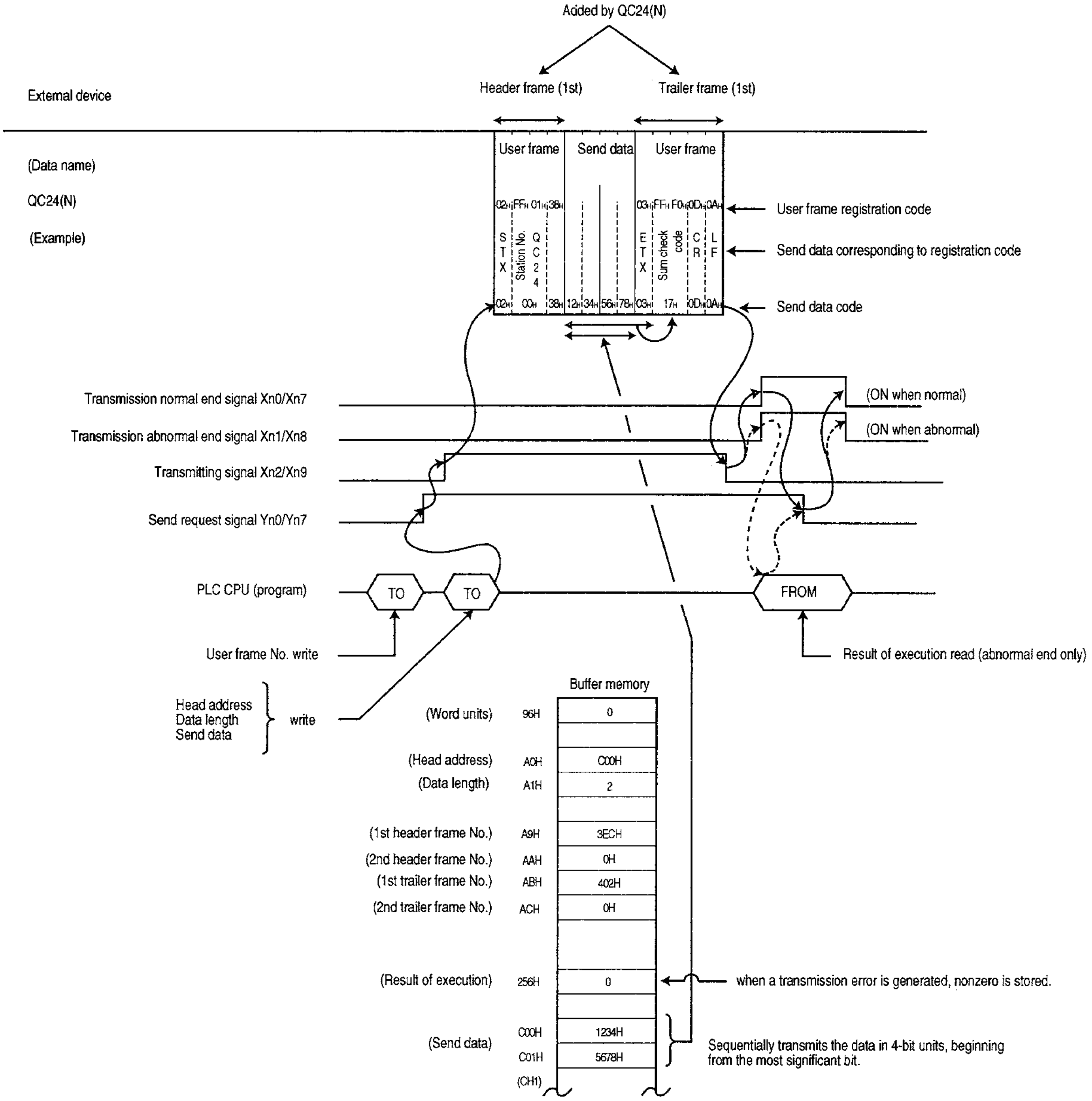
7.4.2 Data communications in binary mode

[Control Procedure]

1 Transmitting using user frames, user arbitrary send data, and user frame combination

- Writing 2 words of the send data to buffer memory addresses C00H to C01H
- The value set to buffer memory addresses 96H/136H "word/byte designation" area is [0] (word units).
- The QC24(N) set station No. is [0].
- The registered user frame contents are shown below.

User frame No.	User frame (Registration code)	User frame registration contents
3ECH(1004)	02H, FFH, 01H, 3BH	STX + QC24(N) station No. + ;
402H(1026)	03H, FFH, F0H, 0DH, 0AH	ETX + sum check code + CR + LF [Sum check code is designated by a 1 byte binary code.]

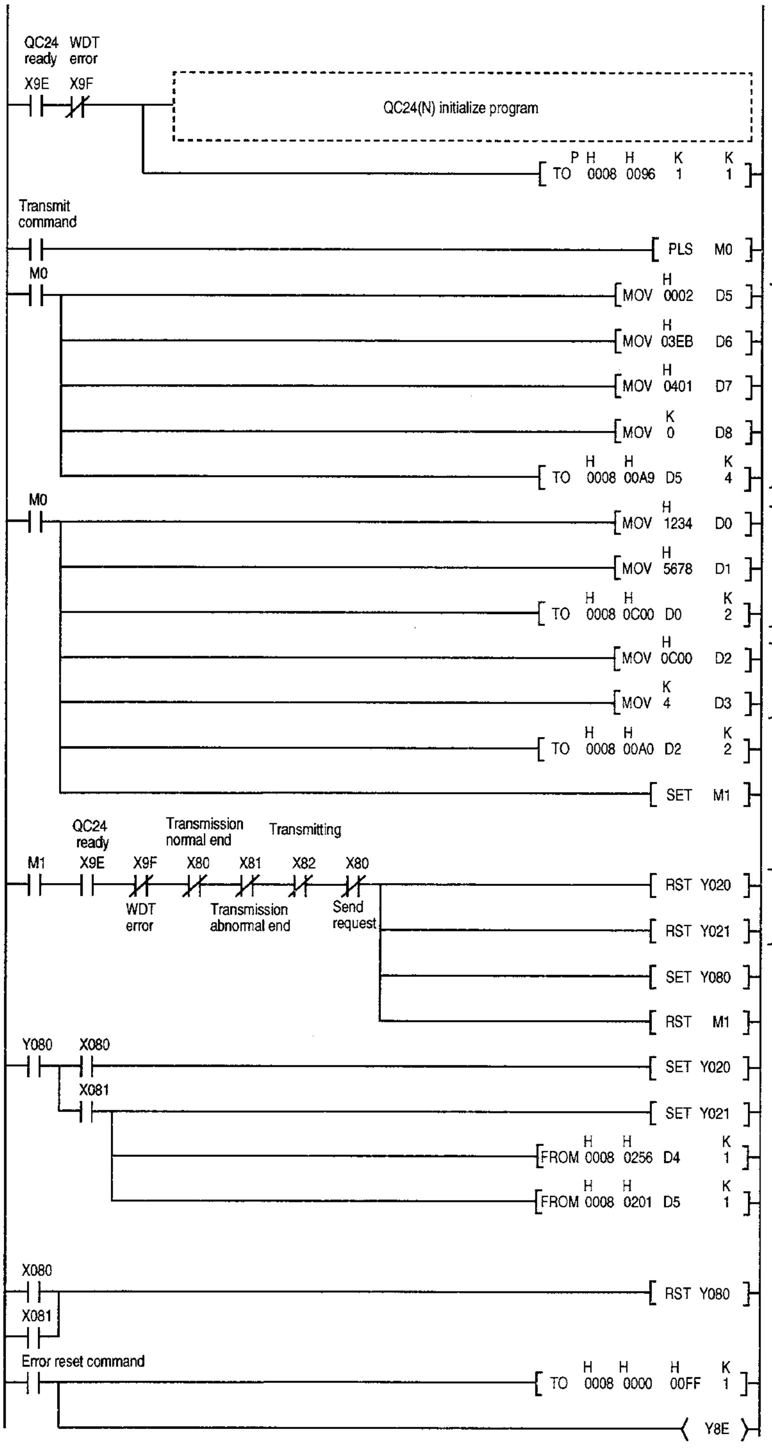


7.5 Sample User Frame On-Demand Data Transmission Sequence Program

A sample sequence program that transmits on-demand data containing a user frame is shown below.

Except for the part that designates the user frame to be transmitted, this program is the same as the program given in Section 6.9.4 3.

(QC24(N) I/O signal 80H to 9FH, transmission from CH1)



Generated according to Chapter 14. (The set contents can be registered to the QC24 EEPROM as described in Chapter 15.)

Sets the send data to byte units. Does not have to be written if the send data is in word units.

Converts the transmit command to PLS.

* Part added to Section 6.9.4 3.
Sets the No. of the user frame (registered) to be transmitted.
(Header frame (2), trailer frame (1))
The values at the left are set for Section 7.4.1 use. For 7.4.2 use, they are made D5: 03ECH, D6: 0H, D7: 0402H, D8: 0H)

Sets the send data.

Sets the head address and data length of the buffer memory that stores the send data. When the send data units is word units, this is made -[MOV $\overset{K}{2}$ D3]-.

Resets the output signal for operator confirmation.

On-demand starting. (Send request)

Normal end

Abnormal end
Determines the cause of the abnormal end by reading the result of on-demand execution and the LED ON status.

Address 256H	0:	Transmitted normally
	Nonzero:	Data could not be transmitted due to an error.

Clears the send request.

Error LED OFF request

Resets the on-demand executed result stored value.

POINT

Designate so that the send data storage range and data length designation range do not exceed the addresses allocated to the on-demand function by the user.

Applicable module	AJ71QC24			A1SJ71QC24		AJ71QC24N			A1SJ71QC24N	
	–	-R2	-R4	–	-R2	–	-R2	-R4	–	-R2
Function availability	×	×	×	×	×	○	○	○	○	○
Remark	–					–				

8. DATA COMMUNICATIONS USING QnA SIMPLIFIED FRAME

This section describes the communication function by the QnA simplified frame which has been added in the QC24N.

8.1 QnA Simplified Frame Data Communications Function

The communications function by the QnA simplified frame is described.

(1) The QnA simplified frame is a frame for the dedicated protocol with simplified message format in order to reduce the communication time from the external device to the device memory of the QnACPU (local station) with a QC24N installed.

(2) Because of less amount of the transmission data, processing of the message by the external device is made easier and the transmission time of the message can be reduced.

8.2 Format of the QnA Simplified Frame, Accessible PCs, and the Accessible Range

The format of the QnA simplified frame, accessible PLCs, and the accessible range are described.

1 Format of the QnA simplified frame

The communication is allowed by format 1 to format 4 for the ASCII mode, and is executed by the format of the number set by the mode setting switch of the QC24N.

There is no QnA simplified frame by format 5 for the binary mode.

	Mode	Frame type (dedicated protocol)	Mode switch No.				
			Format 1	Format 2	Format 3	Format 4	Format 5
Dedicated protocol	ASCII mode	QnA frame	1	2	3	4	
		QnA extension frame					
		A compatible frame					
		QnA simplified frame					
	Binary mode	QnA extension frame					5

2 Accessible PCs and the range by the QnA simplified frame

The communication is allowed only to the following local station QnACPUs.

① Local station QnACPU installed QC24N.

② Other station's QnACPU installed QC24N with the multi-drop connection.

POINT

The access to other station's PLC is not allowed via the MELSECNET/10 remote station installed QC24N (local station), MELSECNET(II)/B, or MELSECNET/10.

8.3 Command for QnA Simplified Frame and Function List

The commands and functions used for the communication by the QnA simplified frame are as follows.

All the commands are for reading data from and writing data to the device memory of the PLC CPU installed QC24N by the dedicated protocol.

Functions		Command	Processing	Number of points processed per communication	PLC CPU state (*1)		
					During STOP	During RUN	
						Write enable set	Write disable set
Batch read	Bit units	1	Bit devices are read in 1 point units. (1 point = 1 bit)	3952 points	○	○	○
	Word units	2	Bit devices are read in 1 point units. (1 point = 16 bits) Word devices are read in 1 point units.	480 points			
Batch write (*2)	Bit units	3	Bit devices are written in 1 point units. (1 point = 1 bit)	3952 points	○	○	×
	Word units	4	Bit devices are written in 1 point units. (1 point = 16 bits) Word devices are written in 1 point units.	480 points			
Random read	Word units	5	Bit devices are read in 1 point units and the devices and device No. are randomly set. (1 point = 16 bits) Word devices are read in 1 point units and the devices and devices No. are randomly set.	96 points	○	○	○
Test (Random write) (*2)	Bit units	6	Bit devices are written in 1 point units and the devices and device No. are randomly set. (1 point = 1 bit)	94 points	○	○	×
	Word units	7	Bit devices are written in 1 point units, and the devices and device No. are randomly set. (1 point = 16 bits) Word devices are written in 1 point units, and the devices and device No. are randomly set.	960 points			
Monitor data registration (*3)	Word units	8	Bit devices that monitor are registered in 1 point units. (1 point = 16 bits) Word devices that monitor are registered in 1 point units.	96 points	○	○	○
Monitor (*3)	Word units	9	Device monitors for which monitor data registration was conducted.	Number of registrations points			

*1 Use the QC24N transmission specification switch SW07 to set whether it is possible to write to the PLC CPU during RUN.
SW07 = ON .... Write possible during RUN (Enable)
SW07 = OFF ...... Write not possible during RUN (Disable)

*2 When the system protect is active (system protect switch SW05=ON) for the QnACPU which executes the command, an error occurs and a NAK message is returned.

*3 The procedure for monitoring is the same as that for monitoring the communication by the QnA (extension) frame.

8.4 Basic Format of the Data Communication by the QnA Simplified Frame

The basic format of the data communication by the QnA simplified frame and the contents of the designated data name are described.

8.4.1 Basic format of the data communication

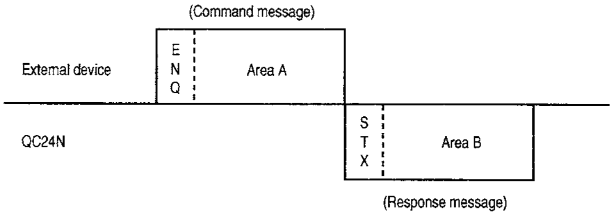
The basic format of the data communication by the QnA simplified frame is as follows:
The differences between the four ASCII mode formats when format 1 is made the standard are shown below.

Format 2 .... Format with block number added to each message
Format 3 .... Format with each message enclosed between STX and ETX
Format 4 .... Format with CR, LF added to each message

● **Basics of dedicated protocol control procedure**

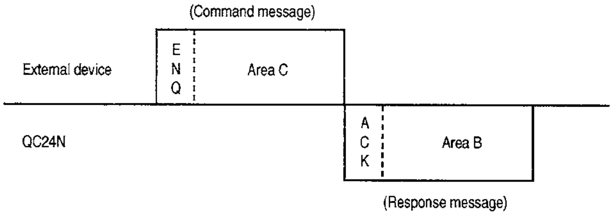
This section describes the basics of the transmission data given in the description of each control procedure.

(a) When the external device reads data from PLC



① Area A indicates transmission from external device to QC24N.
② Area B indicates transmission from QC24N to external device.
③ The external device program is generated so that the data are sequentially sent from left to right.
(Example: For Area A, the data is sequentially sent to the right from ENQ.)

(b) When the external device writes data to PLC



① Area C indicates transmission from external device to QC24N.
② Area B indicates transmission from QC24N to external device.
③ The external device program is generated so that the data are sequentially sent from left to right.
(Example: For Area C, the data is sequentially sent to the right from ENQ.)

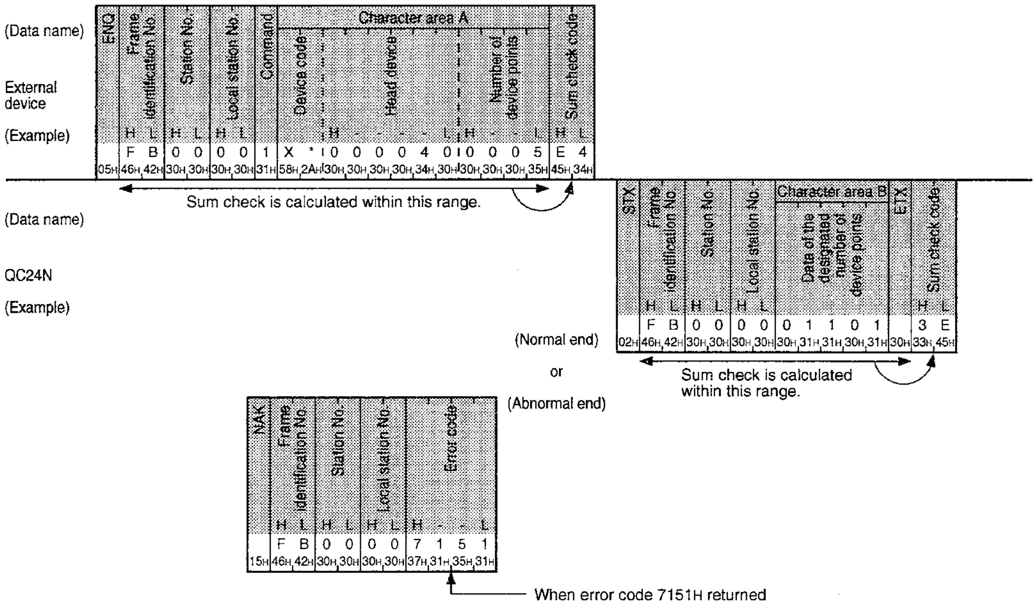
POINT

When the QC24 receives a command message from an external device, after it completes processing of Area A in the message, the QC24N transmits a response message and enters the neutral state.
When the QC24N is in the neutral state, it waits to receive the next command message and a on-demand data transmission request from the PLC CPU.

1 Communication using control procedure format 1

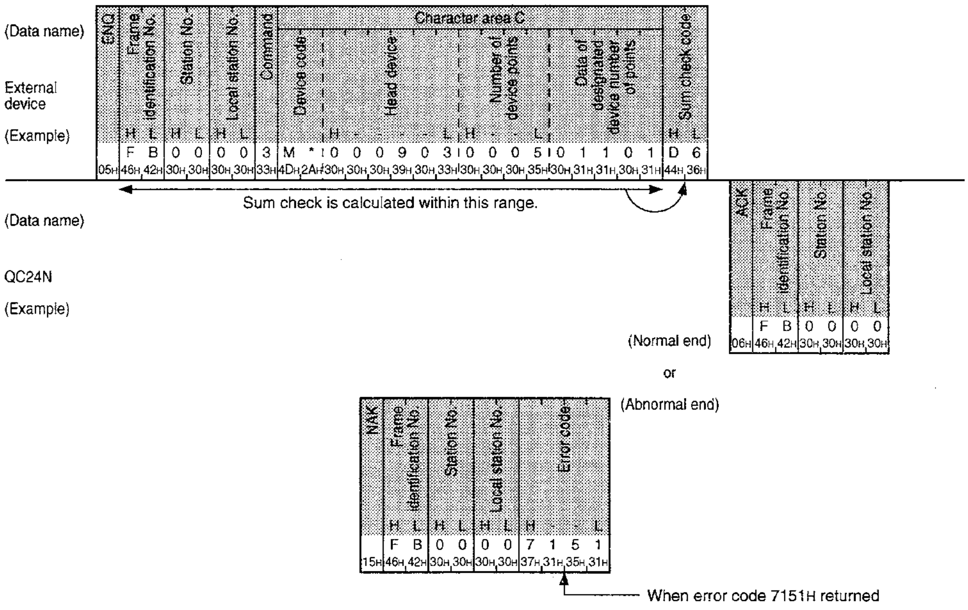
① When the external device reads data from QnACPU

(Example) Using a command 1, the external device reads five points data form X 40 to X 44 of the QnACPU:



② When the external device writes data to QnACPU

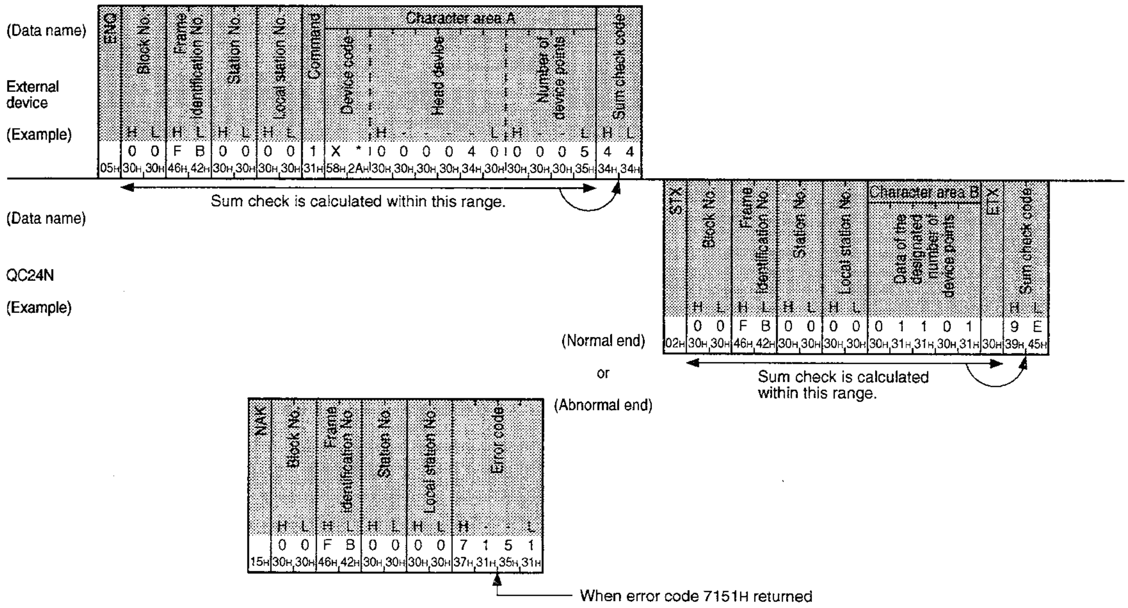
(Example) Using a command 3, the external device writes five points data to M903 to M907 of the QnACPU:



2 Communicaion using control procedure format 2

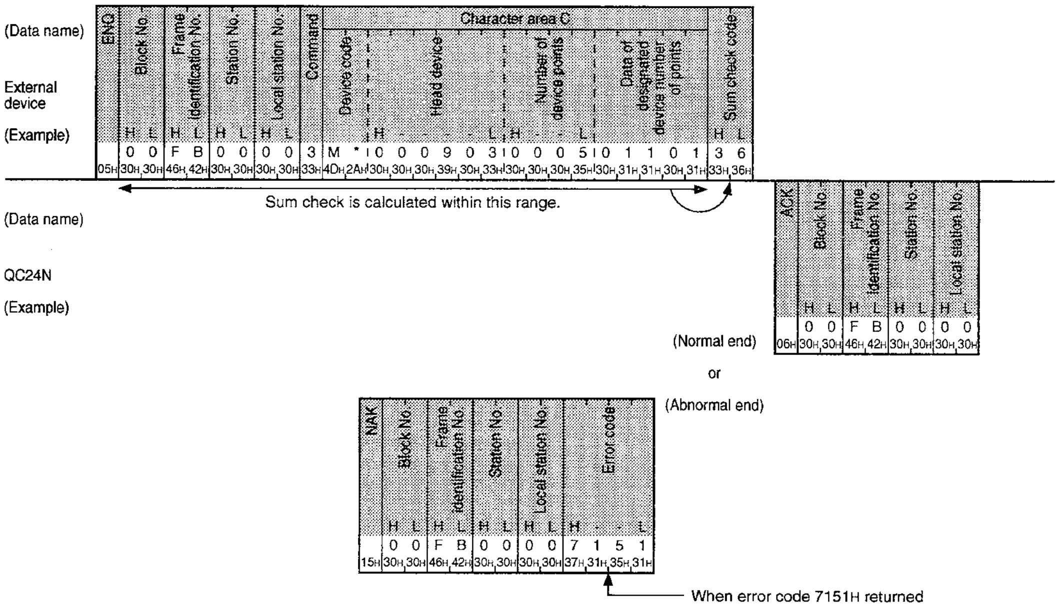
① When the external device reads data from QnACPU

(Example) Using a command 1, the external device reads five points data form X 40 to X 44 of the QnACPU:



② When the external device writes data to QnACPU

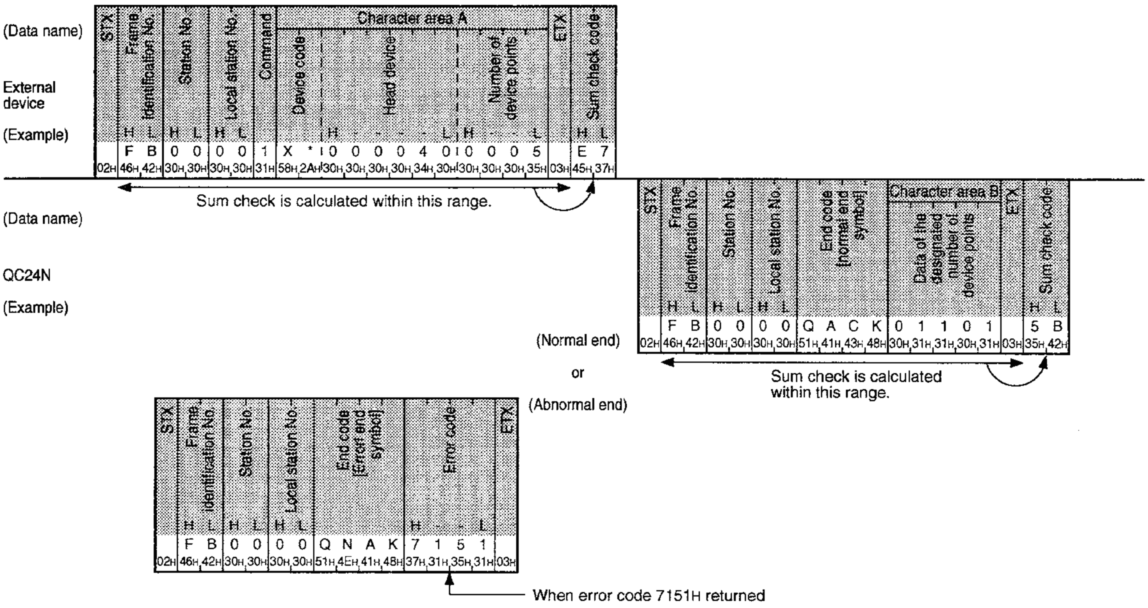
(Example) Using a command 3, the external device writes five points data to M903 to M907 of the QnACPU:



3 Communication using control procedure format 3

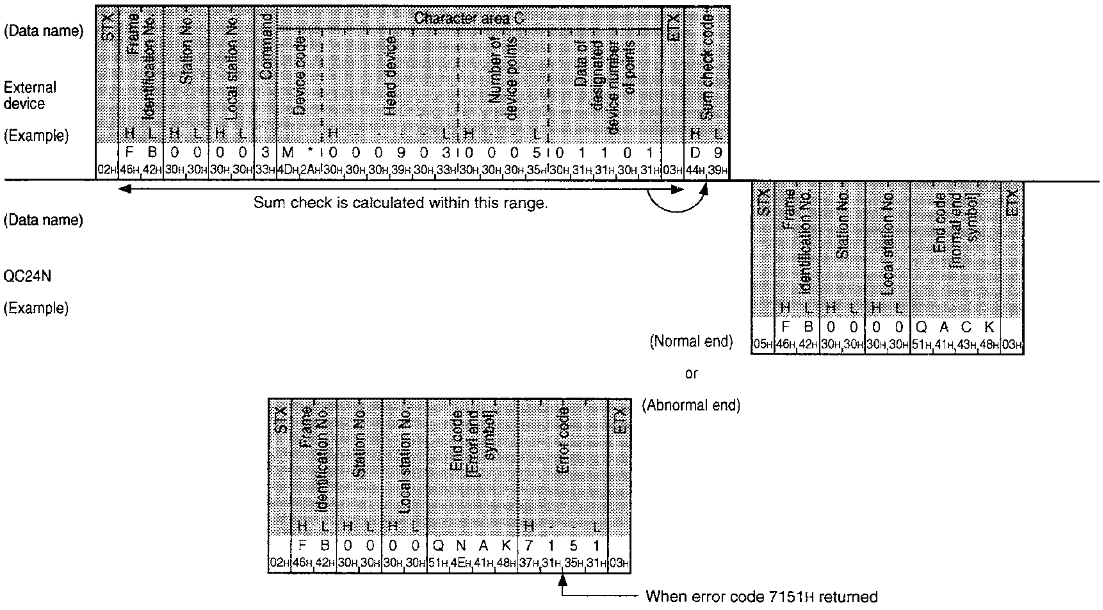
① When the external device reads data from QnACPU

(Example) Using a command 1, the external device reads five points data from X 40 to X 44 of the QnACPU:



② When the external device writes data to QnACPU

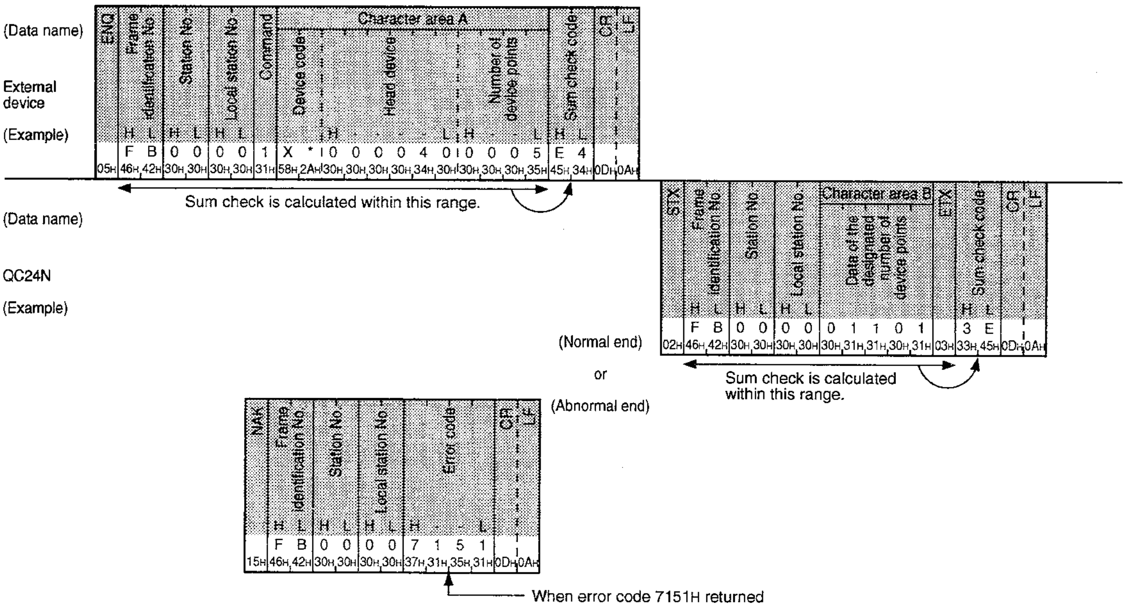
(Example) Using a command 3, the external device writes five points data to M903 to M907 of the QnACPU:



4 Communication using control procedure format 4

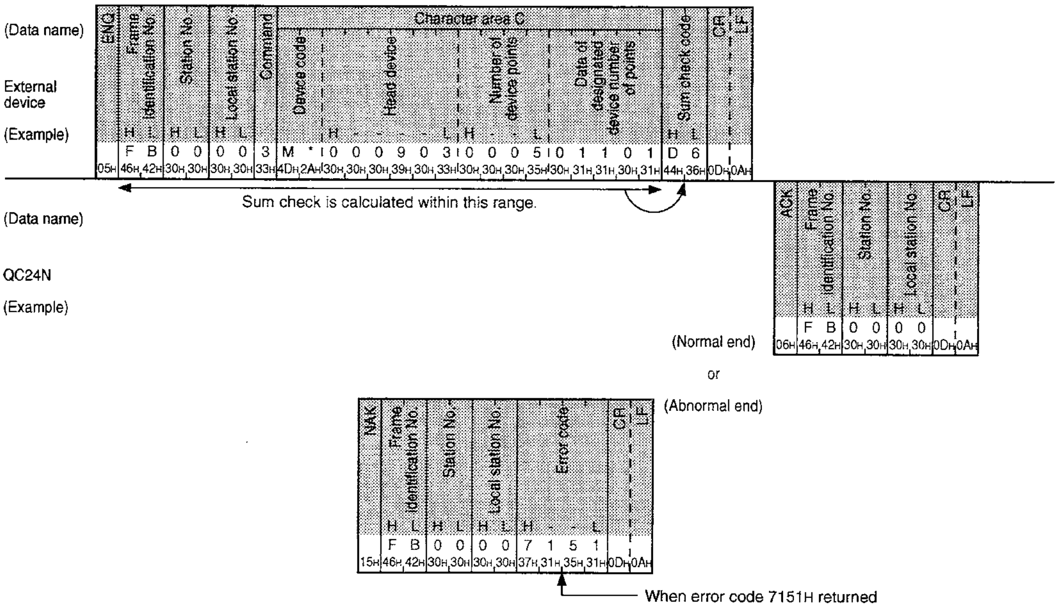
① When the external device reads data from QnACPU

(Example) Using a command 1, the external device reads five points data form X 40 to X 44 of the QnACPU:



② When the external device writes data to QnACPU

(Example) Using a command 3, the external device writes five points data to M903 to M907 of the QnACPU:



8.4.2 Contents of the data designation items

Among the designations of the data name designated by the control procedure in each format of the QnA simplified frame, the contents of the data name dedicated to the QnA simplified frame that are different from those of the QnA frame and QnA extension frame are described.

POINT

The data names other than those shown in this section use the same designation method which is used for the communication by the QnA frame and the QnA extension frame.
See Section 6.1.4 of this manual.
For details on "message wait" time for data communication, see the remarks at the bottom portion of Section 6.1.4 (11).

1 **Frame identification number**

When the communication is executed by the QnA simplified frame, "FB" is used as the frame identification number.

Mode	Frame	Frame identification No.
ASCII mode	QnA frame	"F 9"
	QnA extension frame	"F 8"
	QnA simplified frame	"F B"
Binary mode	QnA extension frame	F 8 H

2 **Command**

One of the commands from "1" to "9" for the QnA simplified frame (See Section 8.3) that corresponds to the function to be used is transmitted as one digit of ASCII code.

3 **Character area (area A, area B, area C)**

The character area use the same designation method and contents as those for the communication by the QnA frame and QnA extension frame.

It depends on the command transmitted from the external device.

The following table shows the QnA simplified frame commands and the corresponding QnA (extension) frame commands whose designation method of the character area is the same as the QnA simplified frame.

Command		QnA simplified frame command	QnA (extension) command which corresponds to the command to the left	
			Command	Subcommand
Batch read	Bit units	1	0401	0001
	Word units	2	0401	0000
Batch write	Bit units	3	1401	0001
	Word units	4	1401	0000
Random read	Word units	5	0403	0000
Test (Random write)	Bit units	6	1402	0001
	Word units	7	1402	0000
Monitor data registration	Word units	8	0801	0000
Monitor	Word units	9	0802	0000

Designate the character area of the command to be used according to Section 6.2 in this manual.

8.4.3 Precautions for the data communication

The precautions for the data communication by the QnA simplified frame are as follows:

(1) Precautions for each format are the same as those for the communication by the QnA frame or QnA extension frame.

See Sections 6.1.1 and 6.1.2 in this manual.

(2) The monitoring conditions for reading data which can be designated by the communication of the QnA frame or the QnA extension frame cannot be designated by the communication by the QnA simplified frame.

In addition, the extension setting of the device memory to read and write is not allowed, either.

(3) When the data is communicated by the QnA simplified frame, the number of points and range of read and write for each command are the same as those when the corresponding QnA (extension) frame command is used.

(The designation method of the character area and the contents are the same.)

The QnA (extension) frame commands which correspond to the QnA simplified frame commands are listed in Section 8.4.2 of this chapter.

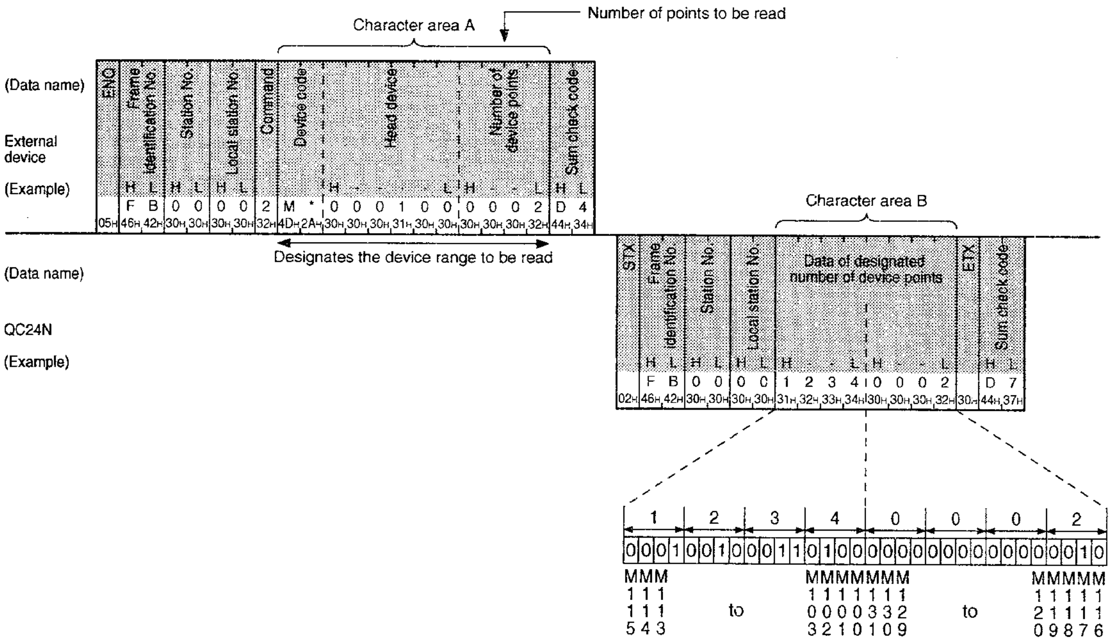
8.5 Example of Data Communication by the QnA Simplified Frame

The control procedure of the data communication by the QnA simplified frame is shown in format 1.

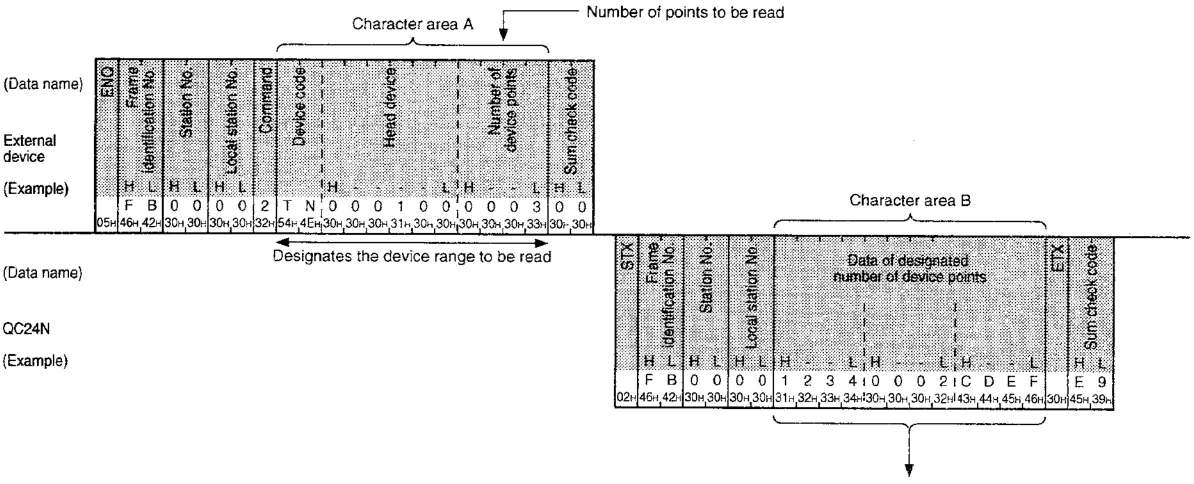
See Section 8.4.1 for examples of the control procedures using command 1 and 3.

1 Batch read in word units (Command: 2)

(a) When reading two points (32 bits) from internal relays M100 to M131



(b) When reading the current value of three points from timer T100 to T102

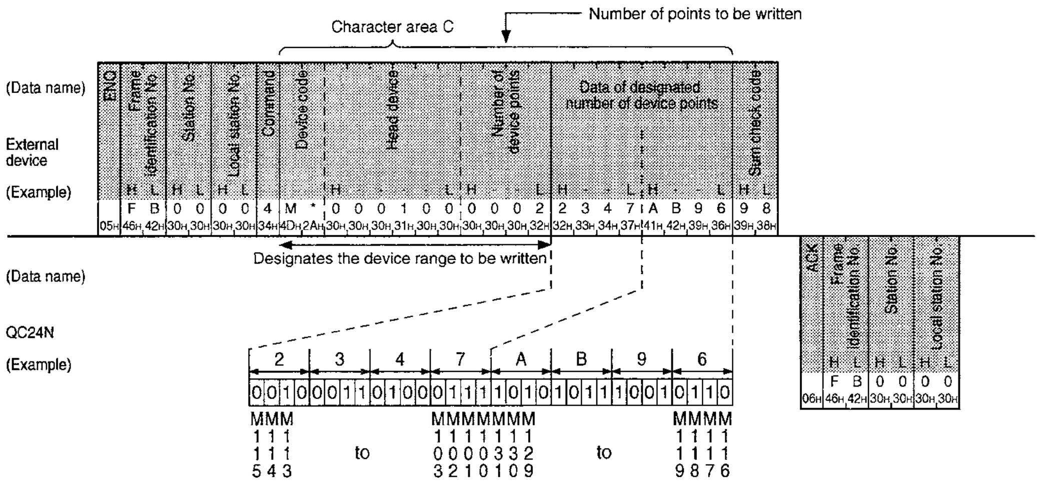


Indicates that the T100 current value 1234H (hexadecimal) is 4660 in decimal.
Indicates that the T101 current value 0002H (hexadecimal) is 2 in decimal.
Indicates that the T102 current value CDEFH (hexadecimal) is -12817 in decimal.

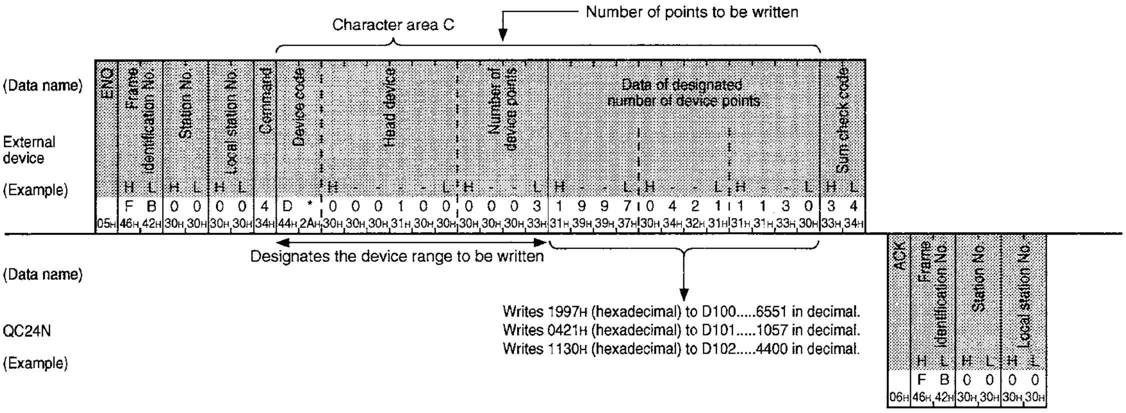
* The designation method and contents for the character area of command 2 are the same as that of the QnA (extension) frame command 0401 (subcommand 0000).

2 Batch write in word units (Command: 4)

(a) When writing two points (32 bits) to internal relays M100 to M131



(b) When writing three points to D100 to D102

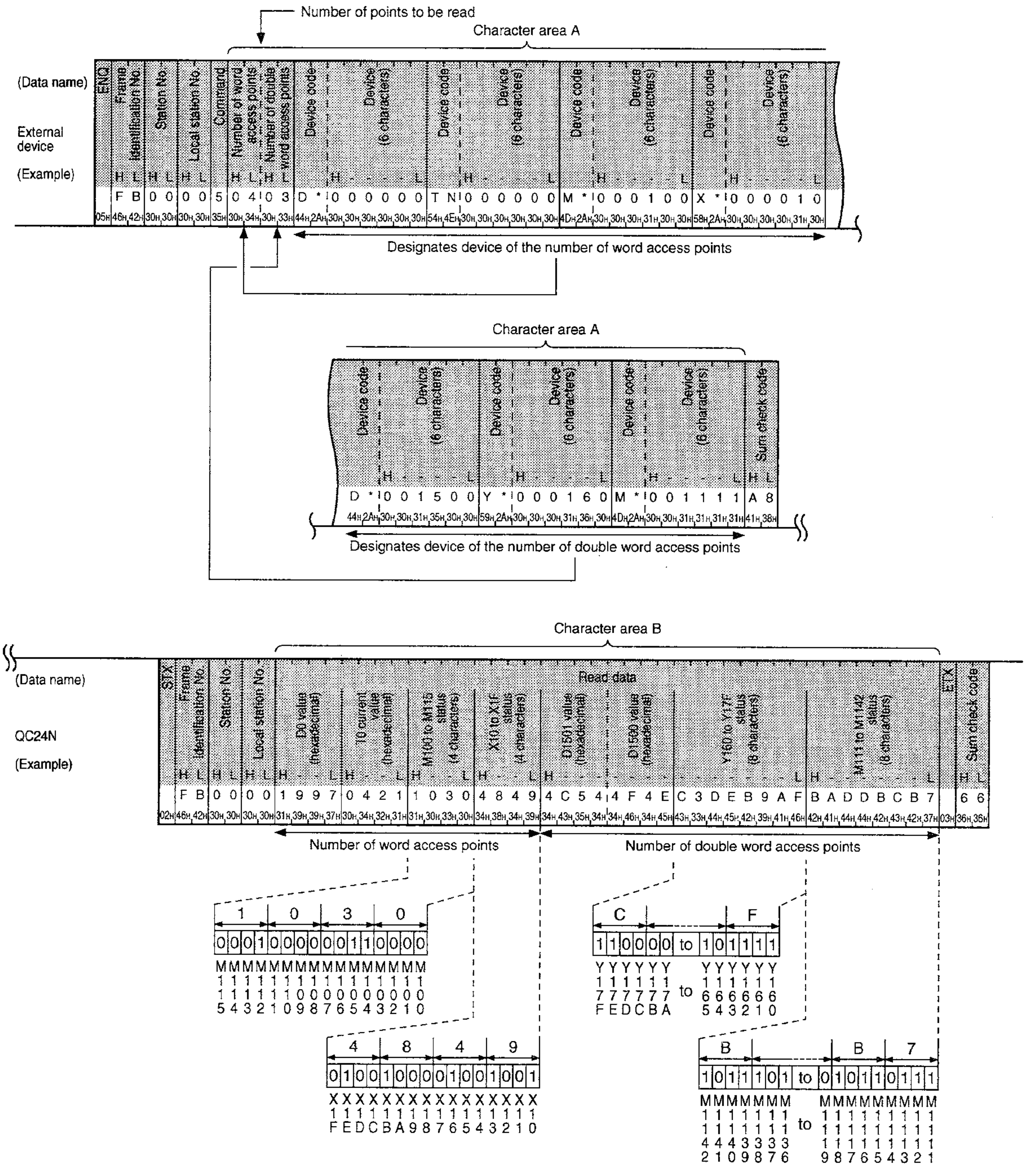


* The designation method and contents for the character area of command 4 are the same as that of the QnA (extension) frame command 1401 (subcommand 0000).

3 Random read in word units (Command: 5)

When reading the following device memories

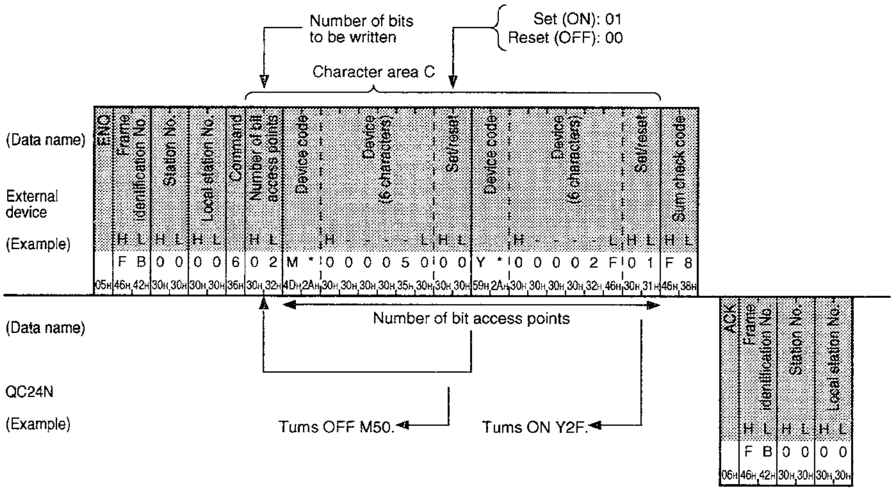
- Word access : D0, T0, M100 to M115, X10 to X1F
- Double word access : D1500 to D1501, Y160 to Y17F, M1111 to M1142



* The designation method and contents for the character area of command 5 are the same as that of the QnA (extension) frame command 0403 (subcommand 0000).

4 Test in bit units (Command: 6)

When turning off internal relay M50 and turning on output relay Y2F

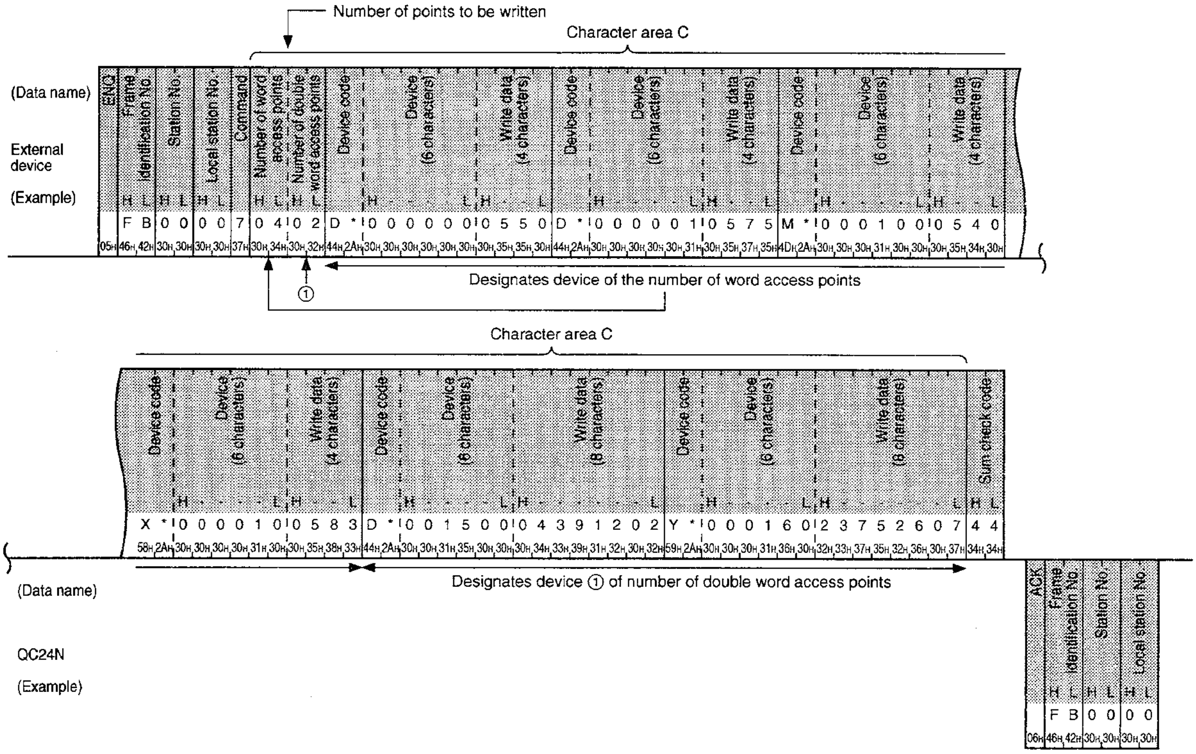


* The designation method and contents for the character area of command 6 are the same as that of the QnA (extension) frame command 1402 (subcommand 0001).

5 Test in word units (Command: 7)

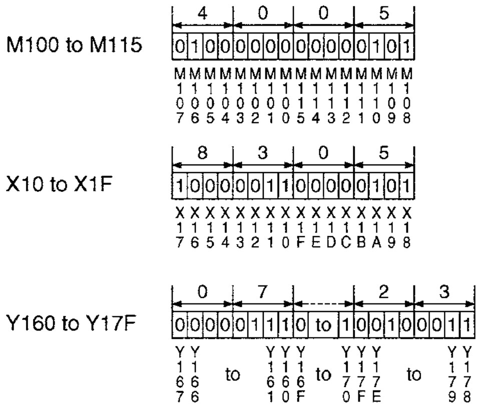
When writing the following device memories

- Word access : D0, D1, M100 to M115, X10 to X1F
- Double word access : D1500 to D1501, Y160 to Y17F



* The designation method and contents for the character area of command 7 are the same as that of the QnA (extension) frame command 1402 (subcommand 0000).

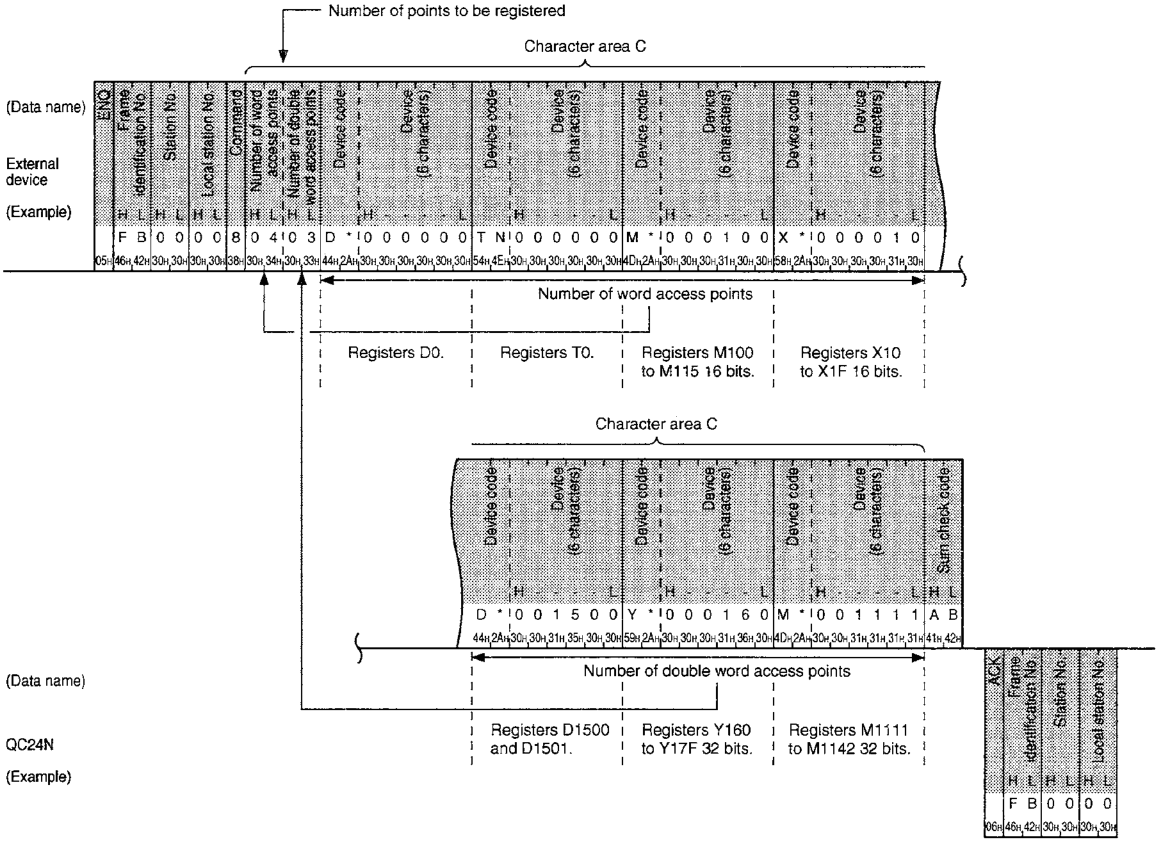
The correspondence between the data to be tested by each word units and the bit device is as follows:



6 Monitor data registration in word units (Command: 8)

When registering the monitor data for the following device memories

- Word access : D0, T0, M100 to M115, X10 to X1F
- Double word access : D1500 to D1501, Y160 to Y17F, M1111 to M1142



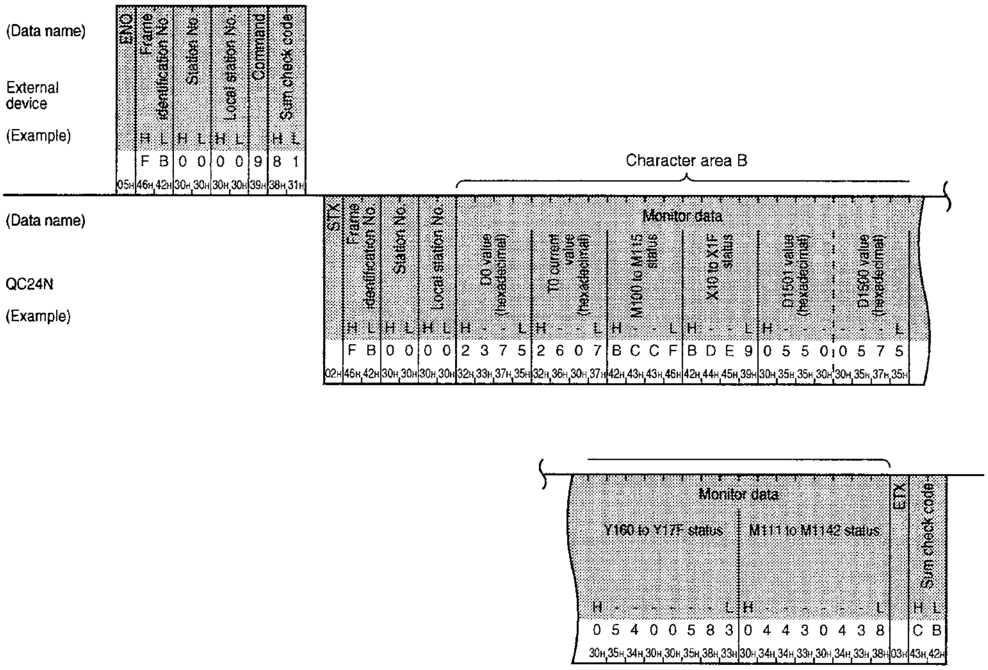
* The designation method and contents for the character area of command 8 are the same as that of the QnA (extension) frame command 0801 (subcommand 0000).

7 Monitor in word units (Command: 9)

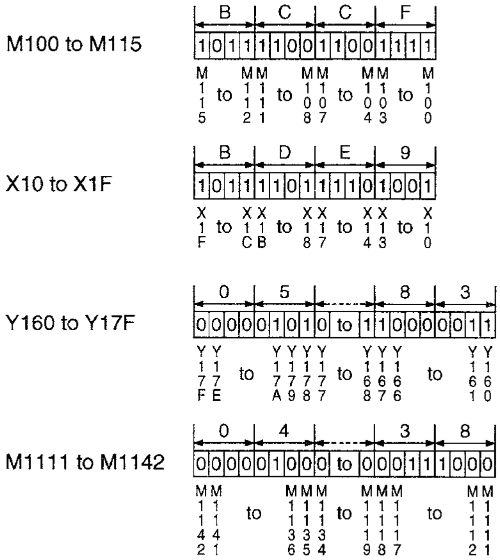
When monitoring the following device memories with monitoring data registered

(Device memories with monitor data registered)

- Word access : D0, T0, M100 to M115, X10 to X1F
- Double word access : D1500 to D1501, Y160 to Y17F, M1111 to M1142



The correspondence between the bit device which is registered as monitor data and the data actually read is as follows:



* The contents for the character area of command 9 is the same as that of the QnA (extension) frame command 0802 (subcommand 0000).

MEMO

NON PROCEDURE PROTOCOL

This section gives a general description of each function and describes the data communications procedures, etc. for using the non procedure protocol to exchange data between external device and PLC CPU through the serial communications module.

When using the non procedure protocol to transmit data, first read Chapter 9 for common information.

When transmitting and receiving data without selecting the message data list, but by using an arbitrary format each time, read Chapter 9 and 10.

When transmitting and receiving data by selecting the message data list, read Chapter 9 and 11.

When designating mode 6 by setting the QC24(N) mode switch to "6", or by mode switching, and using the relevant interface with the non procedure protocol, always read this section.

When using a dedicated protocol or the bidirectional protocol, you do not have to read this section.

9. DATA COMMUNICATIONS USING NON PROCEDURE PROTOCOL

This data communications function uses the user communication protocol to exchange arbitrary data between external device and PLC CPU.
The user selects the format and communications timing of the message transmitted and received by the external device and PLC CPU.
Sequence programs that transmit data, receive data, and read the received data are necessary at the PLC CPU.

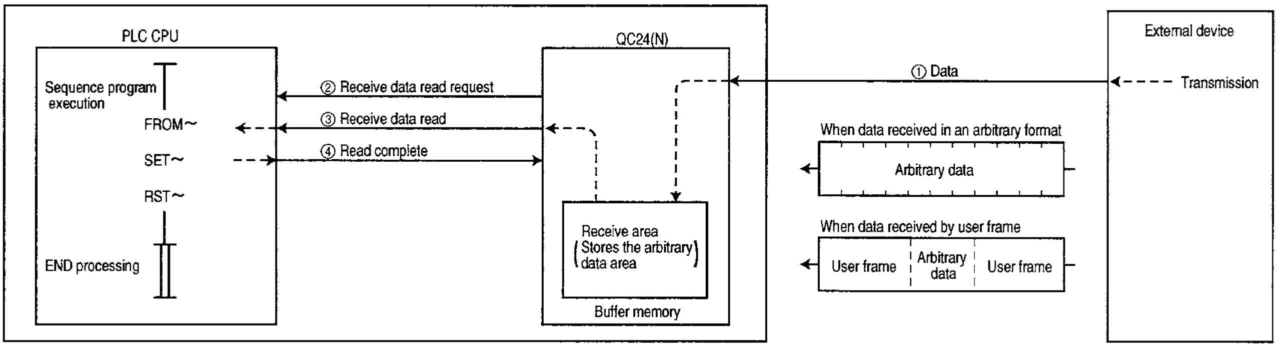
9.1 Non Procedure Protocol PLC CPU Access Timing

The following shows the PLC CPU processing flow when data is exchanged between external device and PLC CPU.
ⓝ in the illustration shows the processing flow sequence.

1 When the PLC CPU receives data from an external device

The QC24(N) reads the data received from the external device from its buffer memory to the PLC CPU when the receive data read request signal (input signal) between the PLC CPU and QC24(N) changes from OFF to ON.

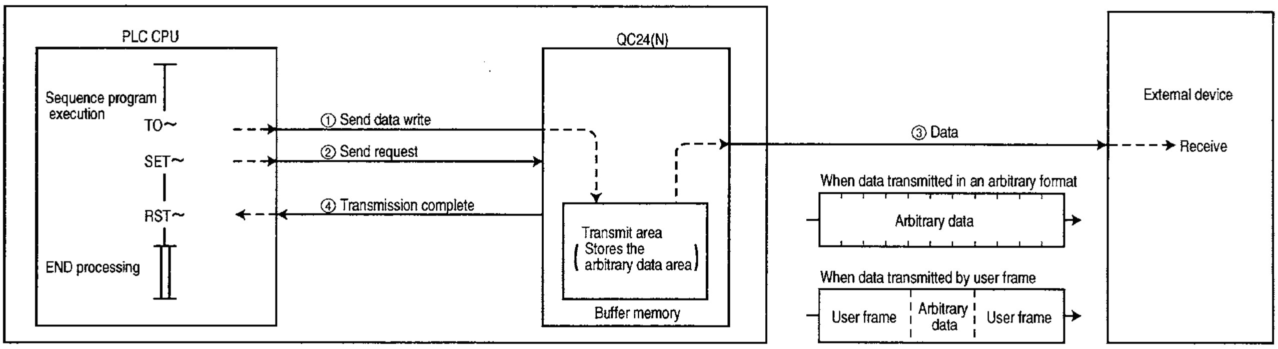
(Processing flow when data received from external device)



2 When PLC CPU transmits data to an external device

The QC24(N) transmits the send data written to its buffer memory to the external device when the send request signal (output signal) between the PLC CPU and the QC24(N) changes from OFF to ON.

(Processing flow when data transmitted to external device)



9.2 Communications Functions

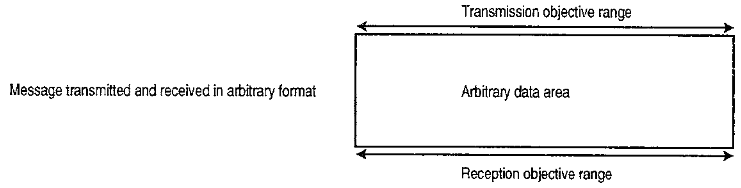
The table below lists the functions for using the non procedure protocol to transmit data between an external device and the PLC CPU.

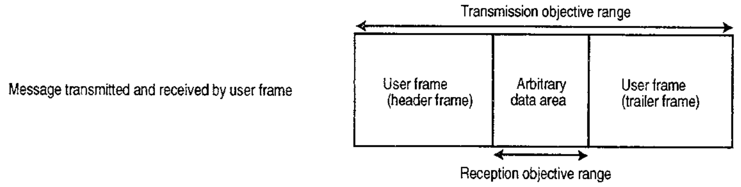
Function		Processing	Reference section
Transmitting and receiving in an arbitrary format	Transmit (PLC CPU →external device)	Transmits the data written to buffer memory by TO instruction, etc. to the external device and completes transmission processing.	Chapter 9 Chapter 10
	Receive (External device→PC CPU)	Stores the data received from the external device to the QC24(N) buffer memory and sends a read request to the PLC CPU.	
Transmitting and receiving by user frame	Transmit (PLC CPU →external device)	Adds a user frame matched to the specifications of the external device to the data written to the QC24(N) buffer memory by TO instruction, etc. and transmits the data to the external device and completes transmission processing.	Chapter 9 Chapter 11
	Receive (External device→PC CPU)	When data containing a user frame matched to the specifications of the external device was received from an external device, stores the arbitrary data area to buffer memory and sends a read request to the PLC CPU.	
Transmitting and receiving by ASCII-BIN conversion *1		Converts the data designated by the user from ASCII to BIN data. During transmission, converts the designated data range to ASCII data and transmits the ASCII data. During reception, stores the arbitrary data of the receive data to binary data and stores the binary data to buffer memory.	Chapter 10 Chapter 11
Transmitting and receiving by transparent code designation *2		Transmits and receives data by adding the (additional code) data designated by the user immediately before the (transparent code) data designated by the user. During transmission, adds additional code data immediately before the transparent code data within the designated data range and transmits the data. During reception, when additional code data is detected in arbitrary data of the receive data, removes the additional code data and performs receive processing.	

*3

Note

The transmit/receive message ASCII-BIN conversion and transparent code designation additional code addition/deletion objective ranges are shown below.





*1 This function treats all the data transmitted and received by the PLC CPU as binary data.

During data communications using an arbitrary format and data communications using user frames, the QC24(N) transmits and receives the data shown in (1) and (2) by setting to buffer memory ASCII-BIN conversion designation area (address: 121H/1C1H).

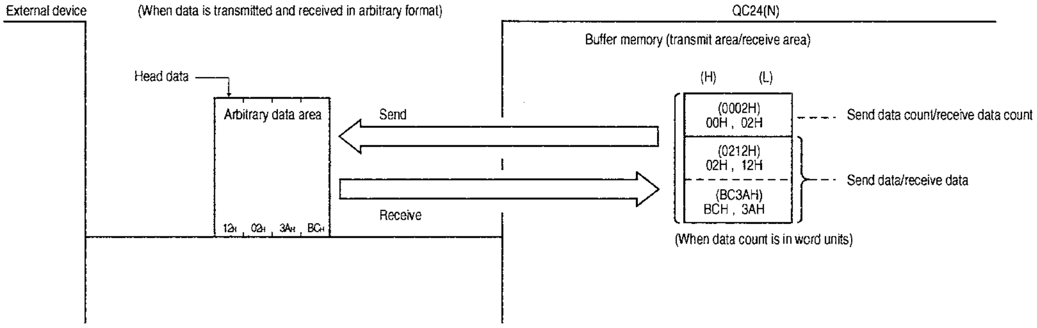
POINT

During transmission, the user frame part of the send and receive data is transmitted as unconverted/converted data, based on the data corresponding to the contents registered to the QC24(N).
During reception, the user frame part is received as unconverted data.
During data transmission by user frame, the arbitrary frame and arbitrary data areas can be transmitted without performing conversion even when ASCII-BIN conversion is set.
Sections 9.4.1 2 (b) *2 and 9.6.2 1 (5) describe the designation method.

1 When ASCII-BIN conversion not designated (No conversion)

① Data codes 00H to FFH are transmitted and received as the user frame and arbitrary data areas.

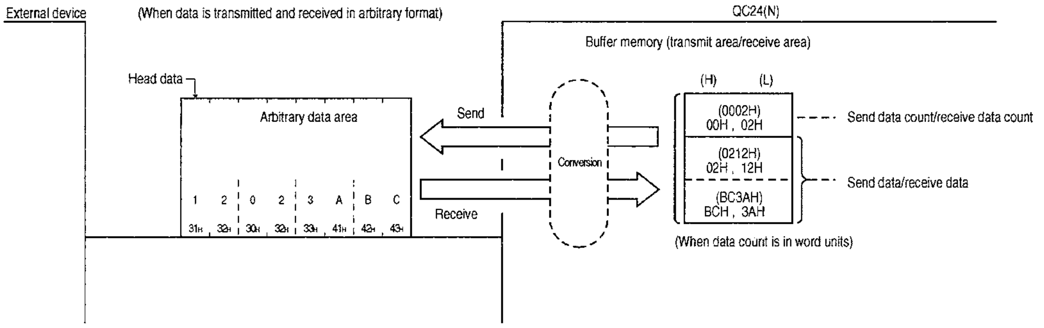
② During data reception, the arbitrary data area is stored to the QC24(N) buffer memory unchanged.
During data transmission, data designated by the PLC CPU (arbitrary data area of transmit message) is transmitted unchanged.



2 When ASCII-BIN conversion designated

① Data codes 30H to 39H ("0" to "9") and 41H to 46H ("A" to "F") are transmitted and received as data within the conversion objective range given on the next page.

② During data reception, the arbitrary data area is assumed to be ASCII data and is converted to binary data and stored to the buffer memory.
The user frame area is received as data corresponding to the contents registered to the QC24(N).
During data transmission, the data designated by the PLC CPU (arbitrary data area of transmit message) and the user frame area are assumed to be binary data and are converted to ASCII data and transmitted.



*2 This function treats the 1-byte data for transmission control of the external device as user data.

During data communications in an arbitrary format and data communications using user frames, the QC24(N) transmits and receives the additional code and transparent code designated data described in $\boxed{1}$ and $\boxed{2}$ by setting the following code to the buffer memory transmit/receive transparent code designation area (address: 11FH to 120H/1BFH to 1C0H).

- Transparent code .... 1-byte data code for transmission control
- Additional code .... 1-byte data code added immediately before the transparent code and additional code data during transmission.
  This 1-byte data code is removed during reception (The one byte of data immediately preceding this code is received.)

$\boxed{1}$ When transparent code not designated

The QC24(N) transmits and receives the send/receive data without performing the processing described in $\boxed{2}$ below.

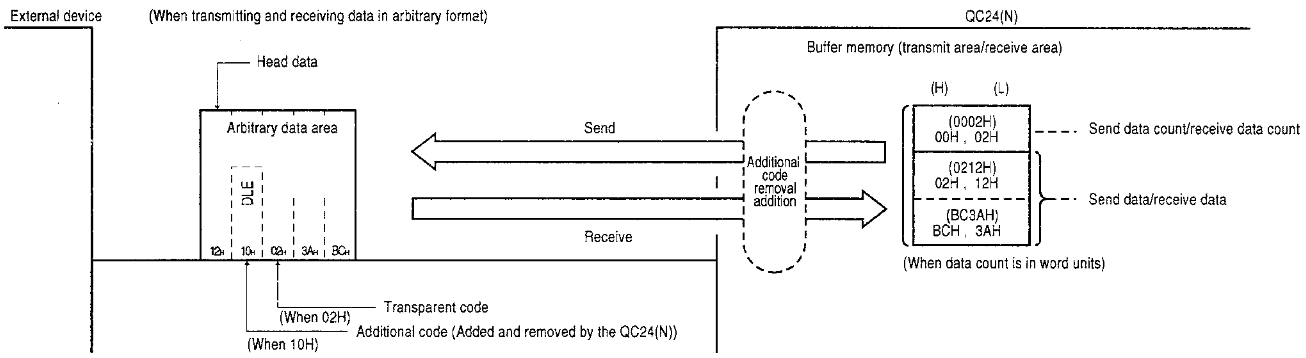
$\boxed{2}$ When transparent code designated

① The QC24(N) adds and removes the additional code designated data.
The data within the objective range shown in Section 9.2 [Note] is the objective.
During data transmission by user frame, data can be transmitted without adding the addition code data to the arbitrary frame area and arbitrary data area data even when transparent code is designated.
Sections 9.4.1 $\boxed{2}$ (b) *2 and 9.6.2 $\boxed{1}$ ⑤ describe the designation method.

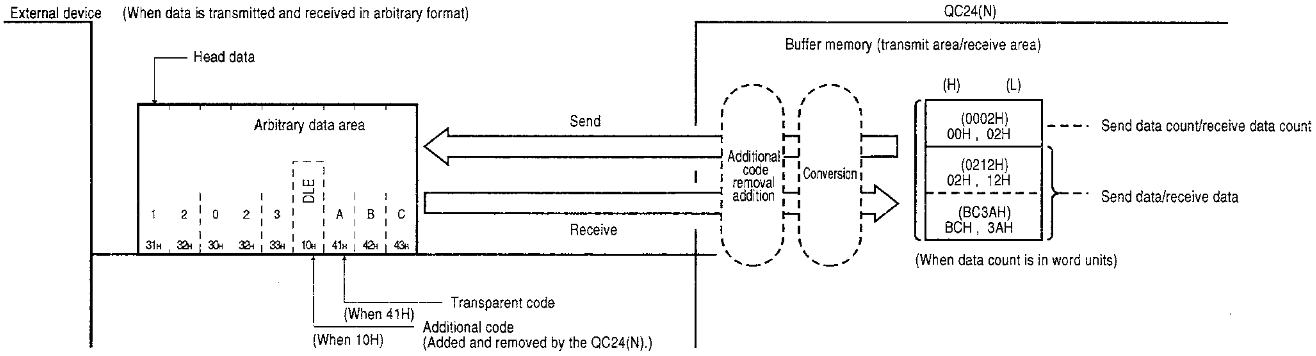
② When the QC24(N) detects a receive additional code use while receiving data, it removes the additional code data and processes the data of the one byte immediately following the additional code data as part of the receive data.

③ When the QC24(N) detects transmit transparent code/addition code data set during data transmission, it adds the additional code designation data immediately before this data.

(Example) When ASCII-BIN conversion not performed



(Example) When ASCII-BIN conversion performed



*Transparent code and additional code can set one kind of each send/receive to QC24(N) according to the specification of external device.

POINT

When additional code data is received during data reception, the QC24(N) does not assume that the 1 byte of data immediately following the additional code data for the following control:

- Data received as user frame header frame and trailer frame (See Sections 16.1 and 16.2.)
- Receive end code data (See Section 9.3.1 $\boxed{1}$ (a).)

Therefore, do not make the following settings.
(The codes of the data mentioned above cannot be designated as receive additional code.)

① Receive user frame containing receive additional code
② Receive end code the same as the receive additional code

*3 The QC24(N) processing sequence when data is transmitted and received by ASCII-BIN conversion and transmitted and received by transparent code.

1 Transmitting and receiving in an arbitrary format

(a) Receive

① If receive transparent code is designated, the QC24(N) removes the additional code designation data.

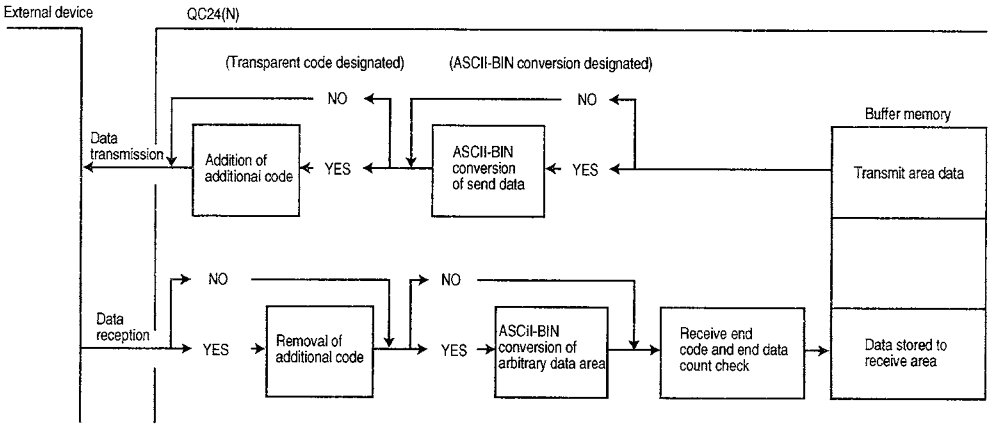
② The QC24(N) stores the arbitrary data area to its buffer memory receive area.
If ASCII-BIN conversion is designated, the QC24(N) converts the received data is converted to binary data, then stores it to buffer memory.

③ When receive end code data is stored, or receive end data count, is stored while the arbitrary data area is being received, the QC24(N) sends a read receive data request to the PLC CPU.

(b) Transmitting

① The QC24(N) transmits the send data (arbitrary data area of transmit message) written to the transmit area of its buffer memory by the PLC CPU.
If ASCII-BIN conversion is designated, the QC24(N) converts the data to ASCII data, then transmits the ASCII data.

② If transmit transparent code is designated, the QC24(N) adds the additional code data immediately before the transparent code/additional code data before transmission.



2 Transmitting and receiving by user frame

(a) Receiving

① The QC24(N) checks if a user frame (header frame, trailer frame) was received.

② If receive transparent code is designated, the QC24(N) removes the additional code designation data from the arbitrary data area.

③ If the sum check code is designated in the user frame (trailer frame), the QC24(N) calculates the sum check.

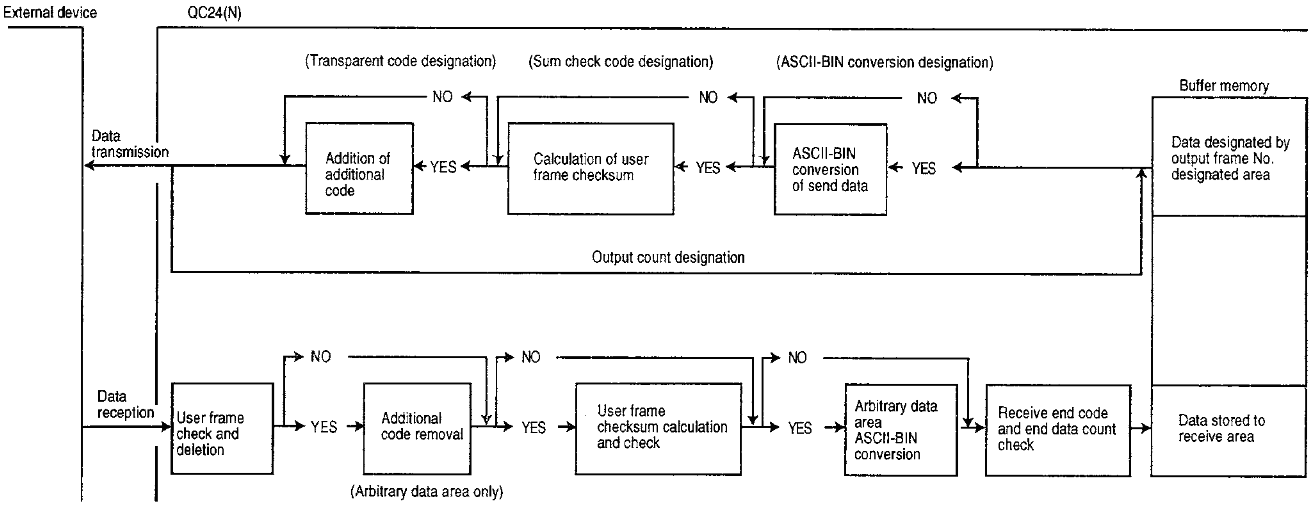
④ The QC24(N) stores the arbitrary data area to its buffer memory receive area. If ASCII-BIN conversion is designated, the QC24(N) converts the data to binary data, then stores it to the buffer memory.

⑤ When receive end code/receive byte count is stored, or a user frame (trailer frame) is received while the arbitrary data area is being received, the QC24(N) requests the PLC CPU to read the receive data.

(b) Transmitting

① The QC24(N) transmits the user frame and send data (arbitrary data area of the transmit message) written to the transmit area of the buffer memory by the PLC CPU in the order designated by the user.

② If ASCII-BIN conversion is designated, the QC24(N) converts the data within the objective range given in Section 9.2 [Note] to ASCII data before transmitting it. If transmit transparent code is designated, when data within the objective range given in Section 9.2 [Note] is transmitted, the QC24(N) adds the additional code data immediately before the transparent code/additional code data.



POINT

The above is the QC24(N) transmit/receive data processing sequence when the user frame transmit/receive functions, ASCII-BIN conversion function, and transparent code designation transmit/receive functions are used and not used.
See it when selecting the transmit/receive method when exchanging data with an external device.

9.3 Receiving Data from an External Device

This section describes the common information you should know to read the data received from an external device from the PLC CPU.

9.3.1 Data reception

The following describes the methods used by the QC24(N) to read data received from an external device. The user can arbitrarily choose method.
In all cases, the QC24(N) reads the data received from the external device from the receive data storage area.

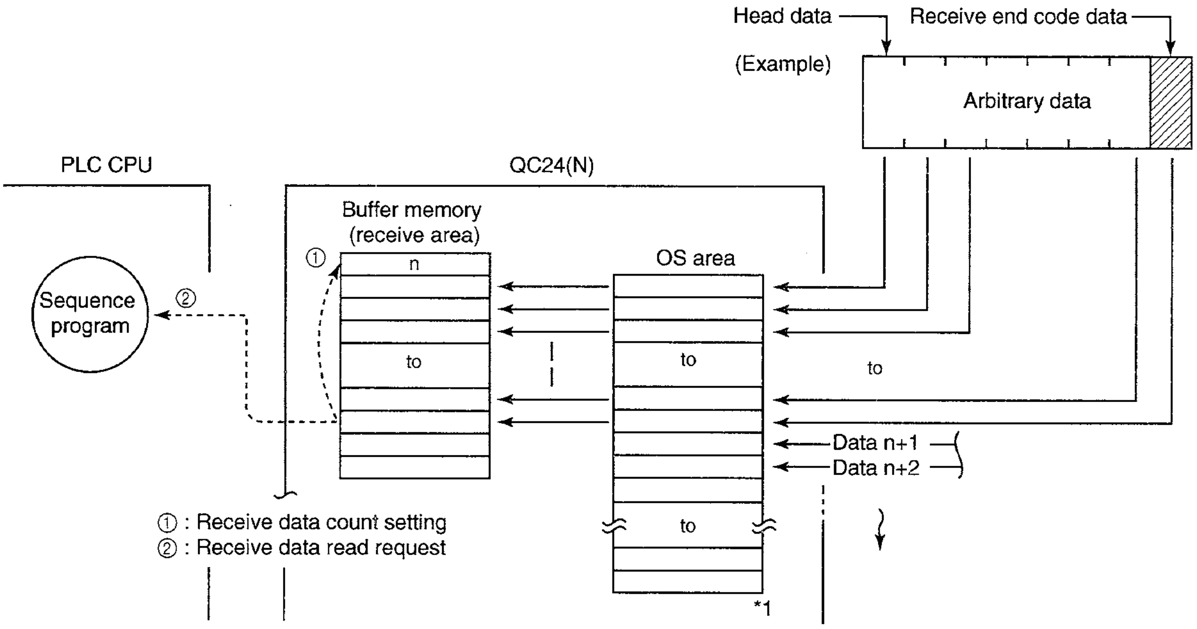
- Reception by receive end code
- Reception by receive end data count
- Reception by trailer user frame

The following describes the data reception method when data is received in an arbitrary format and when data is received by user frame.

1 When data is received in an arbitrary format

(a) Data reception by receive end code (for variable length reception)

When the QC24(N) receives the receive end code data preset in the buffer memory (addresses A5H/145H) by the user, it sends a receive data read request to the sequence program.
The read request from the QC24(N) allows the sequence program to read the receive data up to the receive end code received from the external device.
The receive end code can be changed to match the specifications of the external device. An arbitrary 1-character (1-byte) code within the 00H to FFH range can be designated. (See Section 14.8.3 for a description of the modification method.)

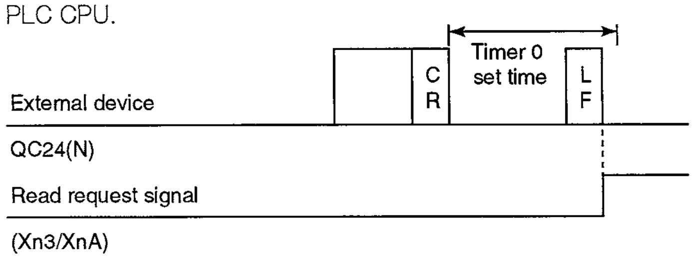


The data received from the external device after the QC24(N) sent a receive data read request to the PLC CPU is stored to the QC24(N) OS area (*1) as data to be read from the next time.
In the descriptions, the CR code is 0DH and the LF code is 0AH.

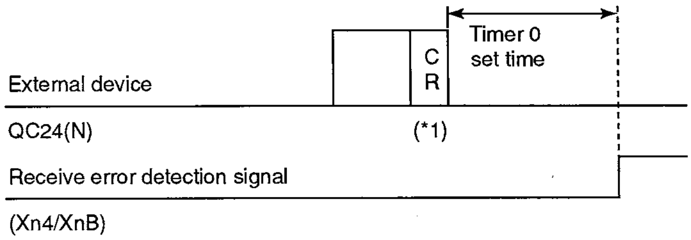
In the following cases, the QC24(N) issues a receive data read request to the PLC CPU according to the value set in the buffer memory receive end code designation area.

① When receive end code not changed (Default value: 0D0AH)

ⓐ If LF is received within the time set in the no reception watchdog timer (timer 0) after CR is received, the QC24(N) stores the receive data up to CR+LF to the buffer memory receive data storage area and turns on the read request signal to the PLC CPU.

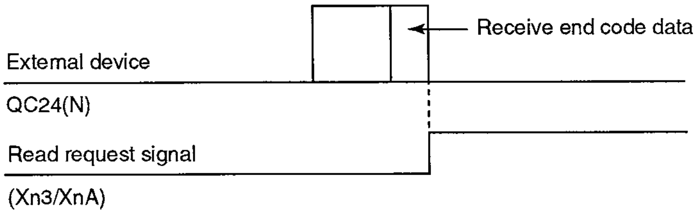


ⓑ If the next data (LF, etc.) is not received within the time set in the no reception watchdog timer (timer 0) after CR is received, the QC24(N) stores the receive data up to CR to the buffer memory receive data storage area of buffer memory and the turns on the receive error detection signal to the PLC CPU.



*1 At this time, CR is handled as 1-byte data included in the message.

② When the receive end code is changed and an arbitrary code is designated (00□□H designated)
When the QC24(N) receives the receive end code data changed by the user, it stores the receive data up to the receive end code to the buffer memory receive area and turned on the read request signal to the PLC CPU.



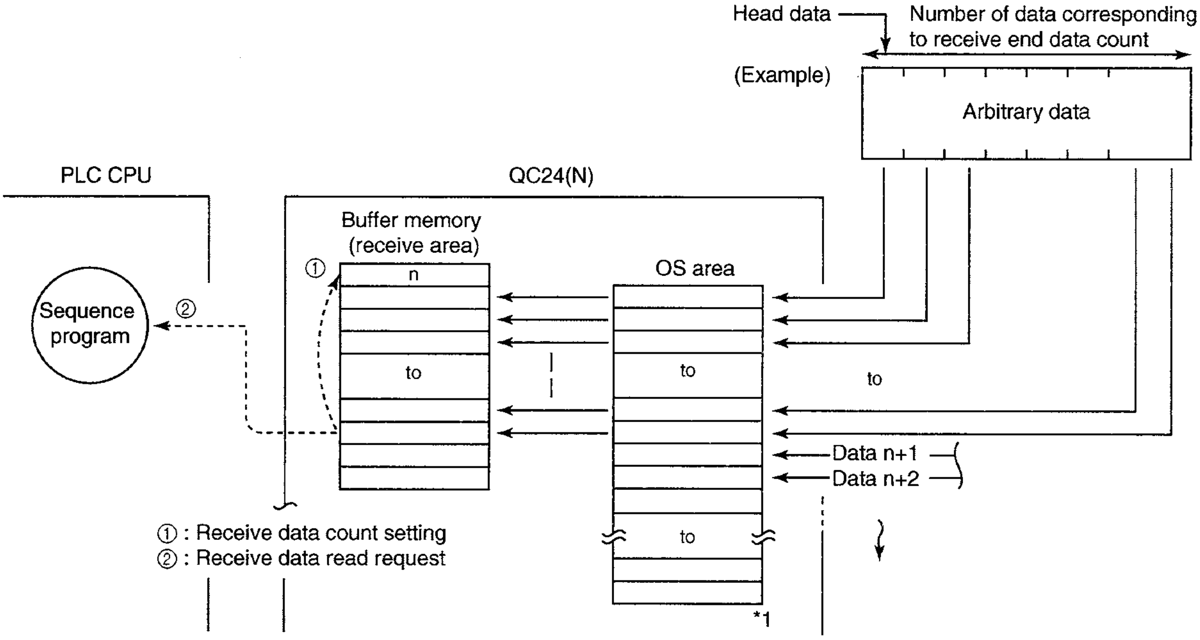
③ When receive end code not designated (FFFFH designated)
Reading by receive end data count is enabled.
See (b) for a description of reading by receive end data count.

POINT

When ASCII-BIN conversion is designated, the receive end code is designated by the code (converted data code) after the receive data is converted to binary data.

(b) Reception by receive end data count (For fixed length reception)

When the QC24(N) receives data of the receive end data count preset in the buffer memory (address A4H/144H) by the user, it sends a receive data read request to the sequence program.
When the sequence program receives the receive data read request from the QC24(N), it reads data up to the receive end data count received from the external device.
The receive end data count default value is set to 511 (words). However, it can be changed within the size of the receive data storage area depending on the data contents exchanged with the external device. (See Section 14.8.2 for a description of the modification method.)



POINTS

(1) When the receive end code and receive end data count are set to the special applications area of buffer memory, both become valid.
In this case, if the QC24(N) receives the receive end code before data corresponding to the receive end data count, it outputs (Xn3/XnA: ON) a read request to the sequence program.

(2) When ASCII-BIN conversion is designated, the receive end data count is designated by byte number of bytes after the receive data was converted to binary data.

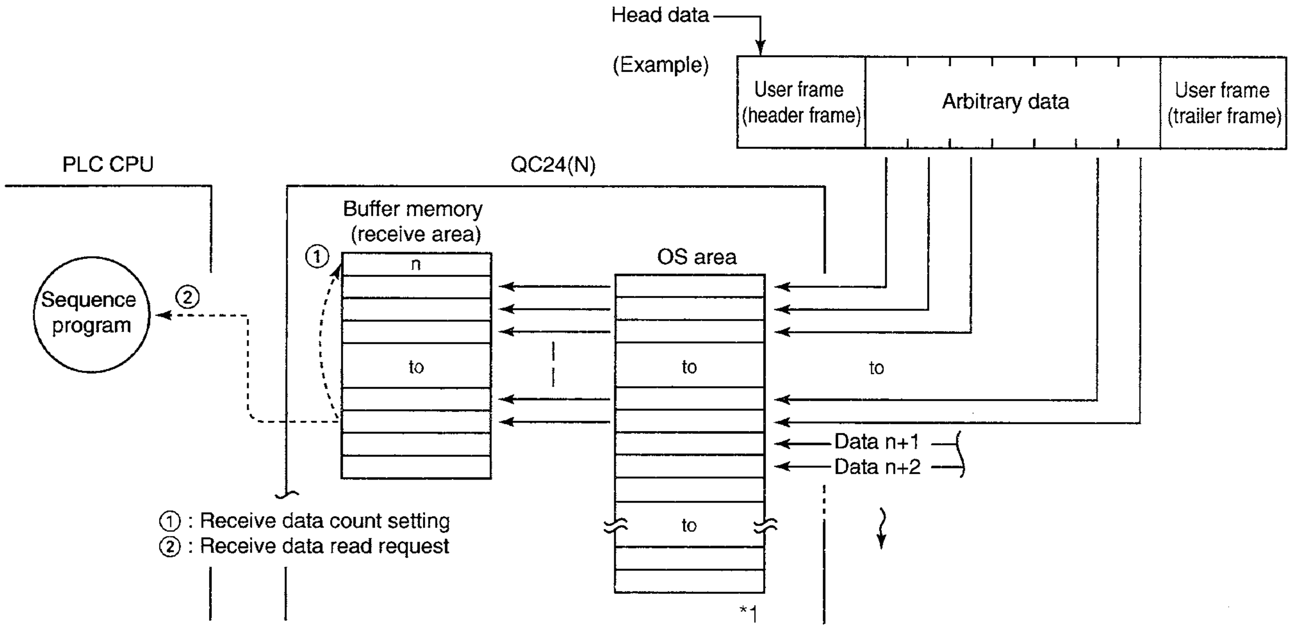
2 Reception by user frame (For variable length reception)

When the QC24(N) receives data a list the same as the user frame trailer frame No. data preset to buffer memory (addresses B2H to B5H/152H to 155H) by the user, it sends a receive data read request to the sequence program.

When the sequence program receives the receive data read request from the QC24(N), it reads the arbitrary data area in the data received from the external device.

Up to 231 user frames can be registered. Any four registered user frames can be designated as trailer frames to match the specifications of the external device.

(See Chapter 14 for a description of the designation method and Chapter 16 for a description of the registration method.)



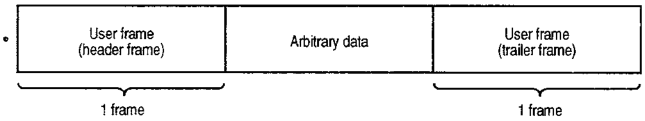
When the receive data is stored to buffer memory, user frames (header frame, trailer frame) corresponding part receive data are removed.

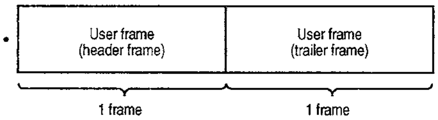
During user frame data reception, messages with the construction shown below can be received.

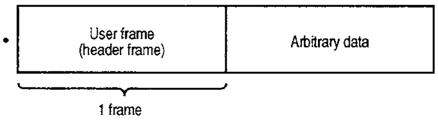
Of the registered user frames, four sets (maximum of four frames each) can be preset in the QC24(N) as the header frame and trailer frame during data reception using the non procedure protocol.

When the QC24(N) receives a message beginning with one of the combinations of the header frames designated contents and receives a message ended by the corresponding trailer frame designated contents of the set user frames (or receives the number of data corresponding to the receive end data count), it stores only the arbitrary data area of that message to the receive data storage area.

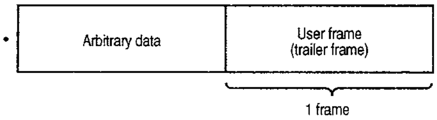
① When setting combinations (max. four combinations) that designate the header frame

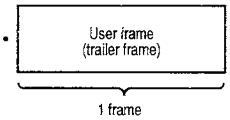






② When setting combinations (max. four combinations) that do not designate the header frame



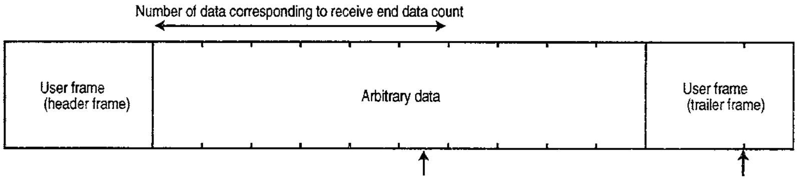


POINTS

(1) The following uses an example to describe the application of messages without arbitrary data.
Data transmission using non procedure protocol ends when all the set data are received.
When the external devices tells the PLC CPU that it has received data from the QC24(N), it sends a message without arbitrary data to the QC24(N).
Since the QC24(N) turns on the receive data read request signal to the PLC CPU even when it receives a message without arbitrary data, the external device can inform the PLC CPU that it has received data from the QC24(N).

(2) When receive end data count (see item 1 (b)) is set, when the size of the arbitrary data area exceeds the receive end data count, the QC24(N) sends a continue request to the sequence program.

(Example)



In the illustration above, two read requests are issued. (For data reception indicated by the ↑, a read request is issued.)

*1 When the QC24(N) OS area shown in the illustration is the memory (size: 4608 bytes (2304 bytes for the QC24)) that temporarily stores the data to be received next when the QC24(N) requests the PLC CPU to read the receive data.
(The user cannot read the receive data in the OS area.)
When the sequence program completes reading the buffer memory receive data currently requested by the QC24(N), the receive data in the OS area and the receive data following it are sequentially stored to the buffer memory receive area when the next reading is requested.
When the vacant OS area that stored the receive data drops below 64 bytes, the following control is implemented by transmission control designation. (See Section 14.3 for more information. The RS signal is not turned off.)

- When DTR control is set, the QC24(N) turns off the DTR signal and requests the opposite device to stop transmitting.
- When DC1/DC3 control is set, the QC24(N) sends DC3 and requests the opposite device to stop transmitting.

If the buffer memory runs out of vacant OS area and cannot store any more receive data, the module SIO LED will light and all the receive data will be ignored until vacant area becomes available.

9.3.2 Receive area and receive data list

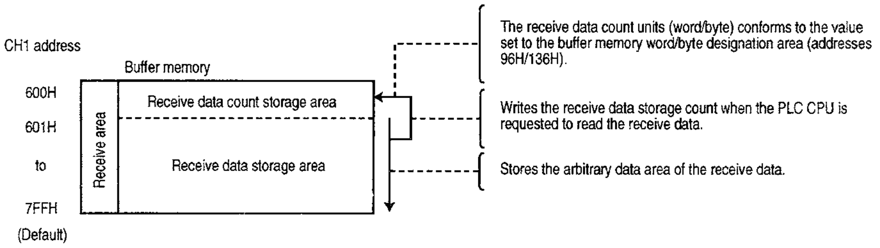
This section describes the QC24(N) buffer memory (receive area) that stores the data received from an external device and the data list when receive data is stored to the receive area.

1 Receive area

The "receive area" is a QC24(N) buffer memory area that stores the receive data and receive data count so that the PLC CPU can read the arbitrary data of a message received from an external device.

The receive area is allocated buffer memory addresses 600H to 7FFH and A00H to BFFH as the default value.

The receive area can be changed to match the purpose of data transmission, specifications of the external device, and the length of the receive data. (See Section 14.8.4 for a description of the modification method.)



POINT

Make the size of the arbitrary data area per transmission from external device to QC24(N) less than the size of the QC24(N) receive data storage area.

(Receive data storage area) ≥ (size of arbitrary data area transmitted from external device)

When you must transmit data so large that it cannot all be stored in the receive data storage area, make the receive area larger.

The receive area addresses and size can be modified.

2 Receive data list

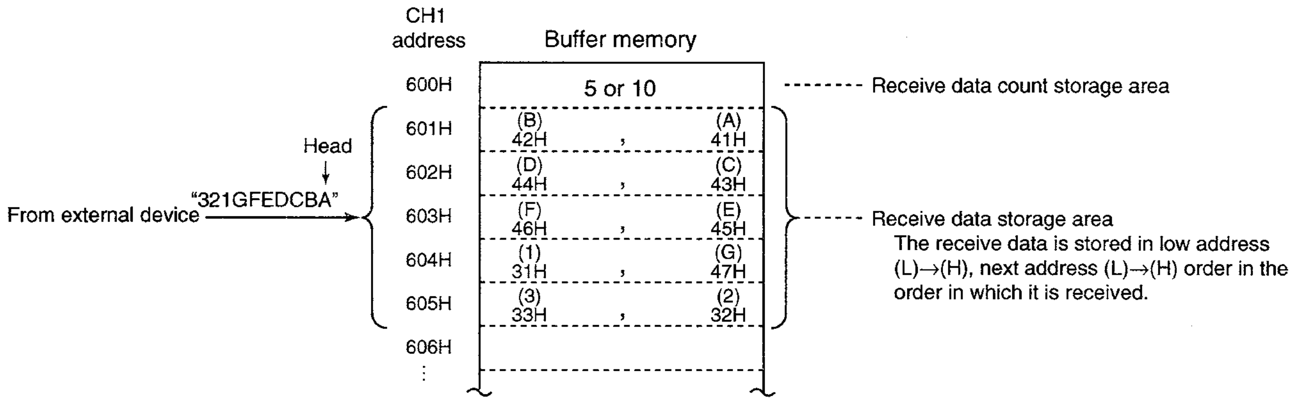
The following describes the data list when data received from an external device is stored to the receive area.

① The arbitrary data area (except the additional code data when receive transparent code is designated) of the receive message is stored to the QC24(N) buffer memory (receive data storage area).

② When ASCII-BIN conversion is designated, the data converted to binary data is stored.

③ The data is stored to the receive data storage area in low address (L) → (H), next address (L) → (H) order.

(Example) When received arbitrary data area "ABCDEFG123" was stored (The receive area is the default value.)



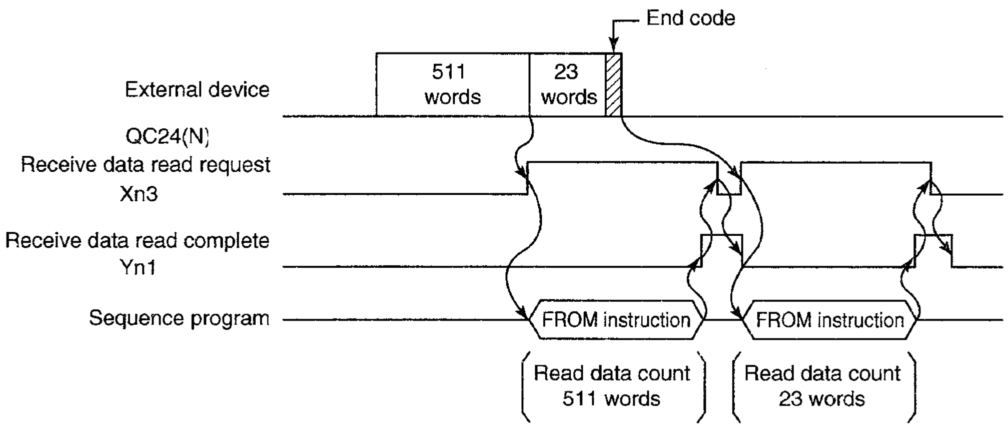
The receive data is stored in low address (L) → (H), next address (L) → (H) order in the order in which it is received.
When the receive end code, or the number of data corresponding to the receive end data count designated by the user described in Section 9.3.1 $\boxed{1}$ and $\boxed{2}$, is received, the QC24(N) turns on the receive data read request signal (Xn3/XnA) to the sequence program.

Notes

① Receive data length > receive data storage area length processing

ⓐ Reception by receive end code/user frame (trailer frame)
When the QC24(N) receives an arbitrary data area larger than the receive data storage area, when it receives data up to the receive data storage area size, it turns ON the receive data read request signal Xn3/XnA.
When the sequence program turns ON the receive data read complete signal Yn1/Yn8, reading of the remaining data is enabled and the above operation is repeated until data of the same list as the end code/user frame (trailer frame) is received.
Set the receive area so that the condition (receive data storage area) > (data length received from external device) is satisfied.

[Example] When receiving 534 words of data through the CH1 interface when the CH1 interface receive area consists of addresses 600H to 7FFH (default value)

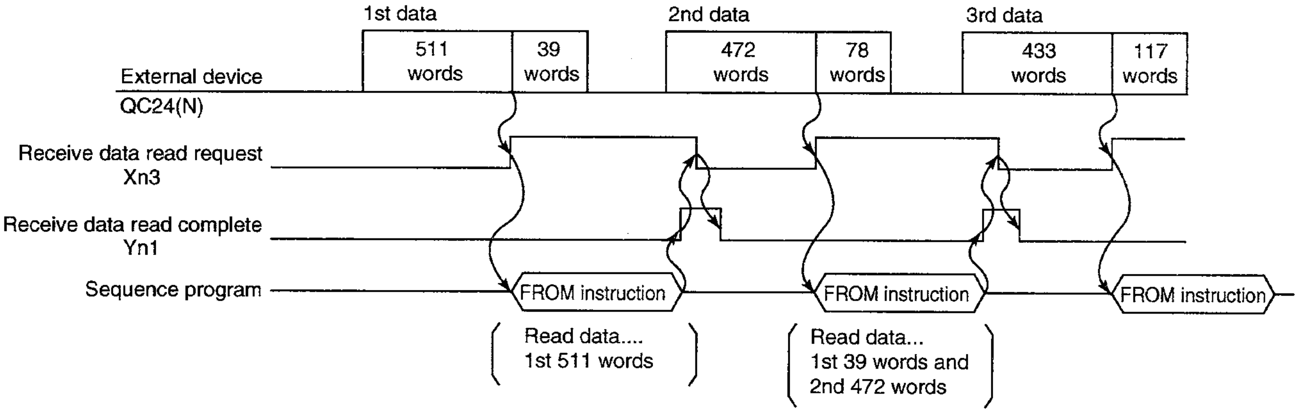


ⓑ Reception by receive end data count

When the receive end data count is larger than the receive data storage area, the receive buffer memory length (default: 512 words) set in buffer memory addresses A7H/147H - 1 is processed as the receive end data count.

(Receive data storage area) > (Data length received from external device)

[Example] When 550 words of data is received through the CH1 interface in three parts when the CH1 interface receive area consists of addresses 600H to 7FFH (default value)



② Receive data when CD signal turned OFF and mode switched

If the following operations are performed while the QC24(N) is receiving data from an external device, the receive data will be cleared.

ⓐ When CD signal turned OFF

- When CD terminal check enable is set, and the QC24(N) CD signal is turned OFF (20 ms or longer) by an external device when there is no read request to the PLC CPU during data communications with an external device over the RS-232C circuit, the receive data is cleared. (Receive area is not initialized.)
- When the CD signal is turned OFF when there is a read request to the PLC CPU, the QC24(N) continues to process the read request to the PLC CPU.
  The requested receive data is not cleared.
- To resume data transmission from the external device, turn on the CD signal.

ⓑ When mode switched

- When the QC24(N) mode is forcefully switched as described in Chapter 18, the QC24(N) enters the same state as when it is started by turning on the power and the receive data is cleared. (The receive area is not initialized.)
- To receive data again, setting to the buffer memory special applications area is necessary.
- To resume data transmission from the external device, turn on the QC24(N) Ready signal (X (n+1) E) and transmit after setting to the buffer memory special applications area is completed.
  (Depending on the data communications system, it may be necessary to resume data transmission from the external device after informing the external device from the PLC CPU that transmission can be resumed.)

9.3.3 Receive error detection (Checked using module LED and buffer memory)

When the QC24(N) detects an error while receiving data from an external device by non procedure protocol, it carries out the following processing.

① Turns on one of the LED from C/N to SIO, depending on the contents of the detected error.
② Turns on LED CH1 ERR. or CH2 ERR..
③ Stores the error code to the buffer memory data receive result storage area (addresses 258H/268) and turns ON the receive error detection signal (input signal Xn4/XnB), depending on the error contents.
④ Turns on the CH□ ERR. LED ON signal (input signal XnE/XnF) between the PLC CPU and QC24(N).

When a data receive error occurs, check it by reading the LED on the front of the module or the buffer memory with the sequence program described in Section 19.1.

POINTS

(1) The data when the receive error occurred is ignored and only the data received normally is sent to the QC24(N). Therefore, data may be missing from the message received when the receive error occurred.
To clear all the current receive data, proceed as described in Section 9.3.4.
(2) At QC24(N) no reception watchdog timer (timer 0) time-up, the receive data is processed as described below.
① When data received without using a user frame
The receive data from the start of reception of the current message to time-up are stored to the receive data storage area or OS area.
② When data received using a user frame
- When the trailer frame is set, the no reception watchdog timer (timer 0) starts after data is received.
When a time-up error is generated, all the arbitrary data area's received data up to that point is sent to the QC24(N) and the receive abnormal end signal is turned ON.

Note

External device status check
Check the status of the external device by connecting the external device Ready signal, etc. as the input signal to the PLC CPU and performing signal ON/OFF interval time-up check, etc.

Also check by data receive interval time-out check.

9.3.4 Receive data clear

When trouble, etc. at the external device generates an error while data is being received from the external device by non procedure protocol, the data received up to that point may be erroneous, or intermediate data may be lost.
All the data received up to that point can be ignored and the buffer memory can be initialized as QC24(N) error recovery processing by designating buffer memory clear.
To clear the receive data, do any of the following.
The QC24(N) ignores the data received up to that point and performs processing with the current receive data count as [0].

1 When using the buffer memory receive data clear request area

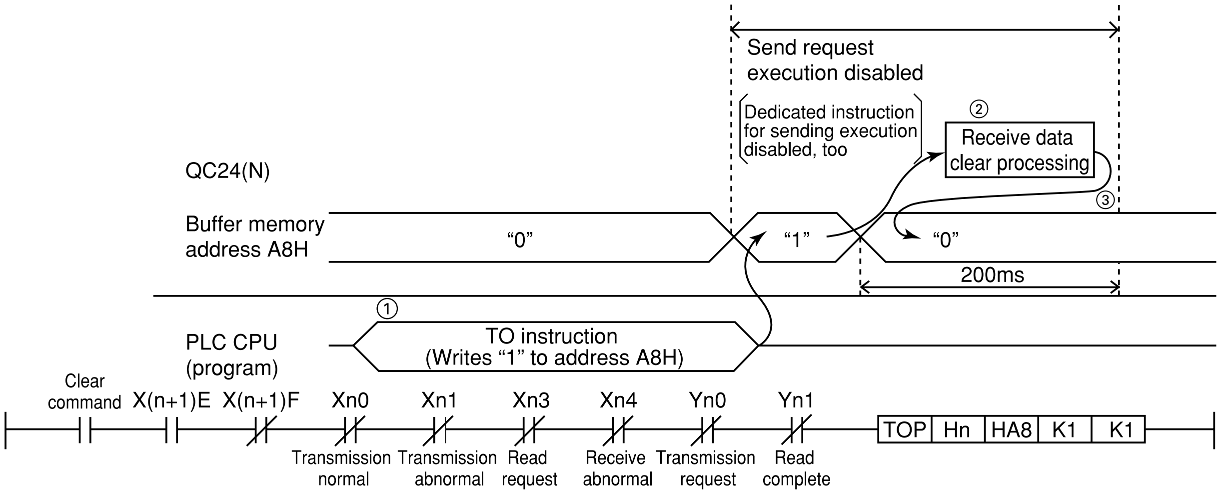
Write and read the buffer memory receive data clear request area (addresses A8H/148H) using the clear procedure described below. (Since the buffer memory receive area is not cleared, the preceding value remains.)
When resuming data communications with the external device, resume data communications 200ms after the value of buffer memory address A8H/148H has changed from [1] to [0].
(Depending on the data communications system, the PLC CPU may have to inform the external device that data communications can be resumed.)

(Clear procedure)....CH1 interface

① Turn off the receive data read request (Xn3), receive data read complete (Yn1), and send request (Yn0) signals by writing [1] to buffer memory address A8H with the sequence program TO instruction.

② The QC24(N) clears receive data in the OS area (see Section 9.3.1*1).

③ When clearing of the receive data is complete, the QC24(N) changes the [1] written to buffer memory address A8H to [0].
Resume data communications 200ms after the value of buffer memory address A8H has changed to [0].



Write a program with Xn0, Xn1, Xn3, Xn4, Yn0, and Yn1 as the interlock at the TO instruction.

Note

When transmitting data from the QC24(N) to an external device while the send request signal is ON, do not issue the receive data clear request described above. (See Appendix 7 for program example.)
If a receive data clear request is issued while data is being transmitted to an external device, the QC24(N) will terminate data transmission. The transmission complete signal is not turned ON either.

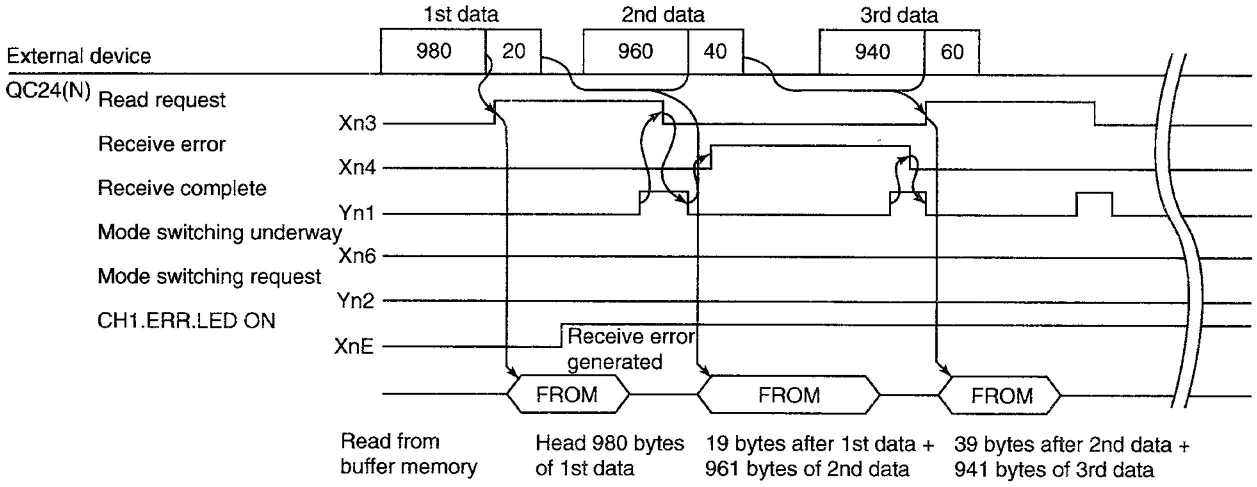
2 When using the mode switching function

When the mode switching function is performed, the QC24(N) terminates the current processing and enters the start state.
Perform the mode switching function as described in Chapter 18.

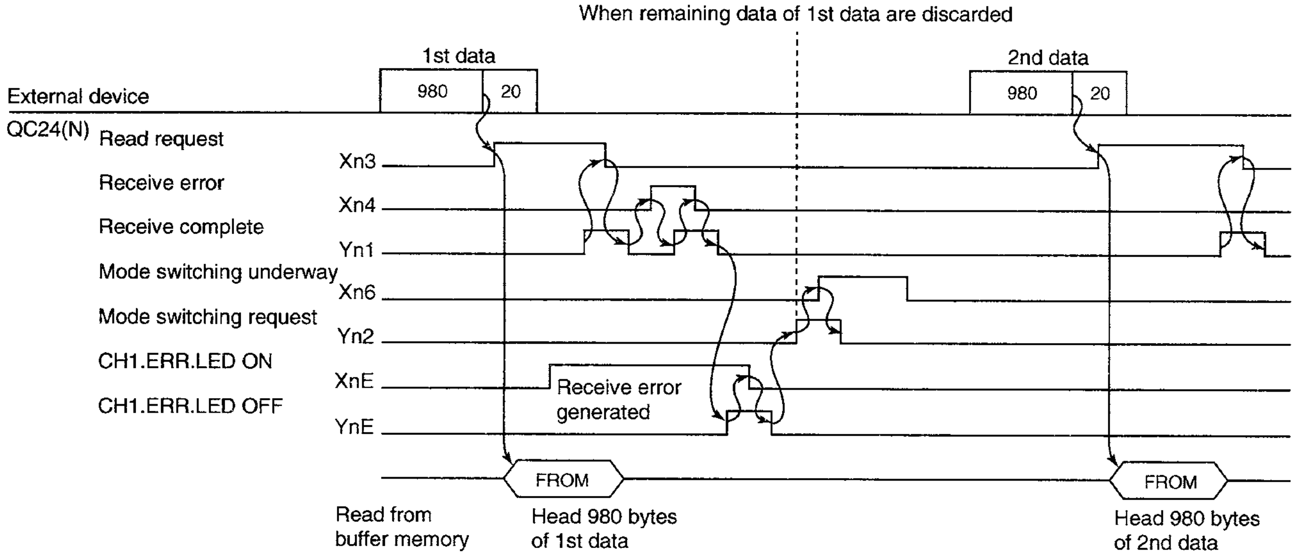
Note

The following is an example of reading the receive data when mode switching is not performed.
In this case, the external device sends 1000 bytes of data through the CH1 interface when 980 bytes is set as the receive end data count.

1 When mode switching not performed after receive error generation



2 When mode switching performed after receive error generation



9.4 Data Transmission to External Device

This section describes the common information you should know to transmit data to an external device.

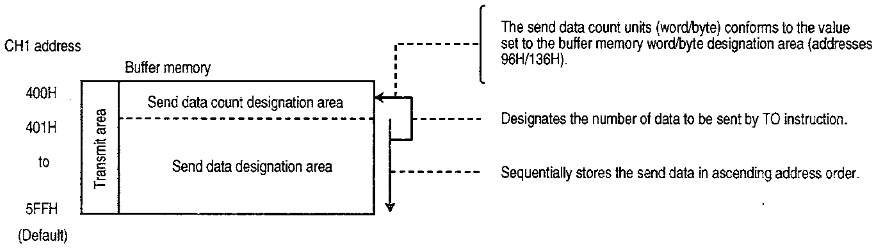
9.4.1 Transmit area and send data designation and write

The following describes the designation method, etc. when writing the data to be transmitted to the external device to the QC24(N) buffer memory (transmit area) that is written by the PLC CPU and transmitting the send data to the external device.

1 **Transmit area**

The "transmit area" is the QC24(N) buffer memory area to which the PLC CPU writes the send data and send data count to transmit data to an external device. The transmit area is allocated buffer memory addresses 400H to 5FFH and 800H to 9FFH as the default value.

The transmit area can be changed to match the purpose of data transmission, specifications of the external device, and the length of the send data. (See Section 14.8.1 for a description of the modification method.)



POINT

Designate so that the data size of the arbitrary data area per transmission from PLC CPU to external device does not exceed the size of the QC24(N) send data designation area.

(Send data designation area) ≥ (data size of arbitrary data area to be transmitted from PLC CPU)

When you must transmit data so large that it cannot all be stored to the transmit data designation area, make the transmit area larger.
The transmit area addresses and size can be changed.

2 Send data designation and write methods

Use any of the following methods to designate the data to be transmitted from the PLC CPU to an external device.

- Transmission in an arbitrary format .... Buffer memory transmit area
- Transmission by user frame .... Buffer memory non procedure protocol transmission user frame designation area and transmit area

The following outlines the send data designation and write methods.

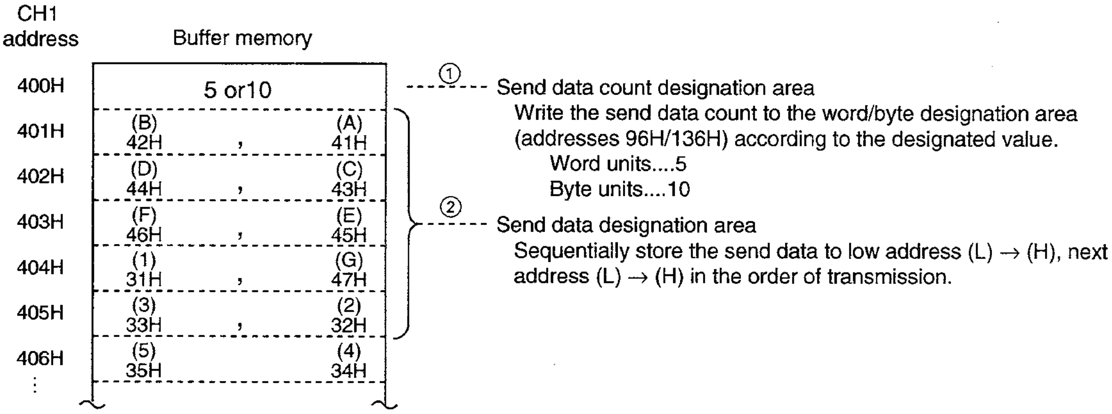
(a) Send data designation and write for transmission in an arbitrary format

The send data count and send data are written to the transmit area as shown below.

① The word count/byte count (conforming to word/byte designation) of the data to be written are written to the send data count designation area and send data designation area.

② The data to be transmitted (arbitrary data area of transmit message) is written to the send data designation area.

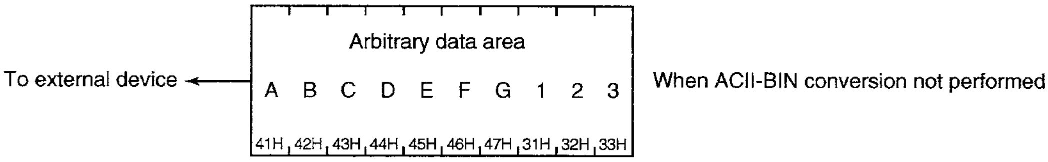
(Example) When transmitting "ABCDEFG123" (The transmit area is the default value.)



Send data count designation area
Write the send data count to the word/byte designation area (addresses 96H/136H) according to the designated value.
Word units....5
Byte units....10

Send data designation area
Sequentially store the send data to low address (L) → (H), next address (L) → (H) in the order of transmission.

When the send request signal (Yn0/Yn7) is turned on after ① and ② above are performed, the designated number of the designated data is sequentially sent from the QC24(N), beginning from the low address of the send data designation area.

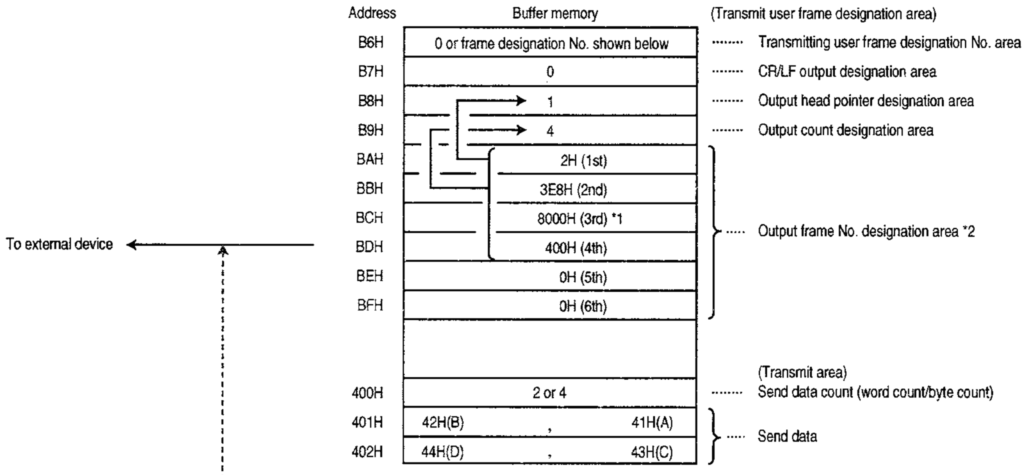


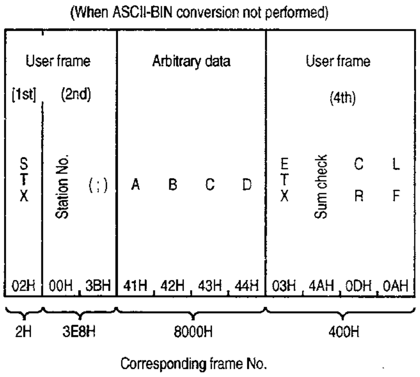
(b) Send data designation and writing during user frame transmission

When transmitting by combining user frames in an arbitrary data area, the arbitrary data area send data count and send data are written to the transmit area, the same as for transmission in an arbitrary format.
For the user frames, the registration No., etc. of the user frame to be transmitted are written to the transmit user frame designation area as shown below.
When the send request signal (Yn0/Yn7) is turned ON after writing to the transmit area and transmit user frame designation area, the QC24(N) sends the designated data in the designated order.
(See Chapter 11 for more information.)

(Example) When data is transmitted in the following order

Transmission order	Kind of send data	User frame No.	Contents of send/registration data
1	User frame	2H (2)	02H (STX)
2	User frame	3E8H (1000)	00H, 3BH (station No., ";")
3	Arbitrary data	8000H (-32768)	41H, 42H, 43H, 44H ("ABCD")
4	User frame	400H (1024)	03H, FFH, F6H, 0DH, 0AH (ETX, sum check, CR, LF)





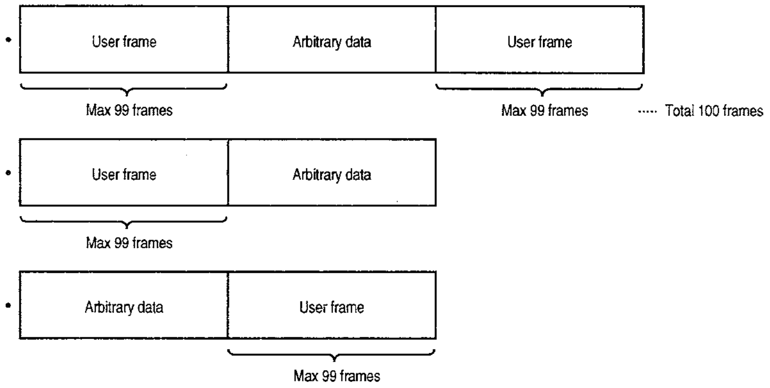
*1 When the data written to the transmit area is transmitted also, 8000H is used as the temporary user frame No.
When user frame No. 8000H is designated, the QC24(N) transmits the designated number of send data designation area data to the send data count designation area.

*2 When ASCII-BIN conversion is performed, data can be transmitted without converting the arbitrary frame area and transmit area data (arbitrary data area of transmit message).
For the part that is transmitted without performing ASCII-BIN conversion, designate the binary data when the user frame No. designated by output frame No. designation area is expressed with 16-bit binary data and designate the user No. by binary data when bit 14 was set to ON (1).
When data of the part designated by 4001H to C01FH is transmitted, addition of the additional code by transparent code designation is also performed.

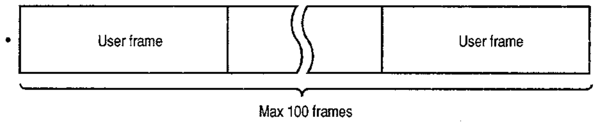
No. of user frame to be transmitted	Designation No. when transmitted without performing ASCII-BIN conversion
1H to 3E7H (1 to 999)	4001H to 43E7H (16385 to 17383)
3E8H to 4AFH (1000 to 1199)	43E8H to 44AFH (17384 to 17583)
8000H to 801FH (-32768 to -32737)	C000H to C01FH (-16384 to -16353)

During data transmission by user frame, messages of the data list shown below can be transmitted.

① When transmitting a message with arbitrary data



② When transmitting a message without arbitrary data



POINTS

(1) Up to 231 user frames can be registered to the QC24(N).

(2) The user frame transmission function can be used for fixed message transmission.

9.4.2 Transmission error detection

When the QC24(N) detects an error during data transmission to an external device using the non procedure protocol, it terminates transmission processing and performs the processing described below.

① Lights one of the LED between C/N and SIO, depending on the contents of the detected error.
② Lights LED CH1 ERR. or CH2 ERR..
③ Stores the error code to the buffer memory data transmission result storage area (addresses 257H/267H) according to the contents of the detected error and turns ON the transmission abnormal end signal (input signal Xn1/Xn8).
④ Turns ON the CH□ ERR. LED on signal (input signal XnE/XnF) between the PLC CPU and QC24(N).

Check generation of a data transmission error by reading the LEDs on the front of the module, or by reading the buffer memory with the sequence program described in Section 19.1.

POINT

When a transmission error occurs, the PLC CPU may not transmit all the designated data.
It is recommended that data communications be performed by establishing a user arbitrary communication procedure that can check normal transmission by reception of a response to data transmission.

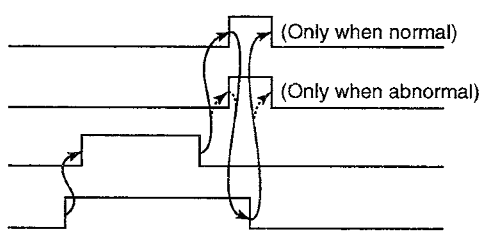
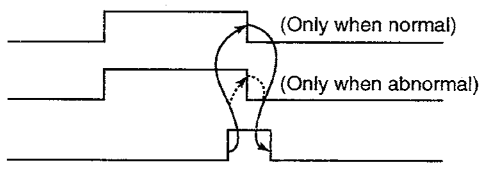
Note

External device status check

Check the status of the external device by connecting the external device Ready signal, etc. as the input signal to the PLC CPU and performing signal ON/OFF interval time-out check, etc.

9.5 I/O Signals for Handshake with PLC CPU

When data is sent and received using the non procedure protocol, the signal that sends the data output from the sequence program to the external device and the signal that detects that data has arrived from the external device and can be read by the sequence program are called handshake input/output signals. These signals are necessary with the non procedure protocol.
The input/output signals for handshake are shown below.

	I/O signal		Signal name	Device turned ON/OFF		Timing
	CH1	CH2		CPU	QC24(N)	
Trans-mission	Xn0	Xn7	Transmission normal end		○	
	Xn1	Xn8	Transmission abnormal end		○	
	Xn2	Xn9	Transmitting		○	
	Yn0	Yn7	Send request	○		
Recep-tion	Xn3	XnA	Receive data read request		○	
	Xn4	XnB	Receive error detected		○	
	Yn1	Yn8	Receive data read complete	○		

POINT

When the transmission abnormal end signal (Xn1/Xn8), or receive abnormal end signal (Xn4/Xn8), was turned ON, read the error code from the buffer memory shown below and check the error contents and take appropriate action according to Section 22.1.

- When transmission abnormal end signal (Xn1/Xn8) turned ON.
  Read the data transmission result storage area (addresses 257H/267H).
- When receive abnormal end signal (Xn4/XnB) was turned ON.
  Read the data receive result storage area (addresses 258H/268H).

Note

The I/O signals that can be used with the non procedure protocol, in addition to the signals mentioned above, are shown below.
See Sections 3.4 and 19.1.3 for a description of the PLC CPU input/output signals.

- CH1 ERR. LED ON signal (XnE) .... Turned ON when an error is generated at the CH1 interface
- CH2 ERR. LED ON signal (XnF) .... Turned ON when an error is generated at the CH2 interface
- QC24(N) Ready signal (X (n+1) E) .... Turned ON when the PLC CPU can access the QC24(N)
- Watchdog timer error signal (X (n+1) F) ...... Turned ON when the QC24(N) cannot operate normally
- CH1 ERR. LED OFF request signal (YnE) ... Turned ON when a request to turn off the CH1 ERR. LED is issued
- CH2 ERR. LED OFF request signal (YnF) ... Turned ON when a request to turn off the CH2 ERR. LED is issued

9.6 Buffer Memory Read/Write

This section describes reading and writing of the QC24(N) buffer memory when the non procedure protocol is used to perform data communications.
Assemble a sequence program for the necessary part.

9.6.1 Initialization to buffer memory special applications area

When the QC24(N) starts, it writes its own default values, or the default values registered to the EEPROM by the user, to the buffer memory special applications area.
The QC24(N) default values enable data communications with external devices. However, it may also be necessary to change the default values, depending on the specifications of the external device.
The setting items, reference section, and examples of initialization when the default values in the QC24(N) buffer memory special applications area must be changed (initialized) to carry out data communications using the non procedure protocol are shown below.

	Read/write contents that must be programmed	**QC24(N) default value**	**Reference Section**
①	To perform QC24(N) CD terminal check during data communications through the RS-232C interface	Not checked	4.7.2 3
②	To use DC codes to control transmission with external devices	DTR/DSR control	14.3
③	To change the units of the data length to be transmitted and received to byte units	Word units	14.4
④	To use half-duplex communications to exchange data through the RS-232C interface	Full-duplex communications	14.5
⑤	To monitor the receive interval (timer 0) with the QC24(N) while data is being received from an external device.	0 (Unlimited wait)	14.7
⑥	To change the transmit area that stores the data to be transmitted to the external device	400H to 5FFH 800H to 9FFH	14.8
⑦	To change the receive complete data	1FFH (511 words)	
⑧	To change the receive end data count	CR+LF	
⑨	To change the receive area that stores the data received from the external device	600H to 7FFH A00H to BFFH	
⑩	To set the receive user frames	None	14.9
⑪	To handle the 1 byte of external device transmission control data as user data (transmit transparent code designation, receive transparent code designation)	None	14.10
⑫	To transmit/receive data by ASCII-BIN conversion	Not converted	14.11

POINTS

(1) When changing a default value, write the new value to the buffer memory special applications area when starting the QC24(N) (when QC24(N) ready signal X (n+1) E is ON).

(2) It is recommended that when a value set in the buffer memory special applications area was changed, you check if subsequent data is transmitted and received normally before you register the special applications area set value to the QC24(N) EEPROM and use it as the default value during QC24(N) starting.

* Using the values registered to the EEPROM are used as the default values eliminates the need for a sequence program of the part whose set value was changed.

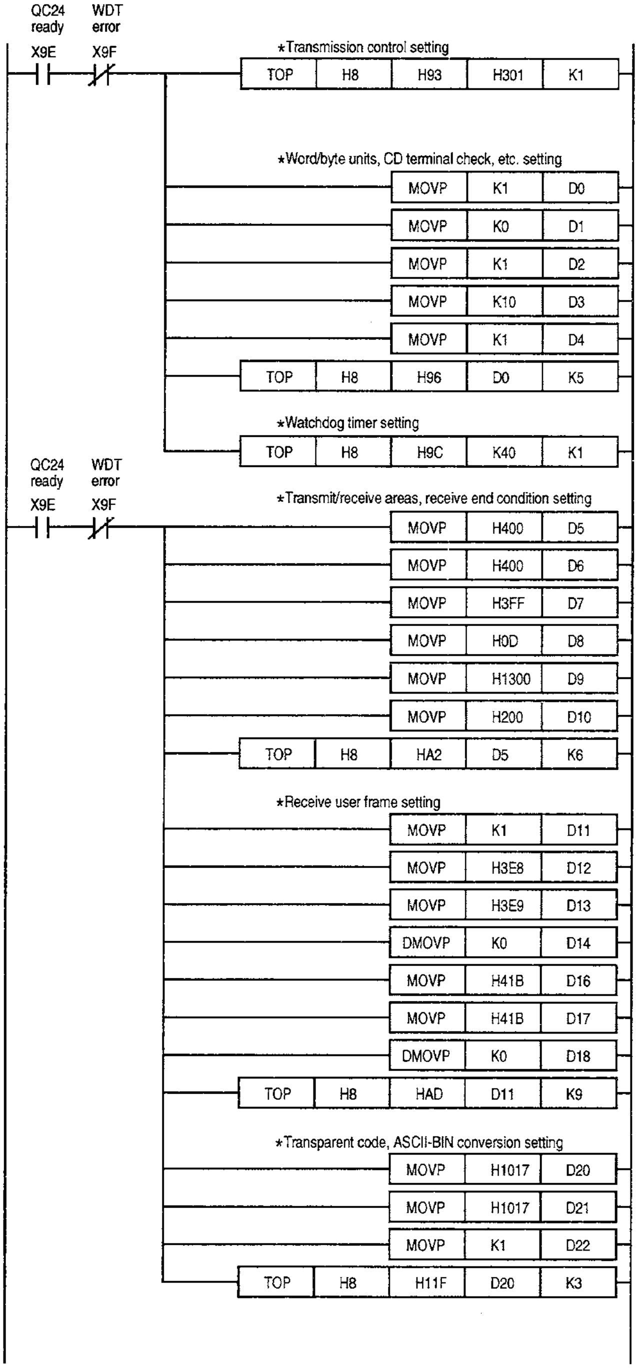
(3) See Section 14.1 and Chapter 15 for a description of the following:
- Areas that can be registered to EEPROM
- Registration to EEPROM
- Initialization of buffer memory set values (return to QC24(N) default values)

(Example of initialization to buffer memory special applications area)

A sample program that changes the default values of the QC24(N) buffer memory special applications area is shown below.
Program only the necessary parts.
This examples shows the setting for the CH1 interface.

Designation Example

(QC24(N) I/O signals 80H to 9FH)



Controls transmission by DC code and enables all DC control.
The DC code uses the default value.
See Section 14.3.

Handles the data send/receive data in byte units.
Sets CD terminal check.
Sets the RS-232C I/F communications system to half-duplex communications.
Sets nonpriority during simultaneous transmission. (Transmission wait time 1000ms)
Sets retransmission at resumption of transmission.
See Sections 4.7.2 $\boxed{3}$, 14.4, and 14.5.

Sets the no reception watchdog timer (timer 0) to 40 bytes.
See Section 14.7. (The set value is enabled by mode switching.)

Sets the transmit area to addresses 400H to 7FFH.

Sets the receive end data count to 3FFH (1023) words/bytes.
Sets the receive end code to CR (0DH).
Sets the receive area to addresses 1300H to 14FFH.

See Section 14.8.

Enables user frame use.
Sets the header frame. (1st)
(2nd)

Sets the trailer frame. (1st)
(2nd)

See Section 14.9. (Reception is possible after address ADH changes from [1] to [2].)

Sets the transmission transparent code to 17H (ETB) and the additional code to 10H (DLE).
Sets the receive transparent code to 17H (ETB) and the additional code to 10H (DLE).
Enables send/receive data ASCII-BIN conversion.
See Sections 14.10 and 14.11.

9.6.2 Reading/writing of buffer memory during data communications

The contents and reference section when reading/writing the QC24(N) buffer memory after the QC24(N) starts are shown below.

	Read/Write contents that must be programmed	Reference section
①	To perform data communications in an arbitrary format.	Chapter 10
②	To perform data communications using user frames.	Chapter 11
③	To clear all the current data by generation of receive trouble.	Section 9.3.4
④	To register data communications parameters to the QC24(N) EEPROM.	Chapter 15
⑤	To register data communications user frames to the QC24(N) EEPROM, etc.	Chapter 16
⑥	To switch the QC24(N) interface used by the non procedure protocol to another protocol.	Chapter 18
⑦	To read the QC24(N) LED ON status and turn off the LED.	Chapter 19
⑧	To read the QC24(N) module status, signal status, and switch setting status.	
⑨	To check the error contents when the CH1 ERR. LED or CH2 ERR. LED is turned on.	
	To check the data transmission result and receive result.	Chapter 9 Chapter 10

POINT

Of the contents given above, write a sequence program that reads/writes the buffer memory for only the contents performed by the user.

1 Transmit user frame designation area

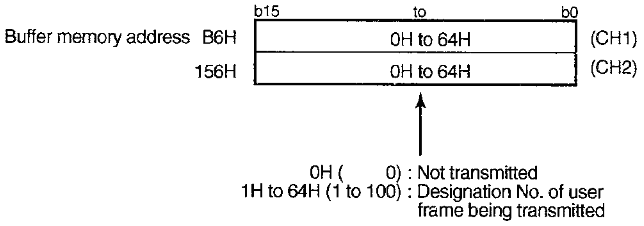
The following describes the applications of the value stored to the buffer memory used during user frame data transmission.

POINT

Section 9.4.1 and Chapter 11 give a general description and details of reading/writing of the transmit user frame designation area.

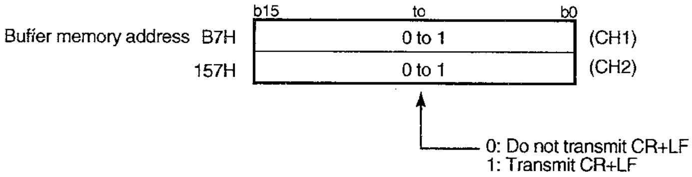
① Transmitting user frame storage area (addresses B6H/156H)

This area stores number of the ⑤ Output frame No. designation area being transmitted during user frame data transmission.



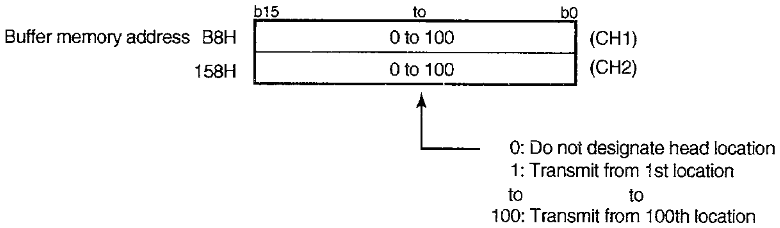
② CR/LF output designation area (address B7H/157H)

Designates whether or not CR+LF is to be transmitted each time a user frame and arbitrary data are transmitted when transmitting a user frame and arbitrary data without CR/LF.



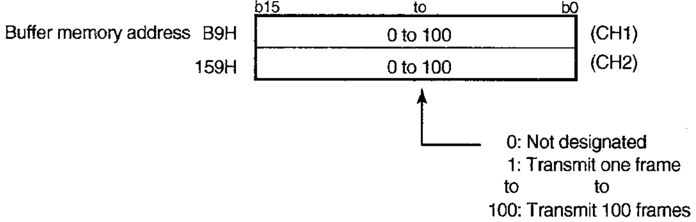
③ Output head pointer designation area (address B8H/158H)

Writes the head location (□th) of the output frame No. designation area that writes the registration number of the user frame to be transmitted.



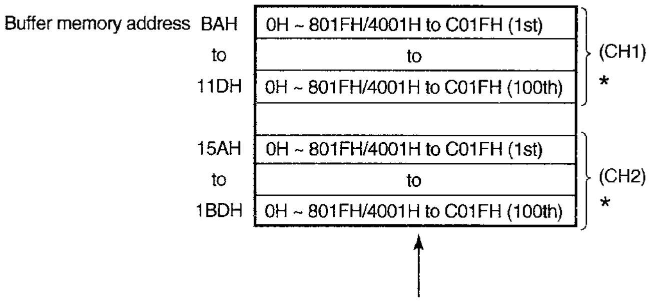
④ Output count designation area (address B9H/159H)

Writes the number of user frames that are to be transmitted to the output head pointer designation area from the designated location.



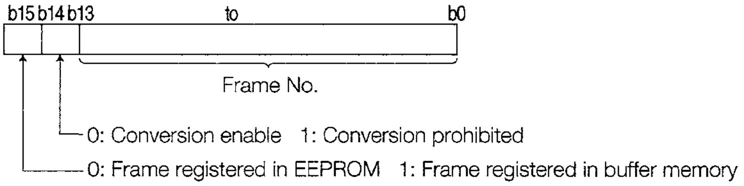
⑤ Output frame No. designation area (addresses BAH to 11DH/15AH to 1BDH)

- Writes the No. of the user frames to be transmitted to the output head pointer area in the output order, beginning from the designated location.
- When the data written in the transmit area is transmitted also, 8000H is used as the temporary user frame No.
- When user frame No. 8000H is designated, the QC24(N) transmits the designated number of send data designation area data to the send data count designation area.



0H (0) : Do not transmit (Other addresses cannot be designated.)
1H to 3E7H (1 to 999) : Transmit default frame of designated No.
3E8H to 4AFH (1000 to 1199) : Transmit user frame of designated No. (Number of frames registered to EEPROM)
8000H (-32768) : Transmit data of buffer memory transmit area.
8000H to 801FH (-32768 to -32737) : Transmit user frame of designated No. (Number of frames registered to buffer memory)

* When [Convert] is set in the buffer memory ASCII-BIN conversion designation area (addresses 121H, 1C1H) and the send data is converted from ASCII data to binary data, the data of an arbitrary frame and the transmit area (arbitrary data area of transmit message) can also be transmitted without conversion.
For example, the transmission area data only can be converted to ASCII-BIN and transmitted without ASCII-BIN converting the control code frame portion.
Designate the part to be transmitted without being converted from ASCII data to binary data by binary data when the No. of the user frame designated by the output frame No. designation and the user frame No. are expressed by 16-bit binary data and bit 14 is turned ON (1).



When the data of the part designated by addresses 4001H to C01FH is transmitted, addition of additional code by transparent code designation in buffer addresses 11FH/1BFH cannot be performed.

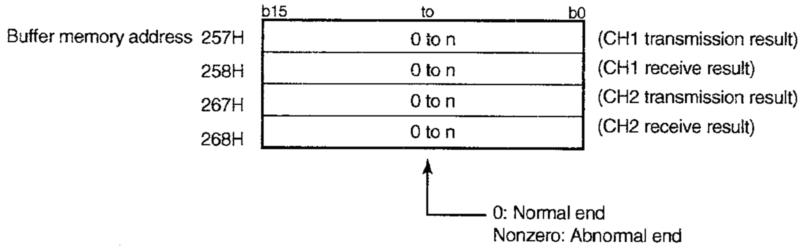
No. of user frame to be transmitted	Designated No. when data transmitted without ASCII-BIN conversion
1H to 3E7H (1 to 999)	4001H to 43E7H (16385 to 17383)
3E8H to 4AFH (1000 to 1199)	43E8H to 44AFH (17384 to 17583)
8000H to 801FH (−32768 to −32737)	C000H to C01FH (−16384 to −16353)

2 Data transmission result storage area (addresses 257H/267H)

Data receive result storage area (addresses 258H/268H)

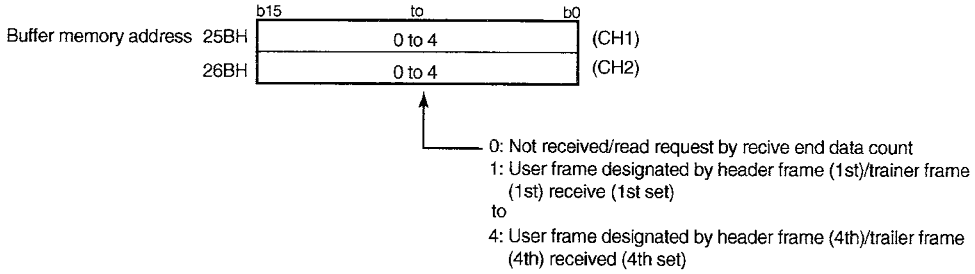
- The data transmission result storage area stores the error code when the QC24(N) detected an error during data transmission.
- The data receive result storage area stores the error contents when the QC24(N) detected an error during data reception.
- When the error code is stored, the input signal to the PLC CPU shown below and the QC24(N) CH□ERR. LED are turned ON.
  When an error is generated, the LED can be turned off and the error code can be cleared as described in Section 19.1.3 3 .

  Data transmission .... Transmission abnormal end signal (Xn1, Xn8)
  Data reception .... Receive abnormal end signal (Xn4, XnB)
- See Section 22.2 for the error code contents and processing.



3 Receive user frame storage area (address 25BH/26BH)

- This area stores which user frame (1 to 4) designated by the receive user frame designation area described in Section 14.9 was received during data reception by user frame.
- The objective of this area is up to 4 sets of user frames, with the nth header frame and nth trailer frame of the receive user frame designation area (addresses AEH to B5H/14EH to 155H) as one set. (n = 1 to 4)
  For instance, when the 2nd header frame and 2nd trailer frame, or the user frame designated at the 2nd trailer frame when all the header frames are not designated, were received, [2] is stored to the receive user frame storage area.



4 Transmit area

The following describes the application of the buffer area used by the PLC CPU to writes the data (arbitrary data area in message) to be sent to the external device.

POINT

Section 9.4.1 and Chapters 10 and 11 give a general description and detailed description of the transmit area storage value and writing.

① Send data count designation area (Default addresses 400H/800H)

- The number of data (number of bytes/number of words) to be transmitted to the external device is written to this area.
- The data count units conforms to the word/byte designation area (addresses 96H/136H) designation.

② Send data designation area (Default addresses 401H to 5FFH/801H to 9FFH)

- The data (arbitrary data area in message) to be transmitted to the external device is written to this area.
- The data size (number of data) to be transmitted is designated by the send data count designation area.

5 Receive area

The following describes the application of the buffer memory used by the PLC CPU to read the data (arbitrary data area in message) received from the external device.

POINT

Section 9.3.2 and Chapters 10 and 11 give a general description and detailed description of the receive area storage value and reading.

① Receive data count storage area (Default addresses 600H/A00H)

- This area stores the number of data (number of bytes/number of words) when the QC24(N) reads the data (arbitrary data area in message) received from the external device to the PLC CPU.
- The data count units are designated by the word/byte designation area (addresses 96H/136H).

② Receive data storage area (Default addresses 601H to 7FFH/A01H to BFFH)

- This area stores the data (arbitrary data area in message) received from the external device.
- The data size (number of data) when the received data is read to the PLC CPU is stored in the receive data count storage area.

9.7 Data Communications Precautions

The following describes the precautions to be taken during non procedure protocol data communications.

1 QC24(N) transmission sequence initialization conditions

The conditions that initialize the QC24(N) transmission sequence are shown below.

- When the power is turned on, the Reset switch on the CPU panel is operated, or the QC24(N) mode is switched
- When the receive data was cleared. (See Section 9.3.4.)
- When the CD signal was turned off when data communications were performed by setting CD terminal check enable (see Section 4.7.2) during full-duplex communications through the RS-232C interface.

2 Generation of framing error in external device

When nothing is transmitted from the QC24(N) to the external device through the RS-422 or RS-422/485 interface, a framing error may be generated in the external device. (See Section 3.3.3.)
First send an arbitrary code to identify the head of the send data from the QC24(N) to the external device.
Before communiction data through the RS-422 or RS-422/485 interface, check the QC24(N) interface specifications given in Section 3.3.3.

3 Data communications with external device (computer, etc.) over a multidrop link

When the external device and PLC CPU are connected by a 1: n multidrop link, each QC24(N) receives the data transmitted by the external device.
With a multidrop link, receive data by user frame.
If data is not received by user frame, a sequence program that ignores the receive data other than the receive data addressed to the local station by sequence program, including the data indicating the objective PLC CPU in the message, must be written.

(Sample message)

STX	Space	Station No.		Data length (BIN data)	Data	CR	LF
		0	2				
(02H)	(20H)	(32H)	(32H)			(0DH)	(0AH)

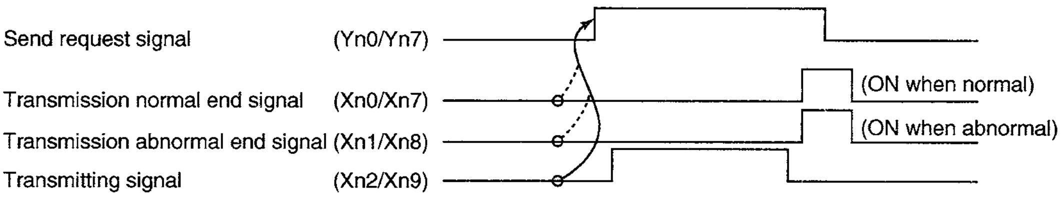
4 Retry processing for data reception errors.

The data when the reception error occurred is discarded and only the data for the normal reception is taken into the QC24(N). For this reason, the reception message may be missing data when an error occurs. To assure the correct transmission and reception of data it is recommended that a normal/error response message is received and a response message reception timeout check is conducted for data transmitted between the PLC CPU and the external equipment and that measures be taken when an error message is received or when an error timeout occurs, such as retransmitting the data (transmission retry).

To clear all of the current reception data on the PLC CPU side, follow the instructions in Section 9.3.4.

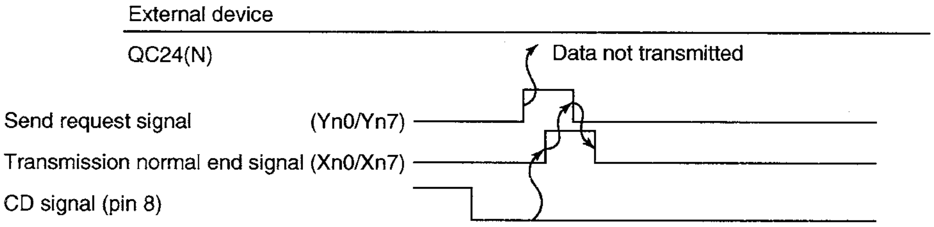
5 Prohibitions when transmitting data from PLC CPU to external device

(a) Issue a send request (Yn0/Yn7) from the PLC CPU to the external device when the input signals shown below are OFF.

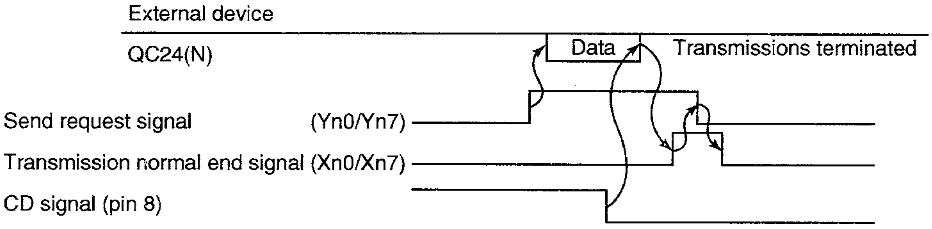


* The QC24(N) accepts a send request from the PLC CPU when the send request signal (Yn0/Yn7) is turned on while the input signals shown above are OFF.

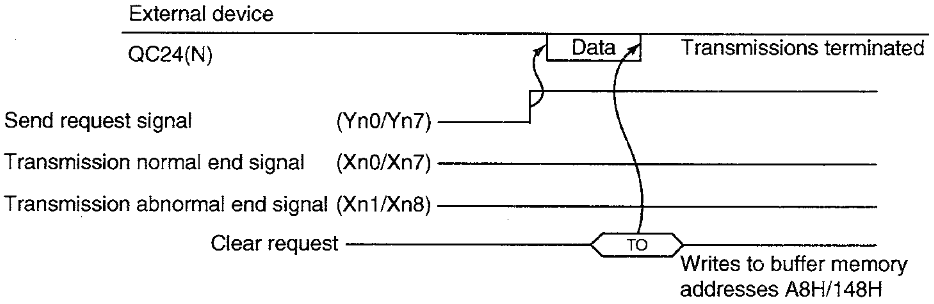
(b) When setting [Check CD Terminal] at the QC24(N) when using the QC24(N) RS-232C interface, do not turn OFF the QC24(N) CD signal when the external device can receive data.
([Check CD Terminal] is set to buffer memory addresses 97H/137H.)
If the CD signal is turned OFF at the beginning of data transmission begins, the QC24(N) will not transmit the data, but will turn ON the transmission normal end signal (Yn0/Yn7).



If the CD signal is turned OFF during data transmission, the QC24(N) will terminate data transmission and turn ON the transmission normal end signal (Yn0/Yn7).



(c) Do not clear the receive data during data transmission. (See Section 9.3.4.)
If the receive data is cleared while data is being transmitted to the external device, the QC24(N) will terminate data transmission.
The transmission normal end signal (Xn0/Xn7) and transmission abnormal end signal (Xn1/Xn8) are not turned ON.



10. DATA COMMUNICATIONS USING AN ARBITRARY FORMAT

This section describes the data transmit/receive method and procedure when the external device and PLC CPU use the non procedure protocol to exchange data in an arbitrary format.

This section describes data communications with the external device using an arbitrary in the following cases:

① QC24(N) I/O signals
When QC24(N) installed at QnACPU input/output signals addresses 80H to 9FH.

② QC24(N) interface used in data communications with external device
QC24(N) CH1 RS-232C interface.

③ Initialization contents of CH1 buffer memory special applications area for data communications using an arbitrary format
The QC24(N) default values used by the areas shown below depend on the contents of the description.
(Change when the QC24(N) starts (when QC24(N) Ready signal X (n+1) E is ON))
Areas other than those shown below do not use the QC24(N) default values.

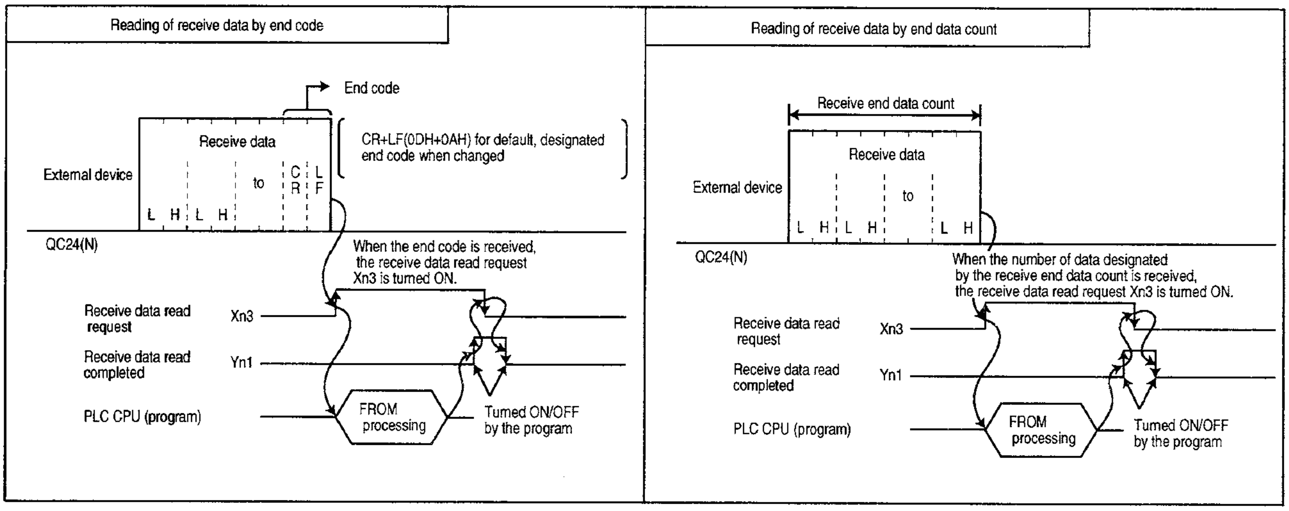
Address	Name	Initialization contents	Reference section
96H	Word/byte designation area	Word units	Section 14.4
A4H	Receive end data count designation	1FFH (511 words)	Section 14.8
11FH	Transmission transparent code designation	None	Section 14.10
120H	Receive transparent code designation	None	
121H	ASCII-BIN conversion designation	Conversion disabled	Section 14.11

10.1 Receive (External Device→QC24(N))

"Receive" is storage of the data received from the external device to the buffer memory receive area by the QC24(N) system and reading of the data by sequence program by FROM instruction.

10.1.1 Receive procedure

The following describes the receive procedure when non procedure protocol receive data is read to the PLC CPU.



POINTS

(1) When data communications are performed using an arbitrary format, data can be received by the following methods.
- Reception by receive end code .... See Section 9.3.1 $\boxed{1}$ (a).
- Reception by receive end data count .... See Section 9.3.1 $\boxed{1}$ (b).

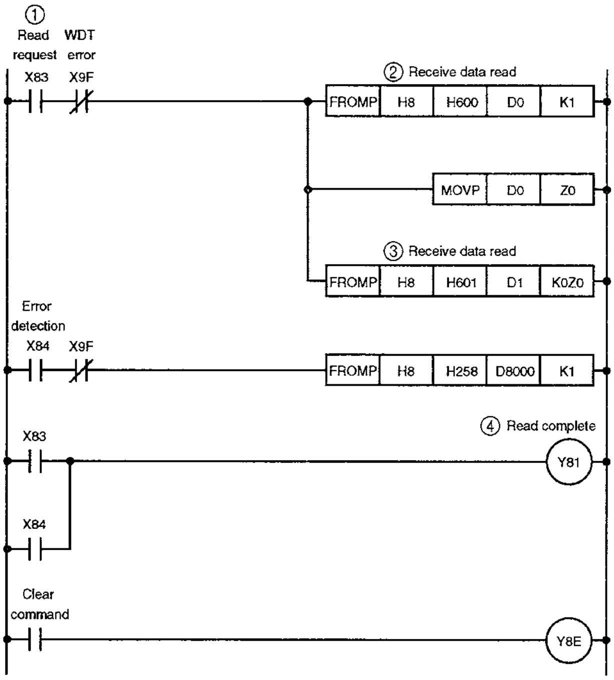
(2) When initialization to the buffer memory special applications area sets receive end code and receive end data count, both methods are valid.
In this case, if receive end code data is received before the number of data designated by receive end data count, the QC24(N) will output (Xn3 ON) a receive data read request signal to the PLC CPU.

10.1.2 Receive program

Sample sequence programs that read the receive data stored in the QC24(N) buffer area to the PLC CPU are shown below.
The receive data is read from the buffer memory receive area (default value: addresses 600H to 7FFH).

1 Sample sequence program when application instructions used (FROM, FROMP. DFRO, DFROP instructions)

See the programming manual (common instructions) for more information.



Reads the receive data count.

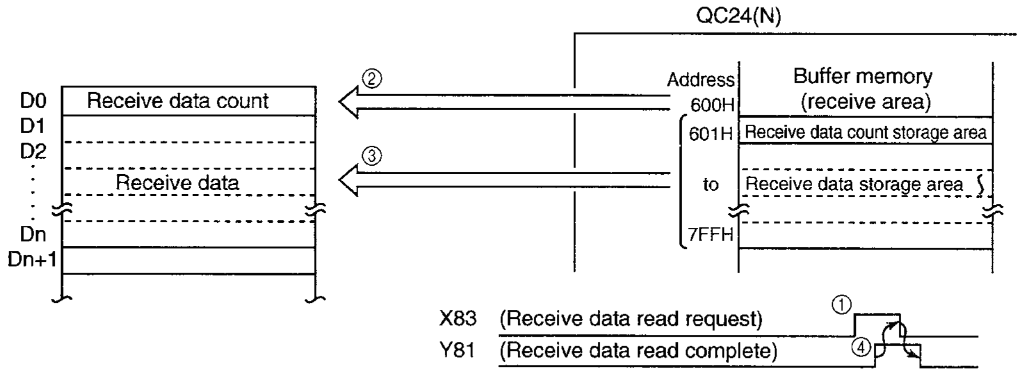
Stores the read data count to the index register (Z0).
(The illustration at the left is for word units.)

Reads the number of receive data corresponding to the receive data count.

Reads the receive error code.
Check the error contents and take appropriate action according to the error code stored in address D8000 and the description in Section 22.1.

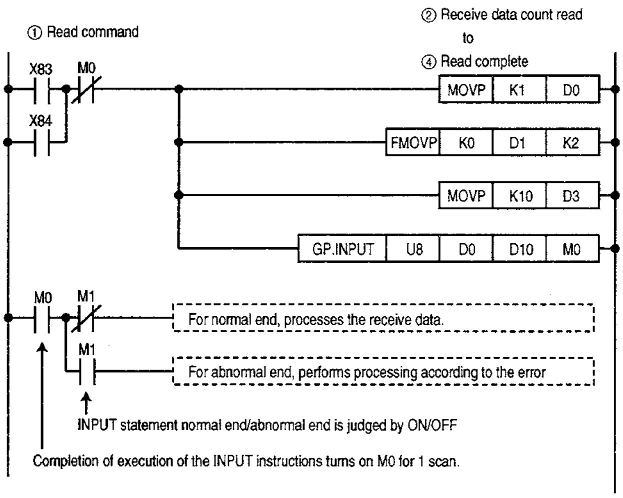
Turns ON the read complete signal (Y81).

Turns off the LED and clears the error code.
* See Section 19.1.3 for a description of error code read and clear and turning off of the LED.



2 Sample sequence program when dedicated instruction used (INPUT instruction)

See the programming manual (special function module) for more information.



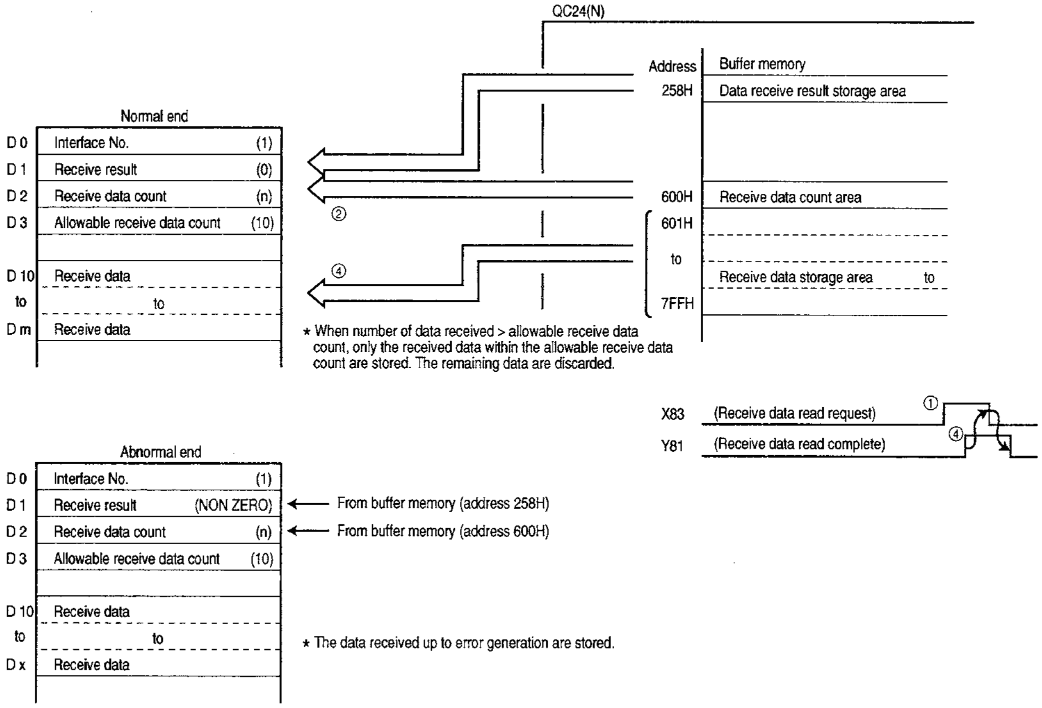
Designates the No. (CH□) of the interface that is to read the receive data.

Clears the receive result and receive data count storage device to zero.

Designates the allowable receive data count.

For normal end, reads the receive data within the allowable receive data count (designated by the user) from the buffer memory receive data storage area.

After execution of the INPUT instruction is completed, turns ON the user designated read complete signal (M0) for one scan. The PLC CPU turns the receive data read and read complete signals ON and OFF.



* When number of data received > allowable receive data count, only the received data within the allowable receive data count are stored. The remaining data are discarded.

* The data received up to error generation are stored.

POINTS

(1) When the QC24(N) dedicated instruction is used, model name registration during I/O allocation of the parameters that are written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and module name (AJ71QC24) at the slot in which the QC24(N) is installed are set.)

(2) The status of communications by dedicated instruction can be read with the SPBUSY instruction.

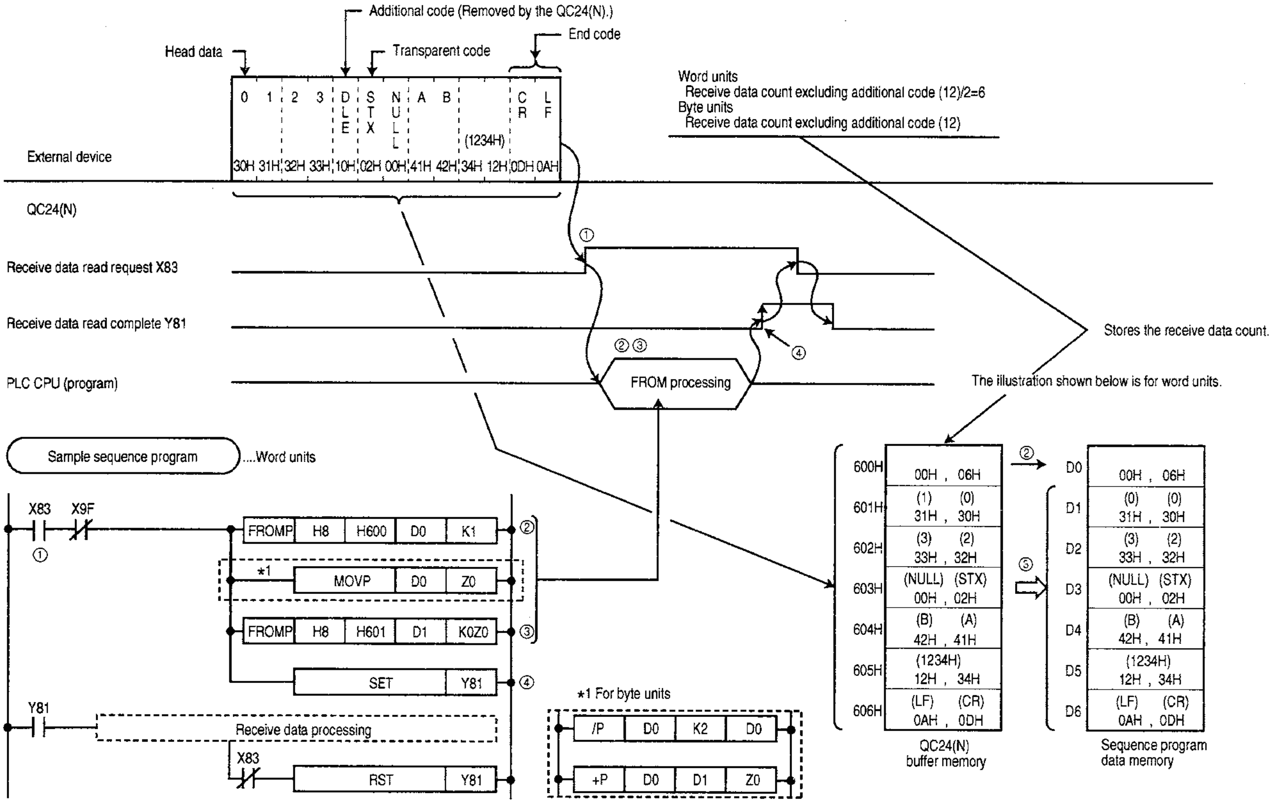
(3) See the programming manual (special function module) for a detailed description of (1) and (2) above.

3 Application examples

The following uses descriptive messages to describe application examples when application instructions are used to store the receive data to the data registers.
Except for the sequence program, the result of storage of the receive data is the same as when the dedicated instruction is used.

(a) Reception by end code

① When receive transparent code designated and ASCII-BIN conversion disable are set
Additional code: 10H (DLE), transparent code: 02H (STX), end code: 0D0AH (CR+LF)



POINTS

(1) The codes when receive transparent code designated and ASCII-BIN conversion disabled are set, the data codes that can be received, and codes when the receive data are stored to the buffer memory receive area are shown below.

		Code that can be received	Code stored to receive area
Receive transparent code designation part	Additional code	01H to FFH	(Removed)
	Transparent code	00H to FFH	00H to FFH
Arbitrary data area (including end code)		00H to FFH	00H to FFH

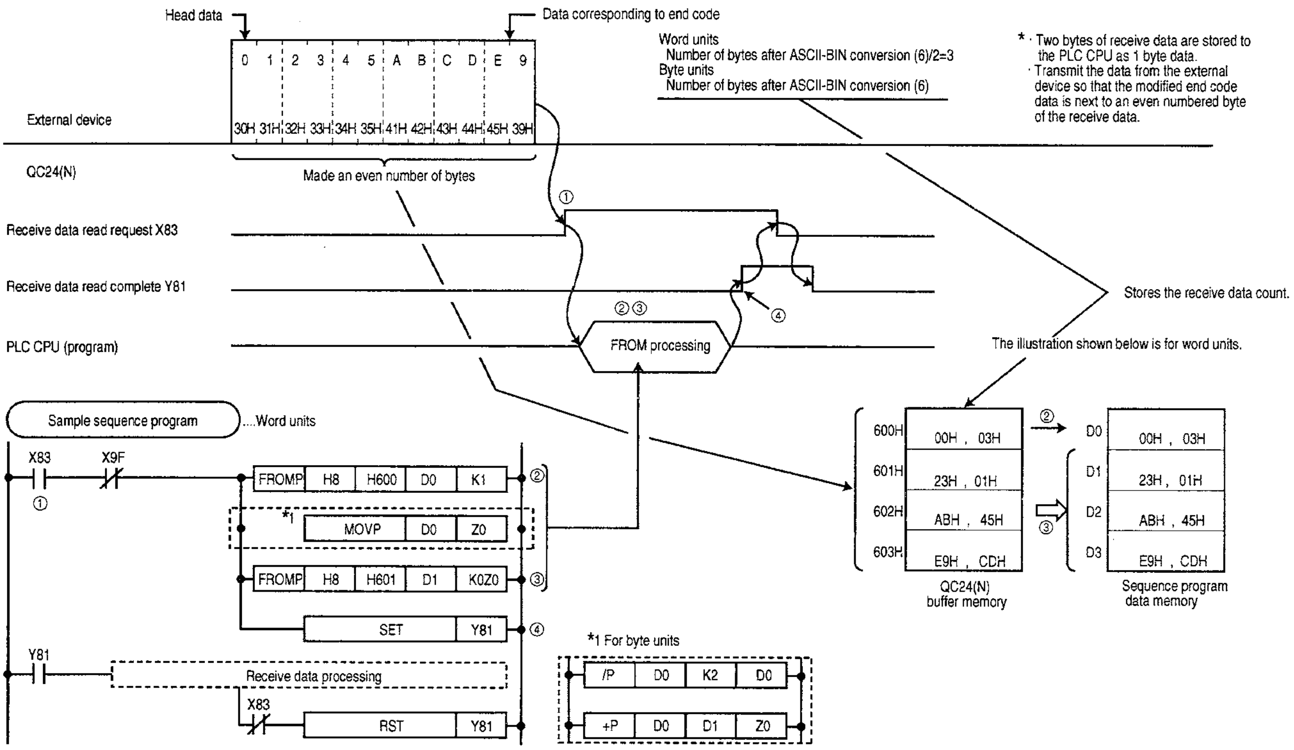
(2) When there is an end code (default value: LF at an odd numbered byte) at an odd numbered byte when the receive data is stored to the receive area, the receive data count shown below is stored to the receive data count storage area.

- Word units
  Receive data count = Number of bytes stored to receive area ÷ 2....Fractions are truncated
- Byte units
  Receive data count = Number of bytes stored to receive area

00H is stored in the higher byte of the last data storage location of the receive area.

(a) Reception by end code

② When receive transparent code not designated and ASCII-BIN conversion enable are set
End code: 9H...(Code after ASCII-BIN conversion)



POINTS

(1) The codes when receive transparent code not designated and ASCII-BIN conversion enable are set, the data codes that can be received, and codes of the receive data stored to the buffer memory receive area are shown below.

	Code that can be received	Code stored to receive area
Arbitrary data area (including end code)	30H to 39H, 41H to 46H	0H to 9H, AH to FH

* If data other than 30H to 39H and 41H to 46H are received as the data code of the arbitrary data area, QC24(N) ASCII-BIN conversion processing will generate an error.

(2) For ASCII-BIN conversion, make the end code the code after conversion.

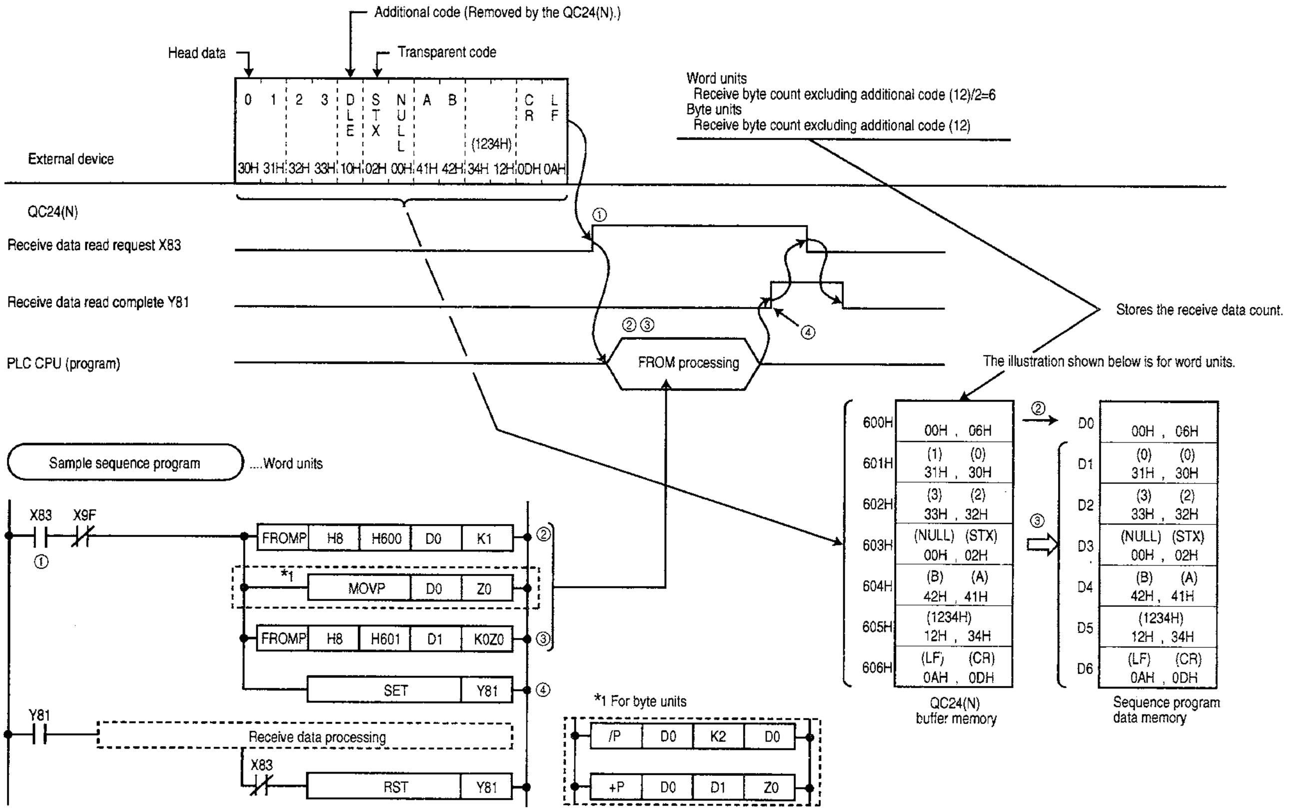
(3) When there is an end code at an odd numbered byte when the receive data is stored to the receive area, the receive data count shown below is stored to the receive data count storage area.

- Word units
  Receive data count = Number of bytes stored to receive area ÷ 2....Fractions are truncated
- Byte units
  Receive area count = Number of bytes stored to receive area

00H is stored in the higher byte of the last data storage location of the receive area.

(b) Reception by end data count

① When receive transparent code designated and ASCII-BIN conversion disabled are set
Additional code: 10H (DLE), transparent code: 02H (STX), end data count: 6 words/12 bytes



POINTS

(1) The codes when receive transparent code designated and ASCII-BIN conversion disabled are set, the data codes that can be received, and the codes of the receive data stored to the buffer memory receive area are shown below.

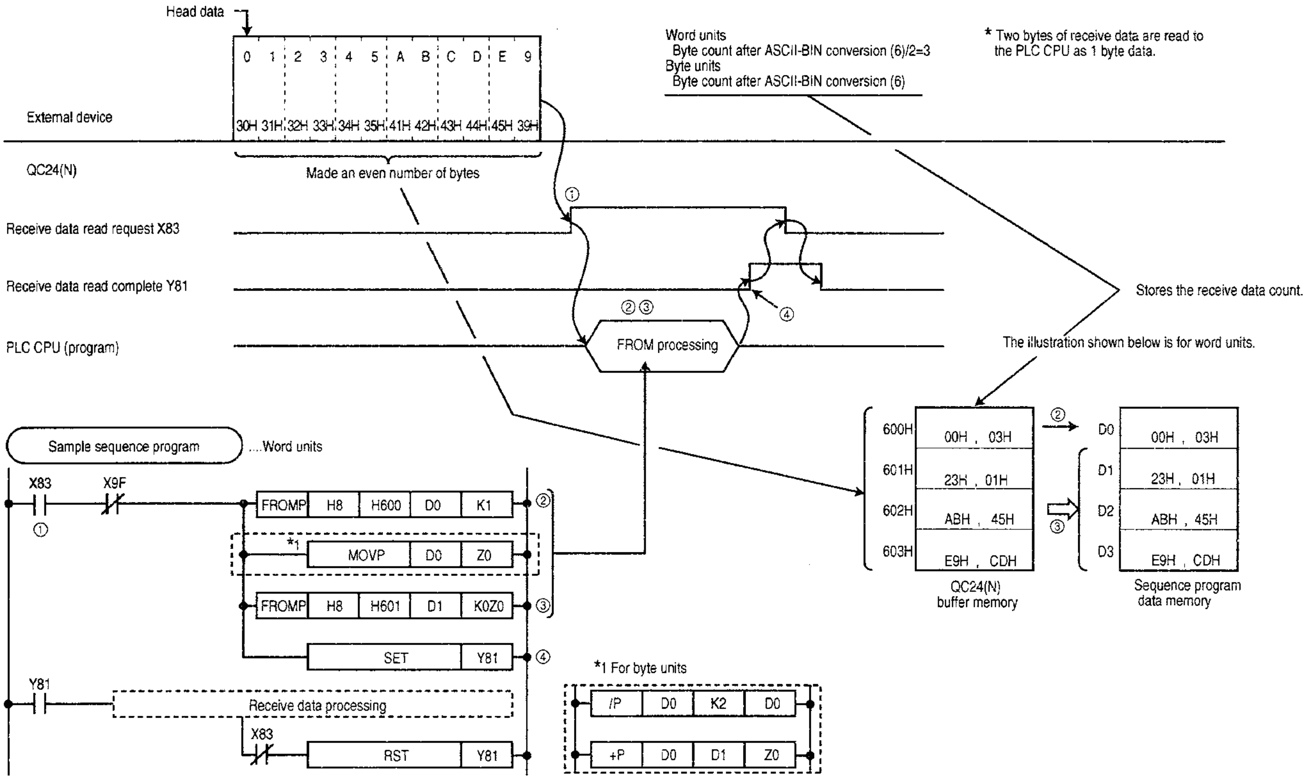
		Code that can be received	Code stored to receive area
Receive transparent code designation part	Additional code	01H to FFH	(Deleted)
	Transparent code	00H to FFH	00H to FFH
Arbitrary data area		00H to FFH	00H to FFH

(2) When receiving data in byte units, the receive data count must be corrected to word count (receive data count ÷ 2) because the FROM instruction is a word units instruction.
For example, when the receive count is 10 bytes and 9 bytes, it is corrected to 5 words.
9 ÷ 2 = 4.5.....Fractions are truncated

(3) When data is received in byte units and by end data count, and the receive data count is an odd number of bytes, 00H is stored in the higher byte of the last data storage location of the receive data storage area.

(b) Reception by end data count

② When receive transparent code not designated and ASCII-BIN conversion enable are set
End data count: 3 words/6 bytes...(Data count after ASCII-BIN conversion)



POINTS

(1) The codes when receive transparent code not designated and ASCII-BIN conversion enable are set, the data codes that can be received, and the codes of the receive data stored to the buffer memory receive area are shown below.

	Code that can be received	Code stored to receive area
Arbitrary data area	30H to 39H, 41H to 46H	0H to 9H, AH to FH

* If data other than 30H to 39H and 41H to 46H are received as the data code of the arbitrary data area, QC24(N) ASCII-BIN conversion processing will generate an error.

(2) When receiving in byte units, the receive data count must be corrected to word count (receive data count ÷ 2) and read because the FROM instruction is a word units instruction.
For example, when the receive data count is 10 bytes and 9 bytes, it is corrected to 5 words.
9 ÷ 2 = 4.5.....Fractions are truncated

(3) When the receive data count is an odd number of bytes during communication in byte units and by end data count, 00H is stored to the higher byte of the last data storage location of the receive data storage area.

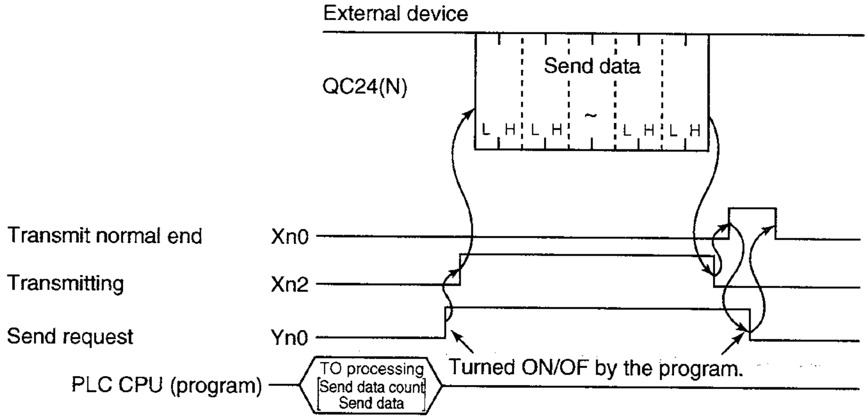
10.2 Transmission (QC24(N) → External Device)

"Transmission" is the transmission of the data written to the transmit area of the buffer memory from the sequence program by TO instruction to the external device by the QC24(N) by PLC CPU send request.

10.2.1 Transmission procedure

The following describes the procedure that transmits the data written in the transmit area to the external device.

Procedure



POINTS

(1) When a transmit data count error or a data transmission error is generated, the QC24 stores the error code to the data transmission result storage area (address: 257H) and turns ON the transmission abnormal end signal (Xn1).

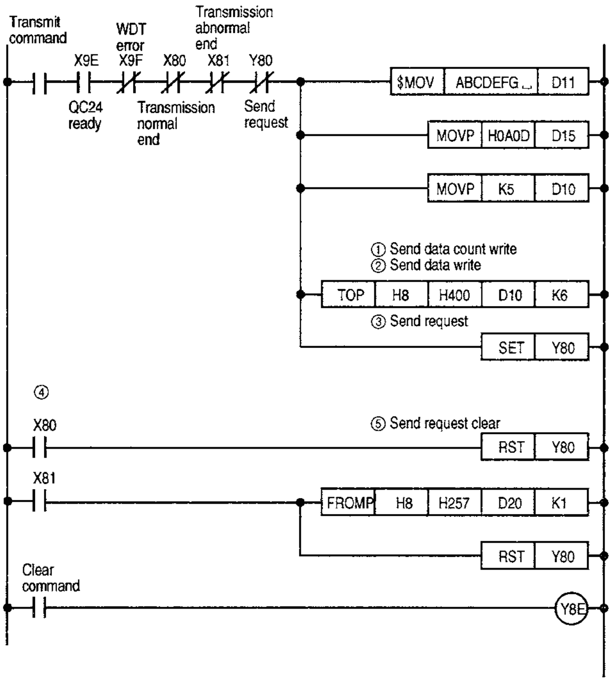
(2) The send data count written in the transmit area head address is not transmitted as data.

10.2.2 Transmission program

The following shows sample sequence programs that transmit data from the PLC CPU to an external device.
The send data is written to the buffer memory transmit area (default value: addresses 400H to 5FFH).

1 Sample sequence program when application instructions used (TO, TOP, DTO, DTOP instructions)

See the programming manual (common instructions) for more information.



* Turn OFF the transmit command signal before turning ON the transmission normal end signal (X80) or transmission abnormal end signal (X81).

Sets the send data and send data count.

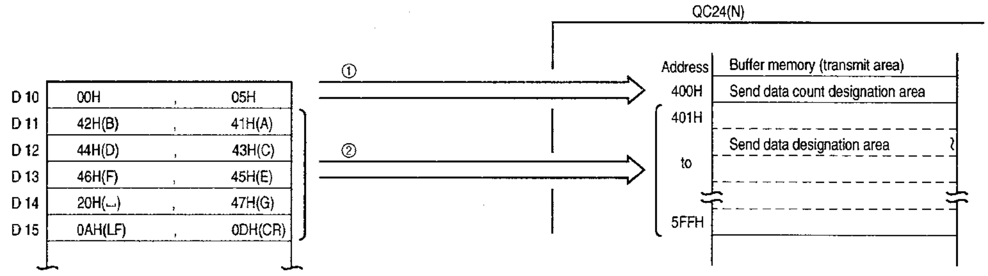
Writes the send data count and send data to the buffer memory.

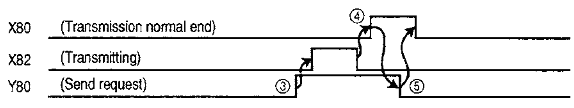
Turns ON the send request signal (Y80) after writing the data.

Turns OFF the send request signal.
Reads the transmission error code
Check the contents of the error and take appropriate action according to the error code stored in D20 and the description given in Section 22.1.

Turns OFF the send request signal.

Turns off the LED and clears the error code.
* See Section 19.1.3 for a description of error code read and clear and of turning off the LED.

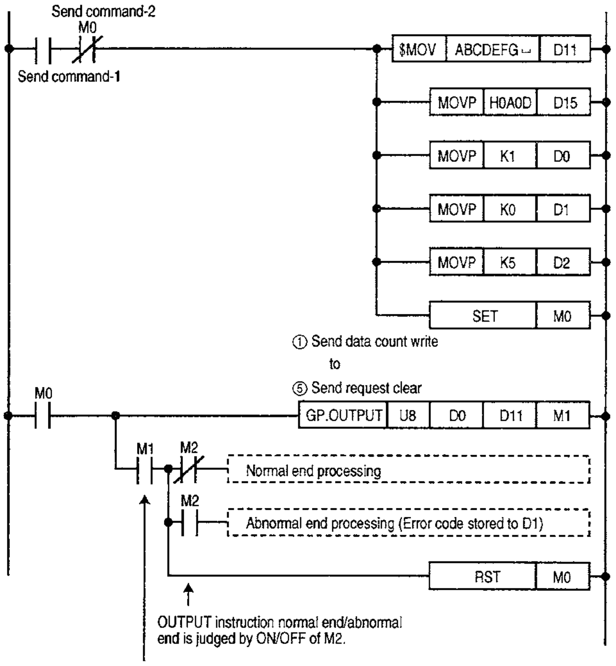




2 Sample sequence program when dedicated instruction used (OUTPUT instruction)

See the programming manual (special function module) for more information.

*Turn OFF the send command-1 signal before turning on the transmission normal end signal (X80) or transmission abnormal end signal (X81).



Sets the send data and send data count.

Designates the No. (CH□) of the interface that is to transmit the data.

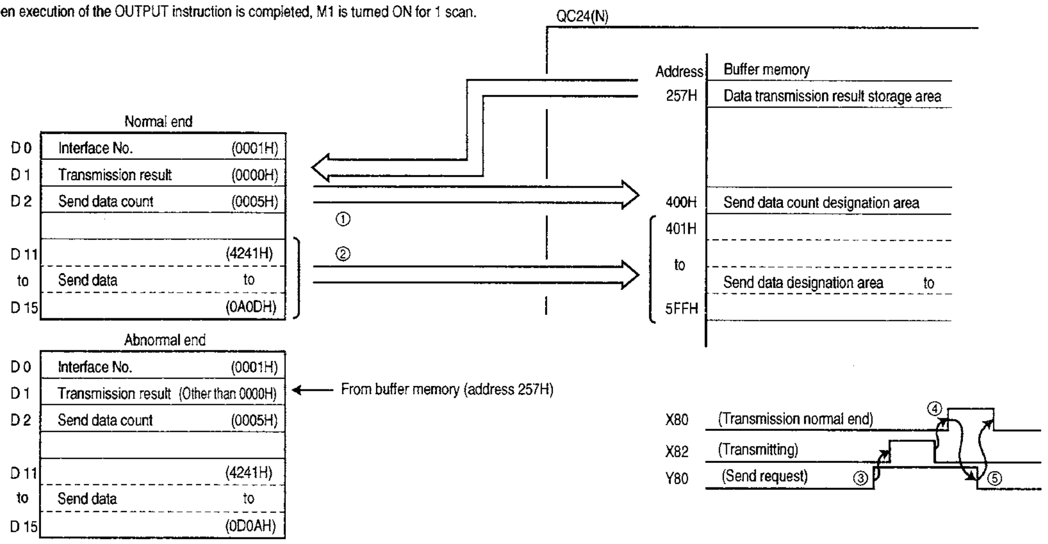
Clears the transmission result storage device to zero.

Designates the send data count for word units. (K10 is designated for byte units.)

Turns ON the send command-2 signal.

Transmits the send data stored in the designated device.
After execution of the OUTPUT instruction is completed, turns on the user designated transmission end signal (M1) for 1 scan.
The PLC CPU writes the send data and send data count to the buffer memory and issues a send request to the QC24(N).

When execution of the OUTPUT instruction is completed, M1 is turned ON for 1 scan.



POINTS

(1) When the QC24(N) dedicated instruction is used, model name registration by I/O allocation of parameters written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and the module name (AJ71QC24) at the slot in which the QC24(N) is installed are set.)

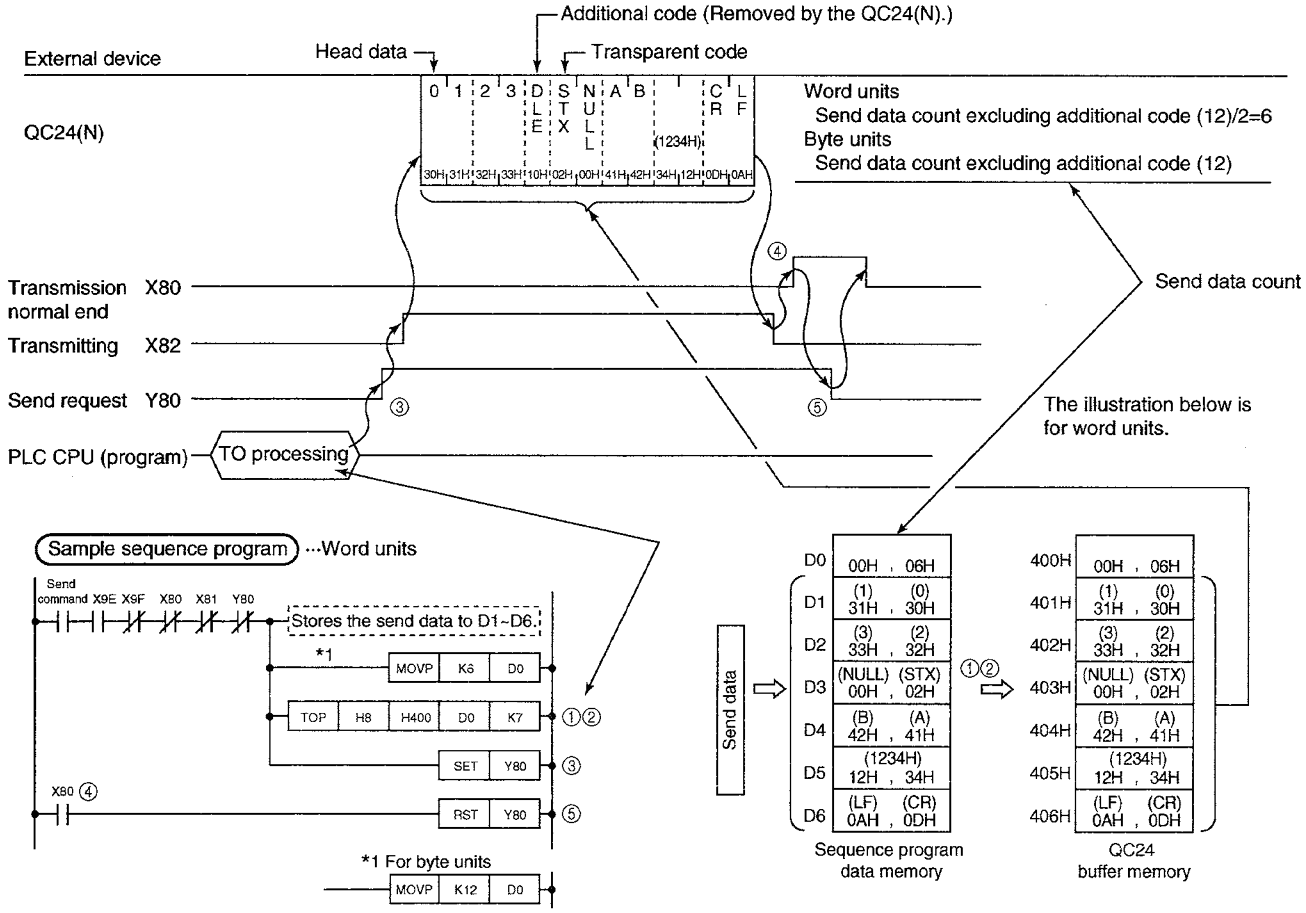
(2) The status of communications by dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of (1) and (2) above.

3 Application example

The following uses a message to describe an example of application when application instructions are used to send data to the external device.
Except for the sequence program, the result of data reception at the external device is the same when a dedicated instruction is used.

① When receive transparent code designated and ASCII-BIN conversion disabled are set
Additional code: 10H (DLE), transparent code: 02H (STX)

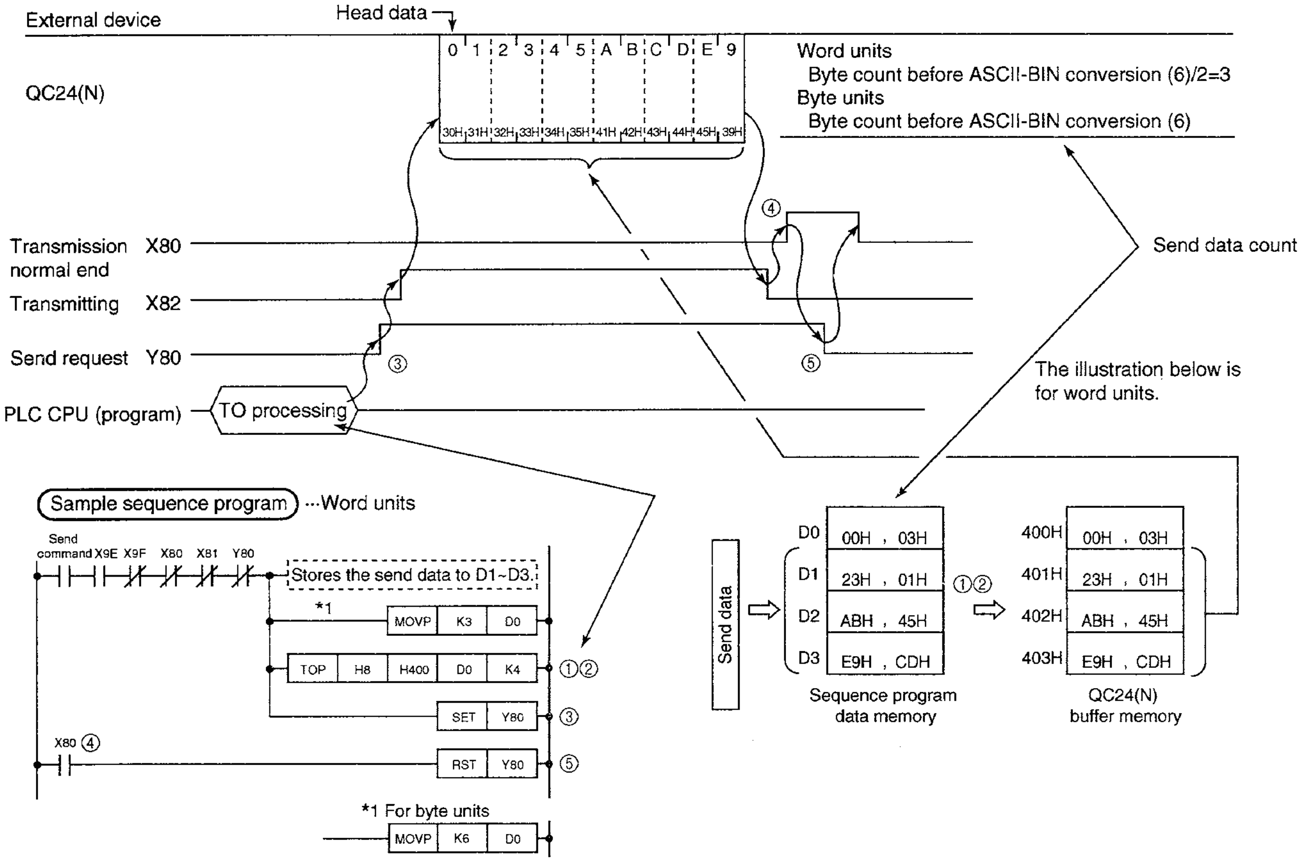


POINTS

(1) The TO instruction write data count is in word units.
When the send data is written to the transmit area by TO instruction during transmission in byte units, the write data count must be corrected to word units (send data count ÷ 2).
For example, when the send data count is 12 bytes and 11 bytes, it is corrected to 6 words.
11 ÷ 2 = 5.5....Fractions are truncated

(2) When the send data count is an odd number of bytes during transmission in byte units, the data of the lower byte of the last send data designation area of the send data designation area is transmitted.

② When transmit transparent code not designated and ASCII-BIN conversion enabled are set



POINTS

(1) The buffer memory transmit area data are converted to 4-byte ASCII code data ("0" to "9", "A" to "F") and transmitted.

(2) The TO instruction write data count is in word units.
When the send data is written to the transmit area by TO instruction during transmission in byte units, the write data count must be corrected to word count (send data count ÷ 2).
For example, when the send data count is 6 bytes and 5 bytes, it is corrected to 3 words.
5 ÷ 2 = 2.5....Fractions are truncated

(3) When the send data count is an odd number of bytes during communications in byte units, the lower byte data of the last send data designation location of the send data designation area are transmitted.

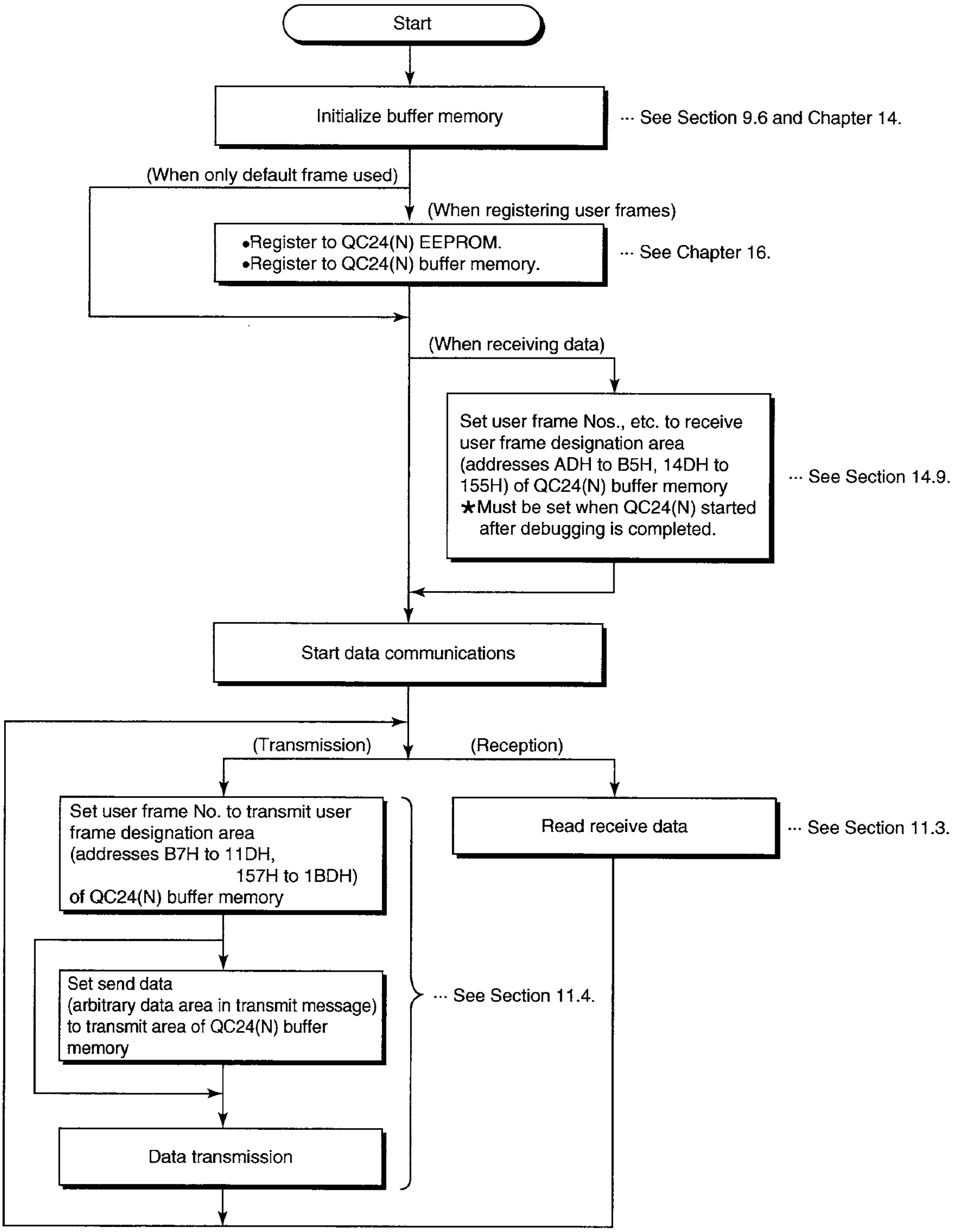
MEMO

11. DATA COMMUNICATIONS USING USER FRAMES

This section describes the data communications method and procedures when the external device and PLC CPU use user frames in data communications using the non procedure protocol.

11.1 Data Communications Procedure

The following outlines the procedure when the external device and PLC CPU use a user frame to exchange data.



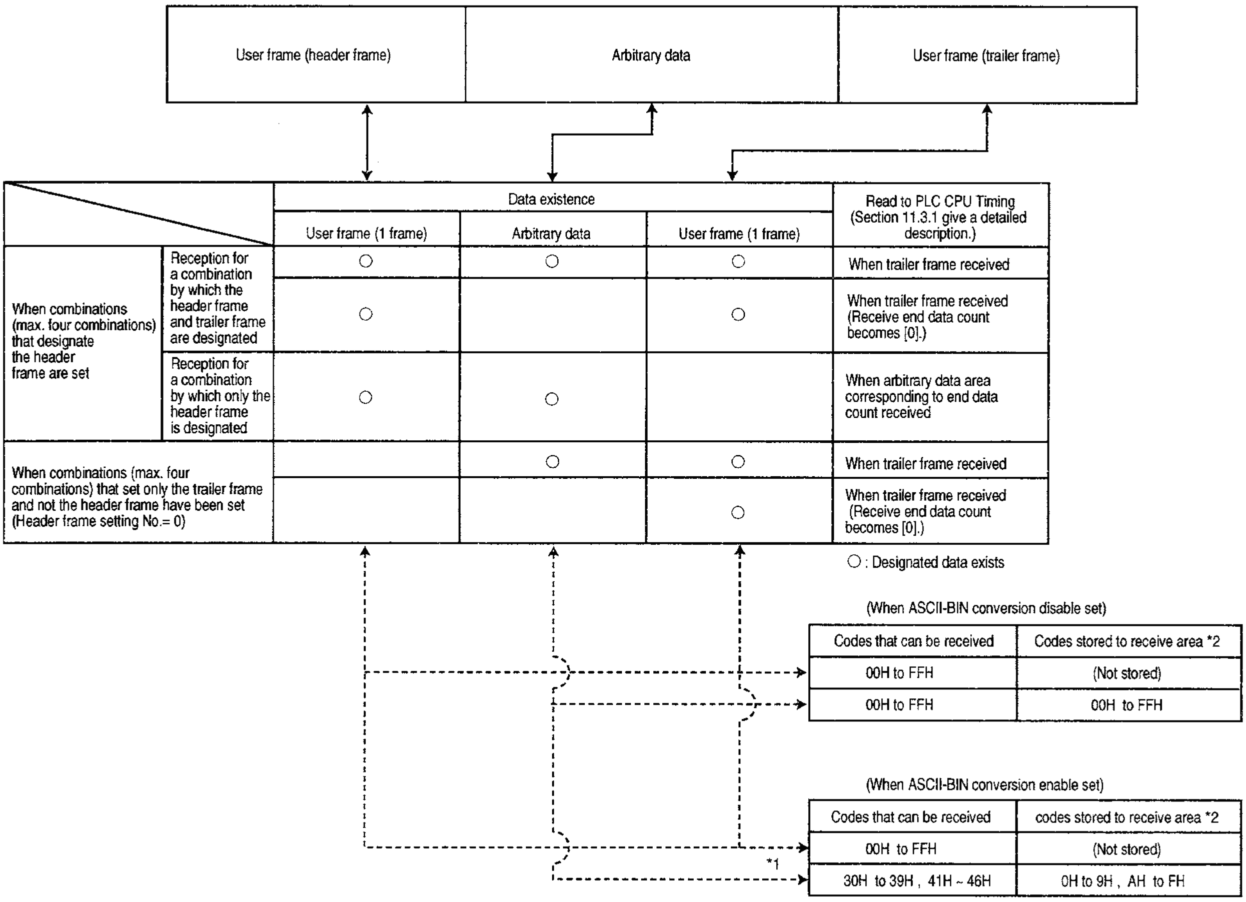
11.2 Send/Receive Data

11.2.1 Receive data

The following describes the data list, codes, and handling of the QC24(N) receive data during data reception using user frames.

1 **Receive data list**

When receiving data via the user registration frame, data of the following format can be received according to the contents of the user registration frames (max. four combinations) for reception set by the user in the buffer memory.



		Data existence			Read to PLC CPU Timing (Section 11.3.1 give a detailed description.)
		User frame (1 frame)	Arbitrary data	User frame (1 frame)	
When combinations (max. four combinations) that designate the header frame are set	Reception for a combination by which the header frame and trailer frame are designated	○	○	○	When trailer frame received
		○		○	When trailer frame received (Receive end data count becomes [0].)
	Reception for a combination by which only the header frame is designated	○	○		When arbitrary data area corresponding to end data count received
When combinations (max. four combinations) that set only the trailer frame and not the header frame have been set (Header frame setting No.= 0)			○	○	When trailer frame received
				○	When trailer frame received (Receive end data count becomes [0].)

○ : Designated data exists

(When ASCII-BIN conversion disable set)

Codes that can be received	Codes stored to receive area *2
00H to FFH	(Not stored)
00H to FFH	00H to FFH

(When ASCII-BIN conversion enable set)

Codes that can be received	codes stored to receive area *2
00H to FFH	(Not stored)
30H to 39H , 41H ~ 46H	0H to 9H , AH to FH

*1 If data of other than 30H to 39H and 41H to 46H are received as the data code of the arbitrary data area (including the transparent code data), QC24(N) ASCII-BIN conversion will generate an error.

*2 Receive data arbitrary data area

① When the arbitrary data area is stored to the receive area, and the storage byte count is an odd number of bytes, the receive data count shown below is stored to the receive data count storage area.
(When ASCII-BIN conversion is enabled, receive data count is the storage byte count when the arbitrary data area is converted to binary code and stored to the receive area.)

- Word units
  Receive data count = Number of bytes stored to receive area ÷ 2....Fractions are truncated
- Byte units
  Receive data count = Number of bytes stored to receive area
  (00H is stored to the lower byte of the last data storage location of the receive area.)

② When ASCII-BIN conversion enabled, make the arbitrary data area of the receive data, excluding the additional code, an odd number of bytes.

POINTS

Handling of QC24(N) receive data

(1) When a user frame (header frame, trailer frame) of a code registered in the QC24(N) is received, receive processing by user frame is performed.

(2) Of the header frame No. and trailer frame No. (maximum 4 sets) initialized by the user at the buffer memory receive user frame designation area, the set No. (□th) of the user frame received from the external device is stored to the receive frame storage area.

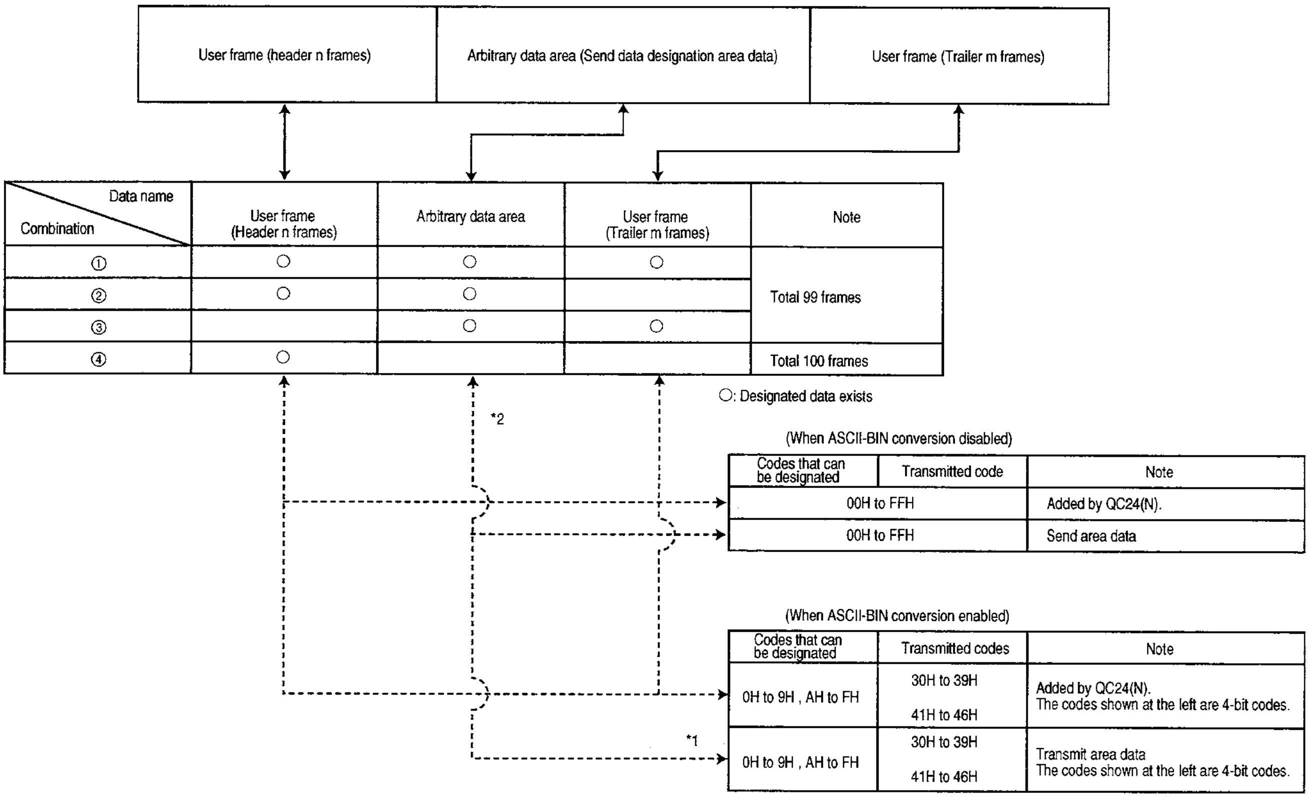
(3) If receive transparent code is designated, the data of the additional code included in the arbitrary data area is removed immediately after reception (before conversion when the receive data is converted from ASCII code to binary code).

11.2.2 Send data

The following describes the data list, codes, and handling of the QC24(N) send data during user frame data transmission.

1 Send data list

Only the data list combinations shown below are allowed during user frame data transmission.



User frame (header n frames)	Arbitrary data area (Send data designation area data)	User frame (Trailer m frames)

Combination \ Data name	User frame (Header n frames)	Arbitrary data area	User frame (Trailer m frames)	Note
①	○	○	○	Total 99 frames
②	○	○		
③		○	○	
④	○			Total 100 frames

○: Designated data exists

(When ASCII-BIN conversion disabled)

Codes that can be designated	Transmitted code	Note
00H to FFH		Added by QC24(N).
00H to FFH		Send area data

(When ASCII-BIN conversion enabled)

Codes that can be designated	Transmitted codes	Note
0H to 9H , AH to FH	30H to 39H 41H to 46H	Added by QC24(N). The codes shown at the left are 4-bit codes.
0H to 9H , AH to FH	30H to 39H 41H to 46H	Transmit area data The codes shown at the left are 4-bit codes.

*1 Four bits of 0H to FH data are converted to 30H to 39H and 41H to 46H ASCII data and transmitted as the data codes of the data to be transmitted (including the transparent code data).

*2 Send data arbitrary data area

① When the send data count designated by the PLC CPU during transmission in byte units is an odd number of bytes, the data of the lower byte of the trailer send data storage location of the send data area are transmitted.

② When ASCII-BIN conversion is enabled, the data to be transmitted is transmitted as 2 characters/byte.

POINTS

Handling of QC24(N) send data

(1) The data of the user frame and the data of the transmit area designated from the PLC CPU are transmitted in the contents and order set in the buffer memory send user frame designation area.

(2) User frame area data corresponding to the registered contents are converted to ASCII-BIN data or are not converted to ASCII-BIN data and transmitted.

(3) For the arbitrary data area, the transmit area data are converted from ASCII code to binary code or are not converted from ASCII code to binary code and transmitted.

(4) If transmit transparent code is designated, the additional code data is added in front of the transparent code/additional code in the data of the designated area during transmission and transmitted.

11.3 Receive (External Device → QC24(N))

"Reception" is storing of the data received from an external device to the buffer memory receive area by the QC24(N) system and reading of the stored data from the sequence program by FROM instruction.

This section describes reception through the QC24(N) CH1 interface.

11.3.1 Reading the receive data

The following describes reading of the receive data during user frame data reception.

1 Comparison of functions when user frames not used

The following compares the functions when user frames are used and are not used.

<table>
<tr><th></th><th>When user frames used
(See 2 for the timings.)</th><th>When user frames not used</th></tr>
<tr><td>Reception start</td><td>When header frame and trailer frame set:
When header frame received.
When header frame set:
When header frame received.
When trailer frame set:
When header frame of arbitrary data area received.
When header frame and trailer frame only set:
When header frame received.</td><td>When header frame received.</td></tr>
<tr><td rowspan="3">Reception complete</td><td colspan="2">When the cause of reception complete (timing that reads the received data to the PLC CPU) is one of the following.</td></tr>
<tr><td>(According to the preset conditions. See 2.)</td><td>—</td></tr>
<tr><td>• When receive end code received.
• When number of data corresponding to receive end data count received.
• When trailer frame received.
• When an receive error (no reception watchdog timer (timer 0) time-up, etc.) generated.
* The arbitrary data received before one of the following is received, or generated, are stored to the buffer memory receive area.</td><td>• When receive end code received.
• When number of data corresponding to receive end data count received.
• When receive error (no reception watchdog timer (timer 0) timeup, etc.) generated.
* All the received data are stored to the buffer memory receive area.</td></tr>
</table>

2 Receive data and read timing

The following shows the timing when the PLC CPU is requested to read the receive data by user frame trailer frame, receive end data count, or receive end code.

The numbers in the table are the receive message and timing pattern Nos. given on the next page.

Setting		Receive data / Receive data size of arbitrary data area	Timing pattern No. (See the next page.)					Notes
			When end code received before header frame	When end code received after header frame	When header frame received	When arbitrary data area of receive message received	When trailer frame received	
Header frame and trailer frame set	End code	Receive data count > end data count	Removed [Everything other than the header frame is removed.]	3-2*	3-2			* The end code data is handled as part of the arbitrary data area.
		Receive data count ≤ end data count		3-1*	3-1			
	No end code	Receive data count > end data count		3-2*	3-2			
		Receive data count ≤ end data count		3-1*	3-1			
Only header frame set	End code	Receive data count > end data count		4-2*	4-2			
		Receive data count ≤ end data count		4-1*	4-1			
	No end code	Receive data count > end data count		4-2*	4-2			
		Receive data count ≤ end data count		4-1*	4-1			
Only trailer frame set	End code	Receive data count > end data count	1-2		5-2 / 6-1			When only the trailer frame is set, the watchdog timer (timer 0) does not monitor the data receive interval.
		Receive data count ≤ end data count	1-1		5-1 / 6-1			
	No end code	Receive data count > end data count	2-2		5-2 / 6-1			
		Receive data count ≤ end data count	2-1		5-1 / 6-1			

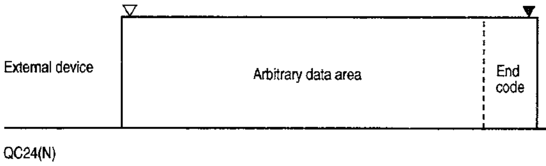
POINT

When the QC24(N) detects a receive error during data reception, it stores the arbitrary data area of the data received up to generation of the error to the buffer memory receive area and turns ON the error detected signal (Xn4).

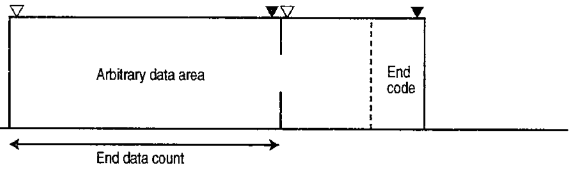
[When a receive error is detected during receiving the trailer frame, the arbitrary data area of the receive data is stored in the receive area.]

Receive start and receive end (read) timing patterns

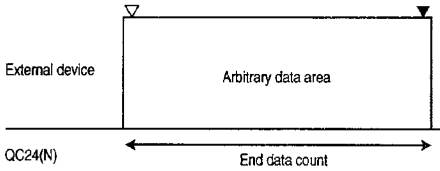
① Pattern No. 1-1



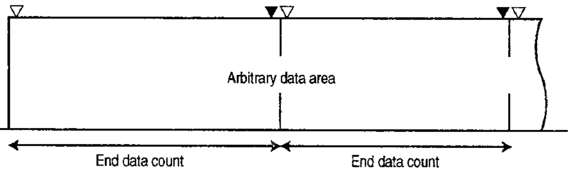
Pattern No. 1-2



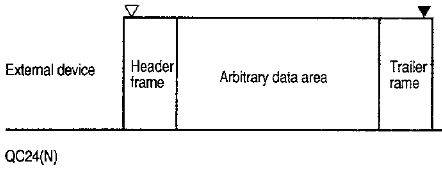
② Pattern No. 2-1



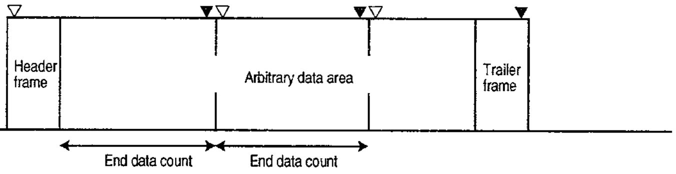
Pattern No. 2-2



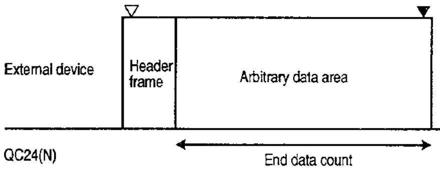
③ Pattern No. 3-1



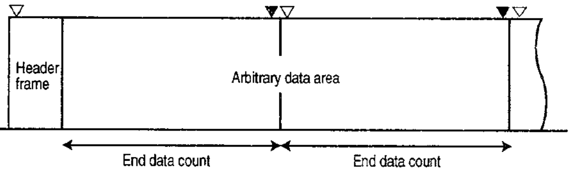
Pattern No. 3-2



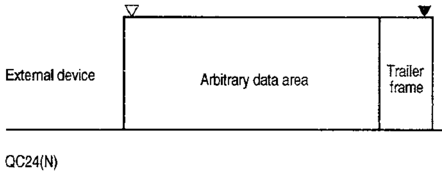
④ Pattern No. 4-1



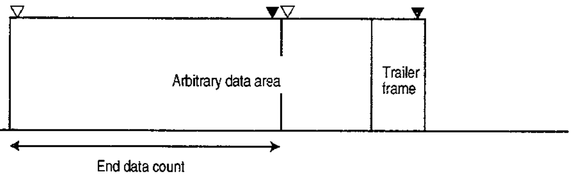
Pattern No. 4-2



⑤ Pattern No. 5-1



Pattern No. 5-2



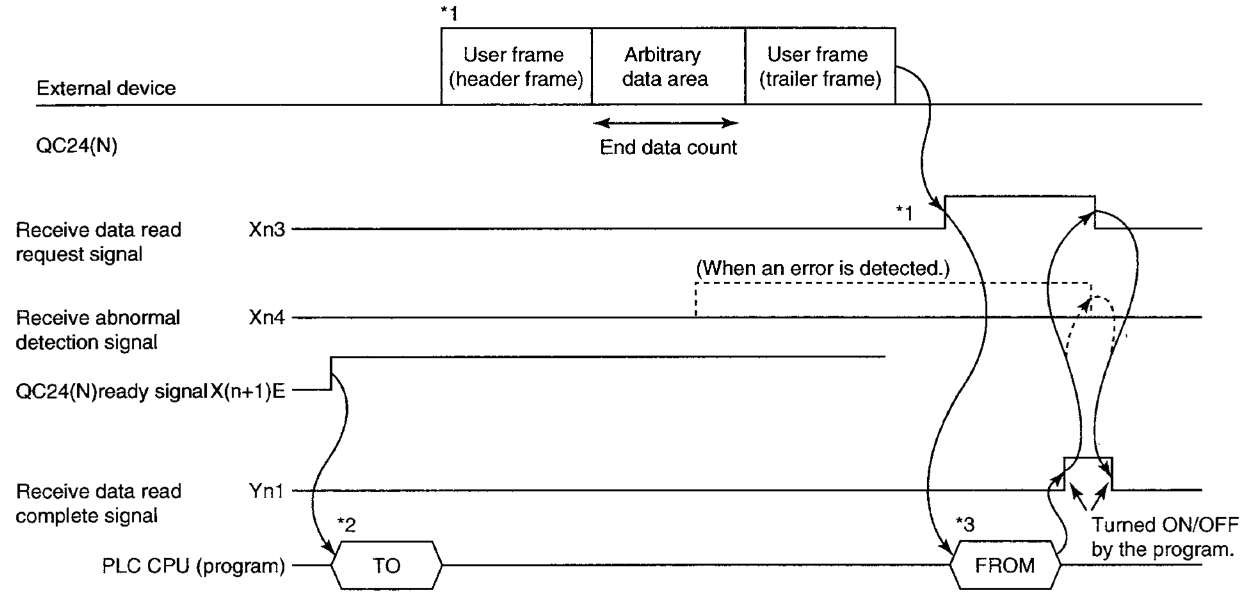
⑥ Pattern No. 6-1

▽: Receive start timing
▼: Receive end timing (read timing)

11.3.2 Receive procedure

The following shows the receive procedure when a message containing a user frame is received and the arbitrary data area is read to the PLC CPU.

Procedure



*1 See Section 11.3.1 $\boxed{2}$ for the receive message and the timing that reads the receive data to the PLC CPU.

*2 Sets the receive user frame registration No., etc. to the receive user frame designation area (addresses: ADH to B5H).
During debugging, make this setting before data reception, but after debugging is complete, make this setting when starting the QC24(N). (See Section 14.9.)

*3 Reading (① below) for checking which user frame was received by the QC24(N) from the PLC CPU and reading of the receive data (② below).

① Reads which of the user frames set in the receiver user frame designation area was received from the receive user frame storage area (address: 25BH).

② Reads the arbitrary data area of the receive message from the receive area (default addresses: 600H to 7FFH).

11.3.3 Receive program

The following describes a sample sequence program that reads the receive data stored in the QC24(N) buffer memory to the PLC CPU when data containing a user frame was received.
In the description of this sample program, user frame data reception is described for the following:

① QC24(N) I/O signals

QC24(N) installed at QnACPU I/O signals addresses 80H to 9FH.

② QC24(N) interface used in data communications with external device

QC24(N) CH1 RS-232C interface

③ QC24(N) set station No.

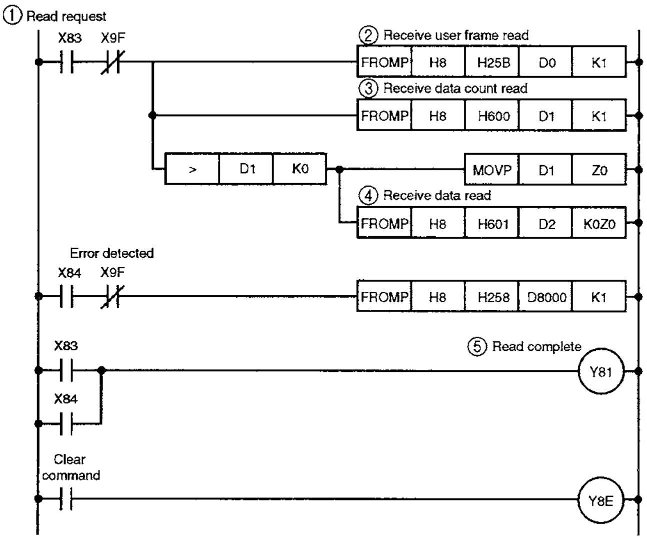
The QC24(N) set station No. is [01]. (Used at header frame of user frames.)

④ Initialization contents of CH1 buffer memory special applications area for data communications using user frames
The QC24(N) default value for the area shown below depends on the description contents.
(In any case, it changes when the QC24(N) is started (when the QC24(N) ready signal X (n+1) E is ON).)
Areas other than the areas shown below use the QC24(N) default value.

Address	Name	Set contents	Notes	Reference section
96H	Word/byte designation area	Word/byte	Set according to the example.	14.4
A4H	Receive end data count	6 to 511	Depends on the example.	14.8
A5H	Receive end code	None	—	
ADH	User frame use control	Use	See the illustration.	14.9
AEH to B5H	Header frame No. designation Trailer frame No. designation	Yes		
120H	Receive transparent code designation	YES/NO	When YES, additional code: 10H (DLE) transparent code: 02H (STX)	14.10
121H	ASCII-BIN conversion designation	Enable/disable	Set according to the example.	14.11

1 Sample sequence program when using application instructions (FROM, FROMP, DFRO, DFROP instructions)

See the programming manual (common instructions) for more information.
This program reads the registered user frame set No. to D0 and reads the received data, beginning from D2.
(QC24(N) I/O signals 80H to 9FH)



Reads the receive user frame set No. and receive data count.

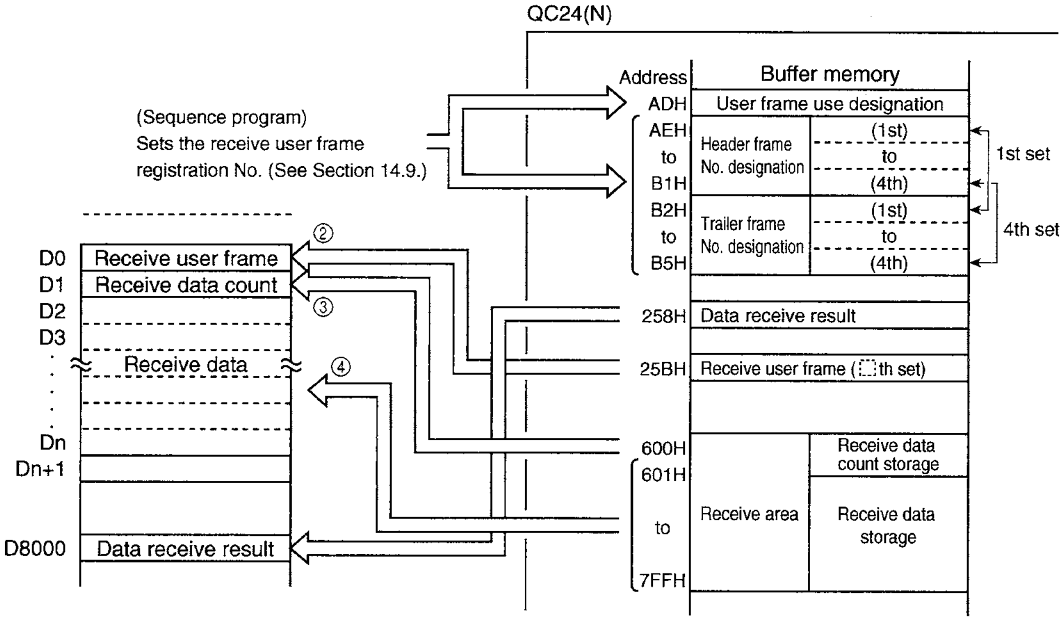
Stores the read received data count to index register (Z0). (The illustration at the left is for word units.)

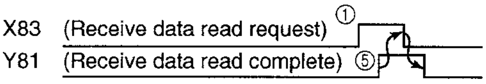
Reads the number of receive data corresponding to the receive data count.

When the error detection signal (X84) is turned ON, reads the receive error code.

Turns ON the receive data read complete signal.
* Processes the data read at step ④ as receive data.

Turns off the LED and clears the error code.
Check the error contents with the error code stored in D8000 and take the action described in Section 22.1.
* See Section 19.1.3 for a description of clearing of the error code and turning off of the LED.





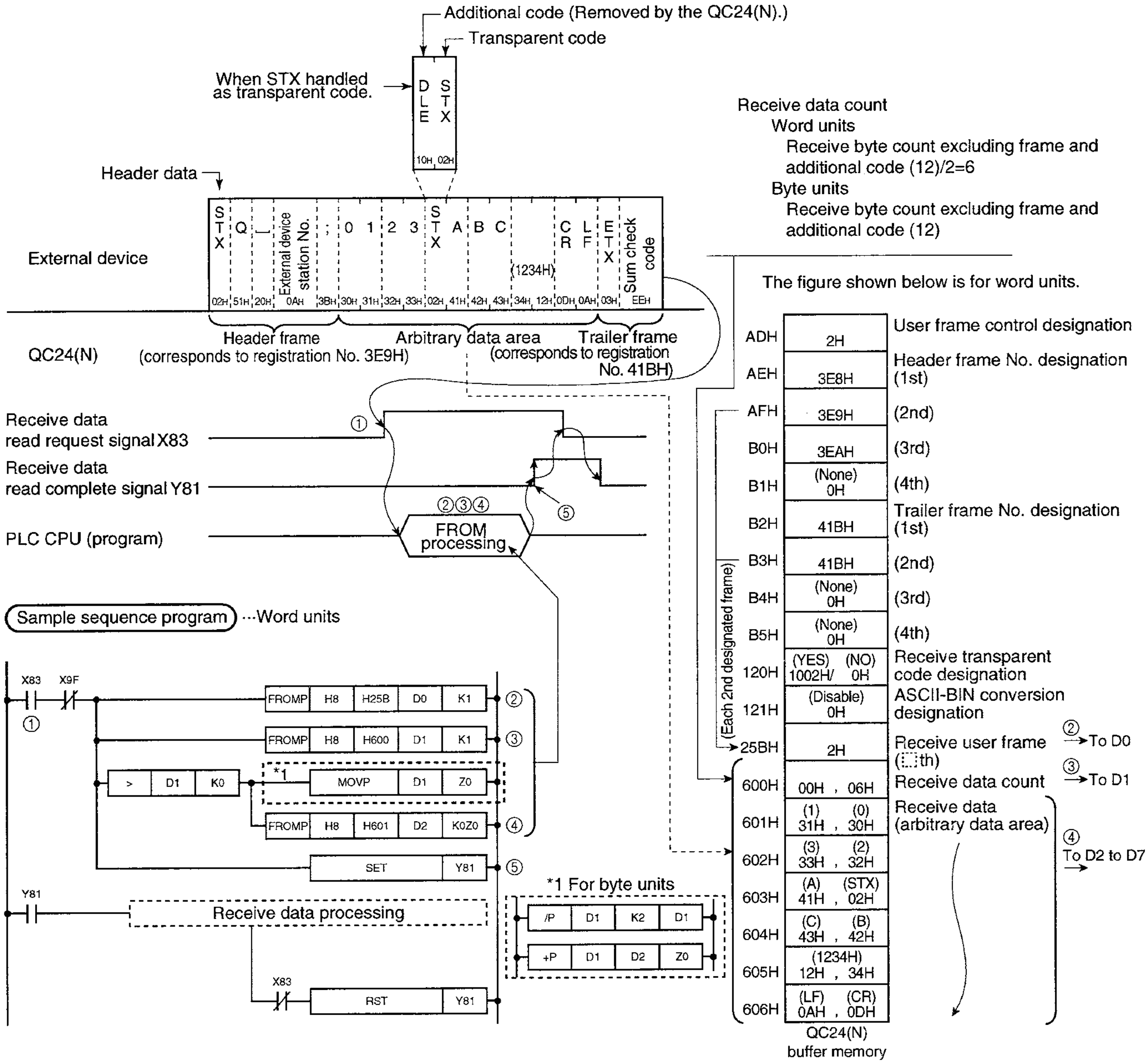
POINT

The dedicated instruction INPUT can be used to read the receive data count and receive data of the data received using user frames, the same as data reception in arbitrary format.
See Section 10.1.2 for a sample sequence program when the INPUT instruction is used.

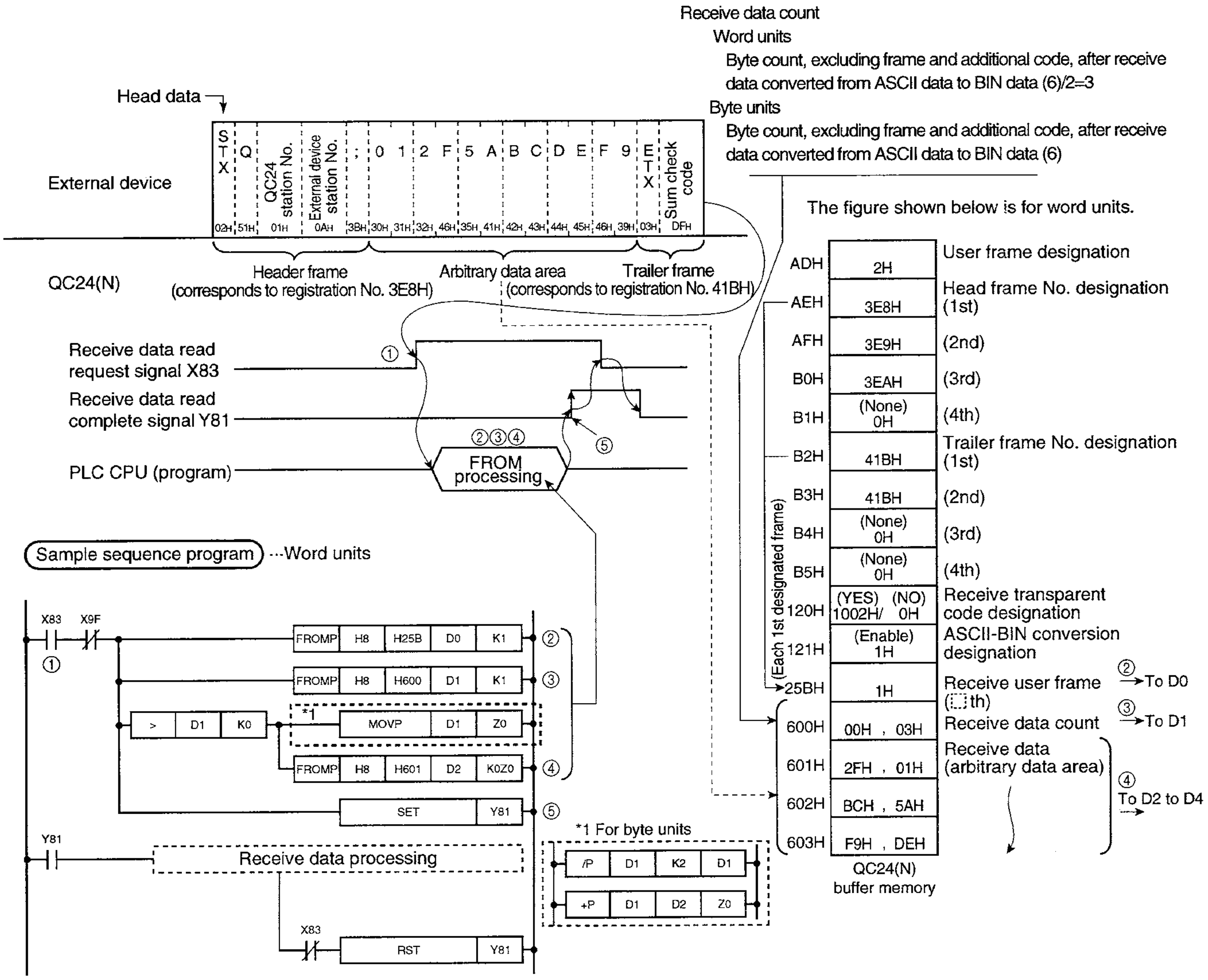
2 Application example

(a) When receiving using header frame, arbitrary data, and trailer frame combination

① When ASCII-BIN conversion disable set

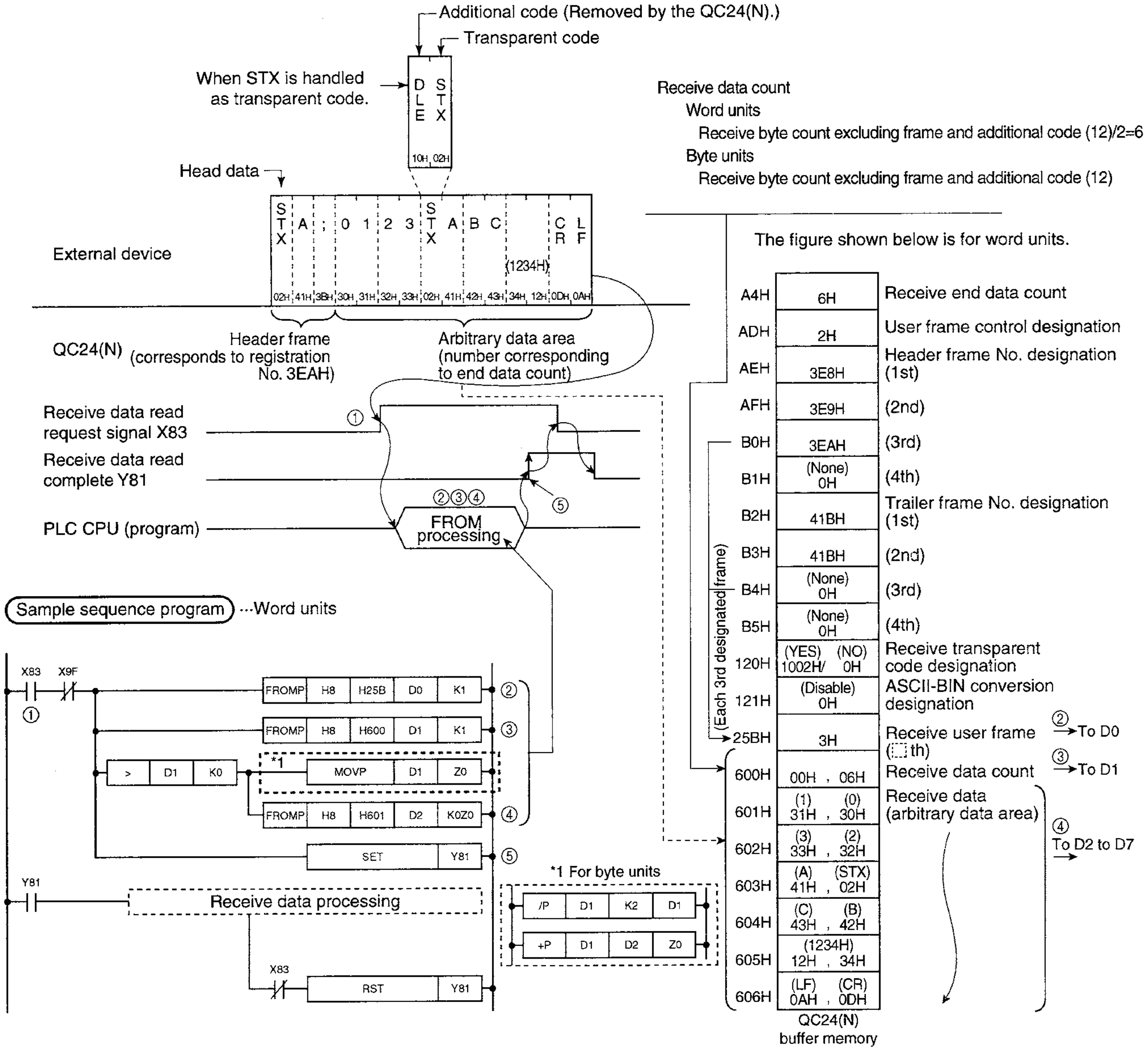


② When ASCII-BIN conversion enable set



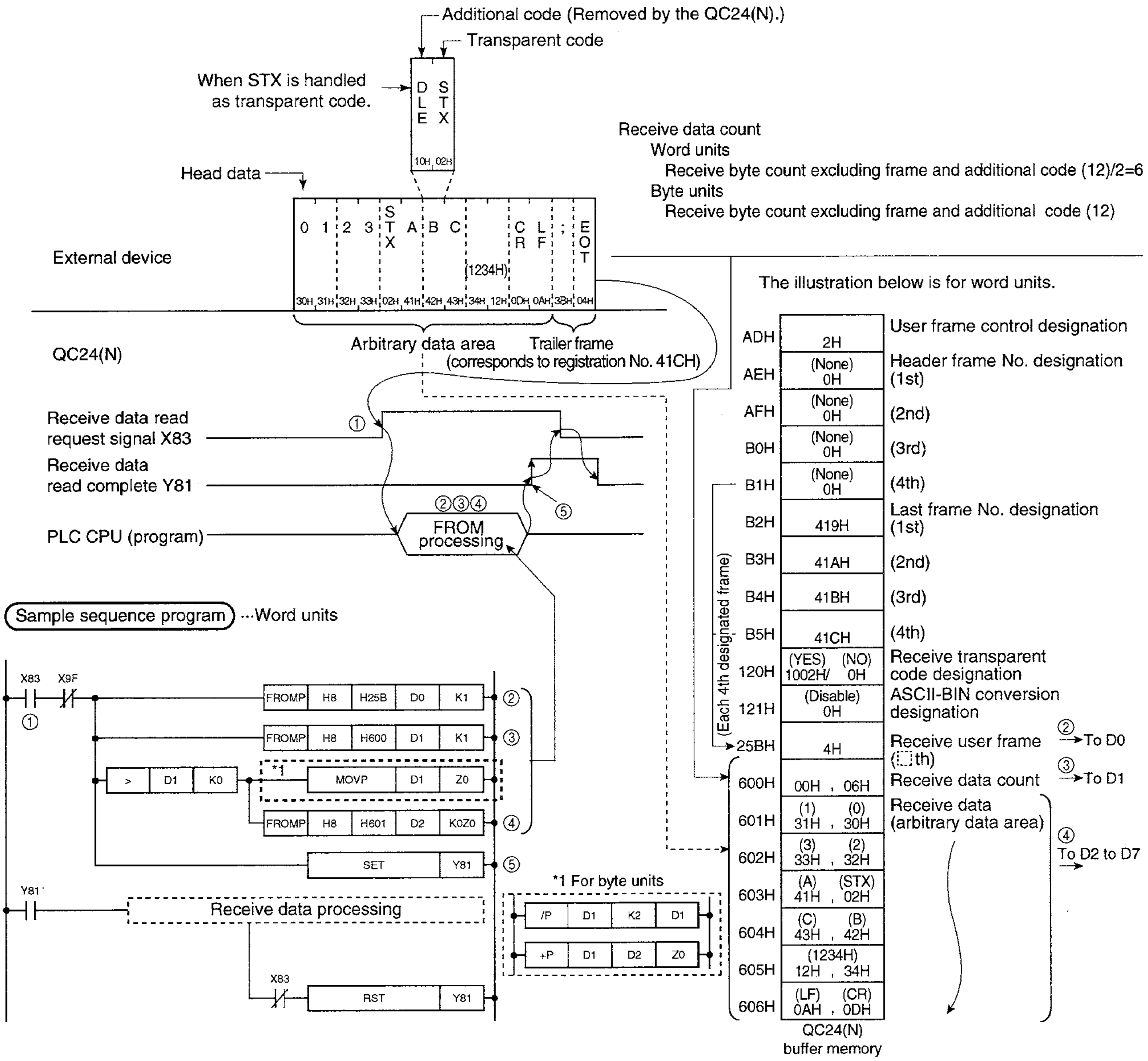
(b) When receiving using header frame and arbitrary data combination

When ASCII-BIN conversion is disabled and the end data count is set to 6 words/12 bytes.

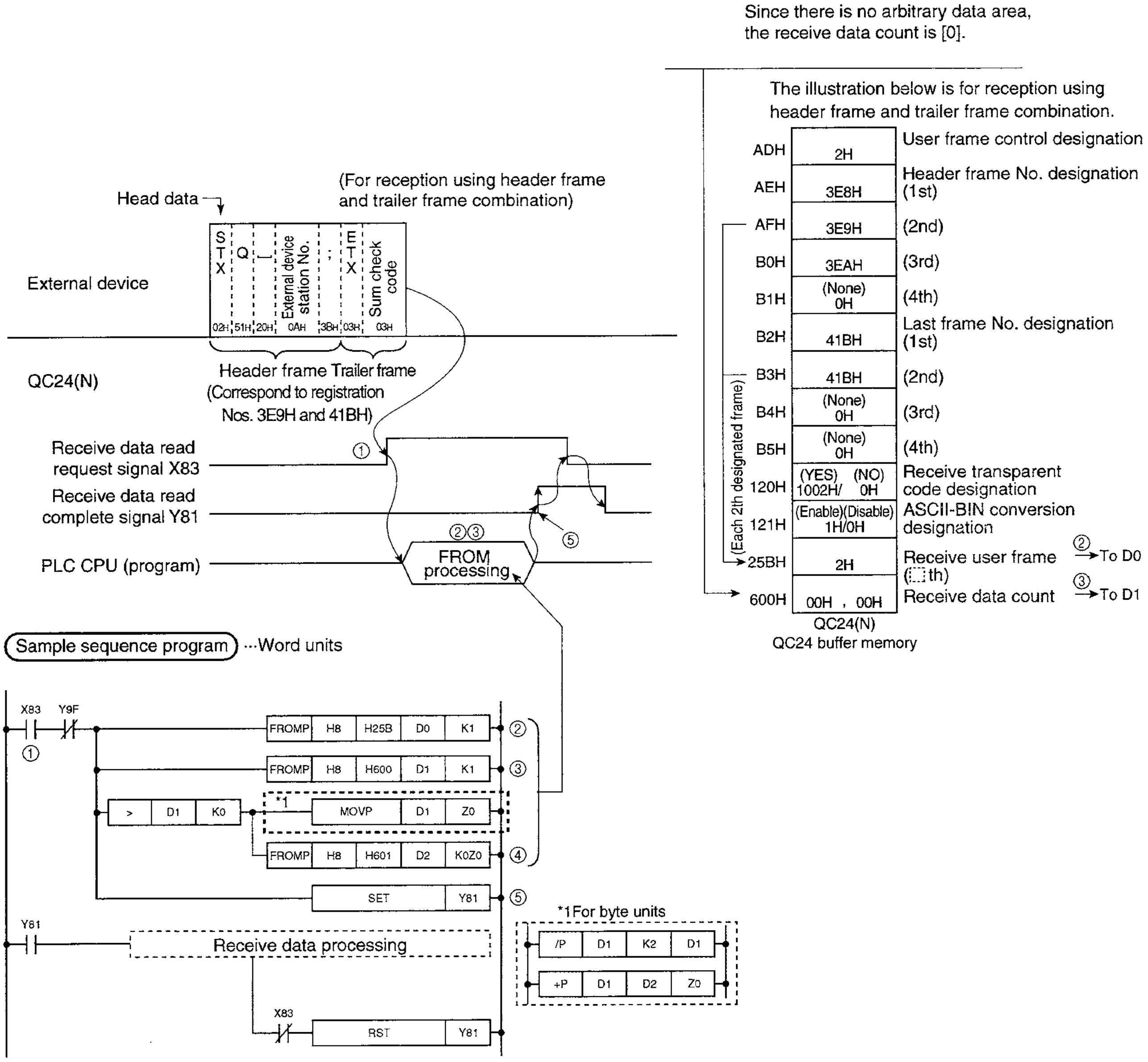


(c) When receiving using arbitrary data and trailer frame combination

When ASCII-BIN conversion disable is set.



(d) When receiving user frame only



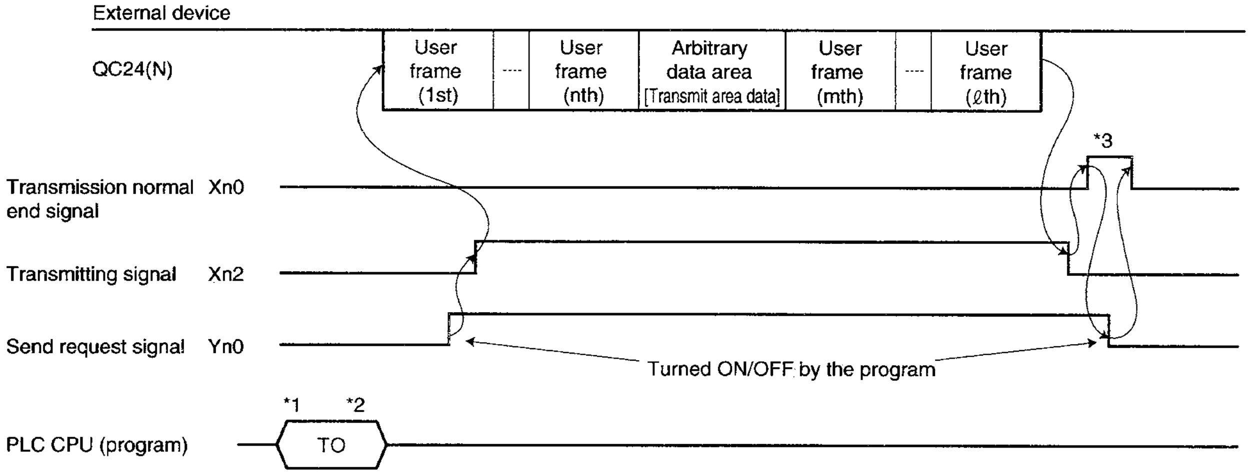
11.4 Transmission (QC24(N) → External Device)

The transmit function transmits the data written to the buffer memory transmit area from the sequence program by TO instruction to the external device from the QC24(N) when the PLC CPU issues a send request.
This section describes transmission through the QC24(N) CH1 interface.

11.4.1 Transmission procedure

The following describes the transmission procedure when transmitting a message containing user frames to the external device.

Procedure



*1 PLC CPU processing

Before issuing a send request to the QC24(N), designate (write) the following data.

- Transmit user frame designation area
  User frame No., transmission method and transmission order registered in the QC24(N)
- Transmit area
  User data corresponding to transmit message arbitrary data area

*2 Write the data to be transmitted to the output No. designation area with one of the following values.

0H : Do not transmit (Data designated after this are not transmitted.)
1H to 3E7H / 4001H to 43E7H : Transmit default registration frame of designated No.
3E8H to 4AFH / 43E8H to 44AFH : Transmit user frames of designated Nos. (number of frames registered to EEPROM)
8000H / C000H : Transmit the data in the buffer memory send data storage area
8001H to 801FH / C001H to C01FH : Transmit user frames of designated Nos. (number of frames registered to buffer memory)

*3 When a transmit data count error or data transmission error is generated, the QC24(N) stores the error code to the data transmission result storage area (addresses: 257H/ 267H) and turns ON the transmission abnormal end signal (Xn1).

11.4.2 Transmission program

This section describes sample programs that transmit data containing user frames.

In the description of the sample programs, data transmission using user frames is described for the following conditions. case:

① QC24(N) I/O signals

QC24(N) installed at QnACPU I/O signal addresses 80H to 9FH.

② QC24(N) interface used in data communications with the external device

QC24(N) CH1 RS-232C interface

③ QC24(N) set station No.

The QC24(N) set station No. is [01]. (Used by user frames)

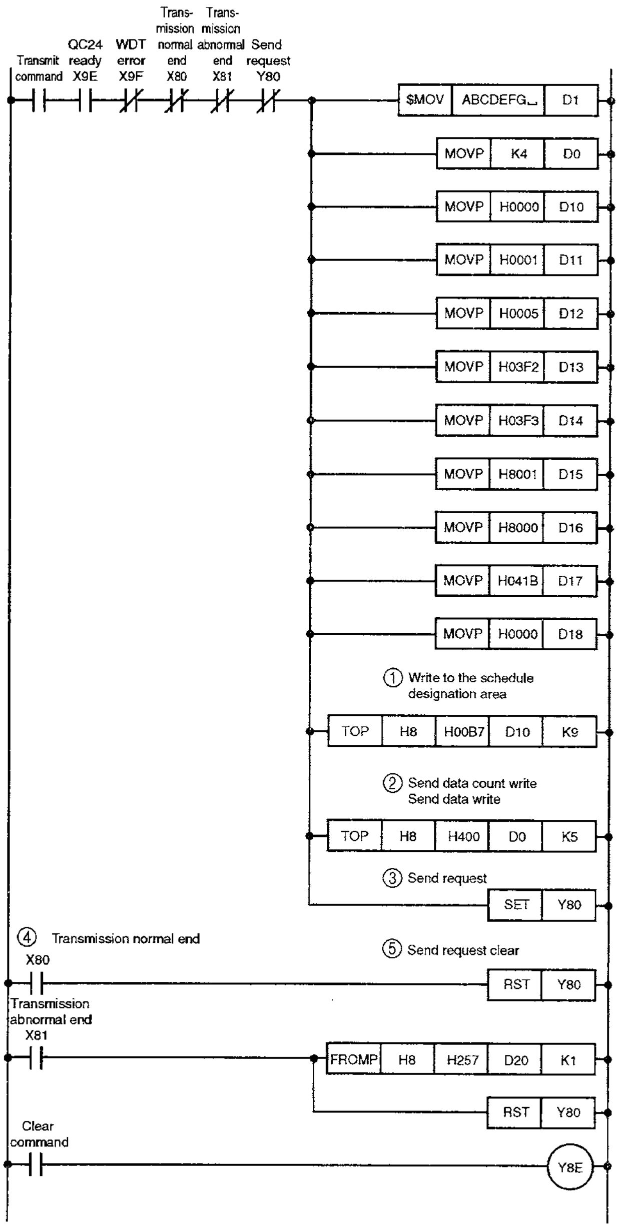
④ Initialization contents of CH1 buffer memory special applications area for data transmission using user frames

The QC24(N) default value of the following areas depends on the description contents.
(The default values change when the QC24(N) starts (QC24(N) ready signal X (n+1) E ON).)
Areas other than the following use the QC24(N) default value.

Address	Name	Setting contents	Notes	Reference section
96H	Word/byte designation area	Word/byte	Set according to the example.	14.4
11FH	Transmit transparent code designation	YES/NO	When YES: Additional code: 10H (DLE) Transparent code: 02H (STX)	14.10
121H	ASCII-BIN conversion designation	Enable/disable	Set according to the example.	14.11

1 Sample sequence program when application instructions used (TO, TOP, DTO, DTOP instructions)

This sample program is the same as the sample program shown in Section 10.2.2 except for the part that designates the user frames to be transmitted, etc. at the schedule designation area.
See the programming manual (common instructions) for more information.



* Turn OFF the transmit command signal before turning ON the transmission normal end signal (X80) or transmission abnormal end signal (X81).

Sets the send data and send data count.

Sets the data to be written to the buffer memory schedule designation area.

Writes the data from the CR/LF output designation data to the output frame No. designation data to the schedule designation area.

Writes the send data count and send data.

Turns ON the send request signal.

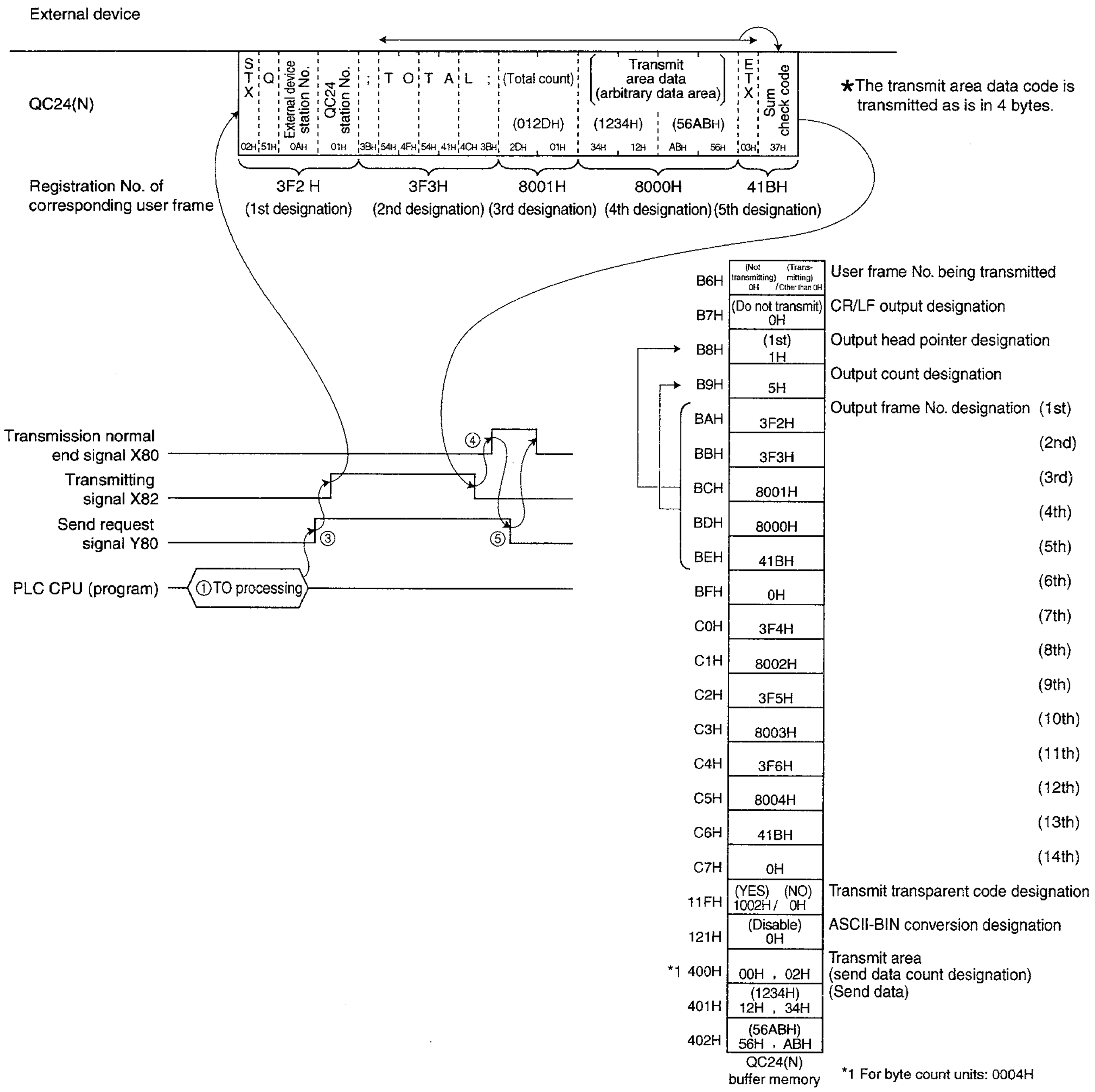
If the data transmission complete signal was turned ON, turns OFF the send request signal.

When the transmission abnormal end signal (Xn1) was turned ON, reads the transmission error code.

Turns OFF the send request signal.

Turns off the LED and clears the error code.
Check the error contents with the error code stored in D20 and take the action described in Section 22.1.
* See Section 19.1.3 for a description of error code read and clear and turning off of the LED.

① ASCII-BIN conversion disable set



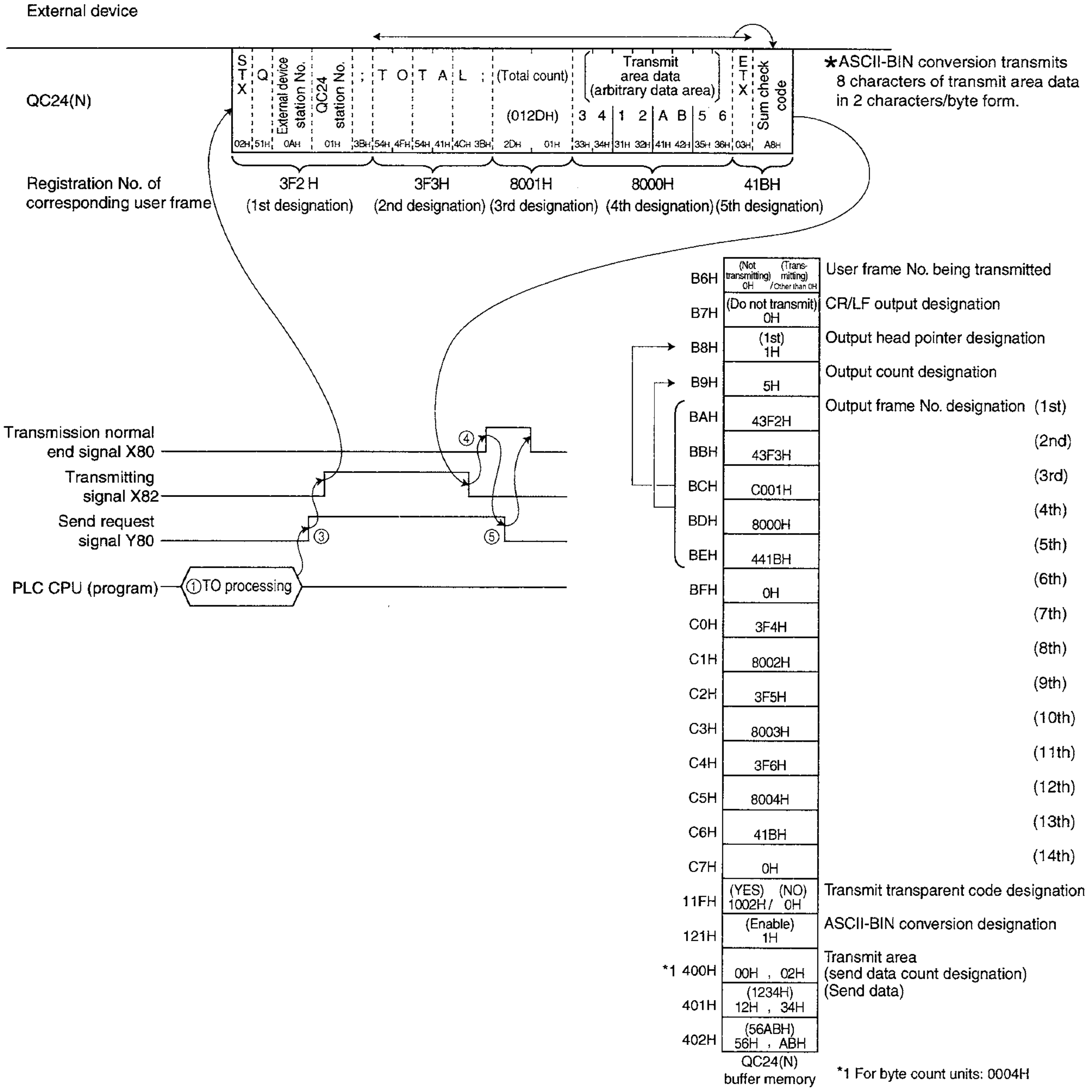
★The transmit area data code is transmitted as is in 4 bytes.

B6H	(Not transmitting) 0H / (Transmitting) Other than 0H	User frame No. being transmitted
B7H	(Do not transmit) 0H	CR/LF output designation
B8H	(1st) 1H	Output head pointer designation
B9H	5H	Output count designation
BAH	3F2H	Output frame No. designation (1st)
BBH	3F3H	(2nd)
BCH	8001H	(3rd)
BDH	8000H	(4th)
BEH	41BH	(5th)
BFH	0H	(6th)
C0H	3F4H	(7th)
C1H	8002H	(8th)
C2H	3F5H	(9th)
C3H	8003H	(10th)
C4H	3F6H	(11th)
C5H	8004H	(12th)
C6H	41BH	(13th)
C7H	0H	(14th)
11FH	(YES) (NO) 1002H / 0H	Transmit transparent code designation
121H	(Disable) 0H	ASCII-BIN conversion designation
*1 400H	00H , 02H	Transmit area (send data count designation)
401H	(1234H) 12H , 34H	(Send data)
402H	(56ABH) 56H , ABH	

QC24(N) buffer memory

*1 For byte count units: 0004H

② ASCII-BIN conversion enable set



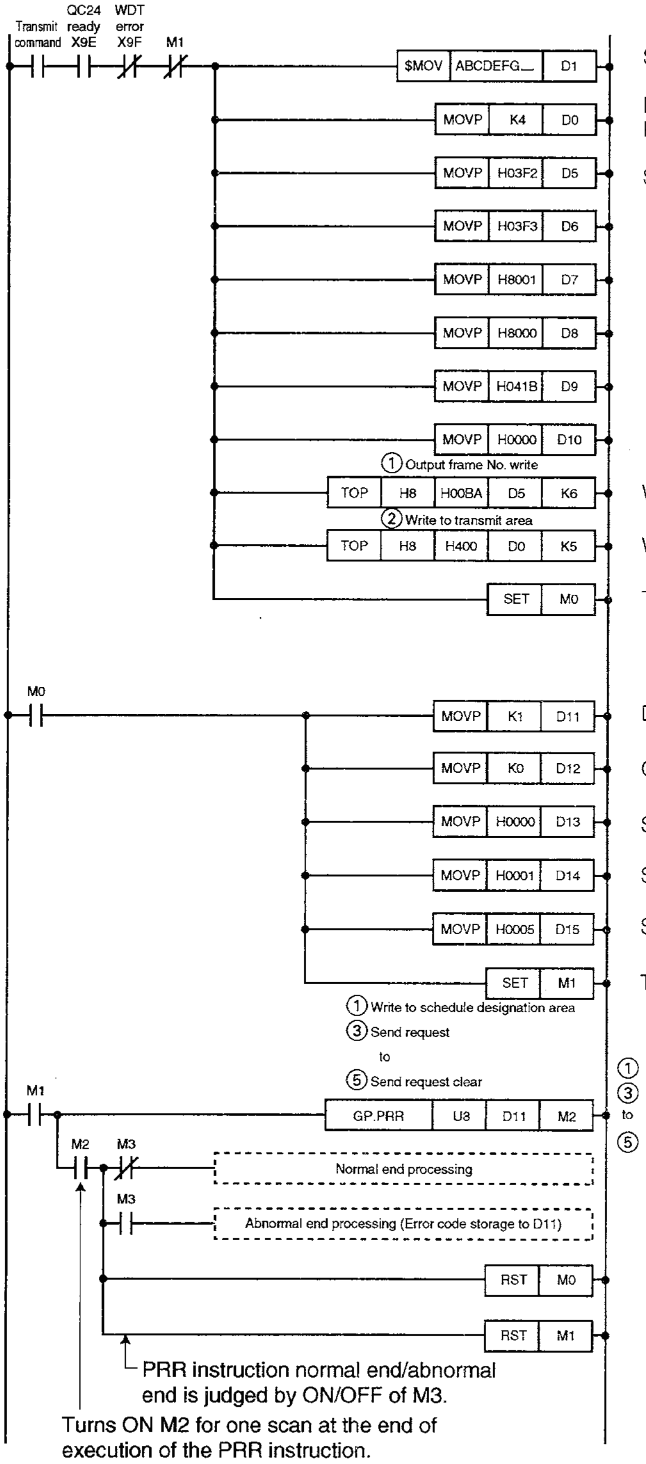
★ASCII-BIN conversion transmits 8 characters of transmit area data in 2 characters/byte form.

B6H	(Not transmitting) 0H / (Transmitting) Other than 0H	User frame No. being transmitted
B7H	(Do not transmit) 0H	CR/LF output designation
B8H	(1st) 1H	Output head pointer designation
B9H	5H	Output count designation
BAH	43F2H	Output frame No. designation (1st)
BBH	43F3H	(2nd)
BCH	C001H	(3rd)
BDH	8000H	(4th)
BEH	441BH	(5th)
BFH	0H	(6th)
C0H	3F4H	(7th)
C1H	8002H	(8th)
C2H	3F5H	(9th)
C3H	8003H	(10th)
C4H	3F6H	(11th)
C5H	8004H	(12th)
C6H	41BH	(13th)
C7H	0H	(14th)
11FH	(YES) 1002H / (NO) 0H	Transmit transparent code designation
121H	(Enable) 1H	ASCII-BIN conversion designation
*1 400H	00H , 02H	Transmit area (send data count designation)
401H	(1234H) 12H , 34H	(Send data)
402H	(56ABH) 56H , ABH	

*1 For byte count units: 0004H

2 Sample sequence program when dedicated instruction used (PRR instruction)

This sample program is the same as the sample program shown in Section 10.2.2 except for the part that designates the user frame to be transmitted at the schedule designation area. See the programming manual (special function module) for more information.



PRR instruction normal end/abnormal end is judged by ON/OFF of M3.

Turns ON M2 for one scan at the end of execution of the PRR instruction.

Sets the send data.

Designates the word units send data count. (For byte units, designates K8.)

Sets the output frame No. [When the data list shown in item (1) is transmitted.]
(1st...User frame)
(2nd...User frame)
(3rd...User frame)
(4th...Transmit area data)
(5th...User frame)
(6th...Not designated)

Writes the output frame No. to the buffer memory. *1

Writes the send data count and send data to the buffer memory.

Turns ON the transmit command-2 signal.

Designates the No. (CH□) of the interface that is to transmit the data.

Clears the transmission result storage device to zero.

Sets "Do not transmit CR/LF".

Sets output head pointer (1).

Sets the output count (5).

Turns ON the transmit command-3 signal.

	Normal end	Abnormal end
D0	Send data count (0004H)	Send data count (0004H)
D1	(4241H)	(4241H)
to	Send data to	Send data to
D4	(2047H)	(2047H)
D5	Output frame No. (03F2H)	Output frame No. (03F2H)
D6	(03F3H)	(03F3H)
D7	(8001H)	(8001H)
D8	(8000H)	(8000H)
D9	(041BH)	(041BH)
D10	(0000H)	(0000H)
D11	Interface No. (0001H)	Interface No. (0001H)
D12	Transmission result (0000H)	Transmission result (other than 0000H)
D13	CR/LF output (0000H)	CR/LF output (0000H)
D14	Output head pointer (0001H)	Output head pointer (0001H)
D15	Output count (0005H)	Output count (0005H)

See 1 for the send data list.

*1 Before executing the PRR instruction, the user frame No. to be transmitted and the send data count and send data must be written to the buffer memory.

POINTS

(1) Except for the sequence program, the result of data reception at the external device when the dedicated instruction is used is the same as when application instructions are used.

(2) When the QC24(N) dedicated instruction is used, model name registration by parameter I/O allocation written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and the module name (AJ71QC24) at the slot in which the QC24(N) is installed are set.)

(3) The status of data communications using the dedicated instruction can be read with the SPBUSY instruction.

(4) See the programming manual (special function module) for a detailed description of (2) and (3) above.

MEMO

BIDIRECTIONAL PROTOCOL

This section outlines the functions and describes the data communications procedure, etc. needed to use the QC24(N) communication procedure to transmit data between external device and PLC CPU through the serial communications module

Data communications using bidirectional protocol can be performed only when the external device and QC24(N) are connected in a 1:1 configuration.

Always read this section when designating mode 7 by setting the QC24(N) mode switch to "7" or by switching the mode and using the objective interface with the bidirectional protocol.

When using the objective interface with a dedicated protocol or the non procedure protocol, you do not have to read this section.

12. DATA COMMUNICATIONS USING BIDIRECTIONAL PROTOCOL

The bidirectional protocol is a data communications function that uses the QC24(N) communications procedure to communicates arbitrary data between an external device and PLC CPU.

The user selects the format of the user data part of the message transmitted and received by the external device and PLC CPU.

Sequence programs for data transmission and data reception are necessary at the PLC CPU.

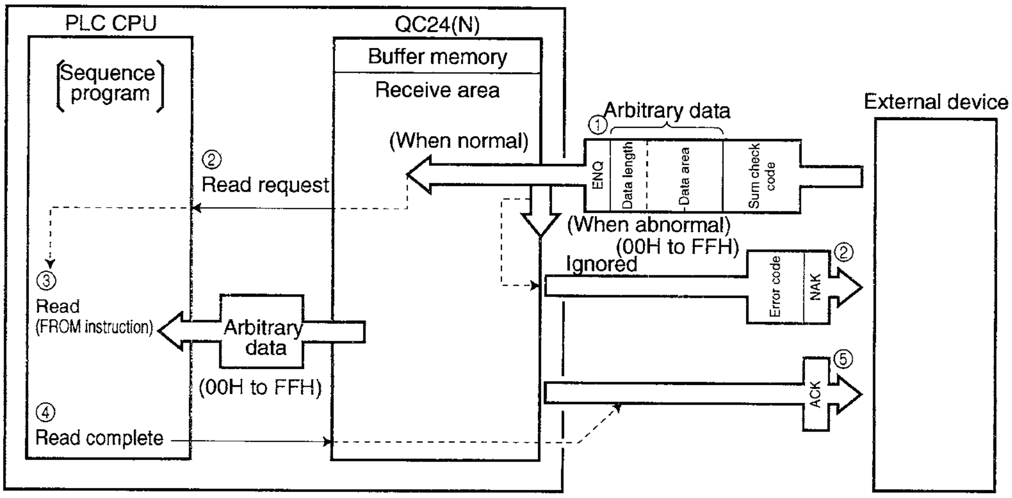
12.1 Bidirectional Protocol PLC CPU Access Timing

The following shows the processing flow at the PLC CPU when data is communicated between an external device and the PLC CPU.

ⓝ in the illustrations indicate the processing flow order.

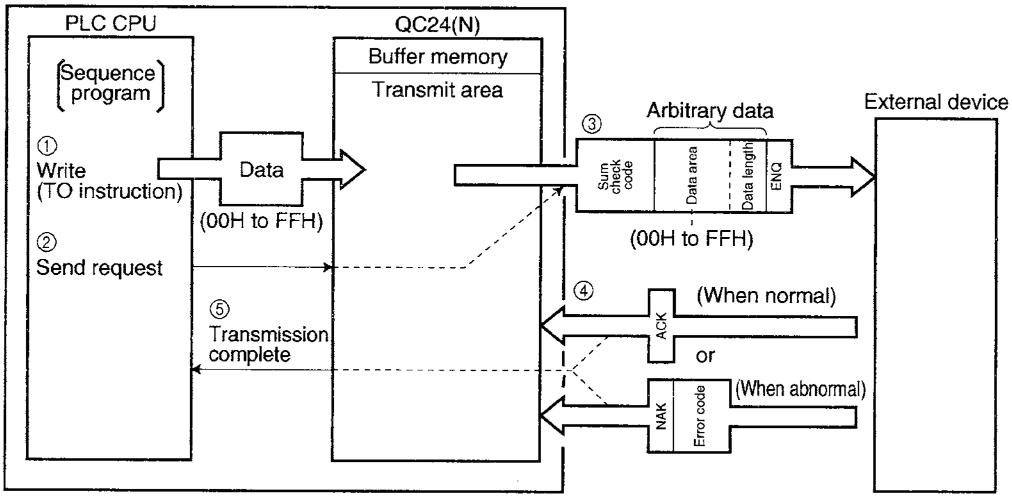
1 When PLC CPU receives data from external device

When the receive data request signal (input signal) between the PLC CPU and QC24(N) changes from OFF to ON, the arbitrary data of the message received from the external device is read to the PLC CPU from the QC24(N) buffer memory.



2 When PLC CPU transmits data to external device

When the send request signal (output signal) between the PLC CPU and QC24(N) changes from OFF to ON, the QC24(N) adds the control code, etc. to the data written to its buffer memory and transmits the data to the external device.



12.2 Communications Functions

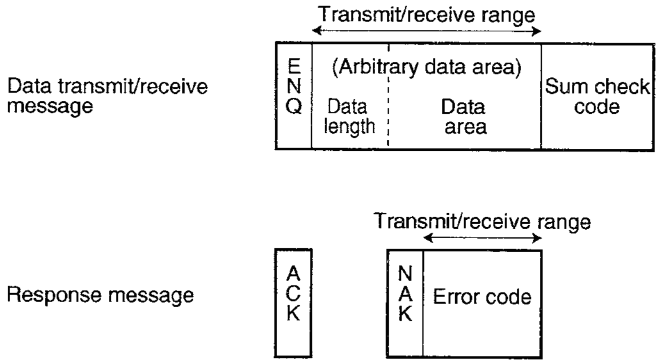
The table below shows the functions for communicating data between an external device and the PLC CPU using the bidirectional protocol.

Function		Processing	Reference section
Transmit/receive in QC24(N) message format	Transmit (PLC CPU → external device)	Transmits the data written to the QC24(N) buffer memory using the TO instruction, etc. to the external device. When a response message is received from the external device after data transmission, transmission processing is completed.	Chapter 12 Chapter 13
	Receive (External device → PLC CPU)	Stores the data received from the external device to the buffer memory and sends a read request to the PLC CPU. When the PLC CPU completes reading the data, it sends a response message to the external device.	
Transmit/receive using ASCII-BIN conversion *1		During transmission and reception in QC24(N) message format, this function converts the arbitrary data area designated by the user from ASCII data to binary data. During transmission, this function converts the transmit area send data count and send data to ASCII data and transmits it. During reception, this function converts the arbitrary data area of the receive data to binary data and stores it to the buffer memory.	Chapter 13
Transmit/receive using transparent code designation *2		During transmission and reception in QC24(N) message format, this function transmits and receives the messages by adding the data (additional code) designated by the user directly before the data (transparent code) designated by the user. During transmission, this function adds the additional code data directly before the transparent code data. When the QC24 detects transparent code + additional code data during reception, it removes the additional code data and receives the remaining data.	

*3

Note

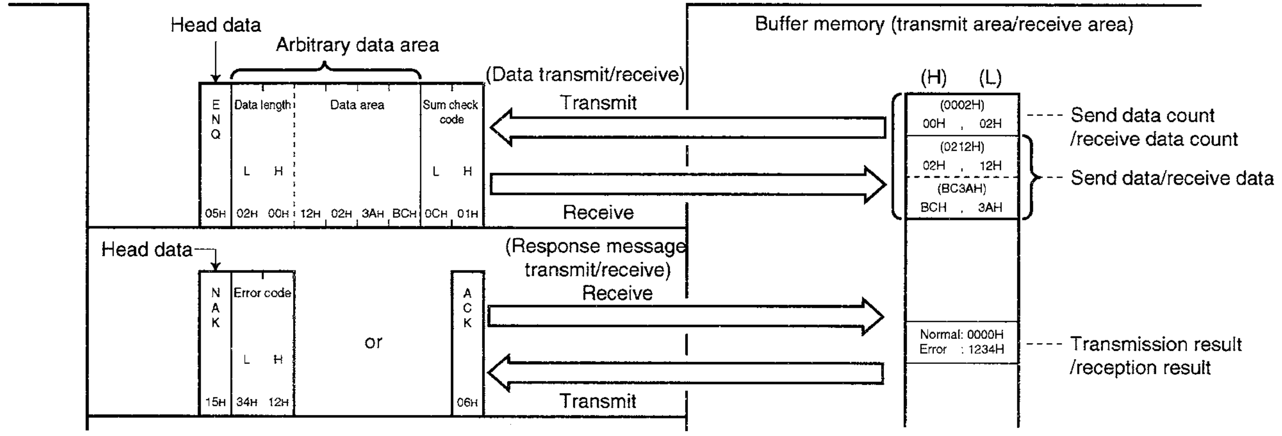
The following shows the transmit and receive message ASCII-BIN conversion and transparent code designation additional code addition and removal ranges.



*1 The PLC CPU uses this function to handle all the send and receive data as binary data.
During transmission and reception in QC24(N) message format, the QC24(N) transmits and receives the data shown in 1 and 2 according to the buffer memory ASCII-BIN conversion designation area (addresses: 12CH/1C1H) designation.

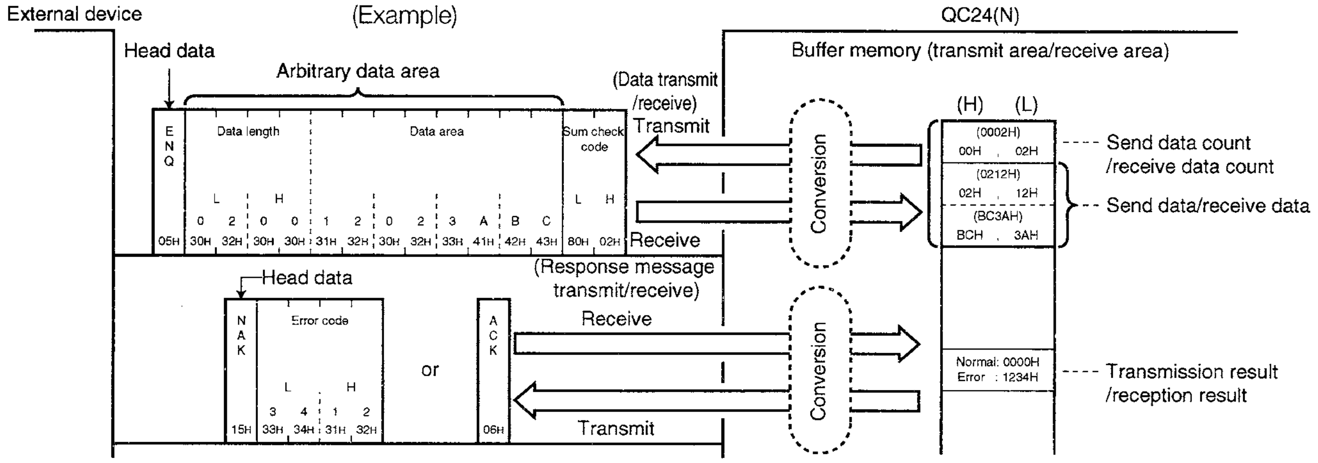
1 ASCII-BIN conversion not designated (no conversion)

① The QC24(N) transmits and receives data codes 00H to FFH data as the arbitrary data area.
② During data reception, the QC24(N) stores the arbitrary data area as is to the buffer memory.
③ During data transmission, the QC24(N) transmits the data designated by the PLC CPU (arbitrary data area of transmit message) as is.
(Example)



2 ASCII-BIN conversion designated

① The QC24(N) transmits and receives data codes 30H to 39H ("0" to "9") and 41H to 46H ("A" to "F") data.
② During data reception, the QC24(N) assumes that the arbitrary data area is ASCII data and converts it to binary data and stores the binary data to the buffer memory.
If an error code is transmitted while the response message is being transmitted, the QC24(N) converts the error code to ASCII data and transmits it to the external device.
③ During data transmission, the QC24(N) assumes that the data designated by the PLC CPU (arbitrary data area of transmit message) is binary data and converts it to ASCII data and transmits the ASCII data to the external device.
If an error code is received while the response message is being received, the QC24(N) converts the error code to binary data and stores the binary data to the buffer memory.
(Example)



*2 This function handles the external device 1-byte transmission control data as user data. During transmission and reception in QC24(N) message format, the QC24(N) transmits and receives the additional code and transparent code designation data described in 1 and 2 to the buffer memory transmit/receive transparent code designation area (addresses: 11FH to 120H/ 1BFH to 1C0H) according to the setting of the codes shown below .

- Transparent code .... 1-byte transmission control data code
- Additional code .... 1-byte data code that is added immediately before the transparent code and additional code data during transmission
  During reception, the QC24 removes this 1-byte code. (The QC24 receives the 1 byte of data immediately following this code.)

1 **Transparent code not designated**

The QC24(N) transmits and receives the send/receive data without performing the processing described in 2 below.

2 **Transparent code designated**

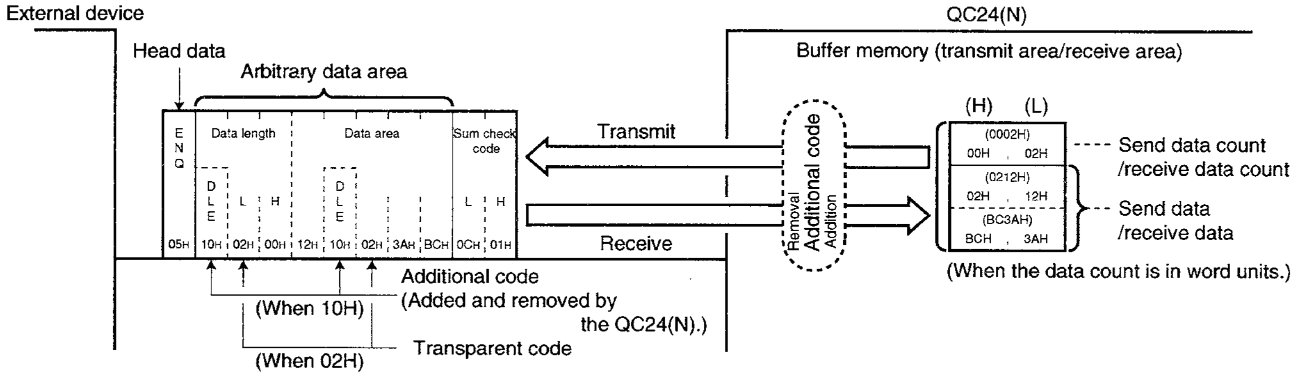
① The QC24(N) adds and removes the additional code designation data.
During data transmission and reception, the QC24(N) performs this processing on the arbitrary data area and response message error code area.
(The QC24(N) does not perform this processing on the head code (ENQ, ACK, NAK) and sum check code area of each message.)

② When the QC24(N) detects a receive additional code during data reception, it removes the additional data and receives the 1 byte of data immediately following the additional data as the receive data area.
When the QC24(N) detects transmit transparent code/additional code data during transmission of the response message sent in reply to data reception, it adds the additional code designation immediately before the code data in the response message and transmits the response message to the external device.

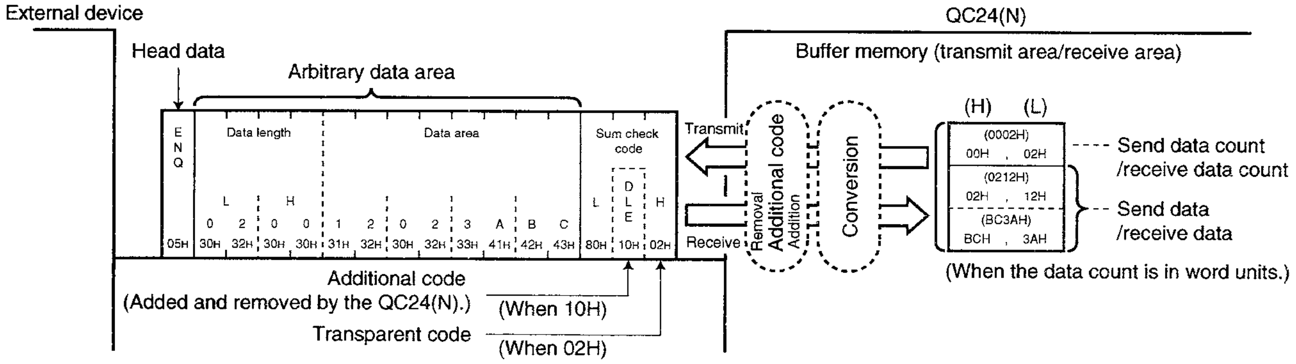
③ When the QC24(N) detects transmit transparent code/additional code data during data transmission, it adds the additional code designation data immediately before the code data and transmits the data to the external device.
When the QC24(N) detects receive additional data while a message is being received in reply to data transmission, it removes the additional code data and receives the 1 byte of data immediately following the additional code data as part of the receive data.

(Example) The data lists when data is transmitted and received are shown below. (The transmit and receive parts of the response message are omitted.)

(ASCII-BIN conversion not performed)



(ASCII-BIN conversion performed)



★One transmit transparent code and one transmit additional code and one receive transparent code and one receive additional code can be set in the QC24(N) to match the specifications of the external device.

*3 The QC24(N) processing order when data is transmitted and received using ASCII-BIN conversion and transparent code designation is shown below.

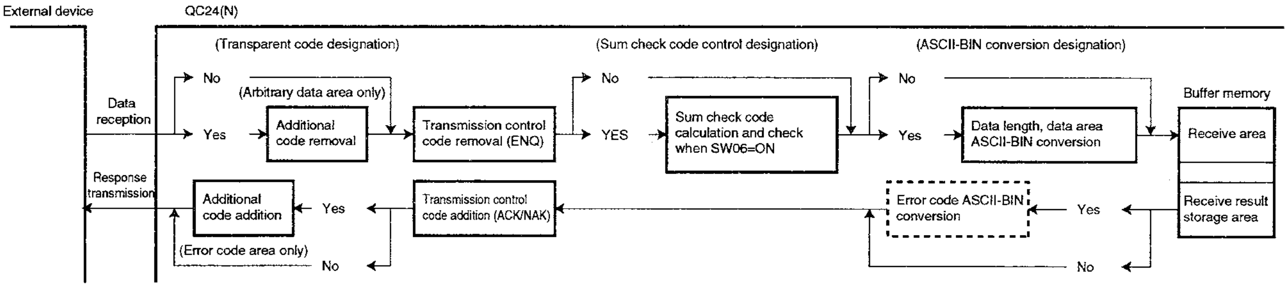
(Transmission and reception in QC24(N) message format)

1 Reception

① If receive transparent code is designated, the QC24(N) removes the additional code designation data from the arbitrary data area.

② The QC24(N) stores the arbitrary data area to the buffer memory receive area.
If ASCII-BIN conversion is designated, the QC24(N) converts the data to binary data before storing it to the buffer memory.

③ When the QC24(N) has received the number of data corresponding to the data length, it sends a request to the PLC CPU to read the receive data.
When QC24(N) transmission specifications switch SW06 is set to ON, the QC24(N) sends a receive data read request to the PLC CPU when the sum check code is received.

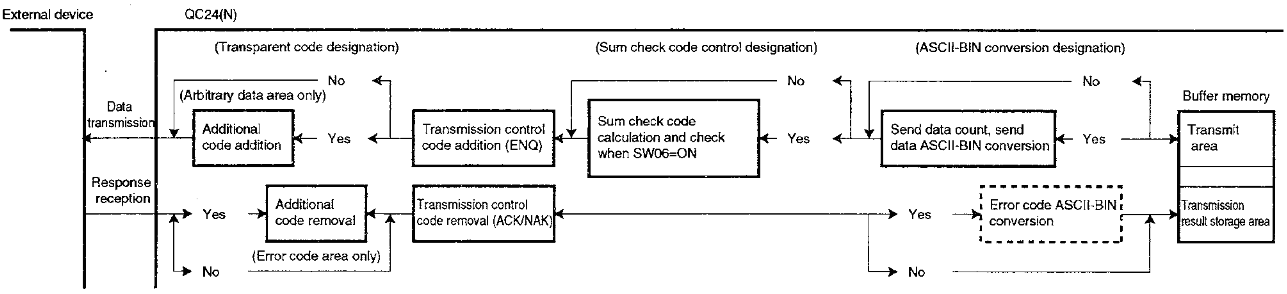


2 Transmission

① The QC24(N) adds the transmission control code data to the send data (arbitrary data area of transmit message) written to the buffer memory by the PLC CPU and transmits the send data to the external device.
If ASCII-BIN conversion is designated, the QC24(N) converts the send data to ASCII data before transmitting it to the external device.

② When QC24(N) transmission specifications SW06 is set to ON, the QC24(N) calculates the sum check code from the transmit message and adds it to the transmit message.

③ If transmit transparent code is designated, the QC24(N) adds the additional code data immediately before the transparent code/additional code data in the arbitrary data area and transmits the data to the external device.



POINT

The above is the QC24(N) transmission and reception processing sequence when the user frame transmit/receive function, ASCII-BIN conversion function, and transparent code designation transmit/receive function are used.
See it when selecting the transmit and receive methods when transmitting and receiving data to and from the external device.

12.3 Data Reception from External Device

This section describes the common information that you should know to use the PLC CPU to read the data received from an external device.

12.3.1 Data receive method

The following describes the method used by the QC24(N) to receive data from an external device. The QC24(N) reads the arbitrary data area of the message received from the external device from the receive area.

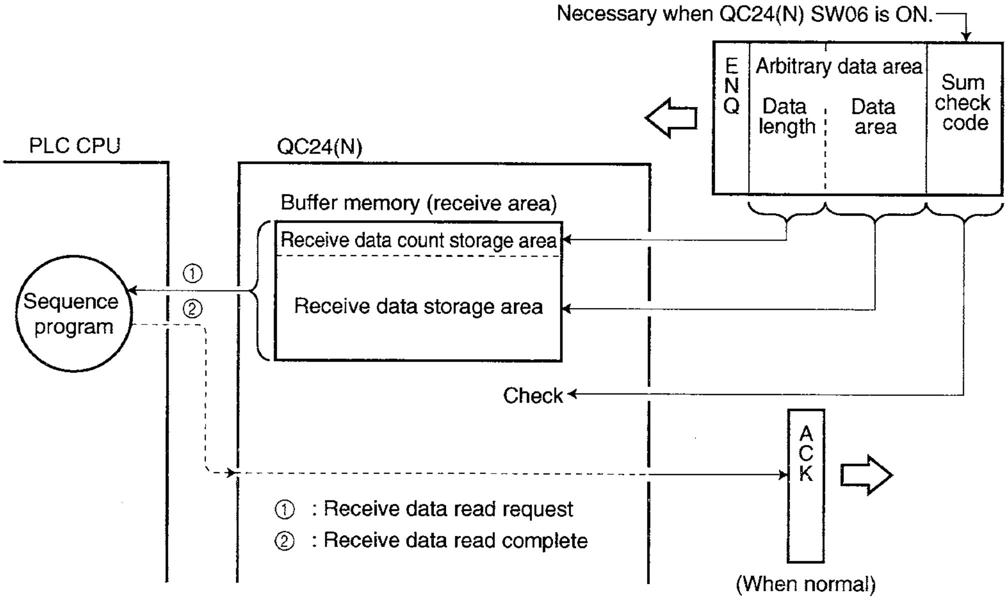
The following describes the data receive method when data is received in QC24(N) message format.

1 **The QC24(N) sends a receive data read request to the sequence program at the following times.**

- When QC24(N) transmission specifications switch SW06 is OFF
  When the QC24(N) receives a data area corresponding to the data length in the receive message, it sends a receive data read request to the sequence program.
- When QC24(N) transmission specifications switch SW06 is ON
  When the QC24(N) receives a data area corresponding to the data length in the receive message and the sum check code, it sends a receive data read request to the sequence program.

2 **The QC24(N) transmits a response message in reply to data reception to the external device at the following times.**

- If the sequence program has completed reading of the receive data, the QC24(N) transmits an ACK message to the external device.
- If the QC24(N) detected an error during data reception, it transmits a NAK message to the external device after the reception complete.

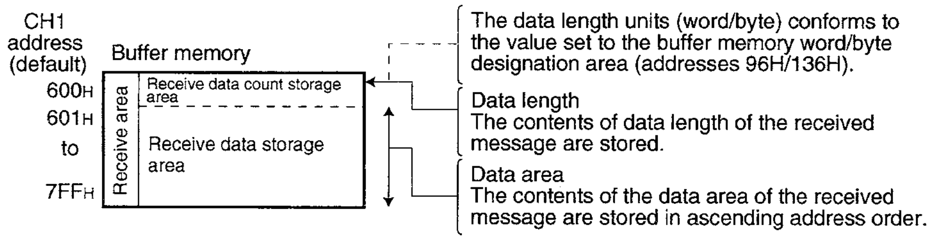


12.3.2 Receive area and receive data list

The following describes the QC24(N) buffer memory (receive area) that stores the data received from the external device and the data list when the arbitrary data area of the receive data is stored to the receive area.

1 Receive area

The receive area is a QC24(N) buffer memory area that stores the received data length and data area so that the PLC CPU can read the data received from an external device.
The data area is allocated buffer memory addresses 600H to 7FFH and A00H to BFFH as the default value.
The receive area can be changed to match the purpose of data transmission, specifications of the external device, and the length of the receive data.
(See Section 14.8.4 for a description of the modification method.)



POINTS

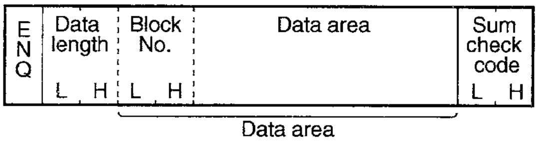
Make the data size per transmission from external device to QC24(N) the size of the QC24(N) receive data storage area, or less.

(Receive data storage area) ≥ (Data size of data area transmitted from external device)

If the external device must transmit data so large that it cannot all be stored in the receive data storage area, do one of the following.

① Receive area modification
The receive area address and size can be changed.

② Data split transmission
Split the data after the size of the receive data storage area and assign a block No. to the data area.
(Message structure example)



2 Receive data list

The following describes the list when the data received from the external device is stored to the receive area.

① The arbitrary data area (excluding the additional code data when receive transparent code is designated) of the received message is stored to the QC24(N) buffer memory (receive area).

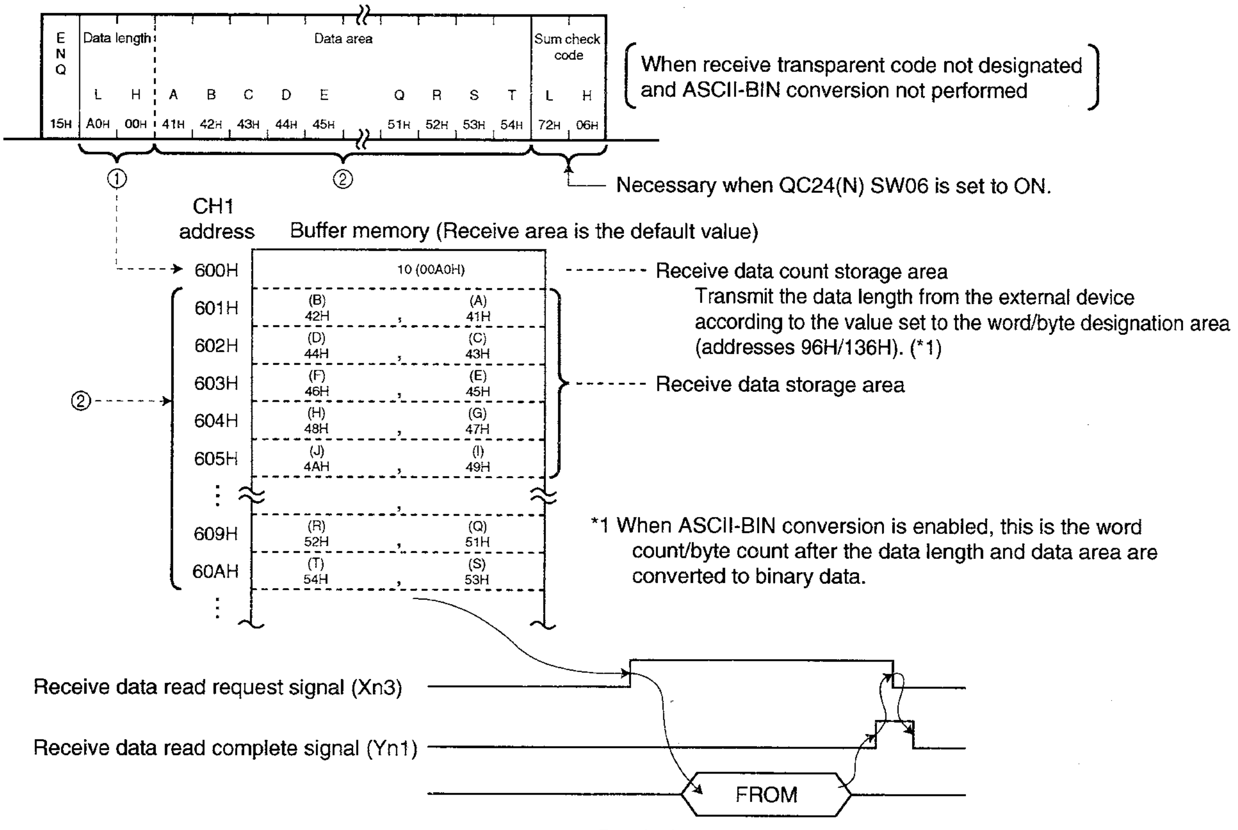
- Data length .... Receive data count storage area
- Data area .... Receive data storage area

② If the receive data is converted from ASCII to BIN data, the data converted to binary data is stored.

③ The data area of the received message is stored to the receive data storage area in low address (L) → (H), next address (L) → (H) order in the receive order.

(Example) Word/byte designation area setting .... Word units
Value of data length in receive message 10

In this case, when storing a 10-word data area, the QC24(N) sends a receive data read request to the PLC CPU.



When receive transparent code not designated and ASCII-BIN conversion not performed

Necessary when QC24(N) SW06 is set to ON.

Buffer memory (Receive area is the default value)

Receive data count storage area
Transmit the data length from the external device according to the value set to the word/byte designation area (addresses 96H/136H). (*1)

Receive data storage area

*1 When ASCII-BIN conversion is enabled, this is the word count/byte count after the data length and data area are converted to binary data.

Reads the receive data count and receive data from the buffer memory receive area.

POINT

The external device and PLC CPU must agree so that the units of the data length (word count/byte count) in the messages that are transmitted and received are the same.
The PLC CPU can be designated using the QC24(N) buffer memory word/byte designation area (addresses 96H/136H).

Notes

Receive data when the CD signal was turned OFF and the mode was switched
Note that if the following operations are performed while the QC24(N) is communicating with the external device, the receive data will be lost.

① When CD signal turned OFF
- If "Check CD terminal" was set when communicating with the external device through the RS-232C interface, when the QC24(N) CD signal was turned off (20 ms or longer) at the external device when the QC24(N) sent a read request to the PLC CPU, the receive data is cleared. (The receive area is not initialized.)
- If the CD signal was turned OFF when the QC24(N) sent a read request to the PLC CPU, the QC24(N) continues read request processing to the PLC CPU. (The receive data that the PLC CPU was requested to read are not cleared.)
  If the CD signal is turned on after the PLC CPU has completed reading the receive data, the QC24(N) sends an ACK message to the external device.
- To resume data transmission from the external device, turn ON the CD signal.

② When mode switched
- When the QC24(N) mode is forcefully switched as described in Section 18, the QC24(N) is placed into the power-on starting state and the receive data is cleared. (The receive data area is not initialized.)
- To transmit data thereafter, parameters must be set to the buffer memory special applications area.
- To resume data transmission from the external device, turn ON the QC24(N) ready signal (X (n+1) E) and resume data transmission after setting to the buffer memory special applications area is complete. (Depending on the data communications system, data transmission from the external device may have to be resumed after the PLC CPU informs the external device that it is ready to resume transmitting.)

12.3.3 Receive error detection

If the QC24(N) detects an error while receiving data from the external device, it performs the following processing.

① Ignores the data received up to that point. (Does not clear the memory receive area.)

② Sends a NAK message (response message) containing the error code showing the error contents to the external device after the data reception complete.

③ Lights one LED P/S to SIO, according to the contents of the detected error.

④ Turns on LED CH1 ERR. or CH2 ERR..

⑤ Stores the error code to the buffer memory data receive result area (addresses 258H/268H), according to the contents of the detected error.

⑥ Turns ON the CH☐ ERR. LED ON signal (input signal XnE/XnF) between the PLC CPU and QC24(N).

POINTS

See the following sections for a description of items ② to ⑥ above.
Contents and processing of the error codes of ② and ⑤ .... Section 22.1
PLC CPU error processing of ③ to ⑥ .... Section 19.1

12.3.4 Receive data clear

Data communications using the bidirectional protocol must be performed after a response message is received in reply to the preceding data transmission.
If the QC24(N) detects an error while receiving data, it sends an NAK message (response message) to the external device after the data reception complete and ignores the data being received when the error was detected.
Therefore, the receive data does not have to be cleared.

Note

When mode switching function was executed

- Note that if the mode switching function is executed during data communications, the QC24(N) will terminate the current processing and enter the start state.
- Execute the mode switching function as described in Chapter 18.

12.4 Data Transmission to External Device

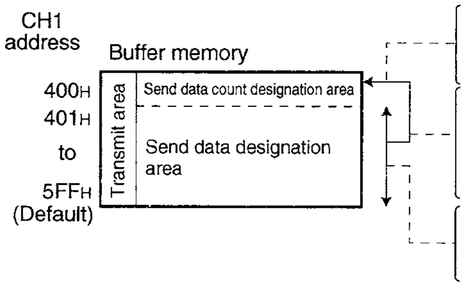
The following describes the common information you should know to transmit data to an external device.

12.4.1 Transmit area and send data designation and writing

The following describes the QC24(N) buffer memory (transmit area) to which the PLC CPU writes the data to be transmitted to the external device and the designation method when the send data is written to the transmit area.

1 **Transmit area**

The transmit area is the QC24(N) buffer memory area to which the PLC CPU writes the send data and send data count to transmit data to an external device.
The transmit area is allocated buffer memory addresses 400H to 5FFH and 800H to 9FFH as the default value.
The transmit area can be changed to match the purpose of data transmission, specifications of the external device, and the length of the send data. (See Section 14.8.1 for a description of the modification method.)



The send data count units (word/byte) conform to the value set to the buffer memory word/byte designation area (addresses 96H/136H).

Send data count
Use the TO instruction to designate the number of data you want to transmit.
The designated value is transmitted as the data length.

Send data
Sequentially stores the send data in ascending address order.

POINTS

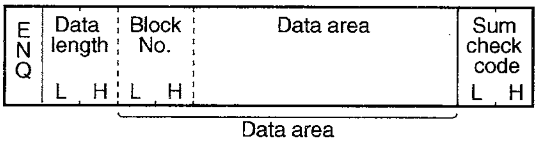
Make the size of the data part per transmission from PLC CPU to external device the size of the QC24(N) send data storage area, or less.

(Send data designation area) ≥ (Data size of data area to be transmitted from PLC CPU)

If the PLC CPU must transmit data so large that it cannot all be stored in the send data designation area, do one of the following.

① Send area modification
The send area address and size can be changed.

② Data split transmission
Transmit the data by splitting the data area after the send data designation area size and giving a block No. to the data area.
(Message structure example)



2 Send data designation and writing

The following outlines the designation and write methods when the PLC CPU writes the data to be transmitted to the external device to the transmit area.
The send data count and send data are written to the transmit area as shown below.

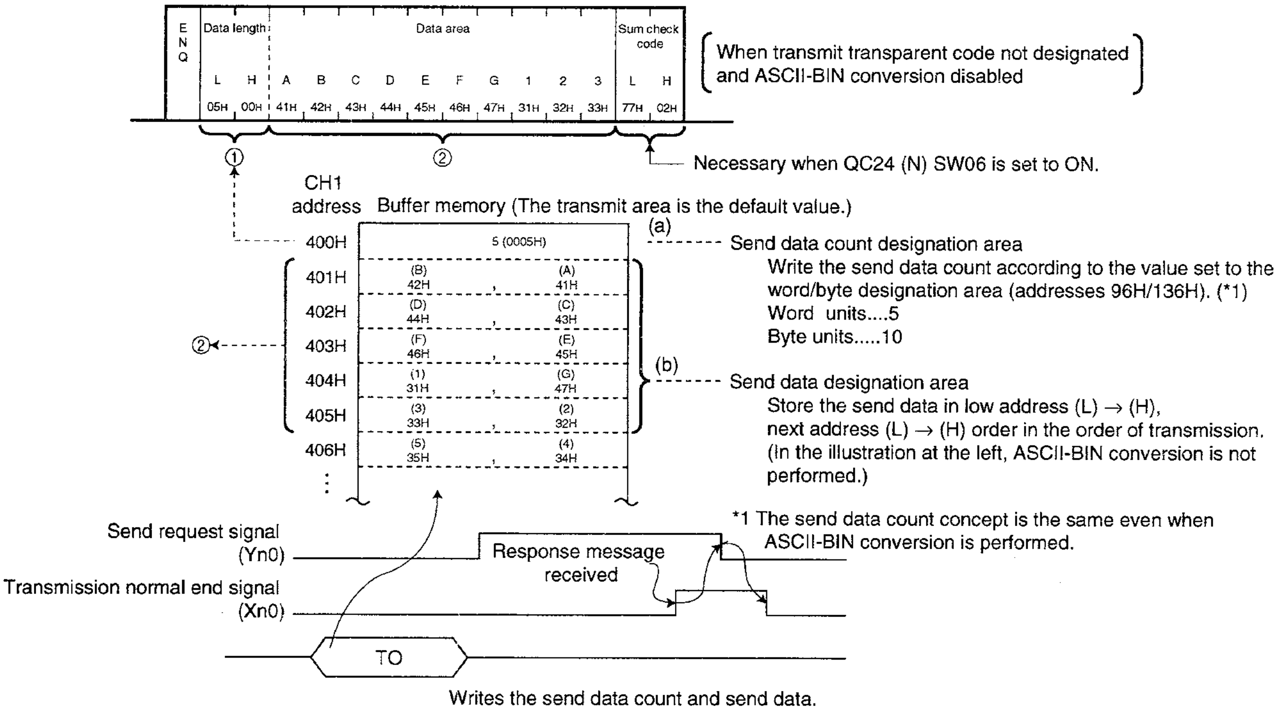
(a) The word count/byte count (by word/byte designation) of the data to be written to the send data designation area is written to the send data count designation area.

(b) The data to be transmitted is written to the send data designation area.

When the send request signal (Yn0/Yn7) is turned ON after executing (a) and (b) above, the QC24(N) sequentially transmits the designated number of the designated data from the low address of the send data designation area.

(Example) Word/byte designation area setting .... Word units
When transmitting .... "ABCDEFG123"

In this case, the QC24(N) completes transmission processing when it receives a response message from the external device after 5 words of data have been transmitted.



> **POINT**
>
> The external device and PLC CPU must agree so that the units of the data length (word count/byte count) in the messages to be transmitted and received are the same.
> The PLC CPU can be designated using the QC24(N) buffer memory word/byte designation area (addresses 96H/136H).

12.4.2 Transmission error detection

If the QC24(N) detects an error while transmitting data to an external device using the bidirectional protocol, it performs the following processing.

① Terminates transmission.

② Lights one of the LED C/N to SIO, according to the contents of the detected error.

③ Lights LED CH1 ERR. or CH2 ERR..

④ Stores the error code received from the external device, or the error code of the detected error contents, to the buffer memory data transmission result storage area (addresses 257H/267H) and turns ON the transmission abnormal end signal (input signal Xn1/Xn8).

* For message transmission, the QC24 also turns ON the transmission abnormal end signal when NAK+error code could not be received normally from the external device.

⑤ Turns on the CH☐ ERR. LED ON signal (input signal XnE/XnF) between PLC CPU and QC24(N).

POINT

See the following sections for a description of items ② to ⑤ above.
Contents and processing of error code of ④ .... Section 22.1
PLC CPU error processing of ② to ⑤ .... Section 19.1

12.5 Processing when Simultaneous Transmission Performed During Full-Duplex Communications

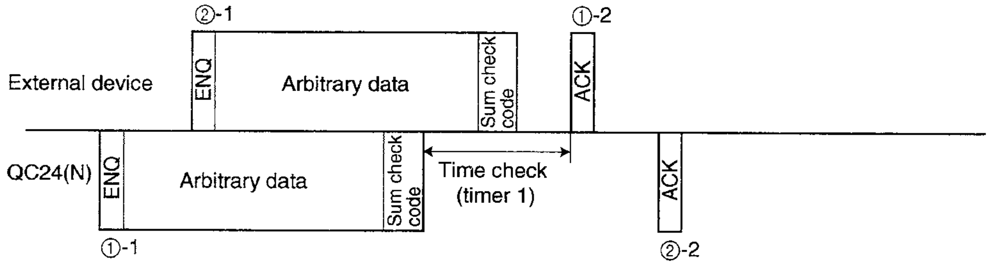
This section describes the processing performed by the QC24(N) when the external device and QC24(N) transmit at the same time during data communications using the bidirectional protocol.
Since the external device and QC24(N) do not transmit at the same time during half-duplex communications when communicating as described in Section 14.5, this section does not have to be read.

When an external device and the QC24(N) transmit at the same time, QC24(N) processing depends on the value set to the QC24(N) buffer memory "simultaneous transmission designation area" (addresses 9BH/13BH).
The following uses communications in QC24(N) message format as an example to describe the contents of QC24(N) processing for each setting contents.

Value set to buffer memory [Addresses 9BH/13BH]	Setting contents	QC24(N) processing	
		Message transmit processing	Message receive processing
0000H	Send data : Valid Receive data: Valid	Waits to receive the response message (①-2) while checking time-out after data transmission (①-1) is complete. Posts normal end or abnormal end according to whether or not the sequence program received a response message through the buffer memory.	Transmits a response message (②-2) at the end of after data reception (②-1). Posts the receive data and receive result to the sequence program through the buffer memory.
0100H	Send data : Invalid Receive data: Invalid	Posts a simultaneous transmission error to the sequence program through the buffer memory at the end of data transmission (①-1). Does not wait for a response message (①-2) in reply to data transmission (①-1).	Transmits a response message (②-2) at the end of data reception (②-1). Posts the receive data and receive result to the sequence program through the buffer memory.
0001H	Send data : Valid Receive data: Invalid	Waits to receive a response message (①-2) while checking time-out at the end of data transmission (①-1). Posts normal end or abnormal end according to whether or not the sequence program received a response message through the buffer memory.	Ignores data reception (②-1) and discards the received data. Does not transmit a response message (②-2). Does not inform the sequence program that data was received.
0101H	Send data : Invalid Receive data: Invalid	Posts a simultaneous transmission error to the sequence program through the buffer memory at the end of data transmission (①-1). Does not wait to receive a response message (①-2) in reply to data transmission (①-1).	Ignores data reception (②-1) and discards the receive data. Does not transmit a response message (②-2). Does not inform the sequence program that data was received.

(ⓝ-m) is the number showing the correspondence with the messages in the illustration shown below.

1 **Transmission: valid, reception: valid**

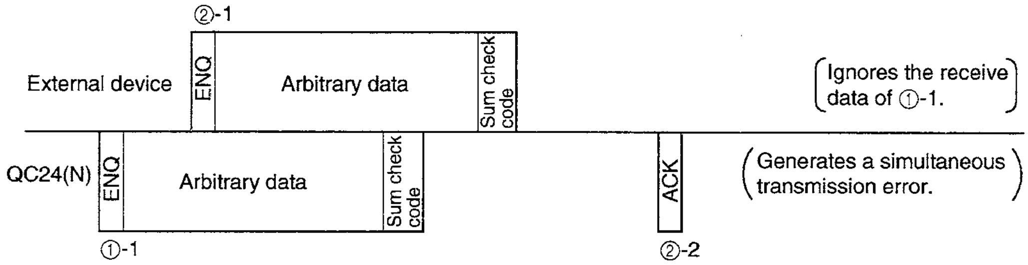


POINT

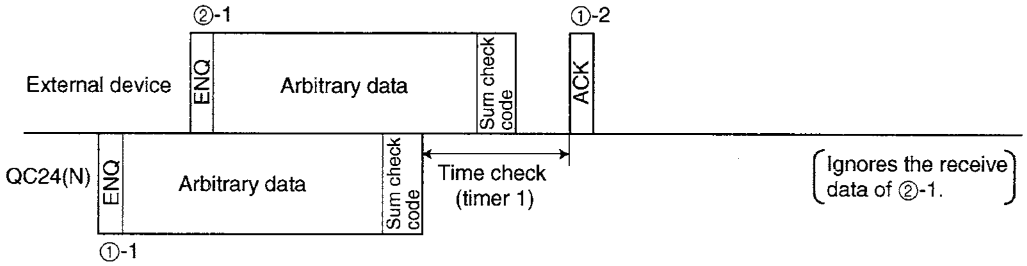
When the entire message of ②-1 was received while transmitting the message of ①-1 in the illustration.

- The QC24(N) outputs the receive data read request signal of ②-1 to the PLC CPU after transmitting ①-1. (Turns ON the Xn3/XnA signal.)

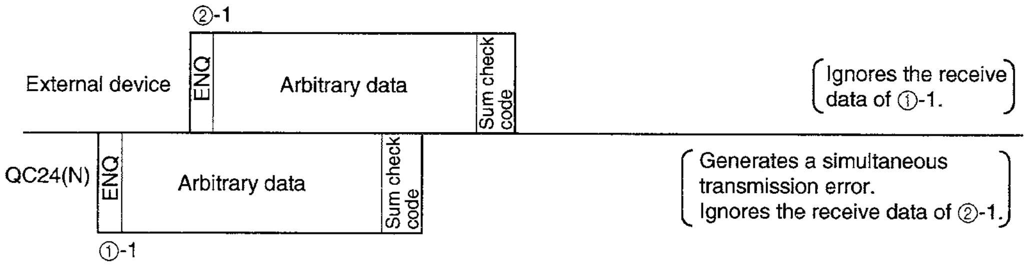
2 Transmission: invalid, reception: valid



3 Transmission: valid, reception: invalid



4 Transmission: invalid, reception: invalid



Note

Section 14.7 describes time-check timer 1 (response watchdog timer) shown in the illustration.

POINTS

When the transmission control described in Section 14.3 is used, and the buffer memory simultaneous transmission data valid/invalid designation area (addresses 9BH/13BH) designates that the receive data is valid, the QC24(N) performs message transmission and message reception processing as described below.

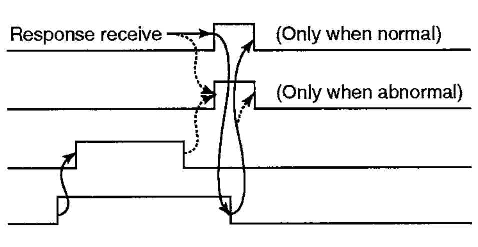
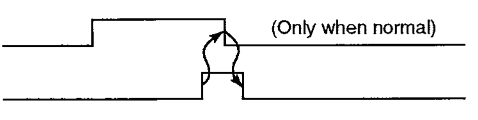
During message transmission processing, time check by timer 1 (response watchdog timer) is performed.

① Message transmission (①-1 in the illustration)
  - If the QC24(N) receives a terminate transmission request (DC3 received/DSR signal OFF) from the external device during message transmission, it terminates data transmission.
  - When the QC24(N) receives the ready to send signal (DC1 received/DSR signal ON), it restarts data transmission.

② Message reception
  - If the QC24(N) cannot send a response message to the external device in response to message reception because the external device issued a terminate transmission request (DC3 received/DSR signal OFF), it transmits the response message after it receives the ready to send signal (DC1 received/DSR signal ON) from the external device.

12.6 I/O Signals for Handshake with PLC CPU

The signals that transmit the data output from the sequence program to the external device, or detect that data has arrived from the external device and enables reading of the data by the sequence program, when the bidirectional protocol is used to transmit and receive data are called I/O signals for handshake. These signals are necessary with the bidirectional protocol.
The I/O signals for handshake are shown below.

	I/O signal		Signal name	Device turned ON/OFF		Timing
	CH1	CH2		CPU	QC24(N)	
Transmission	Xn0	Xn7	Transmission normal end		○	
	Xn1	Xn8	Transmission abnormal end		○	
	Xn2	Xn9	Transmitting		○	
	Yn0	Yn7	Send request	○		
Reception	Xn3	XnA	Receive data read request		○	
	Yn1	Yn8	Receive data read complete	○		

POINT

If the transmission abnormal end signal (Xn1/Xn8) was turned on, read the error code from the buffer memory shown below and check the error contents and take the action described in Section 22.1.

- Transmission abnormal end signal (Xn1/Xn8) turned on
  Read the data transmission result storage area (addresses 257H/267H).

Notes

The following I/O signals can also be used with the bidirectional protocol, in addition to the signals shown above.
See Sections 3.4 and 19.1.3 for a description of the PLC CPU I/O signals.

- CH1 ERR. LED ON signal (XnE) .... Turned ON when an error is generated in the CH1 interface
- CH1 ERR. LED ON signal (XnF) .... Turned ON when an error is generated in the CH2 interface
- QC24(N) ready signal (X (n+1) E) .... Turned ON when the QC24(N) can be accessed from the PLC CPU
- Watchdog timer error signal (X (n+1) F) ...... Turned ON when the QC24(N) cannot operate normally
- CH1 ERR. LED OFF request signal (YnE) ... Turned ON when the QC24(N) issues a request to turn off the CH1 ERR. LED
- CH2 ERR. LED OFF request signal (YnF) ... Turned ON when the QC24(N) issues a request to turn off the CH2 ERR. LED

12.7 Buffer Memory Read/Write

The following describes reading and writing of the QC24(N) buffer memory during data communications using the bidirectional protocol.
Program the sequence program of the necessary part.

12.7.1 Initialization to buffer memory special applications area

When the QC24(N) starts, the QC24(N) default values, or the default values registered to the EEPROM by the user, are written to the buffer memory special applications area.
Data communications with an external device using the QC24(N) default values is possible. However, the default values may have to be changed, depending on the specifications of the external device.
The following shows the setting items, reference section, and initialization examples when the QC24 buffer memory special applications area default values must be changed to use the bidirectional protocol to communicate data.

	Read/write contents that must be programmed	**QC24 default value**	**Reference section**
①	Using the RS-232C interface for data communications and enabling QC24(N) CD terminal check.	Not checked	4.7.2 $\boxed{3}$
②	Using DC code to control transmission with external devices.	DTR/DSR control	14.3
③	Setting the units of the data length to be transmitted and received to byte units.	Word units	14.4
④	Using half-duplex communications to carry out data communications through the RS-232C interface.	Full-duplex communications	14.5
⑤	Changing handling of the QC24(N) transmit and receive messages during simultaneous transmission.	Transmission valid Reception valid	14.6
⑥	Monitoring the receiving interval (timer 0) with the QC24(N) during data reception from an external device.	0 (Unlimited wait)	14.7
⑦	Monitoring the response watchdog time (timer 1) up to the start of transmission and reception of the response message with the QC24(N) during transmission and reception of the response message in reply to message transmission.	5 seconds	
⑧	Monitoring the time (timer 2) from the start of transmission to the end of transmission with the QC24(N) during data transmission to an external device.	3 minutes	
⑨	Changing the transmit area that stores the data to be transmitted to the external device.	400H to 5FFH 800H to 9FFH	14.8
⑩	Changing the receive area that stores the data received from the external device (Area from which the PLC CPU reads the receive data.).	600H to 7FFH A00H to BFFH	
⑪	Handling the external device transmission control 1-byte data as user data. (Transmit transparent code designation, receive transparent code designation).	None	14.10
⑫	ASCII-BIN conversion of send and receive data.	Disabled	14.11

POINTS

(1) When changing a default value, write the new value during QC24(N) starting (QC24(N) ready signal X (n+1) E = ON).

(2) If a buffer memory special applications area set value was changed, it is recommended that the special applications area set value be registered to the QC24(N) EEPROM and used as the default value during QC24(N) starting after checking that subsequent data transmission and reception are performed normally.

* Using the value registered to the EEPROM as the default value eliminates the need for a sequence program for the part whose set value was changed.

(3) See Section 14.1 and Chapter 15 for a description of the following.
- Areas that can be registered to EEPROM
- Registration to EEPROM
- Initialization of set value to buffer memory (return to QC24(N) default value)

(Example of initialization to buffer memory special applications area)

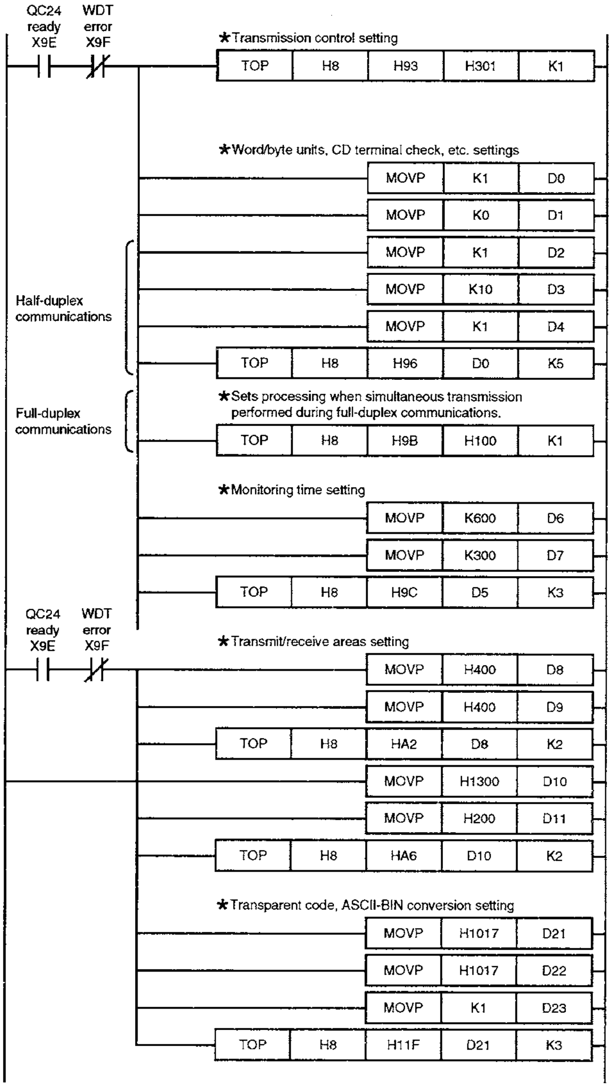
A sample program that changes the QC24(N) buffer memory special applications area default values is shown below.

Program the of the necessary parts.

This example shows the settings for the CH1 interface.

Designation Example

(QC24(N) I/O signals 80H to 9FH)



Uses the DC codes to control transmission and enables all DC control.
The DC codes use the default values.
See Section 14.3.

Handles the send and receive data in byte units.

Sets CD terminal check.

Sets the RS-232C I/F communication method to half-duplex communications.

Sets nonpriority during simultaneous transmission. (Transmission wait time 1000ms)

Sets retransmission at resumption of transmission.

See Sections 4.7.2 [3] and 14.4 to 14.5.

Sets send data: invalid, receive data: valid.
See Section 14.6.

Sets the response watchdog timer (timer 1) to 1 minute.

Sets the transmit watchdog timer (timer 2) to 30 seconds.

See Section 14.7.

Makes addresses 400H to 7FFH the transmit area.

Makes addresses 1300H to 14FFH the receive area.

See Section 14.8.

Sets the transmit transparent code to 17H (ETB) and the additional code to 10H (DLE)
Sets the receive transparent code to 17H (ETB) and the additional code to 10H (DLE)
Enables ASCII-BIN conversion of the data to be transmitted and received.
See Sections 14.10 and 14.11.

12.7.2 Reading and writing of buffer memory during data communications

The following describes the contents and reference sections when the QC24(N) buffer memory is read and written after the QC24(N) is started.

	Read/write contents that must be programmed	Reference section
①	Performing data communications in QC24(N) message format	Chapter 13
②	Registering the data communications parameters to the QC24(N) EEPROM	Chapter 15
③	Registering data communications user frames to EEPROM, etc.	Chapter 16
④	Switching the QC24(N) interface used with the bidirectional protocol to another protocol	Chapter 18
⑤	Reading the QC24(N) LED on status and turning off the LED	Chapter 19
⑥	Reading the QC24(N) module status, signal status, and switch setting status	
⑦	Checking the error contents when the CH1 ERR. LED or CH2 ERR. LED is turned on	
	Checking the results of data transmission and reception	Chapter 13

POINT

Write a sequence program that writes and reads the buffer memory for only the contents performed by the user from among the contents listed above.

$\boxed{1}$ **Data transmission result storage area (addresses 257H/267H)**

Data receive result storage area (addresses 258H/268H)

- If the QC24(N) detects an error during data transmission, the error code is stored to the data transmission result storage area.
- If the QC24(N) detects an error during data reception, the error code is stored to the data receive result storage area.
- If an error code was stored, the input signal to the PLC CPU shown below and the QC24(N) CH□ ERR. LED are turned on.
  When an error was generated, the LED can be turned off and the error code can be cleared as described in Section 19.1.3 $\boxed{3}$.

  Data transmission .....Transmission abnormal end signal (Xn1, Xn8)
- See Section 22.1 for the error code contents and processing.

		b15 to b0	
Buffer memory address	257H	0 to n	(CH1 transmission result)
	258H	0 to n	(CH1 receive result)
	267H	0 to n	(CH2 transmission result)
	268H	0 to n	(CH2 receive result)

0 : Normal end
Nonzero : Abnormal end

2 Transmit area

The following describes the application of the buffer memory used when the PLC CPU writes the data to be transmitted to the external device (arbitrary data area in message).

POINT

Section 12.4.1 and Chapter 13 give a general description and details of the transmit area storage value and writing to the transmit area.

① Send data count designation area (Default: Addresses 400H/800H)

- The number of data (corresponding to the byte count/word count, data length in the message) to be transmitted to the external device is written to this area.
- The data count units are set to the word/byte designation area (addresses 96H/136H).

② Send data designation area (Default: Addresses 401H to 5FFH/801H to 9FFH)

- The data to be transmitted to the external device (corresponds to the data area in the message) is written to this area.
- The data size (data count) to be transmitted is designated by the send data count storage area.

3 Receive area

The following describes the application of the buffer memory used when the PLC CPU reads the data received from an external device (data area in the message).

POINT

Section 12.3.2 and Chapter 13 give a general description and details of the receive area storage value and reading of the receive area.

① Receive data count storage area (Default: Address 600H/A00H)

- The data length in the message received from the external device is stored to this area.
  (Data count (byte count/word count) when the QC24(N) reads the data area of the receive message to the PLC CPU.)
- The data count units are set to the word/byte designation area (addresses 96H/136H).

② Receive data storage area (Default: Addresses 601H to 7FFH/A01H to BFFH)

- The data area of the message received from the external device is stored to this area.
- The data size (data count) when the receive data is read to the PLC CPU is stored to the receive data count storage area.

12.8 Data Communications Precautions

The following describes the precautions to be observed when performing data communications using the bidirectional protocol.

1 **QC24(N) transmission sequence initialization conditions**

The QC24(N) transmission sequence is initialized in the following cases.

- When the power is turned on, the reset switch on the CPU is operated, or the mode is switched
- When a response message (ACK, NAK, etc.) was received in reply to data transmission
- When a response message (ACK, NAK, etc.) was transmitted in reply to data reception
- When the CD signal was turned OFF during data communications using "Check CD terminal" (see Section 4.7.2 3) in full duplex communications through the RS-232C interface

2 **Procedure when transmitting data from external device or QC24(N)**

Wait until reception of a response message in reply to the preceding data transmission before transmitting more data from an external device or QC24(N).

3 **Data length and data area to be transmitted and received**

The external device and PLC CPU must agree so that the units of the data length (word count/ byte count) in the message to be transmitted and received is the same.
The PLC CPU units can be designated using the QC24(N) buffer memory word/byte designation area (addresses 96H/136H).
Make the length of the data area in the message to be transmitted and received the size of the QC24(N) buffer memory send data designation area and receive data storage area, or less.

4 **NAK code response**

① Response from QC24(N) to external device

After the error detection message reception complete, it transmits the NAK code to the external device.

② Response from external device to QC24(N)

Transmit the error code (22H to 5FH) immediately after the NAK response.

POINTS

(1) Perform error processing according to the error code received immediately after the NAK message at the device that received NAK as the response message after data transmission. Section 22.1 describes the error codes that are transmitted from the QC24(N).

(2) If the QC24(N) receives a NAK response while transmitting data to an external device, it completes data transmission, then reads the NAK, writes the error code to buffer memory, and turns ON the transmission abnormal end signal (Xn1/Xn8).

(3) If the QC24(N) detects an error while receiving data, it ignores the receive data corresponding to the data length.
If the data length is abnormal, the QC24(N) ignores all the data up to the receive message head data (ENQ, etc.) received thereafter.

5 External device time-out check

When checking time-out up to reception of the response message at the external device during data transmission from external device to QC24(N), make the time-out time the time shown below, or longer.
(PLC CPU maximum scan time × 2) + 100 ms

6 External device framing error

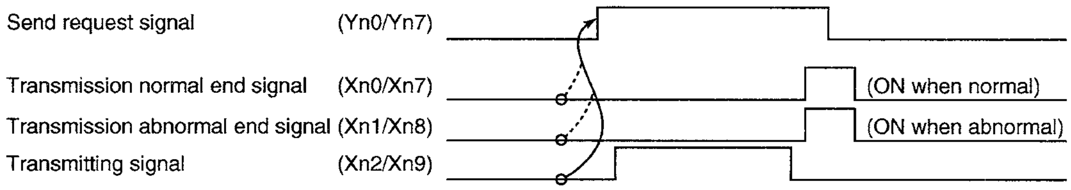
If the QC24(N) places the external device into the Ready to Send state QC24(N) through the RS-422 or RS-422/485 interface, the external device may generate a framing error.
Make the external device skip the data up to transmission of the head data (ENQ, NAK, etc.) of the message from the QC24(N).
Before communicating data through the RS-422 or RS-422/485 interface, check the QC24(N) specifications given in Section 3.3.3.

7 Data bit setting

When QC24(N) transmission specifications switch SW06 is set to ON and a sum check code is added to the message, make the data bit setting 8 bits.
See Section 4.3.2 for a description of data bit setting.

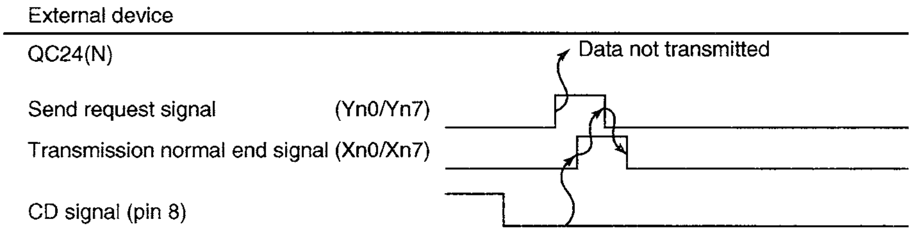
8 Items prohibited when transmitting data from PLC CPU to external device

(a) Issue a send request (Yn0/Yn7: ON) from the PLC CPU to the external device when the following input signals are OFF.

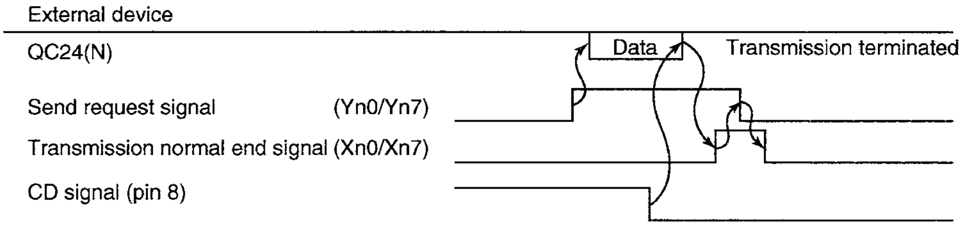


* The QC24(N) accepts send requests from the PLC CPU when the send request signal (Yn0/Yn7) is turned on while the signals shown above are OFF.

(b) When setting [Check CD terminal] in the QC24(N) while using the QC24(N) RS-232C interface, do not turn OFF the QC24(N) CD signal when the external device is ready to receive data.
([Check CD terminal] is set in buffer memory addresses 97H/137H.)
If the CD signal is turned OFF at the start of data transmission, the QC24(N) will turn ON the transmission normal end signal (Xn0/Xn7) instead of transmitting data.



If the CD signal is turned OFF during data transmission, the QC24(N) terminates data transmission and turns ON the transmission normal end signal (Xn0/Xn7).



(c) If the send request signal (Yn0/Yn7) was turned ON, do not turn it OFF until one of the transmission complete signals (Xn0, Xn1/Xn7, or Xn8) is turned ON.

MEMO

13. DATA COMMUNICATIONS USING QC24(N) MESSAGE FORMAT

This section describes the data transmission and reception methods and procedures when an external device and the PLC CPU exchange data in QC24(N) message format.

This section describes data communications with external devices under the following conditions.

① QC24(N) I/O signals

QC24(N) installed at QnACPU I/O signal addresses 80H to 9FH.

② QC24(N) interface used in data communications with external devices

QC24(N) CH1 RS-232C interface

③ CH1 buffer memory special applications area initialization contents for data communications in QC24(N) message format

The QC24(N) defaults of the areas shown below depend on the contents of the description.
In any case, the contents change when the QC24(N) starts (QC24(N) ready signal X (n+1) E = ON).
Areas other than those shown below use the QC24(N) default values.

Address	Name	Initialization contents	Reference section
96H	Word/byte designation area	Word units	Section 14.4
11FH	Transmission transparent code designation	Not designated	Section 14.10
120H	Receive transparent code designation	Not designated	
121H	ASCII-BIN conversion designation	Disabled	Section 14.11

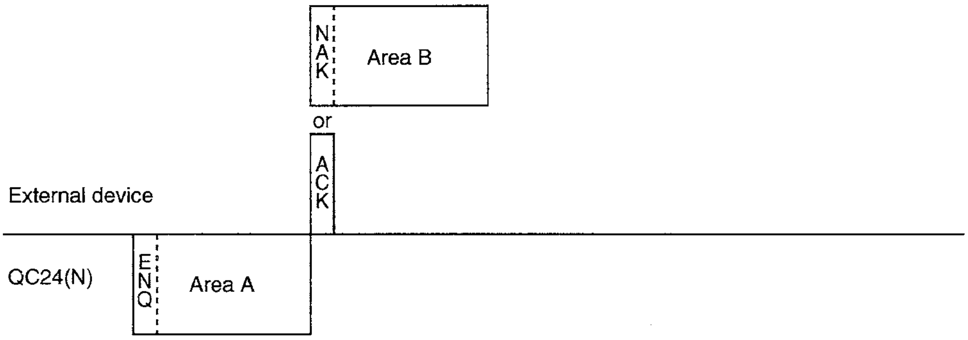
13.1 Bidirectional Protocol Basic Format

The following describes the contents of the bidirectional protocol, control procedure and of each item designated by the control procedure.

13.1.1 Control procedure basics

The following describes the basics of the control procedures described from Section 13.1.2.

1 **Transmitting data from QC24(N) to external device**

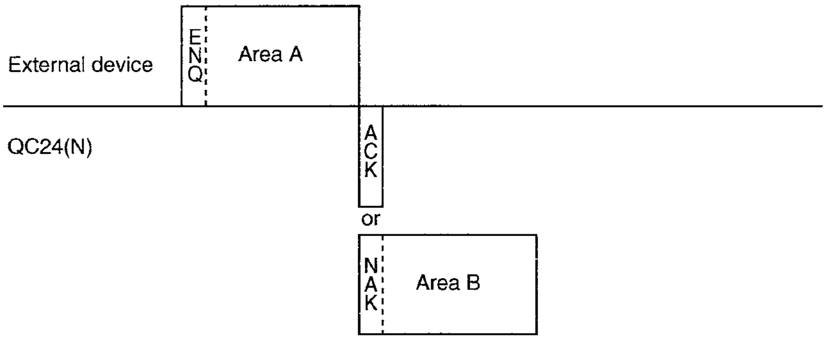


① Area A indicates transmission from QC24(N) to external device.

② Area B indicates transmission from external device to QC24(N).

③ The program sequentially transmits the data from left to right.
(Example: Area A data is sequentially transmitted to the right, beginning from ENQ.)

2 **Transmitting from external device to QC24(N)**



① Area A indicates transmission from external device to QC24(N).

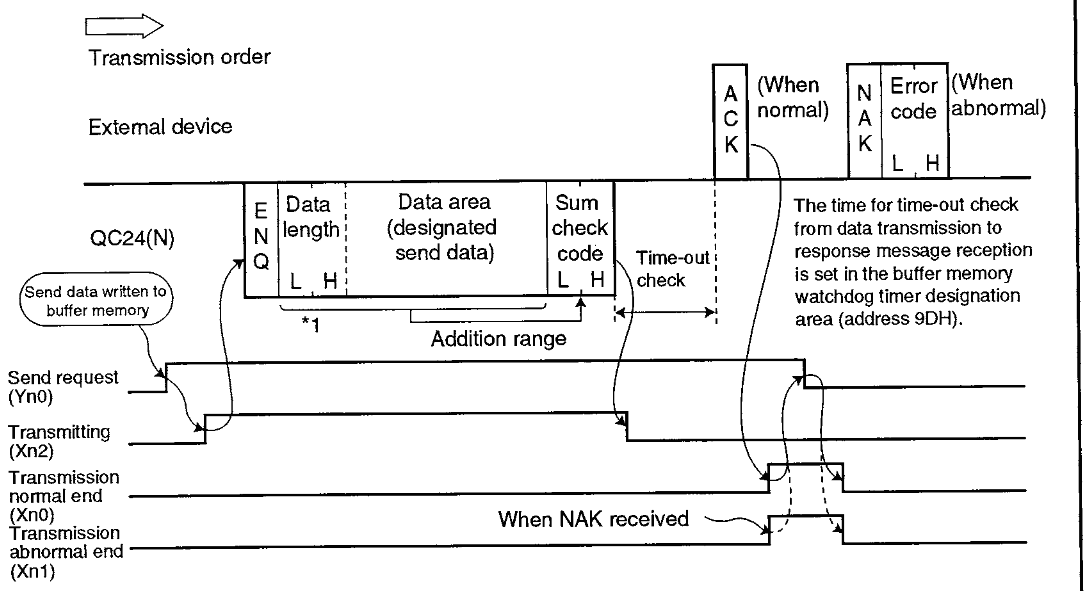
② Area B indicates transmission from QC24(N) to external device.

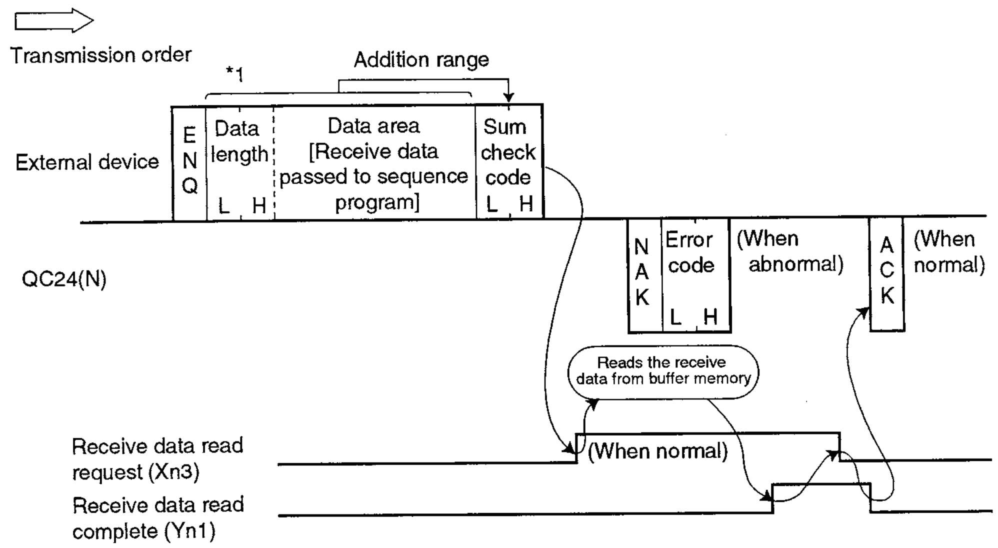
③ The program sequentially transmits the data from left to right.
(Example: The area A data is sequentially transmitted to the right, beginning from ENQ.)

13.1.2 Control procedure

The following describes the basic format for data communications in QC24(N) message format.

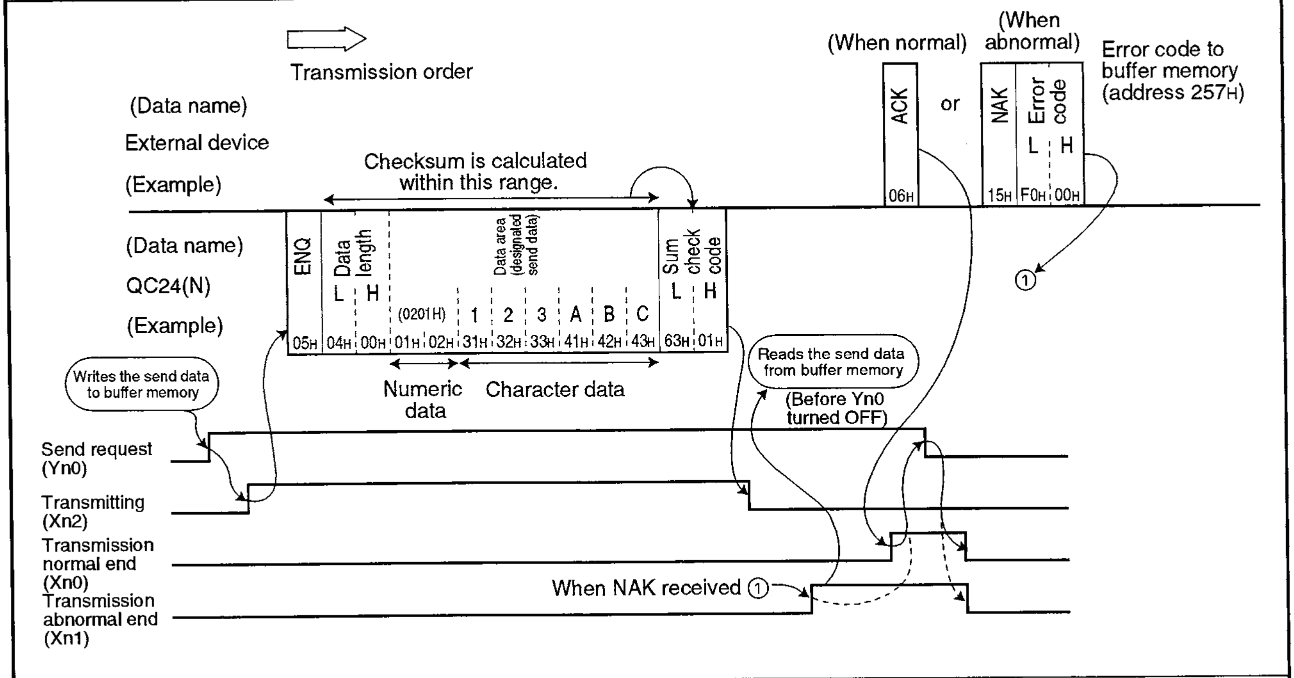
(Control procedure format)

<table>
<tr><th>Contents</th><th>Control procedure (Protocol)</th></tr>
<tr><td>Data transmission to external device</td><td>


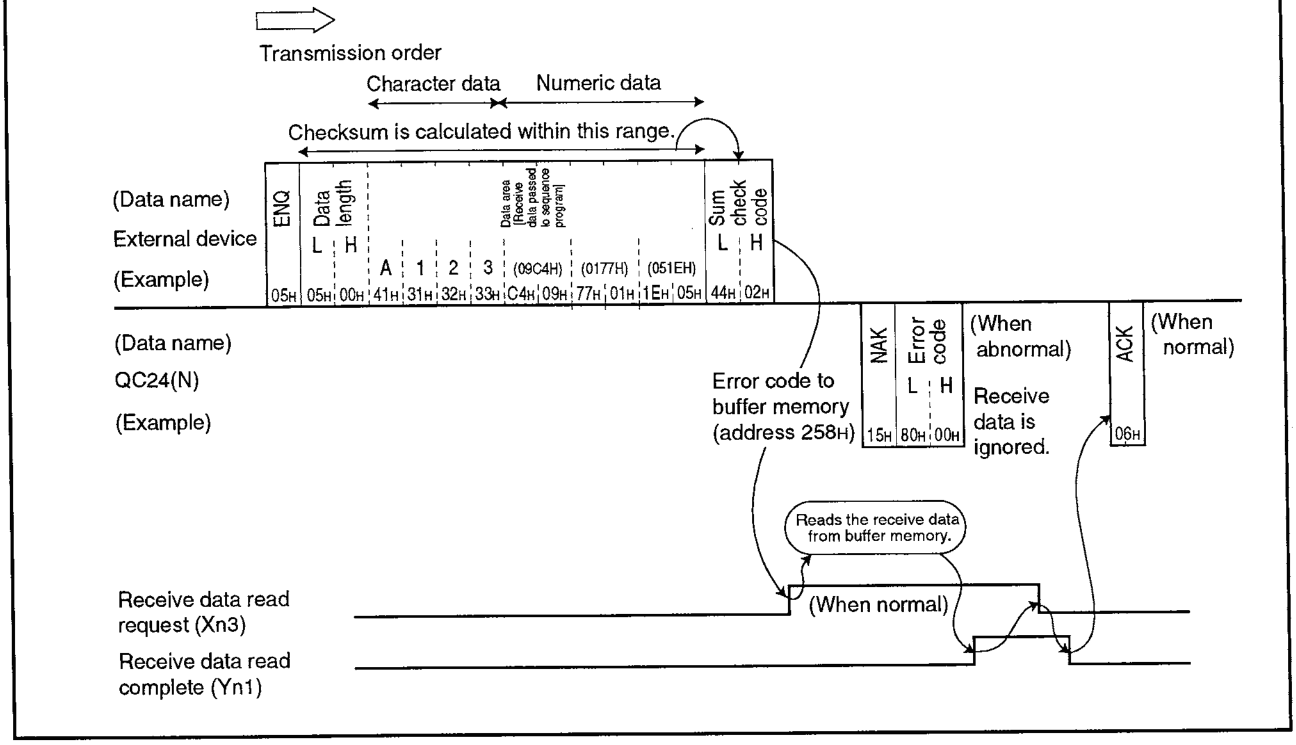
</td></tr>
<tr><td>Reception of data from external device</td><td>


</td></tr>
<tr><td>Notes</td><td>
(1) Sum check is calculated only when [Sum check] (QC24(N) switch (SW06): ON) is set. When [No sum check] is set, sum check is not calculated.
(2) When [Sum check] is set, sum check is calculated only for the data of the part indicated by *1 in the illustration above.
(3) If the QC24(N) detects an error during data reception, it responds with NAK after the data reception complete either full-duplex communication or half-duplex communication. If the QC24(N) detects an error during data reception, it ignores the receive data (see Section 12.3.3) and does not send a receive data read request to the PLC CPU. (Receive error detection signal Xn4, XnB is not turned ON.)
</td></tr>
</table>

Designation Example When the data length units is word units.



Designation Example When data length units are word units.



13.1.3 Contents of data designation items

The following describes the contents of each data designated in the messages transmitted and received between an external device and the QC24(N).

POINTS

(1) 1 to 5 of this section describe the contents when ASCII-BIN conversion disabled and transmit transparent code and receive transparent code not handled are designated by the following.

- Transmit transparent code designation (buffer memory address: 11FH)
- Receive transparent code designation (buffer memory address: 120H)
- ASCII-BIN conversion designation (buffer memory address: 121H)

(2) 6 of this section describes the contents when ASCII-BIN conversion is performed.

(3) 7 of this section describes the contents when data is transmitted and received by designating the transparent code and additional code.

1 Control code

The table below shows the control codes.

Signal name	Code (Hexadecimal)	Contents	Application
ENQ	05H	Enquiry	Starts data transmission.
ACK	06H	Acknowledge	Response to the opposite device when data was received normally.
NAK	15H	Negative Acknowledge	Response to the opposite device when data could not be received normally. (Immediately followed by an error code.)

① QC24(N) → external device
The QC24(N) adds the control code to be transmitted.

② QC24(N) ← external device
The QC24(N) checks and processes the received control code. The control code cannot be read from the sequence program.

2 Data length

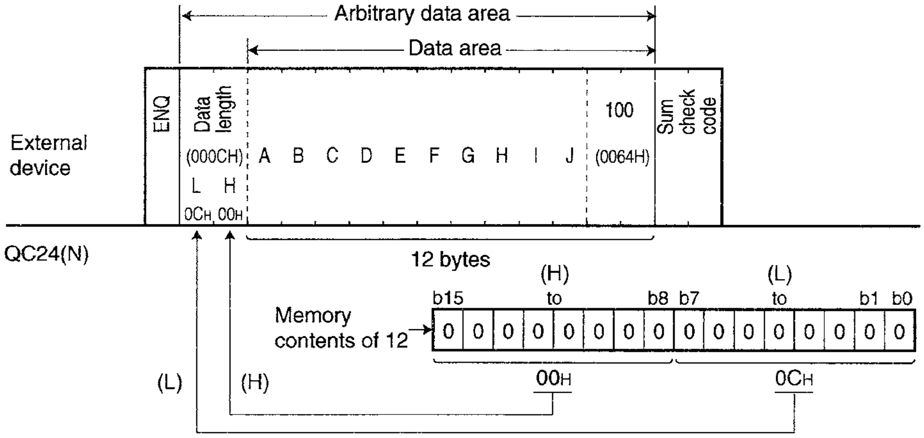
Represents the number of bytes, or number of words, of the data area in the message. The data length units (word/byte) are determined by the contents set to buffer memory address 96H (word/byte designation area).

① QC24(N) → external device
The transmit data length is the value written to the buffer memory send data count designation area by the sequence program by TO instruction.
The QC24(N) transmits this value unchanged, beginning from the lower byte (L).

② QC24(N) ← external device
The QC24(N) checks the received data length. If the received data length is normal, the QC24(N) stores it unchanged to the buffer memory receive data count storage area, with the first byte as the lower byte (L).

The example below shows the data length contents.

(Example) The data length when "ABCDEFGHIJ" and the number 100 are transmitted as data is shown below. (Units: Bytes)



3 Data area

This is the 1 byte of data to be transmitted to the opposite device. Data codes 00H to FFH are handled.

① QC24(N) → external device

The data area to be transmitted are the contents written to the buffer memory send data designation area by the sequence program by TO instruction.

The QC24(N) transmits data of the size designated by the send data count designation area unchanged, beginning from the low address of the send data designation area, according to the value set to the buffer memory word/byte designation area.

② QC24(N) ← external device

If the received data area is normal, the QC24(N) sequentially stores it unchanged to the receive data storage area, beginning from the low address.

The data length data in the message (see 2) and the value set to the buffer memory word/byte designation area determine the storage size.

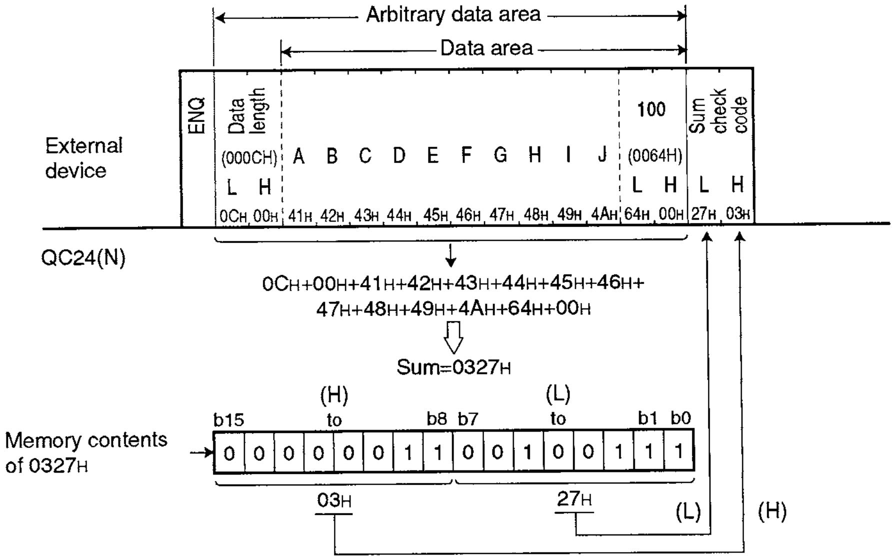
4 Sum check code

The sum check code represents the value of the lower 2 bytes (16 bits) of the result of addition of the message data length data and data area as binary data.
If QC24(N) transmission specifications switch SW06 is set to ON, the sum check code must be added to the end of the message.

① QC24(N)→external device
The QC24(N) calculates and adds the sum check code to be transmitted.
When the sum check code is not handled, it is not transmitted.

② QC24(N)←external device
The QC24(N) checks and processes the received sum check code.
The sequence program cannot read the sum check code.
If the sum check code is not handled, when a the QC24(N) receives a data area corresponding to the message data length data, it ignores the receive data up to next control code (see 1).
The example below shows the contents of the sum check code in the message.

(Example) The sum check code when "ABCDEFGHIJ" and the number 100 are transmitted as data is shown below. (Units: Bytes)



5 Error code

The error code shows the error contents when the opposite device responds with NAK. (See Section 22.1 for a detailed description of the error codes.)

① QC24(N) → external device
The QC24(N) adds one of the error codes shown in Section 22.1.
If an error code was transmitted, the QC24(N) writes it to the buffer memory data receive result storage area (address: 258H).

② QC24(N) ← external device
Transmit the user-determined error code from the external device.
As the error codes, 0022H to 005FH not used by the QC24(N) can be used.
The QC24(N) stores the received error code to the buffer memory data transmission result storage area (address: 257H).

6 ASCII-BIN conversion data communications

The following describes the contents of QC24(N) conversion processing and each data when data is communicated using ASCII-BIN conversion designation (buffer memory address: 121H) to designate ASCII-BIN conversion.

① ASCII-BIN conversion range

The QC24(N) converts the arbitrary data area (data length, data area) and error code of the message from ASCII data to BIN data.

② Data length conversion

- Transmission

  The QC24(N) converts the value of the send data count designation area to 4-digit (hexadecimal) ASCII code and sequentially transmits the ASCII code to the external device, beginning from the lower byte (L).
- Reception

  The QC24(N) converts the received data length (4-digit (hexadecimal) ASCII code) to 2-byte binary code and stores the binary code to the receive data count storage area.

③ Data area conversion

- Transmission

  The QC24(N) converts the send data of the send data designation area to 1 address/ 4-digit (hexadecimal) ASCII code and sequentially transmits the ASCII code to the external device, beginning from the lower byte (L).
- Reception

  The QC24(N) converts every two bytes of received data to a 1 byte binary code and stores the converted data to the receive data storage area.

④ Error code conversion

- Transmission

  The QC24(N) converts the error code of the detected error to 4-digit (hexadecimal) ASCII code and sequentially transmits it to the external device, beginning from the lower byte (L). (3412H is converted to "3412" and sequentially transmitted to the external device, beginning from "12".)
- Reception

  The QC24(N) converts the received error code (4-digit (hexadecimal) ASCII code) to 2-byte binary data, with the first 2 digits as the lower byte, and stores the binary data to the send result storage area.

  (When "1234" was received, it is converted to 3412H and stored.)

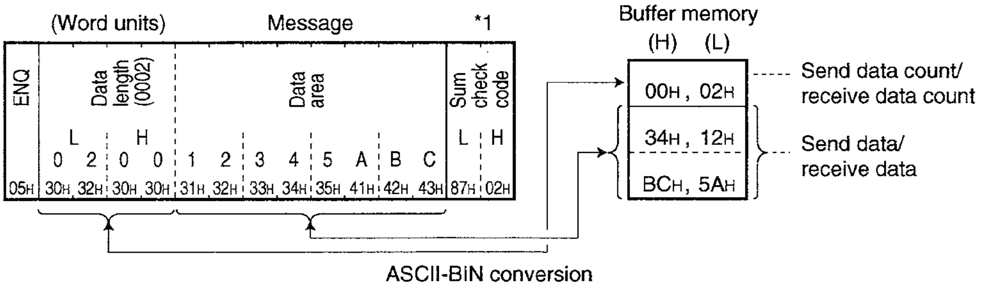
⑤ Handling of sum check code

The value of the lower 2 bytes of the result of addition of the data length and data area converted from ASCII code to binary code as binary data is handled unchanged.

- Transmission

  The QC24(N) calculates the sum check code for the data length and data area converted from ASCII code to binary code and adds it to the transmit message.
- Reception

  The QC24(N) calculates the sum check code for the received data length and data area before ASCII-BIN conversion and checks it, with the head of the received code as the lower byte.



*1 Checksum calculation

$30_H+32_H+30_H+30_H+31_H+32_H+33_H+34_H+35_H+41_H+42_H+43_H=\underset{(H)}{\underline{02}}\underset{(L)}{\underline{87}}_H$

7 The following describes the QC24(N) processing when the transmit and receive transparent code and additional code are designated in the buffer memories shown below and the additional code data is added to the communications data.

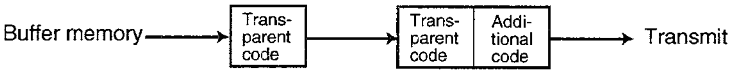
- Transmit transparent code designation (buffer memory address: 11FH)
- Receive transparent code designation (buffer memory address: 120H)

① Range of addition of additional code data
The QC24(N) processes the message data length, data area, and error code according to transparent code designation.

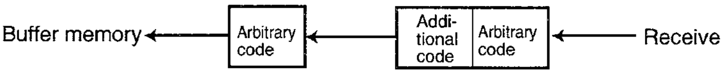
② Handling of transparent code and additional code data

- During data transmission, the QC24(N) adds the additional code data immediately before the transmit transparent code/additional code data.

  (Example)

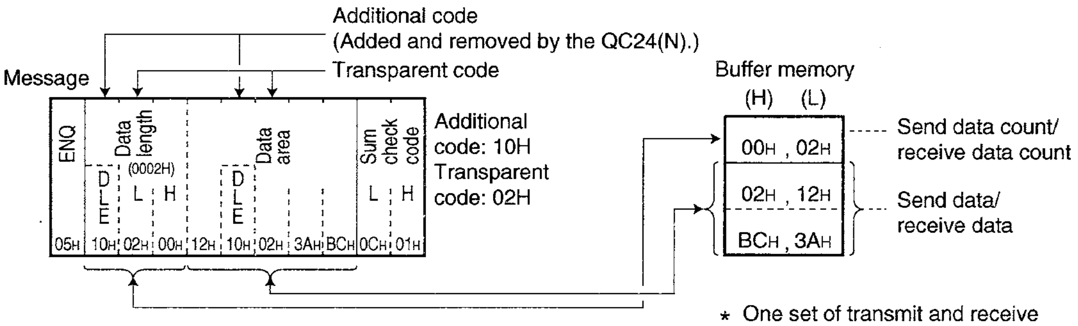


  During reception, when the QC24 detects receive additional code data, it removes the additional code data and receives the 1 byte of data immediately following the additional code data.



- When ASCII-BIN conversion is performed, during transmission the converted data becomes the transparent code and additional code objective and during reception the unconverted data becomes the transparent code and additional code objective. During transmission and reception, the QC24(N) adds and removes the additional code the same as described above.
- The data length does not include the additional code to be added or removed is not included. The additional code to be added and removed is not an objective of the sum check code either.

  (Example) ASCII-BIN conversion not performed



* One set of transmit and receive transparent codes and one set of transmit and receive additional codes can be set in the QC24(N) to match the specifications of the external device.

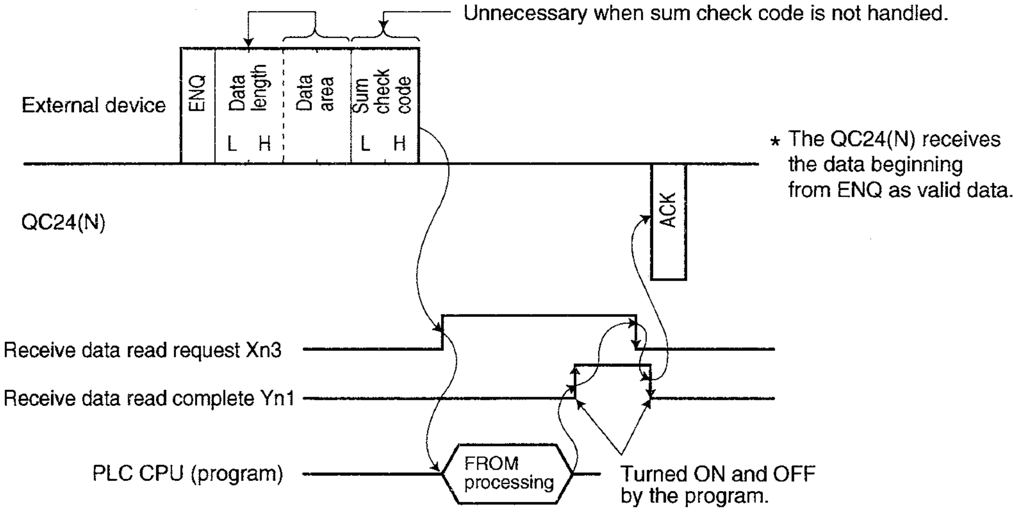
13.2 Receive Method (External Device→QC24(N))

The receive function stores the data received from the external device to the receive area and reads the stored data by the sequence program by FROM instruction.

13.2.1 Receive procedure

The following describes the receive procedure when the receive data is read to the PLC CPU.

Procedure

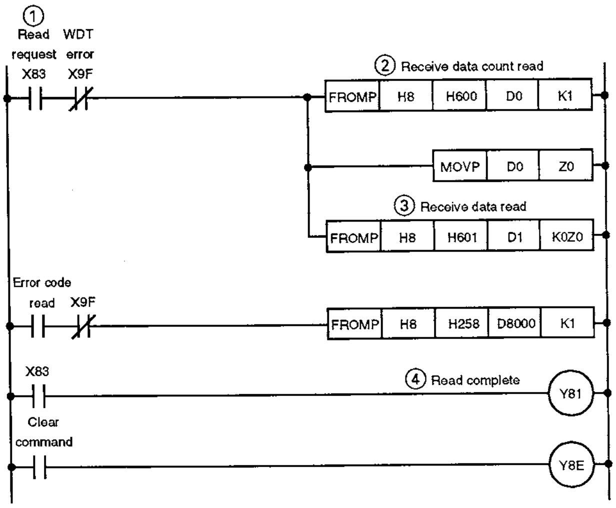


13.2.2 Receive program

The following describes a sample sequence program that reads the receive data stored to the QC24(N) buffer memory to the PLC CPU.
The receive data is read from the buffer memory receive area (default: addresses 600H to 7FFH).

1 Sample sequence program when applications instructions used (FROM, FROMP, DFRO, DFROP instructions)

See the programming manual (common instructions) for more information.



Reads the receive data count.

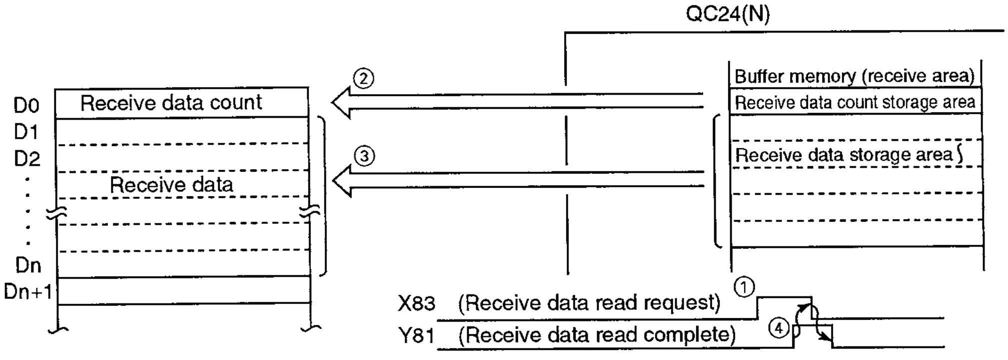
Stores the read data count to the index register (Z0)
(The illustration at the left is for word units.)

Reads the number of receive data corresponding to the receive data count.

Reads the receive error code.
Check the error contents with the error code stored in D8000 and take the action described in Section 22.1.

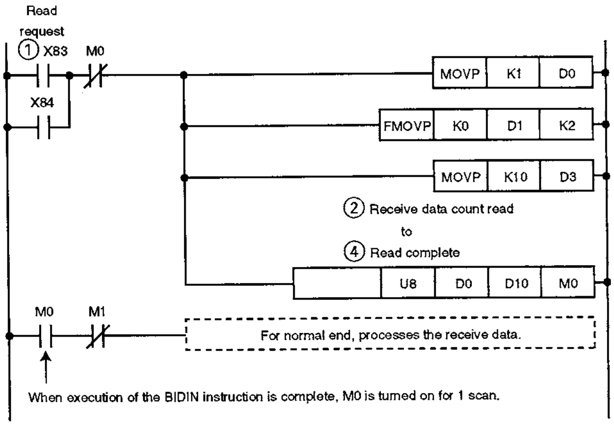
Turns ON the read complete signal.

Turns off the LED and clears the error code.
See Section 19.1.3 for a description of error code reading and clearing and turning off of the LED.



2 Sample sequence program when using the dedicated instruction (BIDIN instruction)

See the programming manual (special function module) for more information.

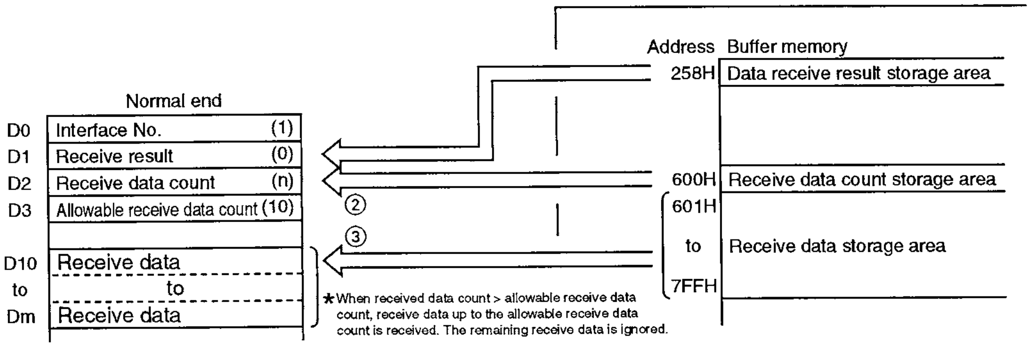


Designates the No. (CHC) of the interface that is to read the receive data.

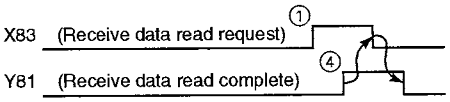
Clears the receive result and receive data storage area device to zero.

Designates the allowable number of receive data.

For normal end, reads the receive data corresponding to the allowable number of receive data (user designated) from the buffer memory receive data storage area.
After execution of the BIDIN instruction is complete, turns ON the user read complete signal (M0) for 1 scan.
The PLC CPU turns the receive data read and read complete signals are ON/OFF.



★When received data count > allowable receive data count, receive data up to the allowable receive data count is received. The remaining receive data is ignored.



POINTS

(1) When the QC24(N) dedicated instruction is used, model name registration by I/O allocation of the parameters that are written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and module model name (AJ71QC24) at the slot into which the QC24(N) is installed are set).

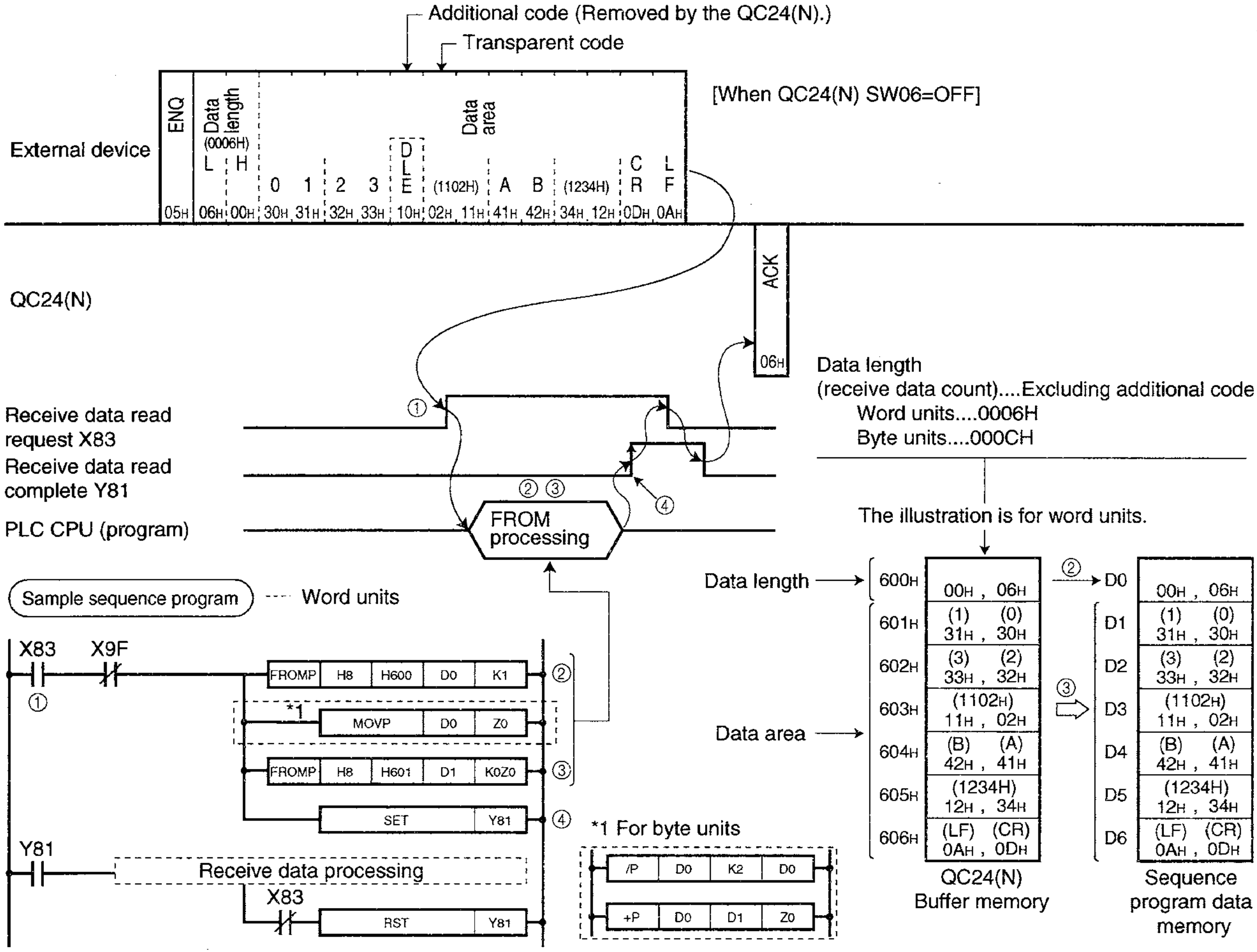
(2) The status of communications using the dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of (1) and (2) above.

3 Application example

The following uses a message to describe an example of application when application instructions are used to store the receive data to the read data register.
Except for the sequence program, the result of receive data storage is the same even when the dedicated instruction is used.

① When receive transparent code designated and ASCII-BIN conversion disabled are set
Additional code: 10H (DLE), transparent code: 02H (STX)



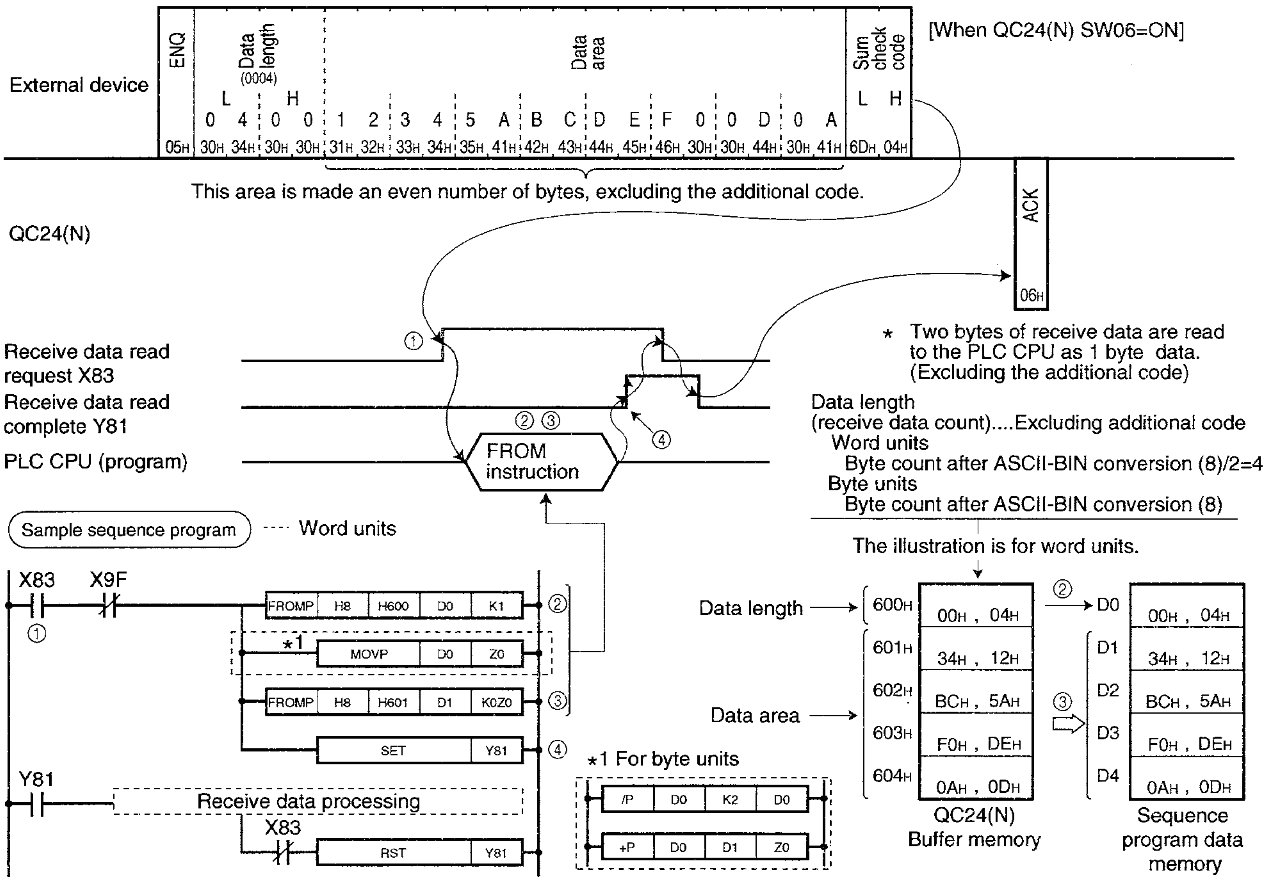
POINTS

(1) The following shows the arbitrary data area codes that can be received and the codes when the receive data is stored to the buffer memory receive area when receive transparent code designated, ASCII-BIN conversion disabled are set.

		Codes that can be received	Codes stored to receive area
Receive transparent code designation part	Additional code	01H to FFH	(Removed)
	Transparent code	00H to FFH	00H to FFH
Data length, data area			

(2) When the data length units are byte units and the data length is an odd number of bytes, 00H is stored to the higher byte of the last data storage location of the receive area.

② When receive transparent code designated, ASCII-BIN conversion enabled are set
Additional code: 10H(DLE), transparent code: 04H (EOT)



POINTS

(1) The following shows the arbitrary receive data area codes that can be received and the codes when the receive data is stored to the buffer memory receive area.

		Codes that can be received	Codes stored to receive area
Receive transparent code designation part	Additional code	01H to FFH	(Removed)
	Transparent code	30H to 39H	0H to 9H
Data length, data area		41H to 46H	AH to FH

(2) When the data length units is byte units and the data length is an odd number of bytes, 00H is stored to the higher byte of the last data storage location of the receive area.

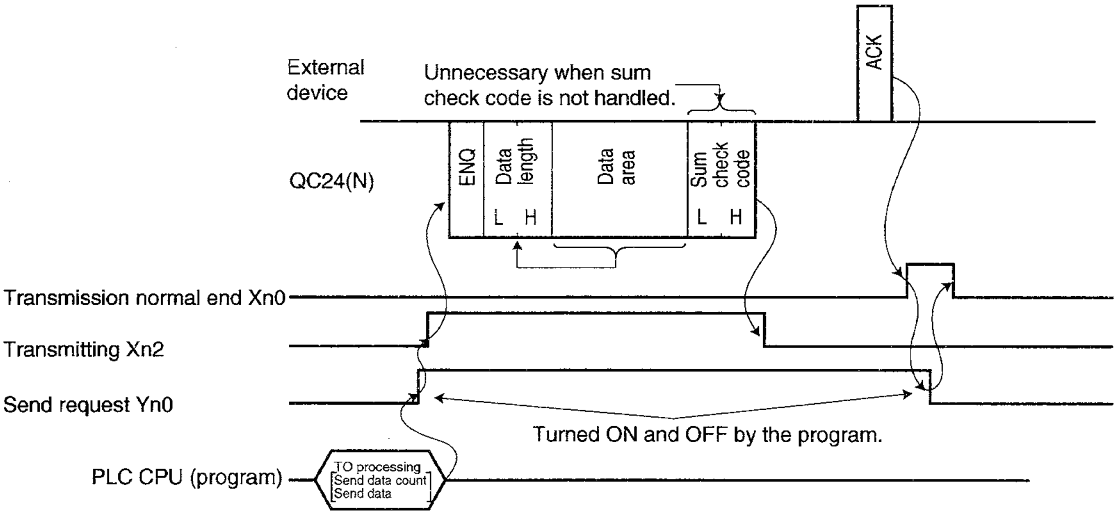
13.3 Transmit (QC24(N) → External Device)

The transmit function transmits the data written to the buffer memory transmit area from the sequence program by TO instruction to an external device from the QC24(N) when the PLC CPU issues a send request.

13.3.1 Transmission procedure

The following describes the procedure that transmits the data written to the transmit area to an external device.

Procedure



POINT

In the following cases, the QC24 stores the error code to the data transmission result storage area (address: 257H) and turns ON the transmission abnormal end signal (Xn1).

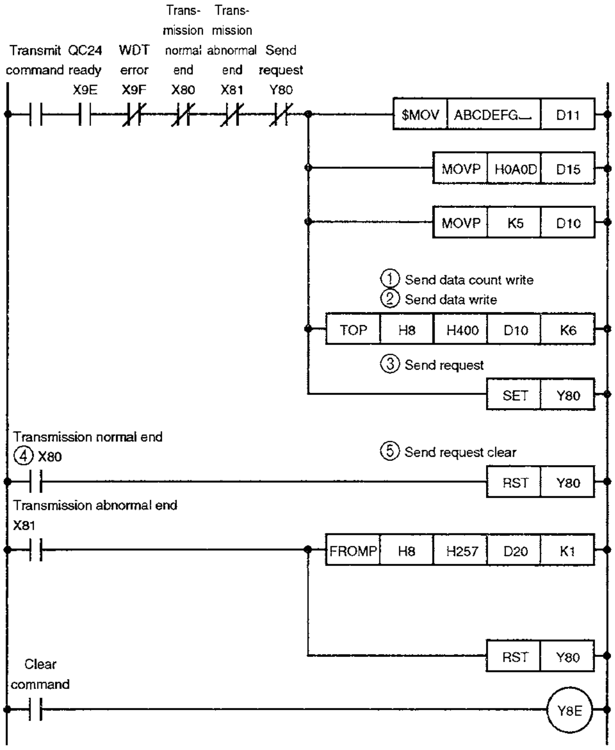
- When the send data count exceeds the size of the send data designation area
- When an error is generated during data transmission

13.3.2 Transmission program

The following describes sample sequence programs that transmit data from the PLC CPU to an external device.
The send data is written to the buffer memory transmit area (default value: addresses 400H to 5FFH).

1 Sample sequence program when application instructions used (TO, TOP, DTO, DTOP instructions)

See the programming manual (common instructions) for more information.



* Turn OFF the transmit command signal before turning on the transmission normal end signal (X80) or transmission abnormal end signal (X81).

Sets the send data and send data count.

Write the send data count and send data to the buffer memory.

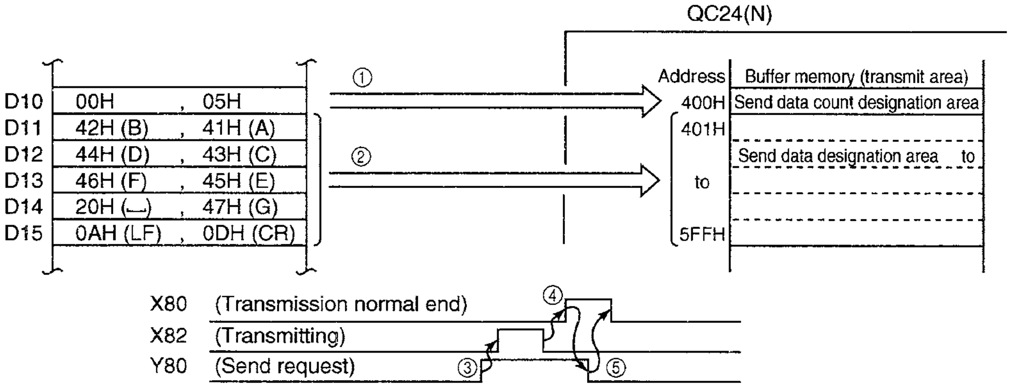
Turns ON the send request signal.

Turns OFF the send request signal.

Reads the send error code from the buffer memory.
Check the error contents with the error code stored in D20 and take the action described in Section 22.1.

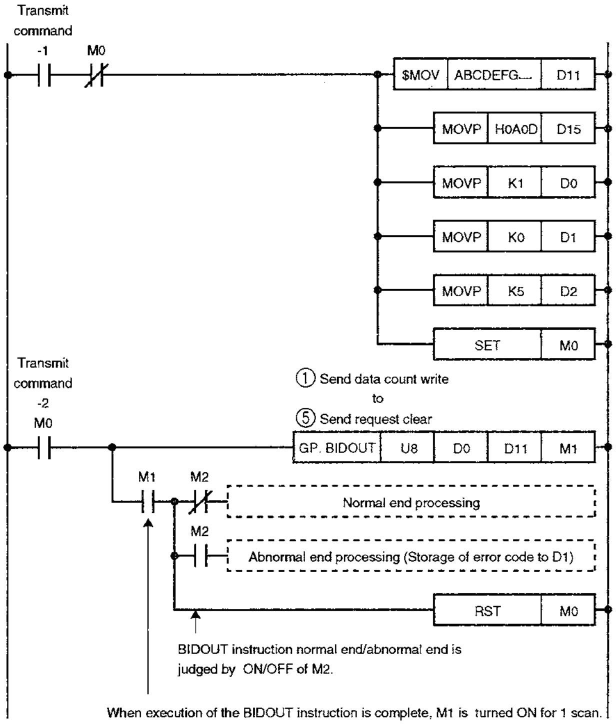
Turns OFF the send request signal.

Turns off the LED and clears the error code.
* See Section 19.1.3 for a description of error code read and clear and turning off of the LED.



2 Sample sequence program when dedicated instruction used (BIDOUT instruction)

See the programming manual (special function module) for more information.



* Turn OFF the transmit command-1 signal before turning ON the transmission normal end signal (X80) or transmission abnormal end signal (X81)

Sets the send data.

Designates the No. (CH☐) of the interface that is to transmit the data.

Clears the transmission result storage device to zero.

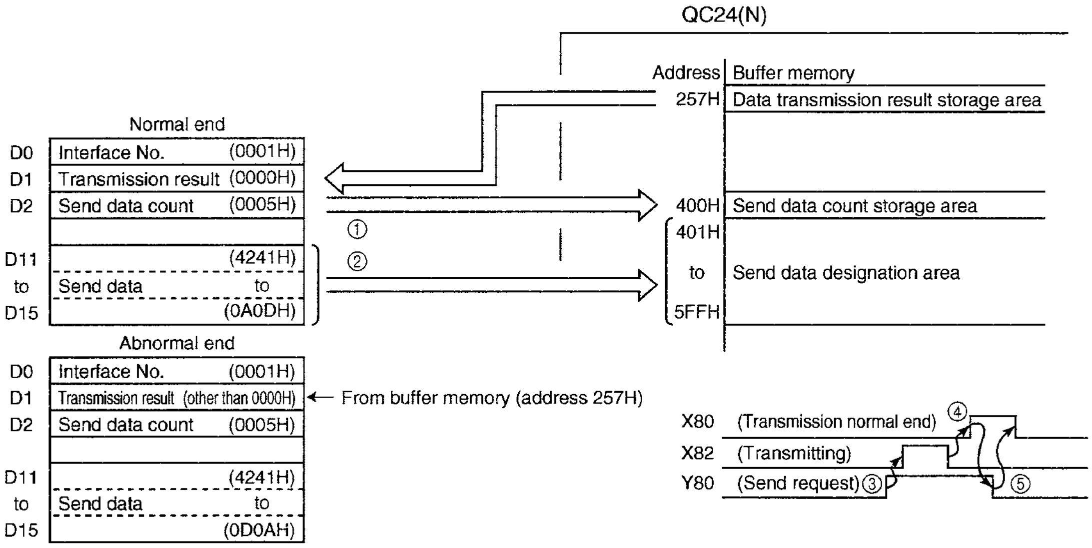
Designates the word units send data count. (For byte units, K10 is designated.)

Turns ON the transmit command-2 signal.

If transmit command signal-2 is ON, or is turned ON, the QC24(N) transmits the send data stored in the device.

After execution of the BIDOUT instruction is complete, the transmission normal end signal (M1) designated by the user is turned ON for 1 scan.

The PLC CPU writes the send data and send data count to the buffer memory and send a send request to the QC24(N).



POINT

(1) When the QC24(N) dedicated instruction is used, model name registration by I/O allocation of parameters written to the PLC CPU is unnecessary.
(During registration, the number of I/O points (special 32 points) and module model name (AJ71QC24) at the slot into which the QC24(N) is installed are set.)

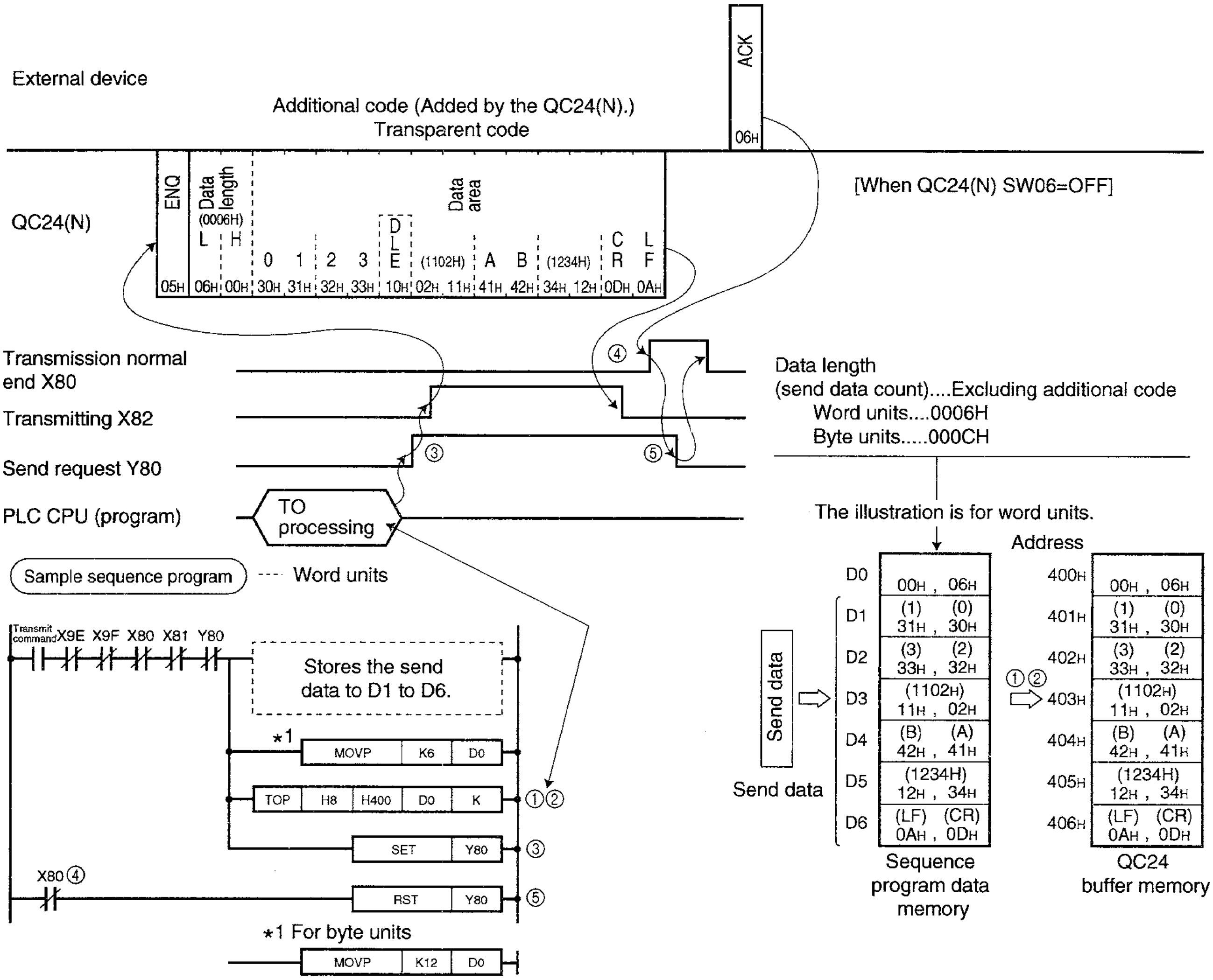
(2) The status of data communications using the dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of (1) and (2) above.

3 Application example

A descriptive message is used to describe an example of application when using application instructions to transmit data to an external device.
Except for the sequence program, the result of data transmission to the external device is the same even when the dedicated instruction is used.

① When transmit transparent code designated, ASCII-BIN conversion disabled are set Additional code: 10H (DLE), transparent code: 02H (STX)



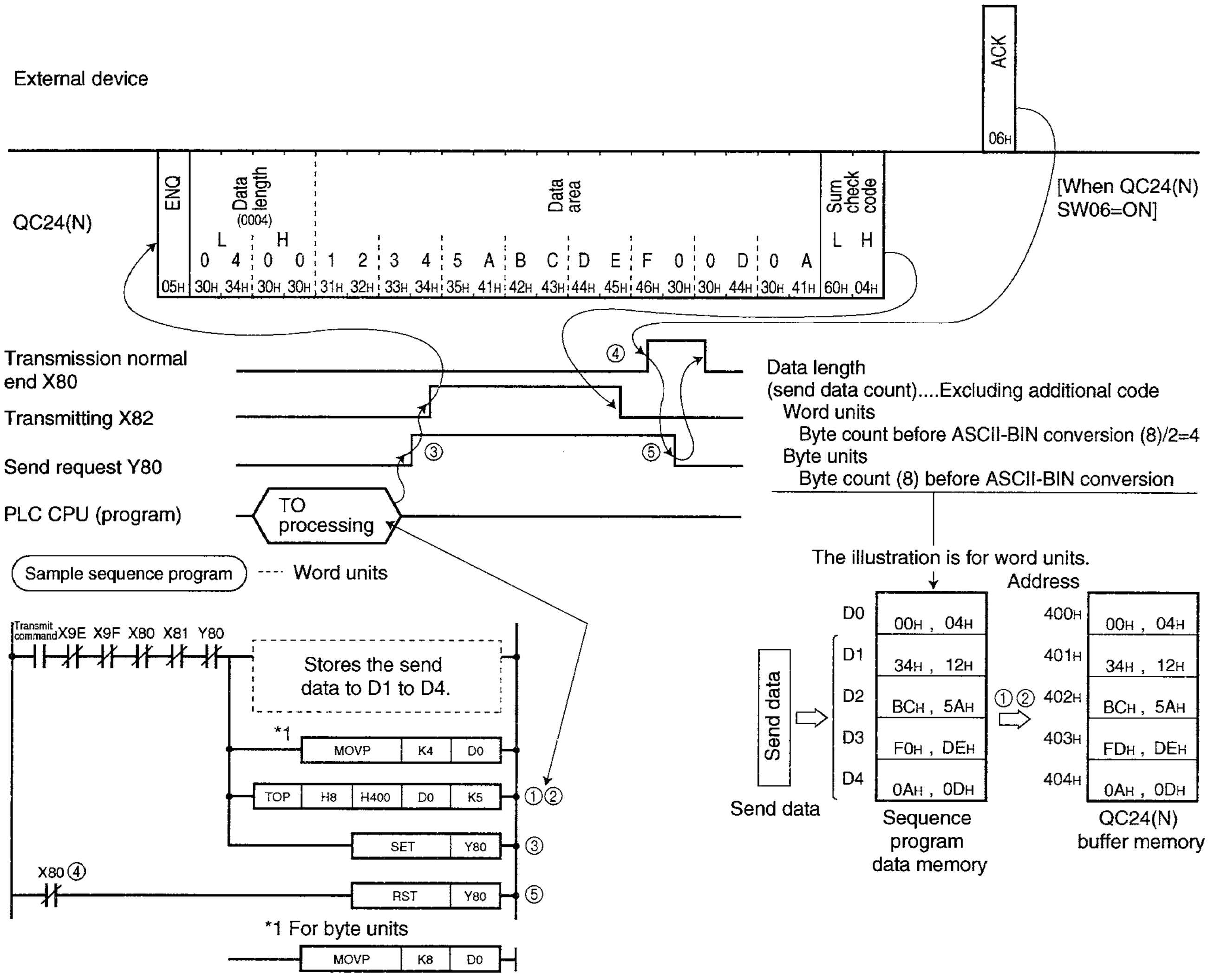
	Sequence program data memory	Address	QC24 buffer memory
D0	00H , 06H	400H	00H , 06H
D1	(1) (0) 31H , 30H	401H	(1) (0) 31H , 30H
D2	(3) (2) 33H , 32H	402H	(3) (2) 33H , 32H
D3	(1102H) 11H , 02H	403H	(1102H) 11H , 02H
D4	(B) (A) 42H , 41H	404H	(B) (A) 42H , 41H
D5	(1234H) 12H , 34H	405H	(1234H) 12H , 34H
D6	(LF) (CR) 0AH , 0DH	406H	(LF) (CR) 0AH , 0DH

POINTS

(1) The TO instruction write data count is in word units.
When writing the send data to the transmit area with the TO instruction when transmitting data in byte units, the write data count must be converted to word count (send data count ÷ 2).
For example, when the send data count is 12 bytes and 11 bytes, it is converted to 6 words.
11÷2=5.5....Fractions are truncated.

(2) When the send data count during transmission using byte units is an odd number, the data of the lower byte of the last send data designation area of the send data designation area is transmitted.

② When transmit transparent code designated, ASCII-BIN conversion enabled are set
Additional code: 10H (DLE), transparent code: 04H (EOT)



POINTS

(1) The data of one address (1 word) of buffer memory transmit area data is converted to 4-byte ASCII code data ("0" to "9", "A" to "F") and transmitted.

(2) The TO instruction write data count is in word units.
When the TO instruction is used to write the send data to the transmit area when data is transmitted in byte units, the write data count must be converted to word count (send data count ÷ 2).
For example, when the send data count is 8 bytes and 7 bytes, it is converted to 4 words.
7÷2=3.5....Fractions are truncated.

(3) When the send data count during data transmission in byte units is an odd number of bytes, the data of the lower byte of the last send data designation location of the send data designation area is transmitted.

SPECIAL FUNCTIONS

This section is divided into chapters that describe serial communications module initialization, initial values, and the user frame registration method and serial communications module operating status check method when using the serial communications module.

Read the descriptions of only the functions that you use.

14. BUFFER MEMORY SPECIAL APPLICATIONS AREA INITIALIZATION

The QC24(N) buffer memory has a special applications area that sets the control information needed to perform the data communications described in Section 3.5.
The QC24(N) default values are set in each area of the special applications area. However, the default values may have to be changed, depending on the data communications purpose and application and the specifications of the external device.
The following describes the contents, setting method, and sample programs of item set to the special applications area.

POINTS

(1) This section describes only the information necessary when changing the default values set to the QC24(N) buffer memory special applications area in advance.
Read only those parts whose default value must be changed.
If you use the default values during data communications, you do not have to read this section.

(2) The values set to the special applications area (including the set values changed by the user) can be registered to the QC24(N) EEPROM.
It is recommended that you check that data communications with external devices is performed normally before registering the values set to the special applications area to the QC24(N) EEPROM and using them as the default values during QC24(N) starting.

* Using the parameters registered to the QC24(N) EEPROM as the default values eliminates the need for a sequence program of the parts whose default value was changed.

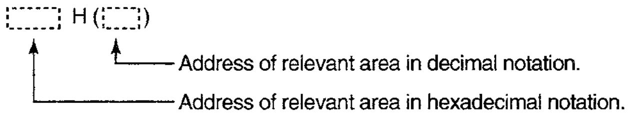
(3) See Section 14.1 for the area that can be registered to the QC24(N) EEPROM and Chapter 15 for a description of the registration method.

14.1 Initialization Areas and Areas that can be Registered to EEPROM

The following describes the objective areas when the QC24(N) buffer memory special applications area is initialized by changing the default values and the areas whose parameters can be registered to the QC24(N) EEPROM.

(How to read the tables)

① Address shown in address and Objective I/F column
When the parameter of the relevant area is related to both the CH1 and CH2 interfaces, the addresses are given in the center of the columns as shown below.
When the parameter of the relevant area is related to the CH1 or the CH2 interface only, the address is given in the objective CH column as shown below.



② Meaning of symbol in Setting column.
○: Initialization area

③ Meaning of symbol in Registration column.
●: Area whose parameter can be registered to the QC24(N) EEPROM

④ Meaning of symbols in Objective Protocol column.
○: Area used by protocol or user related to parameter of relevant area using the control/control method for the QC24(N).
—: System area, or area not used by the relevant protocol.

Address and objective I/F		Setting	Registration	Application	Name		QC24(N) default value	Objective protocol			Reference section
CH1	CH2							Dedicated	Non procedure	Bidirectional	
2EH(46)		○	●	System setting	Modem functions	Modem connection CH designation	0	○			Chapter 21
2FH(47)						Notification execution designation	0 (Not executed)				
30H(48)						Number of connection retries designation	3				
31H(49)						Connection retries interval designation	180 (sec.)				
32H(50)						Initialization/connection time-out designation	60 (sec.)				
33H(51)						Number of initialization retries designation	3				
34H(52)						Data number for initialization designation	2000				
35H(53)						Data number for connection designation	0				
36H(54)						Q6TEL connection designation	0				
37H(55)						No-communication interval time designation	30 (min.)				
38H(56)						RS·CS control/not-control designation	1 (Control)				
40H(64)		○	●		Y signal·buffer memory monitoring timing designation		0	○			Section 14.12
80H(128)					For PLC CPU information clear	PLC CPU information clear request	0	○	—		Section 19.6
93H(147)	133H(307)	○	●		Transmission control	DTR/DSR, DC control designation	0 (DTR/DSR control)	○			Section 14.3
94H(148)	134H(308)					DC1/DC3 code designation	1311H (11H/13H)				
95H(149)	135H(309)					DC2/DC4 code designation	1412H (12H/14H)				
96H(150)	136H(310)				Word/byte designation (message data length units)		0 (word units)	○ [On-demand]	○		Section 14.4
97H(151)	137H(311)				RS-232C CD terminal check designation		1 (Do not check)	○			Section 4.7.2
98H(152)	138H(312)				RS-232C communication method designation		0 (full-duplex communications)	○			Section 14.5
99H(153)	139H(313)				Half-duplex communications	Priority/nonpriority during simultaneous transmission	0 (priority transmission)	○			
9AH(154)	13AH(314)					Transmission method at restart of transmission	0 (Do not retransmit)				
9BH(155)	13BH(315)				Data valid/invalid at simultaneous transmission		0 [Send data and receive data valid]	—		○	Section 14.6
9CH(156)	13CH(316)				No reception watchdog timer (timer 0) designation		0H (Unlimited wait)	○			Section 14.7
9DH(157)	13DH(317)				Response watchdog timer (timer 1) designation		32H (5 seconds)	○	—	○ (receive only)	
9EH(158)	13EH(318)				Transmit watchdog timer (timer 2) designation		708H (3 minutes)	○	—	○	
9FH(159)	13FH(319)				System area (Prohibited to use)		0	—			—
A0H(160)	140H(320)		●		On-demand	Buffer memory head address designation	CH1: 400H CH2: 800H	○	—		Section 6.9, Chapter 7
A1H(161)	141H(321)					Data length designation	0				

Address and objective I/F		Setting	Registration	Appli-cation	Name				QC24(N) default value	Objective protocol			Reference section
CH1	CH2									Dedicated	Non proce-dure	Bidire-ctional	
A2H(162)	142H(322)	○	●	System setting	Transmit/ receive settings	Transmit buffer memory head address designation			CH1: 400H CH2: 800H	—	○		Section 14.8
A3H(163)	143H(323)					Transmit buffer memory length designation			200H				
A4H(164)	144H(324)					Receive end data count designation			1FFH	—	○	—	
A5H(165)	145H(325)					Receive end code designa-tion			0D0AH (CR, LF)				
A6H(166)	146H(326)					Receive buffer memory head address designation			CH1: 600H CH2: A00H	—	○		
A7H(167)	147H(327)					Receive buffer memory length designation			200H				
A9H(169)	149H(329)				On-demand user frame designa-tion	Header frame No. designation	(1st)		0 (None)	○	—		Chapter 7
AAH(170)	14AH(330)						(2nd)						
ABH(171)	14BH(331)					Trailer frame No. designation	(1st)		0 (None)				
ACH(172)	14CH(332)						(2nd)						
ADH(173)	14DH(333)		●		Receive user frame designa-tion	User frame use control			0 (Do not use)	—	○	—	Section 14.9
AEH(174)	14EH(334)					Header frame No. designation	(1st)		0 (None)				
AFH(175)	14FH(335)						(2nd)						
B0H(176)	150H(336)						(3rd)						
B1H(177)	151H(337)						(4th)						
B2H(178)	152H(338)					Trailer frame No. designation	(1st)		0DH (CR)				
B3H(179)	153H(339)						(2nd)		0AH (LF)				
B4H(180)	154H(340)						(3rd)		0 (None)				
B5H(181)	155H(341)						(4th)						
B7H(183)	157H(343)				Transmit user frame designa-tion	Schedule setting	CR/LF output desig-nation		0 (Do not output)	—	○	—	Section 9.4.1 Section 9.6.2 Chapter11
B9H(185)	159H(345)						Output count desig-nation		0 (None)				
BAH(186)	15AH(346)						Output frame No. designation	1st	0 (None)				
BBH(187) to 11DH(285)	15BH(347) to 1BDH(445)							(2nd) to (100th)	0 (None)				
11EH(286)	1BEH(446)	○	●		Message wait time designation (Used in communications other than A compatible frame communications)				0 (No wait time)	○	—		Section 14.7.4
11FH(287)	1BFH(447)				Transmit transparent code designation				0 (None)	—	○		Seciton 14.10
120H(288)	1C0H(448)				Receive transparent code designation				0 (None)				
121H(289)	1C1H(449)				ASCII-BIN conversion designation				0 (Conversion disabled)				Section 14.11

Note

The entire buffer memory allocation table is shown in Section 3.5.

14.2 Precautions when Reading and Writing Buffer Memory Special Applications Area

The following describes the precautions to be observed when using a sequence program to read and write the QC24(N) buffer memory special applications area.

(1) When the QC24(N) is started (QC24(N) ready signal X (n+1) E = ON), writing to the initialization special applications area described in Section 14.1 must be performed.
Therefore, use the sequence program to initialize this area.
Do not initialize this area from an external device. (The QC24(N) will not operate normally.)

(2) Set all settings in each area to values within the allowable ranges designated in the corresponding operation manuals.

(3) The buffer memory is not backed up by battery.
When the QC24(N) starts, the QC24(N) default values, or the default values registered to the QC24(N) EEPROM by the user, are written to the special applications area.

(4) When using the following functions at the same time, allocate the buffer memory user area, which stores the send data and receive data handled by the function used, so that the buffer memory user areas are not duplicated.
If an area is duplicated, the data will be overwritten and data communications will not be performed normally.

- Dedicated protocol buffer memory read and write functions .. See Section 6.3.
- Dedicated protocol on-demand function .... See Section 6.9 and Chapter 7.
- Non procedure protocol transmit and receive functions .... See Sections 9.3.2 and 9.4.1.
- Bidirectional protocol transmit and receive functions .... See Sections 12.3.2 and 12.4.1.

(5) Do not write data in the "system area" of the buffer memory of the special function module.
If data is written in the system area, the PLC system may result in malfunctions.

14.3 Data Communications Using DC Code Transmission Control

The transmission control function controls (termination, restart) the transmission and reception of data between the QC24(N) and external device by turning signals on and off, or by transmitting and receiving DC codes (DC1, DC2, DC3, DC4).
The transmission control function can be set for each QC24(N) interface. The QC24(N) uses the transmission control function set by the user to control data communications with external devices.
Set the transmission control function to match the specifications of the opposite device.

The table below shows the QC24(N) transmission control functions.
Section 14.3.1 describes DTR/DSR signal control and Section 14.3.2 describes DC code control.

Transmission control function	Cind of control	Interface that can be controlled			Protocol that can be controlled			Note
		232C	422	422/485	Dedicated	Non procedure	Bidirectional	
DTR/DSR signal control *1	DTR control	○	○	○ (Ignored)	—	○	—	Cannot be used simultaneously with DC control. One is selected.
	DSR control				○	○	○	
RS/CS signal control *2		○	—	—	○	○	○	Normal control
CD signal control *2		○	—	—	○	○	○	The cable wiring depends on whether or not control is used. With half duplex communications, control is necessary.
DC code control *1	DC1/DC3 transmission control	○	○	○	—	○	—	Cannot be used simultaneously with DTR/DSR signal control. One is selected.
	DC1/DC3 reception control				○	○	○	
	DC2/DC4 transmission control				○	○	○	
	DC2/DC4 reception control				○	○	○	

○ : Possible (transmission control used)
—: Invalid

*1 When using full-duplex communications with bidirectional protocol data communications, see [POINT] in Section 12.5.

*2 See Section 3.2.1 $\boxed{1}$ and check QC24(N) operation according to the RS and CS signal control contents and CD terminal check designation.

POINT

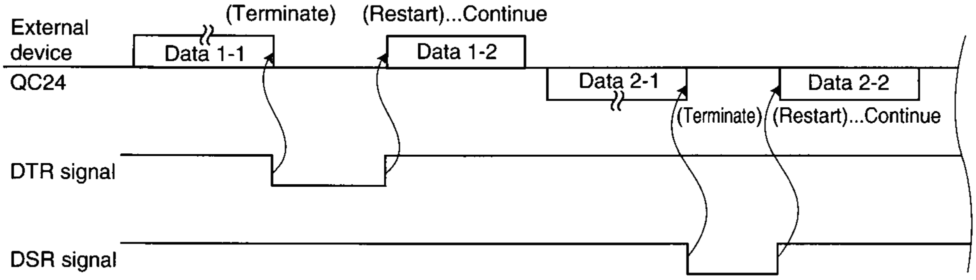
When the QC24(N) is started, DTR/DSR signal control and RS/CS signal control are enabled.

14.3.1 Control contents of DTR/DSR (ER/DR) signal control

This control uses the RS-232C interface DTR/DSR signals and RS422 interface DTR ⬚ /DSR ⬚ signals (hereafter abbreviated DTR/DSR) to inform the opposite device whether or not the local station is ready to receive data.

The QC24(N) uses the DTR (ER) signal to inform the opposite device whether or not the local station is ready to receive data and uses the DSR (DR) signal to check if the opposite device is ready to receive data.

(Example)



1 QC24(N) DTR control contents

The QC24(N) uses the DTR signal to inform the external device whether or not it is ready to receive data.

The data transmitted from the external device by non procedure protocol is stored to the buffer memory receive data storage area through the OS area. (See Section 9.3.1 *1.)

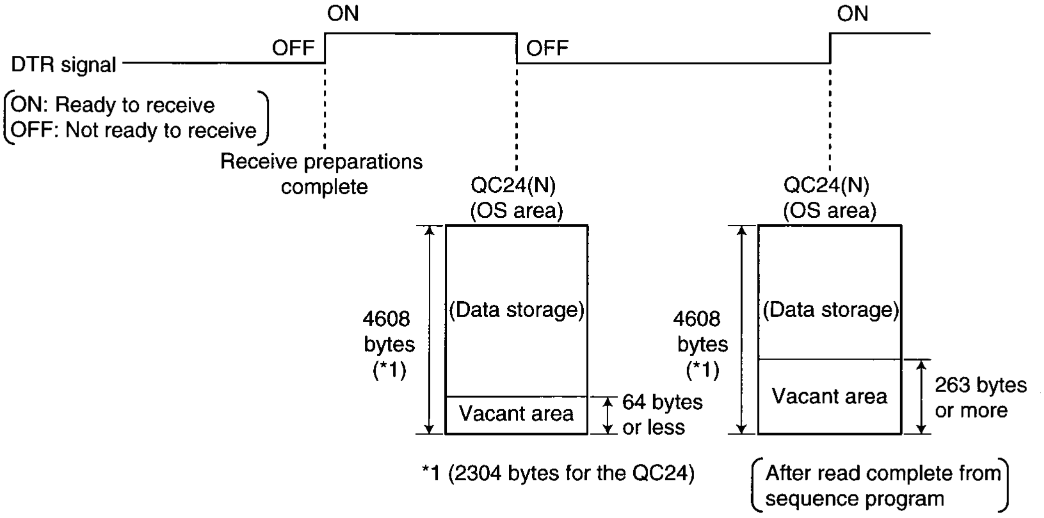
For the following conditions, the receive data is stored to the OS area and is transferred when the QC24(N) is ready to transfer the data to the receive data storage area (read request signal OFF).

① Receive data size exceeds the size of the buffer memory area when receive data storage area < receive data length data was received

② The data was received before the sequence program read the previously received data

The QC24(N) turns the DTR signal ON/OFF as shown below, depending on the size of the vacant OS area.

- Vacant area 64 bytes or less.......... OFF
- Vacant area 263 bytes or more ..... ON



Notes

- "Receive data clear" described in Section 9.3.4 clears the data stored in the OS area. (The receive area in the buffer memory is not cleared.)
- If more data is received when the OS area mentioned above is 0 bytes, an SIO error is generated and the data received until the OS area becomes vacant is ignored. At this time, the SIO LED is turned on. (See Section 4.4.)

2 QC24(N) DSR control

The QC24(N) uses the DSR signal to detect whether or not the external device is ready to receive data and to control data transmission to the external device as shown below, depending on whether the DSR is ON/OFF.

① If the DSR signal is ON and there is send data, the QC24(N) transmits it to the external device.

② If the DSR signal is OFF, even if there is send data, the QC24(N) does not transmit it to the external device.
When the DSR signal is turned ON, the QC24(N) transmits the send data to the external device.

14.3.2 Control contents of DC code control

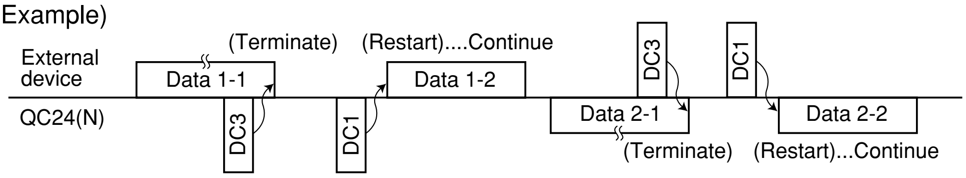
This control uses the QC24(N) transmission control data to inform the opposite device whether or not its own station is ready to receive data and the valid range of the send and receive data.
The four kinds of QC24(N) DC code control shown below are available. These control functions can be used simultaneously.

1 DC1/DC3 transmission control, DC1/DC3 reception control

The QC24(N) tells the opposite device whether or not its own station is ready to receive data by transmitting the DC1 and DC3 signals and checks whether or not the opposite device is ready to receive data by receiving the DC1 and DC3 signals.

DC1 ..... Control data that tells the opposite device that the QC24(N) is ready to receive data
DC3 ..... Control data that tells the opposite device that the QC24(N) is not ready to receive data

(Example)

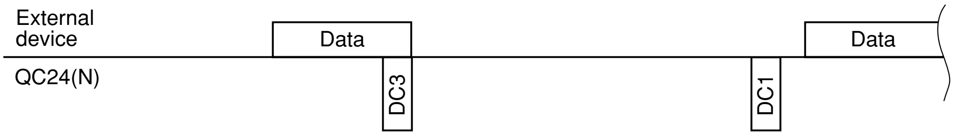


(a) QC24(N) DC1/DC3 transmission control contents

The control contents are the same as those described in Section 14.3.1 1 DTR control.
The QC24(N) transmits DC1 or DC3 to the external device instead of turning the DTR signal ON/OFF.
For the DC1 and DC3 transmit timing, replace DTR signal ON/OFF as shown below.

(DTR control) (DC1, DC3 transmission control)

DTR signal OFF=DC3 transmit ..... Transmitted when the vacant OS area drops to 64 bytes or less
DTR signal ON=DC1 transmit .... Transmitted when the vacant OS area reaches 263 bytes or more



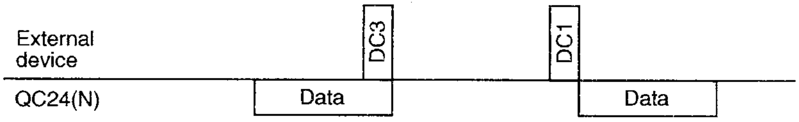
Notes

- Receive data clear described in Section 9.3.4 clears the OS area simultaneously with clearing of the receive data save area.
- If more data is received when the vacant OS area mentioned above is 0 bytes, an SIO error is generated and the data received until the OS area becomes vacant is ignored. At this time, the SIO LED is turned on. (See Section 4.4.)

(b) QC24(N) DC1/DC3 reception control contents

① When the QC24(N) receives DC3 from the external device, it terminates data transmission.
The sequence program cannot read the received DC3 signal.

② When the QC24(N) receives DC1 from the external device, it restarts data transmission.
(The QC24(N) resumes transmission from the terminated data.)
The sequence program cannot read the received DC1 signal.



③ Once DC1 is received, subsequent DC1 signals are ignored and are removed from the receive data.

POINTS

(1) The following describes the state of the QC24(N) when the power is turned on, the CPU is reset, or the mode is switched during DC1, DC3 transmission control and DC1/DC3 reception control.

(2) DC1 is not transmitted to the external device.
- This is the same state as when DC1 was transmitted.
- The same state as when DC1 was received even if DC1 is not received from the external device.

(3) The DC1 and DC3 codes can be changed. See Section 14.3.4 for description of the modification method.

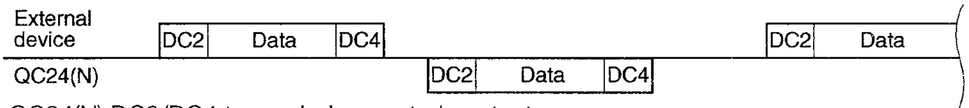
2 DC2/DC4 transmission control, DC2/DC4 reception control

The QC24(N) encloses the send data from the local station in the DC2 and DC4 codes and transmits it to the external device and processes the data received from an external device enclosed in the DC2 and DC4 codes as valid data.

DC2 ..... Control data that tells the opposite device that the data following it is the start of the valid data

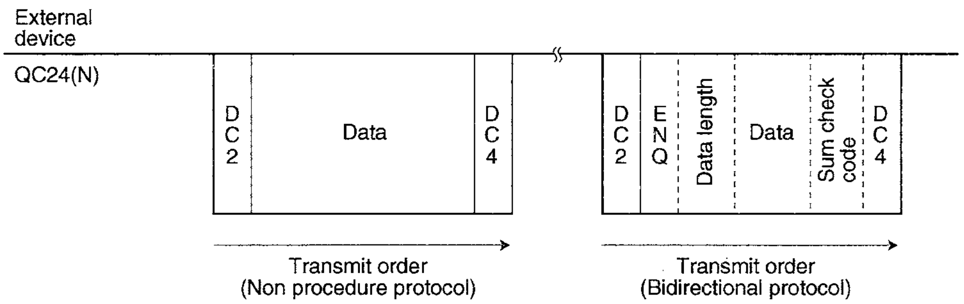
DC4 ..... Control data that tells the opposite device that the data immediately preceding it is the end of the valid data

(Example)



(a) QC24(N) DC2/DC4 transmission control contents

When transmitting data to an external device, the QC24(N) adds the DC2 code to the head of the send data and the DC4 code to the end of the send data.

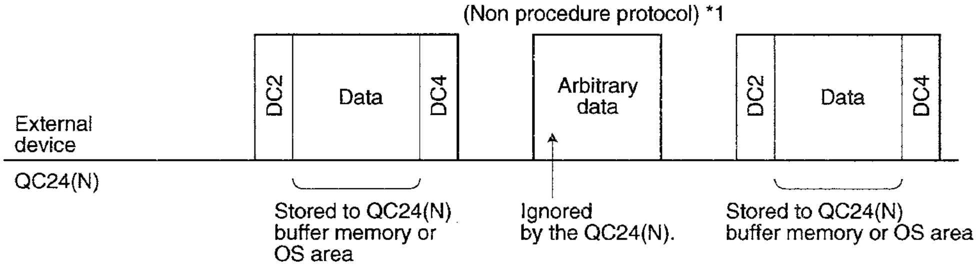


*The DC2 and DC4 codes are also added when dedicated protocol is used.

(b) QC24(N) DC2/DC4 reception control contents

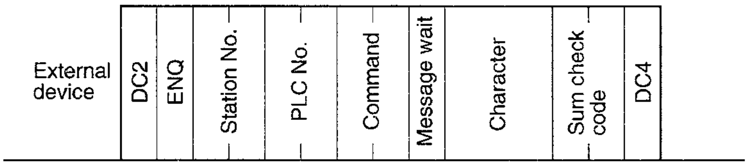
① When the QC24(N) receives DC2 from the external device, it processes the receive data up to DC4 as valid data.
The sequence program cannot read the received DC2 code.

② When the QC24(N) receives DC4, it ignores the receive data up to immediately before DC2 as invalid data.
The sequence program cannot read the received DC4 code.



③ Once DC2 is received, subsequent DC2 are ignored and are removed from the receive data.

*1 Dedicated protocol A compatible frame format 1



14.3.3 Precautions when using the transmission control functions

The following describes the precautions to be observed when using the QC24(N) transmission control functions.

1 Agreement between external device and PLC CPU

The external device and PLC CPU must agree to the following.

① Whether or not a transmission control function is to be used. If a control function is used, which control is to be used for data communications.

② Control timing.

③ DC1 to DC4 codes when DC control performed.
(The DC1 to DC4 codes used can be arbitrarily changed.)

2 Transmission control function usage conditions

① DTR/DSR control and DC code control cannot be used at the same time.
Select one of them using the QC24(N) buffer memory DTR/DSR and DC control designation areas (addresses 93H/133H).

② When using DTR/DSR control, connect the QC24(N) DTR and DSR signals to the external device. (See Section 4.7.2.)

3 Transmission control function setting

Set a transmission control function that can control the objective interface.
If a function that cannot control the objective interface is set, the set contents are invalid.

4 Setting of transmission control function during linked operation

When the two QC24(N) interfaces are linked (see Section 4.3.1), set the transmission control function of only the interface that must be controlled.
Set the other interface to "Do not use transmission control function" (set value: 0001H).

5 DC code control

① DC1/DC3 transmission control and DC1/DC3 reception control are possible when full duplex communications is used to communicate data between the QC24(N) and external devices.
Do not use DC1/DC3 control with half-duplex communications.

② The same data as the DC1 to DC4 codes cannot be included in the user data.
To handle the same data as a DC code as user data, do the following.

- Use DTR/DSR control.
- Change the DC code.
- Do not use the transmission control functions.

POINT

If the user data received from the external device includes the relevant DC code when DC1/DC3 reception control and DC2/DC4 reception control are used, the QC24(N) uses the corresponding DC code control.
If the user data transmitted from the PLC CPU includes a DC code, it is sent unchanged.

6 Handling of DTR and DSR signals when DTR/DSR control not used

When the DTR/DSR control function is not used, the QC24(N) handles the DTR and DSR signals as described below.

① Leaves the DTR signal ON.

② Ignores the DSR signal ON/OFF state.

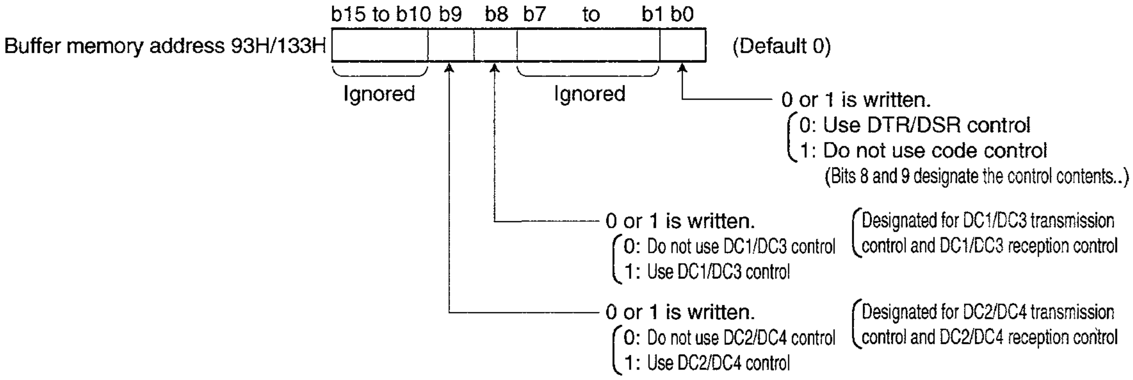
14.3.4 Initialization to buffer memory

When switching from DTR/DSR control to DC code control, or when changing the DC code (control code), writing to the buffer memory special applications area is necessary.
The following describes writing to the buffer memory special applications area when changing the transmission control method or DC code.

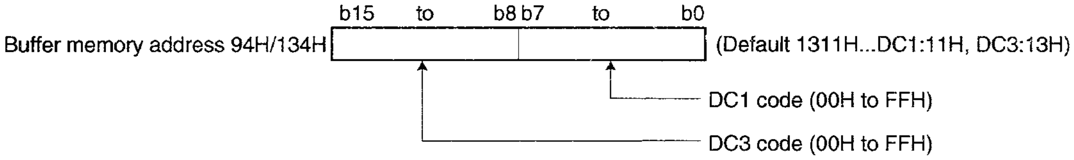
1 **Initialization area**

The transmission control setting data is stored to the buffer memory as described below.

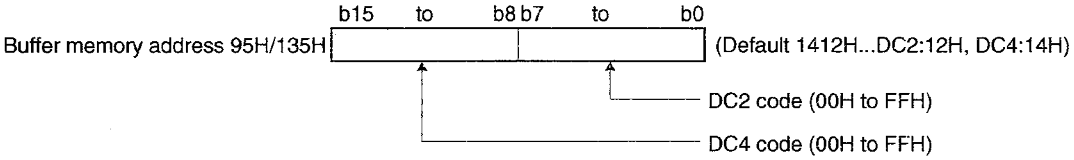
① DTR/DSR, DC control designation area (addresses: 93H/133H)



② DC1/DC3 code designation area (addresses: 94H/134H)



③ DC2/DC4 code designation area (addresses: 95H/135H)



POINTS

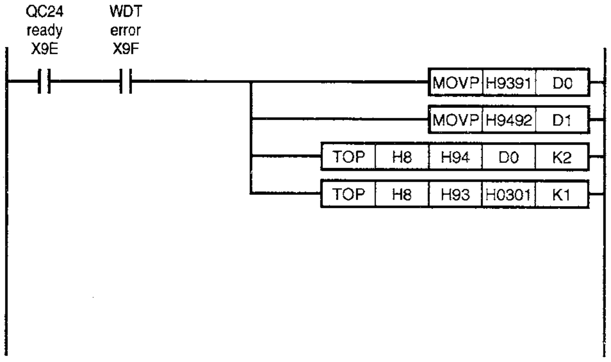
(1) Cannot be set when data is not communicated when the QC24(N) is started.

(2) When changing the DC code, write to ② and ③ above, then designate "Use DC code control" at ①.

2 Transmission control method and control code modification sample program

The following shows a sample program that uses the TO instruction to change the CH1 transmission control method and DC1 to DC4 control codes.
(QC24(N) I/O signals 80H to 9FH)

① When DC code control used



When changing the DC1 and DC3 codes to 91H and 93H. *1

When changing the DC2 and DC4 codes to 92H and 94H. *2

Writes the DC codes to be changed.

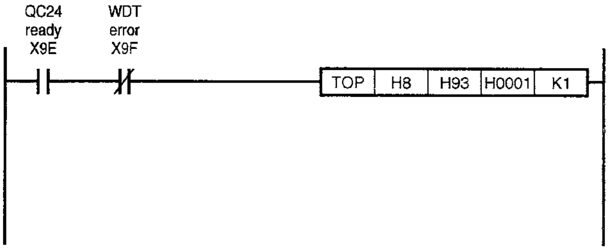
Writes "enable DC code control".
(Enable DC1/DC3 control, disable DC2/DC4)
The written values are shown below. *3
- Use DC1/DC3 control, do not use DC2/DC4 control → 0101H
- Do not use DC1/DC3 control, use DC2/DC4 control → 0201H
- Use DC1/DC3 control, use DC2/DC4 control → 0301H

*1 When the DC1 and DC3 codes are not changed, writing to address 94H is unnecessary,

*2 When the DC2 and DC4 codes are not changed, writing to address 95H is unnecessary.

*3 Write the value of the control function to be used.

② When transmission control function not used



Writes 0001H (transmission control not used).
- Bit 0...Use DC code control.
- Bit 8...Do not use DC1/DC3 control.
- Bit 9...Do not use DC2/DC4 control.

POINT

Designated value when transmission control function used/not used.
The value set to buffer memory addresses 93H/133H when the QC24(N) transmission control functions are used and are not used are shown below.

		Designated value
Control function	DTR/DSR control	0000H (default value)
	DC code control	0101H, 0201H, or 0301H
	When transmission control functions not used	0001H

14.4 Changing Send and Receive Data Length Units to Byte Units

This setting determines the units of the data length (count) of the data size to be sent to and received from the external device.

The data length units can be set for each QC24(N) interface. The QC24(N) controls the number of data to be transmitted to the external unit and the number of data when it requests the PLC CPU to read the data received from the external device according to the units set by the user.

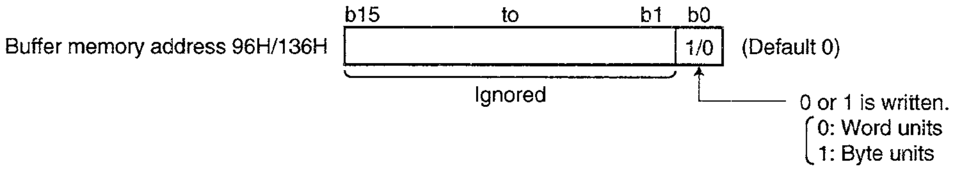
1 Data communication functions and buffer memory related to data length units

The following shows the data communications functions and buffer memory related to the data length units.
(The buffer memory addresses in the table are the default value.)

Data communications function		Name of buffer memory related to data length units (Address CH1, CH2)	Reference section
Dedicated protocol	On-demand function	On-demand data designation area (A1H, 141H)	Section 6.9, Chapter 7
Non procedure protocol	Data transmit function	Send data count storage area (400H, 800H)	Section 9.4.1, Chapter 10, Chapter 11
	Data receive function	Receive end data count designation area (A4H, 144H) Receive data count storage area (600H, A00H)	Section 9.3.1, Section 9.3.2, Chapter 10, Chapter 11
Bidirectional protocol	Data transmit function	Send data count storage area (400H, 800H)	Section 12.4.1, Chapter 13
	Data receive function	Receive data count storage area (600H, A00H)	Section 12.3.1, Section 12.3.2, Chapter 13

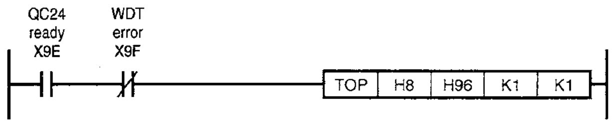
2 Word/byte designation area (addresses: 96H/136H)

The data length units are stored to buffer memory addresses 96H/136H as shown below.



3 Data length units setting sample program

The following shows a sample program that sets byte units as the CH1 data length units.
(QC24(N) I/O signals 80H to 9FH)



Write "1" (byte units) to buffer memory address 96H.

14.5 Data Communications Using Half-Duplex Communications

For data communications between the QC24(N) and an external device using the RS-232C interface, the buffer memory special applications area is set so that the QC24(N) and the external device do not transmit data at the same time.
The AJ71QC24(N)-R2 and A1SJ71QC24(N)-R2 can be set for each interface.
When the QC24(N) is started, full-duplex communications is set. The user can change the communications method to match the specifications of the external device.

POINT

Since half-duplex communications does not have to be set in the following cases, you do not have to read this section.

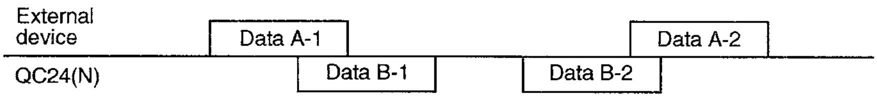
① When data is only transmitted or receive during non procedure protocol data communications
② When the AJ71QC24(N)-R4 is used.

14.5.1 Half-duplex communications

The following describes the differences between full-duplex communications and half-duplex communications.
Since the QC24(N) uses the communications method designated by the user to control PLC CPU communications, control by sequence program is unnecessary.

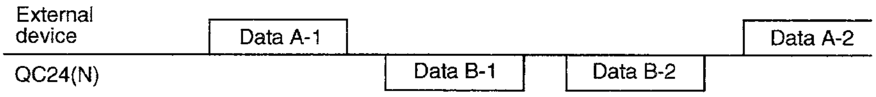
1 **Full-duplex communications**

This communication method uses telephone conversation format image to communicate data with the opposite station.
The QC24(N) can receive data while transmitting data to the external device.
It can also transmit data while receiving data from the external device.



2 **Half-duplex communications**

This communications method uses transceiver conversation format image to communicate data with the opposite device.
If the QC24(N) receives data from the external device while transmitting data to the external device, it controls data transmission and reception according to "Simultaneous transmission priority/nonpriority setting".
The QC24(N) does not transmit data while it is receiving data from the external device.



14.5.2 Data transmit and receive timing

Half-duplex communications uses the QC24(N) RS-232C interface CD and RS signals to control communications.
If the external device can transmit and receive data according to ON/OFF of the QC24(N) RS and CD signals as shown below, half-duplex communications is possible.

RS signall .... Turned ON/OFF by the QC24(N) as shown below.
When data is transmitted from the QC24(N), this signal is turned ON. At the end of transmission, this signal is turned OFF.

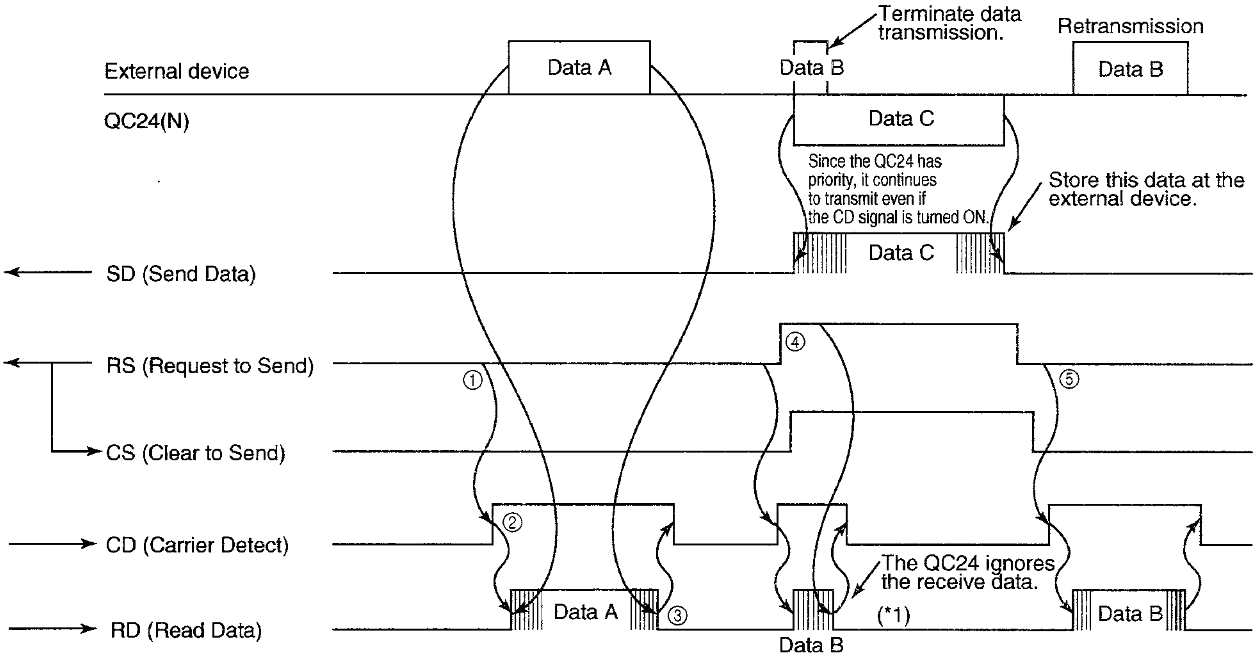
CD signal .... Turn this signal ON and OFF at the external device as shown below.
When transmitting data from the external device, turn this signal ON. When transmission is complete, turn this signal OFF.

The following describes the half-duplex communications data transmit and receive timings by QC24(N) CD signal and RS signal.

1 Timing when transmitting data from external device

Transmit data by controlling the QC24(N) CD signal according to the "simultaneous transmission priority/nonpriority" value set to the QC24(N) buffer memory.

(a) When QC24(N) designated "priority"

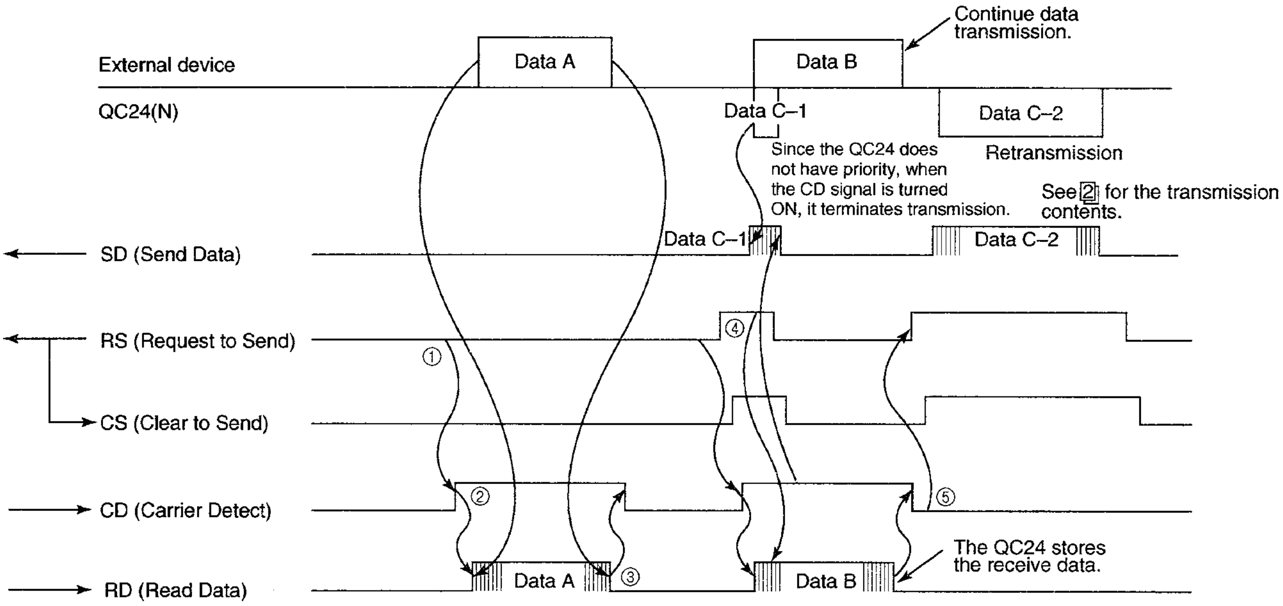


① When receiving data, check the RS signal. If the RS signal is OFF, turn ON the CD signal. If the RS signal is ON, wait until it is turned OFF, then turn ON the CD signal.
② Transmit data after the CD signal is turned on.
③ At the end of data transmission, turn OFF the CD signal.
④ If the RS signal was turned on during data transmission, terminate data transmission and receive the data. (Simultaneous transmission generated)
⑤ After transmission from the QC24(N) is complete, retransmit all the data terminated at step ④.

*1 Take the following measures between the communicating devices as a countermeasure against ignoring of the receive data by the QC24(N).

- Transmit and receive a response message in reply to data transmission
- Retransmit the data not transmitted due to response message time-out check or generation of a time-out error (external device)

(b) When QC24(N) is designated "nonpriority"



The contents of ④ and ⑤ below are different from those of item (a).

① When transmitting data, check the RS signal. If the RS signal is OFF, turn ON the CD signal. If the RS signal is ON, wait until it is turned OFF, then turn ON the CD signal.

② After the CD signal is turned ON, transmit the data.

③ At the end of data transmission, turn OFF the CD signal.

④ The external device will continue to transmit data to the QC24(N) even if the RS signal is turned ON during data transmission. (Simultaneous transmission generated)

⑤ At the end of transmission from the external device, data is transmitted from the QC24(N) to the external device. (See $\boxed{2}$.)

Notes

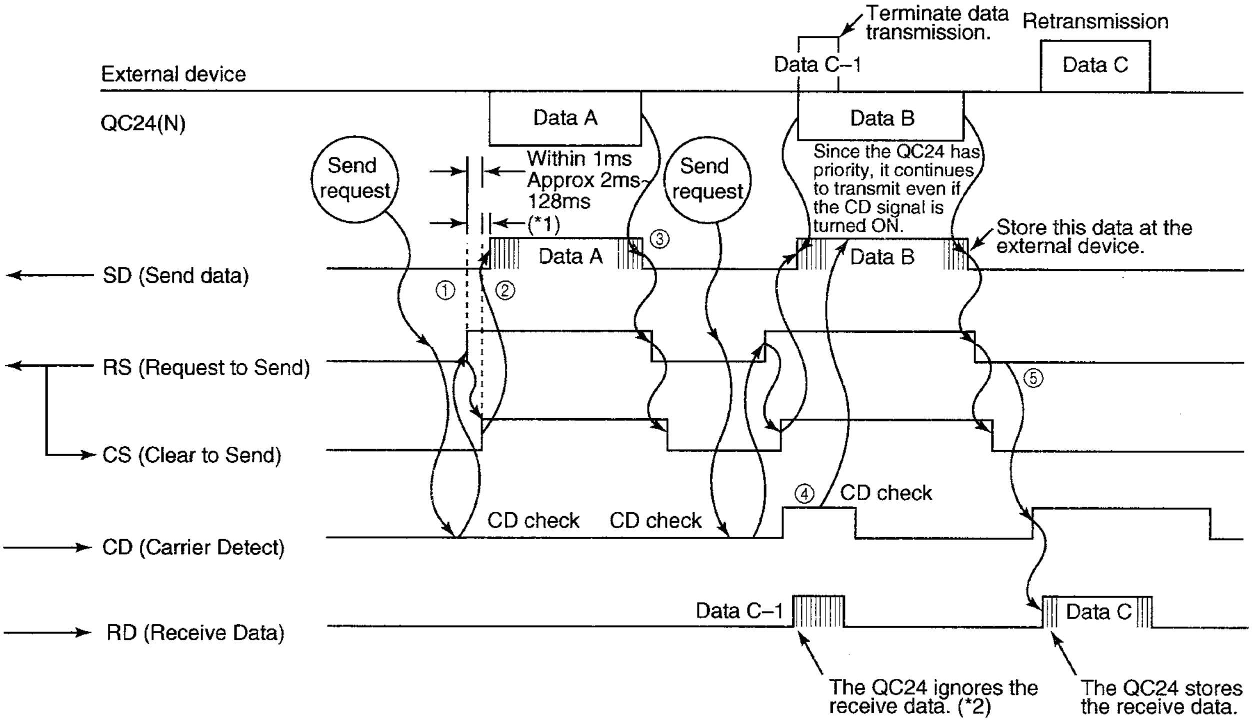
When using the DTR/DSR transmission control function described in Section 14.3 to control communications, transmit data from the external device to the QC24(N) as described below in both cases (a) and (b) above.

- When the QC24(N) DTR signal is turned OFF, terminate data transmission.
- When the QC24(N) DTR signal is turned ON after data transmission was terminated, restart data transmission (beginning from the terminated data).

2 Timing when data is transmitted from the QC24(N)

The QC24(N) RS signal is controlled and data is transmitted according to the "simultaneous transmission priority/nonpriority" value set to the QC24(N) buffer memory.

(a) When QC24(N) is designated "priority"



① When transmitting data, check the QC24(N) CD signal. If the CD signal is OFF, turn ON the QC24(N) RS signal.
If the CD signal is ON, wait until it is turned OFF, then turn ON the RS signal.

② After the RS signal is turned ON, transmit the data.

③ At the end of data transmission, turn OFF the RS signal.

④ If the CD signal is turned ON during data transmission, the QC24(N) continues to transmit data to the external device. (Simultaneous transmission generated)

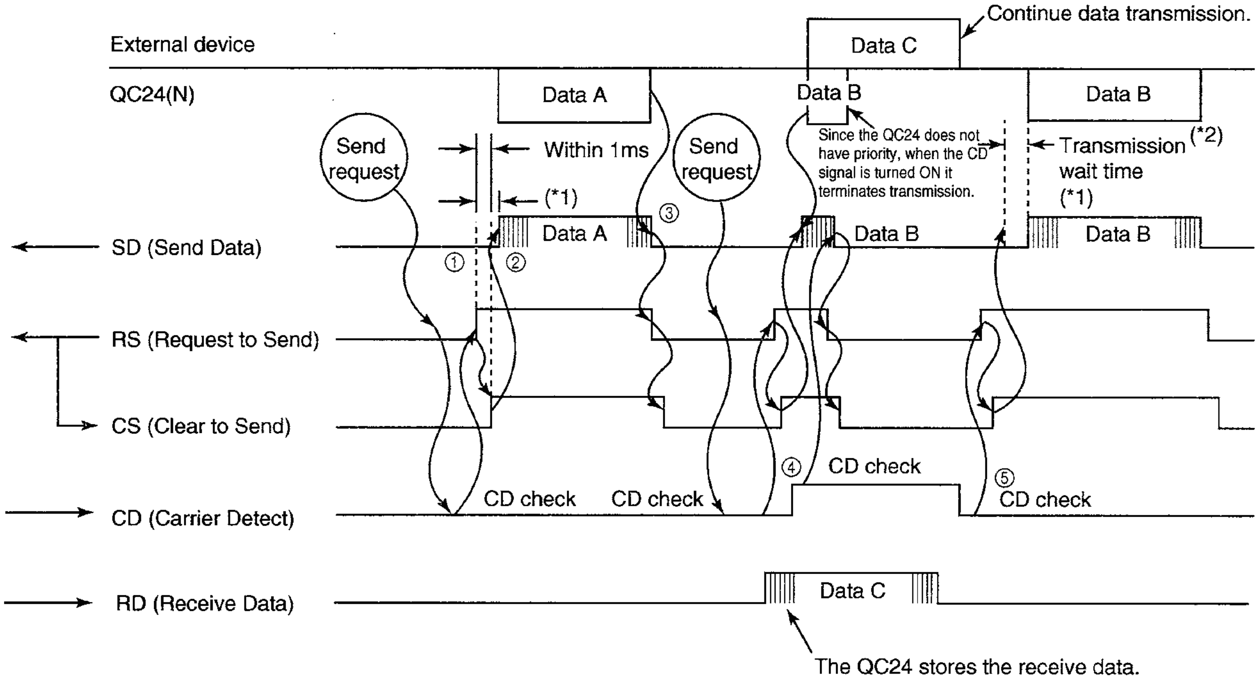
⑤ At the end of transmission from the QC24(N), transmit all the data terminated at step ④ from the external device to the QC24(N).

*1 The time from RS ON to the start of transmission depends on the data transmission rate. The higher the transmission rate, the shorter the time up to the start of transmission.

*2 Do the following between the communicating devices as a countermeasure against ignoring of the receive data by the QC24(N).

- Transmit and receive a response message in reply to data transmission.
- Retransmit the response message time-out check and time-out error data (external device).

(b) When QC24(N) designated "nonpriority"



The contents of ④ and ⑤ below are different from those of item (a).

① When transmitting data, check the QC24(N) CD signal. If the CD signal is OFF, turn ON the QC24(N) RS signal.
If the CD signal is ON, wait until it is turned OFF, then turn ON the RS signal.

② After the RS signal is turned ON, transmit the data.

③ At the end of data transmission, turn OFF the RS signal.

④ If the CD signal is turned ON during data transmission, terminate data transmission and turn OFF the RS signal and receive the data. (Simultaneous transmission generated)

⑤ At the end of transmission from the external device, transmit the data terminated at step ④ from the beginning or from the last data transmitted.

*1 The data size set to buffer memory addresses 99H/139H is not transmitted.

*2 Transmit from the beginning or from the data transmitted immediately before transmission was terminated, according to the contents set to buffer memory addresses 9AH/13AH.

Note

When using the DTR/DSR transmission control function described in Section 14.3, transmit data from the QC24(N) to the external device as shown below in both cases (a) and (b) above.

- When the QC24(N) DSR signal is turned OFF, terminate data transmission.
- When the QC24(N) DSR signal is turned ON after data transmission is terminated, restart data transmission (transmit from the terminated data).

14.5.3 Connector connections for half-duplex communications

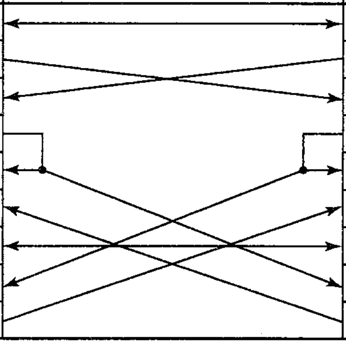
The following describes the functions of the connector that connects the QC24(N) and external device when half-duplex communications is used.
Connect the QC24(N) and external device based on (1) and (2) below.

(1) Connect the QC24(N) RS signal to any of the external device half-duplex communications signals (CS, DSR, or CD).

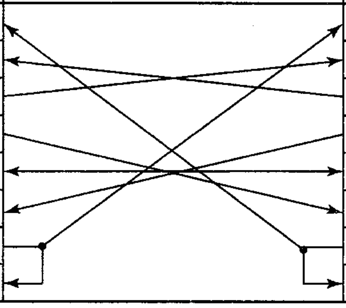
(2) Connect the QC24(N) CD signal to one of the external device half-duplex signals (RS or DTR).

(3) The half-duplex communications described in this section cannot be performed when an RS-232C–RS-422 converter is used.

(Connection example)
① When the QC24(N) is a 25-pin connector

QC24(N)		**Cable connection and signal direction**	**External device**
Signal name	**Pin No.**		**Signal name**
FG	1		FG
SD (TXD)	2		SD (TXD)
RD (RXD)	3		RD (RXD)
RS	4		RS
CS (CTS)	5		CS (CTS)
DSR (DR)	6		DSR (DR)
SG	7		SG
CD	8		CD
DTR (ER)	20		DTR (ER)

② When the QC24(N) is a 9-pin connector

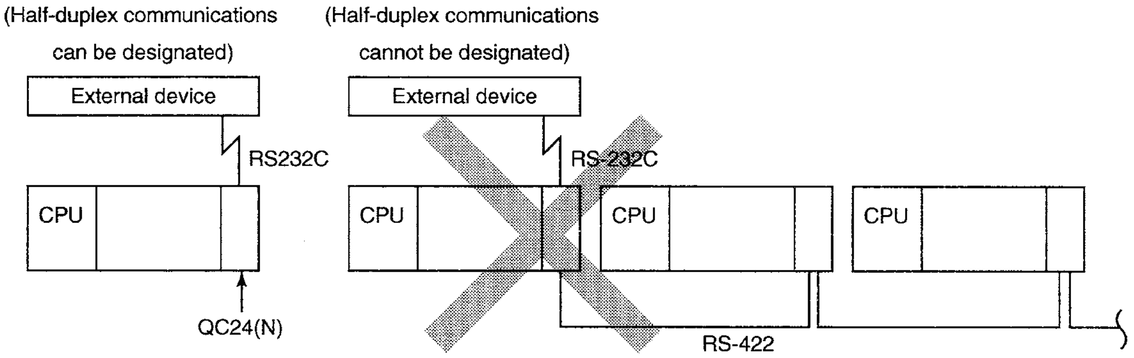
QC24(N)		**Cable connection and signal direction**	**External device**
Signal name	**Pin No.**		**Signal name**
CD	1		CD
RD (RXD)	2		RD (RXD)
SD (TXD)	3		SD (TXD)
DTR (ER)	4		DTR (ER)
SG	5		SG
DSR (DR)	6		DSR (DR)
RS (RTS)	7		RS (RTS)
CS (CTS)	8		CS (CTS)

14.5.4 Half-duplex communications precautions

The following describes the precautions to be observed when using half-duplex communications.

1 **Half-duplex communications system configuration and functions**

Half-duplex communications is possible only with a system that connects the PLC CPU and external device in a 1: 1 configuration.



2 **Agreement and confirmation between external device and PLC CPU**

Agree and confirm the following items between the external device and the PLC CPU.

① Whether or not half-duplex communications can be performed by QC24(N) RS signal and CD signal.

② QC24(N) RS signal and CD signal ON/OFF timing

③ QC24(N) and external device data transmission timing

④ RS-232C cable connection method

3 **Transmission control**

When the transmission control functions described in Section 14.3 are used, DC code control DC1/DC3 transmission control and DC1/DC3 reception control cannot be used with half-duplex communications. Therefore, do not designate them.

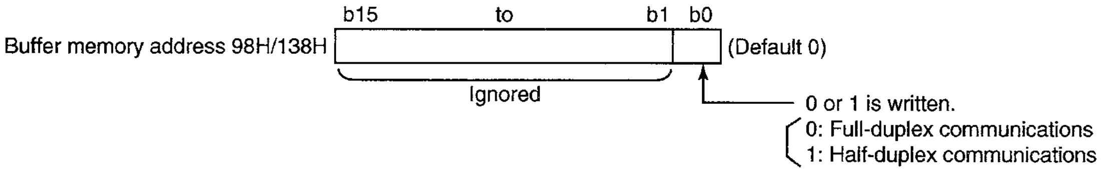
14.5.5 Buffer memory initialization

When data is communicated by switching from full-duplex communications to half-duplex communications, writing to the buffer memory special applications area is necessary.
The following describes writing to the buffer memory special applications area when changing the communications method.

1 Initialization area

The half-duplex communications parameters are stored to the buffer memory as shown below.

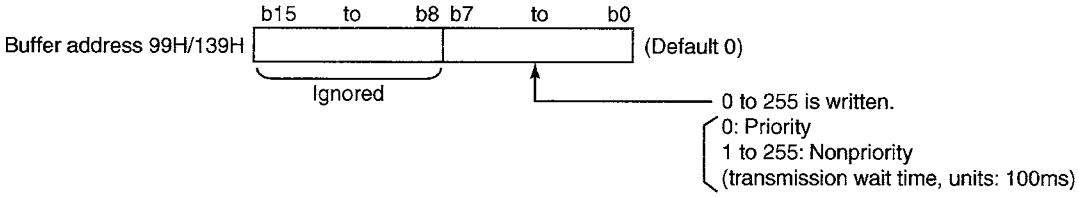
① RS-232C communications method designation area (addresses: 98H/138H)



② Simultaneous transmission priority/nonpriority designation area (addresses: 99H/139H)

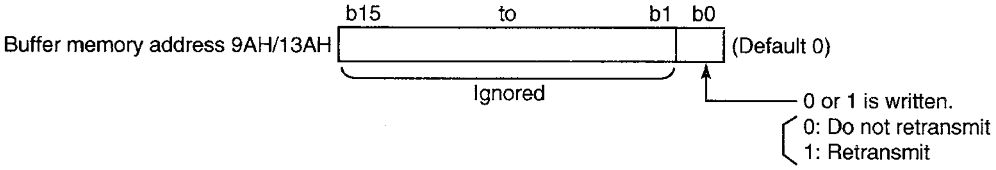
Designates if transmission from the QC24(N) is to be continued ("priority") or terminated ("nonpriority") when the external device and QC24(N) started data transmission at the same time during half-duplex communications.

The value "1" to "255" designated when "nonpriority" is designated is the transmission wait time until data is actually transmitted after data transmission can be restarted.



③ Transmission restart method designation area (addresses: 9AH/13AH)

This setting is valid when "half-duplex communications" + "nonpriority" are set at ① and ② above. It designates if the terminated message is to be transmitted from the beginning ("retransmit") or continued ("do not retransmit") when the QC24(N) restarts a transmission that was terminated at the start of simultaneous transmission by the external device and the QC24(N).



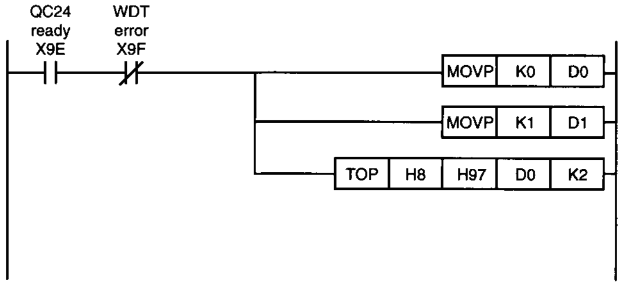
④ RS-232C CD terminal check setting area (addresses: 97H/137H)

With half-duplex communications, [Check CD terminal] (set value: 0) is set as described in Section 4.7.2 3.

2 Communications method modification sample program

The following shows a sample program that uses the TO instruction to change the CH1 communications method.
(QC24(N) I/O signals 80H to 9FH)

① When QC24(N) transmission has priority during half-duplex communications



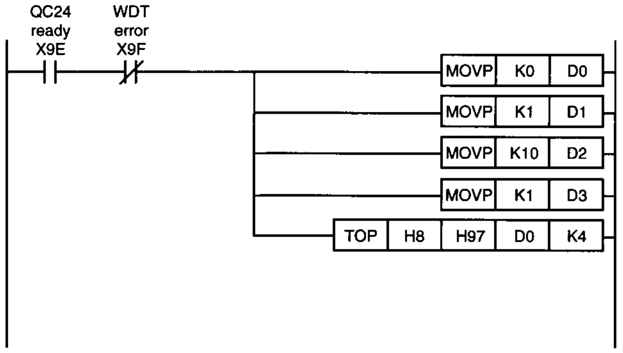
Sets "Check CD terminal".

Sets "Half-duplex communications".

Writes the set values.

Buffer memory addresses 99H and 9AH are made the default value.

② When QC24(N) transmission does not have priority during half-duplex communications



Sets "Check CD terminal".

Sets "Half-duplex communications".

Sets "Nonpriority" (Transmission wait time: 1000ms)

Sets "Retransmit". *1

Writes the set values.

*1 When "Do not retransmit" is designated, writing to address 9AH is unnecessary.

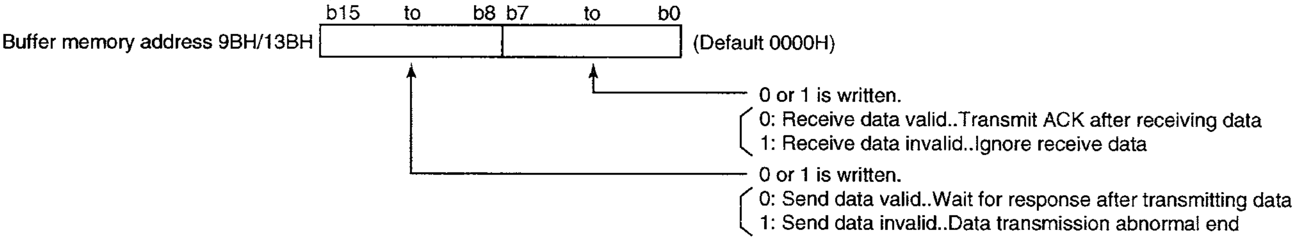
14.6 Invalidating Data During Simultaneous Transmission

This setting designates how the QC24(N) send data and receive data are to be handled when the QC24(N) and external device transmit simultaneously during data communications between the QC24(N) and external device using the bidirectional protocol.
This setting can be made for each interface.
When the QC24(N) is started, both the send data and receive data are valid. This can be changed to invalid to conform to the user specifications.
Before initializing the buffer memory special applications area as described in this section, check Section 12.5 " QC24(N) Processing During Simultaneous Transmission".

This section only describes the initialization method that invalidates the data during simultaneous transmission.

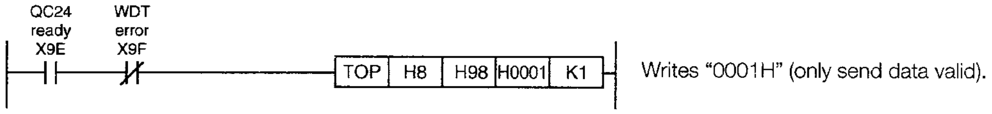
1 Simultaneous transmission data valid/invalid designation area (addresses: 9BH/13BH)

Handling of the QC24(N) send and receive data during simultaneous transmission is stored to buffer memory addresses 9BH/13BH as shown below.



2 Simultaneous transmission data valid/invalid designation sample program

The following shows a sample program that designates send data valid, receive data invalid when simultaneous transmission is generated while CH1 is communicating data.
(QC24(N) I/O signals 80H/9FH)



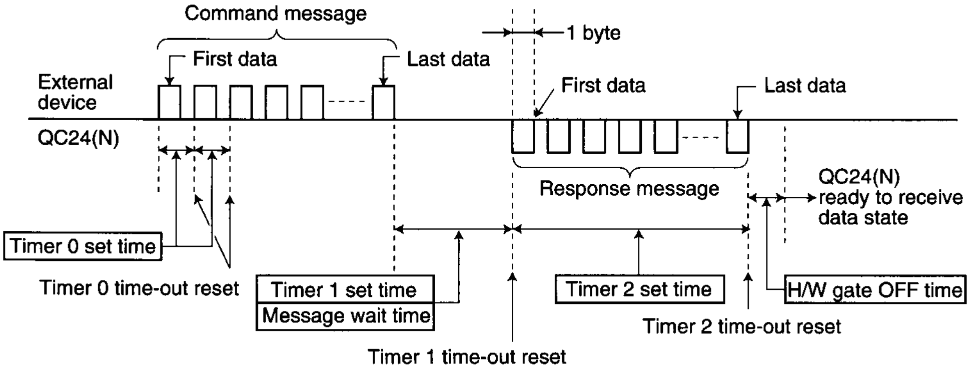
14.7 Changing the Data Communications Watchdog Timers

The watchdog timers are timers used by the QC24(N) to monitor the receiving interval between each byte when receiving data from the external device, the PLC CPU processing time, and the time it takes to transmit to the external device.
The watchdog timers can be set for each QC24(N) interface. The QC24(N) uses the time set by the user to control data transmission to and reception from the external device.
Set the watchdog timers to match the specifications of the opposite device.

The QC24(N) watchdog timers are shown below.

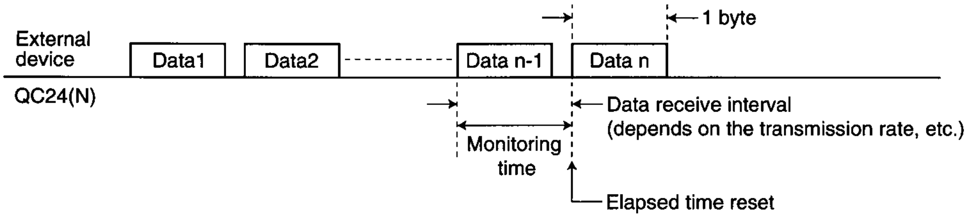
	Watchdog timer	QC24(N) default value	Protocol that can monitor the time			Notes
			Dedicated	Non procedure	Bidirectional	
①	No reception watchdog timer (timer 0)	0 bytes	o	o	o	Transmission time for the set number of bytes. (depends on the transmission rate)
②	Response watchdog timer (timer 1)	5 seconds	o	—	o	For bidirectional protocol, this time is valid for transmission only.
③	Transmission watchdog timer (timer 2)	3 minutes	o	—	o	—
④	Message wait time	0ms	o	—	—	No wait time

(Example) Data communications using a dedicated protocol



14.7.1 No reception watchdog timer (timer 0) setting

The no reception watchdog timer (timer 0) is the time for clearing the QC24(N) status when the QC24(N) was placed into the data receive wait state by trouble in the external device.
The QC24(N) monitors the reception interval in byte units at the start of data reception from the external device and ends monitoring when the preset last data is received and repeats this operation.
The following describes the no reception watchdog timer (timer 0) setting method, etc.



POINT

(1) The no reception watchdog timer (timer 0) performs monitoring, always regarding 1 byte as 12 bits, independently of the transmission setting. (For the guideline for changing the no reception watchdog timer (timer 0) setting, refer to Notes in this section.)

(2) If the non-reception monitoring time (timer 0) was changed in the sequence program, execute any of the following to enable the changed value.
- Mode switching (Refer to Chapter 18.)
- PLC CPU information clear (Refer to Section 19.6.)

1 QC24(N) operation by no reception watchdog timer (timer 0)

Monitors the receive interval in byte units and returns the elapsed time to 0 each time one byte is received.
At time-out, the QC24(N) performs the following processing.

(a) Data communication using dedicated protocol

- Stores the error code to the dedicated protocol transmission error code storage area for the objective interface (buffer memory addresses 25AH, 26AH).
- Transmits a NAK message to the external device and enters the command message receive wait state.

(b) Data communications using non procedure protocol

① Data communications not using user frames

- Passes the receive data up to time-out to the QC24(N).
- Stores the error code to the data receive result storage area for the objective interface (buffer memory addresses 258H, 268H) and turns ON the receive error detection signal (Xn4, XnB) and waits to receive the next data.

② Data communications using user frames

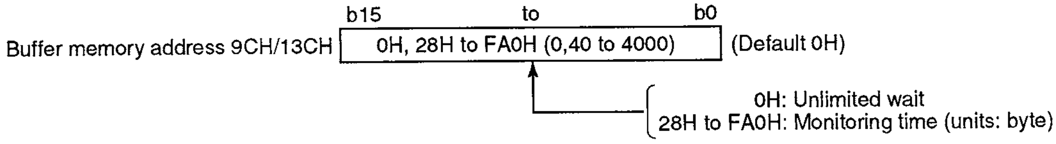
- When designating the trailer frame, an arbitrary part of data in the area starting from the start of the reception of the current message until timeout is read into the QC24(N), and the data in the trailer frame area is ignored (deleted).
- Stores the error code to the data receive result storage area for the objective interface (buffer memory addresses 258H, 268H), turns ON the receive error detection signal (Xn4, XnB), and waits to receive the next data.

(c) Data communications using bidirectional protocol

- Ignores the receive data from the start of reception of the current message to time-out.
- Stores the error code to the receive result storage area for the objective interface (buffer memory addresses 258H, 268H).
- When the receive data continuation complete signal (Yn1, Yn8) is turned ON, transmits a NAK message to the external device and waits to receive the next data.

2 No reception watchdog timer (timer 0) designation area (addresses: 9CH/13CH)

The no reception watchdog timer (timer 0) is the transmitted character count (byte count) corresponding to the data transmission rate set in the objective interface. It is stored to buffer memory addresses 9CH/13CH as shown below.
Adjust and set the character count according to the specifications of the external device.



* When setting other than the above, it will operate as if FA0H is set.

Notes

① Guideline for changing the no reception watchdog timer (timer 0)
Set the no reception watchdog timer (timer 0) to the following bytes or more.

$$\text{No reception watchdog timer (timer 0)} = 1 + \frac{Td \times Vbps}{12000}$$

(Rounded up to the 1 place.)

Td : Maximum delay time in output processing of external device (ms)
Vbps : Transmission speed (bps)

(Example) Example of calculating the no reception watchdog timer (timer 0)

- Transmission speed (Vbps) : 9600bps
- Maximum delay time in output processing of external device (Td) : 50ms

$$\text{No reception watchdog timer (timer 0)} = 1 + \frac{50 \times 9600}{12000} = 41 \text{ bytes}$$

In this case, the actual watchdog time is:

$41 \text{ bytes} \times 12^{*1} / 9600 \times 1000 = 51.25\text{ms}$

*1 Number of transmitted bits for 1 byte (fixed)

② Guideline for changing the no reception watchdog timer (timer 0) when data communications are made with the external device via the RS-422/485 interface of the Q series C24

Set the no reception watchdog timer (timer 0) to the following bytes or more.

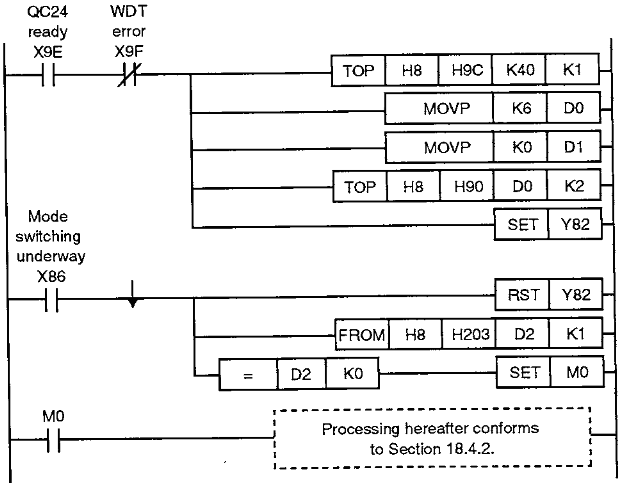
$$\text{No reception watchdog timer (timer 0)} = 1 + \frac{(\text{Td} + \text{T1}) \times \text{Vbps}}{12000}$$

(Rounded up to the 1 place.)

Td : Maximum delay time in output processing of external device (ms)
T1 : H/W gate OFF time on external device side (ms)
Vbps: Transmission speed (bps)

3 No reception watchdog timer (timer 0) setting sample program

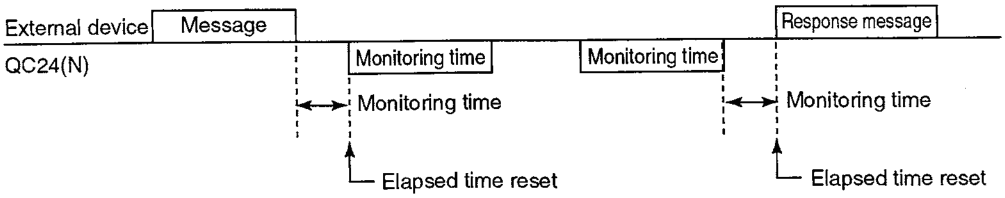
The following shows a sample program that sets the CH1 no reception watchdog timer (timer 0) to 40 bytes.
(QC24(N) I/O signals 80H to 9FH)



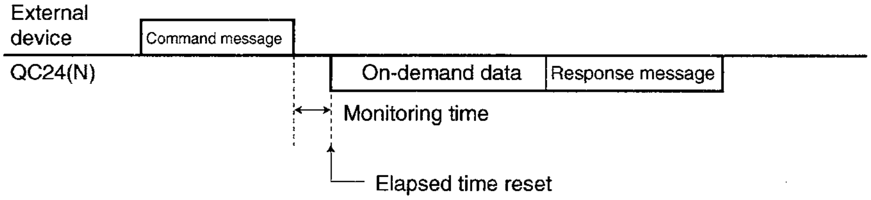
Writes "40" (bytes).
Sets "6" (non procedure protocol mode No.). (See Chapter 18 for more information.)
Sets "0" (the switching transmission specifications match the switch setting).
Writes the mode switching designation contents.
Sets the mode switching request signal.
Turns OFF the mode switching request signal.
Reads the mode switching error contents.
When D2 is nonzero, checks and processes the error contents as described in Sections 19.1.3 and 19.4.

14.7.2 Response watchdog timer (timer 1) setting

The response watchdog timer (timer 1) clears the receive wait state of the device that receives the response message when trouble in the device that received the message does not return a response message (result) to the opposite device.
When the QC24(N) receives a message from the external device, it monitors the PLC CPU processing time up to the start of transmission of the response message to the external device.
When a message was received, it monitors the external device processing time up to the start of reception of the response message from the external device.
The following describes the response watchdog timer (timer 1) setting method, etc.



* If on-demand data is transmitted before a response message during data communications using a dedicated protocol, the time up to the start of transmission of the on-demand data is monitored.



1 QC24(N) operation by response watchdog timer (timer 1)

(a) When response watchdog timer (timer 1) set to 0ms

After receiving a message, the QC24(N) does not monitor the time up to the start of transmission of a response message to the external device, but waits infinitely.
After transmitting a message, the QC24(N) does not monitor the time up to the start of reception of the response message from the external device, but waits infinitely.

(b) When response watchdog timer (timer 1) is set to 100 ms or longer

After receiving a message, the QC24(N) monitors the time up to the start of transmission of a response message to the external device and returns the elapsed time to 0 at the start of transmission.
After transmitting a message, the QC24(N) monitors the time up to the start of reception of the response message from the external device and returns the elapsed time to 0 at the start of reception.
At time-out, the QC24(N) performs the following processing.

① Data communications using a dedicated protocol

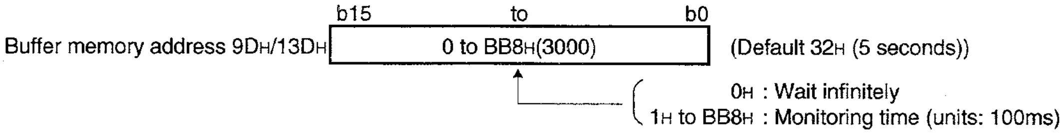
- Stores the error code to the dedicated protocol transmit error code storage area (buffer memory addresses 25AH, 26AH) for the objective interface.
- Transmits a response message (NAK message) to the external device and waits to receive the next command message.

② Data communications using bidirectional protocol

- Stores the error code to the data transmission result storage area (buffer memory addresses 257H, 267H) for the objective interface and turns on the transmission abnormal end signal (Xn1, Xn8).
  If the send request signal (Yn0, Yn7) is turned OFF, turns OFF the transmission abnormal end signal (Xn1, Xn8) and waits to receive the next message.
- While waiting to transmit a response message, the QC24 does not check the response watchdog timer.

2 Response watchdog timer (timer 1) designation area (addresses: 9DH/13DH)

The response watchdog timer (timer 1) is stored to buffer memory addresses 9DH/13DH as shown below.
During data communications using a dedicated protocol, set the response watchdog timer to the message wait time, or longer. *1



*1 The message wait time is designated at the following places.

- A compatible frame : Designated in command message.
- QnA (extension) frame : Designated by buffer memory addresses 11EH,
  QnA simplifed frame 1BEH (See Section 14.7.4.)

POINTS

When changing the response watchdog timer (timer 1) default value (5 seconds), observe the following precautions.

(1) Data communications using a dedicated protocol
In any of the following cases make the default value the message wait time described in Section 14.7.4, or longer.

(a) When designating the monitor conditions with the following functions, set the maximum time matched to system operation.

- Word units random read (See Section 6.2.6.)
- Device memory monitor (See Section 6.2.9.)

(b) Access other than (a) above

① When accessing a station connected (including multidrop link) to an external device, set the default value to the following value, or longer.
Maximum number of scans required to process the command used × connected station scan time

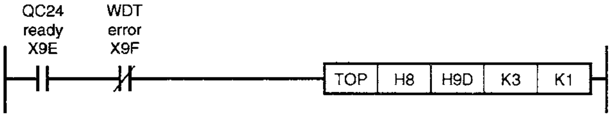
② When accessing another station over a data link system or network system, set the default value to infinity or the following time, or longer.
Maximum number of scans required to process the command used × communications time
When setting the default value to infinity, check the external device response wait time and initialize the QC24(N) transmission sequence when time-out is generated. (See Sections 6.1.4 1 and 6.10.)

* See Appendix 3 for the number of scans required by processing.
See Section 5.7 3 4 for the communications time.,

(2) Data communications using bidirectional protocol
Set the default value to the following time, or longer.
(Sequence scan time × 2) + 100 ms

3 Response watchdog timer (timer 1) setting sample program

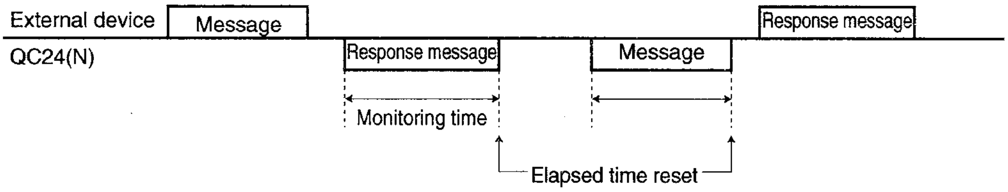
The following shows a sample program that sets the CH1 response watchdog timer (timer 1) to 300 ms
(QC24(N) I/O signals 80H to 9FH)



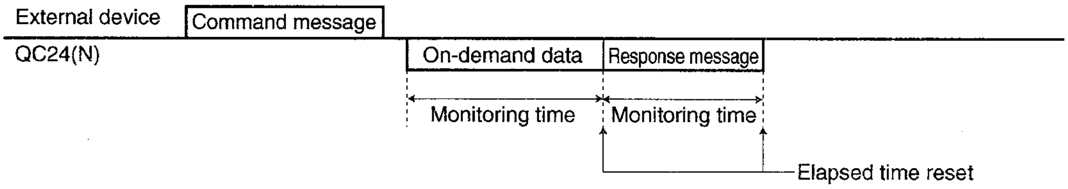
Writes "3" (300ms).

14.7.3 Transmit watchdog timer (timer 2) setting

The transmit watchdog timer (timer 2) clears the wait state when the QC24(N) that is to transmit a command message or response message (response) has entered the transmission end wait state due to trouble in the external device.
When the QC24(N) transmits a message, it monitors the wait time up to the end of transmission of the message.
When the QC24(N) received a message from the external device, it monitors the wait time up to the end of transmission of the response message.
The following describes the transmit watchdog timer (timer 2) setting method, etc.



* If on-demand data is transmitted before a response message during data communications using a dedicated protocol, each time is monitored.



1 QC24(N) operation by transmit watchdog timer (timer 2)

(a) When transmit watchdog timer (timer 2) is set to 0ms
The time until transmission of the control message or response message is not monitored.
If the QC24(N) cannot transmit, it waits infinitely.

(b) When transmit watchdog timer (timer 2) is set to 100 ms or longer
Monitors the time from completion of control message or response message transmission preparations to the end of transmission and returns the elapsed time to 0 at the end of transmission.
At time-out, the QC24(N) performs the following processing.

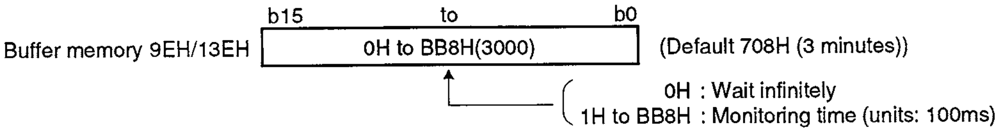
① Data communications using a dedicated protocol
- While waiting for the end of transmission of the response message, the QC24(N) stores the error code to the data transmission result storage area (buffer memory addresses 257H, 267H) for the objective interface.
  The QC24(N) enters the state in which it waits to receive the next command message without sending a response message (NAK message) to the external device.
- During on-demand data transmission, the QC24(N) stores the error code to the on-demand execution result storage area (buffer memory addresses 256H, 266H) for the objective interface.
- If transmission was terminated midway in either of the cases above, the QC24(N) does not transmit the remaining data.

② Data communications using bidirectional protocol
- While waiting for the end of transmission of a message, the QC24(N) stores the error code to the data transmission result storage area (buffer memory addresses 257H, 267H) for the objective interface and turns on the transmission abnormal end signal (Xn1, Xn8).
  When the send request signal (Yn0, Yn7) is turned off, the QC24(N) turns off the transmission abnormal end signal (Xn1, Xn8) and waits for the next message send request.
  If message transmission was terminated midway, the QC24(N) does not transmit the remaining data.

- If waiting for the end of transmission of a response message, the QC24(N) stores the error code to the data receive result storage area (buffer memory addresses 258H, 268H) for the objective device.

2 Transmit watchdog timer (timer 2) designation area (addresses: 9EH/13EH)

The transmit watchdog timer (timer 2) is stored to buffer memory addresses 9EH/13EH as shown below.



POINT

The transmission watchdog timer (timer 2) monitors the transmission termination time when the following states are generated.

- When DTR/DSR signal control is used and the DSR signal is turned off (See Section 14.3.1.)
- When DC1/DC3 receive control is used and DC3 is received (See Section 14.3.2 1.)
- When the RS-232C interface signal is turned OFF (See Section 3.2.1.)

Note

Criteria when changing the transmit watchdog timer (timer 2) setting
Find the transmit watchdog timer (timer 2) time from the maximum delay time of external device message receive processing or response message transmission processing and the transmission time/byte (t) and change the set value.

- Number of bytes transmitted/second (n) = Transmission rate/number of transmit bits/byte
- Transmission time/byte (t) = 1000 (ms)/number of bytes transmitted/second (n)
- Watchdog timer (timer 0) = (Maximum external device processing delay time) + (transmission time/byte (t) × transmit byte count)

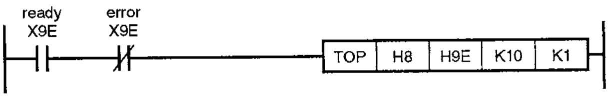
100 ms units truncated

Under the following conditions, the transmit watchdog timer (timer 2) is set to 300 ms

- Transmission rate : 9600BPS
- Number of transmit bits/byte : 11 (start bit: 1, data bits: 8, stop bits: 2)
- Maximum processing delay time : 200 ms
- Transmit byte count : 3 bytes

3 Transmit watchdog timer (timer 2) setting sample program

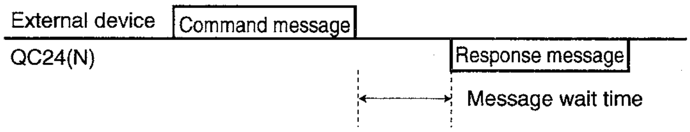
The following shows a sample program that sets the CH1 transmit watchdog timer (timer 2) to 1000 ms.
(QC24(N) I/O signals 80H to 9FH)



Writes "10" (1 second) to 9EH.

14.7.4 Message wait time setting

The message wait time is used during data communications using a dedicated protocol.
It is the time for an external device that cannot receive the data immediately after it has been transmitted.
When the QC24(N) transmits a response message in reply to a command message received from the external device, transmission of the response message is delayed by the message wait time, or longer.
The following describes the message wait time setting method, etc. for data communications using QnA (extension) frames or QnA simplified frame. (For A compatible frames, the message wait delay time is designated in the command message.)



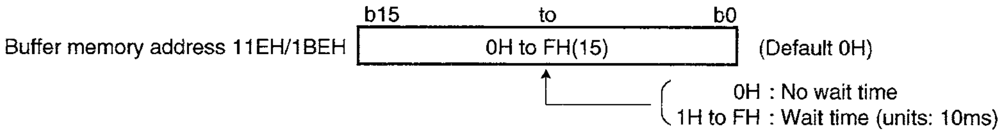
1 **QC24(N) operation by transmission wait time**

① When message wait time is 0ms
If a response message can be transmitted, the QC24(N) immediately transmits the response message. A transmission wait time is not set.

② When the message wait time is 10 ms. or longer
If a response message can be transmitted, and the message wait time after reception of the command message has elapsed, the QC24(N) transmits the response message.

2 **Message wait time designation area (addresses: 11EH/1BEH)**

The message wait time is stored to buffer memory addresses 11EH/1BEH as shown below.

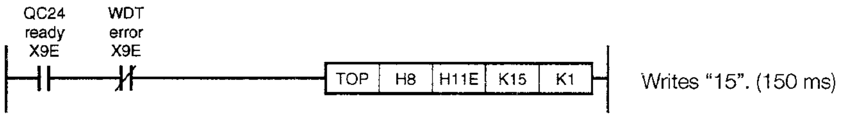


POINTS

(1) If the external device that must wait a certain time before it can receive a response message after a command message was transmitted, set the message wait time as described above. Especially, for data communications with an external device connected to the QC24(N) RS-422/485 interface, set the message wait time to the external device hardware gate OFF time, or longer.
(2) The message wait time described here is the time for data communications using QnA (extension) frames and QnA simplified frame.

3 **Message wait time setting sample program**

The following shows a sample program that sets the CH1 message wait time to 100 ms (QC24(N) I/O signals 80H to 9FH)



14.8 Changing the Transmit and Receive Areas and Received Data Read Conditions

This setting changes the user area of the buffer memory that stores the data to be transmitted to and received from the external device and the non procedure protocol data reception conditions (hereafter called "receive conditions").

- Transmit area modification
- Receive area modification
- Receive conditions modification

The transmit and receive areas and the receive conditions can be set for each QC24(N) interface. When the QC24(N) is started, the area and receive conditions of the parameters described in Section 14.1 are set. The areas and receive conditions can be changed according to the user specifications. Initialize the buffer memory as described in this section after checking the set contents by referring to the Reference Section given in the table below.
This section describes the transmit and receive areas and receive conditions initialization method, etc.

The following shows the buffer memory that sets (changes) the transmit and receive areas described in this section and the related data communications functions, etc.

Setting Item	**Set Buffer Memory Name**	**Address**		**QC24(N) Default Value**	**Related Protocol**		**Reference Section**
		CH1	**CH2**		**Non procedure**	**Bidirec-tional**	
Transmit area modification	Transmit buffer memory head address designation area	A2H	142H	CH1: 400H to 5FFH CH2: 800H to 9FFH	○	○	9.4.1
	Transmit buffer memory length designation area	A3H	143H				12.4.1
Receive conditions modification	Receive end data count designation area	A4H	144H	1FFH (511 words)	○	—	9.3.1
	Receive end code designation area	A5H	145H	0D0AH (CR, LF)			
Receive area modification	Receive buffer memory head address designation area	A6H	146H	CH1: 600H to 7FFH CH2: A00H to BFFH	○	○	9.3.2
	Receive buffer memory length designation area	A7H	147H				12.3.1

POINT

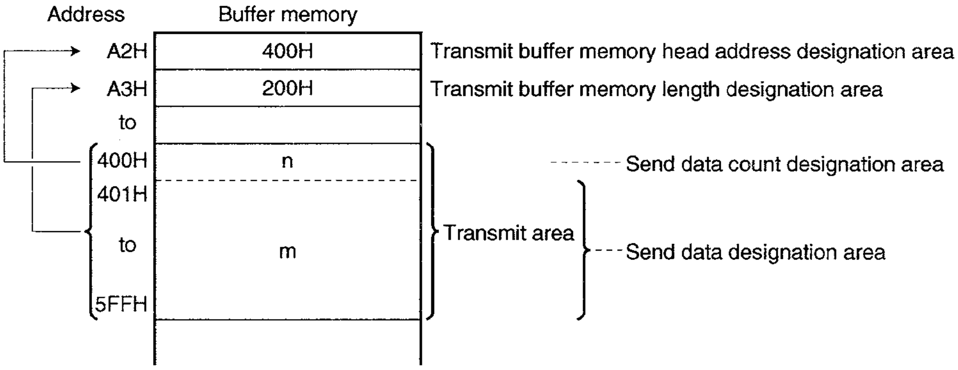
When using the following functions at the same time, do not duplicate allocation of the user areas of the buffer memory that stores the send data and receive data handled by the functions used.

- Dedicated protocol buffer memory read/write function........ See Section 6.3.
- Dedicated protocol on-demand function............................. See Section 6.9 and Chapter 7.
- Non procedure protocol transmit and receive functions ...... See Sections 9.3.2 and 9.4.1.
- Bidirectional protocol transmit and receive functions........... See Sections 12.3.2 and 12.4.1.

14.8.1 Transmit area setting

This setting sets the buffer memory transmit area used by the PLC CPU to write the send data count and send data during data communications to the external device using the non procedure protocol or bidirectional protocol.

(Example) Default value CH1 set contents

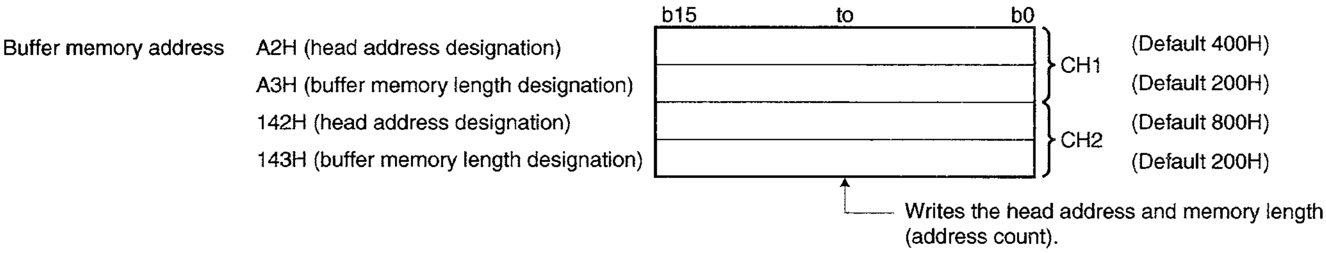


1 **Initialization area**

The setting data for transmit area setting are stored to the buffer memory as described below.

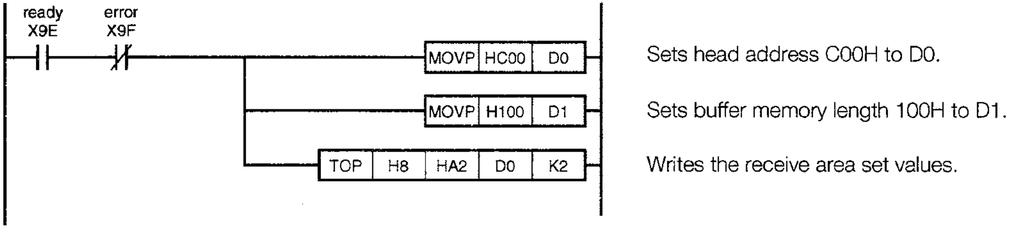
① Transmit buffer memory head address designation area (addresses: A2H/142H)
This area designates the head address of the area used as the transmit area in the buffer memory user area.

② Transmit buffer memory length designation area (addresses: A3H/143H)
This area designates the length of the area used as the transmit area in the buffer memory user area.



2 **Transmit area modification sample program**

The following shows a sample program that changes the transmit area used in CH1 data communications to the addresses C00H to CFFH area.
(QC24(N) I/O signals 80H to 9FH)



Sets head address C00H to D0.

Sets buffer memory length 100H to D1.

Writes the receive area set values.

POINTS

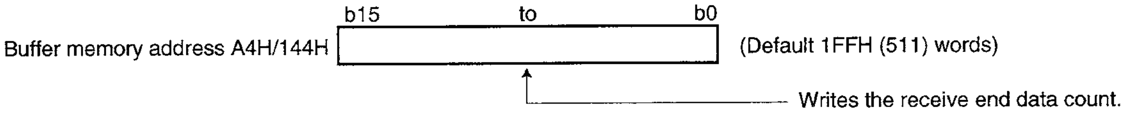
(1) Since buffer memory addresses 0H to 3FFH and 1B00H to 1FFFH are the special applications area, do not include them in the designation.
(2) Also include the send data designation area in buffer addresses A3H/143H.

14.8.2 Receive end data count setting

This setting sets the word count/byte count when receiving fixed length data when the non procedure protocol is used to receive data from the external device.
The value set to the word/byte designation area (see Section 14.4) determines the set value units (words/bytes).

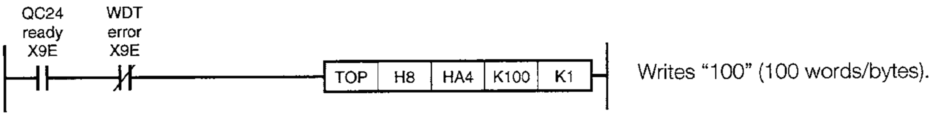
1 **Receive end data count designation area (addresses A4H/144H)**

The receive end data count is stored to buffer addresses A4H/144H as shown below.



2 **Receive end data count modification sample program**

The following shows a sample program that changes the CH1 data communications receive end data count to 100.
(QC24(N) I/O signals 80H to 9FH)

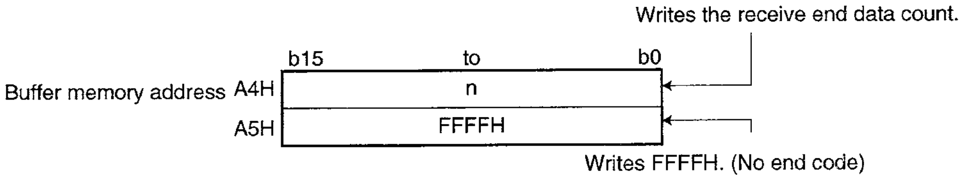


POINTS

(1) Designate the receive end data count within the following range.
(Word units) Receive end data count ≤ Receive data storage area address count
(Byte units) Receive end data count ≤ (Receive data storage area address count) x 2
If the receive end data count is larger than the value given above, the size of the receive data storage area is assumed to be the receive end data count.

(2) For ASCII-BIN conversion, the receive end data count is designated by byte count after the receive data is converted to binary data.

(3) When reading fixed length receive data without the end code described in Section 14.8.3, set the receive end data count as follows.
(CH1)



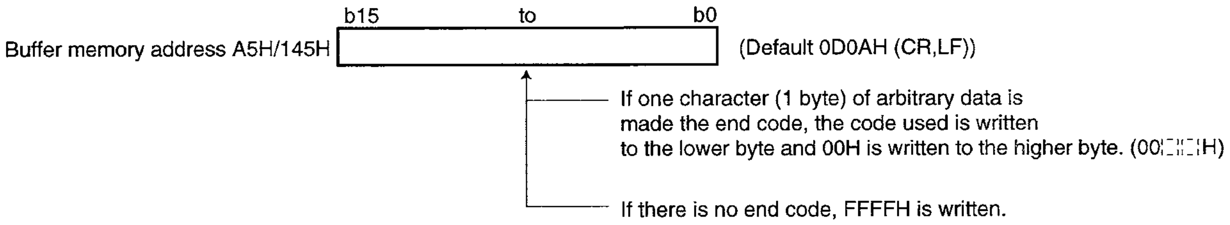
(4) The set value for the number of data that has been received can be changed at the timing indicated in the remarks found at Section 14.8.3, as well as when the QC24 (N) starts up.

14.8.3 Receive end code setting

This setting sets the code of the data to be received last when the non procedure protocol is used to receive variable length data from the external device.

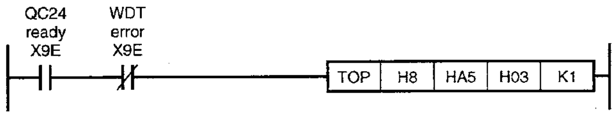
1 Receive end code designation area (addresses A5H/145H)

The receive end code is stored to buffer addresses A5H/145H as shown below.



2 Receive end code modification sample program

The following shows a sample program that changes the CH1 data communications receive end code to 03H (ETX).
(QC24(N) I/O signals 80H to 9FH)



Writes "03H" (ETX).

POINTS

(1) An arbitrary 1 byte code within the 00H to FFH range can be set as the end code to be changed.
For ASCII-BIN conversion, the end code is set by code after the receive data was converted to binary data.

(2) If an end code is not set, the fixed length reception by receive end code described in Section 14.8.2 is possible.

(3) Do not set the same code as the additional code by receive transparent code designation in buffer memory addresses 120H/1C0H as the receive end code for non protocol data reception.

(4) The set value for the reception completion code can be changed at the timing indicated in the remarks, as well as when the QC24 (N) starts up.

Remark

In addition to the time when the QC24(N) starts up, the set values for the number of data received and reception completion code can also be changed after data communication has commenced if the timing is as indicated below.

The following explains the timing and procedures when changing module restrictions or set values in a case where data reception processing is continued by changing the set values for data reception during no-procedure protocol after data communication commences.

(1) Target QC24(N)
After data communication has commenced, the set values for the reception completion code and number of data received can be changed and data reception processing continued with respect to all QC24(N)s.

(2) Set values that can be changed
Of the initial settings via the QC24(N) buffer memory, the set values given below can be changed after data communication has commenced:
- Number of data received (buffer memory address: A4H, 144H)
- Reception completion code (buffer memory address: A5H, 145H)

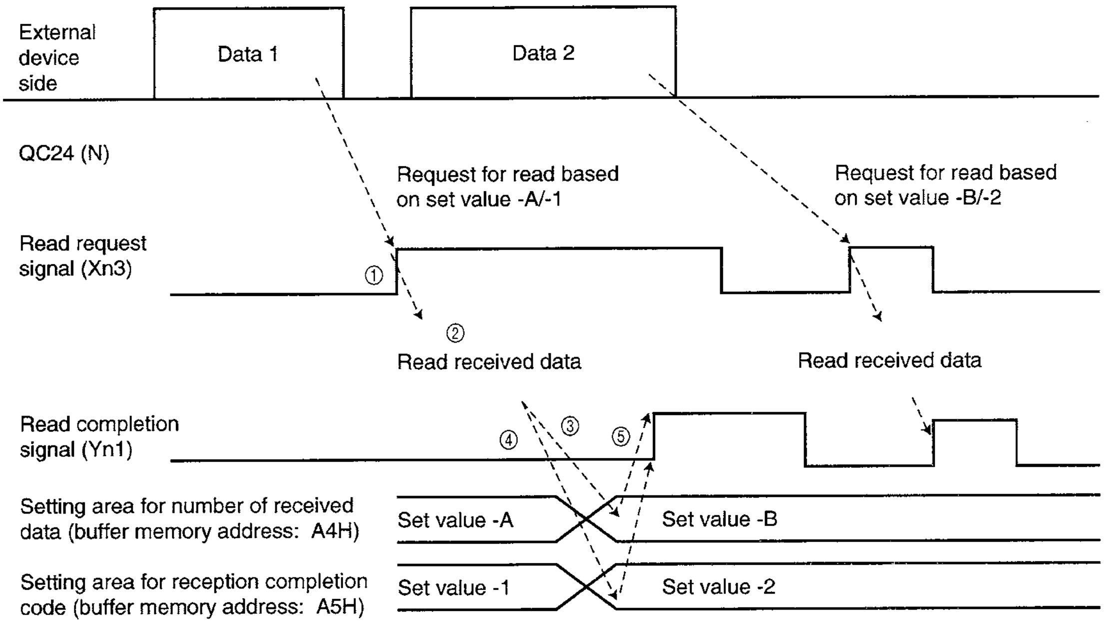
* Previously, the set values could only be changed when the QC24(N) started up (when the QC24(N) ready signal (X $_{(n+1)}$ E) turned from OFF to ON).
Changes to initial set values other than those indicated above should be done when the QC24(N) starts up as before.

(3) Timing and procedure for changing set values

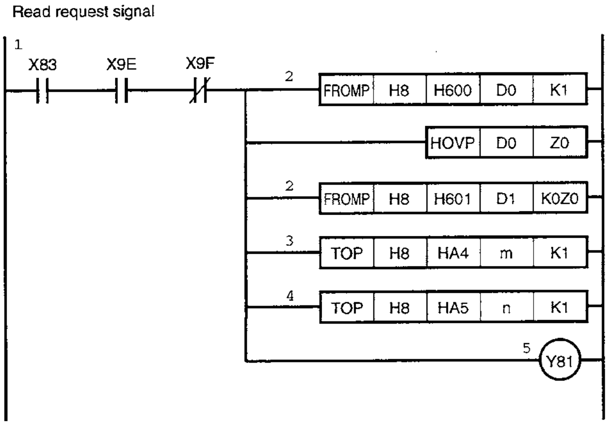
① Timing of changes
When changing the number of data received or the reception completion code after data communication has commenced, make the changes when the status of the I/O signals between the PLC CPU involved in the reading of received data and the QC24(N) is as indicated below:
- Reception-data read request signal (Xn3, XnA): ON
- Reception-data read completion signal (Yn1, Yn8): OFF

② Procedure for changing
When the reception-data read request signal from is turned on when data is received from an external device, the reception-data read completion signal is turned ON after the following have been performed:
- Read the received data.
- Change the set values for the reception completion code and number of data received.

(Example) When reading the data received by the CH1-side interface



(Program example: QC24(N) I/O signal 80H to 9FH)



Read the number of data received.

Read the amount of received data that was specified in the number of data received.

Change the set value for the number of data received as required.

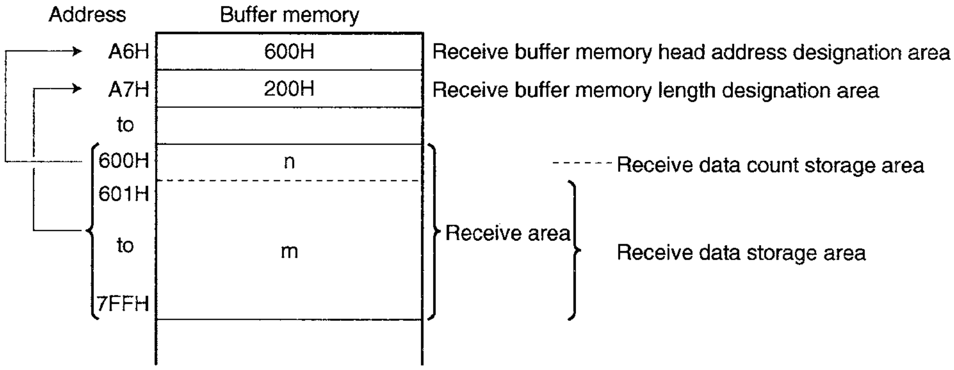
Change the set value for the reception completion code as required.

Turn the read complete signal ON.

14.8.4 Receive area setting

This setting sets the buffer memory receive area that stores the receive data count and receive data for the PLC CPU to read the data received from the external device when non procedure protocol or bidirectional protocol is used to receive data from the external device.

(Example) Default value CH1 set contents

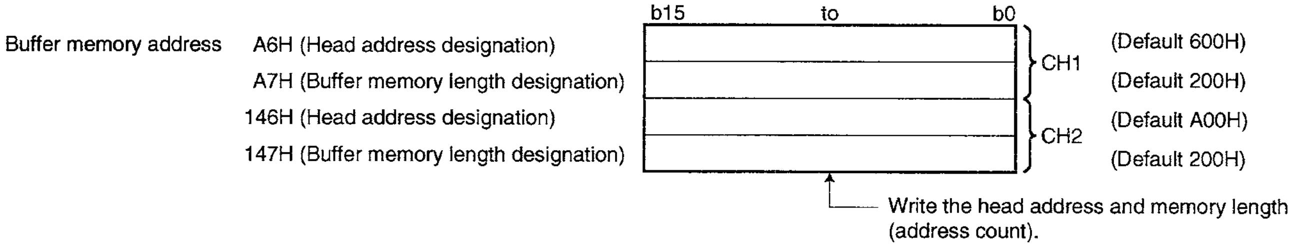


1 **Initialization area**

The setting data for receive area setting are stored to the buffer memory as described below.

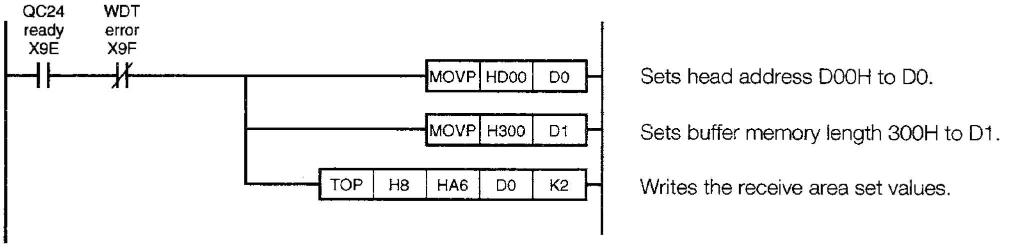
① Receive buffer memory head address designation area (addresses: A6H/146H)
This area designates the head address of the area used as the receive area in the buffer memory user area.

② Receive buffer memory length designation area (addresses: A7H/147H)
This area designates the length of the area used as the receive area in the buffer memory user area by number of addresses.



2 **Receive area modification sample program**

The following shows a sample program that changes the receive area used in CH1 data communications to addresses D00 to FFFH.
(QC24(N) I/O signals 80H to 9FH)



POINTS

(1) Since buffer memory addresses 0H to 3FFH and 1B00H to 1FFFH are the special applications area, do not include them in the designation.
(2) Include the receive data count storage area in buffer memory addresses A7H/147H.

14.9 Setting Receive User Frames

This setting sets the user frames used to receive data from the external device by non procedure protocol using user frames.
The user frames to be used are set by registration No. to the QC24(N). They are also set according to the transmission scheme (whether or not there are header frames and trailer frames) when the external device transmits the user frame part.

1 Receive user frame setting method rules

(a) A receive user frame is set with a header frame and trailer frame as one set, regardless of whether or not a header frame and trailer frame are transmitted.
(If the external device does not transmit one of these frames, the untransmitted frame No. is set as [0] (not set).)

(b) With the non procedure protocol, up to four sets of header frame and trailer frame combinations can be set. (See section 11.2.1.)
* Within the set combinations (max. four combinations), if there is a combination that designates the header frame, designate header frames also in the other combinations.

If there is a combination that designates the trailer frame without designating the header frame, header frames may not be designated in all other combinations.

(c) Of the combinations (max. four combinations) that designate header frame and trailer frame, if there is a combination that designates the header frame, set the following buffer memory starting with the first one using the shown priority.

① Each frame No. of combination that designation a header frame and trailer frame
② Each frame No. of combination that designation a header frame but does not designation a trailer frame

(d) When two or more combinations are set, the registration data cannot designate the header frame of the same list/same frame No.
The trailer frame can be designated.

(e) When data communications starts, the QC24(N) receives the user frame of the combination set by the user.

(Example)
When the QC24(N) receives the header frame of any combination from the external device, it sends a receive data read request to the PLC CPU as soon as it receives the trailer frame of that combination.

(f) Set the receive user frame with the following user frame registration frame No. (See Section 16.1)

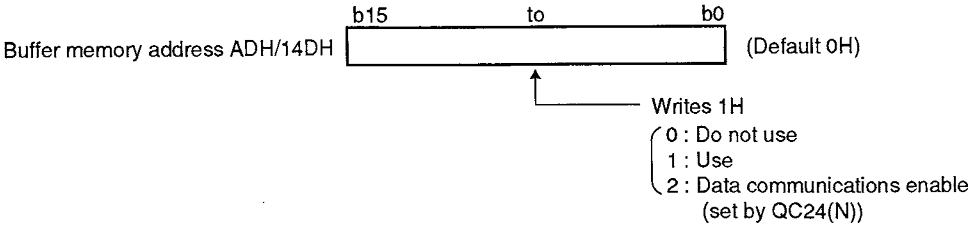
① Default frame No.: 1H to 3E7H
② User frame registered in QC24(N) EEPROM No.: 3E8H to 4AFH
③ User-registered frame No. registered to QC24(N) buffer memory: 8001H to 801FH

(g) As the user-registered frame for data reception by the non procedure protocol, do not designate (set) the user-registered frame containing the data of the additional code by receive transparent code designation at buffer memory address 120H/1C0H.

2 Initialization area

The setting data for user frame data reception is stored to the buffer memory as shown below.

(a) User frame use designation area (addresses: ADH/14DH)
To use user frames to receive data, designate [Use].

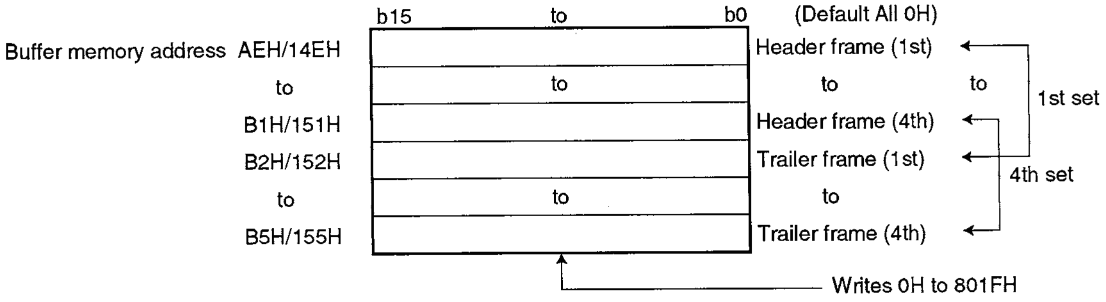


① Write "1" to the user-registered frame use designation area.

② After data reception using the user-registered frame is ready, "2" is written to the user-registered frame use designation area. (Set by the QC24N)

③ After the value of the user-registered frame use designation area has changed from "1" to "2", start data reception using the user-registered frame.
Until "2" is written to the user-registered frame use designation area, data transmission processing cannot be performed, either.

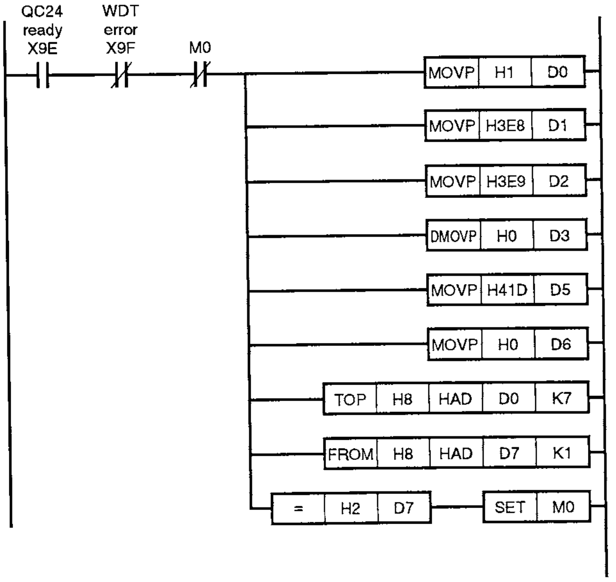
(b) Header frame No. designation area, trailer frame No. designation area (addresses: AEH to B5H/14EH to 155H)
The frame No. of the user frame to be used from among the user frames registered in the QC24(N) are designated by the combinations and priority shown in item (1).



0H (0) : Not designated
1H to 3E7H (1 to 999) : Designate the default frame. (Number registered in QC24(N) OS ROM)
3E8H to 4AFH (1000 to 1199) : Designate the user frame. (Number registered in EEPROM)
8001H to 801FH (-32767 to -32737) : Designate the user-registered frame. (Number registered in buffer memory)

3 Receive user frame setting sample program

The following shows a sample program that sets CH1 data receive user frames.
The receive user frames are the frames when only the two sets (header frame + trailer frame) and (header frame) are set.
(QC24(N) I/O signals 80H to 9FH)



Sets "Use user frames".

Sets header frame (1st) frame No. 3E8H.

Sets header frame (2nd) frame No. 3E9H.

Sets trailer frame (1st) frame No. 41DH corresponding to the header frame (1st).

Writes the frame No. of the receive user frames.

Reads if the QC24(N) has completed preparations. Sets the ready to receive flag (M0) when preparations are complete.

14.10 Setting the Transparent Code

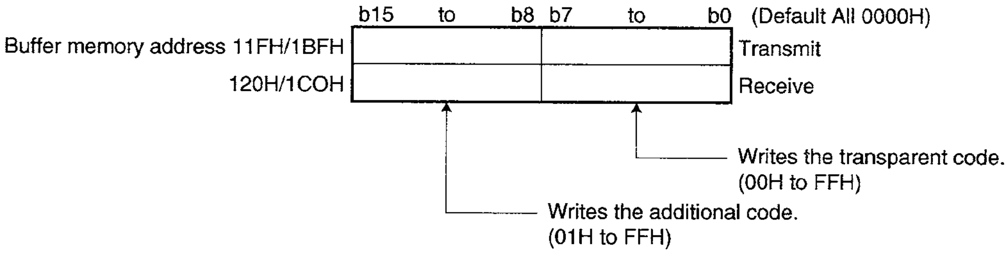
This settings sets the transparent code and additional code to handle the one byte external device transmission control data as user data when the QC24(N) uses the non procedure protocol or bidirectional protocol to exchange data with the external device.
Transparent and additional codes for transmission and reception (1 set each) can be set in the QC24(N).
Set them to match the specifications of the external device.

Initialize the buffer memory as described in this section after checking the QC24(N) processing and the codes that can be designated as described in the description of each protocol.
This section only describes the transparent code and additional code initialization method.

1 Initialization area

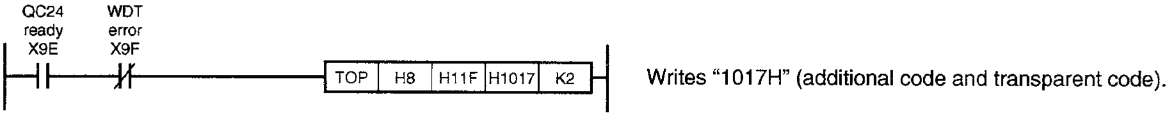
The setting data for transmission and reception is stored to the buffer memory as shown below.

① Transmit transparent code designation area (addresses: 11FH/1BFH)
② Receive transparent code designation area (addresses: 120H/1C0H)



2 Transparent code and additional code setting sample program

The following shows a sample program that sets the transparent code and additional code for CH1 data transmission and reception.
It sets the transparent code to 17H (ETB) and additional code to 10H (DLE)
(QC24(N) I/O signals 80H to 9FH)



POINT

If additional code data is received during non procedure protocol data reception, the QC24(N) does not assume that the one byte of data immediately following the additional code is data for the following control.

- Data that is received as user frame header frame and trailer frame (See Sections 16.1 and 16.2.)
- Receive end code data (See Section 9.3.1 1 (a).)
  Therefore, do not designate (set) codes of the data handled above as the receive additional code.

14.11 Communications Data ASCII-BIN Conversion

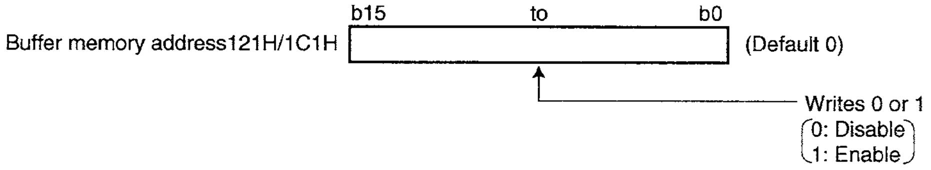
This setting sets ASCII-BIN conversion to transmit and receive ASCII code data (ASCII data) when using the non procedure protocol or bidirectional protocol to exchange data with an external device. Set it according to the specifications of the external device.
The PLC CPU converts the data as described below.

- Transmission..... Assumes that the data to be converted is binary data and converts it to ASCII data and transmits the ASCII data.
- Reception .... Assumes that the data to be converted is ASCII data and converts it to binary data and receives the binary data.

Initialize the buffer memory special applications area as described in this section after checking QC24(N) processing as described in the description of each protocol.
This section only describes initialization for ASCII-BIN conversion.

1 ASCII-BIN conversion designation area (addresses: 121H/1C1H)

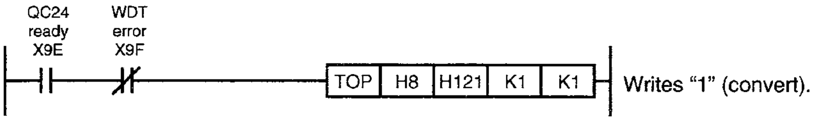
The ASCII-BIN conversion designation data is stored to buffer memory addresses 121H/1C1H as shown below.



2 ASCII-BIN conversion setting sample program

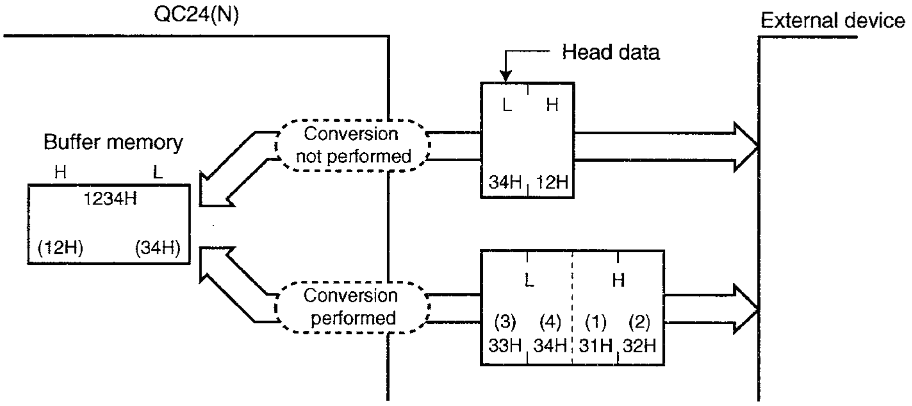
The following is a sample program that enables ASCII-BIN conversion of the CH1 data communications send and receive data.

(QC24 I/O signals 80H to 9FH)



Note

The following uses an example to show the contents of the send data when ASCII-BIN conversion is performed and is not performed when transmitting and receiving buffer memory data.



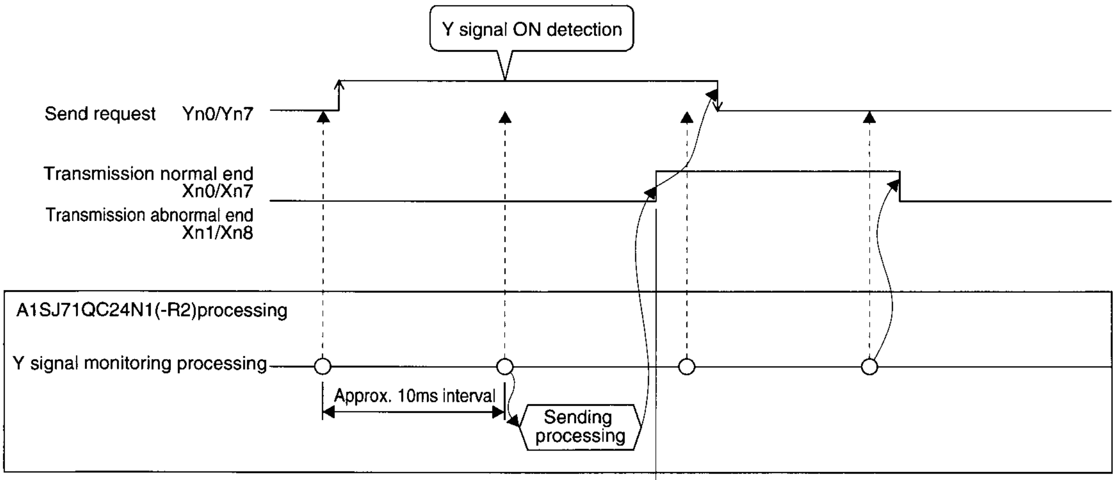
14.12 Setting of the Y Signal·Buffer Memory Monitoring Timing

Monitoring timing of the Y signal and buffer memory can be designated.

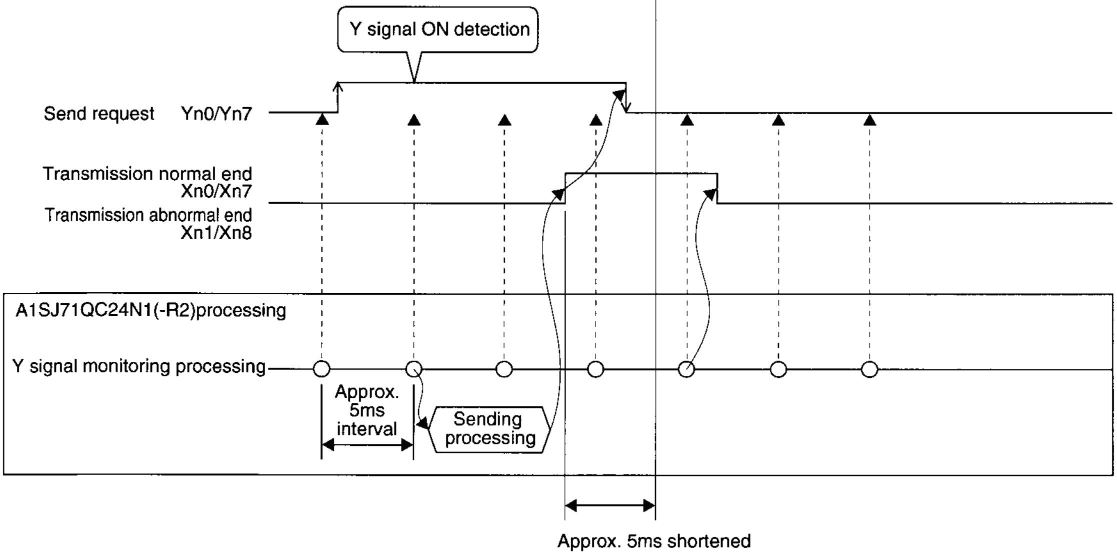
When "high-speed" is set, the delay of the Y signal request acceptance is shortened for approx. 5ms as compared to "QC24N compatible setting".

This function is available with A1SJ71QC24N1(-R2) only.

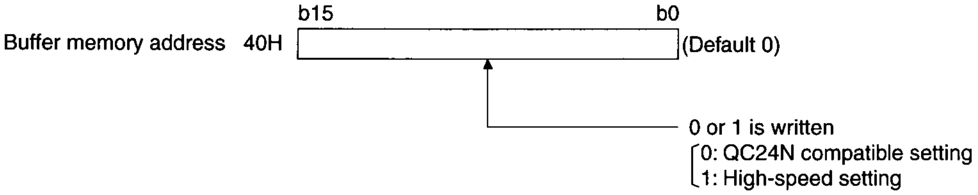
< QC24N compatible setting example : send request >



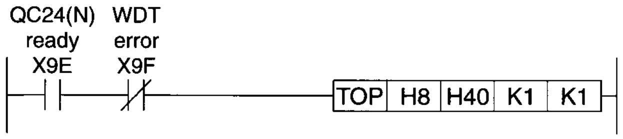
< High-speed setting example : send request >



(1) Y signal·buffer memory monitoring timing designation area (address: 40H)
Y signal·data for buffer memory monitoring timing designation is stored to buffer memory address 40H as shown below.



(2) Y signal·setting program example of buffer memory monitoring timing
Y signal·the following shows the sample program that sets buffer memory monitoring timing to "1: high speed setting".
(I/O signal 80H to 90H of the A1SJ71QC24N1(-R2))



Write "1" (high-speed setting)

MEMO

15. WRITING DATA COMMUNICATIONS PARAMETERS TO EEPROM

The values set to the buffer memory special applications area (including the parameters changed by the user) can be written to the QC24(N) EEPROM and used as the QC24(N) starting default values.
This section describes how to write the parameters set in the buffer memory special applications area to the QC24(N) EEPROM.
Register to the EEPROM when not conducting data communication with external equipment.

15.1 Writing Parameters to EEPROM

The table in Section 14.1 (see the Catalog column) shows the buffer memory special applications area whose contents can be cataloged to the QC24(N) EEPROM.
Before cataloging the parameters to the EEPROM, check that data communications with the external device is normal.
Cataloging the parameters to the EEPROM eliminates the need for a sequence program for the part whose buffer memory special applications area default value was changed.

Notes

(1) When the QC24(N) is started, one of the following parameters is written to the buffer memory special applications area.

① If parameters were not written to the EEPROM, the QC24(N) default values are written to the buffer memory special applications area.

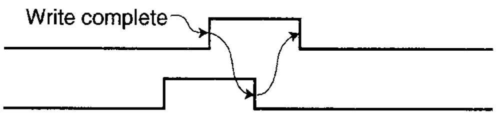
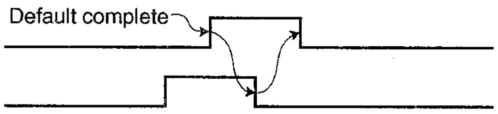
② If parameters were written to the EEPROM, if the system setting default request signal (Y (n+1) C) is turned ON when the QC24(N) is started (QC24(N) ready signal (X (n+1) E) = ON), the QC24(N) default values are written to the buffer memory special applications area.
If the system setting default request signal (Y (n+1) C) is turned OFF, the parameters written to the EEPROM are written to the buffer memory special applications area.

(2) Preset QC24(N) transmission specifications switch SW08 to ON (Enable).

15.2 I/O Signals for Handshake with PLC CPU and Buffer Memory

The I/O signals for handshake with the PLC CPU and the buffer memories used when writing the values set in the buffer memory special applications area to the QC24(N) EEPROM are shown below.
Both the CH1 and CH2 interfaces use the I/O signals for handshake with the PLC CPU and the buffer memories shown below.

1 I/O signals for handshake with PLC CPU

	I/O signal		Signal name	Device turned ON/OFF		Timing
	CH1	CH2		CPU	QC24(N)	
Writing of parameters	X (n+1) 9		System setting write complete		○	
	Y (n+1) 9		System setting write request	○		
Parameters initialization (buffer memory)	X (n+1) C		System setting default complete		○	
	Y (n+1) C		System setting default request	○		

Note

The following signals can also be used as I/O signals, in addition to the signals given above.
See Section 3.4 for a description of the PLC CPU I/O signals.

- QC24(N) ready signal (X (n + 1) E) .... Turned ON when the PLC CPU can access the QC24(N)
- Watchdog timer error signal (X (n + 1) F) ... Turned ON when the QC24(N) cannot operate normally

2 Buffer memory

Address and objective I/F		Name	Stored value
CH1	CH2		
220H (544)		EEPROM system setting write result storage	0 : Normal end Nonzero : Abnormal end (error code)

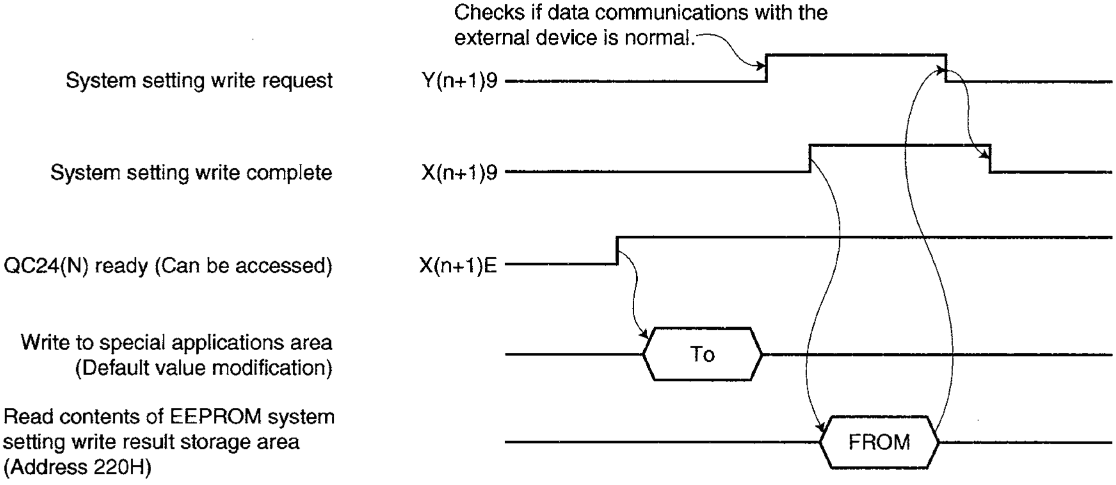
15.3 Writing the Data Communications Parameters to and Reading the Data Communications Parameters from EEPROM

This section describes how to write the values set in the buffer memory special applications area to the QC24(N) EEPROM and to return the values to the QC24(N) starting default values.

15.3.1 Writing the data communications parameters

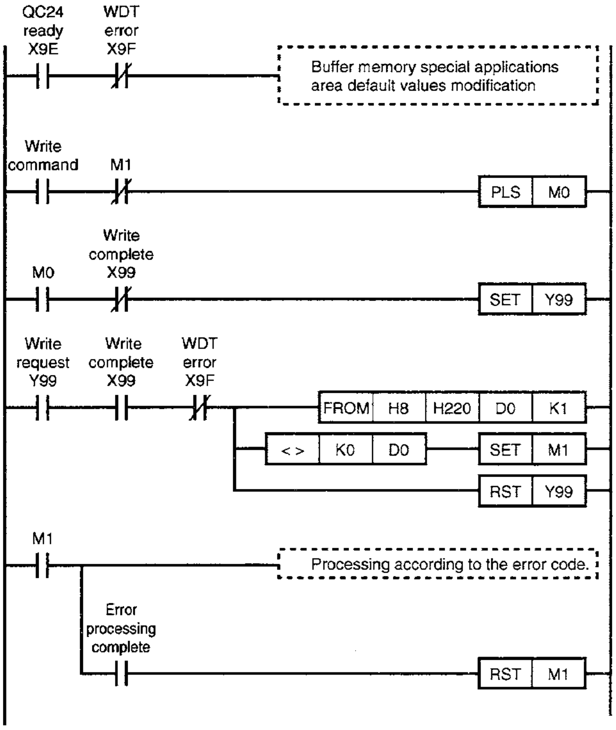
This section describes how to write the values set in the buffer memory special applications area to the QC24(N) EEPROM.
After writing is complete, the written parameters are used as the QC24(N) starting default values.

1 Write procedure



2 Sample write program

(QC24(N) I/O signals 80H to 9FH)



Changes the default values according to the data communications functions used.

Converts the write request to PLS.

Requests writing to EEPROM.

Reads the result at the end of writing.

If writing was abnormally ended (error code stored to D0), turns ON M1.

Clears the Write to EEPROM request.

Processing according to error code stored in D0 and Chapter 22.

15.3.2 Initialization of buffer memory special applications area

This section describes how to return the parameters set in the buffer memory special applications area to the QC24(N) default values.

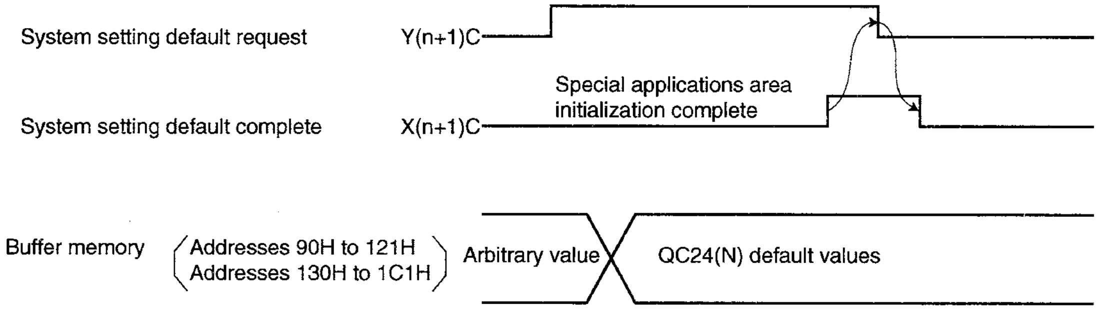
POINT

To return the parameters written to the QC24(N) EEPROM to the QC24(N) default values, proceed as follows.

① Initialize the buffer memory data communications parameters as described in this section.

② Write the data communications parameters as described in Section 15.3.1.

1 Initialization procedure



Note

To change the default values after the buffer memory special applications area was initialized, proceed as follows.

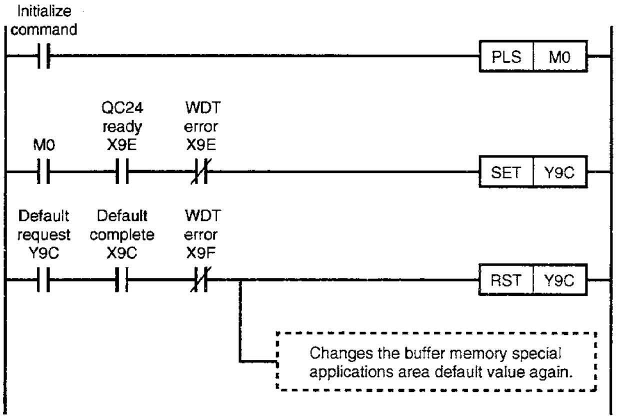
① Turn ON the system setting default complete signal (X (n+1) C).

② Turn OFF the system setting default request signal (Y (n+1) C). (System setting default complete signal: OFF)

③ Write the new parameter to the buffer memory special applications area whose default value is to be changed.

2 Sample initialization program

(QC24(N) I/O signals 80H to 9FH)



Converts the initialize command to PLS.

Requests buffer memory special applications area initialization.

Changes the default value according to the data communications function used. (Necessary part only)

16. WRITING DATA COMMUNICATIONS USER FRAMES TO EEPROM, ETC.

User frames are used to register some, or all, of the messages exchanged between an external device and the QC24(N) in advance and use them to check the send data or receive data.
The following functions can use QC24(N) user frames to transmit and receive data.

- Dedicated protocol on-demand function (See Chapter 7.)
- Non procedure protocol data transmit and receive functions (See Chapter 11.)

Data can be transmitted and received by writing the corresponding user frames to the QC24(N) in advance to match the data contents that are transmitted and received between the external device and the QC24(N).
This section describes the data that can be written, the data contents that are transmitted and received, and writing to the QC24(N) of user frames that can be used in data communications with the external device.
See the description of each function for a description of how each data communications function uses the user frames.

16.1 Kinds of User Frames and Data Contents that are Transmitted and Received

This section describes the kinds of user frames handled by the QC24(N) and the data contents that are transmitted and received.
The following two kinds of user frames are available. Either kind can be used.

User frame (Generic term)
- User frame (Frame described in Section 16.1.1.)
- Default frame (Frame described in Section 16.1.2.)

16.1.1 User frames written by the user

The following describes the written data, data contents that are transmitted and received, and how the QC24(N) handles user frames written the QC24(N) EEPROM or buffer memory by the user.

1 **General description**

User frames written by the user are frames that contain arbitrary data that matches the specifications of the external device. The data contents are selected by the user.

2 **User frame writing**

(a) Up to 231 user frames can be written, read, and deleted at the QC24(N).

① QC24(N) EEPROM (number that can be written:
Maximum 200, frame No.: 3E8H to 4AFH)

② QC24(N) buffer memory (number that can be written:
Maximum 31, frame No.: 8001H to 801FH)

(b) Up to 80 bytes (80 en characters) of data can be written as 1 user frame.

(c) User frames can include data for handling the variable data (sum check code, QC24(N) station No., etc.) shown in 4.

(d) User frames can be overwritten to the QC24(N) buffer memory. (The old contents are destroyed.)

3 Data that can be written as user frame

Up to 80 bytes of data can be written by combining 1 byte of data code 01H to FEH data and 2 bytes of data code FFH+00H to FFH data.

(a) One byte of data code (01H to FEH) data
This is the write code for transmitting and receiving the written code (01H to FEH) data.

(b) Two bytes of data code (FFH) + (00H to FFH) data
This is the write code for transmitting and receiving the variable data (check sum code, QC24(N) station No., etc.) shown in 4 as part of the user frame.
FFH is the write code of the first byte for handling variable data.

4 Variable data

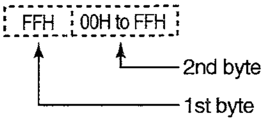
"Variable data" is the generic term for the following data.
These variable data can be handled as part of a user frame.

- Sum check code whose objective is an arbitrary range in the transmit and receive messages.
- QC24(N) station No.
- One byte data in data transmission (NULL: Code 00H)

  One byte of arbitrary data in data reception. (Used to handle an arbitrary byte of data as part of the user frame during receiving check by the QC24(N).)

(a) Variable data designation method

Variable data is designated by combining write code FFH and the data codes shown in the table below.
The sum check code, QC24(N) station No., and other variable data can be handled according to FFH of the first byte and 00H to FFH of the second byte.



(b) Variable data designation contents, data contents transmitted and received, and handling by the QC24(N)
The table below shows the write codes FFH+00H to FFH combinations for handling variable data, the data contents that are transmitted and received, and how the QC24(N) handles the data.
Combinations other than those shown in the table cannot be written.

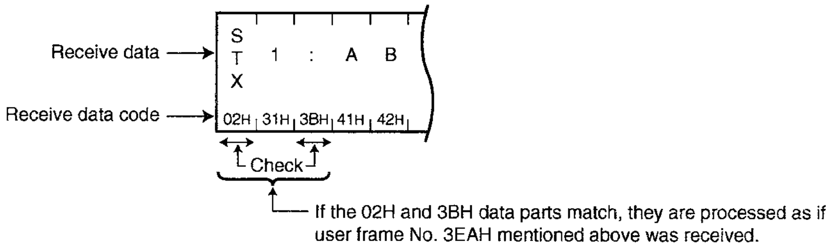
Variable data write code		Data contents transmitted and received/QC24(N) handling		Transmit and receive order
1st byte	2nd byte			
FFH	00H	Transmission : Transmits the data code 00H (NUL) data. Reception: Skips the given part (1 byte) of the receive user frame. (Skips the check and performs receive processing.)		—
	01H	Transmits and receives the station No. set in the QC24(N) station No. switch as 1-byte binary data (00H to 1FH).		—
	EEH	Transmits and receives a sum check code that excludes the send/receive data (message) user frame (1st header frame). *1	Transmits and receives the lower 2 bytes of the calculated sum check as 2-byte binary code.	Transmitted and received in (L) (H) order.
	F0H		Transmits and receives the lower byte of the calculated sum check as 1-byte binary code.	—
	F1H		Converts the lower byte of the calculated sum check to 2-digit ASCII code and transmits and receives the ASCII code.	Transmitted and received from the most significant digit.
	F3H		Converts the lower 4 bits of the calculated sum check to 1digit ASCII code and transmits and receives the ASCII code.	—
	F4H	Transmits and receives a sum check code that includes the send/receive data (message) user frame (header frame). *1	Transmits and receives the lower 2 bytes of the calculated sum check as 2-byte binary code.	Transmitted and received in (L) (H) order.
	F6H		Transmits and receives the lower byte of the calculated sum check as 1-byte binary code.	—
	F7H		Converts the lower byte of the calculated sum check to 2-digit ASCII code and transmits and receives the ASCII code.	Transmitted and received from the most significant digit.
	F9H		Converts the lower 4 bytes of the calculated sum check to 1digit ASCII code and transmits and receives the ASCII code.	—
	FFH	Transmits and receives the data code FFH data (1 byte).		—

*1 During data communications using a user frame that handles a trailer frame, the QC24(N) ignored the setting of transmission specifications switch SW06 (sum check setting). (The QC24(N) operates as if SW06 was set to OFF.)

① QC24(N) processing corresponding to write codes FFH and 00H

The following uses an example to describe the processing performed by the QC24(N) when it receives a user frame part corresponding to write codes FFH and 00H.
Assume that a user frame containing the data codes 02H, FFH, 00H, and 3BH was set as receive user frame No. 3EAH.

- When the QC24(N) receives the 3 bytes of data "STX, arbitrary data (1 byte), ;", it processes them as if user frame No. 3EAH was received.
- The QC24(N) does not check the 2 bytes described above.



If the 02H and 3BH data parts match, they are processed as if user frame No. 3EAH mentioned above was received.

② Send/receive data corresponding to write codes FFH and 01H

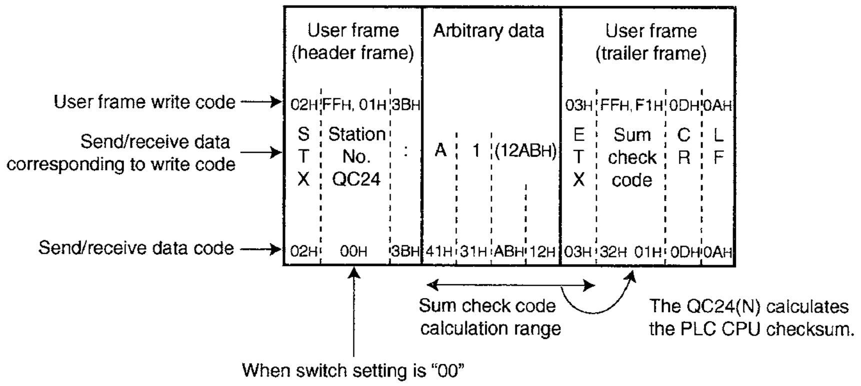
The QC24(N) transmits and receives the user frame part corresponding to write codes FFH and 01H by representing the station No. set in the QC24(N) station No. switch as 1-byte binary data. See the header frame part shown in the illustration in item ③ for an example.

③ Send/receive data corresponding to write codes FFH and EEH to F3H

The QC24(N) transmits and receives the user frame part corresponding to write codes FFH and EEH to F3H by representing the sum check calculated by excluding the send/receive data (message) user frame (1st header frame) as binary data/ASCII data.
The following shows the sum check calculation range and the data contents that are transmitted and received.

- Calculation range
  Calculation includes everything from the data following the user frame (one header frame) at the head of the send/receive data to immediately before the sum check code designation. (Except the transparent code designation additional data)

  (Example) Data contents that are transmitted and received (one header frame and one trailer frame)



- Sum check calculation
  "Sum check" is the result of addition of the data within the range shown above as binary data.
  (In the case of the example)

  $$41H+31H+ABH+12H+03H=\overset{(H)}{01}\overset{(L)}{32}H$$

- The following uses the message shown in the example to describe the data contents when the corresponding sum check code is transmitted and received when the user frame includes the write codes FFH and EEH to F3H.

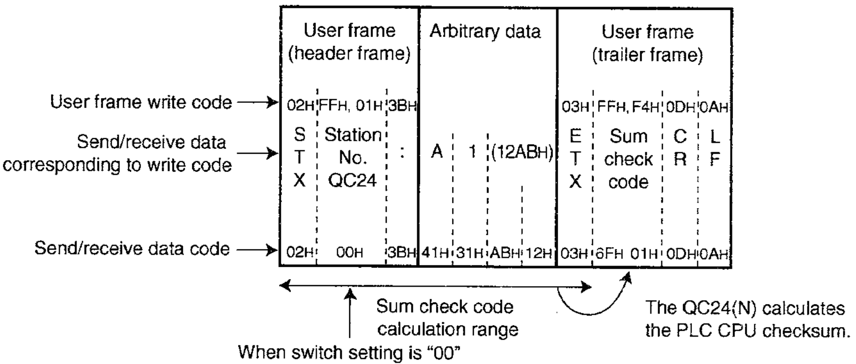
Write code	Data contents transmitted and received
FFH, EEH	01H and 32H are transmitted and received, beginning from 32H.
FFH, F0H	32H is transmitted and received.
FFH, F1H	"3" and "2" are transmitted and received, beginning from the "3".
FFH, F3H	"2" is transmitted and received.

④ Send/receive data corresponding to write codes FFH and F4H to F9H

The QC24(N) transmits and receives the user frame part corresponding to write codes FFH and F4H to F9H by representing the sum check calculated by including the send/receive data (message) user frame (header frame) as binary data/ASCII data.
The following shows the sum check calculation range and the data contents that are transmitted and received.

- Calculation range
  Calculation includes everything from the send/receive data head user frame to immediately before sum check code designation. (Except the transparent code designation additional code.)

  (Example) Transmit/receive data contents (one header frame and one trailer frame)



- Sum check calculation
  This calculation is the result of addition of the data within the range shown above as binary data.
  (It is the same as the calculation method of item ③.)
  (In the case of the example)

  $$02H + 00H + 3BH + 41H + 31H + ABH + 12H + 03H = \overset{(H)}{01}\overset{(L)}{6F}H$$

- The following uses the message shown in the example to describe the data contents when the corresponding sum check code is transmitted and received when the user frame includes the write codes FFH and F4H to F9H.

Write code	Data contents transmitted and received
FFH, F4H	01H and 6FH are transmitted and received, beginning from 6FH.
FFH, F6H	6FH is transmitted and received.
FFH, F7H	"6" and "F" are transmitted and received, beginning from "6".
FFH, F9H	"F" is transmitted and received.

16.1.2 Default frame (read only)

This frame is written to the QC24(N) in advance and can be used in the same way as the other user frames.

1 General description

The default frame writes to and reads from the QC24(N) OS ROM the 1 byte of data (code: 01H to FEH) shown in the table below. Up to 5 bytes of data can be written and read.

(Frame No.: 1H to 3E7H) The default frame is handled as a user frame.

2 Default frame write data and data contents that are transmitted and received

The following shows the codes of the write data of the default frame written to the QC24(N) OS RAM and the data contents that are transmitted and received.

Default frame No. (Hexadecimal (decimal))	Written data code (1st byte to nth byte)	Write byte count	Frame byte count	Data contents that are transmitted and received
				Data contents
1H(1)	01H	1	1	(Data codes shown at the left)
2H(2)	02H			STX
to	to			to
FEH(254)	FEH			(Data codes shown at the left)
FFH(255)	—		—	(For variable data designation)
100H(256)	00H	1	1	NUL
101H(257)	FFH	1		(Data codes shown at the left)
102H(258)	0DH, 0AH	2	2	CR, LF
103H(259)	10H, 02H			DLE, STX
104H(260)	10H, 03H			DLE, ETX
105H(261)	00H, FEH	2	2	(Data codes at the left)
106H(262)	00H, 00H, FEH	3	3	(Data codes at the left)
107H(263)	03H, FFH, F1H	3	2	ETX, sum check code *1
108H(264)	03H, FFH, F1H, 0DH, 0AH	5	4	ETX, sum check code, CR, LF *1
109H(265)	(None)	—	—	—
to				
10DH(269)				
10EH(270)	FFH, EEH	2	1	Sum check code *1
110H(272)	FFH, F0H			
111H(273)	FFH, F1H			
113H(275)	FFH, F3H			
114H(276)	FFH, F4H			
116H(278)	FFH, F6H			
117H(279)	FFH, F7H			
119H(281)	FFH, F9H			
11FH(287)	FFH, FFH	2	1	Register code FFH data (1byte)
120H(288)	(None)	—	—	—
to				
3E7H(999)				

*1 The combination of FFH, □H in the write code is used to handle variable data (check sum code, QC24(N) station No., etc.) as part of the user frame.
The data contents that are transmitted and received and the byte count depend on the code combined with write code FFH.
See Section 16.1.1 4 for the write code combinations that can be handled as variable data and the data contents that are transmitted and received.

16.2 QC24(N) Transmit/Receive Processing Using User Frame Write Data

The following describes how the QC24(N) transmits and receives using user frame write data.

The QC24(N) checks the transmission/reception of following data, using written data.

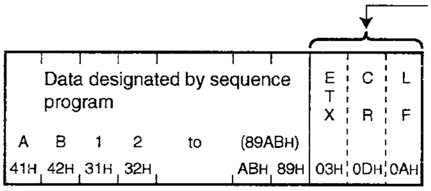
1 Transmission

(a) If user frame transmission is designated, the user frame is converted, or not converted, from ASCII to BIN data and transmitted, depending on the data communications protocol, ASCII-BIN conversion designation, and user frame No. designation, based on the following data as the send data of the given part.

① Write code 01H to FEH 1-byte data write part

QC24(N) transmission is based on the write code (01H to FEH) data.

(Example) Write the data codes 03H, 0DH, and 0AH as user frame No. 3E8H. When user frame No. 3E8H is designated during data transmission, if ASCII-BIN conversion is disabled, the QC24(N) transmits the data codes 03H, 0DH, 0AH (ETX, CR, LF) as the send data of the given user frame part.
If ASCII-BIN conversion is enabled, the QC24(N) converts each of the data above to 2-character ASCII data and transmits the ASCII data.



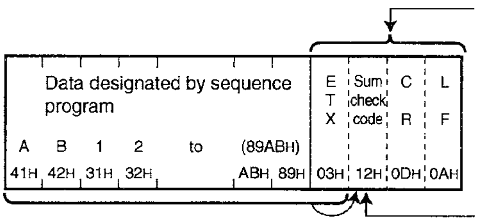
Part that designated user frame No. 3E8H (Added by the QC24(N).)

(When ASCII-BIN conversion disabled)

② Write data codes FFH+00H to FFH 2-byte data write part

QC24(N) transmission is based on the variable data corresponding to the combination of the write codes AFFH and 00H to FFH.
For example, if sum check code is written, the QC24(N) will calculate and transmit the sum check.
If the QC24(N) station No. is written, the station No. set in the QC24(N) is transmitted.

(Example) Write the data codes 03H, FFH, F0H, 0DH, 0AH as user frame No. 3E9H. When user frame No. 3E9H is designated during data transmission, the QC24(N) calculates the sum check. If ASCII-BIN conversion is disabled, the QC24(N) transmits the calculated sum check as the send data of that user frame part.
If ASCII-BIN conversion is enabled, the QC24(N) converts the calculated sum check to 2 characters/byte ASCII data and transmits the ASCII data.



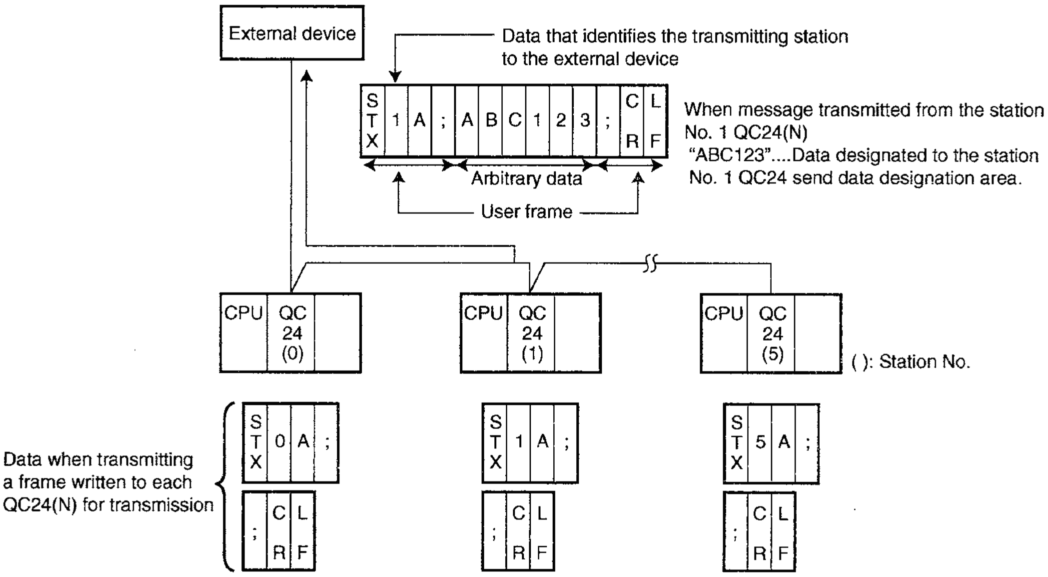
Part that designated user frame No. 3E9H (Added by the QC24(N).)

(When ASCII-BIN conversion disabled)

Calculated by the QC24(N).

Note

With a multidrop link, the user frame includes data that identifies which station transmitted the message to the external device to facilitate generation of arbitrary send data.



QC24: QC24, QC24N

2 Reception

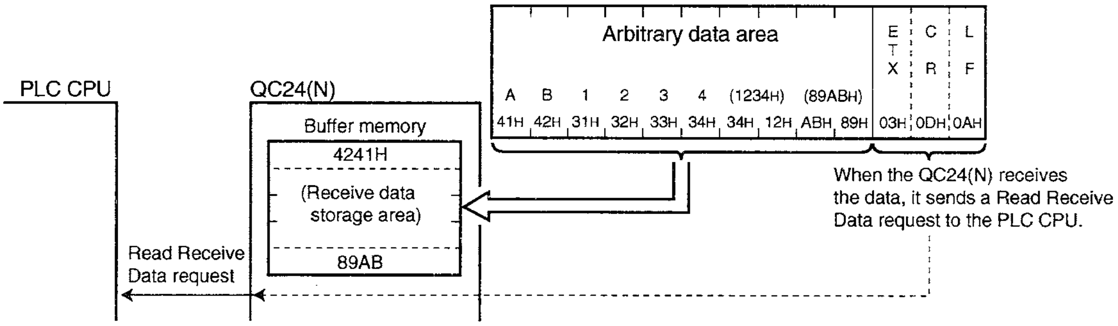
(a) When setting for reception by user frame is performed, and a header frame is set, the QC24(N) receives the message when it receives data with the same contents as the designated header frame.
If a trailer frame is set, when the QC24(N) receives data with the same contents as the designated trailer frame, it sends a Read Receive Data request to the PLC CPU.

(b) The following describes QC24(N) receive processing using write data.

① Write data code 01H to FEH 1-byte data write part

The QC24(N) receives and checks if the received data is data of the same code (01H to FEH) as the written code.

(Example) Write the data codes 03H, 0DH, 0AH as user frame No. 3E8H.
When user frame No. 3E8H is set as data receive user frame No. 3E8H, the QC24(N) receives and checks data codes 03H, 0DH, 0AH (ETX, CR, LF) as the receive data of that user frame part.



② Write data code FFH + 00H to FFH 2-byte data write part

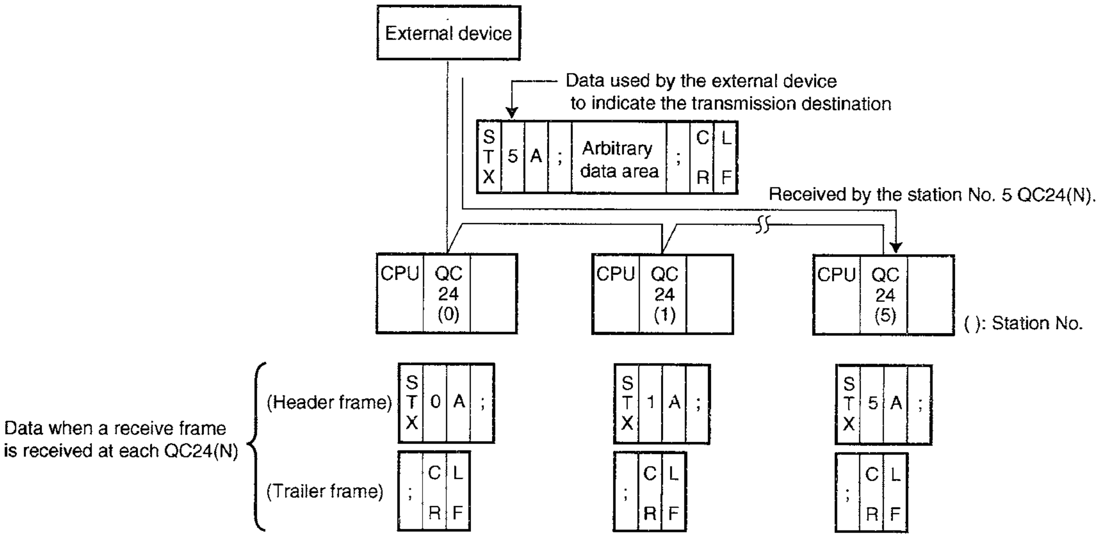
The QC24(N) receives and checks if the received data is variable data corresponding to the combination of the write codes FFH and 00H to FFH.
For example, if a sum check code is written, the QC24(N) calculates the sum check from the receive data and checks if it is the same as the received sum check code. If the two codes are not the same, the QC24(N) performs error processing.
If the QC24(N) station No. is written, the QC24(N) checks if the received station No. is the same as the station No. set in the QC24(N). If the station Nos. are not the same, the QC24(N) processes the data as if normal data was received instead of a user frame.

(Example) Write the data codes 03H, FFH, F0H, 0DH, 0AH as user frame No. 3E9H. When user frame No. 3E9H is set as a data receive frame, the QC24(N) calculates, receives, and checks the sum check code as the receive data of that user frame part.

(c) The QC24(N) removes the user frame data from the received message.
(The PLC CPU cannot read this data.)

Note

With a multidrop link, if the receive user frame inherent to each QC24(N) is connected to the link in advance, the QC24(N) of a given station will store only the arbitrary data area of the message transmitted by the external device to the receive data storage area.



QC24: QC24, QC24N

16.3 Precautions when Writing and Using User Frames

The following describes the precautions which should be observed when writing user frames and using written user frames to transmit data to and receive data from the external device.

1 **Precautions when writing user frames**

① User frames containing only the sum check code of the variable data cannot be written. When writing the sum check code, add arbitrary data.

② Write receive user frames to the QC24(N) EEPROM.

③ Conduct registration, reading, and deletion of the user registration frame from the sequence program when data communication is not being conducted with external equipment.

2 **Precautions when using user frames**

(a) When the QC24(N) is started, the No. of receive user frames must be set in the buffer memory.

Receive user frame data by performing the following operations sequentially. (Section 14.9 describes steps ② and ③.)

① If a user frame used in data reception was written, restart the QC24(N).

② When starting the QC24(N), set the receive user frame No. to the buffer memory and write [1] to buffer memory user frame use designation area (addresses: ADH/14DH).

③ After the value of the buffer memory user frame use designation area changes to [2], start receiving data.

④ Check if the data from the external device was received normally.

(b) If the QC24(N) receives additional code data while receiving data with the non procedure protocol, it does not assume that the last byte of data is the following control data.

- Data received as user frame header frame, trailer frame (See Sections 16.1 and 16.2.)
- Receive end code data (See Section 9.3.1 1 (a).)
  Therefore, do not set a user frame containing data receive additional code data as a non procedure protocol receive user frame.

(c) The arbitrary data area of a message received from an external device cannot include data with the same contents (same code) as the trailer frame.

(Example)

User frame (header frame)	Arbitrary data area	User frame (trailer frame)

(d) In the following cases, set the data bit length of the transmission specifications to 8 bits. (Set QC24(N) switch SW02 to ON.)

① When transmitting and receiving the sum check code of the variable data as binary data
(Write code: FFH, EEH/FFH, F0H/FFH, F4H/FFH, F6H)

② When transmitting and receiving a user frame containing data codes 80H to FFH

16.4 Writing, Reading, and Deleting User Frames

Write, read, and delete QC24(N) EEPROM and buffer memory user frames as described below.

Kind	User frame No. (Hexadecimal (decimal))	Write destination	Note
Default frame	1H to 3E7H (-11111 to -03999)	QC24(N) OS ROM	Can be read from external device.
User frame	3E8H to 4AFH (-31000 to -31199)	QC24(N) EEPROM	Can be written, read, and deleted
	8000H to 801FH (-32768 to -32737)	QC24(N) buffer memory (addresses: 1B00H to 1FF6H)	

1 Writing, reading, and deleting user frames from the PLC CPU

User frame No.	Write	Read	Delete
1H to 3E7H	Not allowed		
3E8H to 4AFH	Performed as described in Sections 16.4.1 to 16.4.4.		
8001H to 801FH	Performed with application instruction (FROM, TO), etc. *1		Not allowed *2

*1 When writing and reading user frames, the contents of the user frame data are the same as the contents of the data when writing and reading the EEPROM.
Write and read user frames by referring to this section.

*2 Write new frames by overwriting old frames.
(The old contents are destroyed.)

2 Writing, reading, and deleting user frames from external devices

User frame No.	Write *1	Read	Delete
1H to 3E7H	Not allowed		Not allowed
3E8H to 4AFH	Performed with the dedicated protocol data communication function described in Section 6.7. *2		
8001H to 801FH			

*1 To check the available user frame Nos., read the buffer memory (addresses: 205H to 21DH) given in Section 16.4.1.

*2 User frames can be written to and read from the QC24(N) buffer memory with the dedicated protocol buffer memory read and write functions described in Section 6.3, but use the function described in Section 6.7 as much as possible.

POINT

Conduct registration, reading, and deletion of the user registration frame from the sequence program when data communication is not being conducted with external equipment.

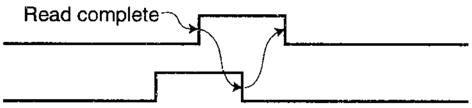
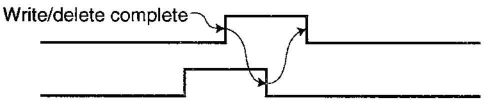
16.4.1 I/O signals for handshake with PLC CPU and buffer memory

The following shows the I/O signals for handshake and the buffer memories used when writing, reading, or deleting user frames from the PLC CPU.

Note

When writing, reading, and deleting user frames from an external device, you do not have to be aware of the I/O signals for handshake and the buffer memories shown below.

1 I/O signals for handshake with PLC CPU

	I/O signal	Signal name	Device turned ON/OFF		Timing
			CPU	QC24(N)	
User frame read	X (n+1) 7	EEPROM read complete		○	
	(Y (n+1) 7	EEPROM read request	○		
User frame write/delete	X (n+1) 8	EEPROM write complete		○	
	Y (n+1) 8	EEPROM write request	○		

Note

The following signals can also be used as I/O signals, in addition to those shown above.
See Section 3.4 for the PLC CPU I/O signals.

- QC24(N) ready signal (X (n+1) E) .... Turned ON when the PLC CPU can access the QC24(N)
- Watchdog timer error signal (X (n+1) F) .. Turned ON when the QC24(N) cannot operate normally

2 Buffer memory

Address (Hexa-decimal (decimal))	Name		Stored value	Processing		
				Write	Read	Delete
2H (2)	EEPROM access	Write/read/delete designation	0: No request 1: Write request 2: Read request 3: Delete request	○	○	○
3H (3)		Frame No. designation	0: No frame No. 1000 to 1199 (3E8H to 4AFH) : Write/read/delete frame No.			
4H (4)		Write/read/delete result storage	0: Normal end Nonzero: Abnormal end (error code)			
5H (5)		Write data byte count designation (See ①.)	0: Delete 1 to 80 (1H to C8H) : Write data byte count	○	○	×
6H (6) to 2DH (45)		User frame (See ②.)	Data code of frame to be written/deleted			
204H (516)		User frame registration count storage	0: Not written to EEPROM 1 to 200 (1H to C8H) : Number written to EEPROM	△	△	△
205H (517) to 21DH (541)		User frame registration status storage (See ③.) (For registration No. check)	0: Given range not written Nonzero: Registration status			
21EH (542)	Default frame registration count storage (OS ROM)		n: Registration count (See Section 16.1.2.)			
1B00H (6912)	Registration No. 8001H	Write data byte count designation	(Write data byte count designation...See ①.) 1 to 80 (1H to C8H) : Write data byte count (User frame storage...See ②.) Write frame data code * Write area for 31 frames	○	△	×
1B01H (6913) to 1B28H (6952)		User frame storage *40 words				
1B29H (6953)	Registration No. 8002H	Write data byte count				
1B2AH (6954) to 1B51H (6993)		User frame storage *40 words				
1B52H (6994) to 1FCDH (8141)	⋮					
1FCEH (8142)	Registration No. 801FH	Write data byte count designation				
1FCFH (8143) to 1FF6H (8182)		User frame storage *40 words				

Read/write from PLC CPU
○ : Always performed
△ : Performed as required
× : Unnecessary

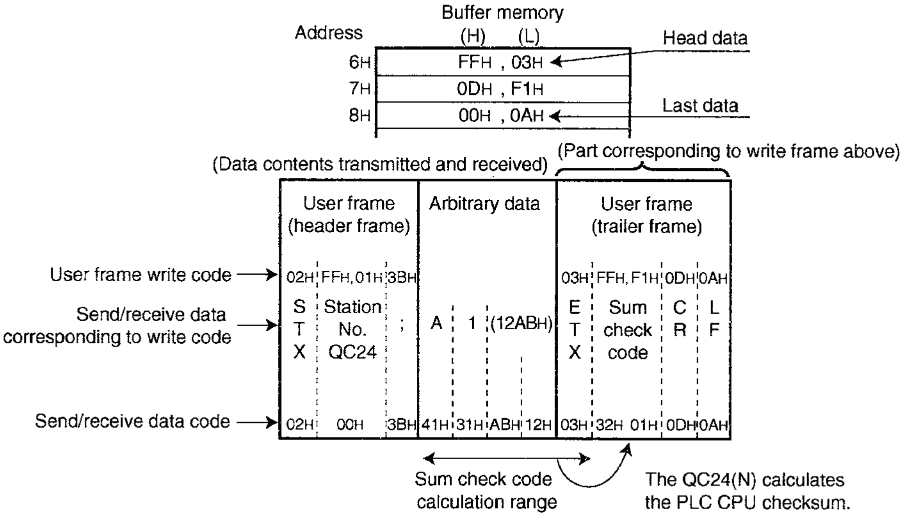
① Write data byte count designation area (Addresses: 5H, 1B00H, 1B29H,..., 1FCEH)

- Indicates the total number of bytes of write data of the user frame to be written/read.
- EEPROM access
  During the write operation, the user writes the total number of bytes of write data
  During the read operation, the total number of bytes of written data.
- Buffer memory access
  During the write operation, the user writes the total number of bytes of write data.

② User frame storage area
(Addresses: 6H to 2DH, 1B01H to 1B28H, 1B2AH to 1B51H,...1FCFH to 1FF6H)

- During the write operation, the user sequentially stores the write data of the user frame to be written in (L) (H) order, beginning from the head area of the given area range.
- During the read operation, the write data of the written user frame is stored with the same contents as when writing.

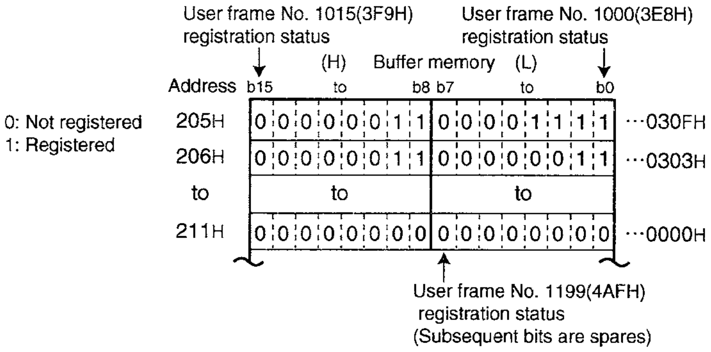
(Example) Contents stored to user frame storage area when a user frame to transmit and receive ETX, sum check code, CR, and LF (registration codes: 03H, FFH, F1H, 0DH, 0AH) is written to the EEPROM.



③ User frame registration status storage area (Addresses: 205H to 21DH)

- The registration status of user frames to the EEPROM is stored as the values shown below.
- The contents of each area that indicates the registration status are shown below. The contents of the area are indicated in one user frame No./1 bit form.

(Example)



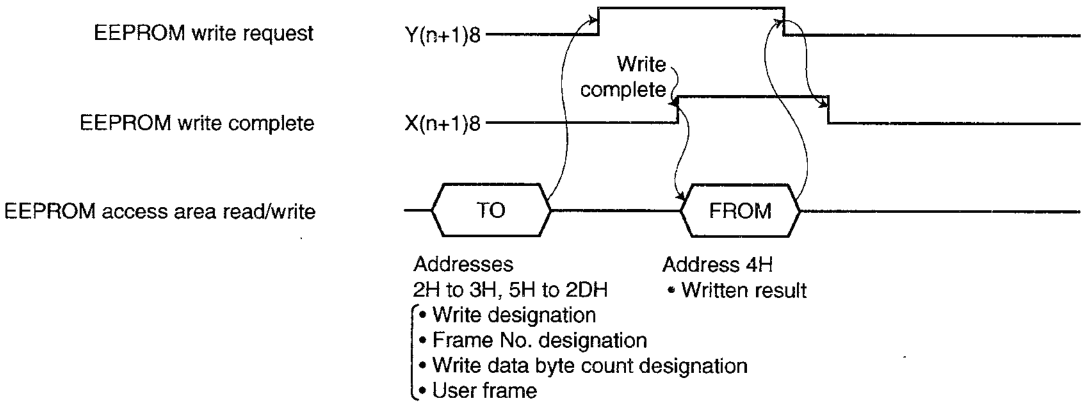
16.4.2 User frame writing

The following describes how to write user frames to the QC24(N) EEPROM.

Note

To check the unwritten user frame Nos., read the buffer memory (addresses: 205H to 21DH) described in Section 16.4.1.

1 **Writing procedure**



2 User frame write sample program

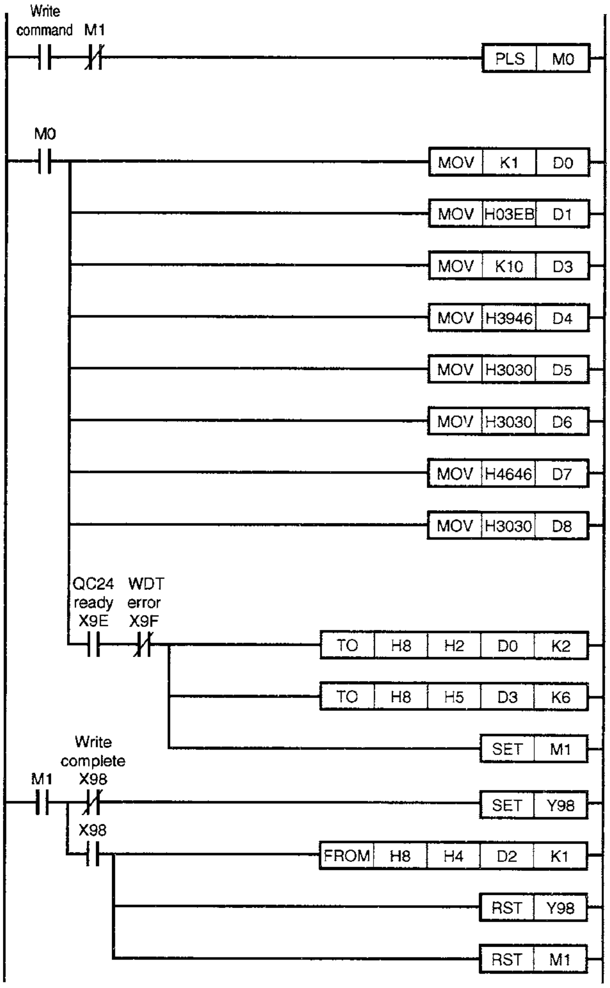
The following shows a sample sequence program that writes user frames.
(QC24(N) I/O signals 80H to 9FH)

POINTS

(1) To designate a No. to which a user frame has already been written when writing a user frame to the EEPROM, delete the old frame No. before designating the new frame No.
(2) The user should control the total number of bytes of write data.

(a) Sequence program when application instructions used (TO, TOP, DTOP, DTOP)
See the programming manual (common instructions) for more information.

① When variable data not included



Converts the write command to PLS.

Sets the write request.

Sets the No. of the frame to be written.

Sets the write data byte count.

Sets the write data of the frame to be written.

In the illustration at the left, the write data contents of the header frame described in Section 7.4.1 are 46H, 39H, 30H, 30H, 30H, 30H, 46H, 46H, 30H, 30H.
[Since variable data is not included, write byte count = frame byte count]

Writes the write directive, etc.

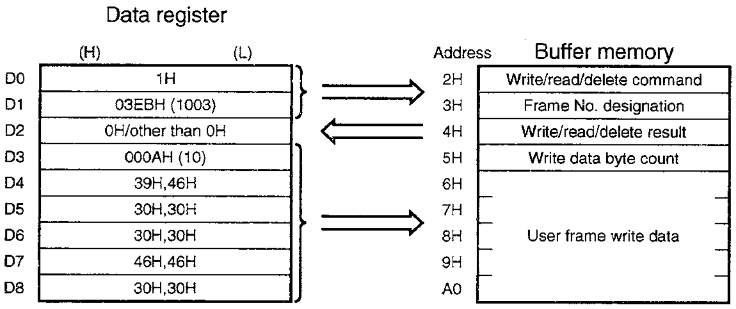
Writes the write data byte count, etc.

Sets the register flag.

Turns ON the EEPROM write request signal.

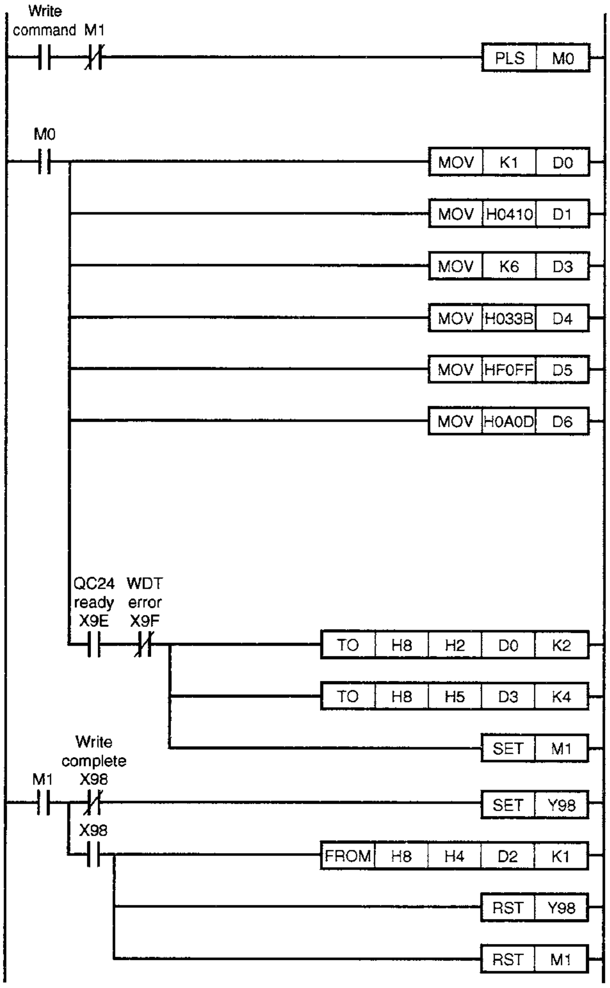
When the write complete signal is turned ON, reads the written result. When D2 is nonzero (error code), takes the action described in Section 22.1.

Resets the register flag.



Data register	(H) (L)		Address	Buffer memory
D0	1H	⟹	2H	Write/read/delete command
D1	03EBH (1003)		3H	Frame No. designation
D2	0H/other than 0H	⟸	4H	Write/read/delete result
D3	000AH (10)	⟹	5H	Write data byte count
D4	39H,46H		6H	User frame write data
D5	30H,30H		7H	
D6	30H,30H		8H	
D7	46H,46H		9H	
D8	30H,30H		A0	

② When variable data included



Converts the write command to PLS.

Sets the write request.

Sets the No. of the frame to be written.

Sets the write data byte count.

Sets the write data of the frame to be written.

The illustration at the left shows the write data to transmit and receive the following data:
;,ETX, sum check code (binary data (1byte)), CR, LF Contents: 3BH, 03H, FFH, F0H, 0DH, 0AH

Since variable data is included, Writer data byte count = 6
Frame byte count = 5

Writes the write directive, etc.

Writes the write data byte count, etc.

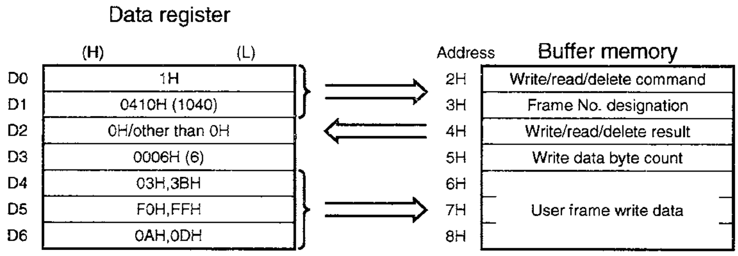
Sets the write flag.

Turns ON the EEPROM write request signal.

When the write complete signal is turned ON, reads the written result.
If D2 is nonzero (error code), takes the action described in Section 22.1.

Turns OFF the write request.

Resets the write flag.

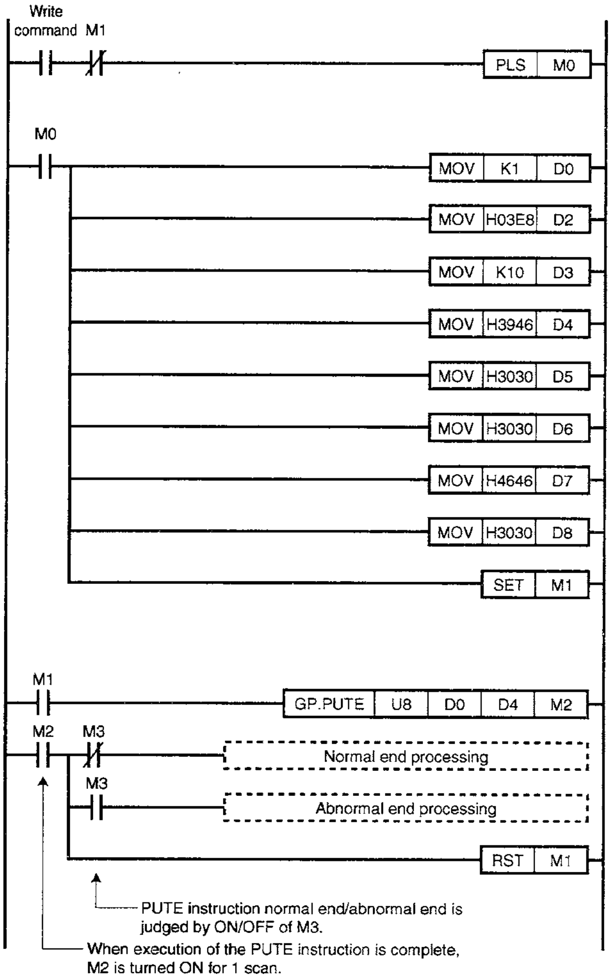


Data register

	(H) (L)
D0	1H
D1	0410H (1040)
D2	0H/other than 0H
D3	0006H (6)
D4	03H,3BH
D5	F0H,FFH
D6	0AH,0DH

Address	Buffer memory
2H	Write/read/delete command
3H	Frame No. designation
4H	Write/read/delete result
5H	Write data byte count
6H	User frame write data
7H	
8H	

(b) Sequence program when dedicated instruction used (PUTE)
See the programming manual (special function module) for more information.
(a) In the following example, the program shown in item ① is replaced by the dedicated instruction.



Converts the write command to PLS.

Sets the write request.

Sets the No. of the frame to be written.

Sets the number of data bytes to be written.

Sets the write data of the frame to be written.

For the illustration at the left, the write data contents for the header frame described in Section 7.4.1 are 46H, 39H, 30H, 30H, 30H, 30H, 46H, 46H, 30H, 30H.
[Since variable data is not included, write data count = frame byte count.]

Sets the write flag.

* The meaning of the values stored to D1 and D2 is different from when application instructions are used.

Takes action according to the error code stored to D1.

Resets the write flag.

POINTS

(1) When the QC24(N) dedicated instruction is used, model name writing by I/O allocation of parameters written to the PLC CPU is unnecessary.
(During the write operation, the number of I/O points (special 32 points) and the module model name (AJ71QC24) at the slot into which the QC24(N) is installed are set.)

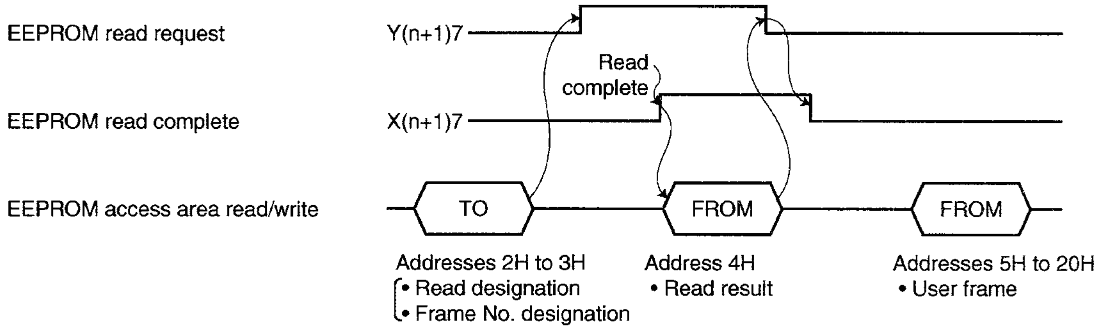
(2) The status of communications using the dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of items (1) and (2) above.

16.4.3 User frame read

The following describes the method used to read user frames written to the QC24(N) EEPROM.

1 Read procedure



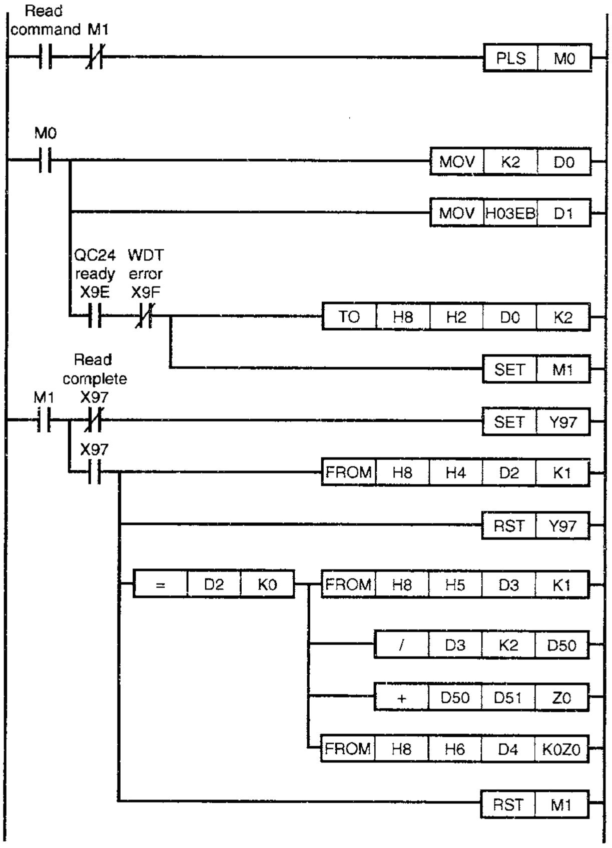
2 User frame read sample sequence programs

The following shows sequence programs that read user frames.
(QC24(N) I/O signals 80H to 9FH)

POINTS

(1) If an unwritten user frame No. is designated, the program is abnormally ended.
(2) When the total number of bytes of write data of the frame to be read is unknown, read 40 words (80 bytes).

(a) Sequence program when application instructions used (FROM, FROMP, DFRO, DFROP)
See the programming manual (common instructions) for more information.



Converts the read command to PLS.

Sets the read request.

Sets the No. of the frame to be read.

Writes the read directive, etc.

Sets the read flag.

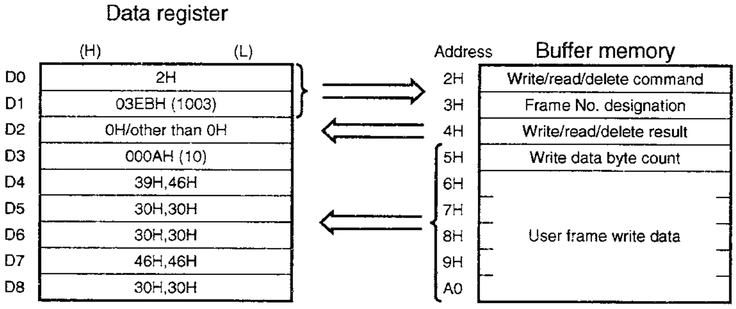
Turns ON the EEPROM read request signal.
When the read complete signal is turned ON, reads the read result.
When D2 is nonzero (error code), takes the action described in Section 22.1.

Turns OFF the read request signal.

Reads the write data byte count, etc.

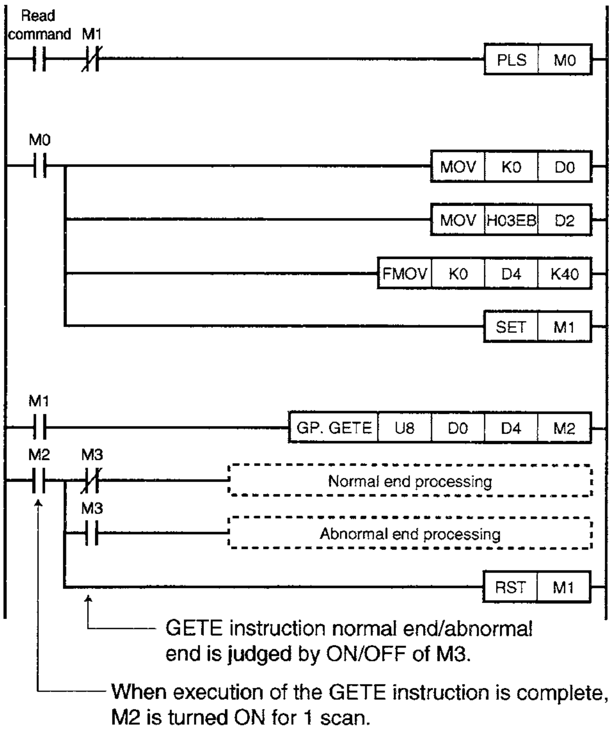
Reads the write data.

Resets the read flag.



When the data described in Section 16.4.21 2 (a)① was written.

(b) Sequence program when dedicated instruction used (GETE)
See the programming manual (special function module) for more information.
The following example replaces the program shown in (a) with the dedicated instruction.



GETE instruction normal end/abnormal end is judged by ON/OFF of M3.

When execution of the GETE instruction is complete, M2 is turned ON for 1 scan.

Converts the read command to PLS.

Sets [0].

Sets the No. of the frame to be read.

Clears D4 to D43, which store the write data when read.

Sets the read flag.

* The meaning of the value stored to D0 to D2 is different from that when application instructions are used.

Processes according to the error code stored to D1.

Resets the read flag.

POINTS

(1) When the QC24(N) dedicated instruction is used, model name writing by I/O allocation of parameters written to PLC CPU is unnecessary.
(During the write operation, the number of I/O points (special 32 points) and module name (AJ71QC24) at the slot into which the QC24(N) is inserted are set.)

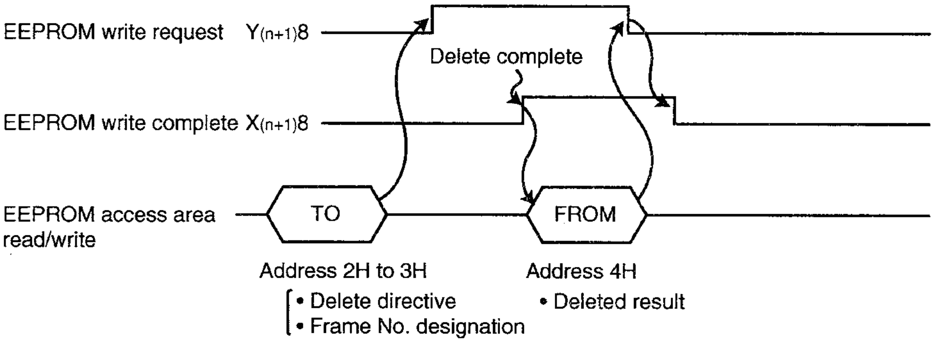
(2) The status of communications by dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of items (1) and (2) above.

16.4.4 User frame deletion

The following describes the method used to delete user frames written to the QC24(N) EEPROM.

1 **Delete procedure**

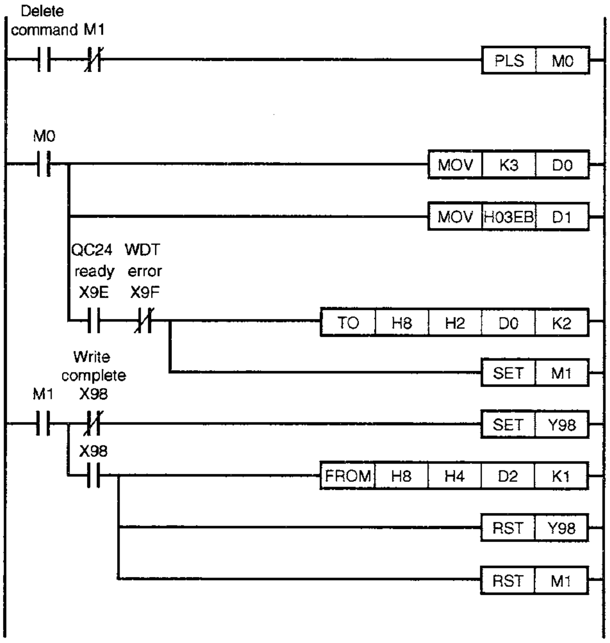


2 **User frame delete sample sequence programs**

The following shows sample sequence programs that delete user frames.
(QC24(N) I/O signals 80H to 9FH)

> **POINT**
>
> If an unwritten user frame No. is designated, the program is abnormally ended.

(a) Sequence program when application instructions used (TO, TOP, DTOP, DTOP)
See the programming manual (common instructions) for more information.



Converts the delete command to PLS.

Sets the delete request.

Sets the No. of the frame to be deleted.

Writes the delete directive to buffer memory addresses 2H to 3H.

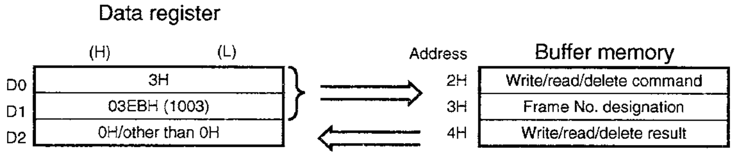
Sets the delete flag.

Turns ON the EEPROM write request signal.

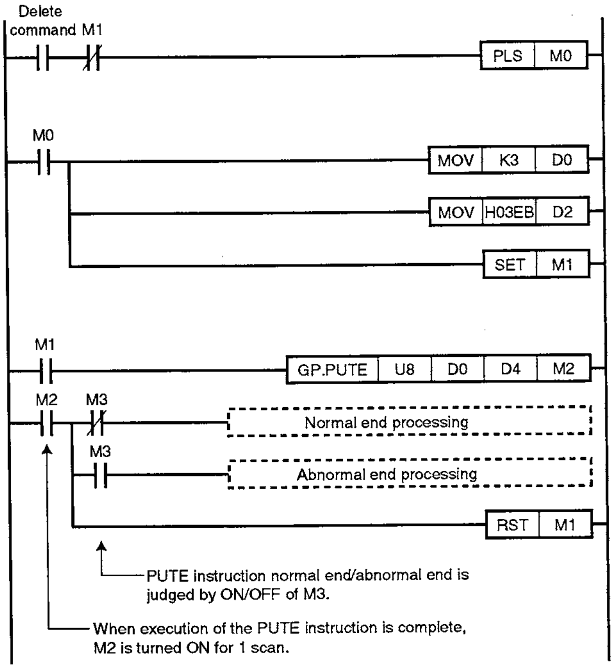
When the write complete signal is turned ON, reads the deleted result. If D2 is nonzero (error code), takes the action described in Section 22.1.

Turns OFF the write request signal.

Resets the delete flag.



(b) Sequence program when dedicated instruction used (PUTE)
See the programming manual (special function module) for more information.
The following examples replaces the program shown in (a) with the dedicated instruction.



PUTE instruction normal end/abnormal end is judged by ON/OFF of M3.

When execution of the PUTE instruction is complete, M2 is turned ON for 1 scan.

Converts the delete command to PLS.

Sets the delete request.

Sets the No. of the frame to be deleted.

Sets the delete flag.

* The meaning of the value stored to D1 and D2 is different from that when application instructions are used.

Processes according to the error code stored to D1.

Resets the delete flag.

POINTS

(1) When the QC24(N) dedicated instruction is used, model name writing by I/O allocation of the parameters written to the PLC CPU is unnecessary.
(During the write operation, the number of I/O points (special 32 points) and module model name (AJ71QC24) at the slot into which the QC24(N) is inserted are set.)

(2) The status of communications by dedicated instruction can be read with the SPBUSY instruction.

(3) See the programming manual (special function module) for a detailed description of items (1) and (2) above.

MEMO

17. DATA COMMUNICATIONS USING EXTERNAL DEVICE AND PLC CPU m: n CONFIGURATION

Always read this section when communicating data by using a multidrop link to connect the external devices and PLC CPU in an m: n configuration.
You do not have to read this section when using a system configuration other than m: n to communicate data.

This section describes the case when data is communicated between external devices and PLC CPU by connecting multiple external devices (m stations) and multiple QC24(N) (n stations) over a multidrop link. (The total number of m and n is up to 32 stations.)
With this m: n multidrop link, only dedicated protocol data communications by command transmission from the external devices can be performed.

17.1 Data Communications Precautions

(1) When communicating data using an m: n system configuration, multiple external devices cannot communicate data with the PLC CPU at the same time.
Interlock the external devices so that they can communicate with the QC24(N) in a 1: 1 configuration.
See Sections 17.2 and 17.3 for the items to be agreed upon and the interlock method to interlock the external devices.

(2) Communicate data between external devices and PLC CPU by the following methods only.

- Full-duplex data communications (m: n data communications is impossible)
- Data communications by command transmission from external device using a dedicated protocol excluding the format 3 and format 5 control procedure (Data communications using the format 3 and format 5 control program and data transmission from sequence program using the on-demand function cannot be performed.)

(3) The data transmitted by one external device is received by all the other external devices, including the external device that transmitted the data. The send data from a PLC CPU is also received by all the external devices.
Therefore, it may be necessary for devices that received data not addressed to them (judged by station No. in the message) to ignore the receive data.
At the PLC CPU, the QC24(N) also ignores the receive data other than that addressed to it.

(4) Connect to multiple external devices and connect the terminating resistor as described in Section 4.7.4 2 (c).

(5) When communicating data over an m: n system, designate the following station number at the [Station No.] and [Local station No.] items in the command message to be transmitted from an external device.

① When accessing the PLC CPU

	Communications using QnA (extension) frame **Communications using QnA simplified frame**	**Communications using A compatible frame**
Station No.	Station No. of QC24(N) to be passed through (Station No. described in Section 6.1.4 $\boxed{5}$(a).)	
Local station No.	Station No. of access source external device *1	Designation unnecessary (No [Local station No.] item)

② When accessing another external device (interlock communications)

	Communications using QnA (extension) frame **Communications using QnA simplified frame**	**Communications using A compatible frame**
Station No.	Station No. of access destination external device *1	
Local station No.	Station No. of access source external device *1	Designation unnecessary (No [Local station No.] item)

*1 A station No. within the [0] to [31] (00H to 1FH) range not set in the QC24(N) at the PLC CPU is used as the external device No. in the [Station No.] and [Local station No.] items in the message.
Select and designate the No. of each external device.
The designation method is described in Section 6.1.4 $\boxed{5}$(a).

- Station No. .... Designates the No. of the transmit destination external device.
- Local station No. .... Designates the No. of the transmit source external device. (Does not have to be designated when A compatible frame is used.)

17.2 External Devices Interlock Conditions

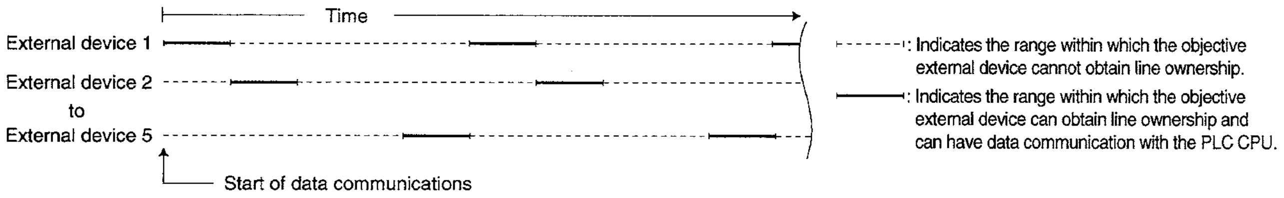
When using a multidrop line to communicate data between external devices and PLC CPU in an m: n configuration, the external devices must be interlocked so that multiple external devices cannot communicate data with the PLC CPU at the same time.
This section describes the conditions for interlocking the external devices so that all of the external devices can communicate data with the PLC CPU.

[Conditions for priority use (obtaining line ownership) of the line from the start to the end of data communications with the PLC CPU.]

17.2.1 Maximum communications time per external device station

This condition determines the maximum time each external device can communicate with the PLC CPU after obtaining line ownership. (~~Time~~ in the illustration below.)
This is selected to prevent loss of data communications between other external devices and the PLC CPU by shutdown of the external device that obtained line ownership.

(Example)



POINTS

(1) Make the maximum data communications time per external device station the maximum time of the external device that requires the most time to communicate data with the PLC CPU.
(2) After system starting, complete data communications from the external device that obtained line ownership and the PLC CPU within the maximum communications time.
[If data communications cannot be completed within this time, initialize the QC24(N) transmission sequence by transmitting the EOT/CL code to the objective PLC CPU within the maximum communications time. (See Section 6.1.4 $\boxed{1}$ (b) or 6.10.)]
(3) While an external device and the PLC CPU are communicating data, have the other external devices check the time so that they do not transmit data during this time.

17.2.2 Message structure when communicating data between external devices

The message structure when communicating data between external devices is determined by any of the following.

This condition is determined to interlock the external devices so that they can exchange data with the PLC CPU in a 1:1 configuration.

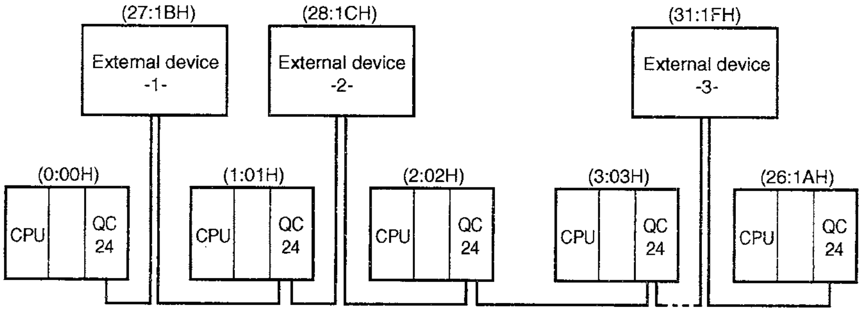
1 When making the message structure the same as that of each control procedure format frame

① Use a number within the [0] to [31] (00H to 1FH) range not set in the QC24(N) of the PLC CPU as the external device No. in the [Station No.] and [Local station No.] items in the message.

② Select and designate the external device numbers.
The designation method is described in Section 6.1.4 5 (a).

- Station No .... Designates the number of the transmission destination external device
- Local station No .... Designates the number of the transmission source external device (Does not have to be designated when A compatible frame is used.)

(Example) When m: n is 5:27
The values in ( ) are the external device and QC24(N) station numbers. (decimal : hexadecimal).



QC24: QC24, QC24N

(ASCII mode QnA frame format 1)

E N Q	Frame identification No.	Station No.	Network No.	PC No.	Local station No.
	H L	H L	H L	H L	H L
	F 9	1 C	0 0	F F	1 B
05H	46H 39H	31H 43H	30H 30H	46H 46H	31H 42H

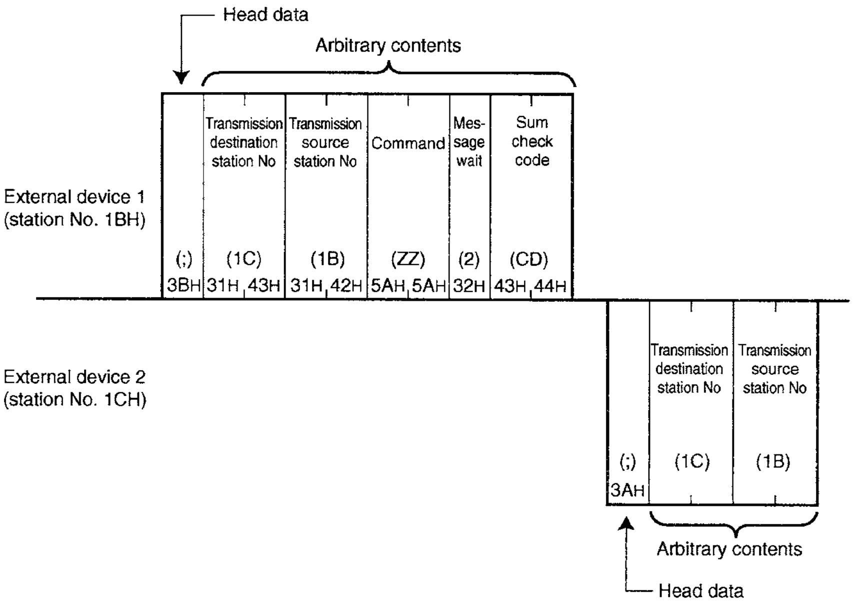
2 When message a structure different from that of control procedure format frames can be used

① Change the header data of each message to other arbitrary data.

- When selecting ASCII mode format 1, format 2, or format 4, change ENQ (05H).

② Arbitrarily list the data following the head data of each message according to the user specifications.

(Example)



POINT

Correspond the message structure for general reporting to all the other external devices using unused station numbers or a message syntax different from the QC24(N) control procedure format.

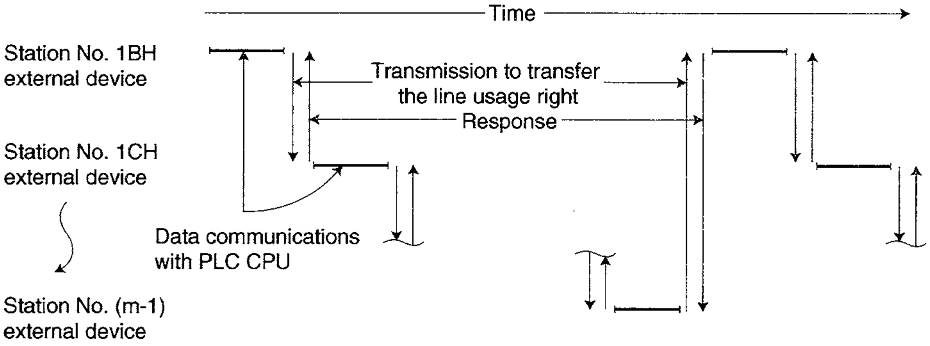
17.3 Examples of Procedure for Data Communications with PLC CPU

The following uses examples to describe the procedure when communicating data with a PLC CPU by interlocking the external devices.

17.3.1 Sequential data communications between external devices and the PLC CPU

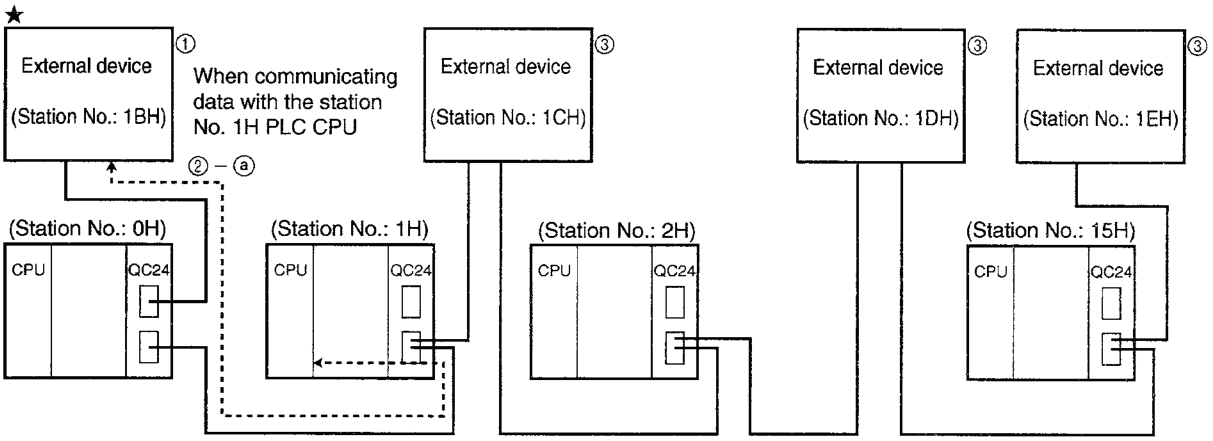
The external devices sequentially obtain the line usage right and communicate data with the PLC CPU based on their station No.

(Example)



The following uses an example to describe the procedure when external devices communicate data with the PLC CPU.

★: External device that obtained the line usage right



QC24: QC24, QC24N

① When the system starts, the external device with the lowest station No. (1BH) is given the line usage right.

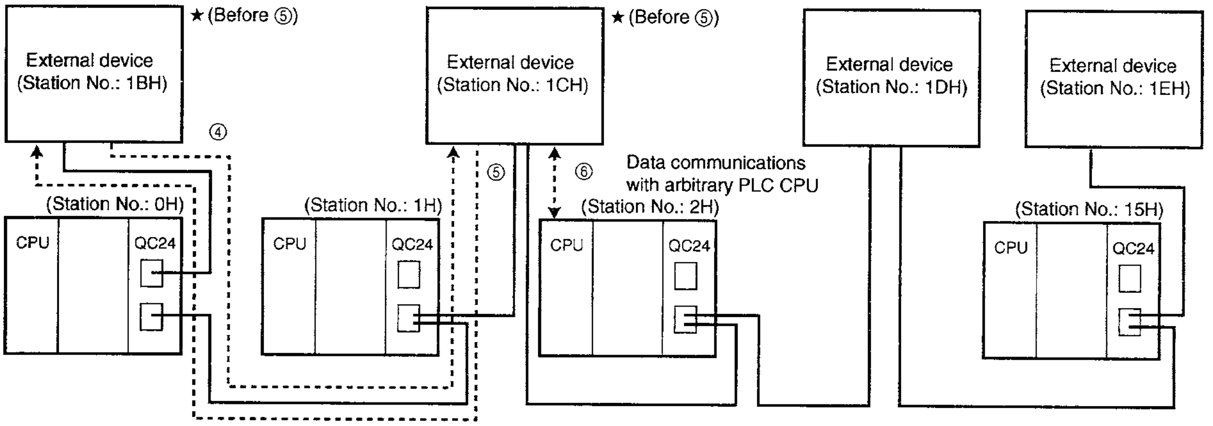
② The external device that obtained the line usage right,

ⓐ When communicating data with the PLC CPU, begins processing from ④ after communicating data with the PLC CPU within the maximum data communications time from among all the external devices

ⓑ When not communicating data with the PLC CPU, immediately begins processing from ④.

③ The external devices that have not obtained the line usage right check the line usage time of the external device that obtained the line usage right and ignore the receive data not addressed to their own station.
When the line usage time exceeds the maximum data communications time, each external device performs the processing of ⑦.

★: External device that obtained the line usage right



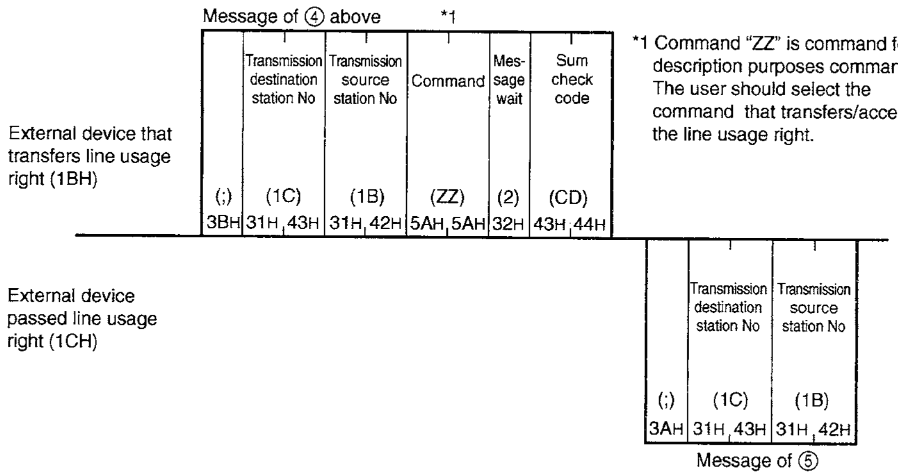
QC24: QC24, QC24N

④ External devices that communicated data with the PLC CPU, or external devices that do not have to communicate data with the PLC CPU, transmit the data for transferring the line usage right to the external device of the next station No. A message structure example is shown in ⑤.

When a response message (see ⑤) is received from the next external device to which the line usage right was passed, data transmission for transferring the line usage right to the external device of the next station No. is repeated until the line usage right is accepted.

⑤ The external device that accepts the line usage right transmits a response message to the external device that passed it the line usage right.

(Example)



	Transmission destination station No	Transmission source station No	Command	Message wait	Sum check code
(;)	(1C)	(1B)	(ZZ)	(2)	(CD)
3BH	31H, 43H	31H, 42H	5AH, 5AH	32H	43H, 44H

	Transmission destination station No	Transmission source station No
(:)	(1C)	(1B)
3AH	31H, 43H	31H, 42H

*1 Command "ZZ" is command for description purposes command. The user should select the command that transfers/accepts the line usage right.

⑥ The external device that accepted the line usage right by transmitting a response message performs processing beginning from ②.

⑦ When line usage time of the external device that currently has the line usage right exceeds the maximum data communications time

ⓐ The external device of the next station No. transmits all external devices general report data and obtains the line usage right and performs step ②.

(Example)

		*1		*2		
		Transmission destination station No	Transmission source station No	Command	Message wait	Sum check code
External device that obtains the line usage right (1CH)	(;) 3BH	(1F) 31H, 46H	(1C) 31H, 43H	(ZZ) 5AH, 5AH	(0) 30H	(0A) 30H, 41H

*1 Unused station No. for all external devices general report

*2 See *1 of ⑤ above.

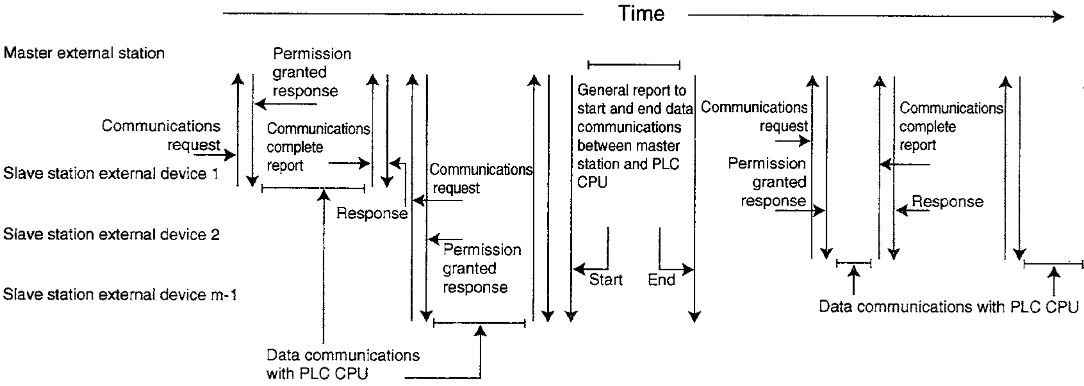
ⓑ The other external devices check if all external devices general report data was received. If the data was received, the external device performs step ③.

If the data was not received, the next external device transmits all external devices general report data and obtains the line usage right and performs step ②. The other external devices perform ⓑ of this item.

17.3.2 Data communications between PLC CPU and external devices by designating a master station and slave stations

One of the external devices is made the master station and the other external devices communicate data with the PLC CPU after obtaining permission from the master station.

(Example)

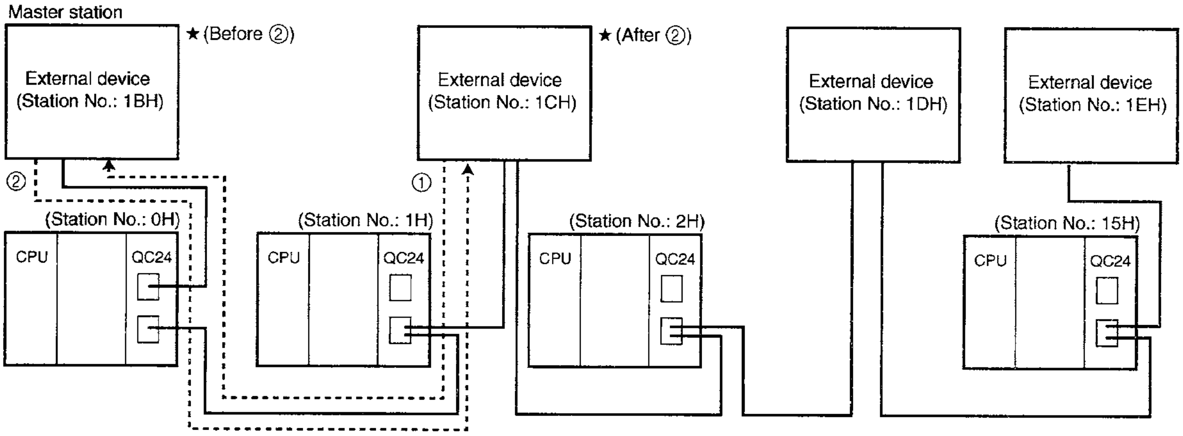


The following uses an example to describe the procedure when external devices communicate data with the PLC CPU.

In this example, after the start of data communications between external devices and the PLC CPU, the external devices perform a maximum data communications time time-out check. Slave station external devices that are not communicating data with the PLC CPU check if the external device that completed data communications with the PLC CPU transmitted a communications complete report.

In the following descriptions, the external device with the lowest station No. (1BH) is assumed to be the master station and the other external devices are assumed to be slave stations.

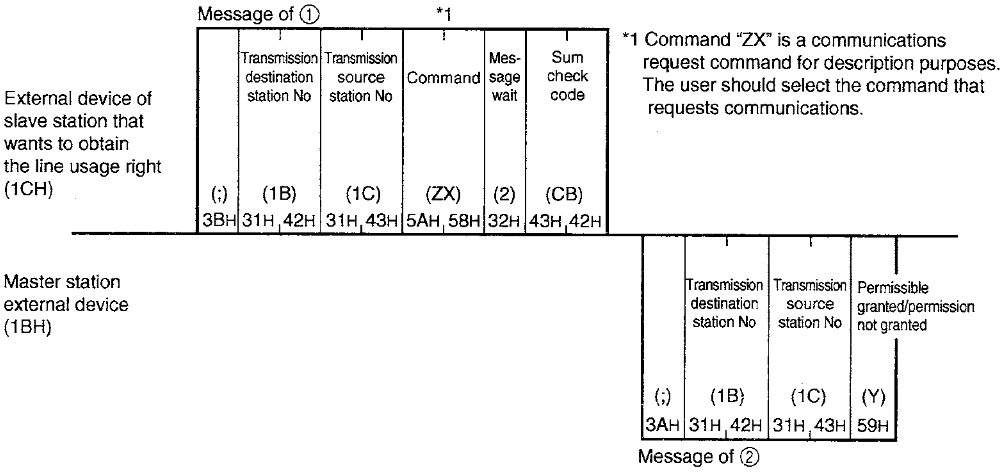
★: External device that obtained the line usage right



QC24: QC24, QC24N

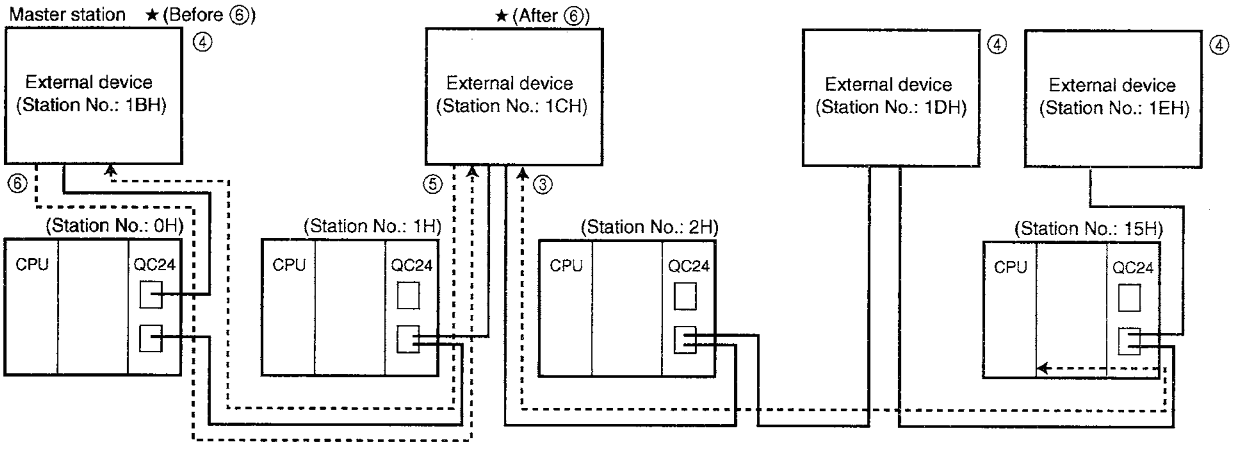
① A slave station that wants to communicate data with the PLC CPU sends a communications request to the master station to obtain the line usage right. A message structure example is shown in ②.

② The master station transmits a permission granted response to the slave station that issued the communications request.



*1 Command "ZX" is a communications request command for description purposes. The user should select the command that requests communications.

★: External device that obtained the line usage right



QC24: QC24, QC24N

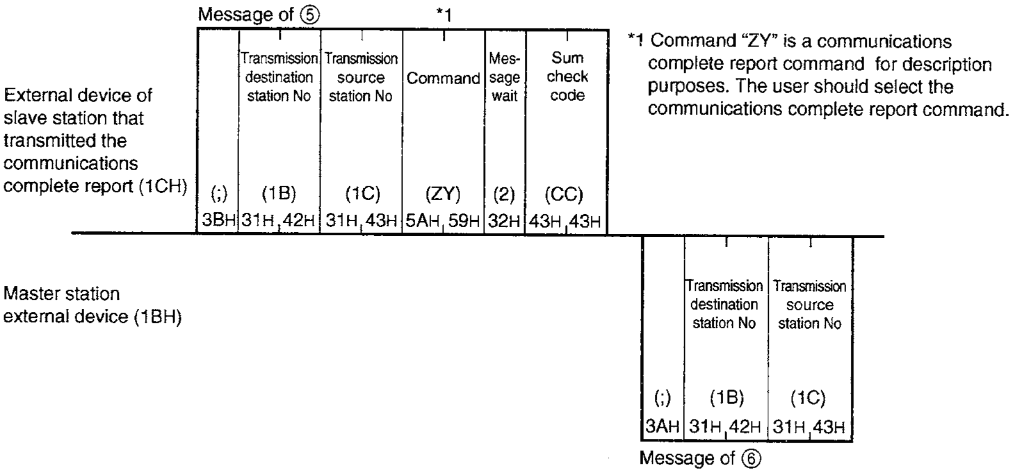
③ After communicating data with the PLC CPU within the maximum data communications time from among the external devices, the slave station that received the "permission granted" response goes to step ⑤.

④ The master station that transmitted the "permission granted" response and the slave stations that did not obtain line usage check the line usage time of the slave station that obtained the line usage right and ignore receive data other than that addressed to their local station.
If the line usage time exceeds the maximum communications time, the external devices perform the processing of step ⑦.

⑤ After data communications are complete, the slave station that exchanged data with the PLC CPU transmits a communications complete report to the master station. A message structure example is shown in ⑥.
Slave stations that do not communicate data with the PLC CPU check if a communications complete report was transmitted and do not communicate data with the master station during that time.

⑥ The master station that received the communications complete report transmits a response to the slave station that transmitted the communications complete report.

(Example)



*1 Command "ZY" is a communications complete report command for description purposes. The user should select the communications complete report command.

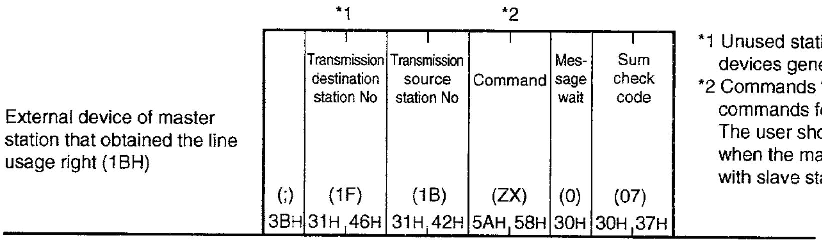
⑦ After completion of ⑥ above, or when the line usage time of the slave station that obtained the line usage right exceeds the maximum data communications time:

ⓐ The master station waits for a communications request from a slave station.
When the master station receives a communication request, it performs processing from step ②.

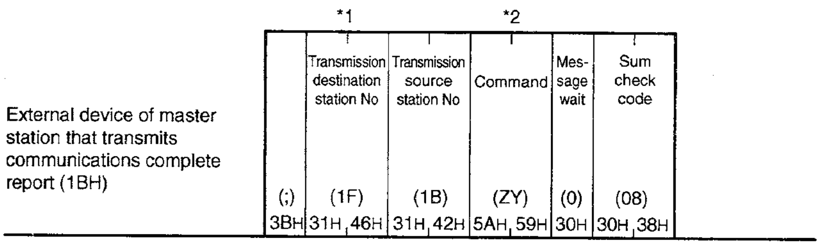
ⓑ The slave stations do not communicate data with the master station until data communications with the PLC CPU is necessary.
When data communications with the PLC CPU becomes necessary, that slave station performs processing from ①.

⑧ When the master station itself wants to exchange data with the PLC CPU and a slave stations does not have the line usage right, it transmits all external devices general report data and obtains the line usage right before communicating data with the PLC CPU.
After data communications with the PLC CPU is complete, the master station transmits all external devices general report data to inform the slave stations that data communications with the PLC CPU is complete.
During this time, the slave stations do not communicate data with the master station until master station data communications is complete.

(Example)



*1 Unused station No. for all external devices general report.
*2 Commands "ZX" and "ZY" are commands for description purposes. The user should select the command when the master station communicates data with slave stations.



18. SWITCHING THE MODE AFTER STARTING

This function forcefully switches the current operation mode and transmission specifications of the designated interface from an external device and the PLC CPU after the QC24(N) starts.
When the QC24(N) starts, it begins operation in the operation mode set in its mode switch and with the transmission specifications set in its transmission specifications switches.
The mode switching function is used when changing the operation mode and transmission specifications of each interface to match the data communications application and continue data communications without restarting the QnACPU.

The following outlines mode switching from an external device and the PLC CPU.

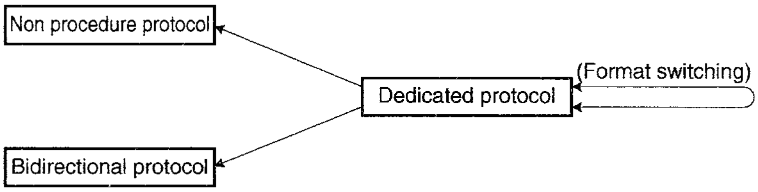
1 Mode switching from external device

① If the operation mode of the interface connecting the external device is dedicated protocol, mode switching can be performed.

② The operation mode can be changed to dedicated protocol format switching or from dedicated protocol to non procedure protocol/bidirectional protocol.

③ The transmission specifications set in QC24(N) transmission specifications switches SW01 to SW12 can be changed.

(Operation mode switching)



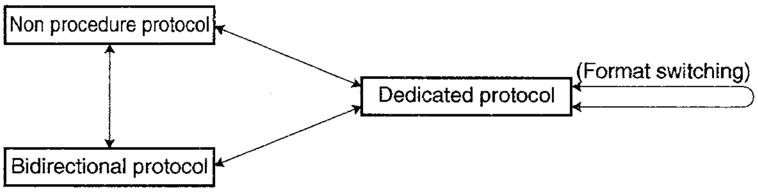
2 Mode switching from PLC CPU

① Mode switching can be performed without regard to the current operation mode of the interface connecting the external device.

② The operation mode can be changed to dedicated protocol format switching or to another operation mode (dedicated protocol, non procedure protocol, bidirectional protocol).

③ The transmission specifications set in QC24(N) transmission specifications switches SW01 to SW12 can be changed.

(Operation mode switching)



POINT

When using the mode switching function, set QC24(N) transmission specifications [Setting change enable/disable] to [Enable]. (SW08 = ON)

18.1 Mode Switching Operation and Contents that can be Changed

This section describes the set contents that can be changed with mode switching and the operation of the QC24(N) after mode switching.

18.1.1 Set contents that can be changed with mode switching

The following describes the contents that can be switched when the QC24(N) mode is switched from an external device or the PLC CPU.
In any case, switching corresponds to the QC24(N) switches.

1 Switching the operation mode switching with the mode switch

(a) The operation mode of each interface can be switched with the QC24(N) mode switch.

(b) The buffer memory mode switching area switching mode No. designation area designates the mode No. after switching (corresponds to the number set in the mode switch).

2 Changing the transmission specifications with the transmission specifications switches

(a) The transmission specifications of each interface can be switched with the QC24(N) transmission specifications switches (SW01 to SW12).

(b) The buffer memory mode switching area switching specifications designation area designates the transmission specifications after switching.

18.1.2 Operation of QC24(N) after mode switching

The following describes the operation of the QC24(N) after the mode was switched from an external device or the PLC CPU.

1 Processing currently executing

(a) If there is a mode switching request, mode switching immediately starts.

(b) If one of the following processings was being performed when a mode switching request was issued, that processing is terminated.

① Data communications using a dedicated protocol

- Command message receive processing and response message or ondemand data transmission processing are all terminated.
- The transmission normal end signal for an on-demand data transmission request is not turned on.

② Data communications using non procedure protocol and bidirectional protocol

- Data and response message transmit and receive processing are all terminated.
- All the input signals from the QC24(N) of the PLC CPU related to transmit and receive processing are turned off.
- If the receive data from the external device was being stored to the QC24(N), the receive data up to that point is ignored and the data is processed with the current receive data count as [0].

2 Modification of buffer memory stored value

(a) Special applications area (addresses: 252H to 253H, 262H to 263H)

The mode setting status (operation mode) and transmission specifications after mode switching is complete are stored.
The values stored to areas other than the above are not changed. The contents before switching are preserved.

(b) User area (addresses: 400H to 1AFFH)

The stored values are not changed. The contents before mode switching are preserved.

18.2 Mode Switching Precautions

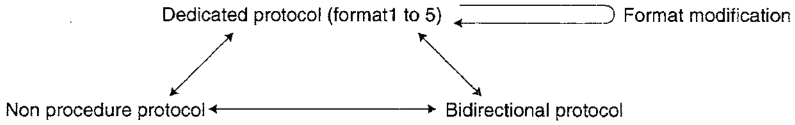
The following describes the precautions which should be observed when switching the QC24(N) mode from an external device or the PLC CPU.

1 Agreement between external device and PLC CPU

Agree upon the following contents related to mode switching between the external device and PLC CPU so that mode switching is not performed during data communications.

① Which external device and PLC CPU is to perform mode switching

② Mode switching timing for each mode switching pattern



③ Interlocking of all connected devices when the mode is switched

- Method and message structure when all the connected stations are informed that the mode was switched.
- Method and message structure when all the connected stations are informed that mode switching is complete.
- Device No. and meaning of value when a PLC CPU word device is used.

2 Mode switching from external device

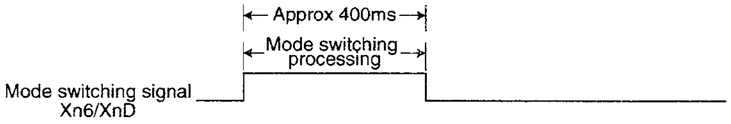
① When the mode was switched, an external device cannot change the QC24(N) buffer memory special applications area parameters.
If the special applications area parameters must be changed after mode switching, write the necessary data from the PLC CPU.

② When the interface of the QC24(N) connecting the external device uses the non procedure protocol or bidirectional protocol, the mode cannot be switched from the external device. (Because the function that switches the mode from an external device cannot be used.)

③ The function that switches the QC24(N) mode from an external device described in Section 6.11 can be used only with QC24(N) connected to an external device (including multilink station).
It cannot be used with other station QC24(N) connected over a data link system or network system.

3 Data communications after mode switching

The QC24(N) a mode switching processing time of about 400 ms.
During this time, including the storage processing time of the value set to the buffer memory special applications area, data can not be communicated between external device and QC24(N).



4 Linked operation mode switching

Do not perform the following mode switchings.

- Mode switching when the two QC24(N) interfaces are currently linked.
- Mode switching to linked operation.

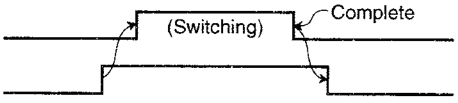
POINT

It is recommended that mode switching be performed from the PLC CPU as described above.

18.3 I/O Signals for Handshake with PLC CPU and Buffer Memory

This section describes the I/O signals for handshake and the buffer memories used when mode switching is performed.

1 I/O signals for handshake with PLC CPU

	I/O signal		Signal name	Device turned ON/OFF		Timing
	CH1	CH2		CPU	QC24(N)	
Mode switching	Xn6	XnD	Mode switching underway		○	
	Yn2	Yn9	Mode switching request	○		

Note

The following signals can also be used as I/O signals, in addition to the above.
See Section 3.4 for the PLC CPU I/O signals.

- QC24(N) ready signal (X (n+1) E) .... Turned ON when the QC24(N) can be accessed from the PLC CPU
- Watchdog timer error signal (X (n+1) F) .... Turned ON when the QC24(N) does not operate normally
- CH1 ERR. LED ON signal (XnE) .... Turned ON when the CH1 ERR. LED is turned on
- CH2 ERR. LED ON signal (XnF) .... Turned ON when the CH2 ERR. LED is turned on

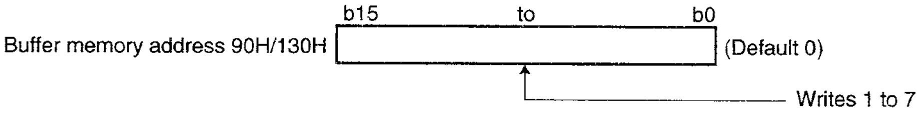
2 Buffer memory

Address and objective I/F (Hexadecimal (decimal))		Name		Stored value
CH1	CH2			
90H (144)	130H (304)	Mode switching	Switching mode No. designation	1: Dedicated protocol (format 1) to 7: Bidirectional protocol (See (a).)
91H (145)	131H (305)		Switching transmission specifications designation	0000H : Matched to switch setting 8000H to 86FFH : Arbitrarily set (See (b).)
203H (515)		Switch setting error, mode switching error storage		0: Normal Nonzero: Abnormal end (See Section 19.4.)

(a) Switching mode No. designation area (addresses: 90H, 130H)

① The mode No. [1] to [7] after mode switching is written to this area.

② The operation mode corresponding to the mode No. and the mode No. that can be designated for each interface are the same as when setting the mode switch. (See Section 4.3.1.)

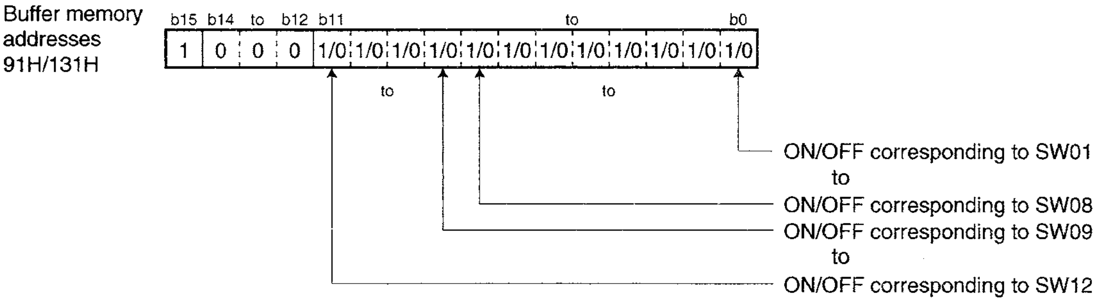


(b) Switching transmission specifications designation area (address: 91H, 131H)

① Designates the transmission specifications after mode switching.

② When the transmission specifications are returned to the contents set in the QC24(N) transmission specifications switches, [0000H] is written to this area.

③ When setting arbitrary transmission specifications (other that the contents set in the transmission specifications switches), the value corresponding to ON/OFF of the relevant bit in the illustration shown below is written.
Relevant bit 1 (ON)/0 (OFF) is designated the same as the ON/OFF setting of the corresponding QC24(N) transmission specifications switch.



1: Corresponding transmission specifications switch is ON
0: Corresponding transmission specifications switch is OFF

Setting bit	Corresponding switch	Designation item
0	SW01	Operation setting
1	SW02	Data bit setting
2	SW03	Parity bit setting
3	SW04	Even parity/odd parity setting
4	SW05	Stop bit setting
5	SW06	Sum check setting
6	SW07	Enable/disable write during RUN setting
7	SW08	Enable/disable setting modification setting
8	SW09	Transmission rate
9	SW10	
10	SW11	
11	SW12	

Note

The PLC CPU must also be aware of the following I/O signals for handshake and buffer memories when the mode is switched from an external device.

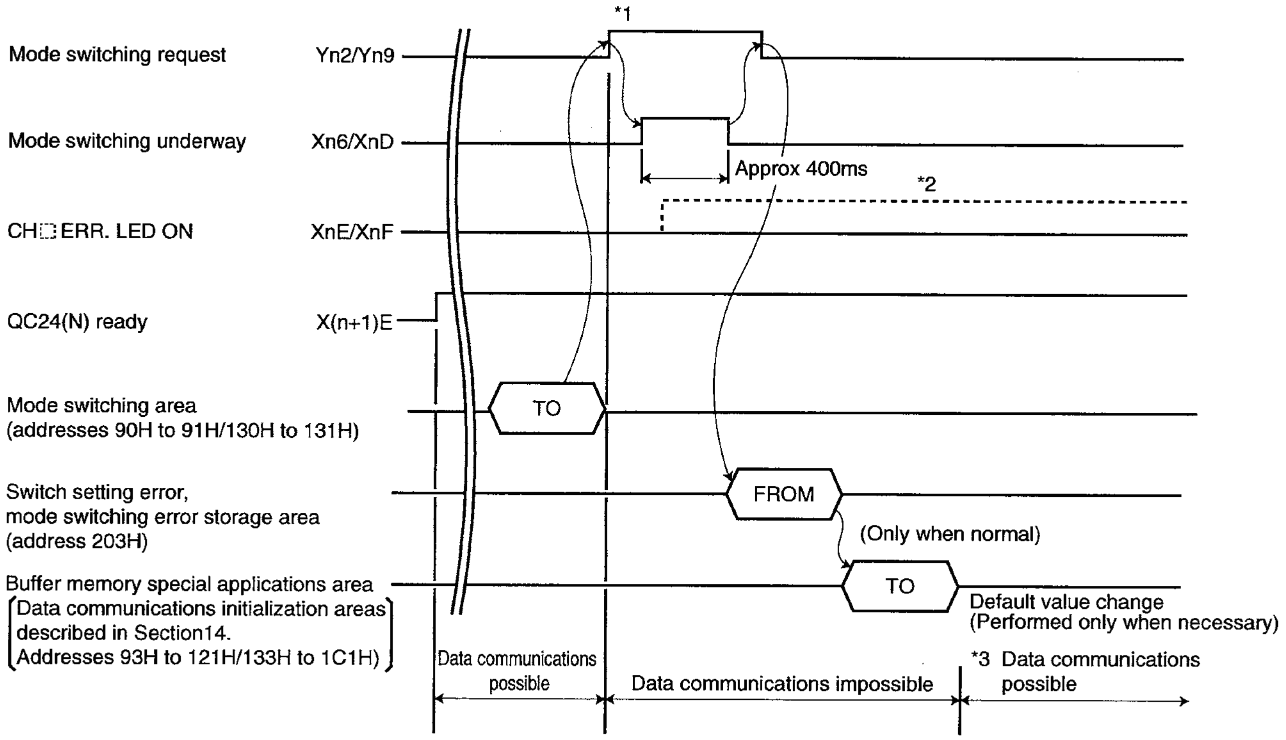
- Mode switching underway signal (Xn6/XnD)
- Switch setting error, mode switching error storage area (address: 203H)

18.4 Switching the Mode from the PLC CPU

This section describes how the QC24(N) is switched mode from the PLC CPU.

18.4.1 Mode switching procedure

The following describes the procedure for switching the QC24(N) mode from the PLC CPU.



*1 Inform in advance all the connected device that data communications by mode switching cannot be performed.

*2 When XnE and XnF were turned ON, check the error contents as described in Sections 19.1.3 and 19.4 and take the corresponding action.

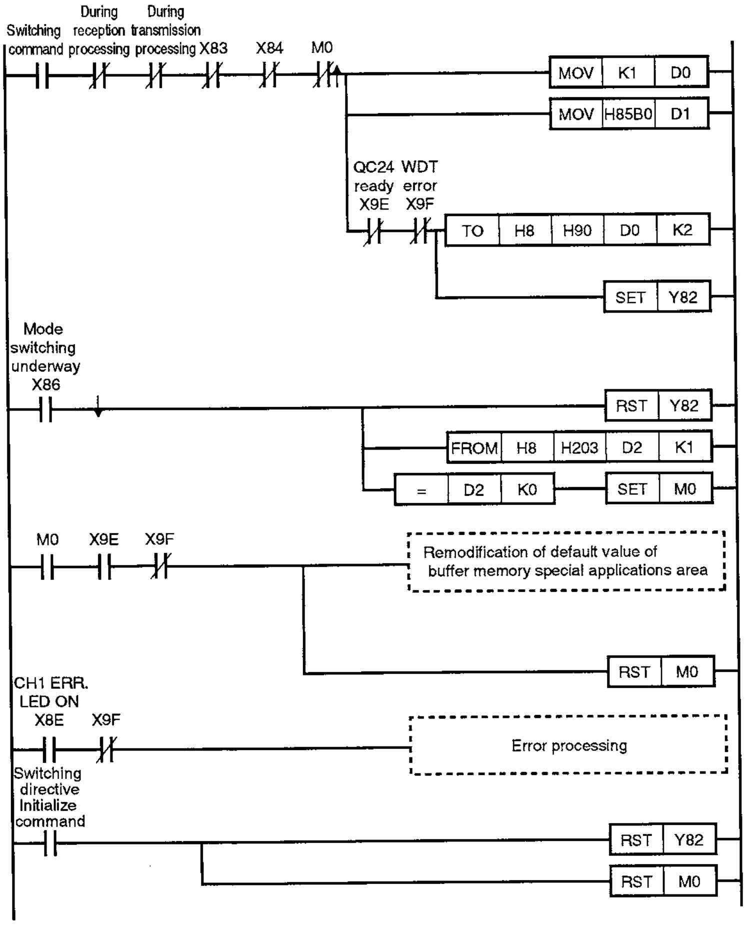
- Checking of buffer memory mode switching area mode switching designation contents and writing of mode switching designation contents within the range that can be designated
- Re-execution of mode switching

*3 After checking that mode switching was completed normally, inform all the connected devices that data communications are possible and restart data communications.
To check the QC24(N) operation mode (operation mode, transmission specifications) after switching, read the buffer memories (addresses: 252H to 253H, 262H to 263H) described in Section 19.5.

18.4.2 Mode switching sample program

The following shows a sample sequence program that switches the CH1 interface mode.

(QC24(N) I/O signals 80H to 9FH)



Sets the operation mode (dedicated protocol format 1).

Sets the transmission specifications.

Writes the mode switching designation contents.

Turns ON the mode switching request signal.

Turns OFF the mode switching request signal.

Reads the mode switching error contents.

When D2 is nonzero, checks the error contents and takes the action described in Sections 19.1.3 and 19.4.

Changes the default value again according to the data communications function used. (Necessary part only)

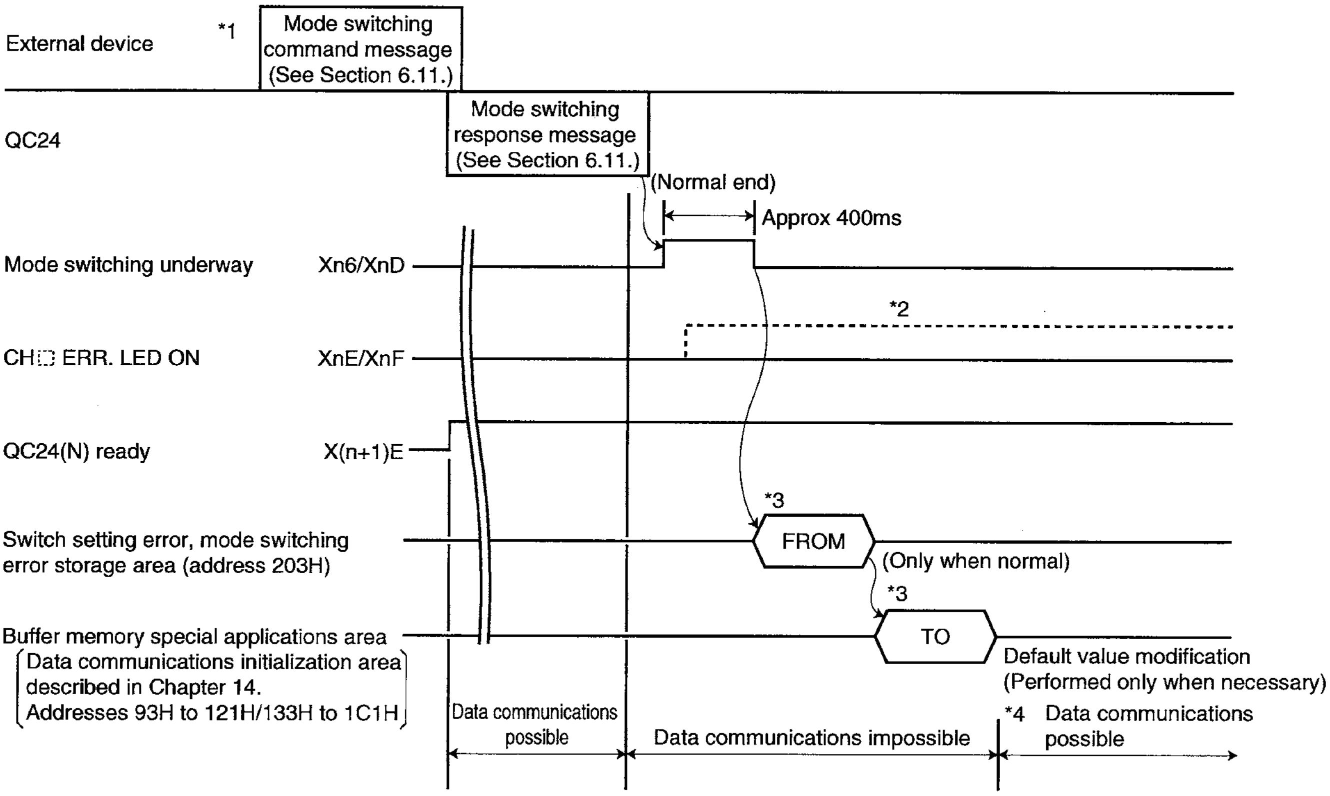
Reads the buffer memory (address 203H) and turns off the LED and clears the error code as described in Sections 19.1.3 and 19.4.

18.5 Switching the Mode from an External Device

This section describes how the QC24(N) mode is switched from an external device.

18.5.1 Mode switching procedure

The following describes the procedure for switching the QC24(N) mode from an external device.



*1 Inform in advance all the connected devices that mode switching has made data communications impossible.

*2 When XnE, XnF was turned ON, check the error contents and take the action described in Sections 19.1.3 and 19.4.

- Checking of buffer memory mode switching area mode switching designation contents and reading of mode switching designation contents within the range that can be designated.
- Re-execution of mode switching

*3 When the mode was switched from an external device, after mode switching is complete, read and write the buffer memory special applications area shown below from the PLC CPU.

- Switch setting error, mode switching error storage area (address: 203H)
- Data communications initialization areas (addresses: 93H to 121H/133H to 1C1H) described in Chapter 14.

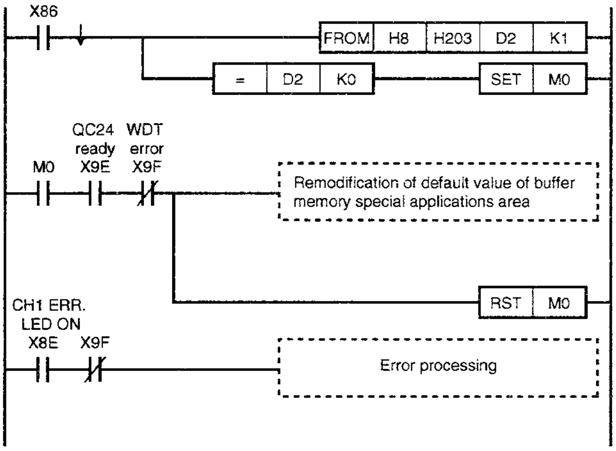
*4 After checking that mode switching was completed normally, inform all the connected devices that data communications are possible and restart data communications.

Note

To check the QC24(N) operation mode (operation mode, transmission specifications) after switching, read the buffer memory (addresses: 252H to 253H, 262H to 263H) described in Section 19.5.
(To check the external device, read the buffer memory with the dedicated protocol buffer memory read function.)

18.5.2 Mode switching sample program

The following shows a PLC CPU sample sequence program that switches the CH1 interface mode from an external device.
(QC24(N) I/O signals 80H to 9FH)



Reads the mode switching error contents.

When D2 is nonzero, check and process the error contents as described in Sections 19.1.3 and 19.4

Changes the default value again according to the data communications function used. (Necessary part only)

Reads the buffer memory (address 203H) and turns off the LED and clears the error code as described in Sections 19.1.3 and 19.4.

19. READING AND WRITING THE MODULE STATUS AND SIGNAL STATUS

This section describes, by purpose, the method used when an external device or the PLC CPU checks the QC24(N) status and turns off the LED after the start of data communications between external device and PLC CPU through the QC24(N).
Module status and signal status read and write described in this section are performed on the QC24(N) buffer memory special applications area.

Check the QC24(N) status and turn off the LED as described in each section below, as required.

19.1 LED ON Status Read and Turning Off

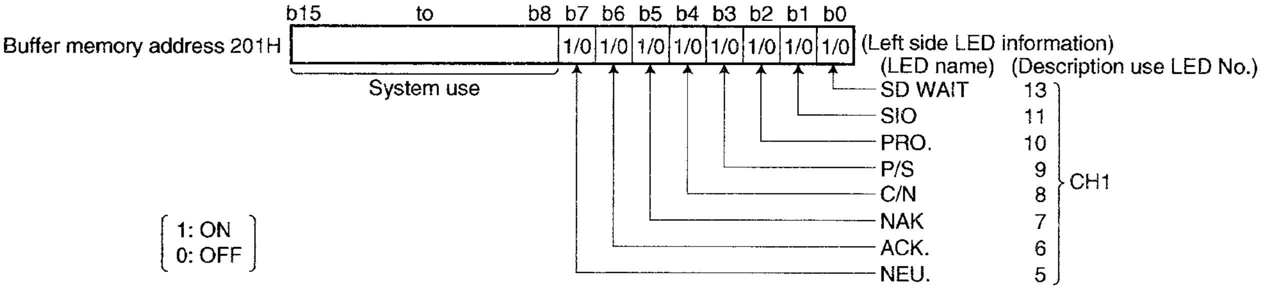
The following describes the LED ON/OFF status contents stored to the buffer memory and how any LED that are on are turned off.

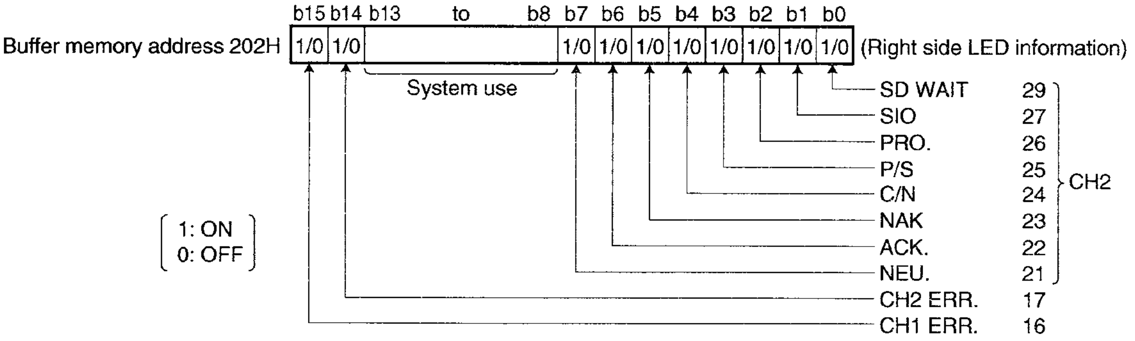
19.1.1 Reading the LED ON status

This function reads the status to check the LED ON status by transmission trouble, etc.

1 **LED ON status storage area (addresses: 201H to 202H)**

The LED ON/OFF status is stored to buffer memory addresses 201H to 202H as shown below.





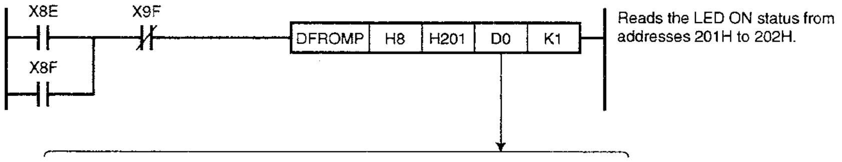
Note

See Section 4.4 for a description of the contents of 1 (ON)/0 (OFF) of each bit of the LED ON status storage area and Chapter 22 for a description of error processing.

2 LED ON status storage area read sample program

The following shows a sample program that reads the LED ON status.
(QC24(N) I/O signals 80H to 9FH)

- Example of FROM instruction use



	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
D0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
D1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

D0: When CH1 NEU., NAK, and PRO. are on.

D1: When CH1 ERR. and CH2 NEU. and ACK. are on.

19.1.2 Writing to turn off the LED

This operation turns off the LED shown in ② below.
The LED can be turned off by writing [1] to the relevant bit of buffer memory addresses 0H to 1H.
The following LED are turned ON and OFF.

① LED that are turned ON/OFF according to the status at that time, such as NEU. to NAK.
② LED that remain ON even after the error is cleared, such as C/N to SIO.

1 LED OFF request area (addresses: 0H to 1H)

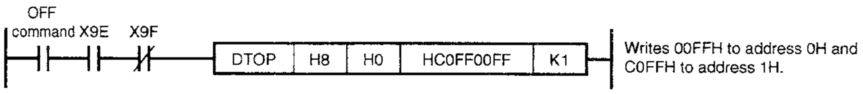
The OFF LED corresponding to each bit of the LED OFF request area are the same as the contents of the LED ON status storage area (addresses: 201H to 202H).
See Section 19.1.1 1.
The following shows the correspondence between the LED OFF request area and LED ON status storage area.

- LED OFF request area (address: 0H) → LED ON status storage area (address: 201H)
- LED OFF request area (address: 1H) → LED ON status storage area (address: 202H)

2 LED OFF sample program

The following shows a sample program that requests that all the objective LED be turned off.
(QC24(N) I/O signals 80H to 9FH)

- Example of TO instruction use



POINTS

(1) The OFF request is valid only when a write operation was executed.
When an OFF request is issued, the data in LED ON status storage area 201H to 202H is simultaneously cleared.
When a CH1 ERR. LED and CH2 ERR. LED OFF request was issued, the XnE and XnF signals are also turned OFF.
(2) After OFF processing, the data written to addresses 0H to 1H is cleared.
(3) If error contents remain when an OFF request was issued, the relevant LED will turn on again and the relevant bit of LED ON status storage area addresses 201H to 202H will also be turned ON (1).

19.1.3 Error handling program

The following describes a program that reads the error contents and turns off the LED when the CH1 ERR. LED or CH2 ERR. LED (hereafter abbreviated CH□ ERR. LED) was turned on.

1 **CH□.ERR LED ON cause**

When any of the errors shown below is generated, the error code is stored to the buffer memory corresponding to the interface (CH) that generated the error and the CH□ ERR. LED is turned on.

Error cause	Error code storage buffer memory			Objective protocol		
	Address		Name	Dedicated	Non procedure	Bi-directional
	CH1	CH2				
Switch setting error	203H		Switch setting error, mode switching error storage area	○	○	○
Mode switching error						
On-demand execution error	256H	266H	On-demand execution result storage area	○	×	×
Data transmission error	257H	267H	Data transmission result storage area	○	○	○
Data receive area	258H	268H	Data receive result storage area	○	○	○

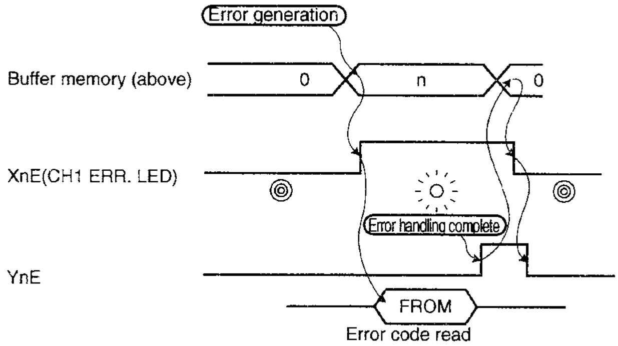
2 **Input signals that turn ON the CH□ ERR. LED and output signals that turn OFF the CH□ ERR. LED**

I/O signal		Signal name	Contents/function
Input signal	XnE	CH1 ERR. LED ON	Turned ON and OFF with ON and OFF of the CH1 ERR. LED.
	XnF	CH2 ERR. LED ON	Turned ON and OFF with ON and OFF of the CH2 ERR. LED.
Output signal	YnE	CH1 ERR. LED OFF request	Turned ON when the CH1 ERR. LED is off and the error code stored in the CH1 buffer memories shown in item 1 above is cleared.(*1)
	YnF	CH2 ERR. LED OFF request	Turned ON when the CH2 ERR. LED is OFF and the error code stored in the CH2 buffer memories shown in item 1 above is cleared.(*1)

*1 The QC24(N) LED is turned off and the error code is cleared using the following timings (the processing timing depends on the software version of the QC24(N)).

	QC24(N) and software version						
	Large-type QC24	Small-type QC24	Large-type QC24N	Small-type QC24N	Large-type QC24	Small-type QC24	Large-type QC24N
	Version Q and later	Version E and later	Version B and later	(All types)	Version P and before	Version D and before	Version A
Processing timing	Always perform while YnE and YnF are ON				Perform once when YnE or YnF switches ON from OFF		

(Example) When an error was generated at CH1



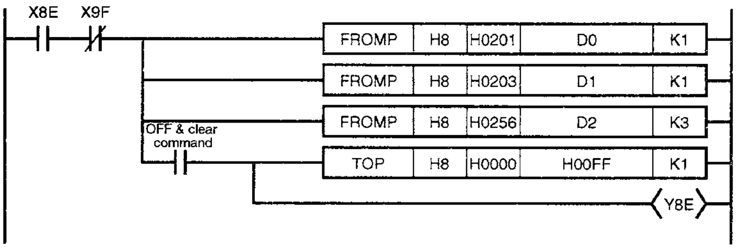
POINT

The CH1 ERR. LED and CH2 ERR. LED can be turned OFF by sending an OFF request to the buffer memory LED OFF request area (address 1H). The error code stored to the buffer memories shown above can also be cleared using the output signals YnE to YnF.

3 Sample error handler

The following shows sample programs that read the error code and turn off the LED when the CH1 interface generates one of the errors given in 1 above.
Program the necessary part.
(QC24(N) I/O signals 80H to 9FH)

① Data communications using a dedicated protocol



Reads the LED ON status from address 201H.

Reads the switch setting error contents from address 203H.

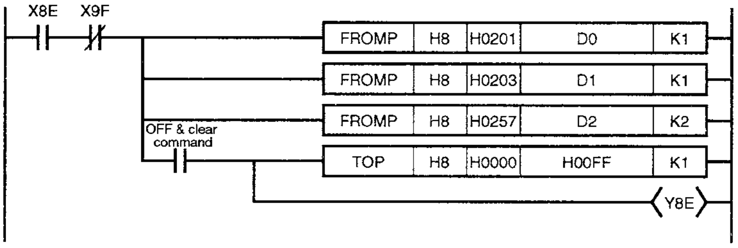
Reads the data transmit/receive results from addresses 256H to 258H.

Writes an LED OFF request to address 0H.

Requests that the CH1 ERR. LED be turned off and the buffer memory error code be cleared.

Check the error code and take the action described in Section 22.1.

② Data communications using non procedure protocol or bidirectional protocol



Reads the LED ON status from address 201H.

Reads the switch setting error contents from address 203H.

Reads the data transmit/receive results from addresses 257H to 258H.

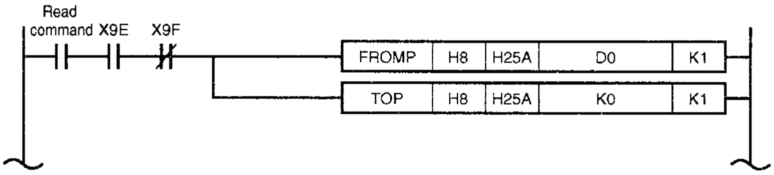
Writes an LED OFF request to address 0H.

Requests that the CH1 ERR. LED be turned off and the buffer memory error code be cleared.

Check the error code and take the action described in Section 22.1.

Note

If the QC24(N) sends an NAK message to the external device in reply to a command message during dedicated protocol data communications, the LED CH□ ERR. may not be turned ON.
The error code (see Section 22.1) corresponding to the error contents when an NAK response was sent to the external device is stored to the area shown below. (Different from the transmit error code during A compatible frame communications.)
When checking the transmitted error code at the PLC CPU, program the program shown below. (CH1 interface)



Reads the transmission error code from address 25AH.

Clears the error code.

Check the error code and take the action described in Section 22.1.

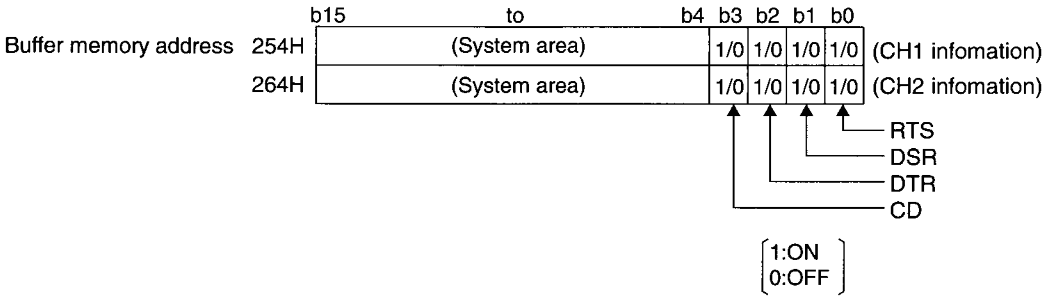
19.2 Reading the RS-232C Control Signals Status

This section describes how the status of the RS-232C communications control signals stored in the buffer memory are read.

This function is used to check the ON/OFF status of the RS-232C interface signals by transmission trouble, etc.

1 RS-232C control signals status storage area (addresses: 254H, 264H)

The status of the RS-232C signals are stored to buffer memory addresses 254H and 264H as shown below.



Notes

(1) See Section 3.2.1 for a description of the RS-232C signals.

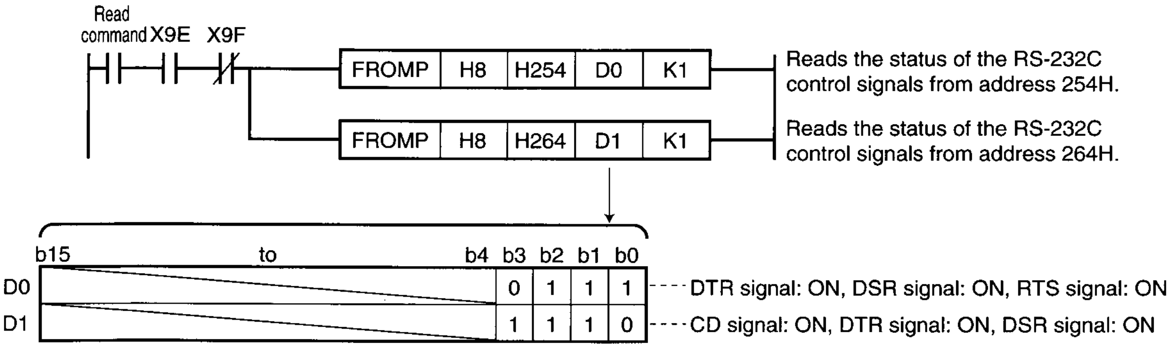
(2) The QC24(N) system (OS) controls the signals (RTS, DTR) output from the QC24(N). The sequence program cannot directly control these signals.

(3) The signal status stored in the buffer memories shown above is delayed up to 100 ms.

2 RS-232C control signals storage area read sample program

The following shows a sample program that reads the status of the RS-232C control signals. (QC24(N) I/O signals 80H to 9FH)

- Example of FROM instruction use



Reads the status of the RS-232C control signals from address 254H.

Reads the status of the RS-232C control signals from address 264H.

DTR signal: ON, DSR signal: ON, RTS signal: ON

CD signal: ON, DTR signal: ON, DSR signal: ON

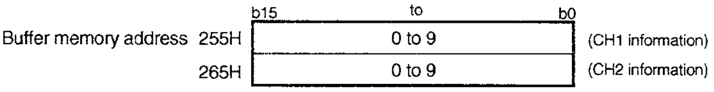
19.3 Reading the Data Communications Status (Transmission Sequence Status)

This section describes how the current dedicated protocol QC24(N) data communications status stored to the buffer memory are read.

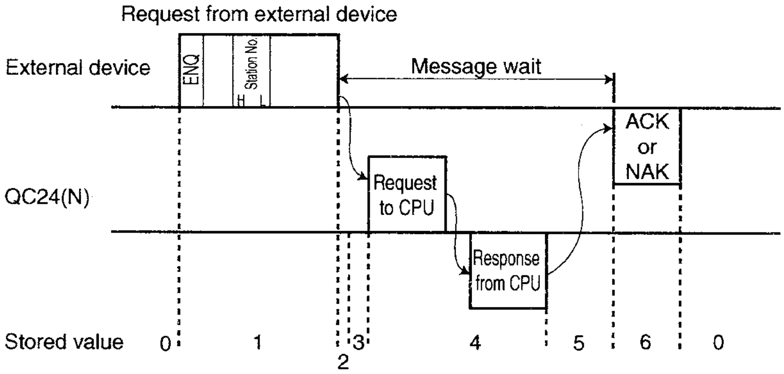
This function is used to check the dedicated protocol data communication status by transmission trouble generation, etc.

1 Transmission sequence status storage area (addresses: 255H, 265H)

The dedicated protocol QC24(N) data communications status is stored to buffer memory addresses 255H and 265H as a numerical value.



The following shows the correspondence between transmission sequence status area numerical value and data communications status.



★Stored values 7 to 9 are stored when [Mode switching] or [Transmission sequence initialize] was performed.

Notes

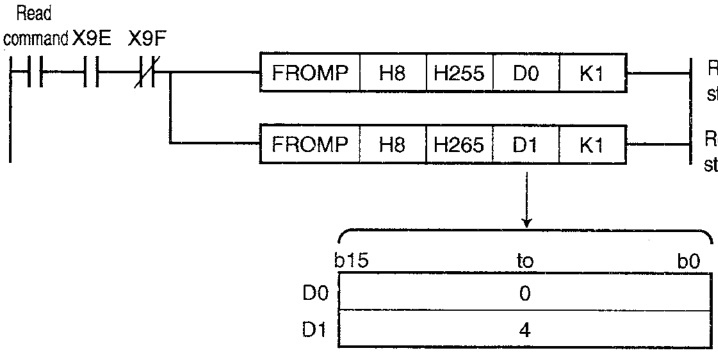
(1) See Section 5.8 for a description of the dedicated protocol transmission sequence.

(2) If the objective interface is not in the dedicated protocol mode, [0] is stored to the transmission sequence status storage area.

2 Sample program that reads the transmission sequence status storage area

The following shows a sample program that reads the transmission sequence status storage area.
(QC24(N) I/O signals 80H to 9FH)

- Example of FROM instruction use



Reads the CH1 data communication status from address 255H.

Reads the CH2 data communication status from address 265H.

CH1 waiting to receive a command, non procedure protocol or bidirectional protocol state.

State in which CH2 is accessing the PLC CPU in response to reception of a command message by the QC24(N).

19.4 Reading the Switches Setting Status

This section describes how the setting status of the QC24(N) switches stored to the buffer memory are read.

This function is used to read the setting contents of the switches mentioned above and to operate the system in accordance with the set contents when the QC24(N) starts.

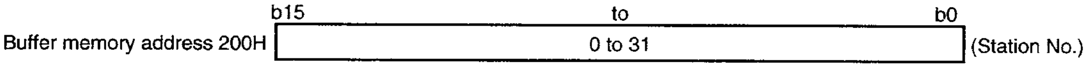
Notes

(1) The contents set in the mode switch and transmission specifications switches can be changed during mode switching (see Chapter 18).
(2) If a switch error occurs after mode switching, use the read function described in Section 19.5 to check the setting contents changed by the user.
(3) See Section 4.3 for a description of the setting contents of the mode switch, station No. switch, and transmission specifications switches.

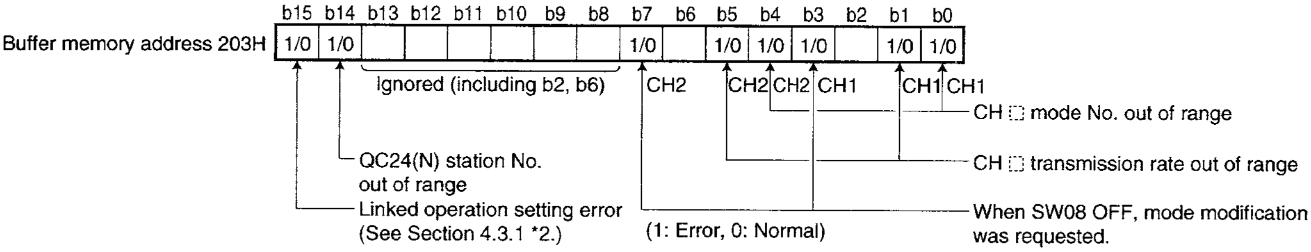
1 Setting status storage area

The setting contents and setting error information of the QC24(N) switches are stored to the buffer memory areas shown below.

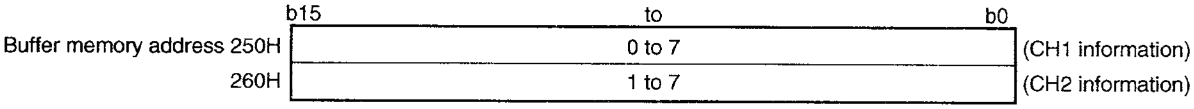
① Station No. switch setting status storage area (address: 200H)



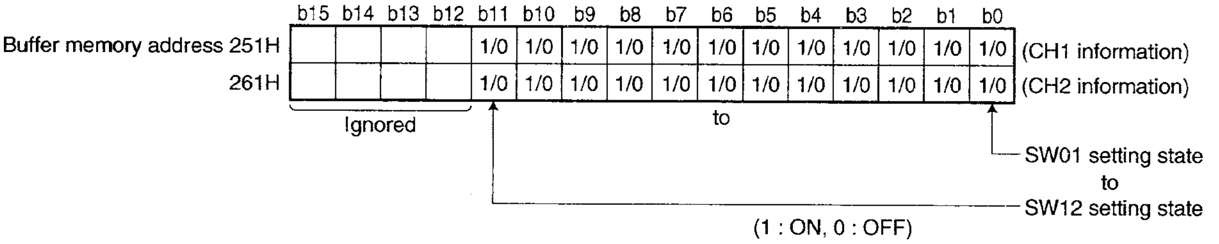
② Switch setting error, mode switching error storage area (address: 203H)



③ Mode switch setting status storage area (addresses: 250H, 260H)



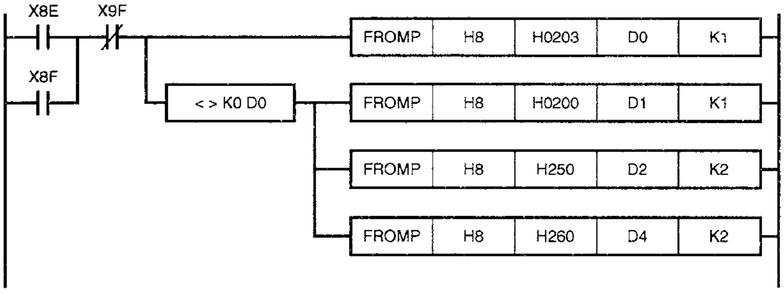
④ Transmission specifications switches setting status storage area (addresses: 251H, 261H)



2 Setting status storage area read sample program

The following shows a sample program that reads the QC24(N) switches setting status storage areas.
See Section 19.1.3 for a description of I/O signals X8E and X8F used in this program.
(QC24(N) I/O signals 80H to 9FH)

- Example of FROM instruction use



Reads the error contents from address 203H.

Reads the contents set in the station No. switch from address 200H.

Reads the contents set in the CH1 mode switch and transmission specifications switches from addresses 250H to 251H.

Reads the contents set in the CH2 mode switch and transmission specifications switches from addresses 260H to 261H.

After checking the error code and resetting the switches, restart the QC24(N).

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0		
D0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Error contents (1....Mode No. setting error)	
D1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	QC24 set station No. (0)	
D2	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	CH1	Mode switch set mode No. (8) SW02, SW04, SW09, SW11 = ON
D3	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0		
D4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	CH2	Mode switch set mode No. (1) SW02, SW04, SW06, SW07, SW09, SW11 = ON
D5	0	0	0	0	0	1	0	1	0	1	1	0	1	0	1	0		

Shows the CH1 mode No. setting error status.

19.5 Reading the Current Operation Mode

This section describes how the QC24(N) current operation mode stored to the buffer memory is read.

This function is used to check the setting contents changed by the user due to generation of a switch setting error after mode switching (see Chapter 18).
The setting of the QC24(N) mode switch and transmission specifications switches can be changed when the mode is switched. If there is an error in the contents set during mode switching, an switch setting error will be generated.

Notes

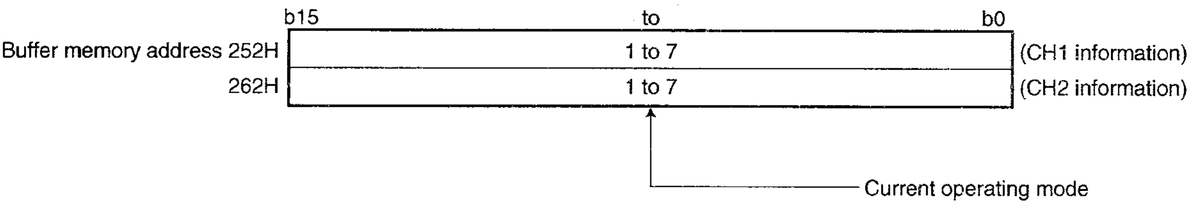
(1) The setting status of the QC24(N) switches can be checked using the read function described in Section 19.4.

(2) See Section 4.3 for a description of the contents set in the mode switch and transmission specifications switches.

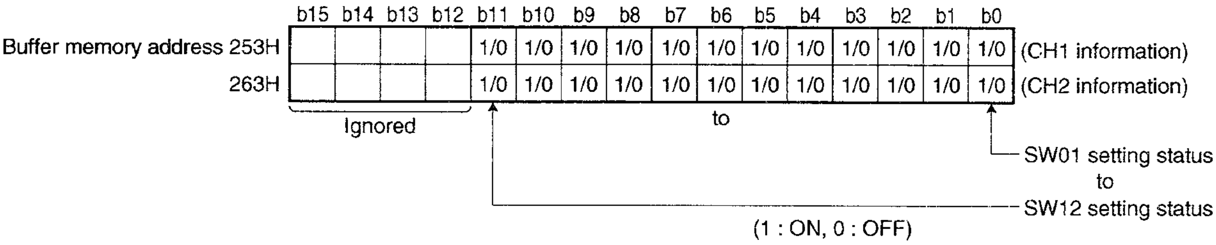
1 Operation mode status storage area

The current QC24(N) operation mode status is stored to the buffer memory areas shown below.

① Mode setting status storage area (addresses: 252H, 262H)



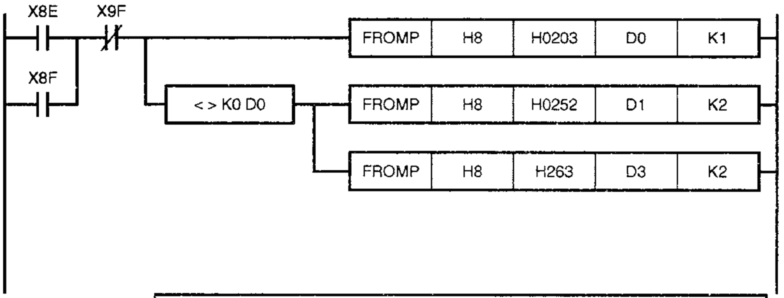
② Transmission specifications setting status storage area (addresses: 253H, 263H)



* The CH1 SW13 (off setting) information is not stored.

2 Operation mode status storage area read sample program

The following shows a sample program that reads the QC24(N) current operation mode status storage area.
See Section 19.1.3 for a description of I/O signals X8E and X8F used in this program.
(QC24(N) I/O signals 80H to 9FH)



Reads the error contents from address 203H.

Reads the CH1 mode setting status and transmission specifications setting status from addresses 252H to 253H.

Reads the CH2 mode setting status and transmission specifications setting status from addresses 262H to 263H.

After checking the error code and setting value modification contents, designate the correct set values and switch the mode.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0		
D0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Error contents (2....CH1 transmission rate error)	
D1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	CH1	Mode No. 6 is being set. SW02, SW04, and SW09 to SW12 are being set by ON designation.
D2	0	0	0	0	1	1	1	1	0	0	0	0	1	0	1	0		
D3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	CH2	Mode No. 1 is being set. SW02, SW04, SW06, SW07, SW09, and SW11 are being set by ON designation.
D4	0	0	0	0	0	1	0	1	0	1	1	0	1	0	1	0		

CH1 is the non procedure protocol and CH2 is a dedicated protocol (format 1) setting state and shows the CH1 transmission rate setting error state.

19.6 Clearing the PLC CPU information

This section explains how to clear the PLC CPU information.

This method is available only for the A1SJ71QC24N1(-R2) of software version B or later.

(1) PLC CPU information

(a) This is information about the access target CPU type used in dedicated protocol communications.
The Q series C24 obtains this information from the access target CPU at the time of initial access, and stores it inside the A1SJ71QC24N1(-R2).
Since access is made based on this information, the processing speed will be increased from the second access.

(b) The PLC CPU information is cleared in the following cases:
- When the PLC is powered OFF and then ON, or when the CPU module is reset
- When the PLC CPU information clear request is executed

(2) If the PLC CPU information has not been correctly obtained

The following problems may occur:
- Accessible device range is narrowed. (Error code: 7140H)
- Some of commands and/or devices cannot be used. (Error code: 7142H, 714DH), etc.

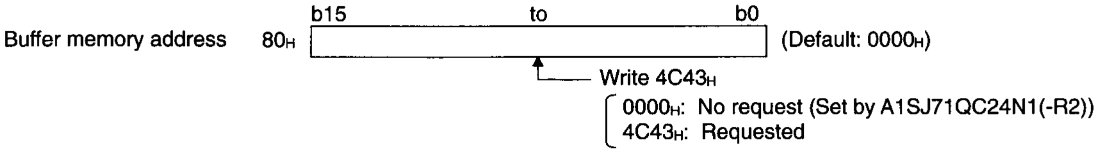
In the above case, execute the PLC CPU information clear request.

POINT

If initial access is made at startup of the access target CPU or while the network is unstable, the PLC CPU information may not be correctly acquired.

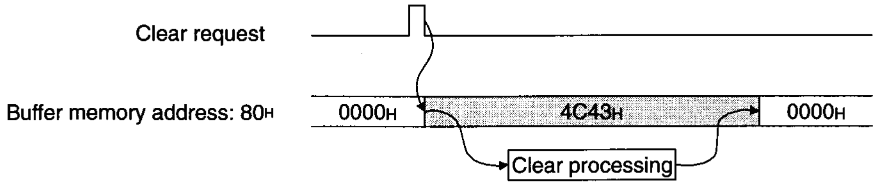
(3) Operation of the PLC CPU information clear request

(a) Write "4C43H" to the PLC CPU information clear request area (address: 80H) in the buffer memory. (Set by the user)



(b) The PLC CPU information clear processing of the A1SJ71QC24N1(-R2) is executed. *1

(c) Upon completion of the clear processing, "0000H" is written to the PLC CPU information clear request area (address: 80H) in the buffer memory. (Set by the A1SJ71QC24N1(-R2))



*1 The transmission sequence status area (address: 255H/265H) in the buffer memory is also initialized.

(4) Executing the PLC CPU information clear request

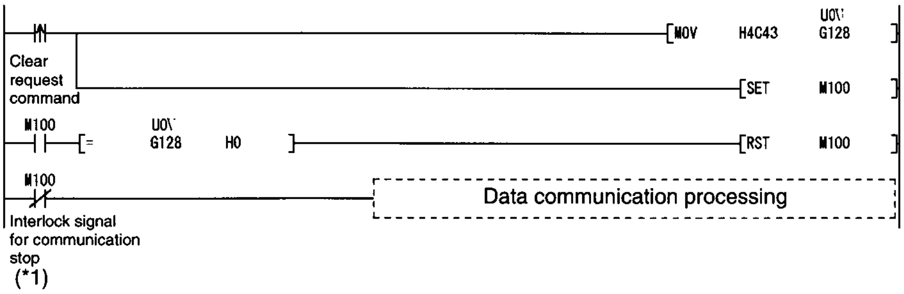
(a) Executing from GPP function peripheral device

1) On the Device test screen, set "4C43H" to buffer memory address 80H.

2) On the Buffer Memory Batch monitor screen, check that the value in buffer memory address 80H is "0000H".

(b) Executing from sequence program

In the following program, turning on the clear request command clears the PLC CPU information of the A1SJ71QC24N1(-R2) that is mounted in the position corresponding to I/O signal X/Y00 to X/Y1F.



PLC CPU information clear request

Turns ON the interlock signal for communication stop during clear processing. *1

After completing clear processing, turns OFF the interlock signal for communication stop. *1

*1 Create a program in which data communication processing will not be performed while the interlock signal for communication stop (M100) is ON.

(5) Precautions

(a) Execute the PLC CPU information clear after communication with the external device is stopped.

And, do not perform communication with the external device during the PLC CPU information clear processing. (If any data are received from the external device during the clear processing, the data will be discarded.)

(b) Do not execute the PLC CPU information clear during execution of the ONDEMAND/OUTPUT/PRR/BIDOUT instruction. Also, do not execute the ONDEMAND/OUTPUT/PRR/BIDOUT instruction during the PLC CPU information clear.

Doing so may result in unsuccessful completion of dedicated instructions.

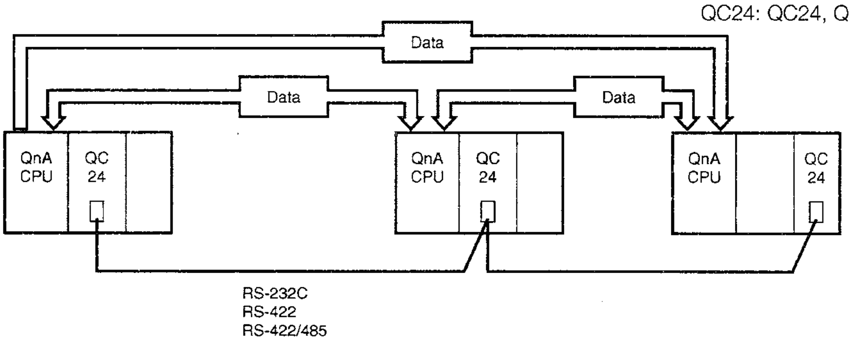
(c) When a modem is connected, cut off the line linked with the external device before executing the PLC CPU information clear. (The line is cut off at execution of the PLC CPU information clear.)

20. WHEN A QnACPU USES A LINK DEDICATED INSTRUCTION TO ACCESS ANOTHER STATION'S PLC CPU

A QnACPU can exchange data with another station's QnACPU in a multidrop link through the QC24(N) by executing a link dedicated instruction.

This section describes the link dedicated instructions used when a given QnACPU communicates data with another station's QnACPU through the QC24(N).

QC24: QC24, QC24N



POINT

See the programming manual (special function module) for a detailed description of the functions and use of the link dedicated instructions.

20.1 Accessing Another Station Using a Link Dedicated Instruction

This section outlines data communications by QC24(N) operation mode and link dedicated instruction.

1 QC24(N) operation mode

If an QC24(N) is set as shown below, another station can be accessed through that QC24(N).

① Operation mode set to a dedicated protocol (format1 to format5). (See Section 4.3.1.)
② Link operation disabled. (See Section 4.3.1 *2.)

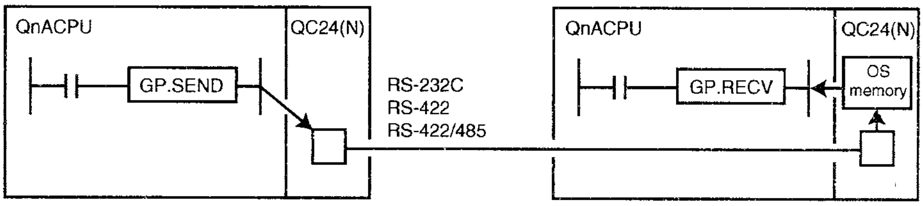
2 Overview of data communications using link dedicated instructions

The following outlines data communications with another station's QnACPU using link dedicated instructions.

① SEND/RECV instructions

These instructions use the QC24(N) OS memory to communicate data between QnACPUs.

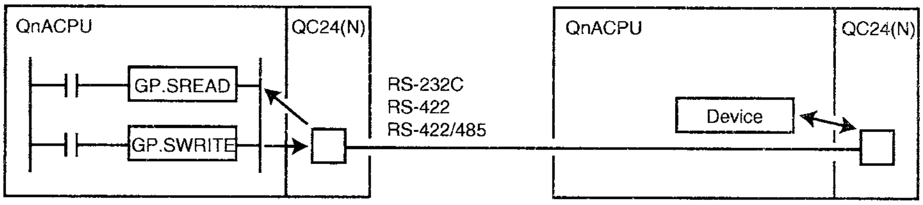
- SEND .... Writes the designated data to the OS memory of the designated QC24(N).
- RECV .... Reads the data from the local station QC24(N) OS memory.



② READ/WRITE (SREAD/SWRITE) instructions

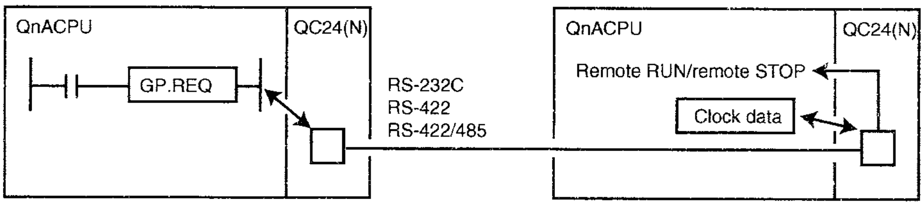
These instructions read data from and write data to the device memory of the designated station's QnACPU.

- READ (SREAD) .... Reads the data of the device memory of the designated station's QnACPU.
- WRITE (SWRITE) ..... Writes the data of the device memory of the designated station's QnACPU.



③ REQ instruction

This instruction reads and writes the status control (remote RUN/remote STOP) or clock data of the designated station's QnACPU.



20.2 Range of Access to Another Station

This section describes the stations that can be accessed through the QC24(N) using link dedicated instruction.
In the following descriptions, the stations that can be accessed are represented by [Target station-1].

[Target station-1]

(1) Through QC24(N) only. This is access between QnACPUs when QC24(N)s are interconnected by RS-232C, RS-422, or RS-422/485 interface.

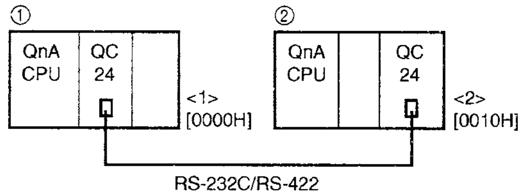
(2) The connected QnACPU (QnACPU ① to ⑨ in the illustration shown below) can communicate data using the link dedicated instructions.

(3) Access between QnACPUs is possible even when QC24(N)s are interconnected by RS-422/485 interface and external devices are connected on the line.
(When QC24(N) are interconnected by RS-232C/Rs-422 interface)....1: 1 connection is possible.

(Example)

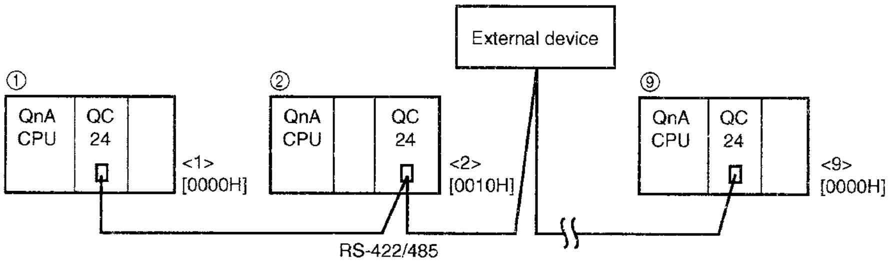
Meaning of symbols at right side of QC24-equipped station
< >: QC24 set station No.
[ ]: QC24 head I/O signal

QC24: QC24, QC24N



(When QC24(N) interconnected by RS-422/485 interface)....1:1, 1: n, and m: n connections are possible.

(Example)



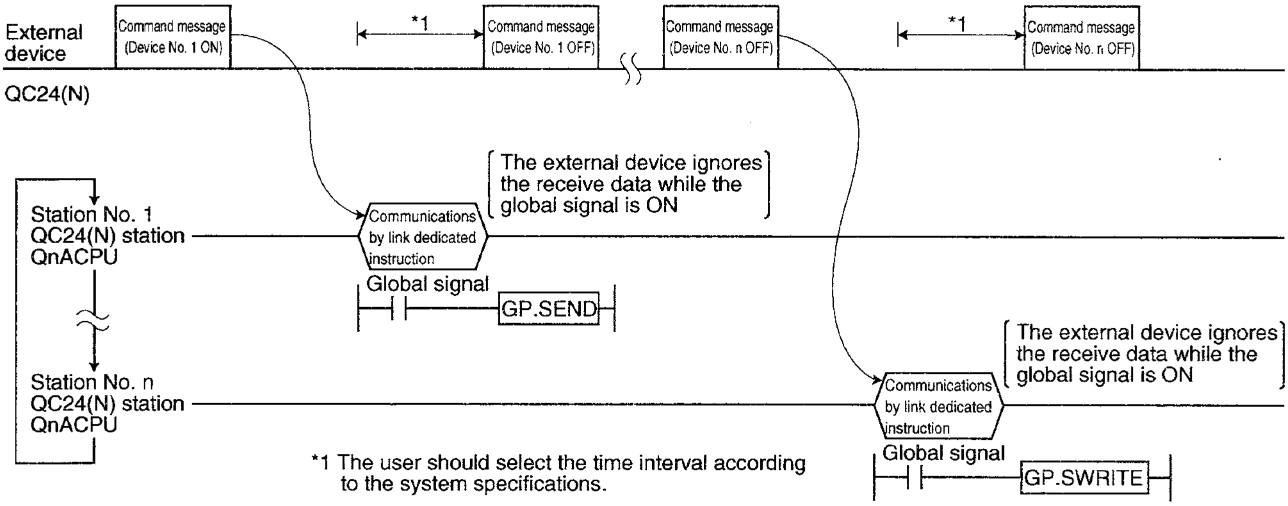
20.3 Precautions when Accessing Another Station

The following describes the precautions which should be observed when using the link dedicated instructions to access another station through a QC24(N).

1 Interlock between external devices and QnACPU

When external devices and QnACPU are connected in a 1: n or m: n configuration, the external devices and QnACPU must be interlocked so that the external devices and QnACPU do not use the RS422/485 line at the same time.
An interlock example is shown below.

(Example) An external device uses the dedicated protocol global function described in Section 6.8 to control execution of the QnACPU link dedicated instructions.



*1 The user should select the time interval according to the system specifications.

2 Simultaneous execution of multiple instructions

A QnACPU cannot execute two or more link dedicated instructions simultaneously by designating the same interface (CH1 or CH2) of the intervening QC24(N).
Always execute the next link instruction after data transmission and reception by the preceding link dedicated instruction is complete.
Simultaneous execution will abnormally end the program.

3 Wiring connection for access through RS-422/485 interface

When accessing another station through the QC24(N) RS-422/485 interface, when the RS-422/485 interface system configuration is 1: n, connect the external devices and QC24(N) on the line with the m: n configuration wiring connection method described in Section 4.7.4 (c).

20.4 Link Dedicated Instructions

This section describes how the instructions are used when a QnACPU uses link dedicated instructions to access another station through the QC24(N).

20.4.1 Transmitting and receiving data (SEND, RECV)

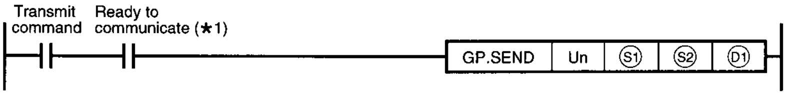
This section describes the SEND/RECV instructions when the OS memory of the designated QC24(N) is used to communicates data between QnACPUs.

1 **SEND instruction**

[Function]

Transmits data to the designated transmission destination station.

[Instruction format]



★1 Signal agreed upon with external device.

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/O No. (Transmit side) When I/O signals are represented by 4 digits, this No. is designated by the most significant 3 digits.	0000H to 00FEH	○	
(S1)	Control data storage head device Designates the local station head device that stores the control data.	Word device *2	○	○
(S2)	Send data storage device Designates the local station head device that stores the send data.	Word device *2	○	
(D1)	Transmission complete device Designates the local station device that is turned on for one scan when transmission is complete. (D1) .... OFF: Incomplete ON: Complete (D1) + 1 ...... OFF: Normal ON: Abnormal	Bit device *1 Word device bit specification *3		○

*1 : Bit device .... X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification .... Word device . Bit number

[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S1)	b15 to b1 b0 0 | 1/0 Execution timer (bit 0) 0: Do not confirm arrival Ends SEND instruction execution when transmission of the send data is complete. 1: Confirm arrival Ends SEND instruction execution when the send data arrives at the transmission destination station.	0000H 0001H	○	
(S1) + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error codes.)	0 or more		○
(S1) + 2	Local station channel Designates the local station QC24(N) interface that transmits data.	1: CH1 2: CH2	○	
(S1) + 3	Target station storage channel Designates the transmission destination station QC24(N) interface that transmits data as the same interface as (S1) + 2 above.	1: CH1 2: CH2	○	
(S1) + 4	Target station network No.	0	○	
(S1) + 5	Target station No.	0	○	
(S1) + 6	Special function module station No. Designates the QC24(N) station No. (0 to 31) of the target station when transmitting to [Target station-1].	0 to 31	○	
(S1) + 7	Number of retransmissions Send request: Designates the number of retransmissions when data cannot be transmitted when (S1) is 0001H (execution type [1]). Transmission complete: Stores the number of retransmissions at normal end/abnormal end.	0 to 15	○	○
(S1) + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of execution of the SEND instruction when (S1) is 0001H (execution type [1]). If data cannot be transmitted within the monitoring time, it is retransmitted (S1) + 17 times.	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
(S1) + 9	Send data length (units: words) Designates the number of send data designated by (S2).	1 to 480	○	
(S1) + 10	(Not used)	—	—	—
to				
(S1) + 15				
(S1) + 16	Error detection network No.	—	—	—
(S1) + 17	Error detection station No.			

POINT

The number of resends ((S1) +7) must be set every time an instruction is executed.

[Caution]

① The QC24(N) can only store the data transmitted at one time by SEND instruction.
Execute the SEND instruction with arrival confirmation of control data execution type Ⓢ1 as much as possible.

② Provide the following number of words of contiguous area at the word device used by the SEND instruction.

- Ⓢ1 (control data storage device) .... 18 words
- Ⓢ1 (send data storage head device)....... Size designated by Ⓢ1 + 9 (send data length).

③ When control data execution type is made "Do not confirm arrival" (Ⓢ1 bit 0 = OFF), the following control data does not have to be designated.

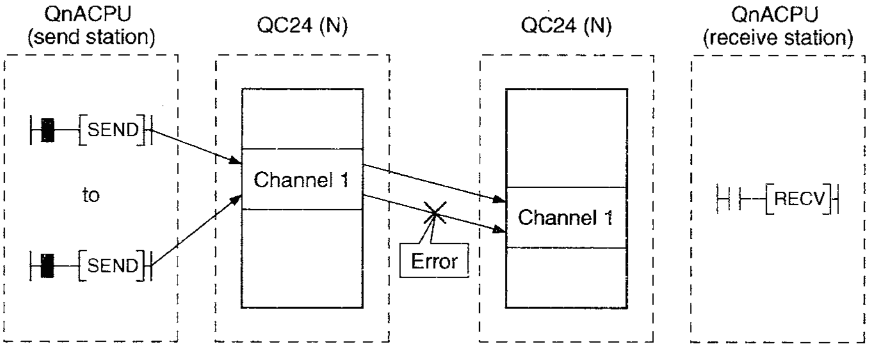
- Ⓢ1 + 7....Number of retransmissions
- Ⓢ1 + 8....Arrival monitoring time

④ When sending data to the same channel of the receiving station, send data after the receiving station has read the data using the RECV instruction.

When "no delivery confirmation" is set as the execution type, the execution completes normally on the sending station even if the contents of the transmission data are abnormal, if the communication is completed normally.

Also, even if the contents of the transmission data is normal, if multiple stations execute instructions to the same station, the sending station will result in a time-out error.

⑤ If the execution type is set to "delivery confirmation", the sending station sends data to the same channel of the receiving station before the receiving station reads the data using the RECV instruction, the receiving terminal will result in a buffer-full error.

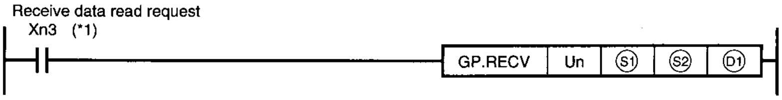


2 RECV instruction

[Function]

Reads the receive data transmitted by SEND instruction.

[Instruction format]



*1 CH1: Xn3
CH2: XnA

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/O No. (transmitting side) When the I/O signals are represented by 4 digits, this No. is designated by the most significant 3 digits.	0000H to 00FEH	○	
(S1)	Control data storage head device Designates the local station head device that is to store the control data.	Word device *2	○	○
(S2)	Receive data storage head device Designates the local station head device that is to read the receive data.	Word device *2	○	○
(D1)	Receive end device Designates the local station device that is turned ON for 1 scan by receive data read complete. (D1) .... OFF: Incomplete, ON: Complete (D1) + 1 ..... OFF: Normal, ON: Error	Bit device *1 Word device bit specification *3		○

*1 : Bit device .... X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification .... Word device . Bit number

[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Ⓢ1	Abnormal end type	0000H	○	
Ⓢ1 + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error code.)	0 or more		○
Ⓢ1 + 2	Local station channel Designates the No. of the QC24(N) interface that is to read the receive data.	1: CH1 2: CH2	○	
Ⓢ1 + 3	Transmission source station channel The No. of the QC24(N) interface that transmitted the data of the transmission source station is stored.	1: CH1 2: CH2		○
Ⓢ1 + 4	Transmission source station network No.	0		○
Ⓢ1 + 5	Transmission destination station No.	0		○
Ⓢ1 + 6 Ⓢ1 + 7	(Not used)	—	—	—
Ⓢ1 + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of RECV instruction execution. When data cannot be received within the monitoring time, the instruction is abnormally ended.	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
Ⓢ1 + 9	Receive data length (units: words) Stores the number of words of receive data stored to the device designated by Ⓢ2.	1 to 480		○
Ⓢ1 + 10 to Ⓢ1 + 15	(Not used)	—	—	—

[Caution]

① The QC24(N) can only store the data transmitted at one time by SEND instruction.
When transmitting data, execute the SEND instruction by control data execution type (Ⓢ1) "arrival confirmed" as much as possible.

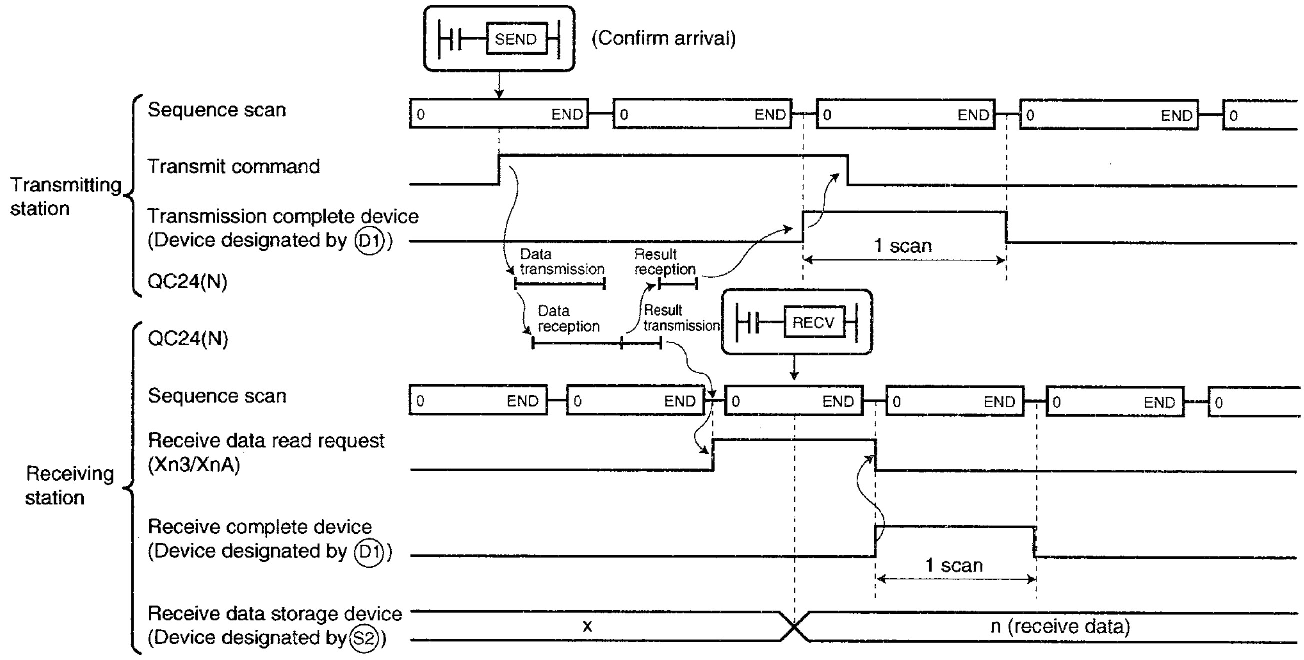
② Provide a contiguous area of the following number of words at the word device used by the RERCV instruction.

- Ⓢ1 (control data storage device) .... 16 words
- Ⓢ2 (receive data storage head device) .... Size of data transmitted by SEND instruction

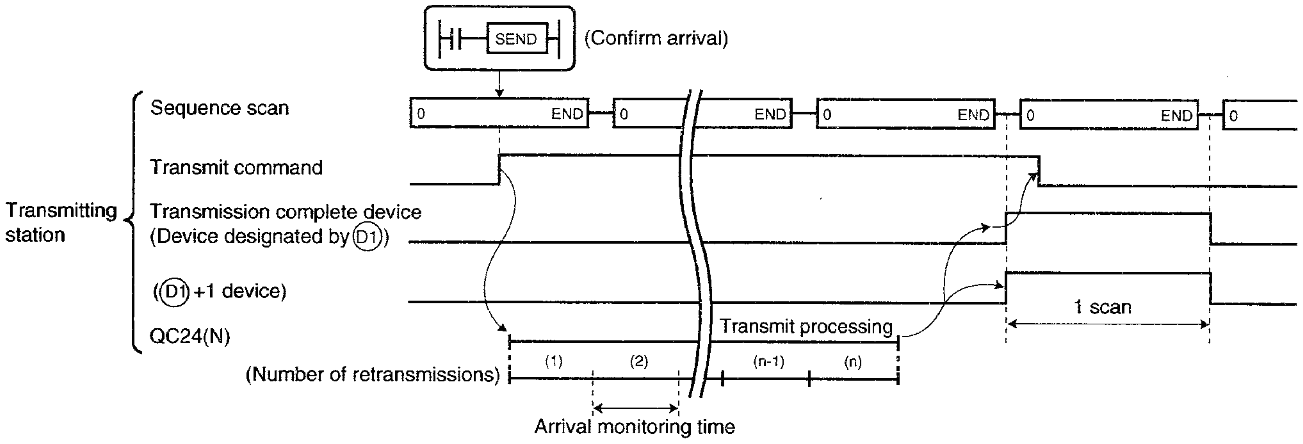
③ If the receive data is not read within the arrival monitoring time designated by control data Ⓢ1 + 8, the instruction is abnormally ended.

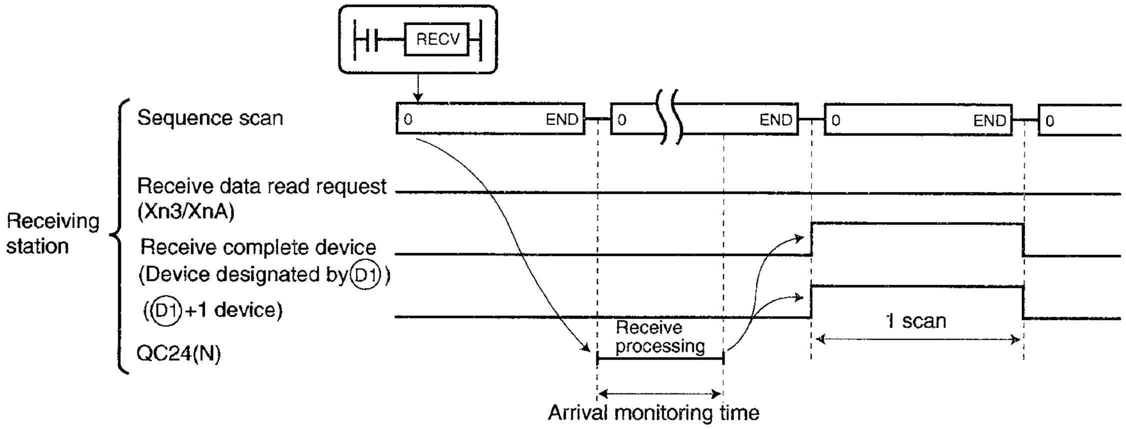
3 Instruction execution timing (Reception between multidrop link stations)

(Normal end)



(Abnormal end)

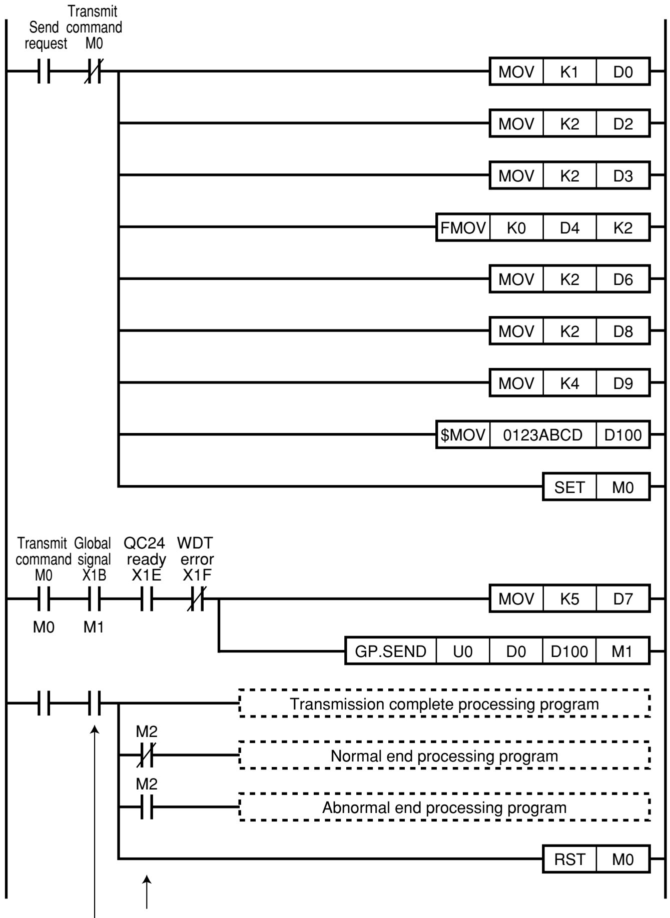




4 Sample program

The following shows a sample program that transmits data from station ① to station ② with the multidrop link system of [Target station-1] described in Section 20.2.

(a) Station ① SEND instruction sample program



Sets the control data.
Sets (Ⓢ1) execution type.
Sets (Ⓢ1 + 2) local station channel (CH2).
Sets the (Ⓢ1 + 3) target station storage channel (CH2).
Sets (Ⓢ1 + 4) to (Ⓢ1 + 5).
Sets the (Ⓢ1 + 6) special function module station No. (target station Q24).
Sets (Ⓢ1 + 8) arrival monitoring time (2 seconds).
Sets (Ⓢ1+ 9) send data length (4words).
Sets the send data.
Sets the transmit command flag.

Sets (Ⓢ1 + 7) number of retransmissions (5 times).

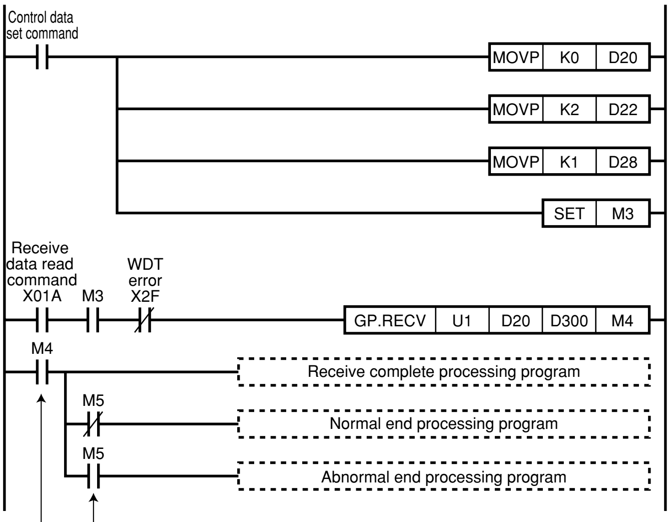
SEND instruction execution.
X1B is the signal agreed upon with the external device to allow line use. (See Section 20.3.)

Performs processing according to the error code of D1 that stores the (Ⓢ1 + 1) end status. (See Section 22.1.3.)

M2 is turned ON/OFF according to SEND instruction normal end/abnormal end.

Completion of execution of SEND instruction turns M1 ON for 1 scan.

(b) Station ② RECV instruction sample program



Sets the control data.
Sets (Ⓢ1) abnormal end type.
Sets (Ⓢ1 + 2) local station channel (CH2).
Sets (Ⓢ1 + 8) arrival monitoring time (1second).
Sets the control data designation complete flag.

RECV instruction execution.

Performs processing according to the error code of D21 that stores the (Ⓢ1 + 1) end status. (See Section 22.1.3.)

M5 is turned ON/OFF according to RECV instruction normal end/abnormal end.

Completion of execution of the RECV instruction turns on M4 for one scan.

20.4.2 Reading/writing other station word device (READ, WRITE)

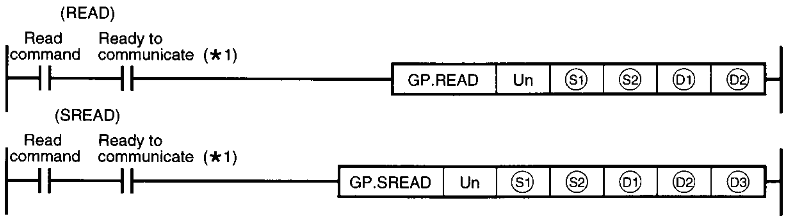
The following describes the READ/WRITE instructions when reading and writing the designated station's QnACPU word device memory.

1 READ instruction

[Function]

Reads the designated station's QnACPU word device memory.
When the SREAD instruction is used, the user-designated bit device of the target station's QnACPU is turned on for one scan when the word device memory is read.

[Instruction format]



★1 Signal agree upon with the external device.

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/O No. Designated by the higher 3 digits when the I/O signals are represented by 4 digits.	0000H to 00FEH	o	
(S1)	Control data storage head device Designates the local station head device that is to store the control data.	Word device *2	o	o
(S2)	Read data storage head device (target station) Designates the target station head device that stores the data to be read.	Word device *2	o	
(D1)	Read data storage head device (local station) Designates the local station head device that stores the read data.	Word device *2		o
(D2)	Read end device (local station) Designates the local station device that is turned on for 1 scan by read complete. (D2) .... OFF: Incomplete, ON: Complete (D2) + 1 .... OFF: Normal, ON: Error	Bit device *1 Word device bit specification *3		o
(D3)	Read report device (target station) Designates the target station device that is turned on for 1 scan by reading. (D3) .... OFF: Incomplete, ON: Complete	Bit device *1 Word device bit specification *3		o

*1 : Bit device ....X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification ....Word device . Bit number

[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S1)	Execution type	0001H	○	
(S1) + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error code.)	0 or more		○
(S1) + 2	Local station channel Designates the local station QC24(N) interface that is to transmit the send request.	1: CH1 2: CH2	○	
(S1) + 3	(Not used)	—	—	—
(S1) + 4	Target station network No.	0	○	
(S1) + 5	Target station No.	0	○	
(S1) + 6	Special function module station No. Designates the target station QC24(N) station No. (0 to 31) when reading from [Target station-1].	0 to 31	○	
(S1) + 7	Number of retransmissions Read request: Designates the number of transmissions of the request when data cannot be read. Read complete: Stores the number of retransmissions at normal end/abnormal end.	0 to 15	○	○
(S1) + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of execution of the READ instruction. If data is not read within the monitoring time, the read request is retransmitted (S1) + 7 times. (Retransmission)	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
(S1) + 9	Read data length (units: words) Designates the number of words of data to be read from the device designated by (S2).	1 to 480	○	
(S1) + 10 to (S1) + 15	(Not used)	—	—	—
(S1) + 16	Error detection network No.	—	—	—
(S1) + 17	Error detection station No.			

[Caution]

① Provide a contiguous area of the number of words shown below at the word device used by the READ instruction.

- Ⓢ1 (control data storage device) .... 18 words
- Ⓓ1 (read data storage head device) .... Size designated by Ⓢ1 + 9 (read data length)

POINT

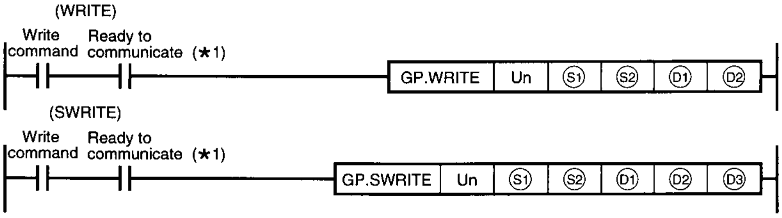
The number of resends (Ⓢ1 +7) must be set every time an instruction is executed.

2 WRITE instruction

[Function]

Writes to the device memory of the designated station's QnACPU.
When the SWRITE instruction is used, the user-designated bit device of the target station's QnACPU is turned on for 1 scan when the word device memory was written.

[Instruction format]



★1 Signal agreed upon with the external device.

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/O No. When the I/O signals were represented by 4 digits, the I/O No. is designated by the higher 3 digits.	0000H to 00FEH	○	
(S1)	Control data storage head device Designates the local station head device that stores the control data.	Word device *2	○	○
(S2)	Write data storage head device (local station) Designates the local station head device that stores the write data.	Word device *2	○	
(D1)	Write head device (target station) Designates the target station head device that writes the data.	Word device *2		○
(D2)	Write complete device (local station) Designates the local station device that is turned on for 1 scan by write complete. (D2) .... OFF: Incomplete, ON: Complete (D2) + 1 .... OFF: Normal, ON: Error	Bit device *1 Word device bit specification *3		○
(D3)	Write report device (target station) Designates the target station device that is turned on for 1 scan by write. (D3) .... OFF: Incomplete, ON: Complete	Bit device *1 Word device bit specification *3		○

*1 : Bit device .... X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification .... Word device . Bit number

[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S1)	b15 to b1 b0 0 | 1/0 Execution type (bit 0) 0: Do not confirm arrival Ends execution of the WRITE instruction when transmission of the send request is complete. 1: Confirm arrival Ends execution of the WRITE instruction when writing of the data to the write destination station is complete.	0000H 0001H	○	
(S1) + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error code.)	0 or more		○
(S1) + 2	Local station channel Designates the local station QC24(N) interface that transmits the send request.	1: CH1 2: CH2	○	
(S1) + 3	(Not used)	—	—	—
(S1) + 4	Target station network No.	0	○	
(S1) + 5	Target station No.	0	○	
(S1) + 6	Special function module station No. Designates the target station QC24(N) station No. (0 to 31) when writing to [Target station-1].	0 to 31	○	
(S1) + 7	Number of retransmissions Write request: Designates the number of retransmissions when data is not written when (S1) is 0001H (execution type [1]). Write complete: Stores the number of retransmissions for normal end/abnormal end.	0 to 15	○	○
(S1) + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of execution of the WRITE instruction when (S1) is 0001H (execution type [1]). If data is not written within the monitoring time, the write request is retransmitted (S1) + 7 times. (Retransmission)	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
(S1) + 9	Write data length (units: words) Designates the number of data when writing the device data designated by (S2).	1 to 480	○	
(S1) + 10	(Not used)	—	—	—
to				
(S1) + 15				
(S1) + 16	Error detection network No.	—	—	—
(S1) + 17	Error detection station No.			

POINT

The number of resends ((S1) +7) must be set every time an instruction is executed.

[Caution]

① Execute the WRITE instruction by control data execution type Ⓢ1 set to "Confirm arrival" as much as possible.

② Provide a contiguous area of the number of bytes shown below at the word device used by the WRITE instruction.

- Ⓢ1 (control data storage device) .... 18 words
- Ⓢ2 (write data storage head device) .... Size designated by Ⓢ1 + 9 (write data length)
- Ⓓ1 (write head device)................................ Size designated by Ⓢ1 + 9 (write data length)

③ When the control data execution type was made "Do not confirm arrival" (Ⓢ1 bit 0 = OFF), the following data do not have to be designated.

- Ⓢ1 + 7....Number of retransmissions
- Ⓢ1 + 8....Arrival monitoring time

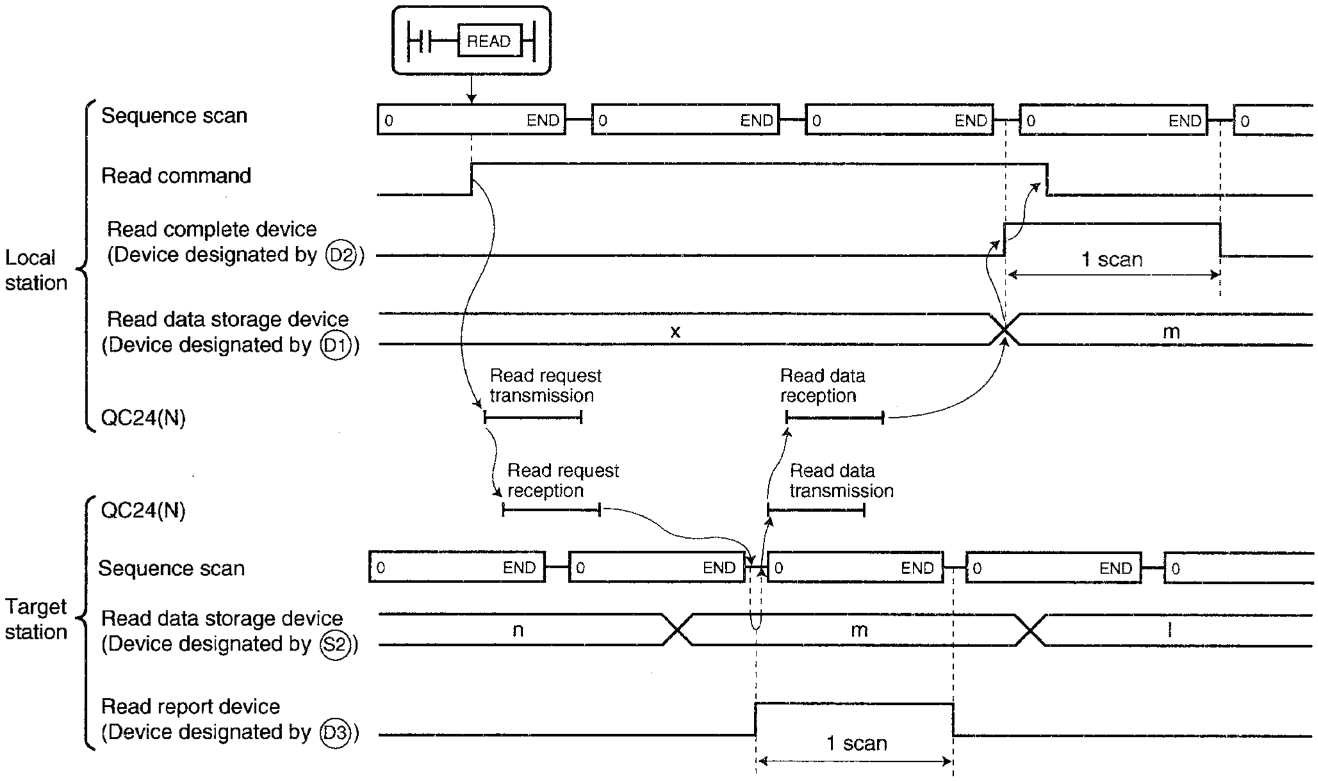
④ When performing device write to one station from multiple stations, do not use the same timing for each device writing.

When "no delivery confirmation" is set as the execution type, the execution completes normally on the writing station even if the contents of the transmission data are abnormal, if the communication is completed normally.

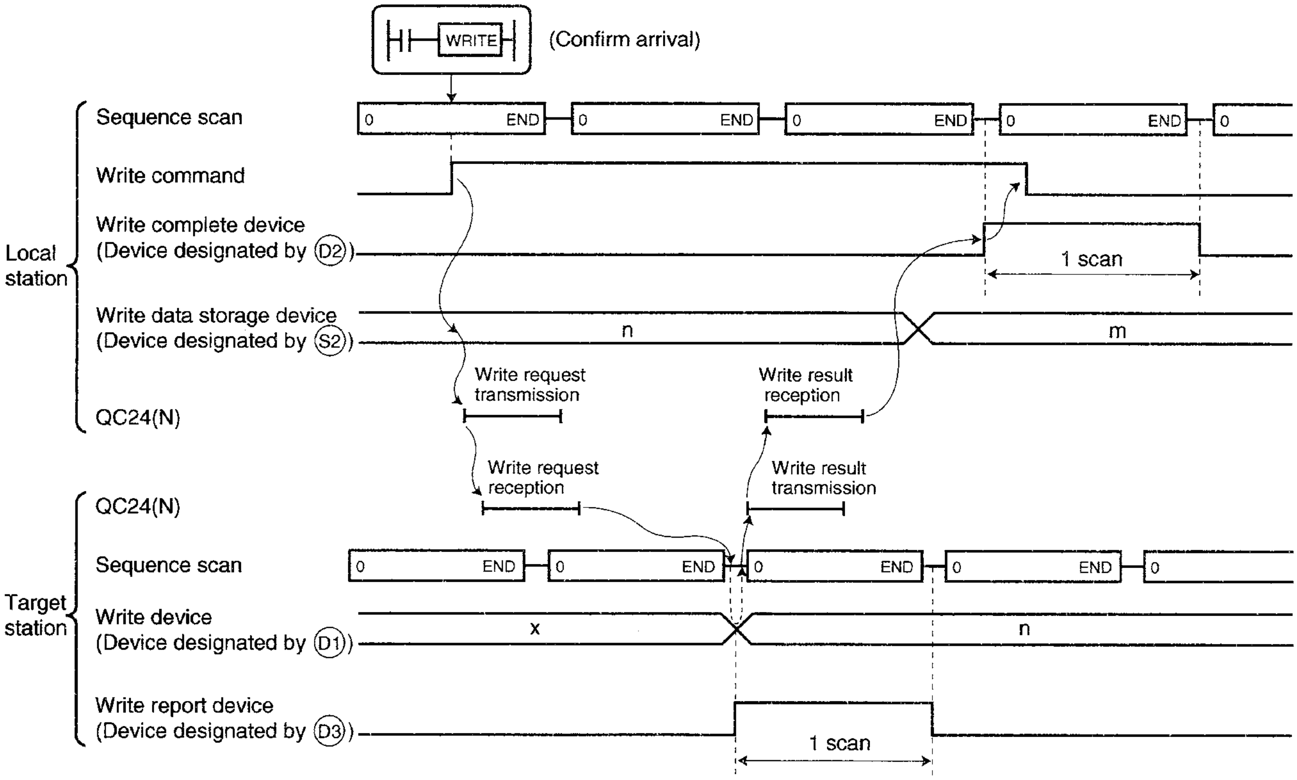
Also, even if the contents of the transmission data is normal, if multiple stations execute instructions to the same station, the writing station will result in a time-out error.

3 Instruction execution timing (When communicating between multidrop link stations)

(a) READ instruction



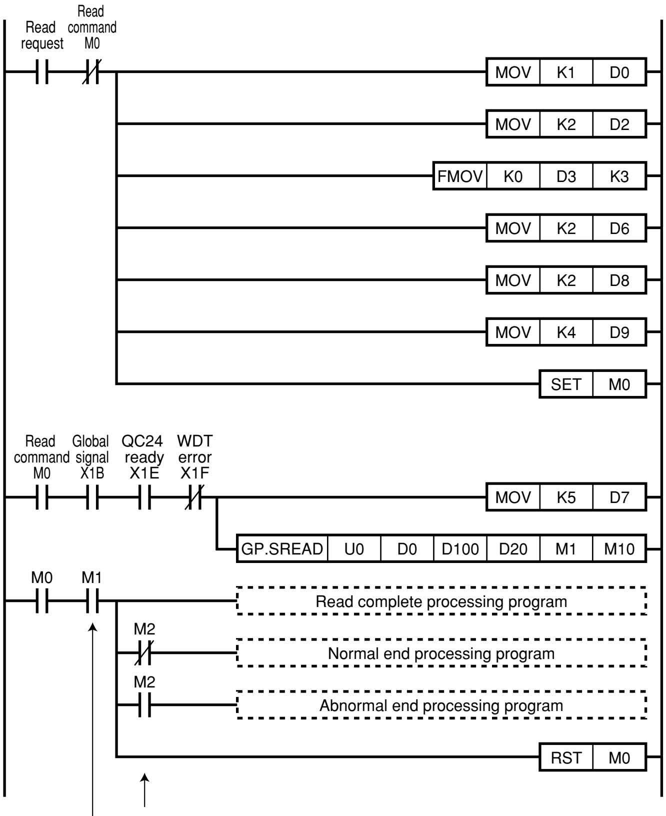
(b) WRITE instruction



4 Sample program

The following shows programs that transmit data from station ① to station ② over the [Target station-1] multidrop link system described in Section 20.2.

(a) Station ① READ instruction sample program



Sets the control data.

Sets (Ⓢ1) execution type.

Sets (Ⓢ1 + 2) local station channel (CH2).

Sets (Ⓢ1 + 3) to (Ⓢ1 + 5).

Sets (Ⓢ1 + 6) special function module station No. (target station QC24(N)).

Sets (Ⓢ1 + 8) arrival monitoring time (2 seconds).

Sets (Ⓢ1 + 9) read data length (4 words).

Sets the read command.

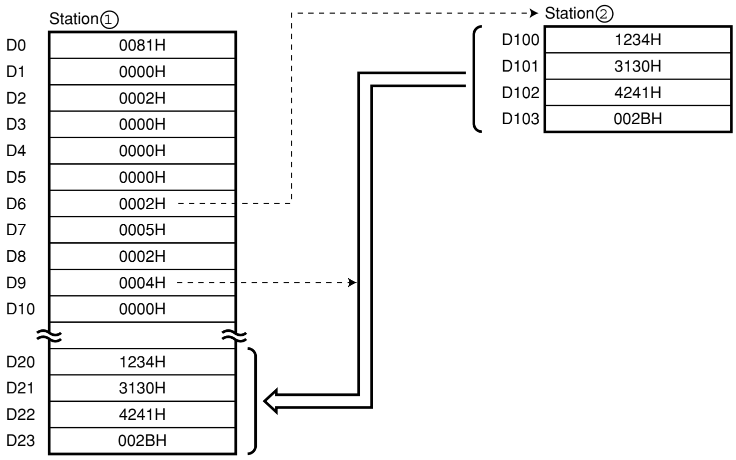
Sets (Ⓢ1 + 7) number of retransmissions (5 times).

READ instruction execution
X1B is the signal agreed upon with the external device to enable line use. (See Section 20.3.)

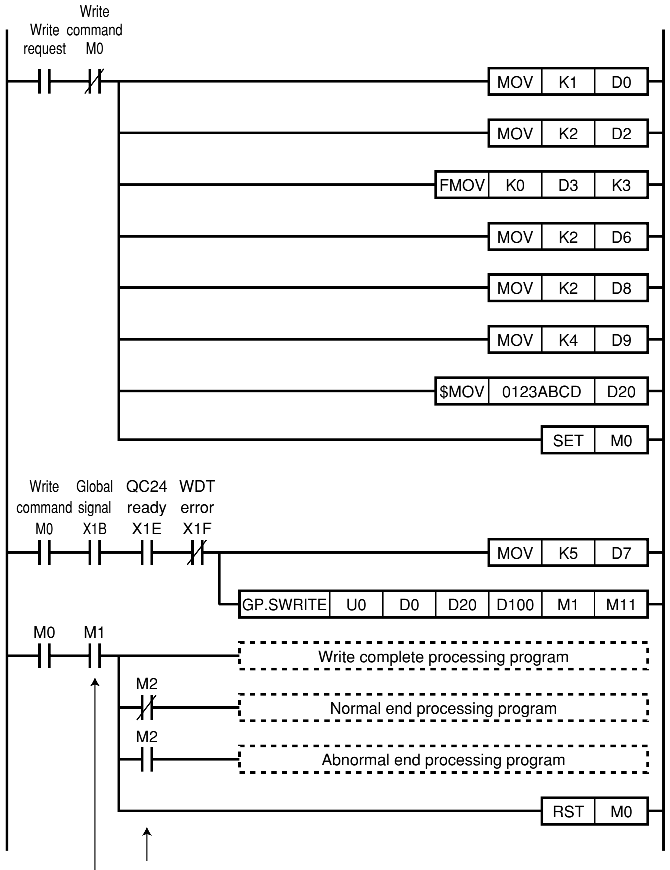
Performs processing according to the error code of D1 that stores the (Ⓢ1 + 1) end status. (See Section 22.1.3.)

M2 is turned ON/OFF according to READ instruction normal end/abnormal end.

Completion of execution of the READ instruction turns ON M1 for 1 scan.



(b) Station ① WRITE instruction sample program



Sets the control data.

Sets (S1) execution type.

Sets (S1 + 2) local station channel (CH2).

Sets (S1 + 3) to (S1 + 5).

Sets (S1 + 6) special function module station No. (target station QC24(N)).

Sets (S1 + 8) arrival monitoring time (2 seconds).

Sets (S1 + 9) write data length (4 words).

Sets the write data.

Sets the write command flag.

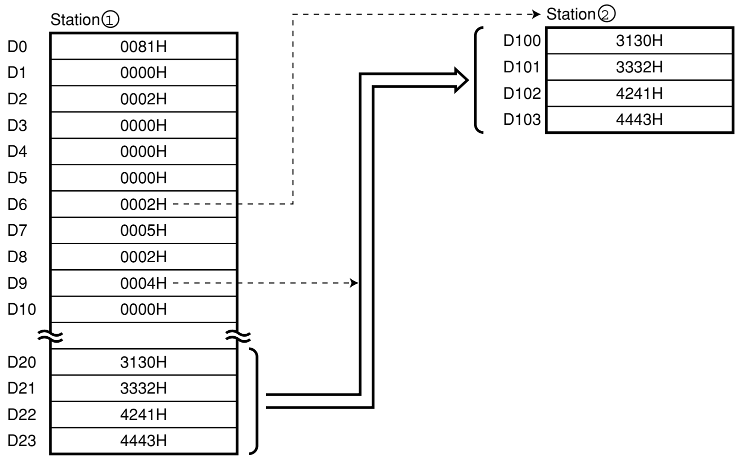
Sets (S1 + 7) number of retransmissions (5 times).

WRITE instruction execution
X1B is the agreed upon with the external device to enable line use. (See Section 20.3.)

Performs processing according to the error code of D1 that stores the (S1 + 1) end status. (See Section 22.1.3.)

M2 is turned ON/OFF according to WRITE instruction normal end/abnormal end.

Completion of execution of the WRITE instructions turns M1 ON for 1 scan.



20.4.3 QnACPU status control

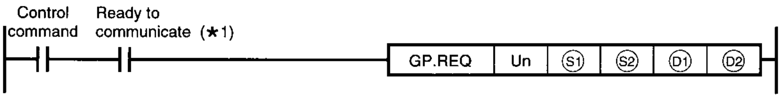
The following describes the REQ instruction when controlling the status (remote RUN/remote STOP) of the designated station's QnACPU.

1 REQ instruction

[Function]

Controls the status (remote RUN/remote STOP) of the designated station's QnACPU.

[Instruction format]



★1 Signal agree upon with the external device.

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/o No. (transmitting side) When the I/O signals are represented by 4 digits, this No. is designated by the 3 most significant digits.	0000H to 00FEH	○	
(S1)	Control data storage head device Designates the local station head device that stores the control data.	Word device *2	○	○
(S2)	Request data storage head device (local station) Designates the local station head device that stores the request contents.	Word device *2	○	
(D1)	Response data storage head device (local station)	Word device *2		○
(D2)	Execution complete device Designates the local station device that is turned ON for 1 scan when execution is complete. (D2) .... OFF: Incomplete, ON: Complete (D2) + 1 .... OFF: Normal, ON: Abnormal	Bit device *1 Word device bit specification *3		○

*1 : Bit device ....X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification ....Word device . Bit number

[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S1)	Execution type	0011H	○	
(S1) + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error codes.)	0 or more		○
(S1) + 2	Local station channel Designates the local station QC24(N) interface that transmits requests.	1: CH1 2: CH2	○	
(S1) + 3	Target station I/O signal	03FFH	○	
(S1) + 4	Target station network No.	0	○	
(S1) + 5	Target station No.	0	○	
(S1) + 6	Special function module station No. Designates the QC24(N) station No. (0 to 31) of the target station when a request is sent to [Target Station-1].	0 to 31	○	
(S1) + 7	Number of retransmissions Control request: Designates the number of times the request is to be retransmitted when control cannot be executed. Control complete: Stores the number of retransmissions for normal end/abnormal end.	0 to 15	○	○
(S1) + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of execution of the REQ instruction. If a response is not received within the monitoring time, the request is transmitted (S1)+ 7 times. (Retransmission)	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
(S1) + 9	Send data length (units: words) Designates the number of words of data designated by (S2).	4	○	
(S1) + 10	Response data length (units: word)	2		○
(S1) + 11	(Not used)	—	—	—
to				
(S1) + 15				
(S1) + 16	Error detection station No.	—	—	—
(S1) + 17	Error detection station No.			

POINT

The number of resends ((S1) +7) must be set every time an instruction is executed.

[Request data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S2)	Remote control	0010H	○	
(S2) + 1	Remote control request contents Designates the remote control request contents.	0001H: Remote RUN 0002H: Remote STOP	○	
(S2) + 2	Mode *1 For remote RUN, designates whether or not RUN is to be executed forcefully. For remote STOP, designates 0003H. [Forced execution is a function that forcibly performs "remote RUN" from another station when the station that performed the "remote STOP" cannot execute "remote RUN."]	0001H: Do not execute forcefully. 0003H: Execute forcefully	○	
(S2) + 3	Clear mode *2 Designates whether or not the QnACPU device memory is to be cleared (initialized) when remote RUN is executed. When remote STOP is executed, designates 0000H.	0000H: Do not clear 0001H: Clear (except latch range) 0002H: Clear (including latch range)	○	

*1 Mode ((S2) + 1) is data that forcefully executes remote RUN.
Forced execution is used when the QnACPU is forcefully RUN from another device, etc. when the QnACPU whose status was controlled could not be remotely RUN because of trouble in the station or external device that requests QnACPU remote STOP/PAUSE.

*2 Clear mode ((S2) + 3) is data that designates QnACPU device memory clear (initialization) processing at the start of operation of the QnACPU by remote RUN.
After the designated clear operation was performed, the QnACPU runs in accordance with the parameters settings (PLC file setting → device initial value).

[Response data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(D1)	Remote control	0090H		○
(D1) + 1	Remote control request contents	0001H: Remote RUN 0002H: Remote STOP		○

[Caution]

① When system protect (system protect switch SW5 = ON) is applied to the target QnACPU, status control cannot be executed. Each request is abnormally ended.

② The table below shows the state of the status control target QnACPU according to the setting of the RUN/STOP key switch.

		State of target station QnACPU front panel key switch	
		RUN	**STOP**
Local station request contents	Remote RUN	RUN	STOP
	Remote STOP	STOP	STOP

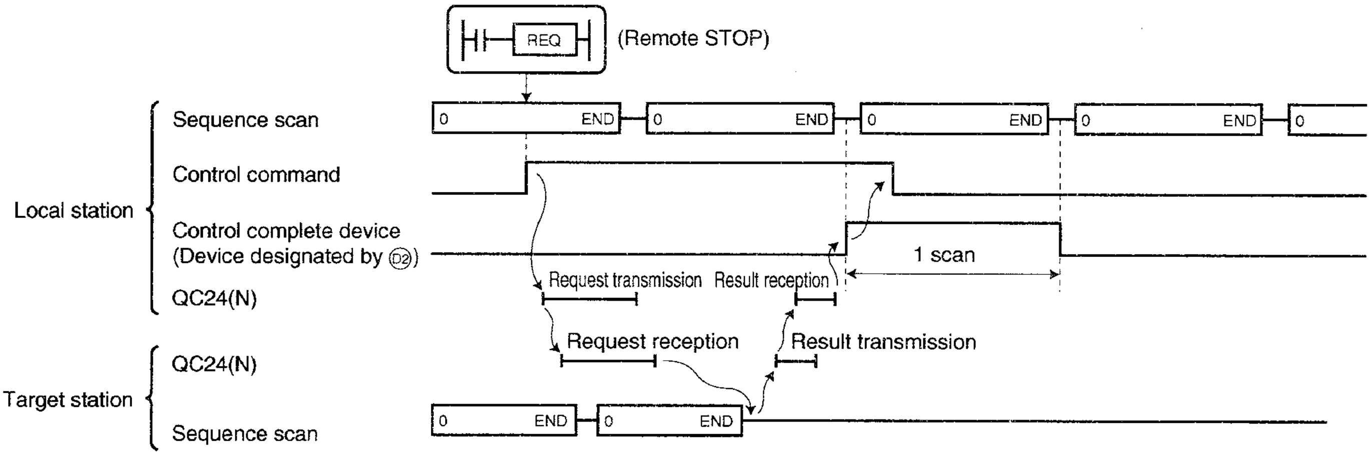
③ When the QnACPU power is turned OFF → ON, or the QnACPU is reset, after remote RUN/STOP is performed, the remote information is cleared.

④ If remote RUN is requested for a station that was placed into the remote STOP/PAUSE state from another station, etc., when "Do not perform forced execution" (mode (B + 2) = 0001H) is designated, the station will not enter the RUN state. The request is abnormally ended.

⑤ Provide a contiguous area of the following number of words at the word device used by the REQ instruction.

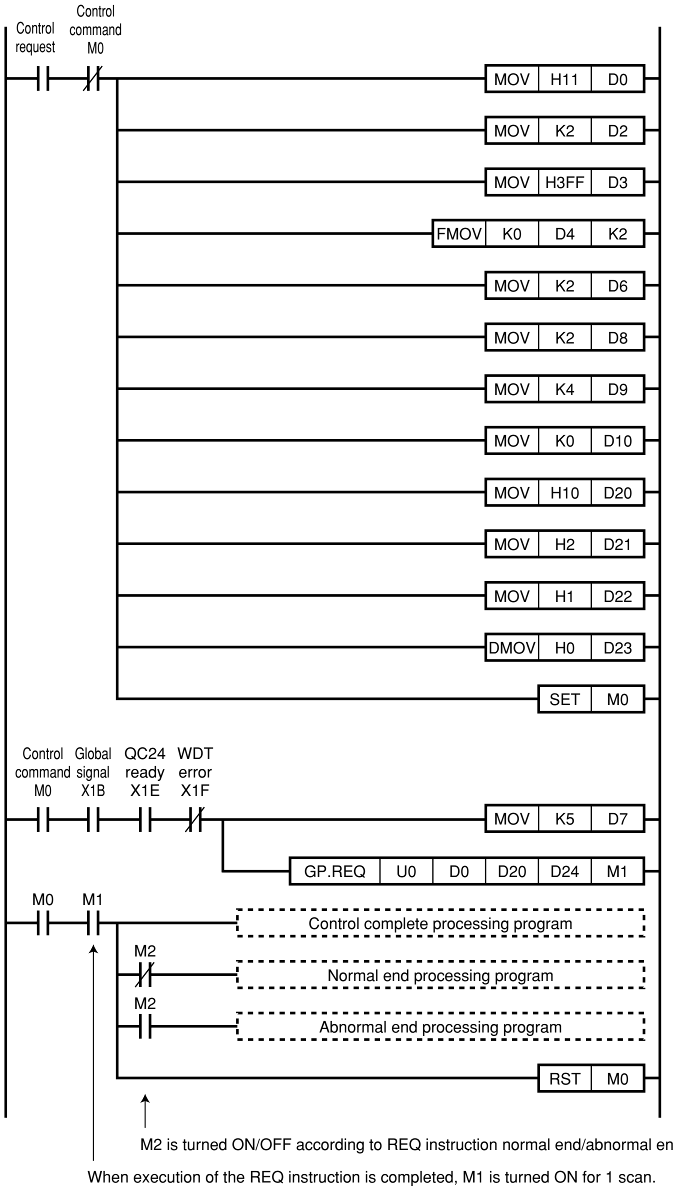
- S1 (control data storage device) .... 18 words
- S2 (request data storage head device)............ Size designated by (S1) + 9 (send data length).
- D1 (response data storage head device) .... 2 words

2 Instruction execution timing (When communicating between multidrop link stations)



3 Sample program

The following shows a sample program by executes remote STOP at station ② from station ① over the [Target Station-1] multidrop link described in Section 20.2.



M2 is turned ON/OFF according to REQ instruction normal end/abnormal end.

When execution of the REQ instruction is completed, M1 is turned ON for 1 scan.

Sets the control data.

Sets (Ⓢ1) execution type.

Sets (Ⓢ1 + 2) local station channel (CH2).

Sets (Ⓢ1 + 3) target station I/O signals.

Sets (Ⓢ1 + 4) to (Ⓢ1 + 5).

Sets (Ⓢ1 + 6) special function module station No. (target station QC24(N)).

Sets (Ⓢ1 + 8) arrival monitoring time (2 seconds).

Sets (Ⓢ1 + 9) read data length (4 words).

Sets (Ⓢ1 + 10).

Sets (Ⓢ2) remote control.

Sets (Ⓢ2 + 1) remote STOP.

Sets (Ⓢ2 + 2).

Sets (Ⓢ2 + 3) (Ⓓ1).

Sets the control command flag.

Sets (Ⓢ1 + 7) number of retransmissions (5 times).

REQ instruction execution
X1B is the signal agreed upon with the external device to enable line use. (See Section 20.3.)

Performs processing according to the error code of D1, which stores the (Ⓢ1 + 1) end status. (See Section 22.1.3.)

20.4.4 Reading and writing the QnACPU clock data

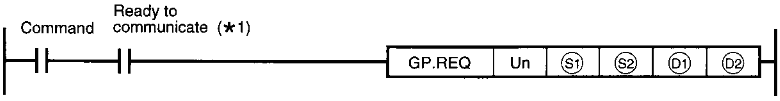
The following describes the REQ instruction when reading and writing the clock data of the designated station QnACPU.

1 REQ instruction

[Function]

Reads clock data from and writes clock data to the designated station QnACPU.

[Instruction format]



★1 Signal agree upon with external device

[Setting data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
Un	Local station QC24(N) head I/O No. When the I/O signals are represented by 4 digits, this No. is designated by the most significant 3 digits.	0000H to 00FEH	○	
(S1)	Control data storage head device Designates the local station head device that stores the control data.	Word device *2	○	○
(S2)	Request data storage head device (local station) Designates the local station head device that stores the request contents, etc.	Word device *2	○	
(D1)	Response data storage head device (local station) Designates the local station head device that stores the read clock data. When clock data is written, (D1) is designated with a dummy.	Word device *2		○
(D2)	Execution complete device Designates the local station device that is turned on when execution is complete. (D2) .... OFF: Incomplete, ON: Complete (D2) + 1 .... OFF: Normal, ON: Abnormal	Bit device *1 Word device bit specification *3		○

*1 : Bit device .... X, Y, M, L, F, V, B
*2 : Word device .... T, C, D, W, ST, R, ZR
*3 : Word device bit specification .... Word device . Bit number

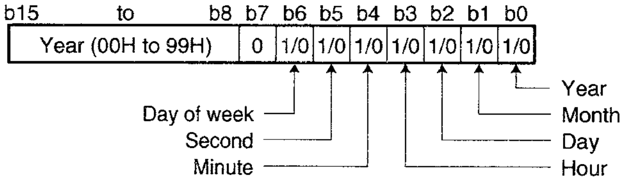
[Control data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
(S1)	Execution type	0011H	○	
(S1) + 1	End status 0: Normal end Nonzero: Abnormal end (See Section 22.1.3 for the error codes.)	0 or more		○
(S1) + 2	Local station channel Designates the local station QC24(N) interface that transmits requests.	1: CH1 2: CH2	○	
(S1) + 3	Target station I/O signal	03FFH	○	
(S1) + 4	Target station network No.	0	○	
(S1) + 5	Target station No.	0	○	
(S1) + 6	Special function module station No. Designates the QC24(N) station No. (0 to 31) of the target station when a request is sent to [Target Station-1].	0 to 31	○	
(S1) + 7	Number of retransmissions Read/write request: Designates the number of time the request is to be retransmitted when read/write cannot be performed. Read/write complete: Stores the number of retransmissions for normal end/abnormal end.	0 to 15	○	
(S1) + 8	Arrival monitoring time (units: seconds) Designates the monitoring time up to the end of execution of the REQ instruction. If a response is not received within the monitoring time, the request is transmitted (S1) + 7 times. (Retransmission)	0 : Default (10 seconds) 1 to 32767 : 1 to 32767 seconds	○	
(S1) + 9	Send data length (units: words) Designates the number of words of the data designated by (S2).	2: Read 6: Write	○	
(S1) + 10	Receive data length (units: words)	6: Read 2: Write		○
(S1) + 11 to (S1) + 15	(Not used)	—	—	—
(S1) + 16	Error detection network No.	—	—	—
(S1) + 17	Error detection station No.			

POINT

The number of resends ((S1) +7) must be set every time an instruction is executed.

[Request data]

	Contents	Setting range	Data detting	
		[Target station-1]	User	System
(S2)	System read/write	0001H: Read 0011H: Write	○	
(S2) + 1	Request contents Designates the system write/read request contents.	0002H: Clock read 0001H: Clock write	○	
(S2) + 2	Modification pattern, Modification year Clock data read : (S2)+2 to (S2)+5 designation is unnecessary. Clock data write : Designates the modification pattern and modification year as shown below. · Modification pattern (bit 0 to 7) Designates the item to be written in (S2)+2 higher bytes to (S2)+5. 0: Do not change (Do not write) 1: Change (Write) · Modification year (bit 8 to 15) Designates the year (last 2 digits) by BCD code  *Designates the month to day of week to modify by (S2)+3 to (S2)+5.	0000H to 997FH	○	
(S2) + 3	Modification month and day Higher 8 bits: Day (01H to 31H) Lower 8 bits: Month (01H to 12H)	0101H to 3112H	○	
(S2) + 4	Modification hour and minute Higher 8 bits: Minute (00H to 59H) Lower 8 bits: Hour (00H to 23H)	0000H to 5923H	○	
(S2) + 5	Modification second and day of week Higher 8 bits : Day of week (00H to 06H) Lower 8 bits: Second ↑ (00H to 59H) 00H (Sunday) to 06H (Saturday)	0000H to 0659H	○	

[Response data]

	Contents	Setting range	Data setting	
		[Target station-1]	User	System
D1	System read/write	0081H: Clock data read 0091H: Clock data write		○
D1 + 1	Request contents	0002H: Clock data read 0001H: Clock data write		○
D1 + 2	Read month and year (last 2 digits) Higher 8 bits: Month (01H to 12H), lower 8 bits: Year (00H to 99H)	0100H to 1299H		○
D1 + 3	Read hour and day Higher 8 bits: Hour (00H to 23H), lower 8 bits: Day (01H to 31H)	0001H to 2331H		○
D1 + 4	Read second and minute Higher 8 bits: Second (00H to 59H), lower 8 bits: Minute (00H to 59H)	0000H to 5959H		○
D1 + 5	Read day of week Day of week (0000H: Sunday to 0006H: Saturday)	0000H to 0006H		○

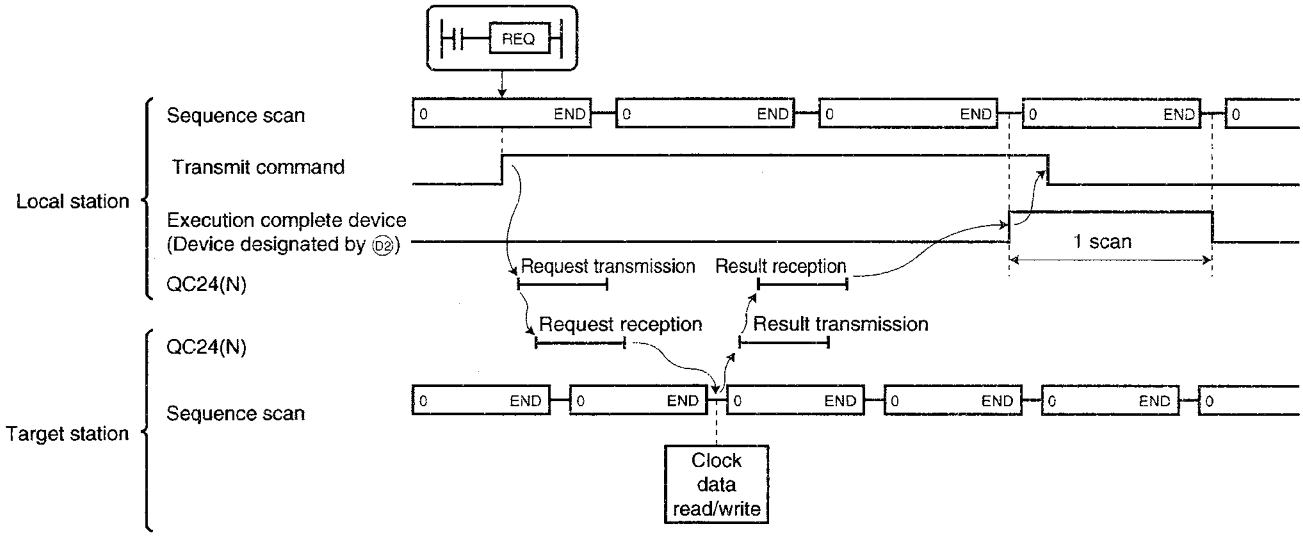
[Caution]

(1) When system protect (system protect switch SW5 = ON) is applied to the target QnACPU, the clock data is not written. All requests are abnormally ended.

(2) Provide a contiguous area of the following number of bytes at the word device used with the REQ instruction.

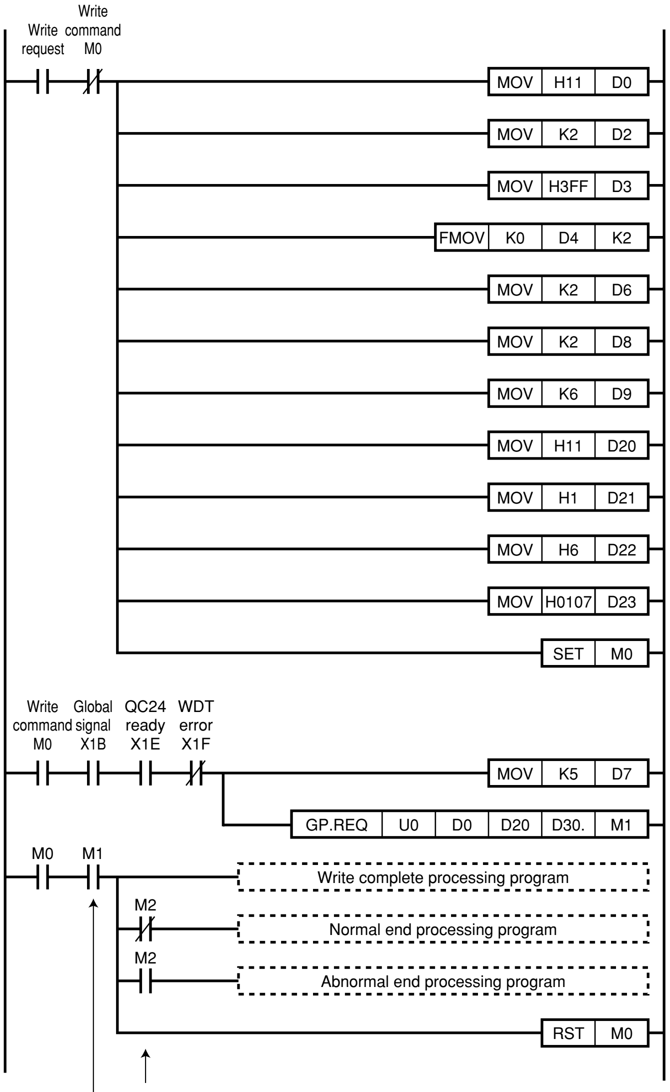
- S1 (control data storage device) .... 18 words
- S2 (request data storage head device) .... 6 words (write)
  2 words (read)
- D1 (response data storage head device). .... 2 word (write)
  6 words (read)

2 Instruction execution timing (When communicating between multidrop link stations)



3 Sample program

The following shows a sample program that changes the month and day of the clock data at station ② from station ① over the [Target Station-1] multidrop link system described in Section 20.2.



Sets the control data.

Sets (S1) execution type.

Sets (S1 + 2) local station channel (CH2).

Sets (S1 + 3) target station I/O signals.

Sets (S1 + 4) to (S1 + 5).

Sets (S1 + 6) special function module station No. (target station QC24(N)).

Sets (S1 + 8) arrival monitoring time (2 seconds).

Sets (S1 + 9) send data length (6 words).

Sets (S2) system write.

Sets (S2 + 1) clock write.

Sets (S2 + 2) modification pattern. (Month and day modification)

Sets (S2 + 3) July 1st.

Sets the write command flag.

Sets (S1 + 7) number of retransmissions (5 times).

REQ instruction execution
X1B is the signal agreed upon with the external device to enable line use. (See Section 20.3.)

Performs processing according to the error code of D1, which stores the (S1 + 1) end status. (See Section 22.1.3.)

M2 is turned ON/OFF according to REQ instruction normal end/abnormal end.

When execution of the REQ instruction is complete, M1 is turned ON for 1 scan.

Applicable module	AJ71QC24			A1SJ71QC24		AJ71QC24N			A1SJ71QC24N	
	–	-R2	-R4	–	-R2	–	-R2	-R4	–	-R2
Function availability	×	×	×	×	×	△	△	×	○	○
Remark	–					See section 1.4		–	–	

21. COMMUNICATIONS BY THE MODEM FUNCTION

This chapter explains the outline and how to use the modem function, which can be used for data communication with remote external devices and paging pager terminals.

21.1 Communications by the Modem Function

The overview, features, and functions of the modem function of the QC24N are herein described.

21.1.1 Overview

The overview of the modem function is described below:

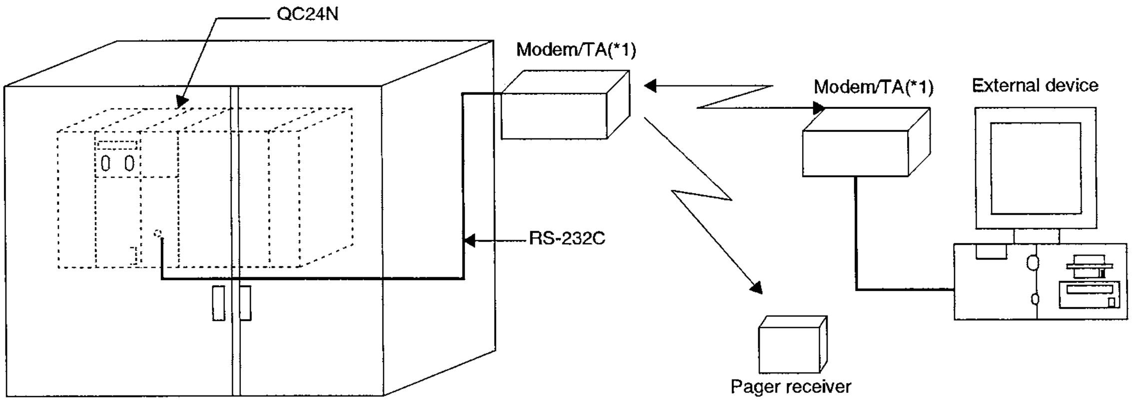
(1) The modem function easily performs data transmission/reception to remote devices via public lines/office telephone systems/digital lines (ISDN) by connecting a modem or TA (terminal adapter) to the QC24N's RS-232C interface.

① Communicating arbitrary data with an external device

② Call pager receiver to notify the PLC's system maintenance information.

(2) Initialization of the modem or TA, line connection (dialing), and line disconnection are performed using the PLC CPU.

(3) Once the line is connected, data communication with the external device via public line/office telephone system/digital line, or a call to pager receiver can be made.



*1 TA: terminal adapter

21.1.2 Features

The features of the modem function are described below:

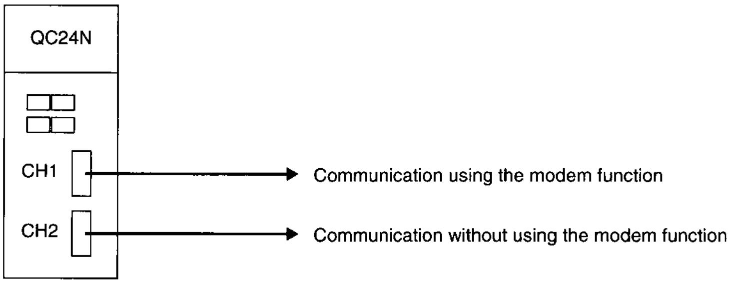
1 Types of QC24N that can use the modem function

① The modem function can be used with the QC24N using an RS-232C interface shown in Section 1.4.

* The AJ71QC24N-R4 cannot use the modem function because it does not have an RS-232C interface.

② For the AJ71QC24N-R2, A1SJ71QC24N-R2 and A1SJ71QC24N1-R2, the modem function can only be used by one of the two existing RS-232C interfaces.

With the interface of the QC24N, which does not use the modem function, direct data communication with an external device can be performed using a dedicated protocol, non procedure protocol or bidirectional protocol (independent operation).



2 Initialization, line connection and disconnection of the modem or TA

① The following set values for line connection can be stored to the QC24N EEPROM in multiple sets.

- Modem/TA initialization data (AT command)

  User setup: 30 sets (78 bytes/set); default value: 5 sets

- Connection data
  User setup: 30 sets (80 bytes/set)
  (Telephone number of the connection destination or display message to the pager receiver, etc.)

② By registering the above data to the QC24N ahead of time, the modem/TA (terminal adapter) initialization, line connection (dialing), and line cutoff can be performed with ease.

③ When the no-communication interval time (1 min. to 120 min.) is set, the QC24N disconnects the line when a no-communication condition has occurred for the set period of time following the line connection.

3 Communication between a remote external device and PLC CPU

① Data communication can be performed via full-duplex communication.

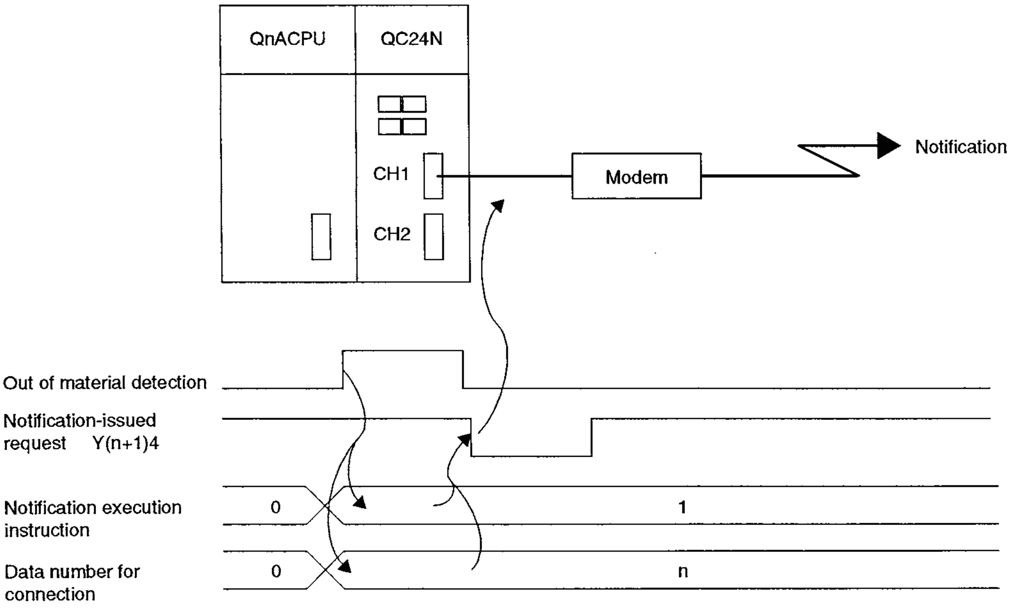
② From the external device to the PLC CPU, communication using the dedicated protocol, non procedure protocol and bidirectional protocol can be performed.

③ From the PLC CPU to the external device (transmission by the on-demand dedicated-protocol function only), communication by the non procedure protocol and bidirectional protocol can be performed.

4 Notification to the pager receiver

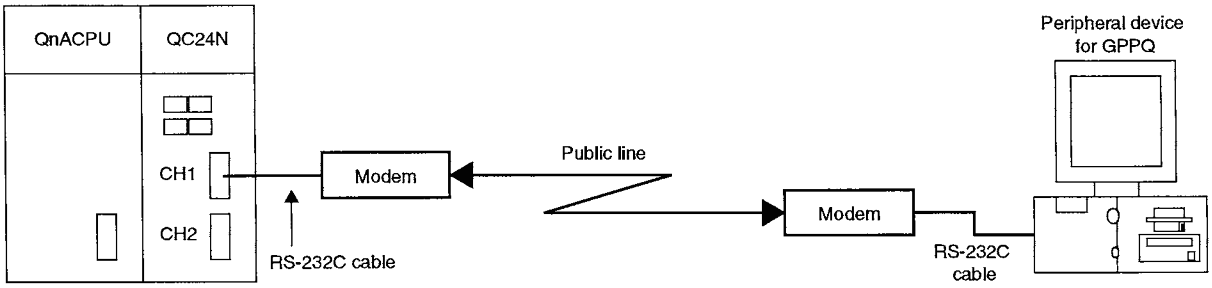
① In order to notify to the pager receiver of the PLC system maintenance information, the QC24N performs calling and message transmission according to the user-designated connection data when the output signal from PLC CPU is turned from ON to OFF.

② Because notification processing is performed while the output signals from PLC CPU are turned OFF from ON, dedicated notification can be performed when the PLC CPU enters the STOP state due to an error, etc.



5 Communication from the peripheral device for GPPQ

The peripheral devices for GPPQ can read and write the device data and sequence program from/to the remote PLC CPU. (It is possible to communicate with only CH1 side of QC24N)



* The peripheral device for GPPQ regards the QnACPU station with QC24N installed as a QnACPU station with a Q6TEL installed (or connected).

21.1.3 Function list

The overview of the modem function is shown below:

<table>
<tr><th>Function</th><th colspan="2">Overview</th></tr>
<tr><td>Modem/TA initialization</td><td colspan="2">Initializes the modem/TA using the user-designated initialization data (AT command).</td></tr>
<tr><td>Line connection (dialing)</td><td colspan="2">Dials the partner telephone number according to the user-designated connection data and enables data communication after establishing the line connection. When the modem/TA is not initialized, performs initialization.</td></tr>
<tr><td rowspan="3">Data communication</td><td>Performs communication with an external device using the dedicated protocol, non procedure protocol or bidirectional protocol.</td><td rowspan="4">Communication method: full duplex communication
Synchronization method: start-stop synchronous system (asynchronous)</td></tr>
<tr><td>Performs communication with the partner QC24N-installed station by modem/TA connection using non procedure protocol or bidirectional protocol. (Station-to-station communication.)</td></tr>
<tr><td>Enables the communication between peripheral devices for GPPQ and PLC via QC24N.</td></tr>
<tr><td>Notification</td><td>Calls and transmits messages to the pager receiver.</td></tr>
<tr><td>Line disconnection</td><td colspan="2">Forcefully disconnects the line from the connected destination device.</td></tr>
<tr><td>EEPROM reading, writing (registration) and deletion</td><td colspan="2">Reads, writes (registers) and deletes the initialization data (AT command) and data for connection from/to the EEPROM in the QC24N according to the request from PLC CPU.</td></tr>
</table>

21.1.4 Comparisons with related devices

Shown below is a comparison with the related products which support data communication with the PLC using the modem and public line, etc., similarly to the communication performed via the QC24N modem function.

Communication function name		QC24N (modem function)	Q6TEL	A6TEL	A1SJ71CMO
Modem/TA initialization		○	○		(Processing for built-in modem)
Line connection (dialing)		○	(Performed on the partner side)		○
Communication between same products (such as QC24N-QC24N)	Dedicated protocol	×	×		○
	Non procedure protocol	○	×		○
	Bidirectional protocol	○	×		○
Communication between QC24N and other products		–	–	–	○
Remote communication from peripheral device for GPPQ		○	○	×	×
Remote communication from peripheral device for GPPA		×	○	○	×
Notification	Pager receiver	○	○	○	×
Password check from the GPPQ function		○ (*1)	○	○	×
Line disconnection		○	(Performed on the partner side)		○
Data for initialization registration		○ (EEPROM)	○	○	(Unnecessary)
Data for connection registration		○ (EEPROM)	○	○	× (*2)
Number of connectable modems/TAs		1			(Built-in)
Transmission type		Pulse/tone			
Connectable lines	Analog 2-line method	○	○	○	○
	Analog 4-line method	○	×	×	○
	Digital line (ISDN)	○	○	×	×

○ : enable
× : disable

*1 The QC24N transmits a response without checking the password received from the peripheral device for GPPQ.

*2 When data communications are started, the data for connection is designated in the buffer memory.

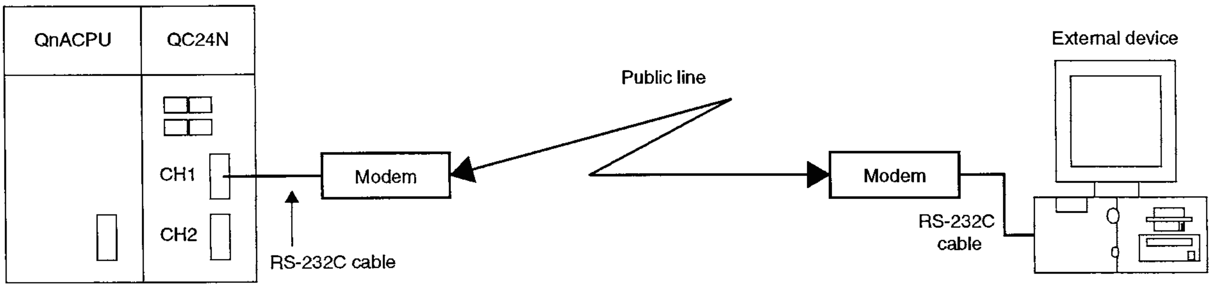
21.2 System Configuration

This section covers system configurations when the QC24N modem function is used to call a pager receiver or to perform data communication with an external device via public lines.

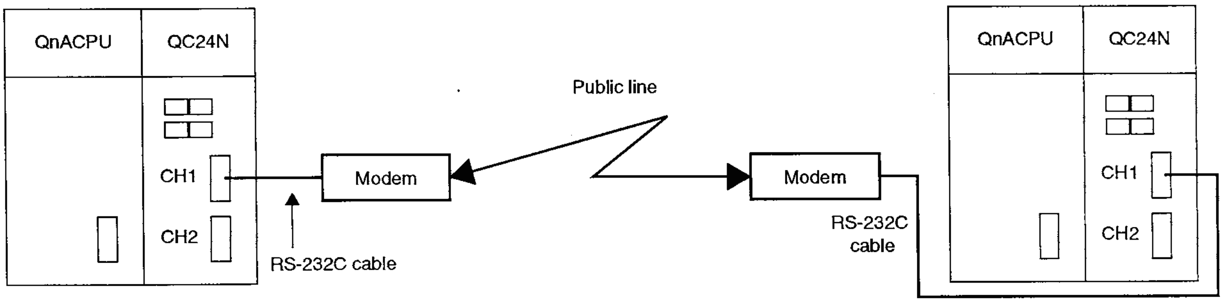
21.2.1 System configuration when performing data communication with an external device

The system configuration examples shown below are used when performing data communication between the external device and PLC using the QC24N's dedicated protocol/non procedure protocol/ bidirectional protocol.

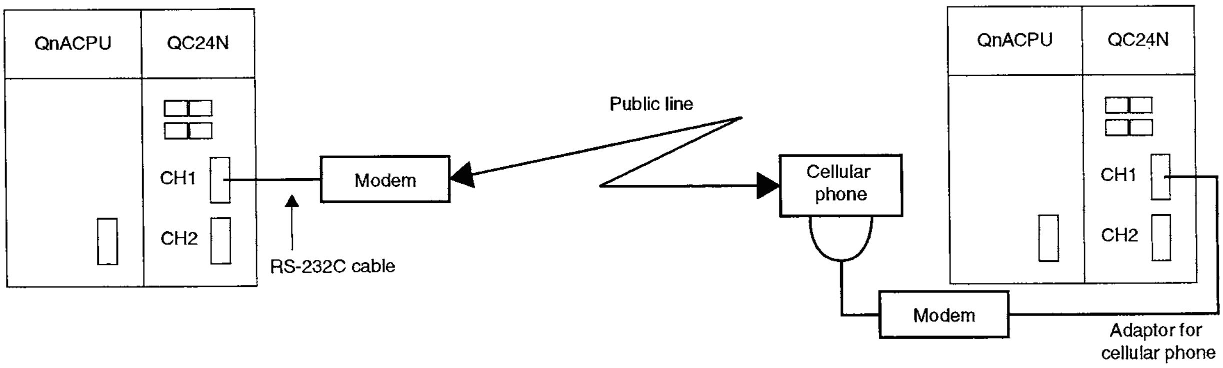
1 Connection example with an external device



2 Connection example with a QC24N



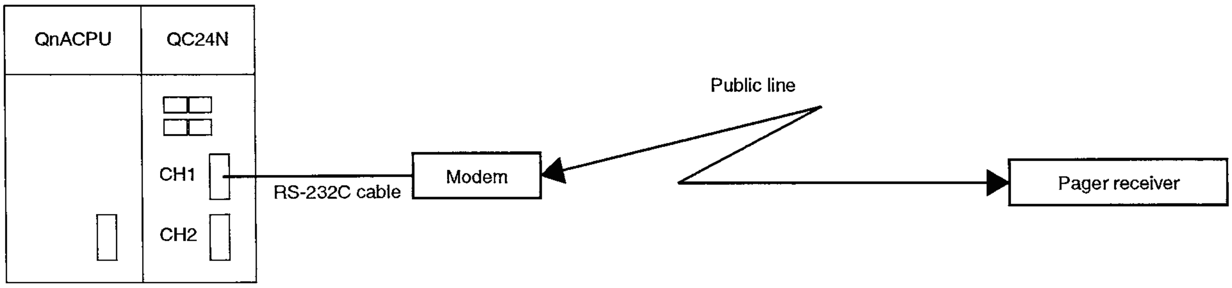
3 Connection example with a QC24N via cellular phone



- * The public lines indicated in 1 to 3 above are compatible with the office telephone system as well.
- * In the system configurations shown in 1 and 2 above, the digital line (ISDN) can replace the public line.
  When connecting via a digital line, a TA (terminal adapter) and a DSU (digital service module) are used instead of a modem.

21.2.2 System configuration when using the notification function

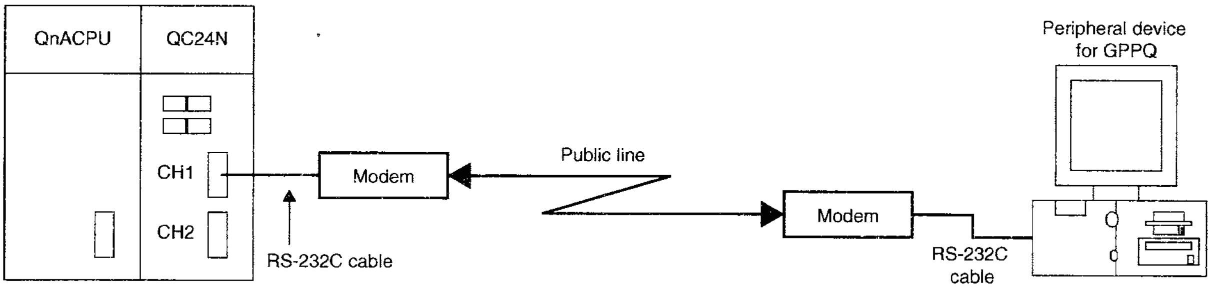
The system configuration example when calling the pager receiver by the QC24N notification function is shown below.



* The public line indicated above is compatible with the office telephone system as well.

21.2.3 System configuration when connecting the peripheral device for GPPQ

The system configuration examples shown below when the peripheral device for GPPQ performs data communication with a remote station PLC via QC24N.



* Select "Via modem interface module for QnA" in the GPPQ PLC-side interface setup.
* The public lines indicated above is compatible with the office telephone system as well.
* In the system configuration shown above, the digital line (ISDN) can replace the public line. When connecting via a digital line, a TA (terminal adapter) and a DSU (digital service module) are used instead of a modem.
* It is possible to communicate with only CH1 side of QC24N when communicating with the peripheral device for GPPQ.

21.2.4 Precautions for system configurations

The precautionary items when configuring the system to perform data communication with an external device or call a pager receiver via public line, an office telephone system or digital line (ISDN) using the QC24N modem function are explained.

1 QC24N insertable station

① The QC24N that uses the modem function can only be installed to the QnACPU stations.

② The QC24N cannot be installed to MELSECNET (II) remote station.

Also, the QC24N which uses the modem function cannot be installed to MELSECNET/10 remote station.

2 Usable QC24N interface

① The modem function can be used with the RS-232C interface only.

The modem function cannot be used with the AJ71QC24N-R4, since it does not have the RS-232C interface.

② For AJ71QC24N-R2, A1SJ71QC24N-R2 and A1SJ71QC24N1-R2, the modem function can only be used with one of the two existing RS-232C interfaces.

With the interface of the QC24N, which does not use the modem function, direct data communication with an external device can be performed using a dedicated protocol, non procedure protocol or bidirectional protocol (independent operation).

③ The peripheral device for GPPQ can only be connected to the CH1-side interface of the QC24N.

④ It is not possible to communicate using the two QC24N interfaces in linked operation (data communication via two interfaces).

3 Connectable modem/TA

Only the modems indicated in Section 21.3.2 can be used for the QC24N RS-232C interface using the modem function.

4 Number of connectable modems/TA's

Only one modem/TA can be connected to the QC24N RS-232C interface that uses the modem function.

5 Modem/TA connection cables

① The RS-232C cable supplied with the modem/TA or the designated modem/TA cable can be used for connection between the QC24N and modem/TA.

② The QC24N RS-232C interface connector has a 25-pin (female) D-sub. Depending on the RS-232C cable connector, the 9-25 pin converter (user supplied) may be necessary.

6 Modem/TA installation

① Install the modem/TA according to the modem/TA manual.

When installed in an area in which a lot of noises exists, malfunctions may occur.

② In order to prevent the effects of noise and power surges, do not connect near or tie the cable together with a main circuit line, high-voltage line or load line other than for the PLC with the modem/TA connection cable.

7 Connectable lines

① The connections can be made with the following lines. Perform connection tests beforehand and confirm that connection is possible.

- Public line or office telephone system of analog two-line/four-line method
- Digital line (ISDN)

② It is not possible to connect to call-waiting lines, in order to avoid data errors or automatic line disconnection due to the call-waiting interrupt tone.

③ Avoid connections with party-line telephones to avoid interrupted calls during communication.

④ If an alert sound is sent at fixed intervals from the communication machine to prevent long-term calls, data may experience errors.

It is recommended to check the normality/abnormality of data reception between devices, and perform transmission-retry processing when an abnormality is detected.

⑤ See the modem/TA manual regarding the connection from a modem to public line/office telephone system, or from a TA (terminal adapter) to a digital line.

8 Communication system

Communication via the modem function is performed using full-duplex communication.

Connections cannot be made devices designed for half-duplex communication.

9 Data communication and notification to external devices

① Data communication with external devices and notification to a pager receiver are performed using the public line or electric wave transmitted from the electric wave transmission base.

There might occur a condition in which correct data communication or notification cannot be carried out due to an error from the system's setup environment, electric-wave transmission status, error in the partner device, etc.

Perform a connection test beforehand, and confirm that connection is possible.

② In notification processing via electric-wave transmission, errors from the pager receiver cannot be detected.

Setup a separate call circuit with a lamp display or buzzer to ensure the safety of the PLC system.

21.3 Specification

The transmission specification on the QC24N side, connectable modems/TA's (terminal adapter), I/O signals related to the modem function, and buffer memory for the usage of the QC24N modem function are described.

21.3.1 Transmission specification

The transmission specification on the QC24N side when communicate by the modem function is as shown below.

The transmission specification between QC24N and a modem/TA of local station QC24N end not described in this chart is follows the specification indicated in Chapter 3.

Item		AJ71QC24N A1SJ71QC24N A1SJ71QC24N1	AJ71QC24N-R2 A1SJ71QC24N-R2 A1SJ71QC24N1-R2	AJ71QC24N-R4
Modem function usage availability		Yes		Unusable
Interface for the modem function		RS-232C	RS-232C (*1)	—
Linked operation between CH1 and CH2 of the QC24N		No		
Communication system		Full duplex communication		
Synchronization method		Start-stop synchronous system		
Transmission speed (Unit: bps)		38400, 19200, 9600, 4800, 2400, 1200, 115200, 57600, 28800, 4400 (selectable)		
Data format	Start bit	1		
	Data bit	7 / 8		
	Parity bit	1 (On) / 0 (Off)		
	Stop bit	1 / 2		
Error detection	Parity check	On (odd/even selectable) / Off		
	Sum check code	On / Off		
Transmission control		RS·CS control / not-control (selectable)		
Data communication availability	No procedure protocol	Communication enabled		
	Bidirectional protocol	Communication enabled		
	Dedicated protocol	Communication enabled		
	Link-dedicated instruction communication	Communication disabled		
Line connection (QC24N: modem)		1 : 1		

*1 Communicates by the modem function is possible only using one of the two RS-232C interfaces.

Communicates with a peripheral device for GPPQ can only be performed on the CH1 side.

21.3.2 Specification of connectable modems/terminal adapters

The specification of modems/TA's that can be connected to the QC24N side when using the QC24N's modem function is shown below.

1 Specification and precautions for the connectable modems

(a) Modem specification

Item			Specification		Remarks
			When using the subscriber's telephone line/ office telephone system	When using a manual line connection	
Modem-to-modem communication specification	Connection line		Analog 2-line/4-line		—
	Initialization		Hayes AT command compatible		
	Telephone line		A line compatible with NTT communication protocol		See Section 21.2.4 regarding the restrictions
	Communication standard	ITU-T	V. 34/V.32bis/V.32/V. 22bis/V. 22/V. 21/V. fc		—
		Bell	212A/103		
	Error correction (*1)	MNP	Class 4 and 10 compliant		
		ITU-T	V.42 compliant		
	Data compression (*1)	MNP	Class 5 compliant		
		ITU-T	V.42bis compliant		
	ANS-ORG mode switch		—	Mode switching required	
QC24N-to modem communication specification	QC24N-side connector (RS-232C)		25-pin (female) D sub		See Section 3.2
	DR signal control		Only the DR (DSR) signal must be able to turn on		(*2)
	Other		Compatible with the QC24N specification		See Chapter 3, Section 21.3.1

*1 The following are the functions of the modem itself that become available by issuing the AT commands to the modem. See the modem manual for details.

(1) Error correction

① When a noise occurs on the line, scrambled data may appear due to interrupted communication data.
The error correction function is intended to suppress effects from such noises.

② If an error such as scrambled data is detected by the error correction, the modem retries the transmission.
When the number of retries has exceeded the modem's limit, the modem determines that communication cannot be performed in that environment and disconnects the line.

③ Both modems must support the MNP4 or V.42 protocol.

(2) Data compression

① This function compresses data to be sent prior to transmission, and inflates the compressed data upon reception, then forwards to the terminal.

② The data compression is effective for the execution speed at a maximum of 200% for the MNP5 and 300% for the V.42bis.

③ Both modems must support the MNP5 or V.42bis protocol.

(3) Flow control (RS·CS control)
When communication between a modem and terminal is faster than between two modems, the flow control is performed in the following order:

① The modem transmits data to the partner by storing the data from the terminal in the modem buffer.

② When the buffer in the modem becomes almost full, the modem outputs a data-transmission temporary stop request (CS signal = OFF) to the terminal.
The terminal then stops data transmission to the modem when the data-transmission temporary stop request (CS signal = OFF) is received.

* Even while the terminal pauses data transmission, the modem continues to send data to the partner.

③ When a free space is present in the modem buffer, the modem outputs the data-transmission resume request (CS signal = ON) to the terminal.
The terminal then resumes data transmission to the modem when the data-transmission resume request (CS signal = ON) is received.

*2 Modems that turn on the CD signal simultaneously cannot be used.

(b) Precautions for selecting a modem

① When using a cellular phone

A modem with the error correction function of MNP class-10 is recommended. However, note that communication may not be established depending on the line condition.

② Modem setting

- Set the modem on the QC24N side as shown below:

Setting item		Setting range
Communication speed		Depends on the modem in use (*1)
Modem command		Hayes AT command
SI/SO control		None
Communication method		No procedure
Data format	Data bit	Match the QC24N
	Stop bit	
	Parity bit	

*1 When using different modems, the slower communication speed will be in effect.

- When using a modem whose DR terminal (signal) is set by a switch, set the DR-terminal (modem output) switch level to high.

  When using a modem whose DR terminal is set by a software, write the AT command that turns on the DR terminal into the EEPROM etc., of the QC24N-side modem from a personal computer.

* In order to write the AT command that turns on the DR terminal from a personal computer, a terminal software (supplied with the modem) must be installed to the personal computer.

An overview of the procedure from installation to writing AT commands and connecting to the QC24N is described below.

(Procedure 1) Install a terminal software to the personal computer.

(Procedure 2) Connect the modem to be connected to the QC24N side and personal computer using the RS-232C cable.

(Procedure 3) Startup the personal computer, and start the terminal software.

(Procedure 4) Write the AT command that turns on the DR terminal.

(Example 1) AT&SO&W Enter

(Example 2) ATZ Enter
AT&F&W Enter

The AT command that turns on the DR terminal may differ depending on the modem. See the manual of the terminal software manual for details.

(Procedure 5) After turning on the DR terminal, connect the modem and QC24N.

2 Specification and precautions for the connectable TA's (terminal adapters)

(a) TA specification

Item		Specification	Remarks
TA-to-TA communication specification	Connection line	ISDN (INS net 64) equivalent High-speed digital dedicated line	DSU and TA are required
	Initialization	Hayes AT command compatible	—
	Communication standard	B-channel line exchange (V.110) D-channel packet exchange	
QC24N-to-TA communication specification	Electrical condition	V.28 compliant	
	Circuit definition	V.24 compliant	
	QC24N-side connector (RS-232C)	25-pin (female) D sub	See Section 3.2
	DR signal control	Only the DR (DSR) signal must be able to turn on	(*1)
	Other	Compatible with the QC24N specification	See Chapter 3, Section 21.3.1

*1 TA's that turn on the CD signal simultaneously cannot be used.

Use a TA capable of flow control as described in 1 (a) in this section also for the communication between the TA and terminal.

Flow control is a function of the TA itself that becomes available by issuing the AT commands to the modem. See the TA manual for details.

(b) Precautions for selecting a TA

① Set the TA on the QC24N side as shown below:

Setting item		Setting range
Communication speed		Depends on the TA in use
TA command		Hayes AT command
SI/SO control		None
Communication method		No procedure
Data format	Data bit	Match the QC24N
	Stop bit	
	Parity bit	

② When using a TA whose DR terminal (signal) is set by a switch, set the DR-terminal (TA output) switch level to high.
When using a TA whose DR terminal is set by a software, write the AT command that turns on the DR terminal into the EEPROM etc., of the QC24-side TA from a computer.

* In order to write the AT command that turns on the DR terminal from a personal computer, a terminal software (supplied with the TA) must be installed to the personal computer.

An overview of the procedure from installation to writing AT commands and connecting to the QC24N is described below.

(Procedure 1) Install a terminal software to the personal computer.

(Procedure 2) Connect the TA to be connected to the QC24N and personal computer using the RS-232C cable.

(Procedure 3) Startup the personal computer, and start the terminal software.

(Procedure 4) Write the AT command that turns on the DR terminal.

(Example) AT&SO&W Enter

The AT command that turns on the DR terminal may differ depending on the TA. See the manual of the terminal software manual for details.

(Procedure 5) After turning on the DR terminal, connect the TA and QC24N.

21.3.3 I/O signals with the PLC CPU

The I/O signals with the PLC CPU added for the QC24N's modem function are described. See Section 3.4 for the I/O signals not related to the modem function.

1 I/O signal list

Signal direction: QC24N → PLC CPU			Signal direction: PLC CPU → QC24N		
Device number	Signal name		Device number	Signal name	
Xn0	CH1 side	Transmission normal completion	Yn0	CH1 side	Transmission request
Xn1		Transmission abnormal completion	Yn1		Reception data read completion
Xn2		Transmission processing in progress	Yn2		Mode switching request
Xn3		Reception data read request	Yn3	(Prohibited to use)	
Xn4		Reception abnormal detection	Yn4		
Xn5	————————		Yn5		
Xn6	CH1 side	Mode switching in progress	Yn6		
Xn7	CH2 side	Transmission normal completion	Yn7	CH2 side	Transmission request
Xn8		Transmission abnormal completion	Yn8		Reception data read completion
Xn9		Transmission processing in progress	Yn9		Mode switching request
XnA		Reception data read request	YnA	(Prohibited to use)	
XnB		Abnormal reception detection	YnB		
XnC	————————		YnC		
XnD	CH2 side	Mode switching in progress	YnD		
XnE	CH1 ERR LED on		YnE	CH1 ERR LED off request	
XnF	CH2 ERR LED on		YnF	CH2 ERR LED off request	
X (n+1) 0	Initialization completion		Y (n+1) 0	Initialization request (standby request)	
X (n+1) 1	Dial in progress		Y (n+1) 1	Connection request	
X (n+1) 2	Connection in progress		Y (n+1) 2	Modem disconnection request	
X (n+1) 3	Initialization/connection abnormal completion		Y (n+1) 3	(Prohibited to use)	
X (n+1) 4	Modem disconnection completion		Y (n+1) 4	Notification-issued request	
X (n+1) 5	Notification normal completion		Y (n+1) 5	(Prohibited to use)	
X (n+1) 6	Notification abnormal completion		Y (n+1) 6		
X (n+1) 7	EEPROM read completion		Y (n+1) 7	EEPROM read request	
X (n+1) 8	EEPROM write completion		Y (n+1) 8	EEPROM write request	
X (n+1) 9	EEPROM system setting write completion		Y (n+1) 9	EEPROM system setting write request	
X (n+1) A	CH1 side	Global signal	Y (n+1) A	(Prohibited to use)	
X (n+1) B	CH2 side	Global signal	Y (n+1) B		
X (n+1) C	System setting default completion		Y (n+1) C	System setting default request	
X (n+1) D	————————		Y (n+1) D	(Prohibited to use)	
X (n+1) E	QC24N ready (accessible)		Y (n+1) E		
X (n+1) F	Watchdog timer error		Y (n+1) F		

The signals in the ▨ are the new I/O signals added to the modem function.

IMPORTANT

Do not output (turn ON) the "prohibited to use" signal as the output signal to a special function module from the PLC CPU.
Outputting a signal for "prohibited to use" may cause system malfunctions in the PLC.

2 Function and description of each I/O signal

I/O signal	Signal name	Function/description	Description section
X (n+1) 0	Initialization completion	Indicates normal completion of the QC24N's initialization of the modem/TA connected to itself according to the initialization data designated in the buffer memory.	Section 21.4.7
X (n+1) 1	Dial in progress	Indicates that the QC24N is dialing (connection processing) the partner side according to the data for connection designated in the buffer memory.	Section 21.4.8
X (n+1) 2	Connection in progress	1) Indicates normal completion of the line-connection processing from or to the partner side. 2) When this signal is on, data communication with the destination is possible (notification is not possible).	
X (n+1) 3	Initialization/ connection abnormal completion	1) Indicates abnormal completion of the modem/TA initialization or line connection processing (dialing) to the destination. 2) Check the cause of the abnormal completion in the modem-error code storage area (address: 221H) and remove the cause.	Section 22.1.4
X (n+1) 4	Modem disconnection completion	Indicates that the line for data communication with the destination has been disconnected.	Section 21.4.10
X (n+1) 5	Notification normal completion	Indicates the normal completion when performing the notification processing to the destination.	Section 21.4.9
X (n+1) 6	Notification abnormal completion	1) Indicates abnormal completion when the notification processing is performed with the destination. 2) Check the cause of the abnormal completion in the modem error code storage area (address: 221H) and remove the cause.	Section 22.1.4
Y (n+1) 0	Initialization request (standby request)	1) Indicates the initialization request to the modem connected to the local station QC24N. 2) Turn on the initialization-request signal after designating the initialization data to the buffer memory.	Section 21.4.7
Y (n+1) 1	Connection request	1) Indicates the connection request (dialing) to enable data communication with the destination. 2) Turn on the connection request signal after designating the data for connection to the buffer memory. 3) If the modem/TA connected to the local station is not initialized, the QC24N-side modem is initialized as well prior to dialing, according to the initialization data designated in the buffer memory.	Section 21.4.8
Y (n+1) 2	Modem disconnection request	Indicates a line-disconnection request from the partner side upon completion of data communication.	Section 21.4.10
Y (n+1) 4	Notification-issued request	1) Indicates the notification request to the partner side. 2) Turns on before completing the QC24N-side modem/TA initialization is complete. 3) Turns off the notification-issued request signal after designating the data for connection in the buffer memory.	Section 21.4.9

POINT

In the descriptions hereafter, I/O signal numbers between QnACPU and QC24N are indicated assuming that the QC24N is installed to slot 0 of the QnACPU basic base unit.

21.3.4 Buffer memory

The buffer memory added for the QC24N modem function is described.

See Section 3.5 for the buffer memory not related to the modem function.

1 Buffer memory list

Address and target I/F		Application	Name			QC24N default value
CH1	CH2					
0H (0)		System setting	LED off request (for LED No. 5 to 13)			0
1H (1)			LED off request (for LED No. 16 to 29)			
2H (2)			For EEPROM access	Register/read/delete instruction		
3H (3)				Frame number instruction		
4H (4)				Register/read/delete result storage		
5H (5)				Number of registration data bytes designation/storage		
6H (6) to 2DH (45)				User registration frame designation/storage *For 40 words		
2EH (46)			For modem functions	Modem connection channel designation		0
2FH (47)				Notification execution designation		0 (Not executed)
30H (48)				Number of connection retries designation		3
31H (49)				Connection retry interval designation		180 (sec.)
32H (50)				Initialization/connection timeout designation		60 (sec.)
33H (51)				Number of initialization retries designation		3
34H (52)				Data number for initialization designation		2000
35H (53)				Data number for connection designation		0
36H (54)				Q6TEL connection designation		0
37H (55)				No-communication interval time designation		30 (min.)
38H (56)				RS·CS control/not-control designation		1 (control)
39H (57) to 3FH (63)			System area (Prohibited to use)			0
40H (64)			Y signal·buffer memory monitoring timing designation			0
41H (65) to 7FH (127)			System area (Prohibited to use)			0
80H(128)			For PLC CPU information clear	PLC CPU information clear request		0
81H (129) to 8FH (143)			System area (Prohibited to use)			0
90H (144)	130H (304)		For modem switching	Switching mode number designation		0
91H (145)	131H (305)			Switching transmission designation		0
92H (146)	132H (306)		System area (Prohibited to use)			0
B2H (178)	152H (338)	System setting	User registration frame for reception designation	Final frame number	(1st)	0DH
B3H (179)	153H (339)				(2nd)	0AH
B4H (180)	154H (340)				(3rd)	0
B5H (181)	155H (341)				(4th)	

Address and target I/F		**Application**	**Name**			**QC24N default value**
CH1	**CH2**					
B6H (182)	156H (342)	System setting	User registration frame for transmission designation	Transmission-in-progress user registration frame number		0
B7H (183)	157H (343)			Schedule designation	CR/LF output	0
B8H (184)	158H (344)				Output head pointer	0
B9H (185)	159H (345)				Number of outputs	0
BAH (186)	15AH (346)			Output frame number designation	(1st)	0
BBH (187) to 11DH (285)	15BH (347) to 1BDH (445)				(2nd) to (100th)	0
11EH (286)	1BEH (446)		Message wait time designation			0

21EH (542)	System information	Number of default registration frame registrations storage				No. of actual registrations
21FD (543)		Number of EEPROM writes				0
220H (544)		EEPROM system setting write result storage				0
221H (545)		For modem function	Modem function error code storage			0
222H (546)			Modem function sequence status storage			0
223H (547)			For EEPROM access	Number of data registrations for connection storage		0 (No registration)
224H (548) 225H (549)				Data registration status for connection storage		0
226H (550)				Number of data registrations for initialization storage		0 (No registration)
227H (551) 228H (552)				Data registration status for initialization storage		0
229H (553)			Number of notification execution storage			0
22AH (554)			For notification execution data storage	Data 1	Notification execution data number	0
22BH (555) 22CH (556) 22DH (557)					System area (Prohibited to use)	0
22EH (558)				Data 2	Notification execution data number	0
22FH (559) 230H (560) 231H (561)					System area (Prohibited to use)	0
to				to	to	
23AH (570)				Data 3	Notification execution data number	0
23BH (571) 23CH (572) 23DH (573)					System area (Prohibited to use)	0
23EH (574) to 24FH (591)		System area (Prohibited to use)				0

Address and target I/F		Application	Name		QC24N default value
CH1	CH2				
250H (592)	260H (608)	System information	Mode setting switch setting status storage		(Depends on the switch setting)
~					~
C00H (3072) to 1AFFH (6911)		For users	User free area *for 3840 words		0
1B00H (6912)		For user registration frame registration	Registration number: 8001H	Number of registration data bytes designation	0
1B01H (6913) to 1B28H (6952)				User registration frame designation *for 40 words	0
1B29H (6953)			Registration number: 8002H	Number of registration data bytes designation	0
1B2AH (6954) to 1B51H (6993)				User registration frame designation *for 40 words	0
1B52H (6994) to 1FCDH (8141)			to	to	
1FCEH (8142)			Registration number: 801FH	Number of registration data bytes designation	0
1FCFH (8143) to 1FF6H (8182)				User registration frame designation *for 40 words	0
1FF7H (8183) to 1FFFH (8191)		——	System area (Prohibited to use)		0

The area in the ▨ are the new area added to the modem function.

IMPORTANT

(1) Perform read/write of the buffer memory (such as changing the default value) according to the description section of the corresponding areas.

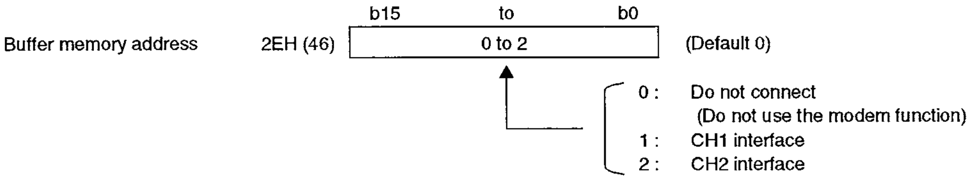
(2) Do not write data into the "system area" of the buffer memory.
Writing data into the "system area" may cause system malfunctions in the PLC.

(3) The buffer memory is not backed up by battery.
The QC24N default values or default values in the QC24N EEPROM registered by the user is written to the special application area during QC24N startup. (See Chapter 15 in the User's Manual.)

2 Details of the buffer memory

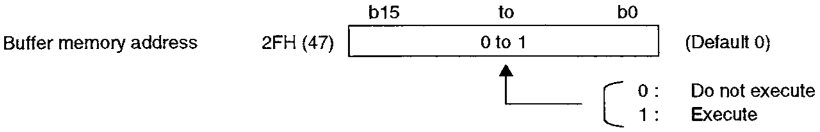
(a) Modem connection channel designation area (address 2EH(46))

The interface on the QC24N side to which a modem/TA is connected is designated.



(b) Notification execution designation area (address 2FH(47))

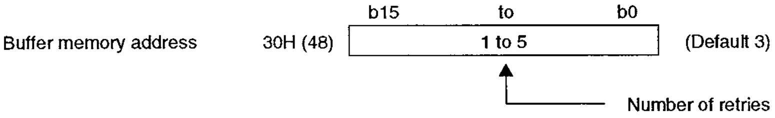
Whether or not to perform notification (message transmission) to the pager receiver during the fall of the notification-issued request signal Y14 is designated.



(c) Number of connection retries designation area (address 30H(48))

① Designates the number of retries for the notification/connection request when the connection could not be made to the partner device by the notification request/connection request.

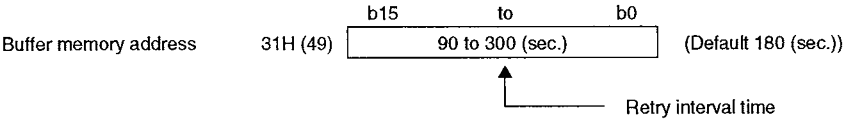
② The default value is recommended for the number of connection retries.



(d) Connection retry interval designation area (address 31H(49))

① Designates the interval time of the retry processing for the notification/connection request when the connection could not be made to the partner device by the notification request/connection request.

② The default value is recommended for the connection retry interval.

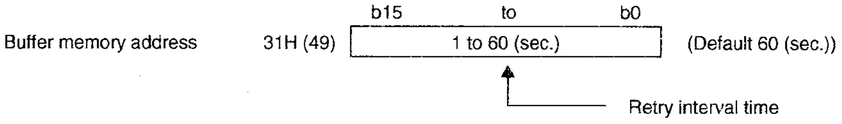


(e) Initialization/connection timeout designation area (address 32H(50))

① The following wait times are designated.

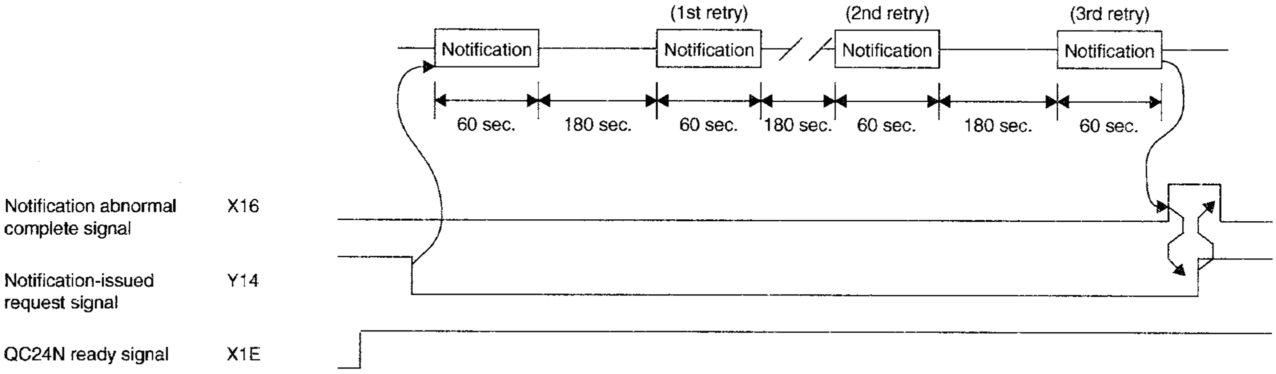
- Wait time until the modem/TA initialization is complete.
- Wait time per wait when the connection could not be made to the destination by the notification/connection request.

② The default value is recommended for the initialization/connection retry timeout.



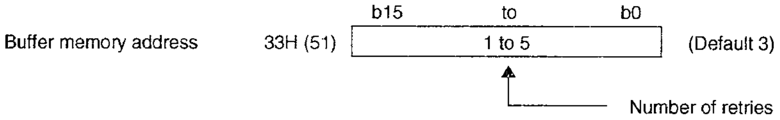
* Shown below is the relationship of the number of connection retries designation, connection retry interval designation and the time for initialization/connection timeout designation used for the notification/connection request to the partner device.

(When the number of retries is 3, retry interval is 180 sec., and timeout is 60 seconds.)



(f) Number of initialization retries designation area (address 33H(51))

The number of retries when the initialization per the initialization request to the modem on to the QC24N side has failed.

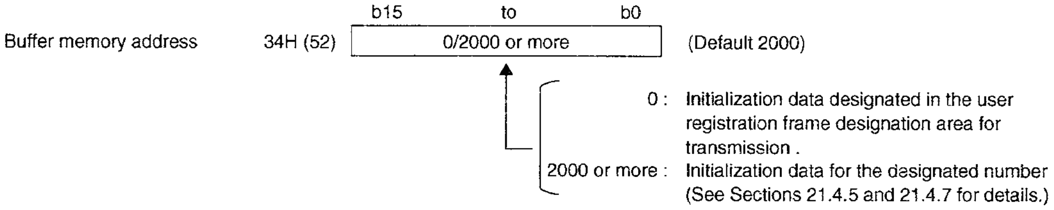


(g) Data number for initialization designation area (address 34H(52))

① The registration number for the initialization data transmitted with the initialization request to the modem on the QC24N side is designated.

The registration number for the QC24N is used.

② The designation method is described in Section 21.4.7.

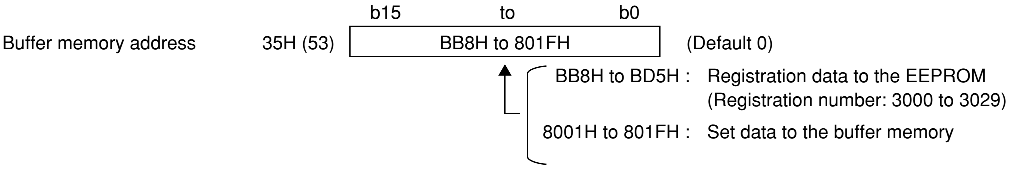


(h) Data number for connection designation area (address 35H(53))

① Designates the registration number of the data for connection used by the QC24N for the connection processing to the partner device in order to perform data communication/notification.

The registration number for the QC24N is used.

② The designation method is described in Section 21.4.8.

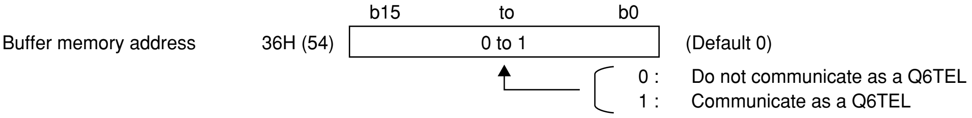


(i) Q6TEL connection designation area (address 36H(54))

① Whether to access the PLC from the peripheral device for GPPQ by connecting the QC24N and peripheral device for GPPQ using the QC24N modem function is designated.

② When connecting the QC24N and peripheral device for GPPQ using the QC24N modem function, select "personal computer-side interface = via QnA modem interface module" in the GPPQ connection designation (When connecting direct shown in Section 21.2.3).

When this GPPQ designation is performed, designate "1" in this area on the QC24N side.

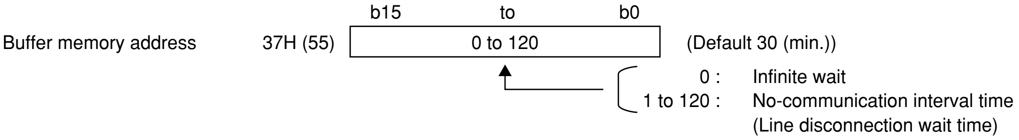


(j) No-communication interval time designation area (address 37H(55))

① Designates the wait time until the line is closed when the data communication has ceased with the destination device after the line connection.

② The QC24N automatically performs the line disconnection processing when no data communication is performed with the destination device for a designated time.

When the line is disconnected, the connecting (X12) signal and the initialization ended (X10) signal turn off, and the modem disconnection ended (X14) signal turns on.



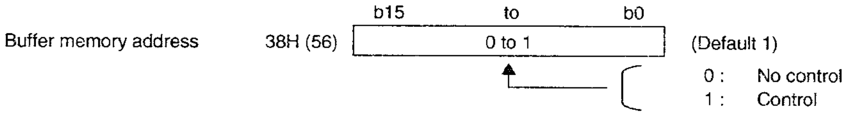
(k) RS·CS control / not-control designation area (address 38H(56))

① Designates whether to use the RS·CS signals for controls to notify local station-side data reception capability to the partner side during data transmission between the QC24N and modem/TA.

② This setting is for the interface designated by the modem connection channel indicated in (a).

The control of the other interface that does not use the modem function is performed by the settings in the buffer memory DTR/DSR and DC control designation area (address: 93H/133H).

* Among the settings of the DTR/DSR and DC control designation area in the buffer memory (address: 93H/133H), the setting for the interface that uses the modem function is ignored.



Remark

The overview of the RS·CS controls are described.

(1) When transmission data

① The QC24N detects the modem/TA data reception capability from on/off of the CS signal.

② When the CS signal is on, data transmission from the QC24N starts or continues.

When the CS signal is off, data transmission from the QC24N is interrupted.

(2) When reception data

① The QC24N side reception capability is notified to the modem/TA by the on/off of the RS signal.

② When the RS signal is on, the QC24N can receive data. Start/continue data transmission from the modem/TA to the QC24N.

When the RS signal is off, the QC24N cannot receive data. Cancel data transmission from the modem/TA to QC24N.

③ The on/off of the RS signal is controlled by the following conditions of the QC24N:

- ON → OFF control of the RS signal

  Performed when the OS area for reception data storage in the QC24N becomes 64 bytes or less.

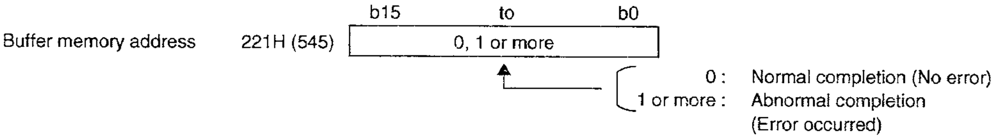
- OFF → ON control of the RS signal

  Performed when the OS area for reception data storage in the QC24N becomes 263 bytes or more.

(l) Modem function error code storage area (address 221H(545))

① Stores the error code when an error occurs during the modem function or abnormal signal (such as the initialization/connection abnormal completion X13) turns on.

② See Section 22.1.4 for the error codes.



(m) Modem function sequence status storage area (address 222H(546))

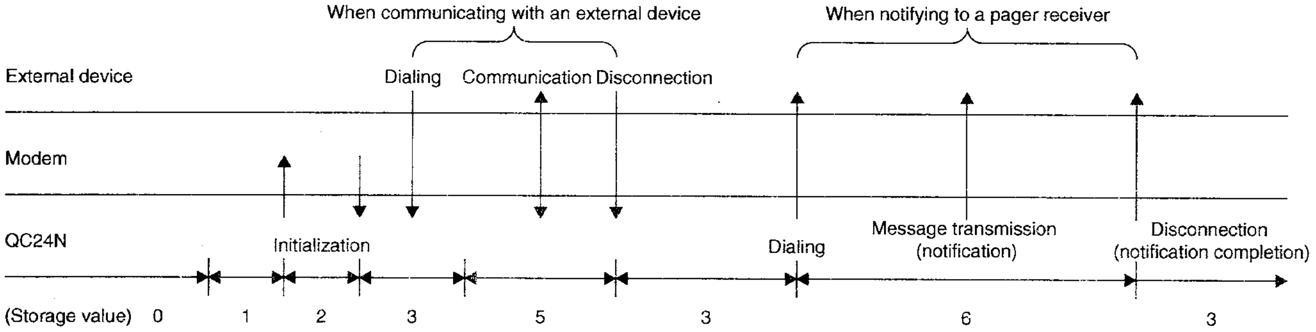
The current status of the modem function is stored as a number.

b15 to b0

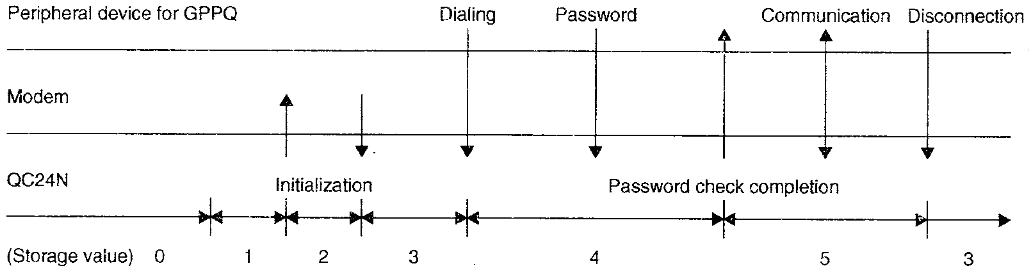
Buffer memory address 222H (546) [0 to 6]

0 : Idle status	Not connected to the modem
1 : Wait for initialization	Standby status for the initialization command issuance for the modem
2 : Modem initialization in progress	Initializing the modem using the AT command
3 : Standby status	Dialing wait status from the external device Or connection complete wait status from the external device by the connection request.
4 : Checking password	Checking the Q6TEL password received from the GPPQ
5 : Communication in progress	Data transmission/reception status with an external device
6 : Notification in progress	Notifying to a pager receiver, etc.

(Example 1) When communicating with an external device or notifying to a pager receiver



(Example 2) When communicating with a peripheral device for GPPQ



(n) For EEPROM access: Number of data registrations for connection storage area (address 223H(547))

① Stores in EEPROM the number of registered data for connection used by the QC24N for the connection processing with the partner device in order to perform data communication/notification.

The number of registrations is the number of data for connection registered to the EEPROM by the user.

② The registration of data for connection is described in Section 21.4.6.

b15 to b0

Buffer memory address 223H (547) [0 to 30]

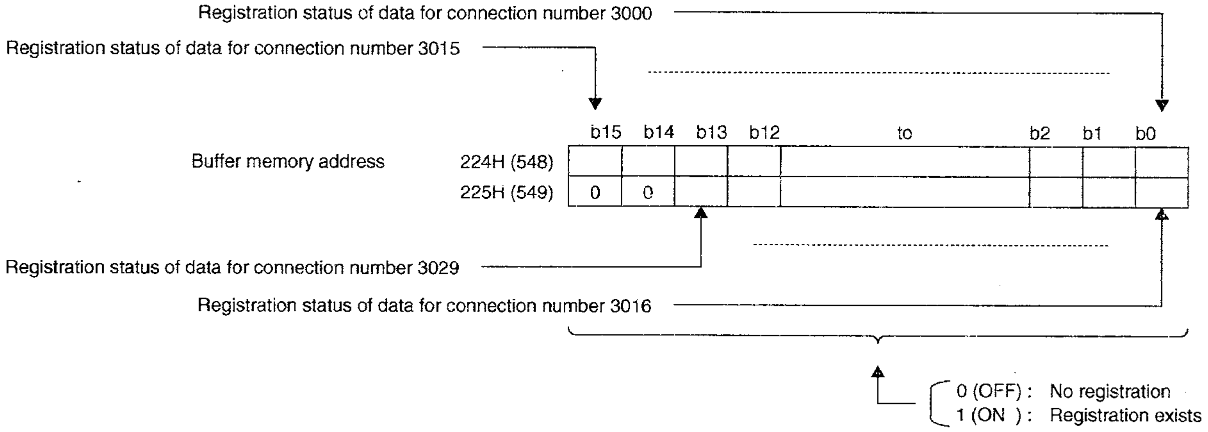
0 : No registration
1 or more : Number of registrations

(o) For EEPROM access: Data registration status for connection storage area (address 224H to 225H(548 to 549))

① Stores in EEPROM registration status of data for connection used by the QC24N in the connection processing with the partner device in order to perform data communication/notification.

② The registration status of each data for connection with registration numbers of 3000 to 3029 is indicated in the corresponding bit in the range shown in the figure below.

③ The registration of data for connection is described in Section 21.4.6.

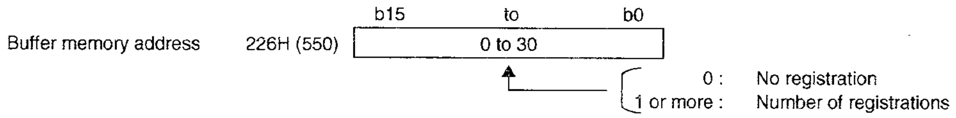


(p) For EEPROM access: Number of data registrations for initialization storage area (address 226H(550))

① Stores in EEPROM the number of data registrations for initialization, sent to the modem on the QC24N side with the initialization request.

The number of registrations indicates the number of data for initialization registered to the EEPROM by the user.

② The registration of data for initialization is described in Section 21.4.5.

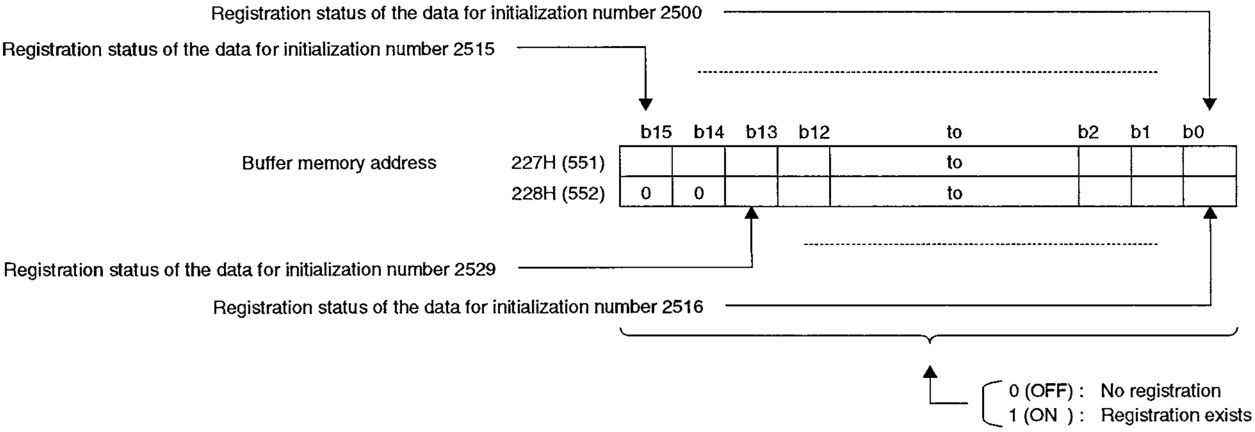


(q) For EEPROM access: Data registration status for initialization storage area (address 227H to 228H(551 to 552))

① Stores in EEPROM registration status for initialization of data for initialization transmitted with the initialization request to the modem on the QC24N side.

② The registration status of each data for initialization with registration numbers of 2500 to 2529 is indicated in the corresponding bit in the range shown in the figure below.

③ The registration of data for initialization is described in Section 21.4.5



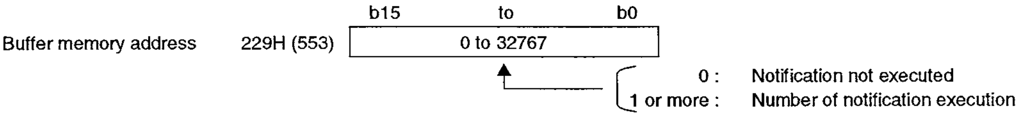
(r) Number of notification execution storage area (address 229H(553))

① Stores the number of execution of the QC24N notification (message transmission) processing for the pager receiver.

② The storage value when the number of notification execution exceeds 32767 remains at 32767.

③ The value for this area can be changed by the user in the range of 0 to 32767.

When the storage value is changed by the user, the number of execution is stored according to the changed value.

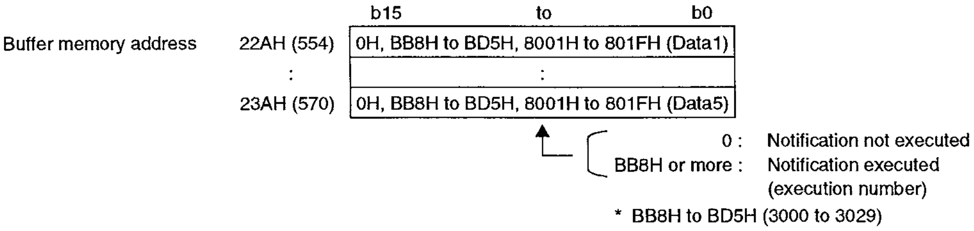


(s) For notification execution data storage: Notification execution data number storage area (address 22AH, 22EH... (554, 558...))

① Stores the registration number of the data for connection used in the QC24N notification (message transmission) processing to the pager receiver as log information.

② The latest five data is stored in order at the corresponding areas (data 1, data 2, ...). (The latest information is stored in the data 1 notification execution data number storage area.)

The old notification execution data number other than the latest five are deleted in order.



(t) For user registration frame registration: Number of bytes in registration data designation area (address 1B00H, 1B29H... (6912, 6953...))

① The initialization data or data for connection can be stored into the buffer memory as well as the QC24N's EEPROM.

Data type	Registration destination		Registration number (Decimal (Hex.))
Initialization data	EEPROM	Data registered by the OS	2000 to 2004 (7D0H to 7D4H)
		User-registered data	2500 to 2529 (9C4H to 9E1H)
	Buffer memory	(All registered by user)	-32767 to -32737 (8001H to 801FH)
Data for connection	EEPROM	(All registered by user)	3000 to 3029 (BB8H to BD5H)
	Buffer memory	(All registered by user)	-32767 to -32737 (8001H to 801FH)

* A registration number for the initialization data or data for connection to the buffer memory is in the range of -32767 to 32737 (8001H to 801FH), and determined by the used area.

② In this area, the number of bytes for the initialization data or data for connection (for 1 data) to be registered to the buffer memory is designated.

③ The registration of data for initialization is described in Section 21.4.5.

The registration of data for connection is described in Section 21.4.6.

Buffer memory address	b15 to b0
1B00H (6912)	0 to 78/80
:	:
1FCEH (8142)	0 to 78/80

(Number of bytes)
0 : No registration data
1 to 78 : Registration data exists (for initialization)
80 : Registration data exists (for connection)

(u) For user registration frame registration: User registration frame designation area (address 1B01H to 1B28H, 1B2AH to 1B51H...(6913 to 6952, 6954 to 6993...))

① When registering the initialization data or data for connection to the buffer memory, the number of registration data bytes (for 1 data) is designated.

② The registration of data for initialization is described in Section 21.4.5.

The registration of data for connection is described in Section 21.4.6.

Buffer memory address	b15 to b0
1B01H (6913) to 1B28H (6952)	Data for initialization or data for connection (Area for registration number 8001H)
:	:
1FCFH (8143) to 1FF6H (8182)	Data for initialization or data for connection (Area for registration number 801FH)

21.3.5 Precautions when using the modem function

Precautions when using the QC24N modem function to perform data communication with an external device via public line or call to the pager receiver are described.

1 **Line connection and disconnection**

When performing data communication with an external device, it must be predetermined which station is to perform the line connection (dialing) and disconnection processing with the partner device as well as the timings.

2 **Reception data before connection completion**

Before the connection processing to the modem is completed the reception data other than modem commands is ignored (read and disposed) at the interface (*1) that uses the modem function.

(Example) The QC24N will ignore the data even when a dedicated protocol command message is received.

*1 This is set in the modem connection channel designation area in the buffer memory (address: 2EH).

3 **Transmission control**

Delays may occur in transmission controls to notify the partner device of the data reception capability at the local station.

In order not to have a state in which the partner device cannot receive the transmission data, the amount of transmission/reception data and intervals should be determined beforehand.

When transmission/reception data in the no procedure protocol, the procedure must also be predetermined.

4 **Communication with the peripheral devices for GPPQ**

The QnACPU with QC24N installed can be considered as a PLC CPU station with a Q6TEL installed (or connected), and the PLC can be accessed form the peripheral devices for GPPQ via QC24N.

When the password for Q6TEL is set at the GPPQ in the PLC access from the peripheral device for GPPQ, the password for Q6TEL (*1) is first transmitted from the peripheral device for GPPQ to the QC24N after the connection is complete.

However, since the QC24N does not maintain the password for Q6TEL, it cannot determine whether the password is correct or not.

The QC24N returns the corresponding response, and enables data read/write and status control for the PLC CPU.

*1 The password consists of a string for enabling/disabling access to the PLC via Q6TEL, and is entered using keys on the peripheral device for GPPQ prior to accessing

5 **Priority of data communication and notification**

After line connection is established, the data transmission/reception processing with the partner device is performed in the order of the processing request occurrence.

At the same time, when the line disconnect processing or data transmission reception (including data transmission processing, reception processing and EEPROM access processing) occurs, the line disconnect processing has the priority.

6 **Data communication time**

The data transmission/reception time after line connection has been established with the partner device is the total time of the transmission time between the QC24N and modem/TA, between modem and TA, and between modem/TA and partner device.

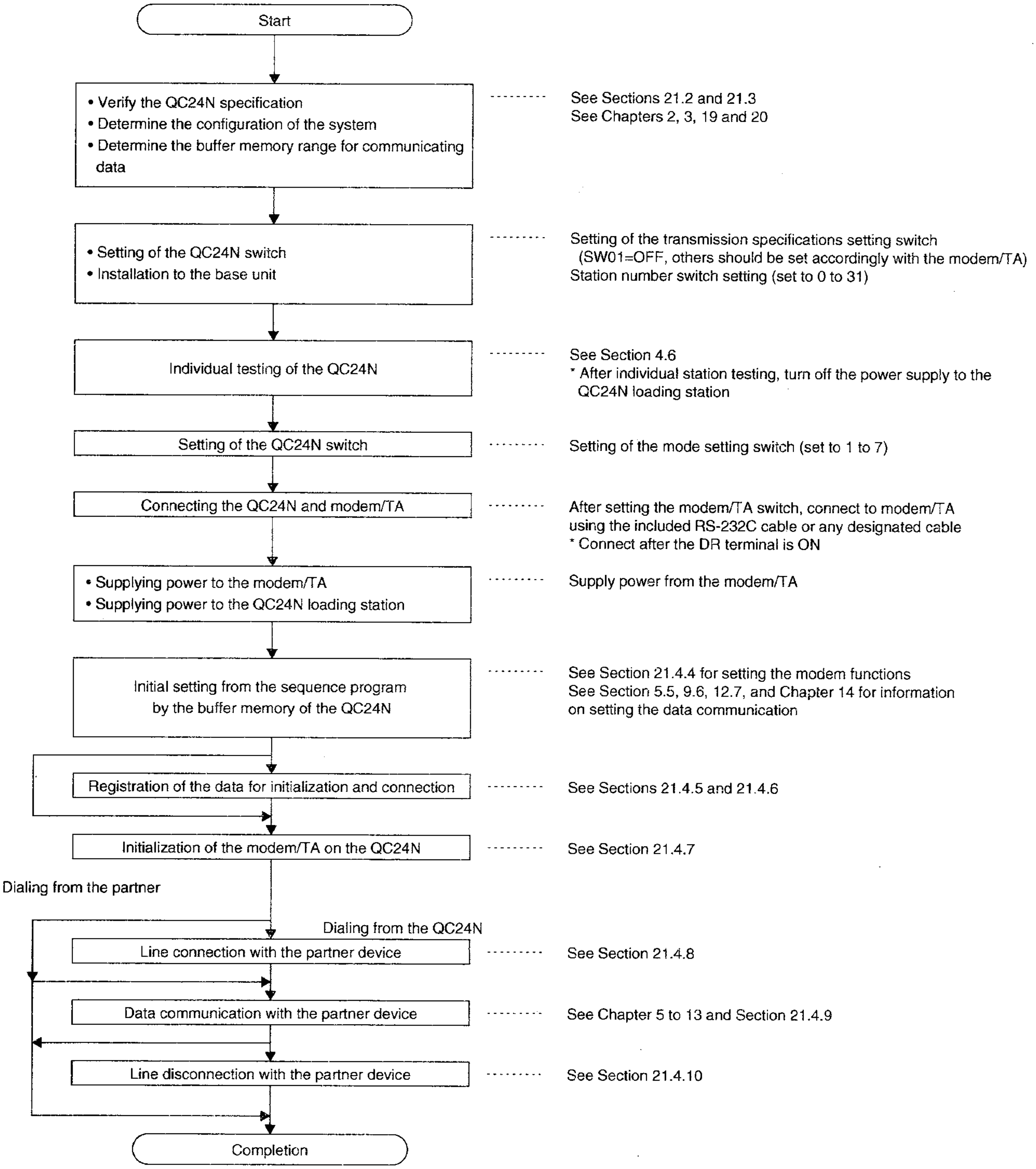
When communicating via the dedicated protocol, the transmission time (such as T0 and T3) indicated in Section 5.7 must include the transmission time between the QC24N-side modem/TA and the destination device.

21.4 Start-up of the Modem Function

This section explains the start-up procedures, processing methods and programming when the modem function of the QC24N is to be used.

21.4.1 Start-up procedures when communicating data with external devices

The following is a summary of the start-up procedures when communicating data with external devices in a remote location via the dedicated protocol/non procedure protocol/bidirectional protocol using the modem functions.



See Sections 21.2 and 21.3
See Chapters 2, 3, 19 and 20

Setting of the transmission specifications setting switch
(SW01=OFF, others should be set accordingly with the modem/TA)
Station number switch setting (set to 0 to 31)

See Section 4.6
* After individual station testing, turn off the power supply to the QC24N loading station

Setting of the mode setting switch (set to 1 to 7)

After setting the modem/TA switch, connect to modem/TA using the included RS-232C cable or any designated cable
* Connect after the DR terminal is ON

Supply power from the modem/TA

See Section 21.4.4 for setting the modem functions
See Section 5.5, 9.6, 12.7, and Chapter 14 for information on setting the data communication

See Sections 21.4.5 and 21.4.6

See Section 21.4.7

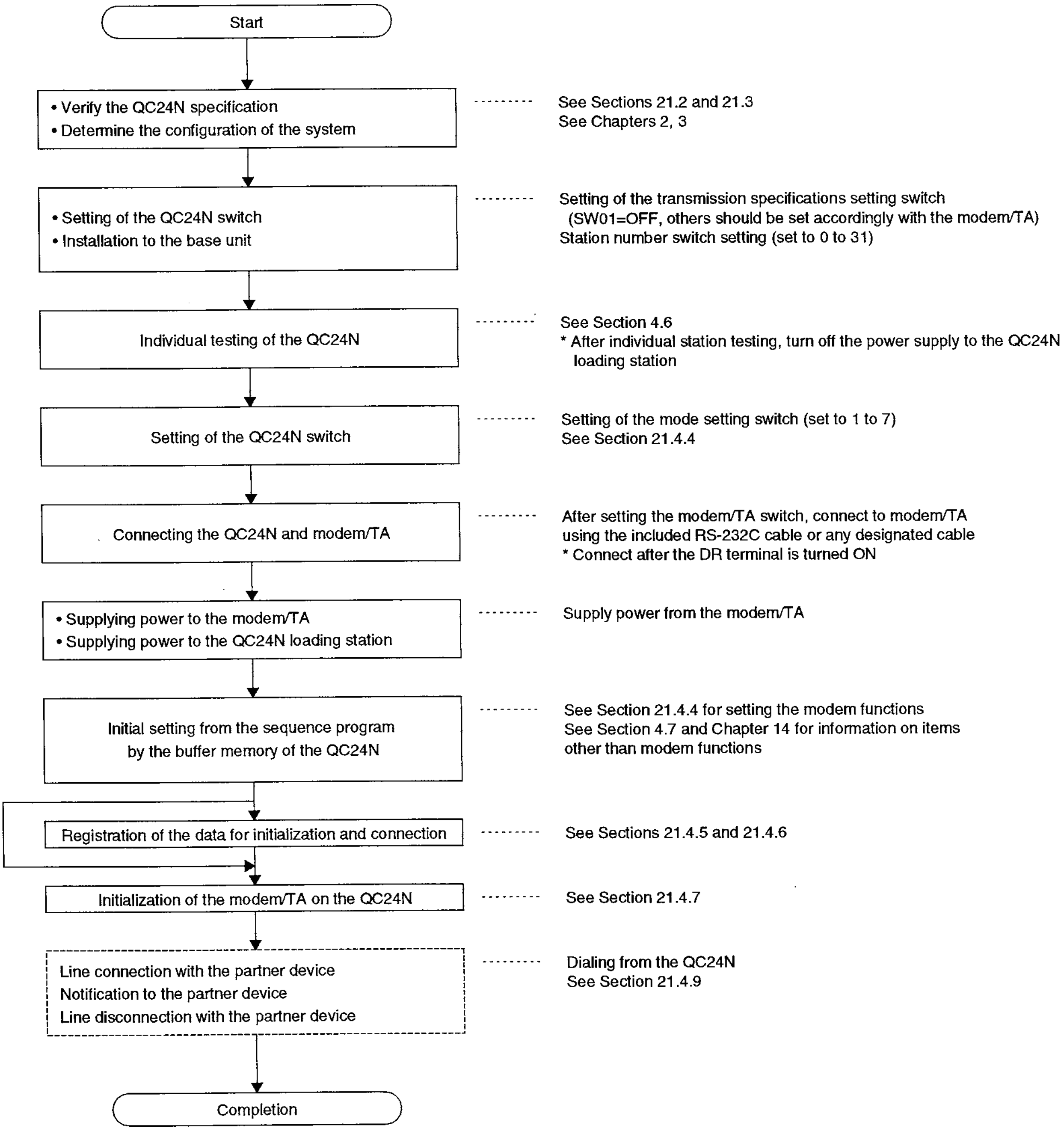
See Section 21.4.8

See Chapter 5 to 13 and Section 21.4.9

See Section 21.4.10

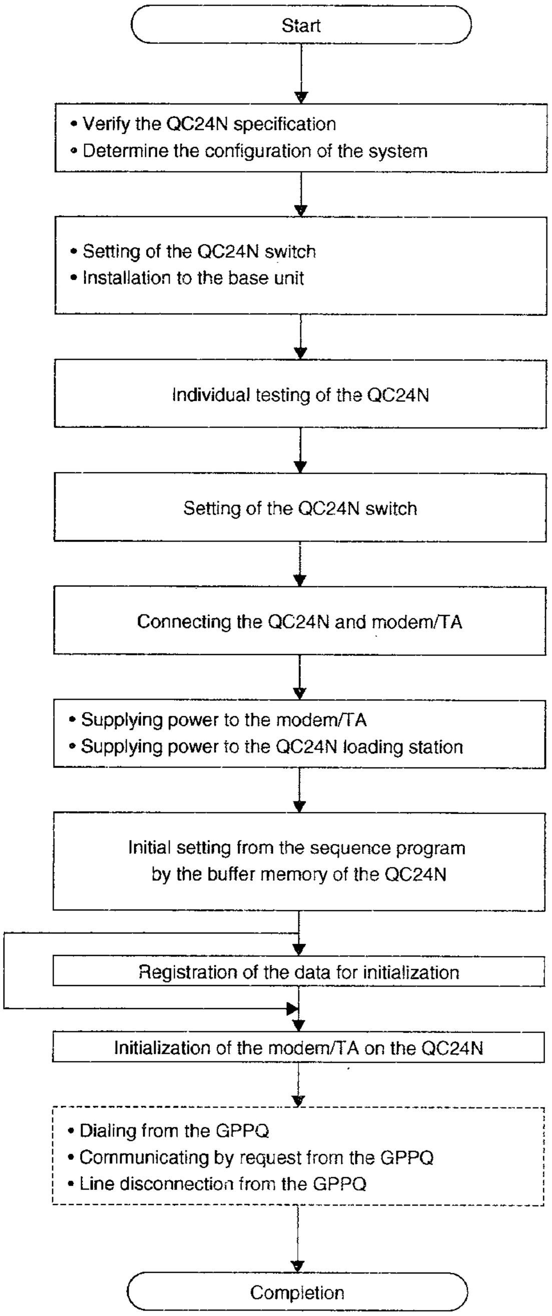
21.4.2 Start-up procedures when using the notification functions

The following is a summary of the start-up procedures when remotely notifying a pager receiver (call-up, message display) using the modem function.



21.4.3 Start-up procedures when using the peripheral devices for GPPQ

The following is a summary of the start-up procedures when accessing a PLC in a remote location from the peripheral devices for GPPQ via the QC24N using the modem function.



See Sections 21.2 and 21.3
See Section 4.9

Setting of the transmission specifications setting switch
(SW01=OFF, others should be set accordingly with the modem/TA)
Station number switch setting (set to 0 to 31)

See Section 4.6
* After individual station testing, turn off the power supply to the QC24N loading station

Setting of the mode setting switch (set to 5)
See Section 21.4.4

After setting the modem/TA switch, connect to the modem/TA using the supplied RS-232C cable or any designated cable (only CH1 side enable)
* Connect after the DR terminal is turned ON

Supply power from the modem/TA

See Section 21.4.4

See Section 21.4.5

See Section 21.4.7

See the GPPQ Operating Manual (Online)

POINT

The above procedures are used when accessing a remote PLC from a peripheral device for GPPQ using a public line via the QC24N.
When accessing the PLC with the peripheral device for GPPQ directly connected to the QC24N channel 1 (CH1) interface without using the modem function of the QC24N, perform the setting described in Section 4.9.

21.4.4 Initial settings of the QC24N

The following explains the initial settings of the QC24N when data communicating with external device or remotely notifying a pager receiver (call-up, message display) using the modem function.

1 Switch settings

Switch			Data communicate	Notification	GPPQ access	Remarks
Mode setting switch		MODE	1 to 7	1 to 7	5	—
Transmission specification setting switch	Operation setting	SW01	OFF (Independent operation)			Set both CH1 and CH2 OFF
	Data bit setting	SW02	(Set according to modem/ TA on local station)		(Set according to modem/TA on local station) (*1)	OFF=7 bits, ON=8 bits
	Setting of parity/non-parity	SW03				OFF = Non-parity, ON = Parity
	Even/odd parity setting	SW04				OFF = Odd, ON = Even
	Stop bit setting	SW05				OFF = 1 bit, ON = 2 bits
	Sum check enable/disable setting	SW06	(Set according to system specification)	OFF/ON	ON	OFF = Disabled, ON = Enabled
	Write during RUN enable/ disable setting	SW07		OFF/ON	ON	OFF = Disabled, ON = Enabled
	Setting modifications enable/disable setting	SW08		OFF/ON	OFF/ON	OFF = Disabled, ON = Enabled
	Transmission speed setting	SW09 to SW12	(Set according to modem/TA on local station)			(bps)
Station number setting switch		STATION NO.	00 to 31			—

*1 The peripheral device for GPPQ side communicates with a modem with the following settings:

- Data bit length : 8 bits
- Parity bit : Non-parity
- Stop bit length : 1 bit
- Transmission speed : 19200 BPS (When communication is not possible, auto-switched to 9600 BPS)

2 Initial settings of the buffer memory

(a) Perform initial settings on the interface side that use the modem function as outlined below:

① Modem connection channel (Set using address 2EH)

Be sure to set the interface side that uses the modem function. However, at the interface side that uses the modem function, all reception data other than modem commands prior to the completion of the connection process with the modem will be ignored (read and discarded).

② Notify enabled/disabled (Set using address 2FH)

When notifying to a pager receiver, always set to "Notify."

③ Q6TEL connection (Set using address 36H)

When accessing the PLC from the peripheral device for GPPQ through the QC24N considering the QC24N as a Q6TEL, set as "Communication as Q6TEL."
(When connecting direct shown in Section 21.2.3)

④ No-communication interval time (Set using address 37H)

Even if the PLC CPU on the QC24N loading station (local station) becomes STOP state under the following circumstances, the line (telephone) with the partner devices will be left connected. In order to prevent the line from being left connected when the line is not in use, be sure to make the appropriate settings.

- When the PLC CPU is stopped when the connected signal (X(n+1)2) is at the ON state.

* This occurs because the program write after remote stop is enabled.

- When the PLC CPU performs an error stop during self-diagnosis, etc.

POINT

When setting the No-communication interval time as infinite wait (set value = 0), be sure to perform line disconnection processing after the data has been communicated. If the line is left connected for long periods of time without performing line disconnection after data has been communicated, not only will telephone bills be applied, but it may violate electronic communication business laws.

(b) All transmissions using the modem function are transmitted in full-duplex.

Leave the following initial settings for the interface side that uses the modem function as default.

(Default value)

① CD terminal check (Set using address 97H/137H) : Not checked

② Communication system (Set using address 98H/138H) : Full-duplex communication

(c) The processes that correspond to the following output signals may not be aborted.

Output signal	Requesting process name
Y10	Initialization request (standby request)
Y11	Connection request
Y12	Modem disconnection request
Y14	Notification-issued request

It is recommended to leave the following initial settings for the modem functions as default.
(Upon error, it will end due to time out.)

(Default value)

① Number of connection retries (Set using address 30H) : 3 times

② Connection retry intervals (Set using address 31H) : 180 seconds

③ Initialization/connection time out (Set using address 32H) : 60 seconds

21.4.5 Registration/reading/deletion of initialization command

The registration/reading/deletion of the data for initialization such as initialization commands for the modem/TA connected to the QC24N side for data communication with the external device and pager receiver notification using the QC24N modem functions are explained below.

1 Registration destination of the data for initialization

① The data for initialization may be used by registering to the QC24N EEPROM or buffer memory.

② The buffer memory may register the data for connection shown in Section 21.4.6 and will register the data for initialization or data for connection in the designated area.

③ It is recommended to store the data for initialization to the EEPROM after completing the debug process.

By registering it to the EEPROM, the registration process of the data for initialization will be unnecessary thereafter.

④ It is recommended that the data for initialization during the debug process is stored in the buffer memory. The registration data in the buffer memory will be erased after starting up the QC24N loading station again. It is necessary to register the data for initialization in the buffer memory after each start-up of the QC24N.

2 Types of data for initialization

① There are data for initialization that are registered in the EEPROM of the QC24N upon shipping and data for initialization that are set by the user.

② The number of times registered/number of possible registrations are shown in the chart below.

3 Data for initialization registration number

① The registration numbers shown in the table below are used from the memory of the registration destination.

② The data for initialization registration number registered in the buffer memory is determined by the area of registration.

Registration data	Registration destination		Registration number (Decimal (hexadecimal))	Number of registrations
Data for initialization	EEPROM	Data registered by the OS	2000 to 2004 (7D0H to 7D4H)	5
		Data registered by the user	2500 to 2529 (9C4H to 9E1H)	30
	Buffer memory	(All are set by the user)	-32767 to -32737 (8001H to 801FH)	31

4 Precautions during the registration of data for initialization

① The maximum size of the initialization commands that may be registered as one data for initialization is 78 bytes (78 bytes in single-byte characters)

② Do not include CR/LF (data code : 0DH/0AH) in the data for initialization to be registered to the QC24N. The CR/LF is automatically added at the end of the AT command by the QC24N.

③ The registration status of the data for initialization stored in the EEPROM may be checked in the buffer memory (address : 226H to 228H (550 to 552).

When newly registering, register by designating an unregistered number.

When designating a registration number that has already been registered, first delete the registration data in the preoccupied registration number prior to registration.

④ When connecting the QC24N to an external device using a cellular phone and a modem, set the transmission speed supported by the cellular communication module on the modem side.

5 Registration contents at shipment

① The data for initialization registered in the EEPROM of the QC24N are shown below:

Registration number		Initialization command
Hexadecimal	Decimal	
7D0H	2000	ATQ0V1E1X1\J0\Q2\V2\N3S0=1
7D1H	2001	ATQ0V1E1X1\Q2\V2\N3S0=1
7D2H	2002	ATQ0V1E1X1&K3\N3S0=1
7D3H	2003	ATQ0V1E1X1&H1&R2&A3&D2S0=1
7D4H	2004	ATQ0V1E1X1\J0\Q2\N3S0=1

② If initialization commands other than listed above are needed, the data for initialization needs to be registered to the EEPROM or the buffer memory of the QC24N.

Remark

- Perform the following setting in respect to the modem/TA connected to the QC24N side.

  For settings other than listed below, perform the setting as specified by the modem/TA.

Setting contents	Setting command example
—	AT
Display the result code (or, return the result code).	Qn
Set the result code as a word.	Vn
Perform character echo.	En
Dial tone and busy tone detection + X1	Xn
Set register 0 at 2	Sr=n
The modem and the serial speed are not equal.	\Jn
Control RTS/CTS.	\Qn
Control DSR.	&Sn
Control DTR.	&Dn
Enable extension result code (display MNP class).	\Vn
MNP/normal mode auto selection	\N3

- The following shows an specification example of the transmission speed supported by the cellular communication module using the modem initialization command, when connecting the QC24N to an external device using a cellular phone and a modem.

  For the details, see the manual of the modem used.

  (When changing the data for initialization of registration number 2003.)

  ATQ0V1E1X1&H1&R2&A3&D0S0=1&N6

  (When changing the data for initialization of registration number 2004.)

  ATQ0V1E1X1\J0\Q2\N3&D0+MS=,,9600, 9600S0=1

6 Data for initialization registration/reading/deletion method

(a) In respect to the EEPROM in the QC24N

① Data for initialization registration/reading/deletion is performed using the EEPROM access area in the buffer memory used in the registration/reading/deletion process of the user registration frame (address : 2H to 2DH) and the EEPROM read/write signal of the I/O signal (X/Y17 toX/Y18).

② The buffer memory and the designated/stored value of each area that is used for the registration, reading, and deletion process of the data for initialization are shown below.

For details, see Chapter 16.

(Read the table by replacing the user registration frame with the data for initialization.)

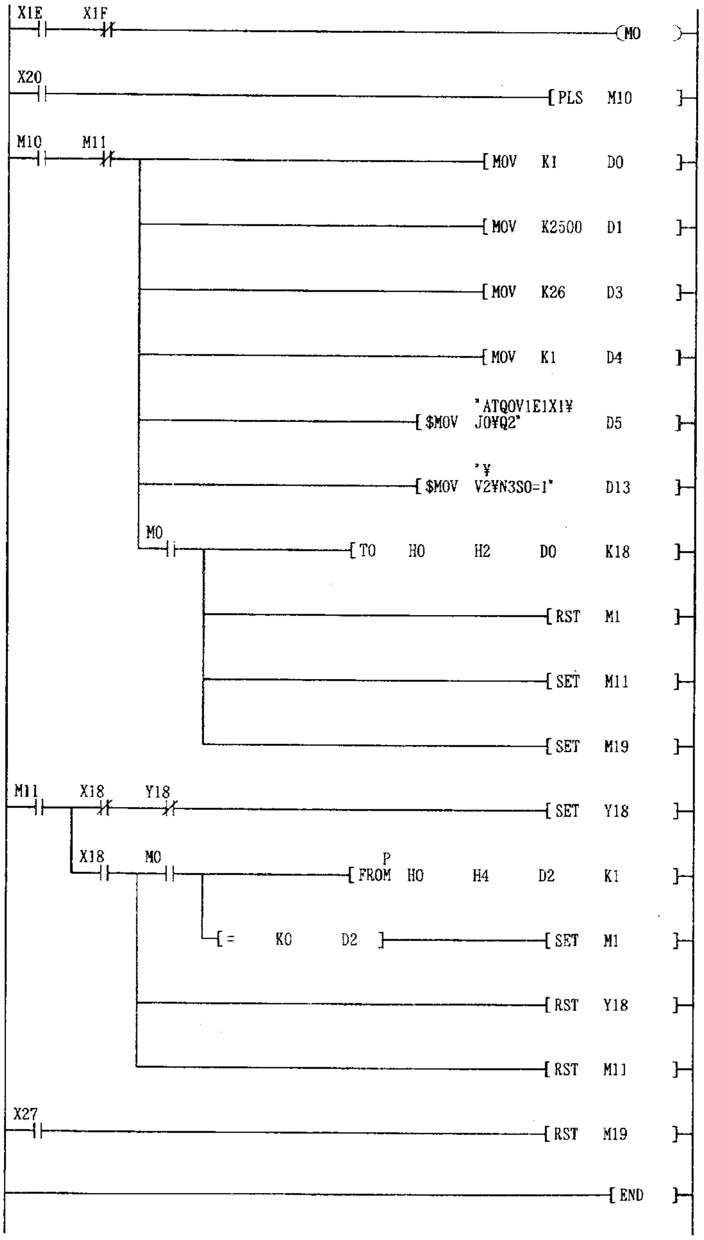
Address		Name		Designated/stored value	Designation necessary (O)/unnecessary (x)		
Hexadecimal	Decimal				Registration	Reading	Deletion
2H	2	Registration/reading/ deletion instruction		0 : No request 2: Read request 1 : Registration request 3: Delete request	○		
3H	3	Frame number instruction (*1)		0 : No frame number designated 2500 to 2529 :Registration number of the data for target initialization	○		
4H	4	Registration/reading/ deletion result storage (*2)		0 : Normal completion Other than 0 : Abnormal completion	× (Stored)		
5H	5	Number of registration data bytes designation		1 to 78 : Number of registration data bytes (Applicable only to the initialization command section.)	○	× (Stored)	×
6H	6	Registration/ read data	User control data	Arbitrary data that the user uses to control registration data (manufacturer code, control number, etc.)			
7H to 2DH	7 to 45		Initialization command	Data code for the initialization command for registration/read			

*1 The data for initialization stored in the EEPROM of the QC24N upon shipping cannot be deleted.

*2 When an abnormal completion occurs, the error code is stored. Perform corrective actions and verification of the error content according to Section 22.1.

③ An example of a sequence program used for registration/reading/deletion of data for initialization is shown below.

- Example of registration data for initialization



X1E: QC24N ready signal
X1F: WDT error signal

Convert the registration command into pulse

Set the registration request

Set the data for initialization registration number

Set the number of registration data bytes

Set user controlled data (control number)

Initialization command

Continuation of initialization command

Buffer memory write

Write the request signal is turned ON

Read the execution results

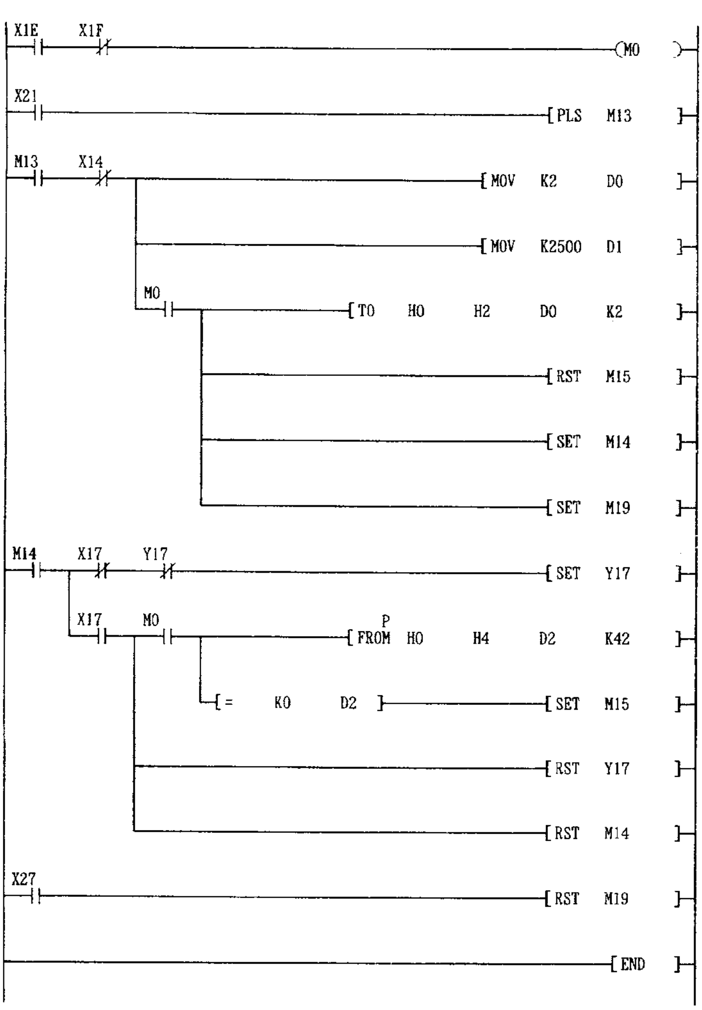
When the normal completion, the complete flag is turned ON

When the write complete signal ON, the request signal is turned OFF

When the clear command of the flag, the write flag is turned OFF

(Item name)	(Address)	Buffer memory		EEPROM (Area for registration No. 2500)	
Registration/reading/deletion instructions	2H	1			
Frame number instructions	3H	2500			
Registration/reading/deletion results	4H	0	←		
Number of registration data bytes	5H	23	→	23	Data for initialization
User control data	6H	1	→	1	
Initialization command	7H to 2DH	Initialization command	→	Initialization command	

- Example of reading data for initialization



X1E: QC24N ready signal

X1F: WDT error signal

Convert the read command into pulse

Set the read request

Set the data for initialization registration number

Buffer memory write

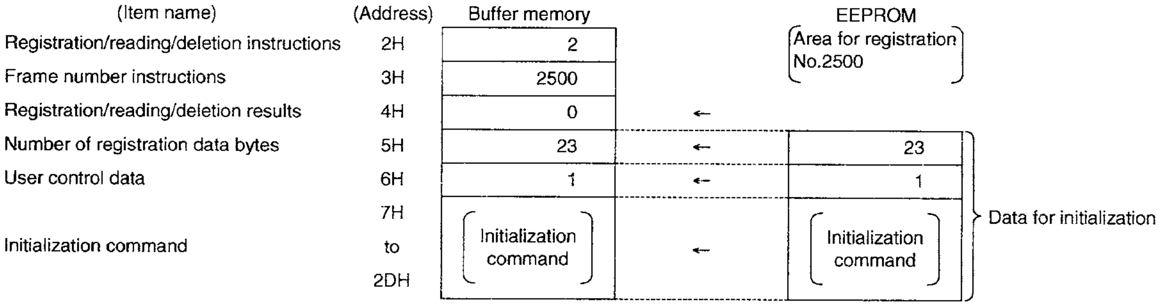
Read request signal is turned ON

Read execution results

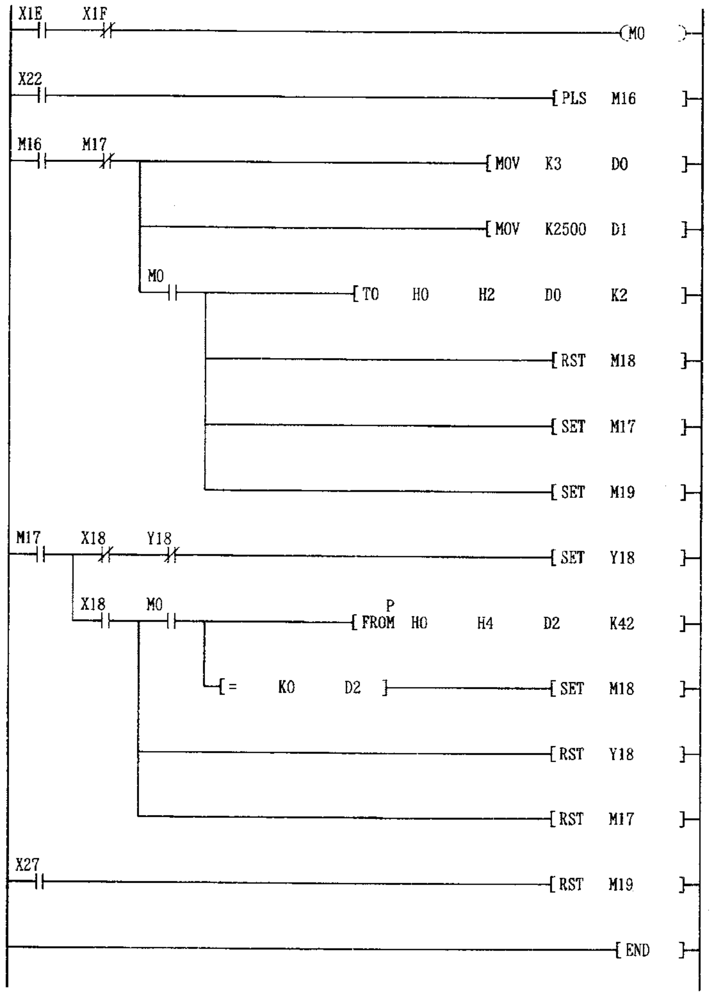
When the normal completion, the complete flag is turned ON

When the read complete signal ON, the request signal is turned OFF

When the clear command of the flag, the write flag is turned OFF



- Example of deletion data initialization



X1E: QC24N ready signal

X1F: WDT error signal

Convert the delete command into pulse

Set the delete request

Set the data for initialization registration number

Buffer memory write

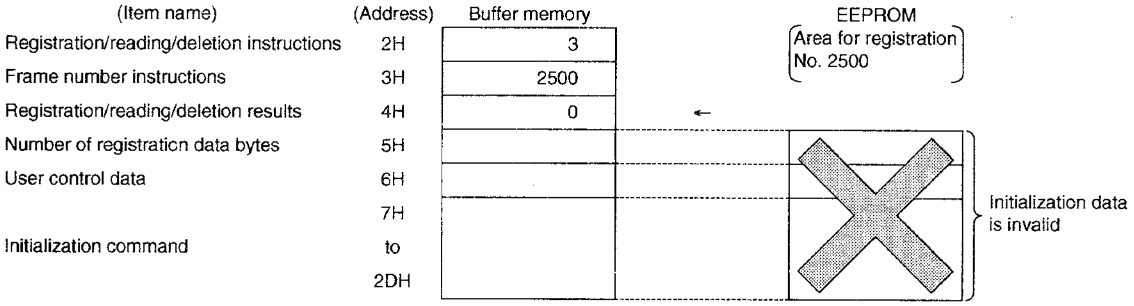
Write request signal is turned ON

Read execution results

When the normal completion, the complete flag is turned ON

When the write complete signal ON, the request signal is turned OFF

When the clear command of the flag, the write flag is turned OFF



(b) In the case of the buffer memory of the QC24N

① The data for initialization write (registration)/read is performed by designating a corresponding area that is compatible with registration number 8001H to 801FH in respect to the area for user registration frame registration (address : 1B00 to 1FF6H).
When deleting the data for initialization, write "0" to the number of registration data bytes designation area.

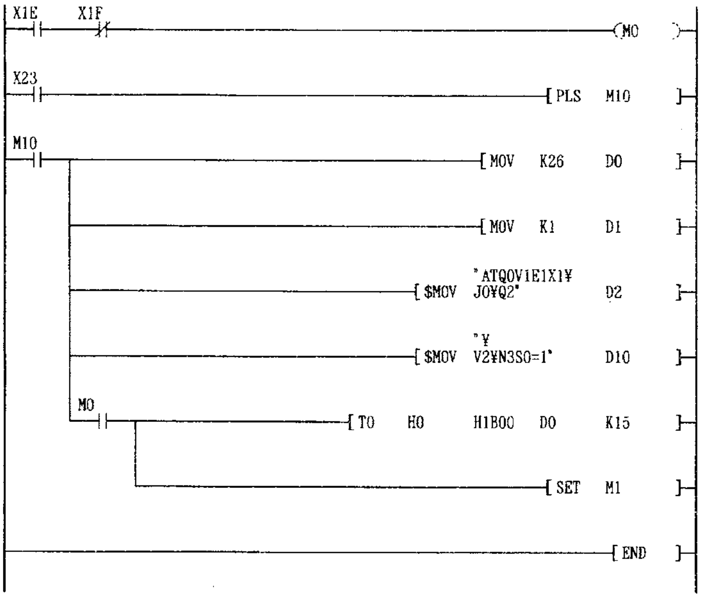
② An overview of the buffer memory used in the writing, reading, and deleting process of the data for initialization as well as the designated value for each area are shown in the table below.
For details, see Chapter 16.
(Read the table by replacing the user registration frame with the data for initialization.)

Address		Name		Designated/stored value	Designation necessary (O)/unnecessary (×)		
Hexadecimal	Decimal				Write	Read	Deletion
1B00H	6912	Registration number 8001H	Number of registration data bytes designation	0 : When deleting 1 to 78 : Number of registration data bytes (Applicable only to the initialization command section.)	○	Read processing unnecessary	○
1B01H	6913		User control data	Arbitrary data that the user uses to control registration data (manufacturer code, control number, etc.)			×
1B02H to 1B28H	6914 to 6952		Initialization command	Data code for the initialization command for register			
1B29H	6953	Registration number 8002H	Number of registration data bytes designation	0 : When deleting 1 to 78 : Number of registration data bytes (Applicable only to the initialization command section.)	○	Read processing unnecessary	○
1B2AH	6954		User control data	Arbitrary data that the user uses to control registration data (manufacturer code, control number, etc.)			×
1B2BH to 1B51H	6955 to 6993		Initialization command	Data code for the initialization command for register			
1FCEH	8142	Registration number 801FH	Number of registration data bytes designation	0 : When deleting 1 to 78 : Number of registration data bytes (Applicable only to the initialization command section.)	○	Read processing unnecessary	○
1FCFH	8143		User control data	Arbitrary data that the user uses to control registration data (manufacturer code, control number, etc.)			×
1FD0H to 1FF6H	8144 to 8182		Initialization command	Data code for the initialization command for register			

③ The contents of the data to be written into the designated area that is compatible with registration number 8001H to 801FH is the same as the situation in respect to the EEPRQM.

④ An example of a sequence program used for writing (registering) of data for initialization is shown below.

- Example of writing data for initialization to the registration number 8001H area



X1E: QC24N ready signal
X1F: WDT error signal

Convert the registration command into pulse

Set the number of registration data bytes

Set the user control data (control number)

Initialization command

Continuation of initialization command

Buffer memory write

Complete flag is turned ON

(Item name)		Data register		(Address)	Buffer memory Area for registration No. 8001H	
Number of registration data bytes	D0	23	→	1B00H	23	Data for initialization
User control data	D1	1	→	1B01H	1	
Initialization command	D2 to D13	Initialization command	→	1B02H to 1B0DH	Initialization command	
				to 1B28H		

21.4.6 Registration/reading/deletion of data for connection

This section explains the registration/reading/deletion of data for connection such as the telephone number of the partner device and notification messages that are used for communicating data with external devices and notify pager receivers using the QC24N modem functions.

1 **Registration destination of data for connection**

① The data for connection can be used by registering to the QC24N's EEPROM or buffer memory.

② The buffer memory can register the data for initialization shown in Section 21.4.5. The data for initialization or data for connection will be registered in the applicable area.

③ It is recommended to store the data for connection to the EEPROM after completing the debug process.

By registering it to the EEPROM, the registration process of the data for connection will be unnecessary thereafter.

④ It is recommended to store the data for connection during the debug process in the buffer memory. The registration data in the buffer memory will be erased after the starting up the QC24N loading station again. It is necessary to register the data for connection in the buffer memory after each start-up of the QC24N.

2 **Types of data for connection**

① All data for connection are registered and used as defined by the user.

② The number of possible registrations are shown in the table below.

3 **Data for connection registration number**

① The registration numbers shown in the table below are used by the memory of the registration destination.

② The data-for-connection registration number registered in the buffer memory is determined by the area of registration.

Registration data	Registration destination		Registration number (Decimal (hexadecimal))	Number of registrations
Data for connection	EEPROM	(All are set by user)	3000 to 3029 (BB8H to BD5H)	30
	Buffer memory		-32767 to -32737 (8001H to 801FH)	31

4 **Precautions during the registration of data for connection**

① The maximum size of data that can be registered as one data for connection is 80 bytes. Do not deviate from the following data sizes for the following items:

Message area for notification = 36 bytes, data-for-connection area = 44 bytes

② Designate the messages for notification accordingly with the display designation of the partner devices.

③ The registration status of the data for initialization stored in the EEPROM can be checked in the buffer memory (address : 223H to 225H (547 to 549)

When newly registering, register by designating an unregistered number.

When designating a number which is already registered, delete the registered data for that number first, then perform the registration.

5 **Data for connection registration/reading/deletion method**

(a) In respect to the EEPROM in the QC24N

① Registration/reading/deletion of data for connection is performed using the EEPROM access area in the buffer memory used in the registration/reading/deletion process of the user registration frame (address : 2H to 2DH) and the EEPROM read and write I/O signals (X/Y17 to X/Y18).

② The buffer memory and the designated/stored value of each area used for the registration, reading and deletion process of data for connection is shown below.

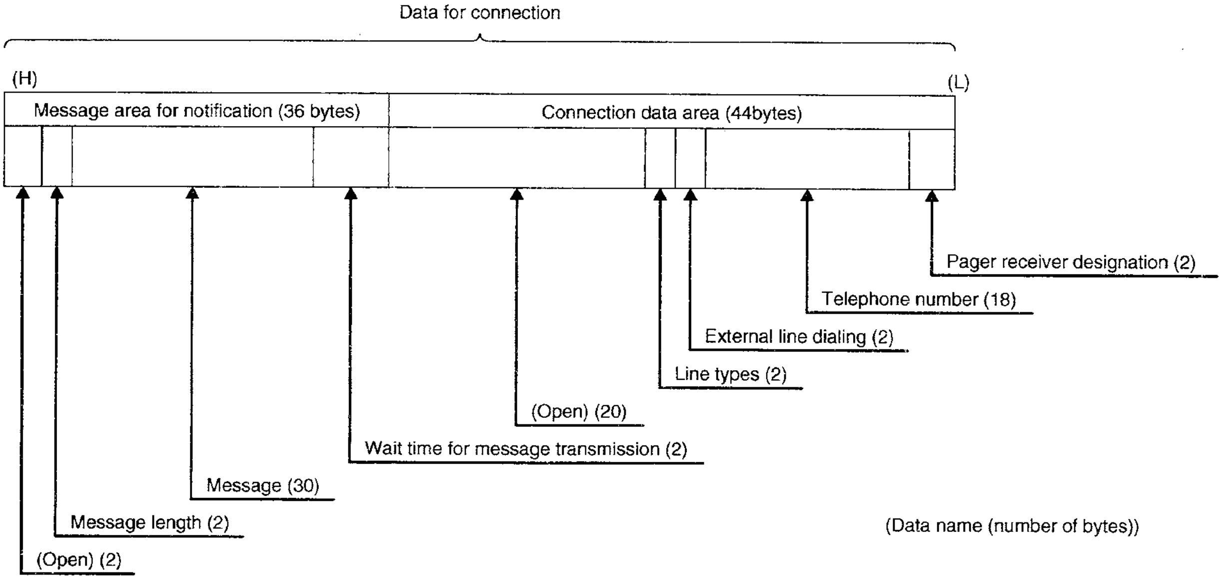
Address		**Name**	**Designated/stored value**	**Designation necessary (○)/unnecessary (×)**		
Hexadecimal	**Decimal**			**Registration**	**Reading**	**Deletion**
2H	2	Registration/reading/ deletion designation	0 : No request 2 : Read request 1 : Registration request 3 : Delete request	○		
3H	3	Frame number designation	0 : No frame number instructed 3000 to 3029 : Registration number of the target data for connection	○		
4H	4	Registration/reading/ deletion result storage (*1)	0 : Normal completion Other than 0 : Abnormal completion	× (Stored)		
5H	5	Number of registration data bytes designation	80 : Number of registration data bytes	○	× (Stored)	×
6H to 2DH	6 to 45	Data for connection	Messages for notification to be registered/ read, data for connection			

*1 When an abnormal completion occurs, the error code is stored. Perform corrective actions and verification of the error content according to Section 22.1.

③ The data structure in the data for connection area in the buffer memory that is used for the registration, reading and deletion process of the data for connection is shown below, as well as designated values and stored values.

For other than data for connection area, see Chapter 16.

(Read the table by replacing the user registration frame with data for connection.)



(Data for connection area) ··· 44 bytes

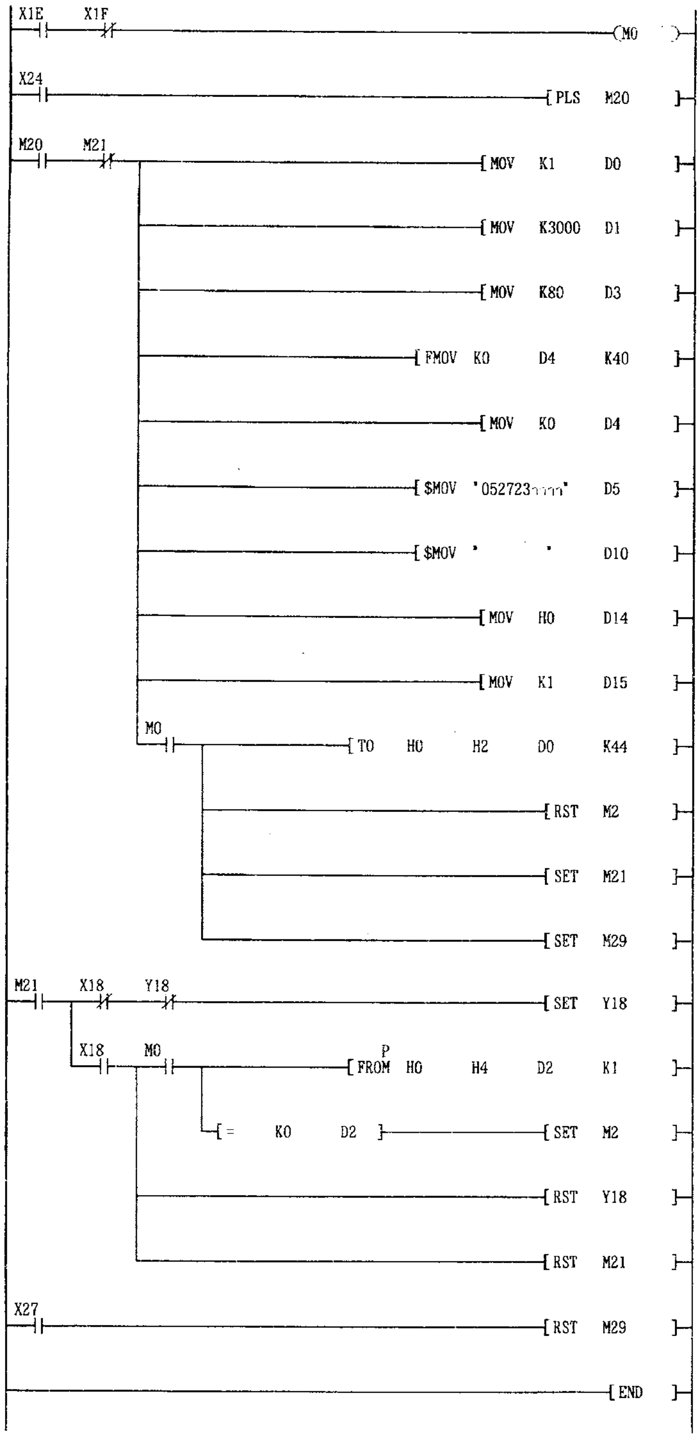
Data name	Designated/stored value and contents	Number of bytes	Data type
Pager receiver designation	Whether or not notification is performed, and the notification target module are designated. 0 : No notification 1 : Notification performed, target device = NTT DoCoMo 2 : Notification performed, target device = Tele-Message 3 : Notification performed, target device = Other than above * In the case of 3 above, the wait time for message transmission in the notification message must be designated.	2	Binary
Telephone number	• The other party's phone number used to establish line connection when communicating data or performing notification is designated. (Any phone number, even non-NTT numbers can be used) • When phone number is less than 18 characters, a space (code: 20H) must be entered for the remainder.	18	ASCII
External line dialling number	The external-line access number required when performing data communication/notification to the partner device is designated here. 0 to 9, 10(*), 11(#) : External-line access number on the QC24N side 255 : No external-line access number required on the QC24N side	2	Binary
Line type	The line type used to perform data communication/notification with the partner device is designated. 0 : Pulse 1 : Tone 2 : ISDN	2	Binary
(Open)	Designate "0."	20	Binary

(Notifying message area) ··· 36 bytes (Designated when performing notification)

Data name	Designated/stored value and contents	Number of bytes	Data type
Wait time for message transmission	The wait time after line connection until message transmission is designated. (Unit: seconds) 0 to 255 : Wait time * Valid when the pager receiver type designation is "3."	2	Binary
Message	Designate the notification message according to the display specification on the other party's device.	30	Binary
Message length	The number of designated message bytes shown above is designated. 0 : No message designation 1 to 30 : Number of message bytes	2	Binary
(Open)	Designate "0."	2	Binary

④ An example of a sequence program used for data for connection registration/reading/ deletion is shown below.

- Example of registration of data for connection



X1E: QC24N ready signal

X1F: WDT error signal

Convert the registration command into pulse

Set the registration request

Set the data-for-connection registration number

Set the number of registration data bytes

Clear the data storage device for connection

Set the pager receiver designation
(Notification is not executed)

Set the telephone number

Set the space to the remainder of the telephone number designation area

Set the external-line dialing number (0)

Set the line type (tone)

Buffer memory write

Write request signal is turned ON

Read the execution result

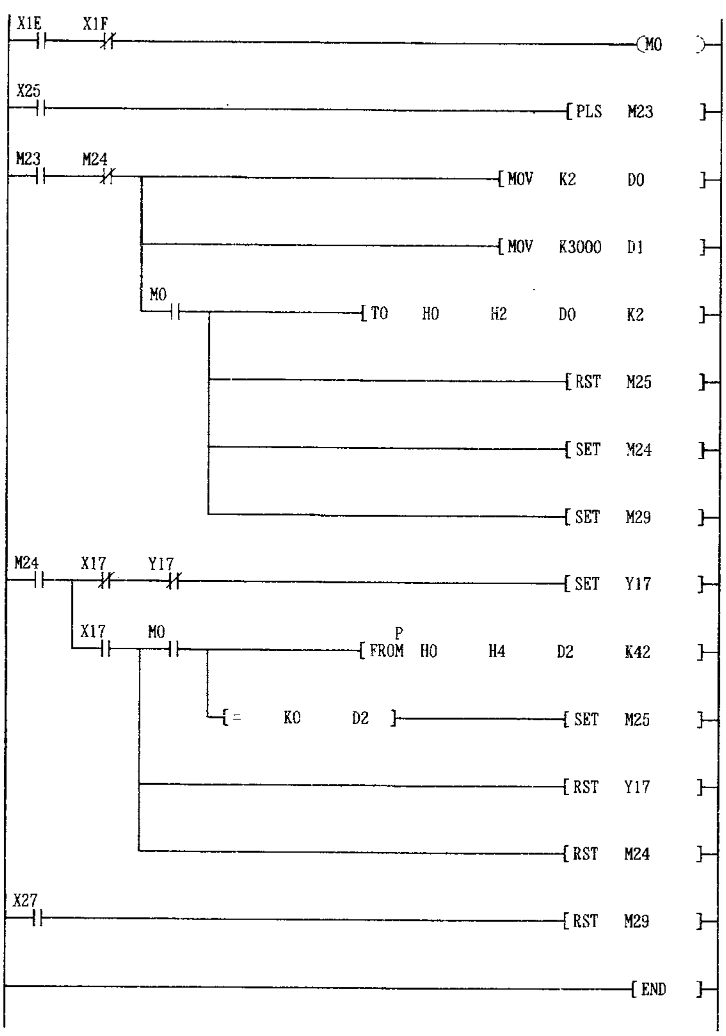
When the normal completion, the complete flag is turned ON

When the write complete flag ON, the request signal is turned OFF

When the clear command of the flag, the write flag is turned OFF

* For a image diagram of registration, see the read example diagram.

- Example of reading data for connection



X1E: QC24N ready signal

X1F: WDT error signal

Convert the read command into pulse

Set the read request

Set the data for connection registration number

Buffer memory write

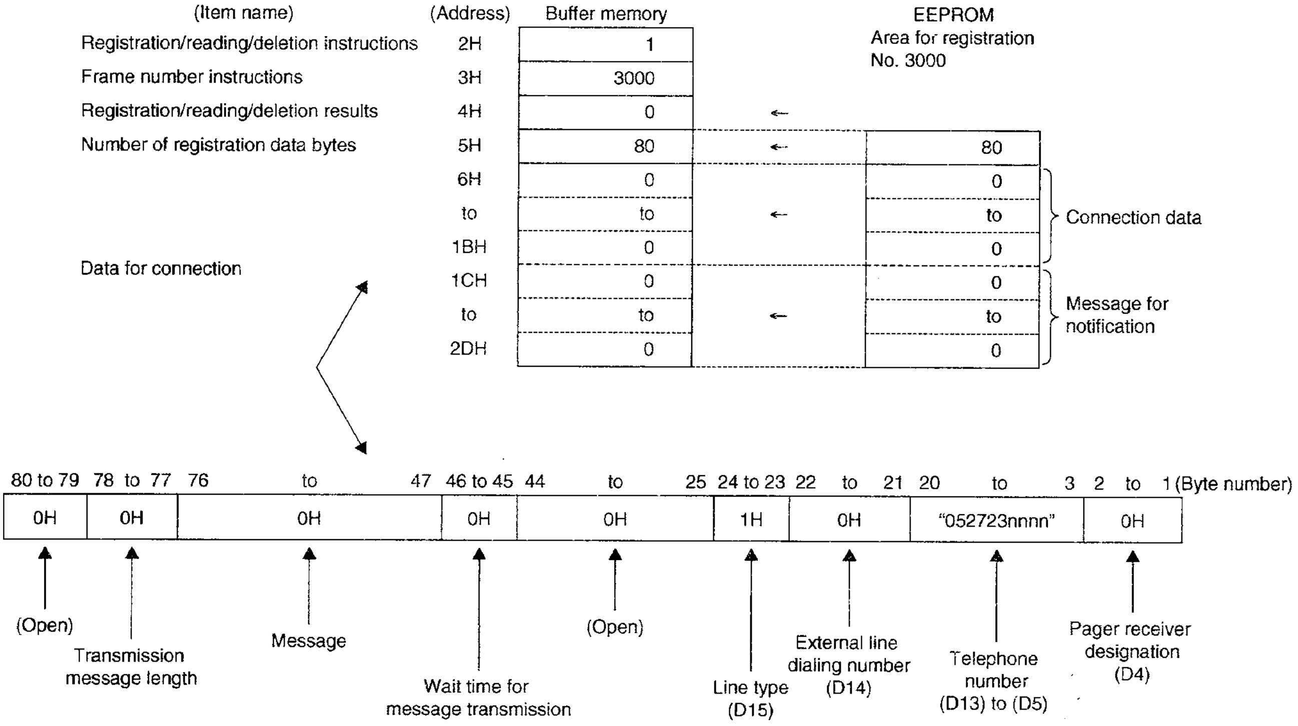
Read request signal is turned ON

Read the execution result

When the normal completion, the complete flag is turned ON

When the read complete flag ON, the request signal is turned OFF

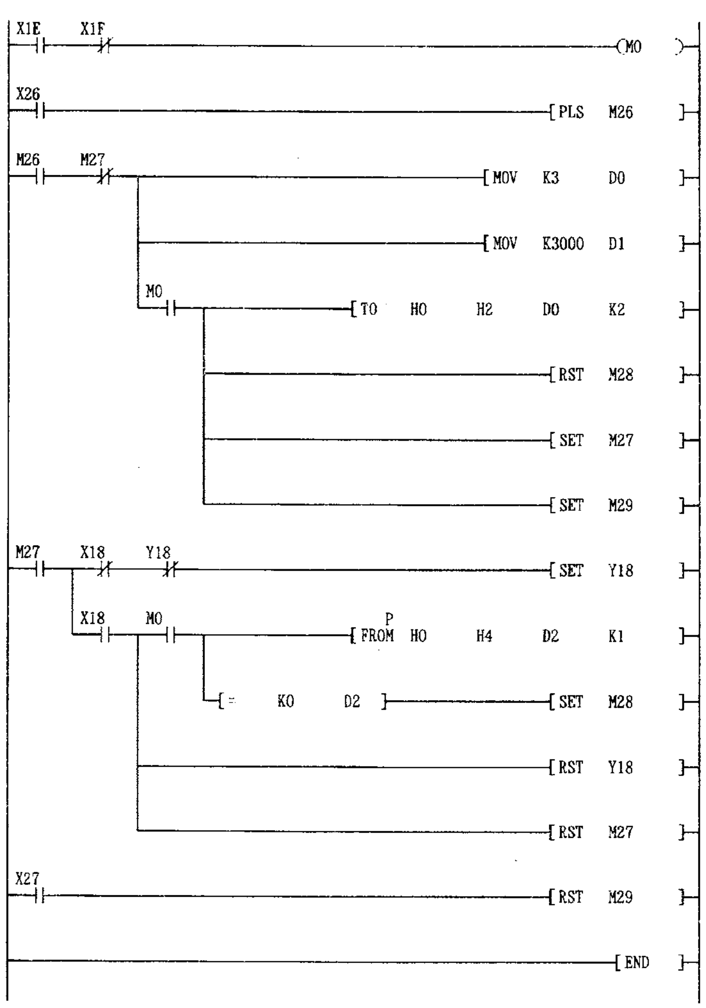
When the clear command of the flag, the write flag is turned OFF



(Item name)	(Address)	Buffer memory		EEPROM Area for registration No. 3000	
Registration/reading/deletion instructions	2H	1			
Frame number instructions	3H	3000			
Registration/reading/deletion results	4H	0	←		
Number of registration data bytes	5H	80	←	80	
Data for connection	6H	0		0	Connection data
	to	to	←	to	
	1BH	0		0	
	1CH	0		0	Message for notification
	to	to	←	to	
	2DH	0		0	

80 to 79	78 to 77	76 to 47	46 to 45	44 to 25	24 to 23	22 to 21	20 to 3	2 to 1 (Byte number)
0H	0H	0H	0H	0H	1H	0H	"052723nnnn"	0H
(Open)	Transmission message length	Message	Wait time for message transmission	(Open)	Line type (D15)	External line dialing number (D14)	Telephone number (D13) to (D5)	Pager receiver designation (D4)

- Example of deletion data for connection



X1E: QC24N ready signal
X1F: WDT error signal

Convert deletion command into pulse

Set the delete request

Set the data for connection registration number

Buffer memory write

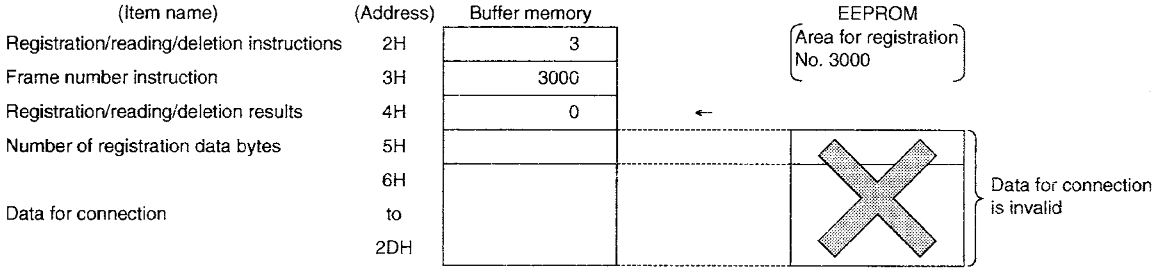
Write request signal is turned ON

Read the execution result

When the normal completion, the complete flag is turned ON

When the write complete signal ON, the request signal is turned OFF

When the clear command of the flag, the write flag is turned OFF



(b) In the case of the buffer memory of the QC24N

① The data for connection write (registration)/read is performed by designating a corresponding area that is compatible with registration number 8001H to 801FH in respect to the area for user registration frame registration (address : 1B00 to 1FF6H).

When deleting the data for connection, write "0" to the number of registration data bytes designation area.

② An overview of the buffer memory used in the writing, reading and deleting process of the data for connection as well as the designated value for each area are shown in the table below.

For details, see Chapter 16.

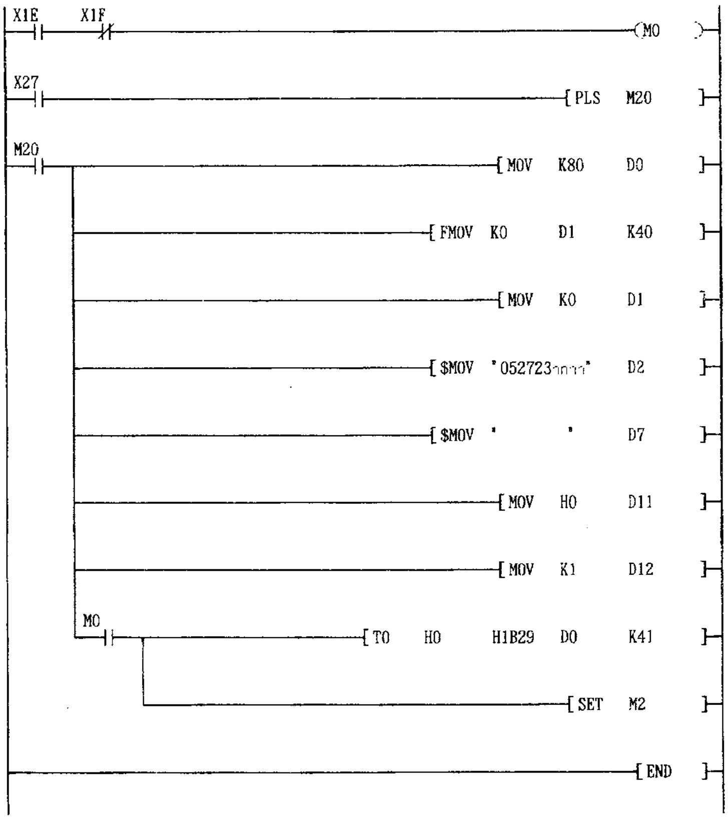
(Read the table by replacing the user registration frame with data for connection.)

Address		Name		Designated/stored value	Designation necessary (○)/unnecessary (×)		
Hexadecimal	Decimal				Write	Read	Deletion
1B00H	6912	Registration number 8001H	Number of registration data bytes designation	0 : When deleting 80 : Number of registration data bytes	○	Read processing unnecessary	○
1B01H to 1B28H	6913 to 6952		Data for connection	Notification message for the data for connection to be registered, connection data	○		×
1B29H	6953	Registration number 8002H	Number of registration data bytes designation	0 : When deleting 80 : Number of registration data bytes	○	Read processing unnecessary	○
1B2AH to 1B51H	6954 to 6993		Data for connection	Notification message for the data for connection to be registered, connection data	○		×
1FCEH	8142	Registration number 801FH	Number of registration data bytes designation	0 : When deleting 80 : Number of registration data bytes	○	Read processing unnecessary	○
1FCFH to 1FF6H	8143 to 8182		Data for connection	Notification message for the data for connection to be registered, connection data	○		×

③ The contents of the data to be written into the designated area that is compatible with registration number 8001H to 801FH is the same as the situation in respect to the EEPROM.

④ An example of a sequence program used for writing (registering) of data for connection is shown below.

- Example of writing data for connection to the registration number 8002H area



X1E: QC24N ready signal
X1F: WDT error signal

Convert the registration command into pulse

Set the number of registration data bytes

Clear the data storage device for connection

Set the pager receiver designation
(Notification is not executed)

Set the telephone number

Set the space to the remainder of the telephone number designation area

Set the external line dialing number (0)

Set the line type (tone)

Buffer memory write

(Item name)		Data register		(Address)	Buffer memory Area for registration No. 8002H
Number of registration data bytes	D0	80	→	1B29H	80
Data for connection	D1 to D22	(Connection data)	→	1B2AH to 1B3FH	(Connection data)
	D23 to D40	(Data for notification)	→	1B40H to 1B51H	(Data for notification)

21.4.7 Initialization of modem/terminal adapter

The initialization of the modem/TA connected to the QC24N, used for communicating data and performing notifications to pager receivers using the QC24N modem function, will be discussed.

1 Requirements for initialization

Perform the following setting and registration:

① The QC24N initial settings as shown in Section 21.4.4

② The data for initialization registration shown in Section 21.4.5, when initializing the modem/TA with the data for initialization set by the user.

Remark

It is possible to initialize and connect by performing the connection process by designating the data for initialization and data for connection . (See Section 21.4.8.)

2 Buffer memory used in initialization

This is determined by the number of data for initialization to be used among the data for initialization registered in the EEPROM or the buffer memory of QC24N.
The designated values for the buffer memory are shown below:

	Used buffer memory				The number of data for initialization used and buffer memory designated value	
	Name		Address (CH1/CH2)			
			Hexadecimal	Decimal	When number used = 1	When number used = 2 or more
1	Data number for initialization designation		34H	52	7D0H to 801FH : Data for initialization registration number (*1)	0H
2	Transmission-in-progress user registration frame number		B6H/156H	182/338	(Unused)	(During initialization, the data registration number currently being sent is stored.
3	CR/LF output designation		B7H/157H	183/339		0 (default value)
4	Output head pointer designation		B8H/158H	184/340		1 to 100 (See ①)
5	Number of outputs designation		B9H/159H	185/341		1 to 100 (See ②)
6	Output frame number designation	First	BAH/15AH	186/342		7D0H to 801FH : Data for initialization registration number (*1)
		Second	BBH/15BH	187/343		
		to	to	to		
		Hundredth	11DH/1BDH	285/445		

*1 The data for initialization registration number to be used is designated.

7D0H to 7D4H (2000 to 2004) : Data registered by the OS
9C4H to 9E1H (2500 to 2529) : Data registered in the EEPROM by the user
8001H to 801FH (-32767 to -32737): Data registered in the buffer memory by the user

① Output head pointer designation area (address: B8H/158H)

Designate the location of the head position (n-th unit) in the output frame number designation area to which the registration number of the data for initialization to be sent is written.

1 : Transmitted form the first unit
to
100 : Transmitted from the 100th unit

② Number of outputs designation area (address: B9H/159H)

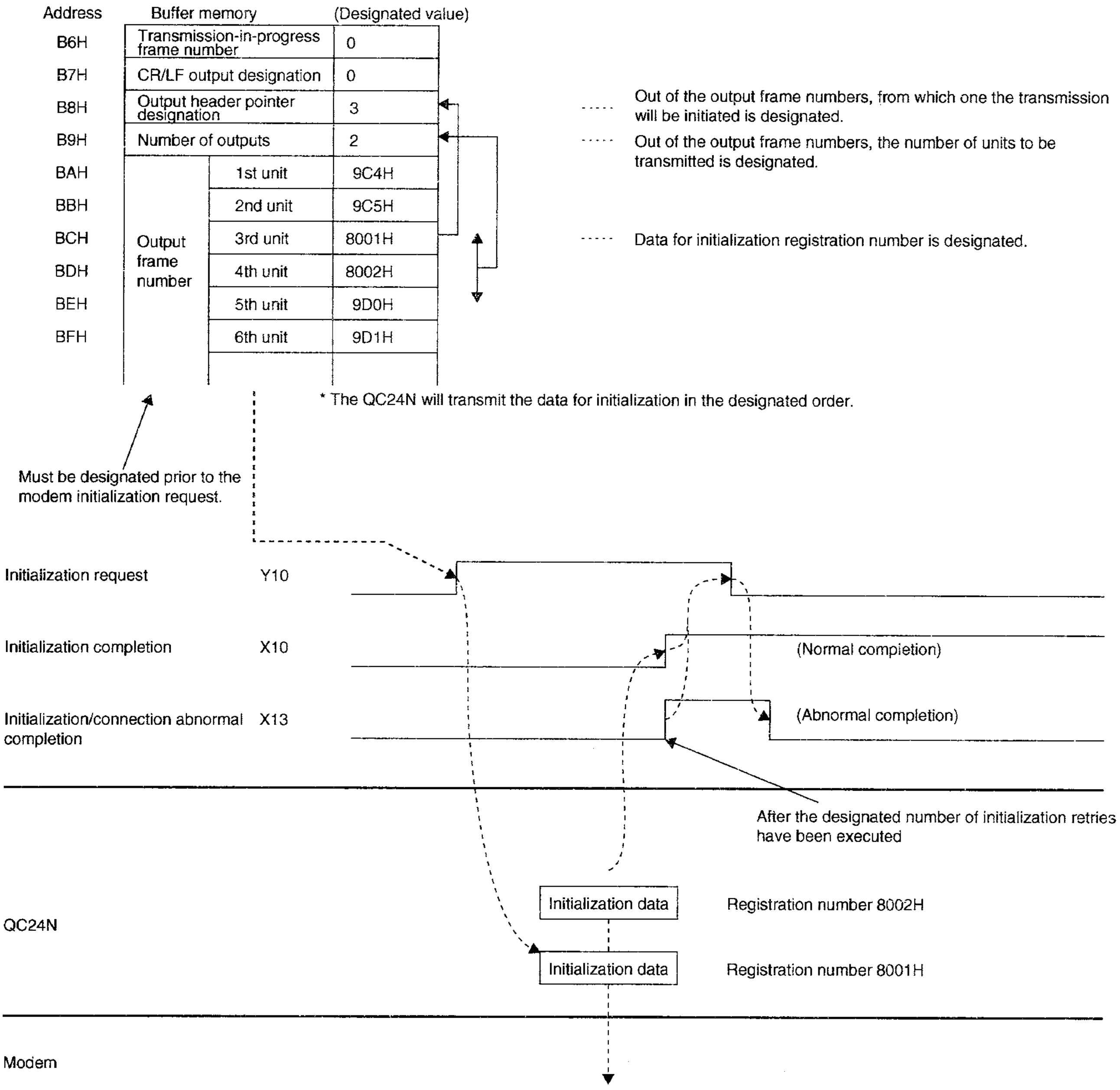
The number of data for initialization units to be transmitted starting from the location set by the output head pointer designation area is designated here.

1 : 1 data will be transmitted
to
100 : 100 data will be transmitted

3 I/O signals used in initialization

The initialization request signal (Y10), initialization complete signal (X10) and initialization/connection abnormal complete signal (X13) are used.

(Example) When initializing the modem connected to CH1 of the QC24N using two set of data for initialization (registration numbers 8001H and 8002H) that are registered in the buffer memory



Address	Buffer memory		(Designated value)
B6H	Transmission-in-progress frame number		0
B7H	CR/LF output designation		0
B8H	Output header pointer designation		3
B9H	Number of outputs		2
BAH	Output frame number	1st unit	9C4H
BBH		2nd unit	9C5H
BCH		3rd unit	8001H
BDH		4th unit	8002H
BEH		5th unit	9D0H
BFH		6th unit	9D1H

..... Out of the output frame numbers, from which one the transmission will be initiated is designated.

..... Out of the output frame numbers, the number of units to be transmitted is designated.

..... Data for initialization registration number is designated.

* The QC24N will transmit the data for initialization in the designated order.

Must be designated prior to the modem initialization request.

4 Precautions during modem/TA initialization

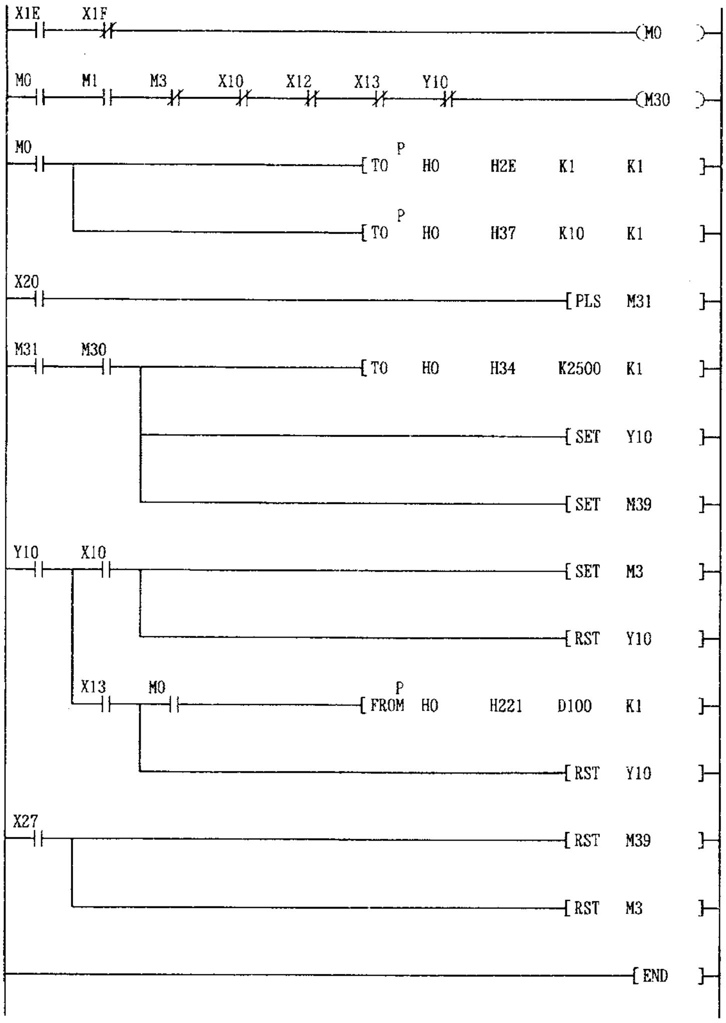
After the initialization for the QC24N-side modem/TA has been completed by the PLC CPU, the QC24N monitors the status of the modem/TA as long as the initialization complete signal (X10) is ON.

If the line to the modem/TA is disconnected during the initialization complete signal (X10) is ON, the QC24N will automatically start the initialization process of the modem/TA when the line is restored regardless of the ON/OFF setting of the initialization request signal Y(n+1)0.

5 Modem/TA initialization program example

An example of the modem/TA initialization program by the PLC CPU is shown below.

- Example of using one data for initialization



X12: Connection in progress signal
X1E: QC24N ready signal
X1F: WDT error signal
M0: QC24N inaccessible flag
M1: Data registration complete flag for initialization
See Section 21.4.5
M30:Initialization enabled flag

Initial settings of the QC24N
See Section 21.4.4
- Set the modem connection channel on the QC24N
- Set the no-communication interval time (10 minutes)

Convert the modem initialization command into pulse

Modem/TA initialization
- Designate the data number for initialization
- Initialization request signal is turned ON

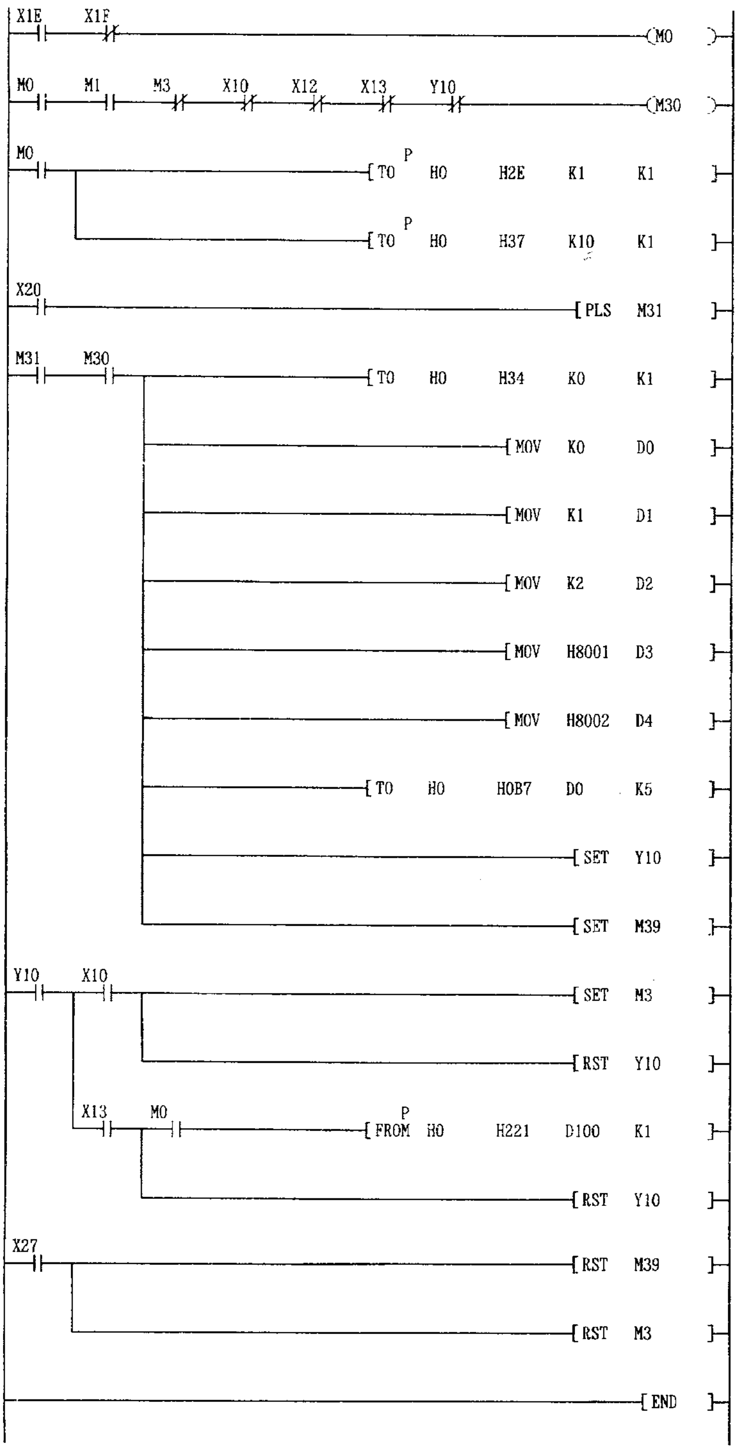
- When the initialization complete signal ON, the initialization complete flag is turned ON and request signal is turned OFF

- When the abnormal complete signal ON, the error code is read and request signal is turned OFF

When the clear command of the flag, the initialization request and the complete flag are turned OFF

- Example of using two data for initialization

X12: Connection in progress signal
X1E: QC24N ready signal
X1F: WDT error signal
M0: QC24N inaccessible flag
M1: Data registration complete flag for initialization
See Section 21.4.5
M30: Initialization enabled flag



Initial settings of the QC24N
See Section 21.4.4
- Set the modem connection channel on the QC24N
- Set the no-communication interval time (10 minutes)

Convert the initialization command into pulse

Modem/TA initialization
- Designate the data number for initialization
- Set the CR/LF output designation
- Set the output header pointer
- Set the number of outputs
- Set the data number for initialization (first unit) (second unit)
- Write to the user-registration frame for transmission designation area
- Initialization request signal is turned ON
- When the initialization complete signal ON, the initialization complete flag is turned ON and the request signal is turned OFF
- When the abnormal complete signal ON, the error code is read and the request signal is turned OFF

When the clear command of the flag, the initialization request and the complete flag are turned OFF

21.4.8 Line connection

This section explains the connection (dialing) with the partner devices for the purpose of data communication with external devices using the QC24N modem functions.

In case of notification to a pager receiver, the line is connected while the notification is being processed. The connection processing such as a connection request (Y11) to I/O signal is, therefore, unnecessary.

* The data for connection indicated in this section should be set to perform the notification processing.

1 Requirements for connection

Complete the following settings and registrations in advance.

① The initial settings for the QC24N as shown in Section 21.4.4

② The registration of the data for initialization as shown in Section 21.4.5

③ The registration of the data for connection as shown in Section 21.4.6

④ The initialization of the modem/TA connected to the QC24N side as shown in Section 21.4.7

In addition, both the initialization and line connection can be conducted simultaneously by designating the data for initialization and data for connection to perform connection processing.

For the data setting for initialization to perform initialization and line connection simultaneously, see Section 21.4.7. Explanation on the above-mentioned setting is omitted in this section.

2 Buffer memory used in line connection

The buffer memory is determined by whether the line is connected from the QC24N side or the partner device.

The buffer memory used and designated value are explained below.

① When initiating line connection from the QC24N

- Data number for connection designation area (address : 35H(53))

  The data for connection registration number is designated.

  BB8H to BD5H (3000 to 3029) : Data registered to the EEPROM by the user

  8001H to 801FH (-32767 to -32737) : Data registered to the buffer memory by the user

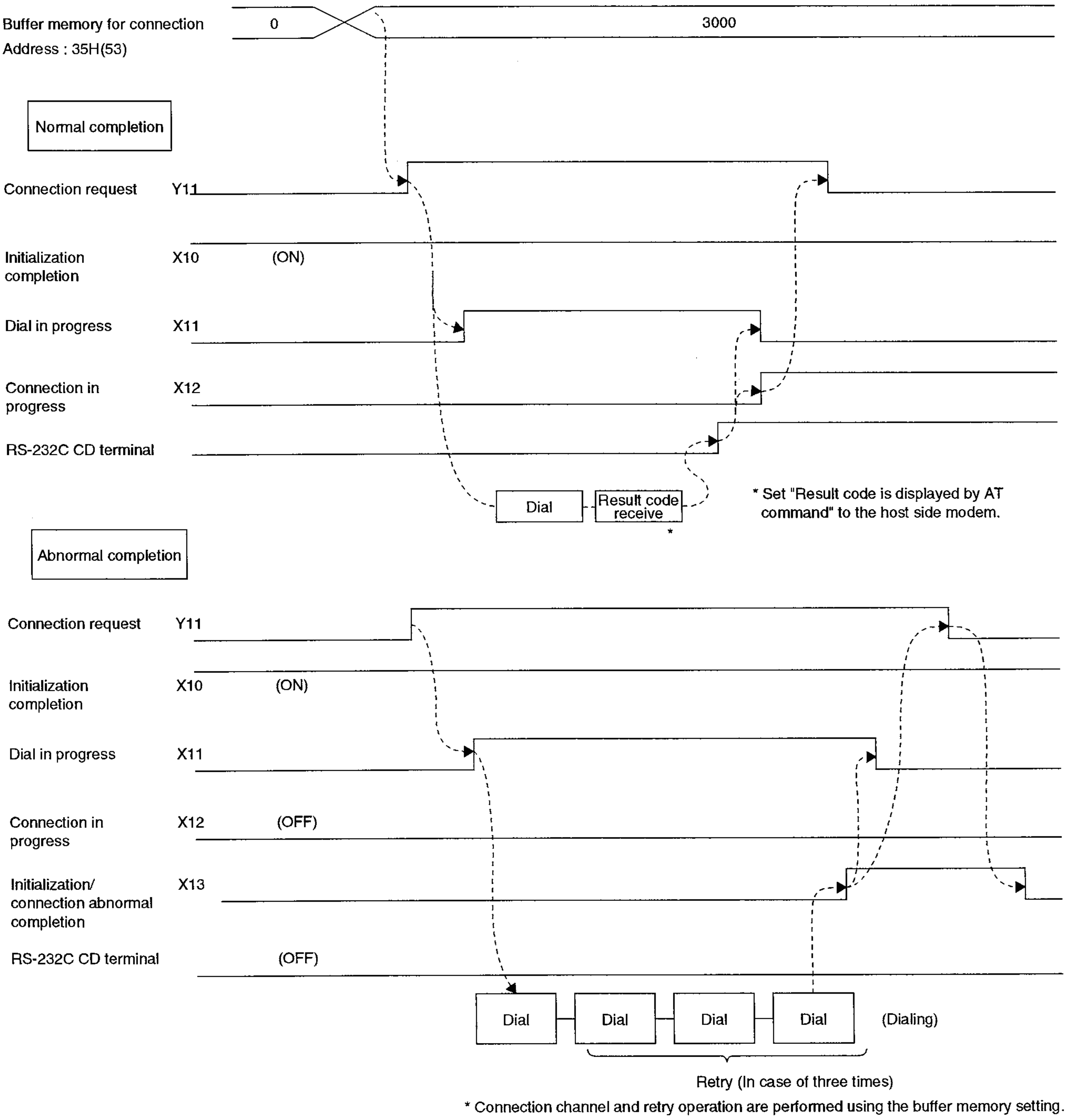
② When initiating line connection from the partner device

Since the line connection processing is not necessary on the QC24N side, the line connection buffer memory is not used.

3 I/O signals used in line connection

Connection request signal (Y11), dial in progress signal (X11), connection in progress signal (X12) and initialization/connection abnormal complete signal (X13) are used.

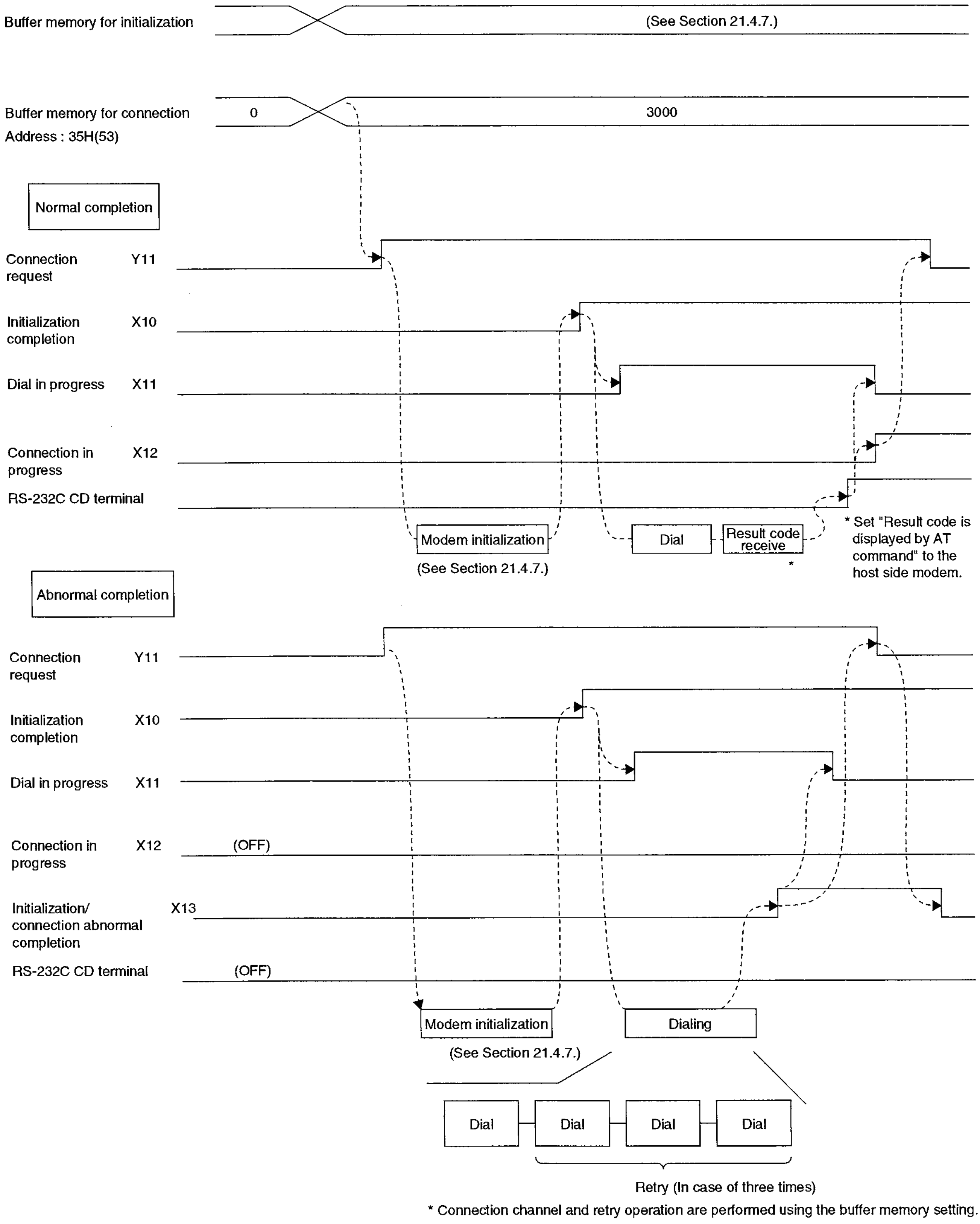
(Example 1) When performing the line connection from the QC24N side only following the completion of initialization



* Set "Result code is displayed by AT command" to the host side modem.

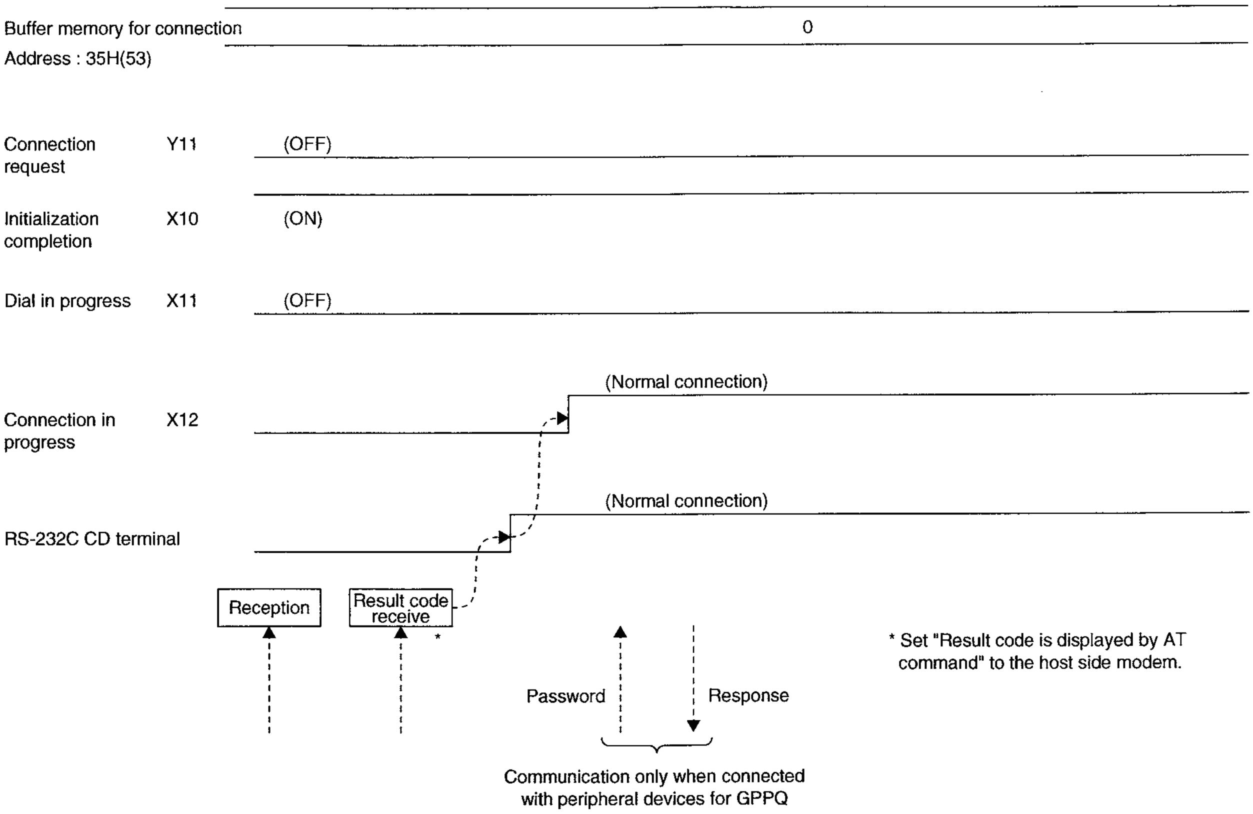
* Connection channel and retry operation are performed using the buffer memory setting.

(Example 2) When performing the initialization and the line connection from the QC24N side simultaneously



* Connection channel and retry operation are performed using the buffer memory setting.

(Example 3) When initiating the line connection from the partner device after the completion of initialization



* Set "Result code is displayed by AT command" to the host side modem.

POINT

(1) The connection channel on the QC24N side is set in the modem connection channel designation area (address : 2EH(46)) of the buffer memory.

(2) Abnormal processing when the partner device initiate the line connection is left entirely to the partner device.
There is no method on the QC24N side to check a line connection error occurrence at the partner device.

4 Precautions during the line connection

① During connection to the peripheral devices for GPPQ, the GPPQ side will consider the QnACPU station loaded with QC24N as the PLC CPU station loaded (or connected) with Q6TEL.

When the password for Q6TEL is set on the GPPQ side, the Q6TEL password (*1) is first transmitted from the peripheral device for GPPQ upon completion of connection. However, because QC24N does not control the Q6TEL password, it can not determine whether or not it received the correct password.

The QC24N then returns a corresponding response, enabling data read/write and status control for the PLC CPU thereafter.

*1 The password is entered on the peripheral device for GPPQ side using the keyboard, prior to access, with character strings for PLC access enabled/disabled through Q6TEL.

② Prior to data communication with external devices, determine when and which station will perform the line connection (dialing) and line disconnection processing to the partner device.

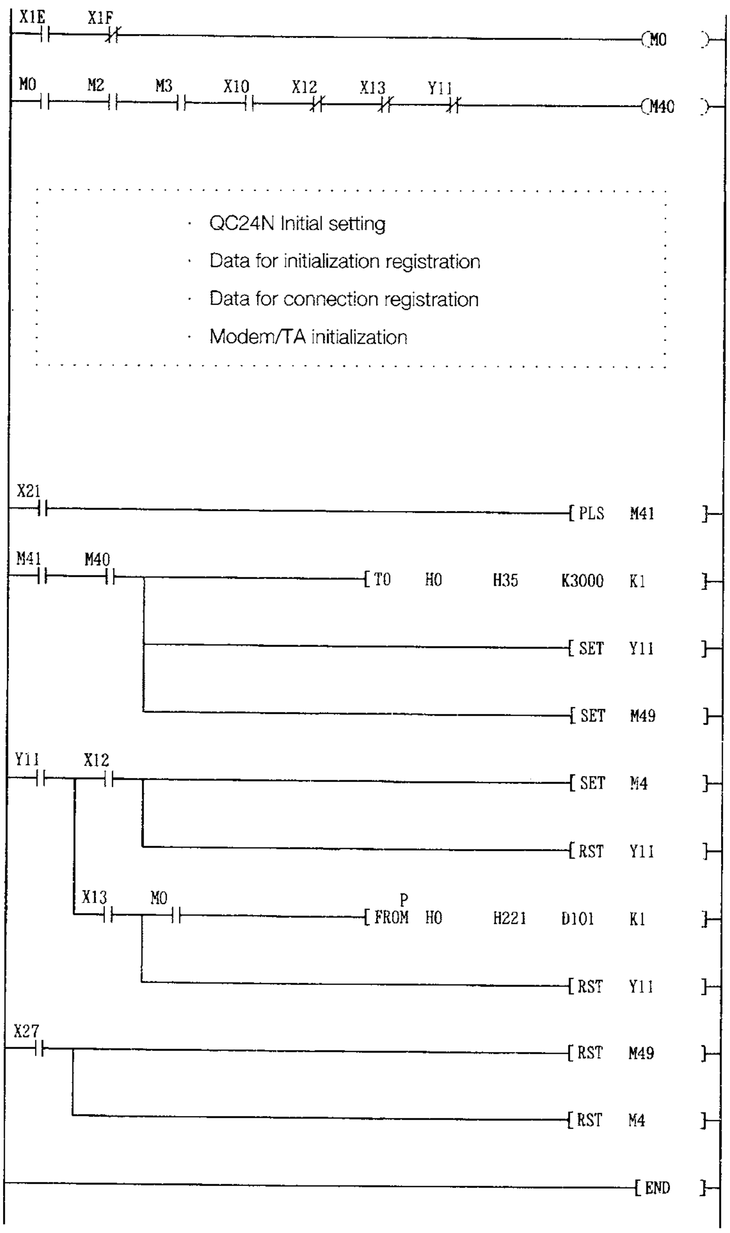
③ When reconnecting the line after disconnection, allow several seconds for the modem before turning on the Connection request (Y11). If it (Y11) is turned on immediately after line disconnection, the modem may not accept the first connection request, resulting in connection failure, and the user may be forced to wait for the retry time to elapse.

5 Line connection program example

An example of a line connection program is shown below.

- Example of initiating line connection from the QC24N side following the initialization completion

X10: Initialization complete signal
X1E: QC24N ready signal
X1F: WDT error signal
M0: QC24N accessible flag
M2: Data registration complete flag for connection
See Section 21.4.6
M3: Initialization complete flag
M40: Connectable flag



See Section 21.4.4.
See Section 21.4.5.
See Section 21.4.6.
See Section 21.4.7.

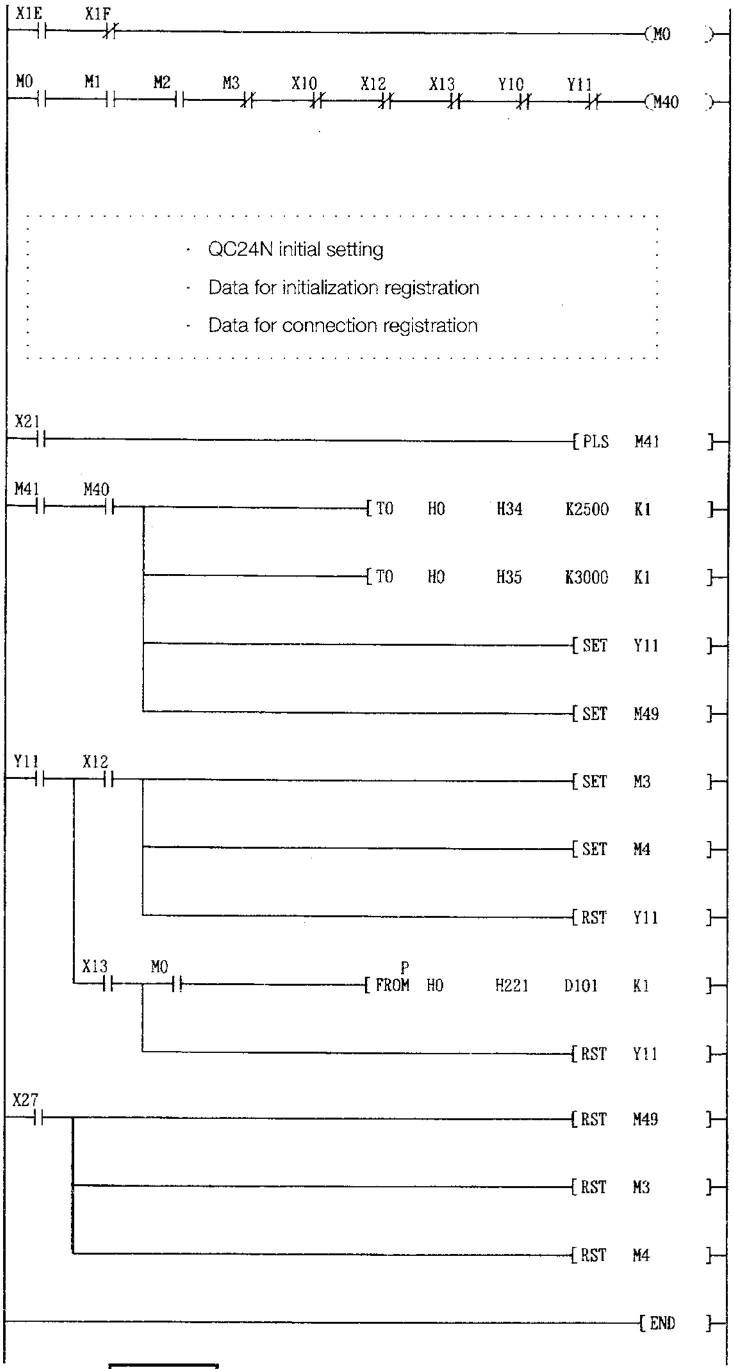
Convert the line connection command into pulse

Line connection
- Set the data number for connection
- Connection request signal is turned ON
- When the connection in progress signal ON (normal completion), the connection complete flag is turned ON and the request signal is turned OFF
- When the abnormal completion signal ON, the error code is read and the request signal is turned OFF

When the clear command of the flag, the connection request and the complete flag are turned OFF

- Example of simultaneous execution of initialization and line connection from the QC24N side

X10: Initialization complete signal
X12: Connection in progress signal
X1E: QC24N ready signal
X1F: WDT error signal
M0: QC24N accessible flag
M1: Data registration complete flag for initialization
M2: Data registration complete flag for connection
See Section 21.4.6
M3: Initialization complete flag
M40:Connectable flag



See Section 21.4.4.
See Section 21.4.5.
See Section 21.4.6.

Convert the line connection command into pulse

Initialization and line connection for modem/TA
- Set the data number for initialization
- Set the data number for connection
- Connection request signal is turned ON
- When the connection in progress signal ON (normal completion), the initialization complete flag and connection complete flag are turned ON and the request signal is turned OFF.
- When the abnormal complete signal ON, the error code is read and the request signal is turned OFF.

When the clear command of the flag, the connection request and the complete flag are turned OFF

Remark

When the line connection is initiated from the partner device, neither registration, setting nor connection processing is necessary.

As shown in example (3) of this section's 3 , data communication is possible if the connection in progress signal (X12) turns ON after the completion of QC24N modem/TA initialization.

For an example of the modem/TA program for initialization, see Section 21.4.7.

21.4.9 Data communication and notification

This section explains the cautions for data communication with the partner device using QC24N modem function and procedures for notification to pager receivers.

1 **Requirements for data communication and notification**

(a) When communicating data with external devices

Perform the appropriate processing up to line connection or modem/TA initialization, depending on whether or not the line connection is initiated from the QC24N side.

After line connection, data communication can be performed using a dedicated protocol/ non-procedure protocol/bidirectional protocol in full-duplex communication.

① When initiating the line connection from the QC24N side

Processing up to line connection as shown in Section 21.4.8

② When the line connection is initiated from the partner device

Processing up to the initialization of the modem/TA as shown in Section 21.4.7.

(b) When notifying to pager receivers

Perform processing up to the initialization of the modem/TA as shown in Section 21.4.7.

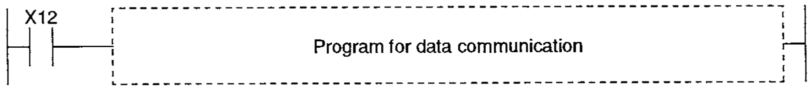
* In notification to pager receiver, since the line connection is performed during notification processing, line connection processing is unnecessary. However, be sure to register data for connection.

2 **Buffer memory used and I/O signals**

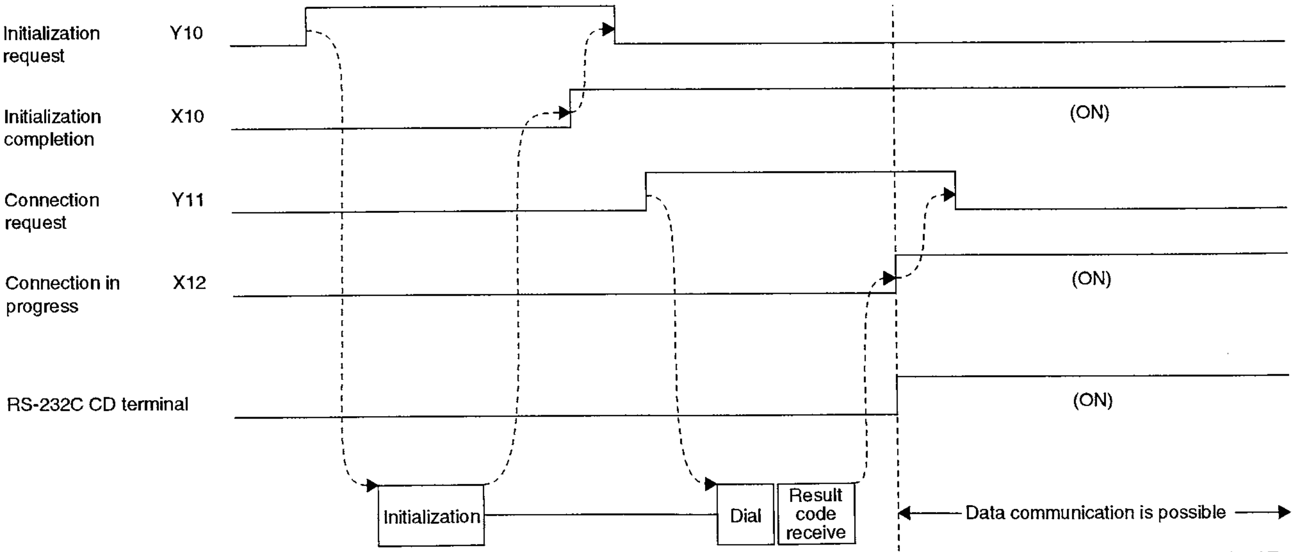
(a) When communicating data with the partner device

Only buffer memory and I/O signals the user uses for data communication (dedicated protocol/non-procedure protocol/bidirectional protocol).

Communicate data using the connection in progress signal (X12) ON as the interlock signal.



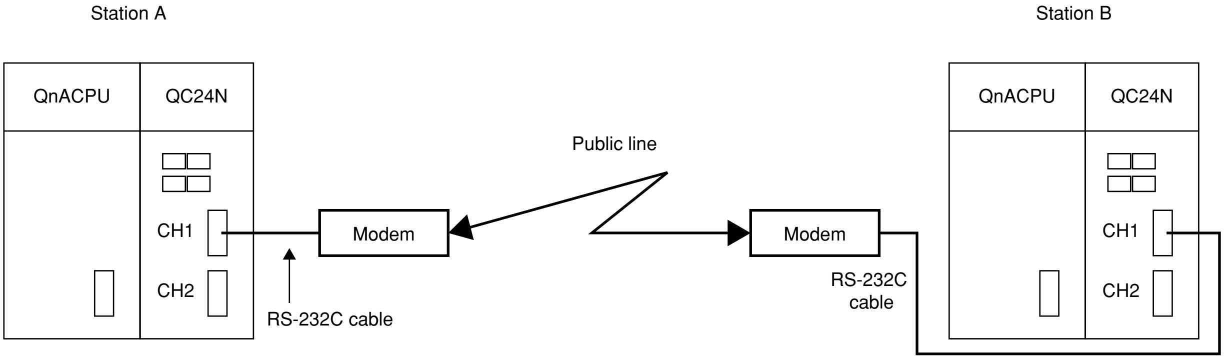
There is no I/O signal or buffer memory for modem functions used in data communication.



* Set "Result code is displayed by AT command" to the host side modem.

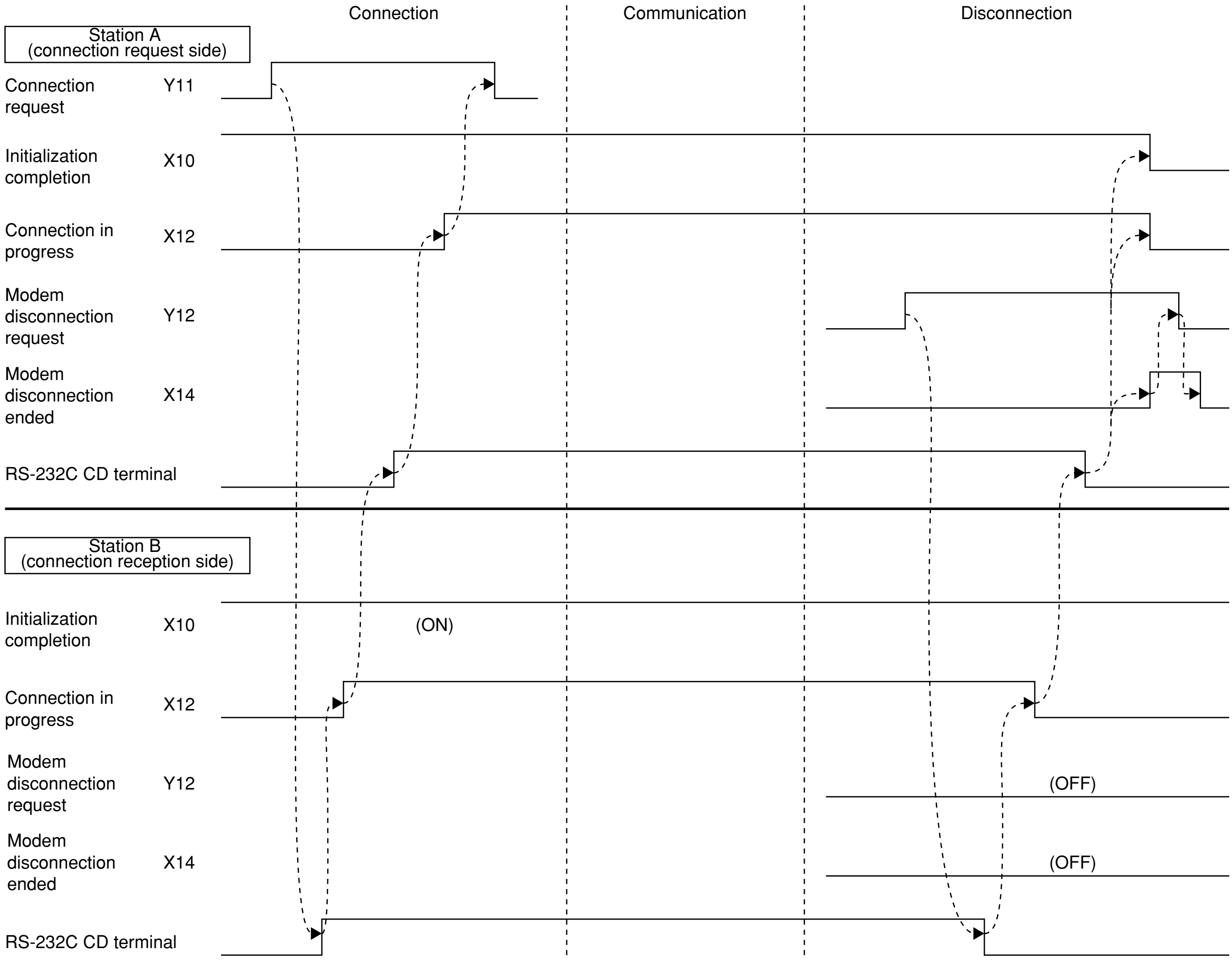
Remark

This section explains the general procedure for non-procedure protocol/bidirectional protocol (executed in full-duplex communication) data communication using the modem function between the PLC CPU with QC24N installed.



(General Procedure)

① Perform initial setting for QC24N at both station A and station B
② Perform modem/TA initialization in station B.
③ Perform modem/TA initialization and line connection in station B.
④ Communicate data using the non-procedure protocol/bidirectional protocol.
⑤ In order to end the communication, disconnect line from station A that initiated the line connection.



* It is possible to disconnect line from Station B, as well.

(b) When notifying to pager receiver

Use the data number designation area for connection.

① Buffer memory

Designate the data number designation area for connection (address : 35H(53)) to designate the following data for connection registration number.

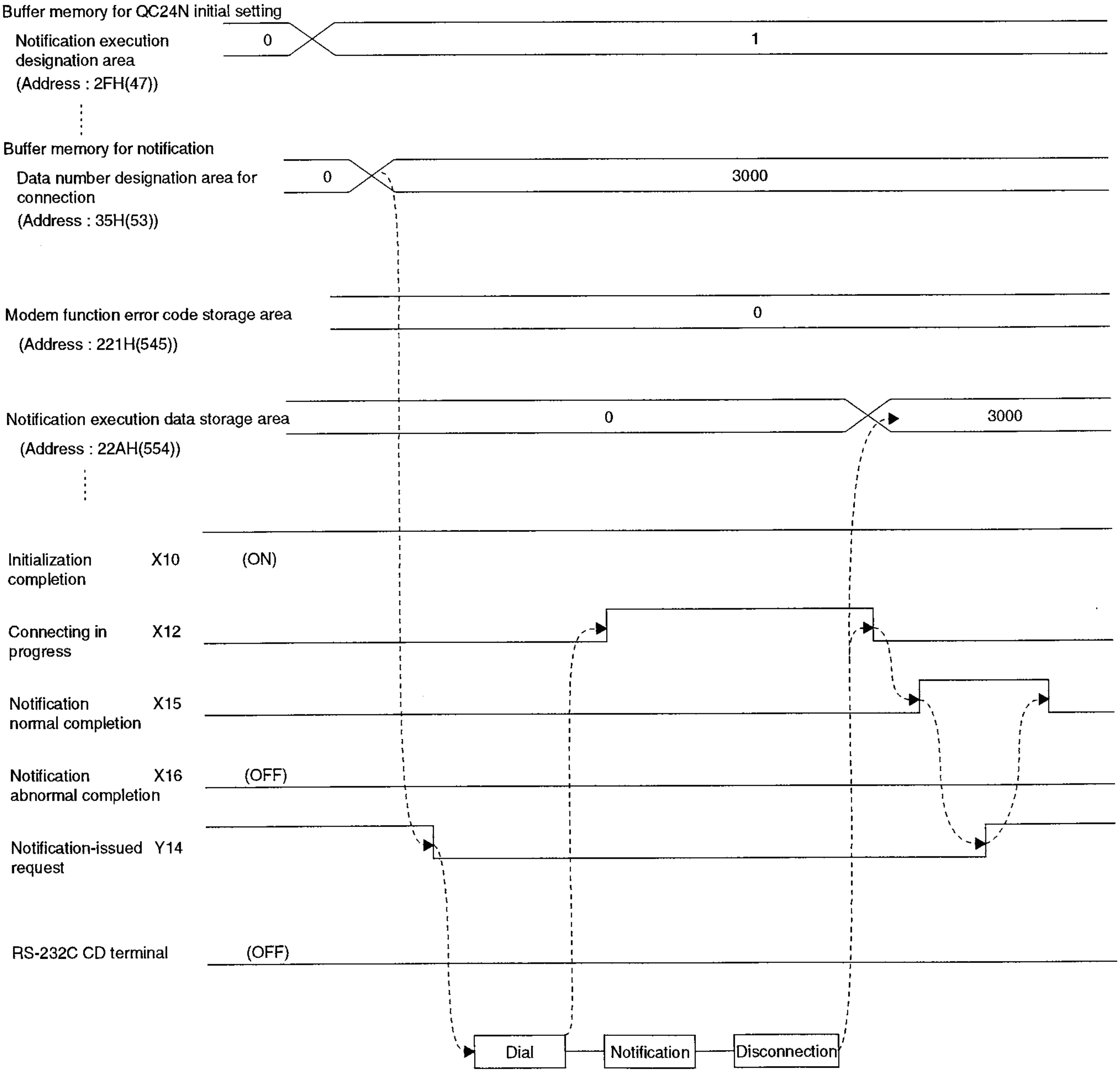
BB8H to BD5H (3000 to 3029) : Data registered to the EEPROM by the user

8001H to 801FH (-32767 to -32737) : Data registered to the buffer memory by the user

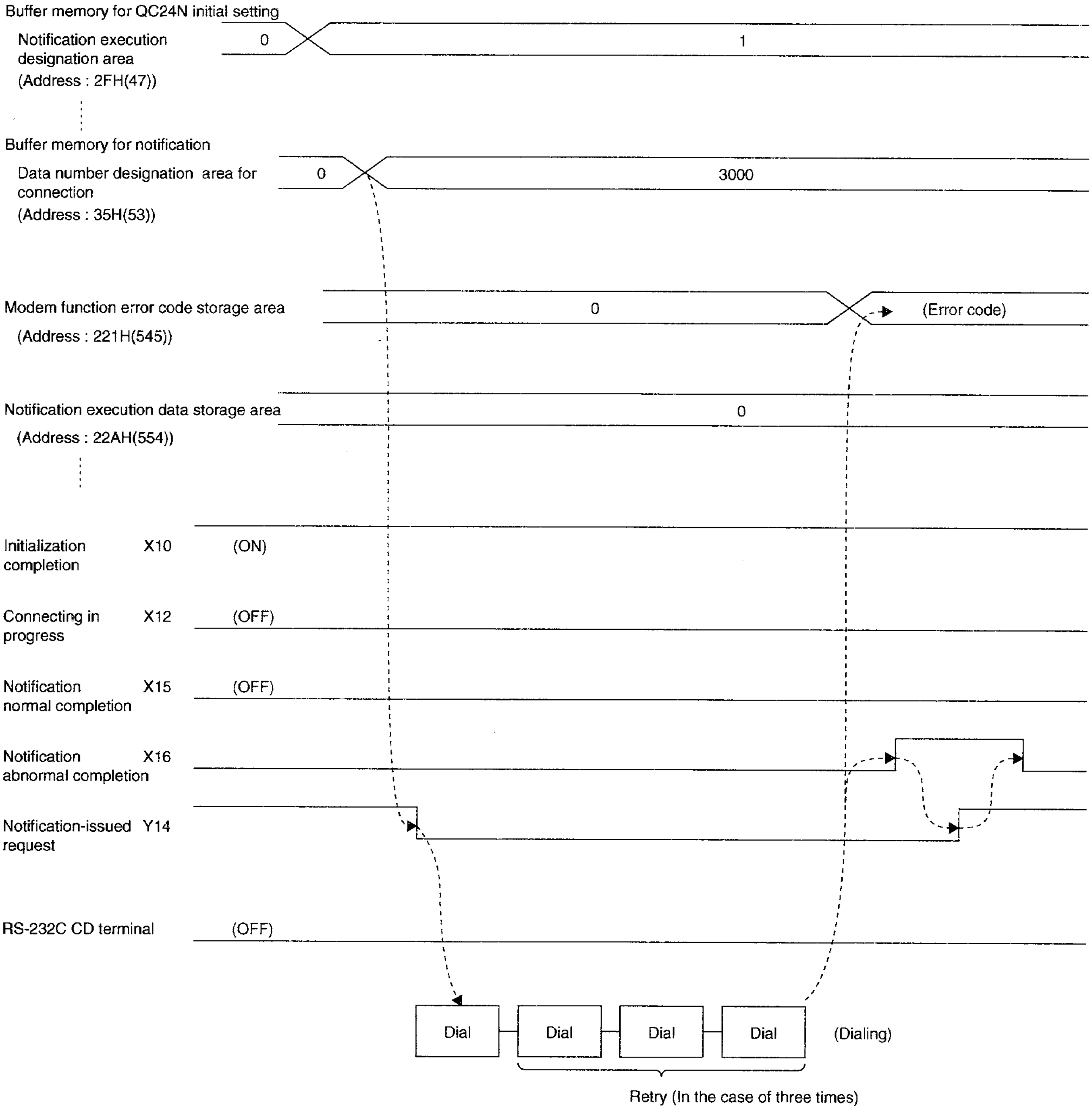
② I/O signal

Use notification-issued request signal (Y14), notification normal complete signal (X15), notification abnormal complete signal (X16).

(Example 1) When normal completion



(Example 2) When abnormal completion



* Retry processing is conducted according to the values for the connection retry number to initialization/connection time out (address : 30H to 32H) set in the buffer memory.

3 Precautions for performing data communication and notification

(a) When communicating data with the partner device

① When setting the no-communication interval time (set for address 37H) to infinite wait (set value=0) in the initial setting of QC24N, be sure to perform line disconnection after the completion of data communication.

② Only the no-procedure protocol/bidirectional protocol data communication can be performed in the PLC CPU with QC24N installed.

③ The QC24N automatically performs line disconnection processing if no data exchange is performed during the no-communication interval time (set for address 37H).

When the line is disconnected, the connecting (X12) signal and the initialization ended (X10) signal turn off, and the modem disconnection ended (X14) signal turns on.

(b) When notifying to pager receivers

① Turn on the notification-issued request signal (Y14) before the QC24N modem/TA initialization is completed.

② Notification processing is conducted when the notification-issued request signal (Y14) turns from ON to OFF after the completion of modem/TA initialization.

Therefore, notification processing is conducted when the PLC CPU of the station loaded with QC24N is in stop status, or the PLC CPU stops due to error, since the notification-issued request signal (Y14) is turned off in either case.

Write the data number for connection in the buffer memory (address : 35H) before the PLC CPU turns to a stop status.

③ When the notification-issued request signal (Y14) is turned OFF from ON before initialization of the QC24N modem/TA, the processing will end abnormally.

④ When the notification-issued request signal (Y14) is turned OFF from ON during initialization of the QC24N modem/TA, notification processing will be conducted after the completion of the modem/TA initialization.

⑤ Notification processing is completed in the order of line connection, message transmission, and line disconnection from QC24N for the transmission station of the radio wave to the notification destination.

Therefore, even if the power to the notification destination equipment is off, the notification processing will end normally as long as the above processing is completed.

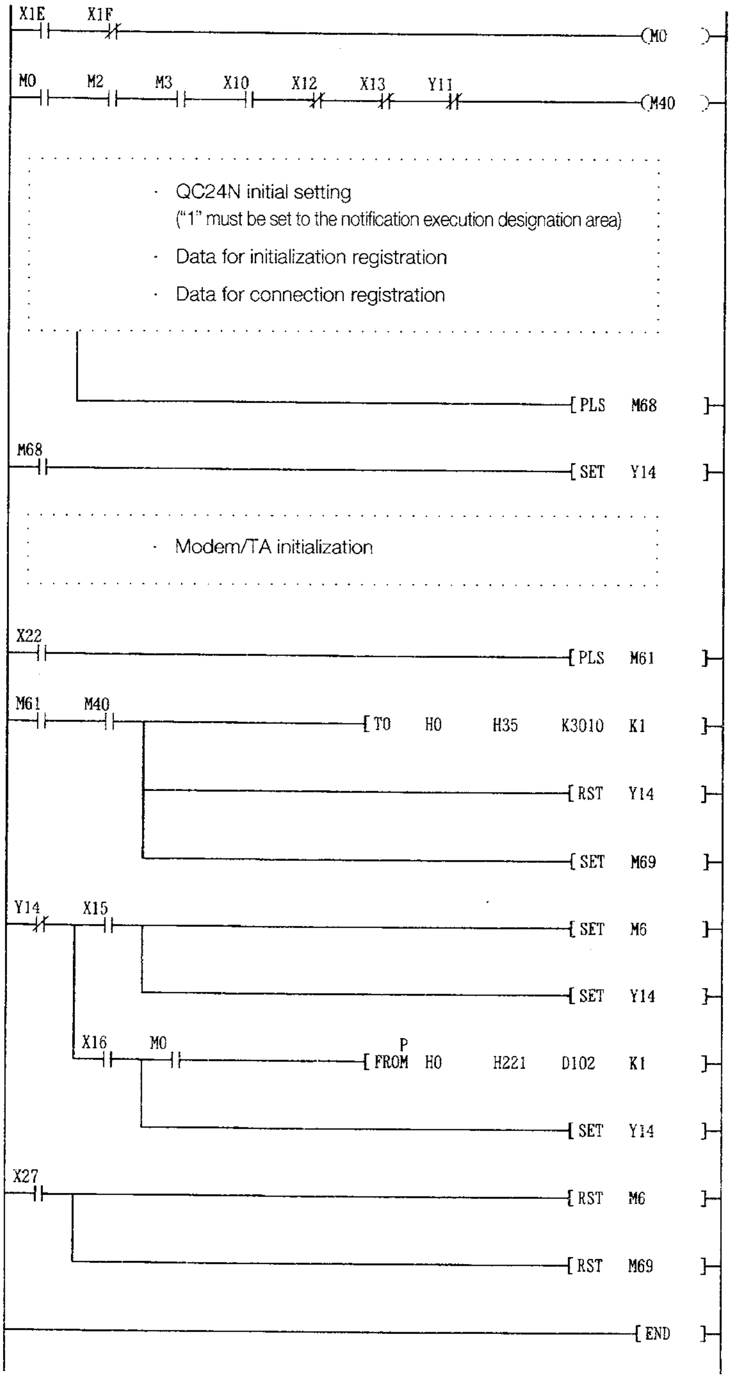
⑥ When the notification-issued request signal (Y14=ON) is turned ON before notification processing is complete, some messages may not be sent.

POINT

Turn on the notification-issued request signal (Y14) before the initialization processing of the QC24N modem/TA is completed, and turn it off after the initialization complete signal (X10) is turned ON.

4 Program for notification example

An example of program for notification is shown below.



X10: initialization complete signal

X12: Connection in progress signal

X1E: QC24N ready signal

X1F: WDT error signal

M0: QC24N accessible flag

M2: Data registration complete flag for connection

See Section 21.4.6

M3: Initialization complete flag

M40: Connectable flag

See Section 21.4.4.

See Section 21.4.5.

See Section 21.4.6.

Notification-issued request signal is turned ON (only 1 time)

See Section 21.4.7.

Convert the notification command into pulse

Notification processing

- Set the data number for connection (for notification)
- Notification-issued request signal is turned OFF

- When the notification normal complete signal ON, the notification complete flag is turned ON and the notification-issued request signal is turned ON
- When the notification abnormal complete signal ON, the error code is read and the notification-issued request signal is turned ON

When the clear command of the flag, the notification request and the complete flag are turned OFF

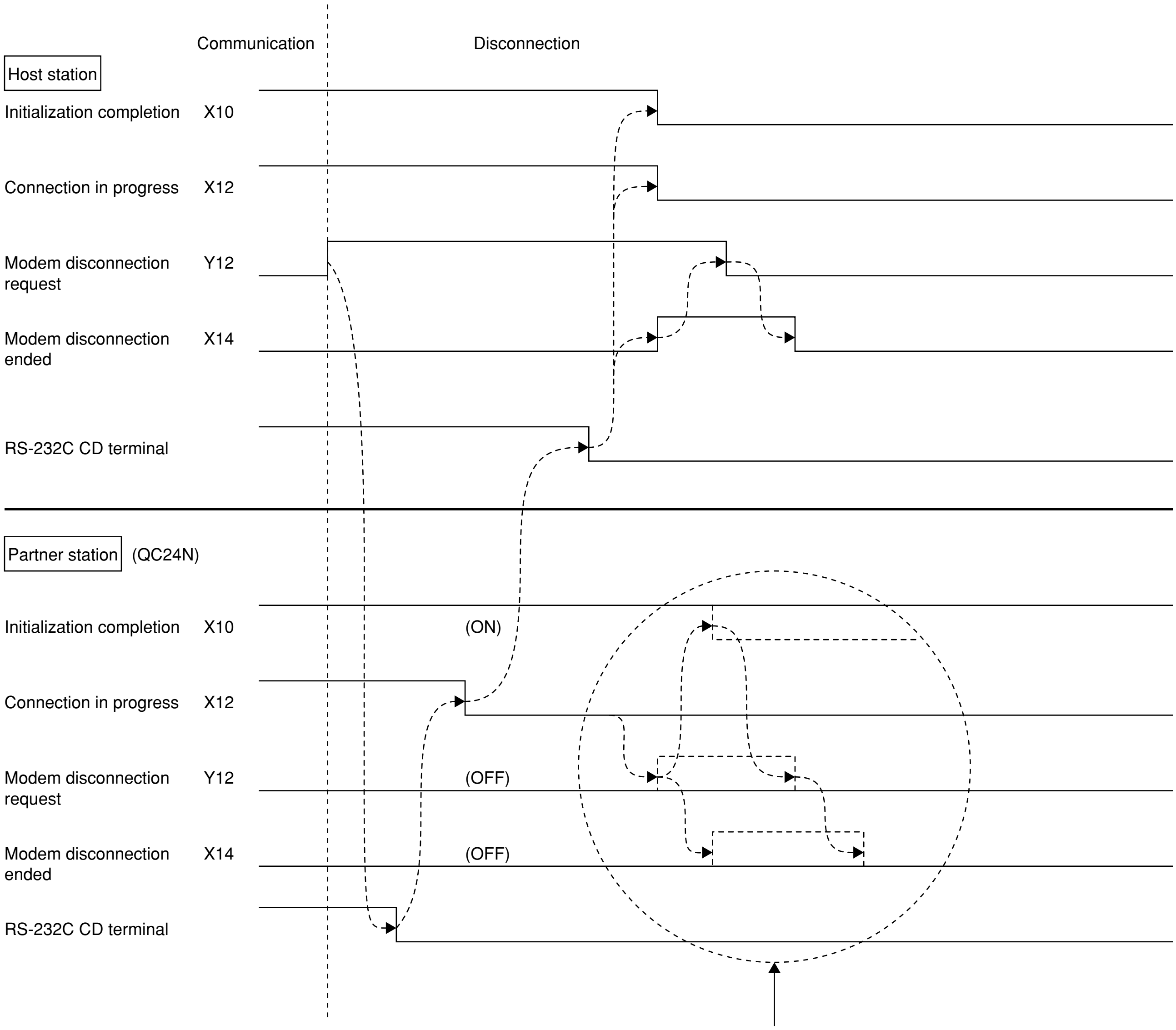
21.4.10 Line disconnection

This section explains the line disconnection upon communication completion when communicating data with the partner device using the QC24N modem functions.

In case of notification to pager receivers, since the line will be disconnected at the end of the notification processing, disconnection processing using an I/O signal, such as the modem disconnection request (Y12) signal is unnecessary.

1 I/O signal used

Uses the modem disconnection request (Y12) signal and modem disconnection complete signal (Y14).



This is the procedure to take in order to turn off the initialization complete signal (X10).
* In the case of QC24N, when the line is disconnected from the partner device, the initialization complete signal (X10) at the local station is not turned OFF.

POINT

(1) Line disconnection processing can be conducted from either device as long as the connection is in progress.

(2) The line disconnection processing disconnects the line connection with the partner device as well as the connection with the local station's QC24N modem.

(3) Even when an error occurs during the line disconnection, the disconnection processing will be forced.

(4) If data communication is to be resumed after line disconnection, either one of the following processing will be initiated depending on the initialization complete signal (X10).

① If the initialization complete signal is OFF
Start from the initialization of the modem/TA

② If the initialization complete signal is ON
Start from the line connection with the partner device

Remark

There is no buffer memory for line disconnection processing.

2 Precautions during the line disconnection

① Prior to data communication with external devices, determine when and which station will perform the line connection (dialing) and line disconnection processing to the partner device.

② If the line is disconnected during data transmission, transmission processing will be performed depending on the signal status of the local station's QC24N RS-232C interface.

③ If the line is disconnected during data reception, data reception will be disabled. This may cause an error occurrence such as a reception time out.

④ When data communications are not performed by the no-communication interval time, the QC24N disconnects the line.

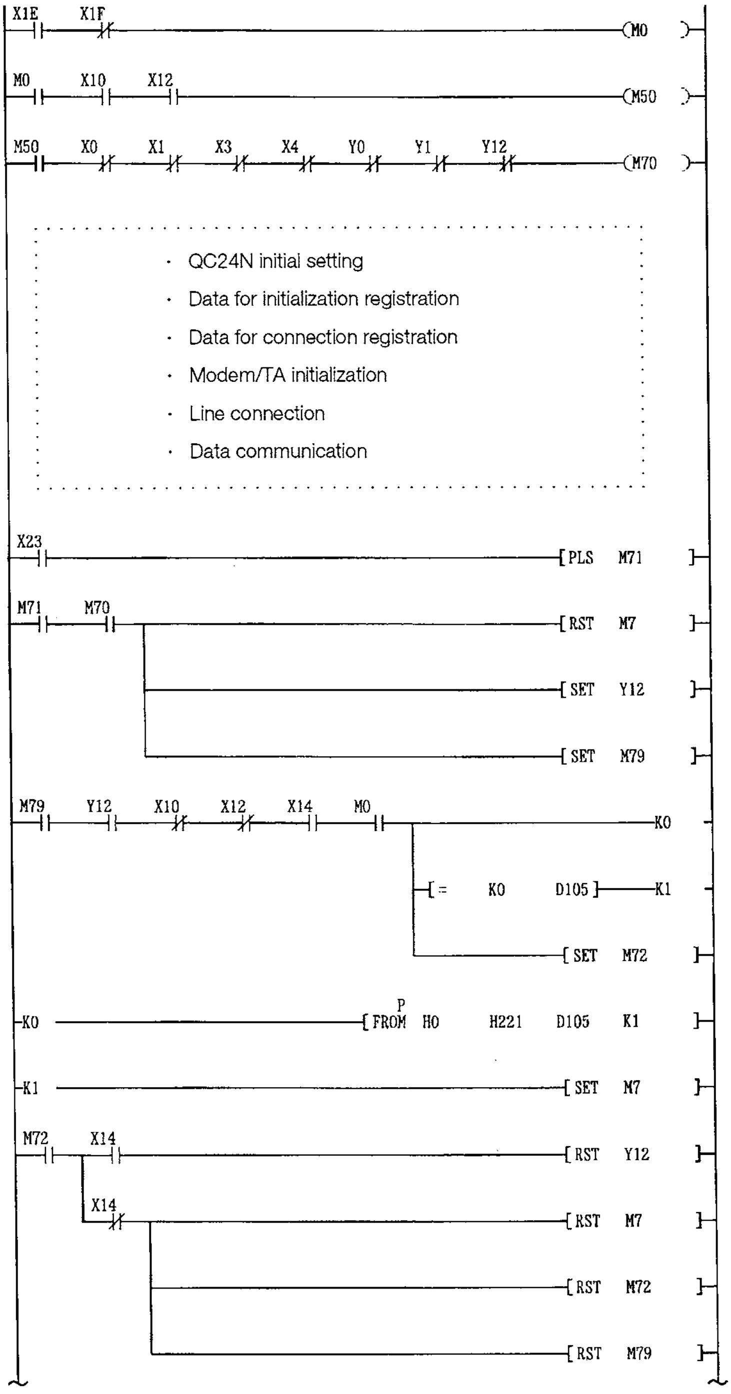
When the line is disconnected, the connecting (X12) signal and the initialization ended (X10) signal turn off, and the modem disconnection ended (X14) signal turns on.

After the modem disconnection ended (X14) signal turns on, turn on the modem disconnection request (Y12) signal for one second to turn off the modem disconnection ended (X14) signal.

3 Program for line disconnection example

An example of a program for line disconnection is shown below.

X0: Transmission normal complete signal
X1: Transmission abnormal complete signal
X3: Reception data read request signal
X4: Reception abnormal detection signal
X10: Initialization complete signal
X12: Connection in progress signal
X1E: QC24N ready signal
X1F: WDT error signal
Y0: Transmission request signal
Y1: Reception data read complete signal
M0: QC24N accessible flag
M50:Data exchangeable flag
M70:Line disconnection enabled flag



· QC24N initial setting	See Section 21.4.4.
· Data for initialization registration	See Section 21.4.5.
· Data for connection registration	See Section 21.4.6.
· Modem/TA initialization	See Section 21.4.7.
· Line connection	See Section 21.4.8.
· Data communication	See Section 21.4.9.

Convert the line disconnection command into pulse

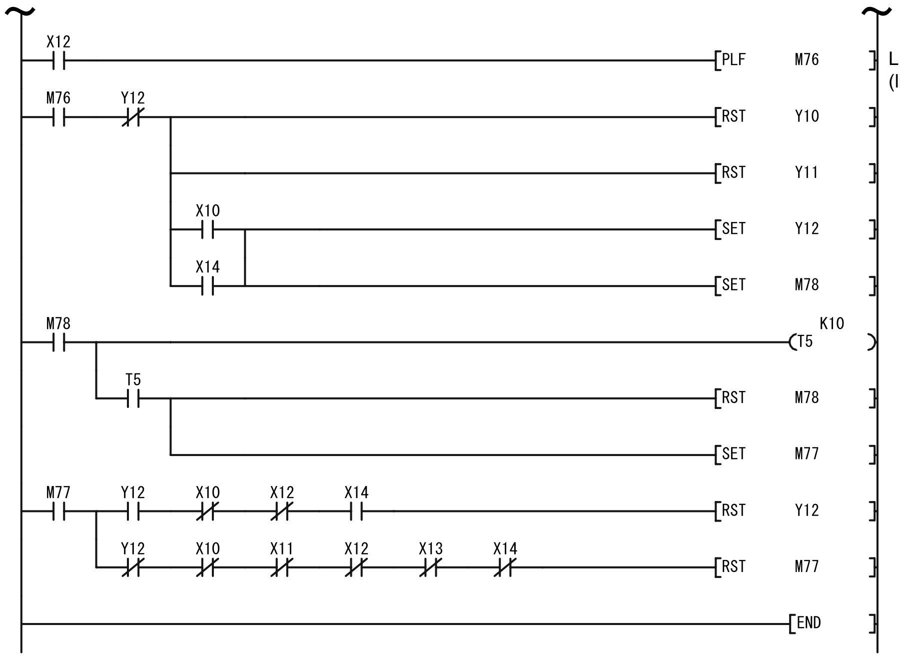
Line disconnection processing
(Line disconnection from host station)

- Modem disconnection request signal is turned ON

- When the modem disconnection complete signal ON, the error code is read
- When the normal completion, the line disconnection complete flag is turned ON

- Modem disconnection request signal is turned OFF

- When the clear command of the flag, the line disconnection request and the complete flag are turned OFF



Line disconnection processing
(line disconnection from the external device)

- Turn off each request signal.
- Turn on the modem disconnection request signal when any of complete signals or the connecting signal is turned on.
- To turn off the modem disconnection ended (X14) signal, turn on the modem disconnection request (Y12) signal and wait for one second.
- Turn off the request signal when the modem disconnection ended signal is turned on.
- End the processing when the modem disconnection ended signal is turned off.

21.5 Sample Programs

This section shows sample programs to test the connection with the remote station's PLC CPU to which QC24N is installed.

Each program contains a minimum set of processing necessary for performing a exchange test.

Modify the data for initialization and data for connection to match each system environment.

When adding error-handling procedures, add them separately by seeing the explanation in Chapter 21 in this manual,.

In these sample programs, the data for initialization and data for connection are registered to the buffer memory (not in the EEPROM).

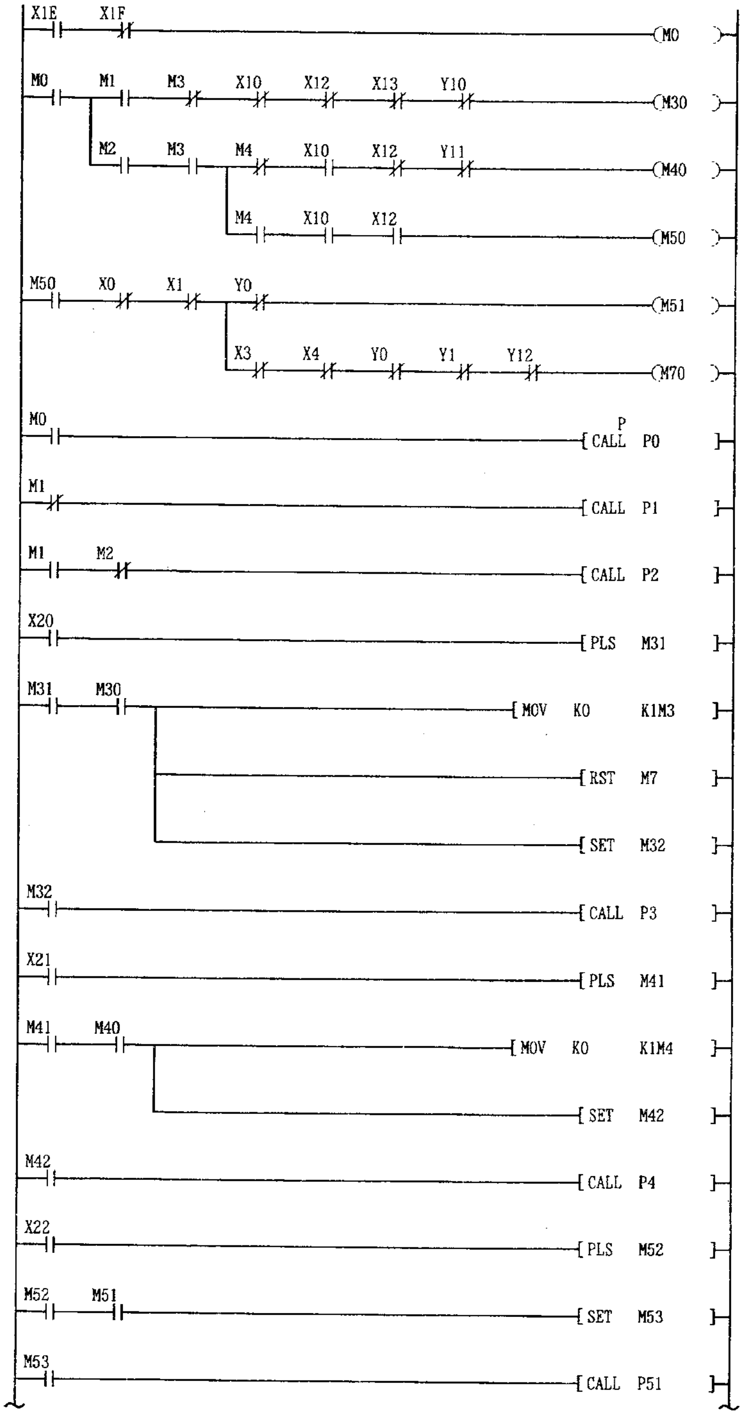
The uses of major devices that are used in these sample programs are listed below.

Application of device (comment list)					
Device	Application	Device	Application	Device	Application
X0	Transmission normal completion	Y61	Initialization data registration completion	M100	Initialization request execution
X1	Transmission abnormal completion	Y62	Data registration completion for connection	M101	Connection request execution Notification execution
X2	Transmission processing in progress	Y63	Initialization completion	M102	Transmission request execution
X3	Reception data read request	Y64	Line connection completion	M103	Reception data read execution
X4	Reception abnormal detection	Y66	Notification completion		
X10	Initialization completion	Y67	Line disconnection completion	SM400	Always ON
X11	Dialing				
X12	Connection in progress	M0	QC24N accessible	D0	Number of registration data bytes
X13	Initialization/connection abnormal completion	M1	Initialization data registration completion	D1	Control number designation Receiver designation
X14	Modem disconnection ended	M2	Data registration completion for connection	D2	Initialization command/telephone number
X15	Notification normal completion	M3	Initialization completion	D11	External line dialing number, etc.
X16	Notification abnormal completion	M4	Line connection completion	D12	Line type, etc.
X1E	QC24N ready	M6	Notification completion	D23	Message transmission waiting time
X1F	WDT error	M7	Line disconnection completion	D24	Message
X20	Initialization command	M10	Convert the registration command into pulse	D39	Message length
X21	Line connection command	M20	Convert the registration command into pulse	D50	Number of transmission data
X22	Data communication command	M30	Initialization enabled	D51	Transmission data
X23	Line disconnection command	M31	Convert the initialization command into pulse	D60	Number of reception data
X24	Notification command	M40	Connectable	D61	Reception data
		M41	Convert the connection command into pulse	D100	Initialization error code
Y0	Transmission request	M50	Data communication is possible	D101	Line connection error code
Y1	Reception data read completion	M51	Transmission enabled	D102	Notification error code
Y10	Initialization request	M52	Convert the transmission command into pulse	D103	Data transmission error code
Y11	Connection request	M60	Convert the notification command into pulse	D104	Data reception error code
Y12	Modem disconnection request	M70	Line disconnection enabled	D105	Line disconnection error code
Y14	Notification-issued request	M71	Convert the line disconnection command into pulse		
Y60	QC24N accessible	M80	Line disconnection (request) occurrence		

21.5.1 Sample program for data communication

1 Sample program on the connection request station side

The modem initialization, line connection, data communication by the non procedure protocol and line disconnection are executed by commands from the user.



Accessible flag to QC24N is turned ON

Modem initialization enabled flag is turned ON

Line connectable flag with the remote station is turned ON

Exchangeable flag with the partner station is turned ON

Data transmission enabled flag to the partner station is turned ON

Line disconnection enabled flag with the partner station is turned ON

To the QC24N initial setting processing subroutine

To the data registration processing for initialization subroutine

To the data registration processing for connection subroutine

Convert the initialization command into pulse

Various complete flags after the modem initialization processing is turned OFF

To the modem initialization processing subroutine

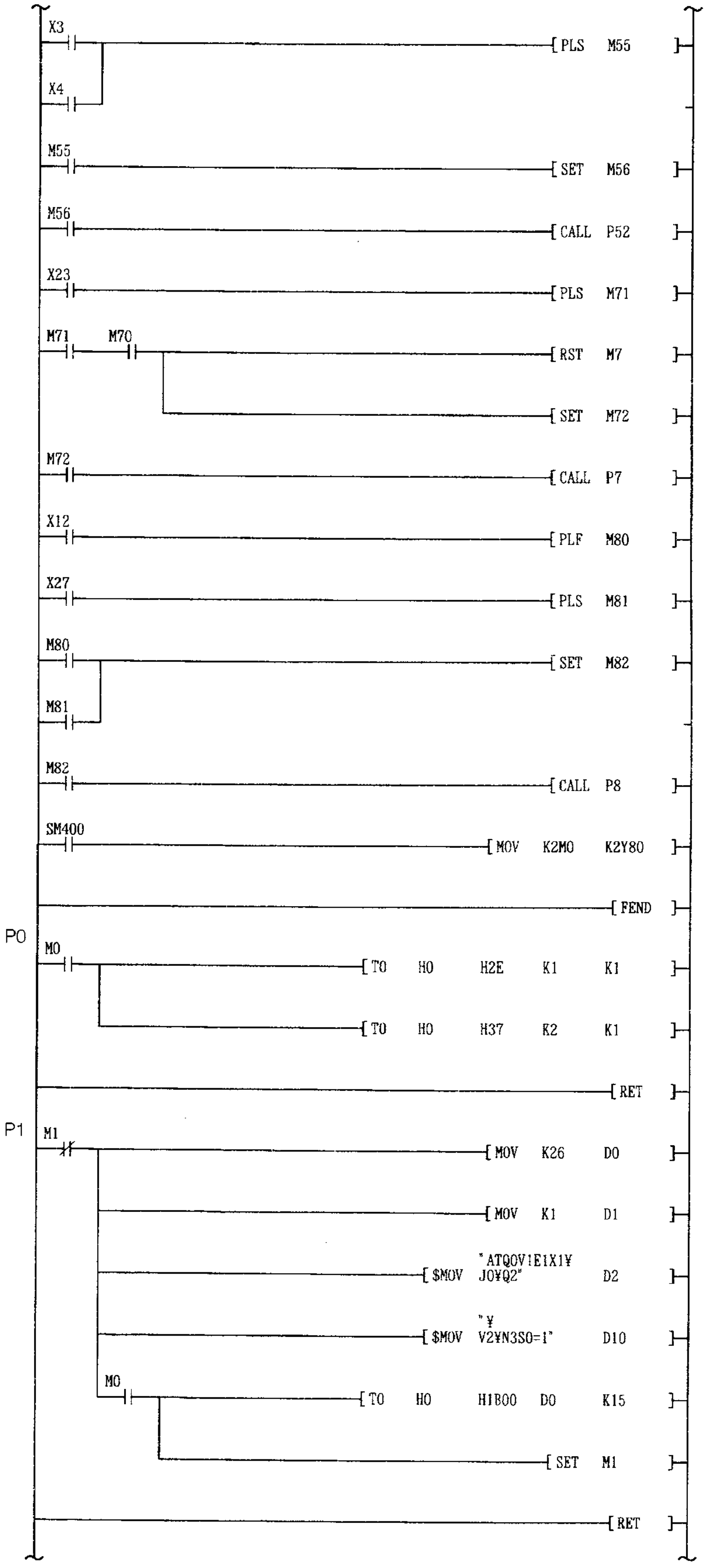
Convert the line connection command into pulse

Various complete flags after the line connection processing into pulse

To the line connection processing subroutine

Convert the data communication (transmission) command into pulse

To the data transmission processing subroutine



Convert the reception data read request into pulse

To the reception data read processing subroutine

Convert the line disconnection command into pulse
(Line disconnection from host station)

Line disconnection complete flag is turned OFF

To the line disconnection processing subroutine

Convert the connection in progress signal OFF into pulse
(Line disconnection from partner side)

Convert the OFF command of various request signal into pulse

To the various request signal and the complete signal OFF subroutine

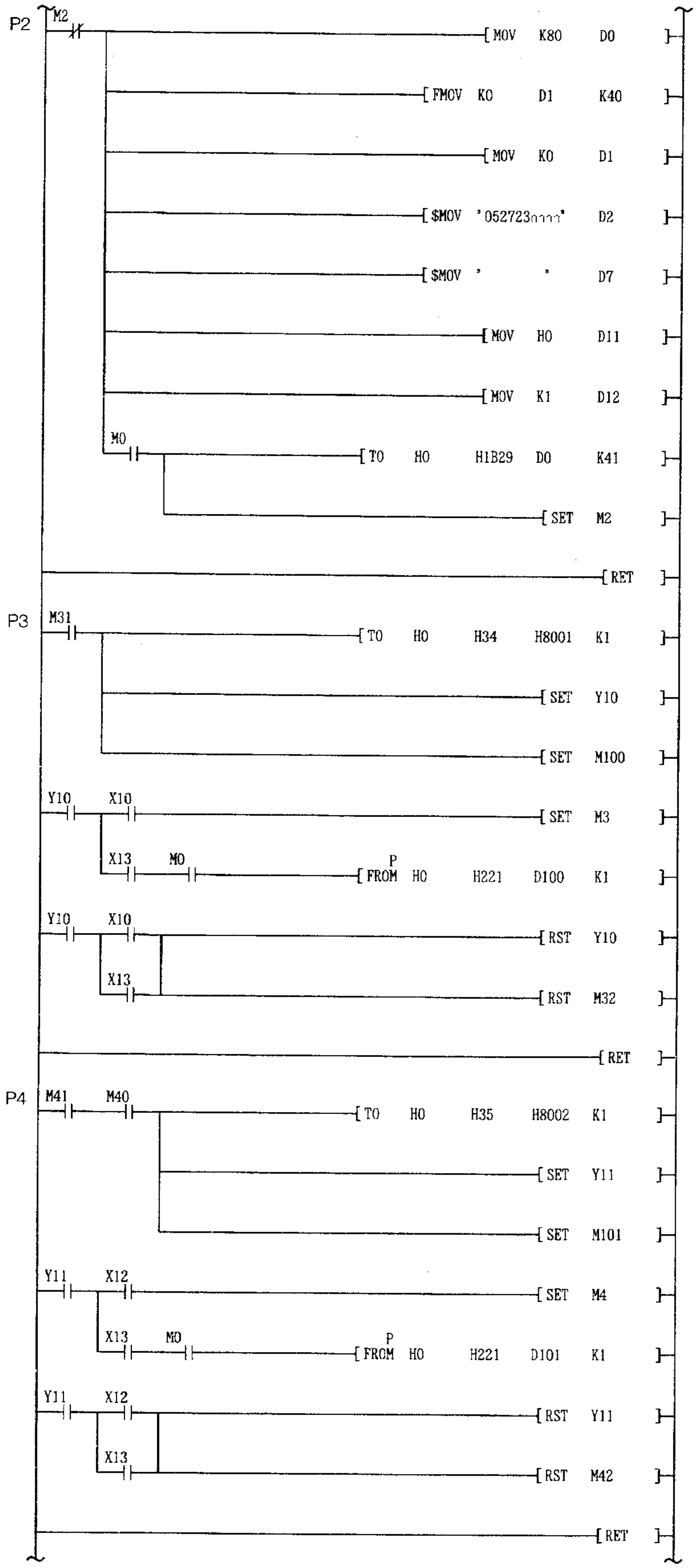
Output the various complete flag status (LED display)

Initial setting processing subroutine

- Set the modem connection channel number
- Set the no-communication interval time (2 minutes)

Data registration processing for initialization subroutine

- Set the number of bytes of the registration data
- Set the user control data (control number)
- Set the initialization command
- Write the data for initialization
  (Registration to buffer memory)
- Data registration complete flag for initialization is turned ON



Data registration processing for connection subroutine

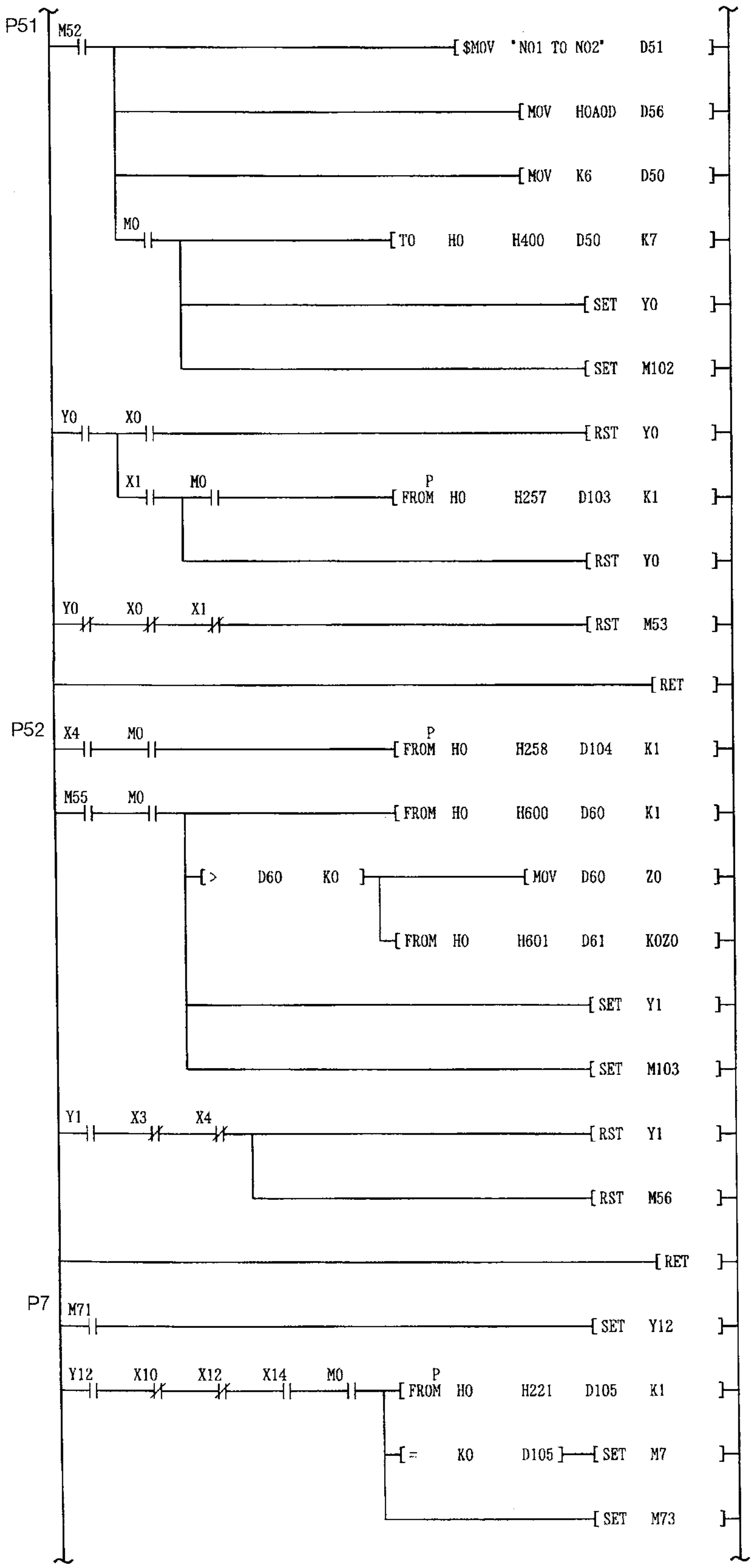
- Set the number of bytes of the registration data
- Clear the data storage device for connection
- Set the pager receiver designation (Notification is not executed)
- Set the telephone number
- Set the space to the remainder of the telephone number designation area
- Set the external line dialing number (0)
- Set the line type (tone)
- Write the data for connection (Registration to buffer memory)
- Data registration complete flag for connection is turned ON

Modem initialization processing subroutine

- Write the data number for initialization
- Initialization request signal is turned ON
- Initialization request execution flag is turned ON
- When the initialization complete signal ON, the initialization complete flag is turned ON and the request signal is turned OFF
- When the initialization/connection abnormal complete signal ON, the error code is read and the request signal is turned OFF

Line connection processing subroutine

- Write the data number for connection
- Connection request signal is turned ON
- Connection request execution flag is turned ON
- When the connection in progress signal ON, the connection complete flag is turned ON and the request signal is turned OFF
- When the initialization/connection abnormal complete signal ON, the error code is read and the request signal is turned OFF



Data communication processing subroutine
(Non-procedure protocol, transmission)

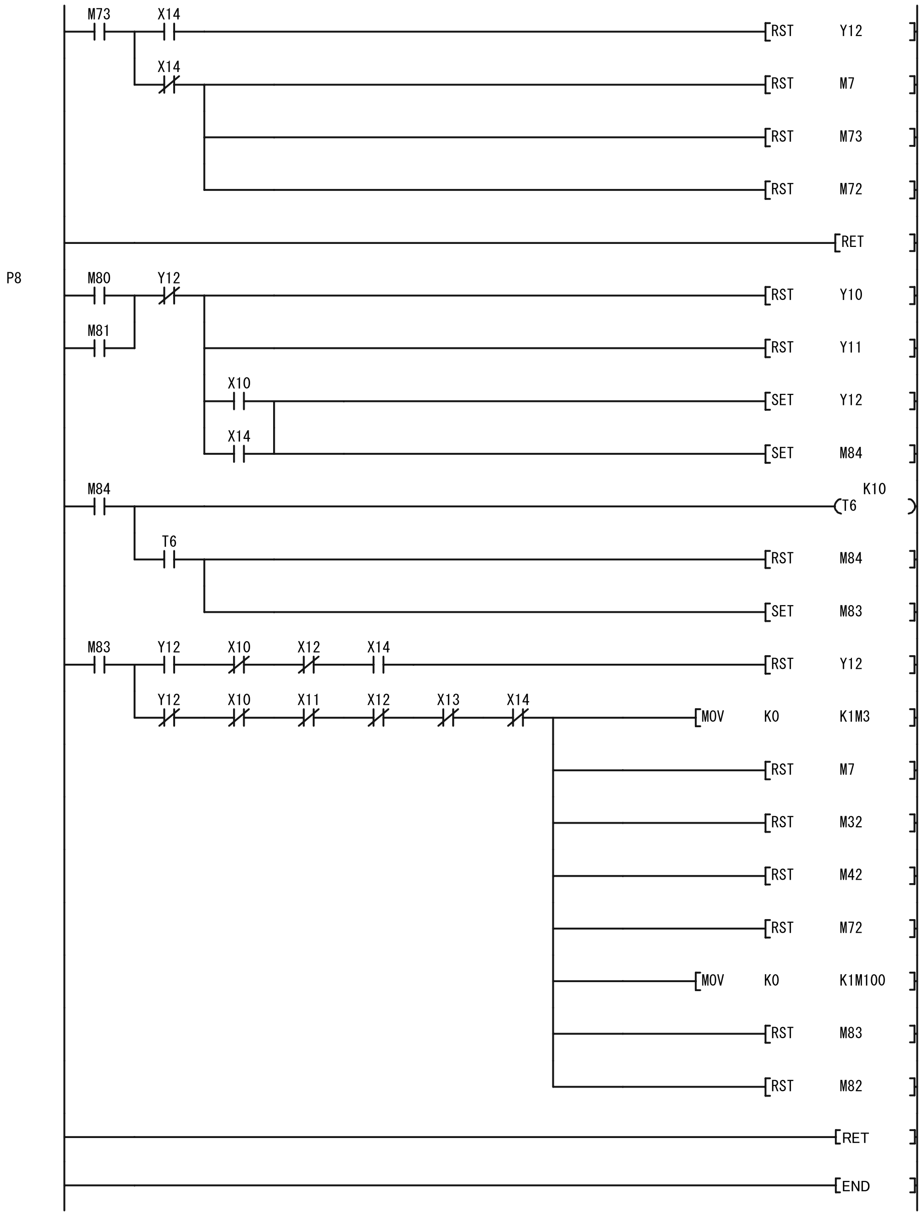
- Set the transmission data
- Set the number of transmission data (words)
- Write the transmission data, etc.
- Transmission request signal is turned ON
- Transmission request execution flag is turned ON
- When the transmission normal complete signal ON, the transmission request signal is turned OFF
- When the transmission abnormal complete signal ON, the error code is read and the request signal is turned OFF

Data reception processing subroutine
(Non-procedure protocol, reception)

- When the reception abnormal detection signal ON, the error code is read
- Read the reception data, the reception data read complete signal is turned ON
- Reception data read execution flag is turned ON
- When the reception data read request signal OFF, the reception data read complete signal is turned OFF

Line disconnection processing subroutine
(Line disconnection from host station)

- When the modem disconnection complete signal ON, the error code is read
- When the normal complete signal ON, the line disconnection complete flag is turned ON



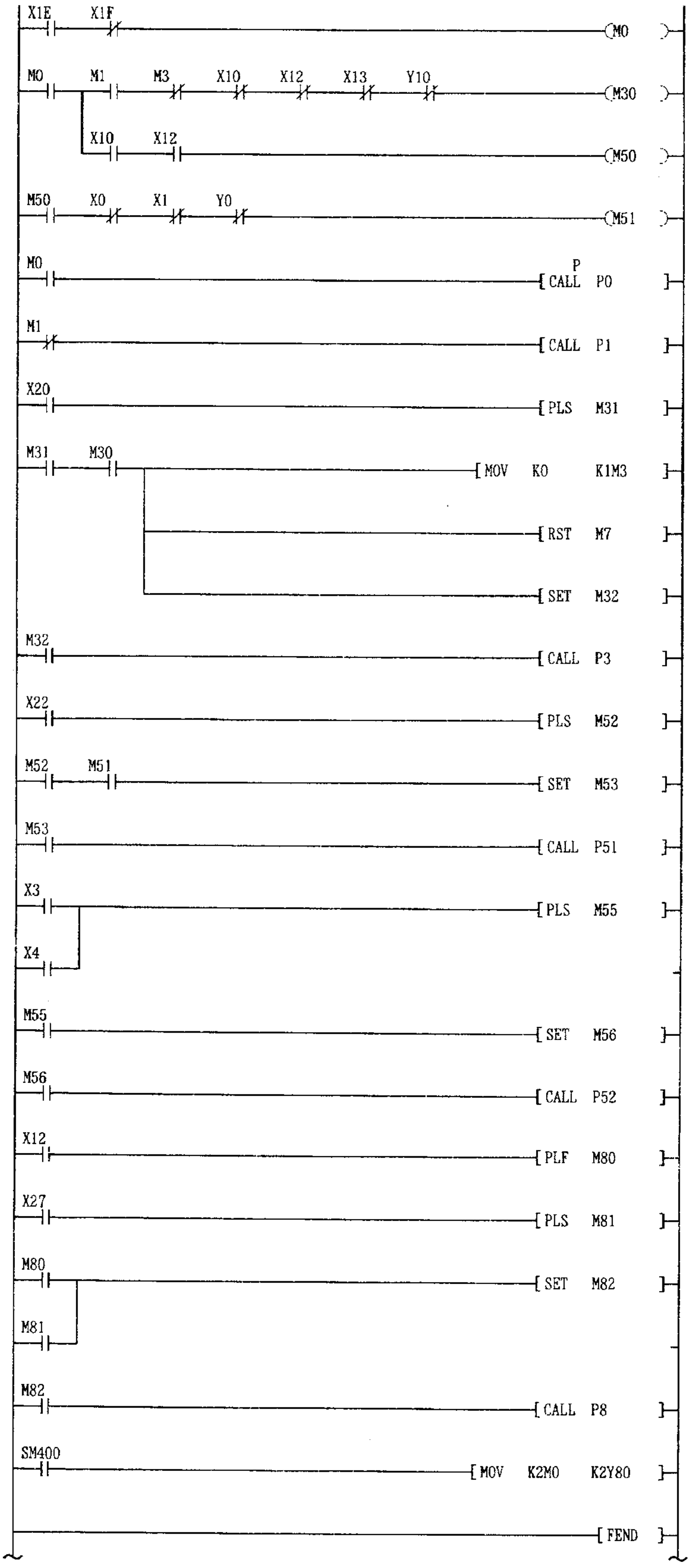
- Turn off the modem disconnection request signal.

A subroutine program that turns off each request signal and complete signal

- Turn off each request signal.
- Turn on the modem disconnection request signal when any of complete signals is turned on.
- To turn off the modem disconnection ended (X14) signal, turn on the modem disconnection request (Y12) signal and wait for one second.
- Turn off the request signal when the initialization ended signal is turned off and the modem disconnection ended signal is turned on.
- Turn off the flag when the corresponding signal is turned off.

2 Sample program on the connection reception station side

The modem initialization and data communication by the non procedure protocol are executed by commands from the user.



QC24N accessible flag is turned ON

Modem initialization enabled flag is turned ON

Exchangeable flag with the partner station is turned ON

Data transmission enabled flag to the partner station is turned ON

To the QC24N initial setting processing subroutine

To the data registration processing for initialization subroutine

Convert the initialization command into pulse

Various complete flags after the modem initialization processing is turned OFF

To the modem initialization processing subroutine

Convert the data communication (transmission) command into pulse

To the data communication processing subroutine

Convert the reception data read request into pulse

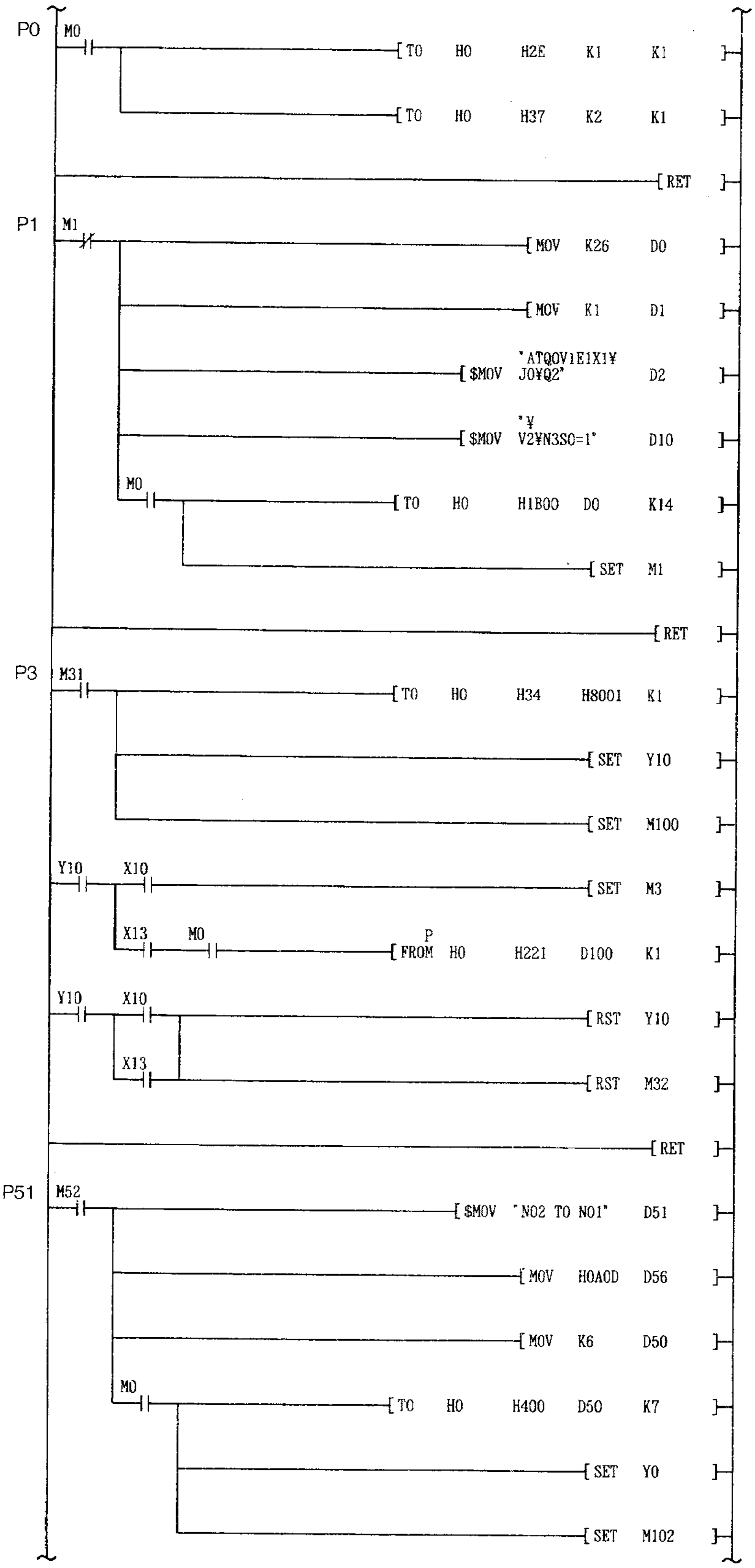
To the reception data read processing subroutine

Convert the connection in progress signal OFF into pulse (Line disconnection from partner side)

Convert the OFF command of various request signal into pulse

To the various request signal and the complete signal OFF subroutine

Output the various complete flag status (LED display)



Initial setting processing subroutine

- Set the modem connection channel number
- Set the no-communication interval time (2 minutes)

Data registration processing for initialization subroutine

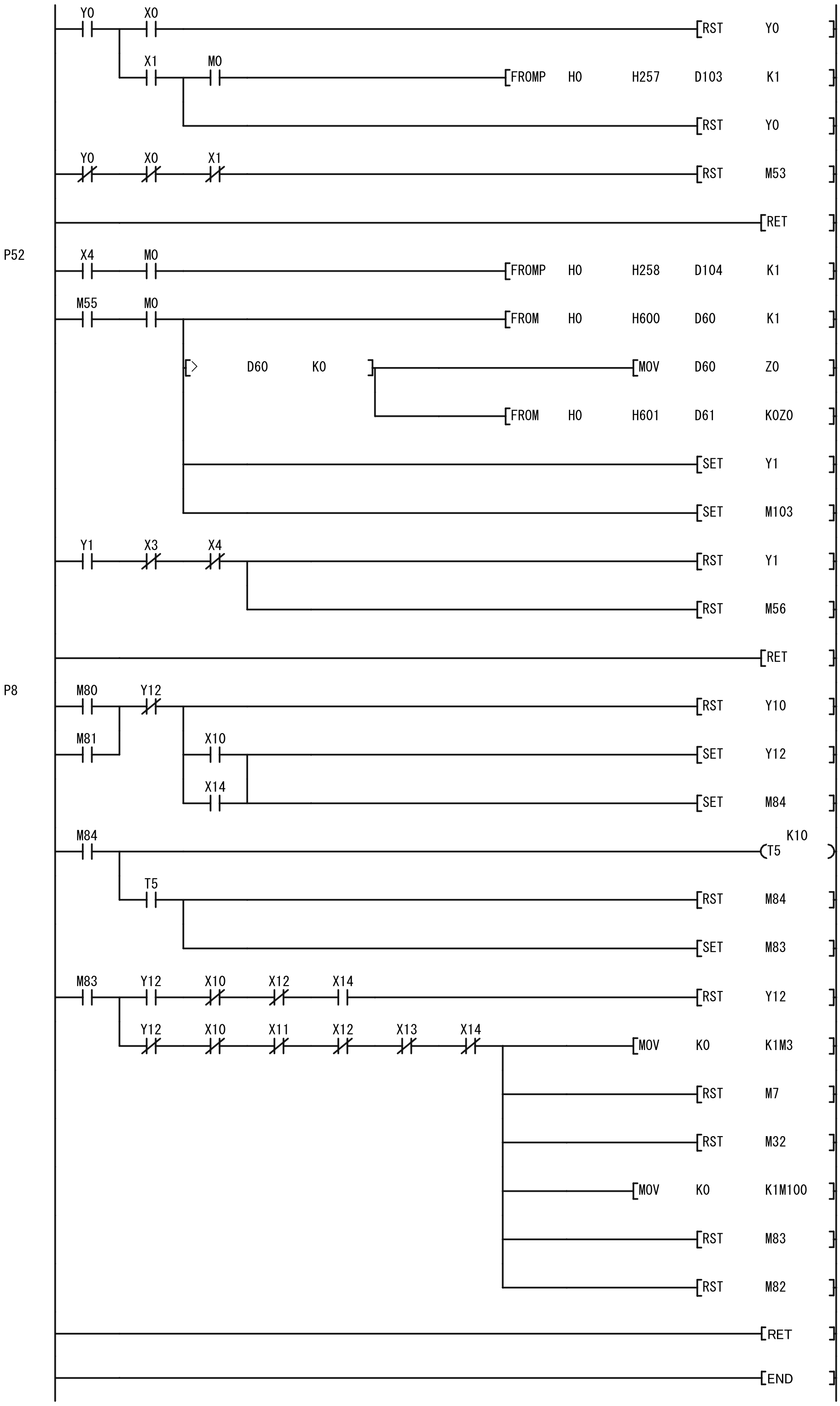
- Set the number of bytes of the registration data
- Set the user control data (control number)
- Set the initialization command
- Write the data for initialization (Registration to buffer memory)
- Data registration complete flag for initialization is turned ON

Modem initialization processing subroutine

- Write the data number for initialization
- Initialization request signal is turned ON
- Initialization request complete flag is turned ON
- When the initialization complete signal ON, the initialization complete flag is turned ON and the request signal is turned OFF
- When the initialization/connection abnormal complete signal ON, the error code is read and the request signal is turned OFF

Data communication processing subroutine (Non-procedure protocol, transmission)

- Set the transmission data
- Set the number of transmission data (words)
- Write the transmission data, etc.
- Transmission request signal is turned ON
- Transmission request execution flag is turned ON



- Turn off the transmission request signal when the transmission normal complete signal is turned on.
- Read an error code and turn off the request signal when the transmission abnormal complete signal is turned on.

Data reception processing subroutine (nonprocedural protocol, reception)

- Read an error code when the reception abnormal detection signal is turned on.
- Read the receive data and turn on the reception data read complete signal.

- Turn on the reception data read execution flag.
- Turn off the reception data read complete signal when the reception data read request signal is turned off.

A subroutine program that turns off each request signal and complete signal

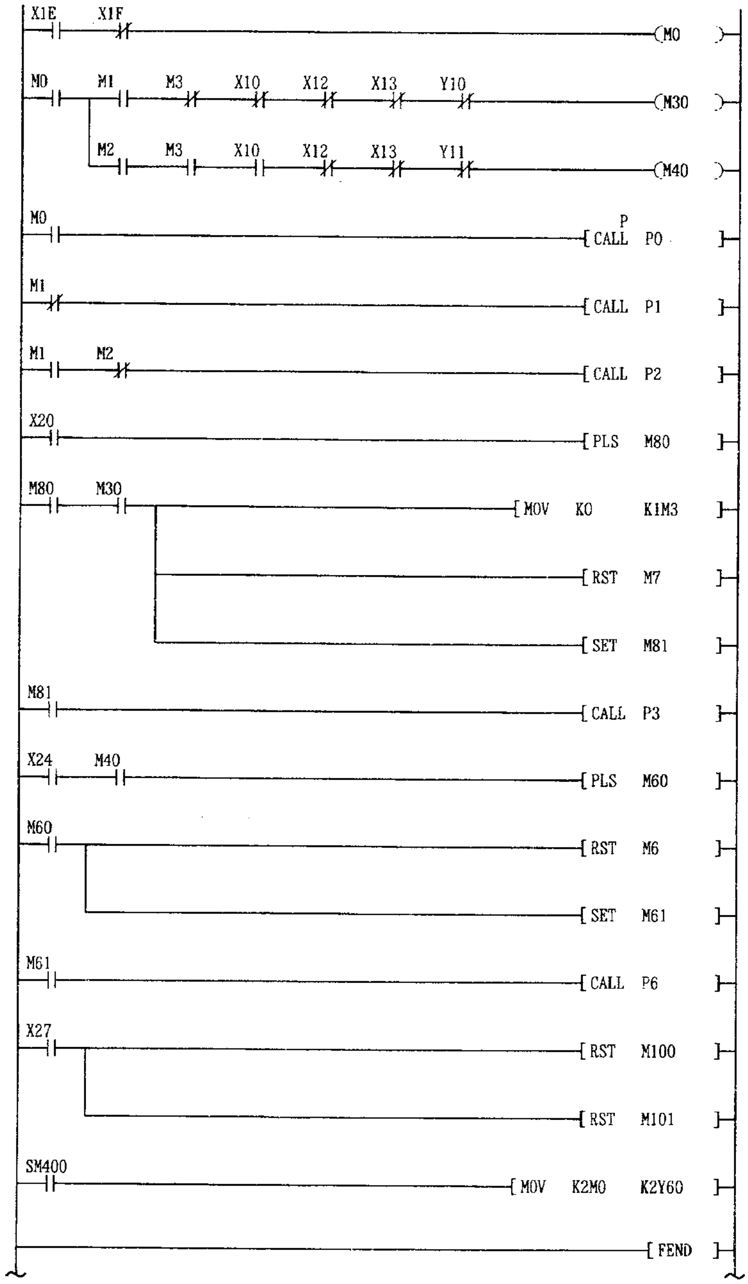
- Turn off each request signal.
- Turn on the modem disconnection request signal when any of complete signals is turned on.

- To turn off the modem disconnection ended (X14) signal, turn on the modem disconnection request (Y12) signal and wait for one second.

- Turn off the request signal when the initialization ended signal is turned off and the modem disconnection ended signal is turned on.
- Turn off the flag when the corresponding signal is turned off.

21.5.2 Sample program for notification

Modem initialization and notification are executed by commands from the user.



QC24N accessible flag is turned ON

Modem initialization enabled flag is turned ON

Line connectable flag with the remote station is turned ON

To the QC24N initial setting processing subroutine

To the data registration processing for initialization subroutine

To the data registration processing for connection subroutine

Convert the initialization command into pulse

Various complete flags after the modem initialization processing is turned OFF

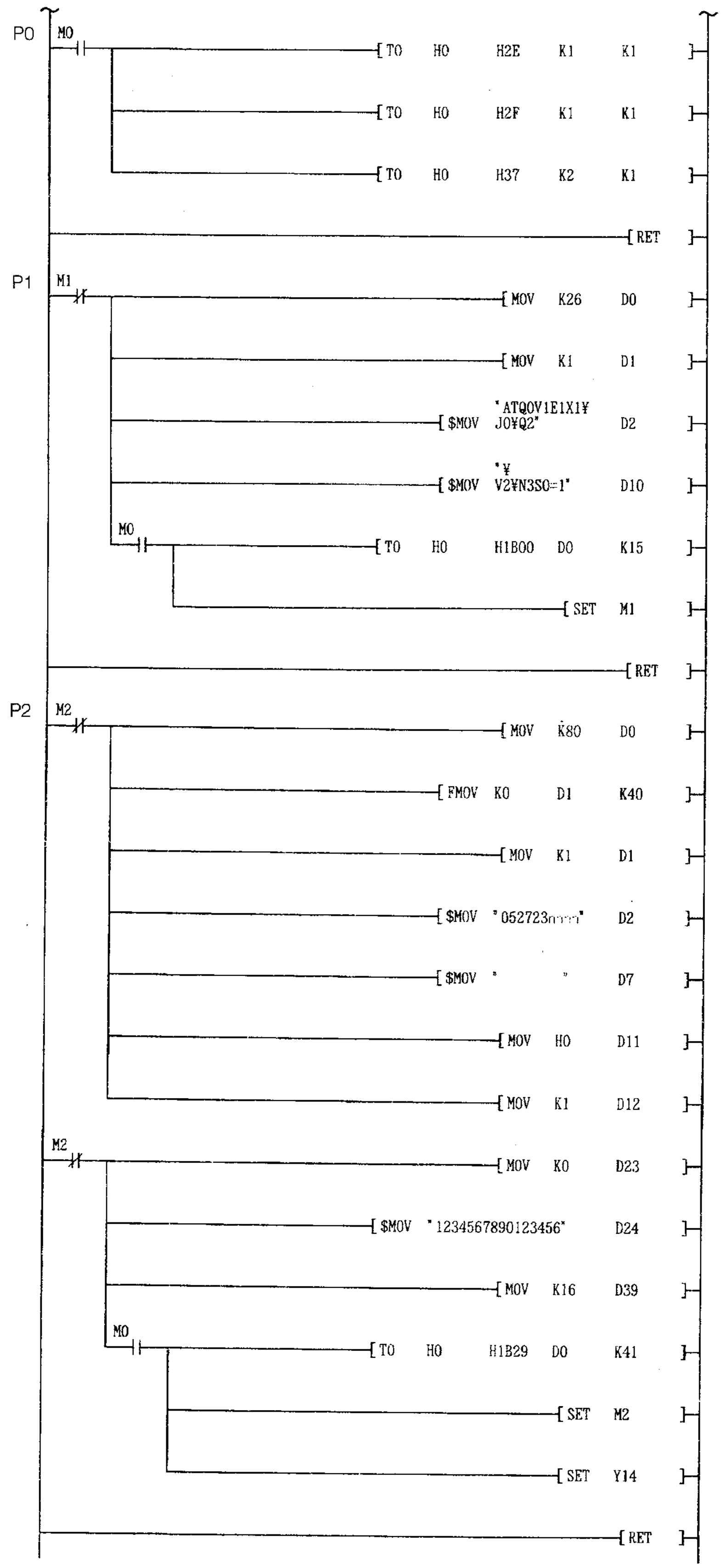
To the modem initialization processing subroutine

Convert the notification command into pulse

To the notification processing subroutine

When the flag OFF command, the complete flag is turned OFF

Output the various complete flag status (LED display)



```
P0  M0
        [TO    H0   H2E   K1   K1  ]
        [TO    H0   H2F   K1   K1  ]
        [TO    H0   H37   K2   K1  ]
        [RET                       ]
P1  M1
        [MOV   K26        D0       ]
        [MOV   K1         D1       ]
        [$MOV  "ATQ0V1E1X1¥J0¥Q2"  D2  ]
        [$MOV  "¥V2¥N3S0=1"        D10 ]
    M0
        [TO    H0   H1B00 D0   K15 ]
        [SET   M1                  ]
        [RET                       ]
P2  M2
        [MOV   K80        D0       ]
        [FMOV  K0    D1   K40      ]
        [MOV   K1         D1       ]
        [$MOV  "052723nnnn"  D2    ]
        [$MOV  "          "  D7    ]
        [MOV   H0         D11      ]
        [MOV   K1         D12      ]
    M2
        [MOV   K0         D23      ]
        [$MOV  "1234567890123456"  D24 ]
        [MOV   K16        D39      ]
    M0
        [TO    H0   H1B29 D0   K41 ]
        [SET   M2                  ]
        [SET   Y14                 ]
        [RET                       ]
```

Initial setting processing subroutine

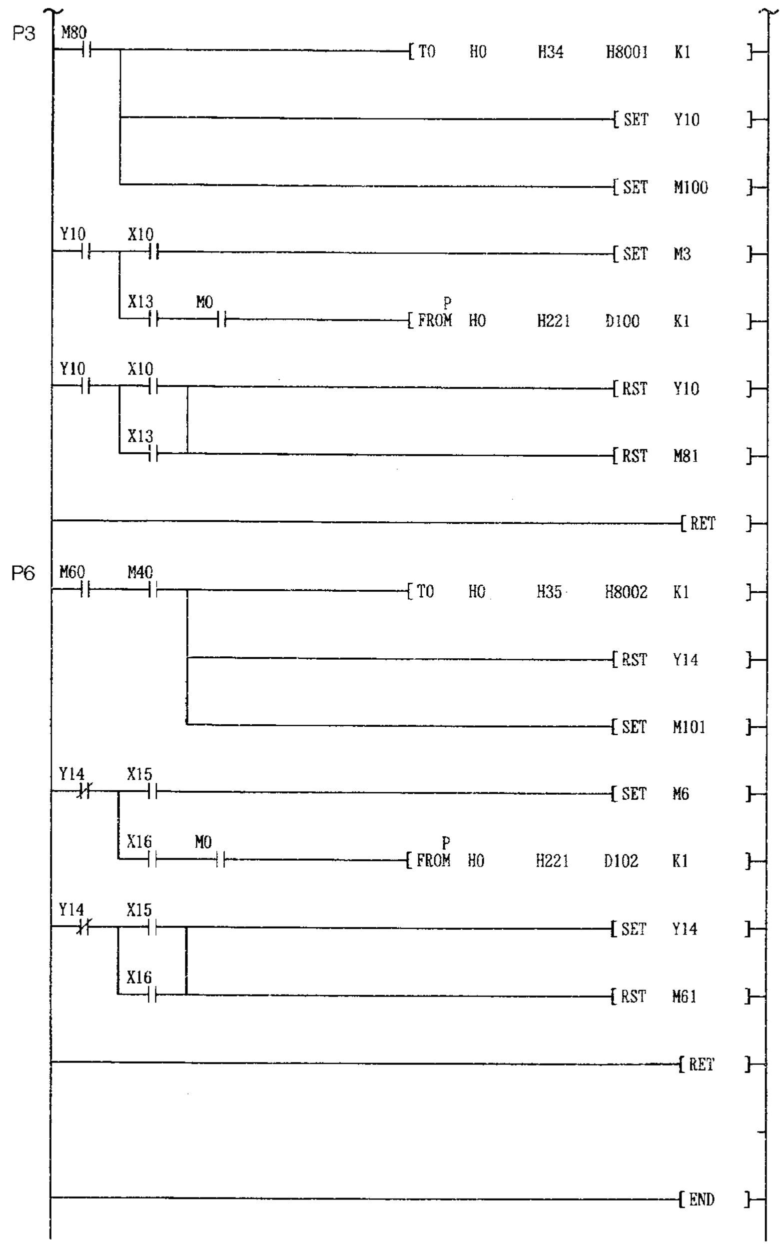
- Set the modem connection channel number
- Set the notification execution
- Set the no-communication interval time (2 minutes)

Data registration processing for initialization subroutine

- Set the number of bytes of the registration data
- Set the user control data (control number)
- Set the initialization command
- Write the data for initialization (Registration to buffer memory)
- Data registration complete flag for initialization is turned ON

Data registration processing for connection subroutine

- Set the number of bytes of the registration data
- Clear the data storage device for connection
- Set the pager receiver specification (Notification is executed)
- Set the telephone number
- Set the space to the remainder of the telephone number designation area
- Set the external line dialing number (0)
- Set the line type (tone)
- Set the waiting time for the message transmission (This is dummy because the pager receiver designated data is 1)
- Set the message
- Set the message length
- Write the data for connection (Registration to buffer memory)
- Data registration complete flag for connection is turned ON
- Notification-issued request signal is turned ON (Initial status)



Modem initialization processing subroutine

- Write the data number for initialization
- Initialization request signal is turned ON
- Initialization request execution flag is turned ON
- When the initialization complete signal ON, the initialization complete flag is turned ON and the request signal is turned OFF
- When the initialization/connection abnormal complete signal is turned ON, the error code is read and the request signal is turned OFF

Notification processing subroutine

- Write the data number for connection (for notification)
- Notification-issued request signal is turned OFF (Issue request)
- Notification execution flag is turned ON
- When the notification normal complete signal ON, the notification complete flag is turned ON and the request signal is turned ON (Initial status)
- When the notification abnormal complete signal ON, the error code is read and the request signal is turned ON (Initial status)

TROUBLESHOOTING

This section describes the error codes and their contents, processing method, and troubleshooting by symptom when trouble occurs while using the serial communications module.

22. TROUBLESHOOTING

When the QC24(N) and external devices cannot communicate normally, whether the cause of the trouble is in the QC24(N) or the external device must be determined.
This sections describes the contents, corrective, and corrective action of errors generated during communications between the QC24(N) and an external device.

22.1 Error Code Tables

The following shows the error codes, error contents, and corrective action for errors that are generated during communications between the QC24(N) and an external device.
For errors without a corresponding LED entered, only the "NAK" LED is turned ON.

22.1.1 Error code table

The following indicates the error codes, error contents, and corrective action for errors generated during communications using the MC protocol (except the A compatible frame), communications using the non procedure protocol, and communications using the bidirectional protocol.
("*" in the table is the error code when the target CPU is not a QnACPU.)

Error code (Hexa-decimal)	Error	Error contents	Indicator LED	Corrective action	Protocol		
					Dedicated	Non procedure	Bidirectional
3E8H to 3FFFH	—	• (Error detected by the CPU)	—	• See Troubleshooting of the CPU user's manual (detailed) and take corrective action.	○		
4000H to 4FFFH	—	• (Error detected by the CPU)	—	• See Appendix 5 of the QnACPU user's manual (details) and take corrective action.	○		
7101H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7102H							
7103H	PLC access error	• Cannot communicate with QC24(N) CPU.	C/N	• Make the watchdog timer (timer 1) time longer. • Check if the CPU can communicate in mode "F".	○		
7104H to 7116H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7140H*	Request data error	• Number of request points exceeds the range for the command. • A word device was designated in a bit units command. • The last device No. exceeds the range. [Given device last No. ≥ Designated head device No. + Designated number of points]	PRO	• Check and correct the external device transmit message and restart data communications. • If no error is found in the device range, clear the PLC CPU information and retry. (Refer to Section 19.6)	○		
7141H*	Target ACPU error	• A request was given to the CPU which is not corresponding with the compatible frame command.	PRO	• Check the command description and communicate with a corresponding command again. • Make a communication with the CPU which corresponds to the requested command.	○		
7142H*	Device name error	• A device that cannot be designated by the given command was designated.	PRO	• Check and correct the external device transmit message and restart data communications. • If no error is found in the device name, clear the PLC CPU information and retry. (Refer to Section 19.6)	○		
7143H*	Device No. error	• The head device No. is out of range.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7144H*	Monitor data write error	• Monitoring was requested before the device to be monitored was written.	PRO	• Write the device to be monitored before issuing a monitor request.	○		
7145H*	Monitor PLC No. error	• The written PLC No. and PLC No. in the monitor request are different.	C/N	• Rewrite the monitor data.	○		

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7146H*	Monitor CPU model name error	• The written CPU model name and the CPU monitor name in the monitor request are different.	C/N	• Rewrite the monitor data.	o		
7147H*	Written number of monitoring points overrun error	• The written number of monitoring points exceeds the designated range.	PRO	• Check and correct the external device transmit message and restart data communications.	o		
7148H*	Extension block No. error	• A nonexistent extension file register block No. was designated. • A block No. being used as an extension comment area, sampling trace area, or status latch area was designated.	PRO	• Correct the designated block No. and restart data communications.	o		
7149H*	ACPU error during ROM running	• Parameter or PLC program write is performed during ROM running.	—	• Restart communication after switching to the RAM operation.	o		
714AH*	Cannot execute a command during RUN	• A write command was designated when "Disable write during RUN" was set. • Parameter or sequence program was written during RUN.	C/N	• Change the setting to "Enable write during RUN" and restart data communications. • Stop the CPU and restart data communications.	o		
714CH*	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
714DH*	Unsable command error	• A command of QnA frame not corresponding was requested to the ACPU.	C/N	• Check the sending message/request description and use a command supported by the ACPU. Or change the command to the A compatible frame and recommunicate. • If no error is found in the command, clear the PLC CPU information and retry. (Refer to Section 19.6)	o		
714EH*	Monitor network No. error	• The written monitor network No. and the monitor request network No. are different.	C/N	• Check and correct the other station access valid module Nos. in the network parameters. • Rewrite the monitor data.	o		
7150H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7151H	PLC No. designation error	• A PLC No. other than "FF" or "0 to 64(00H to 40H)" was designated.	C/N	• Check and correct the external device transmit message and restart data communications.	o		
7152H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7153H	Frame length error	• The received message length has exceeded the allowable range.	CHn ERR.	• Review the transmission message. • Correct the message format so the number of access points is within the allowable range.	o		
7154H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7155H	Unwritten monitor data error	• Monitoring was requested before monitor data was written.	PRO	• Write the device to be monitored before issuing a monitor request.	o		
7156H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7160H	PLC access error	• CPU model name cannot be confirmed.	C/N	• If there is an error in the CPU, remove the CPU error and restart data communications.	o		
7161H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7164H	Request contents error	• Error in request contents or in the device specified method.	—	• Check and correct the external device transmit message and/or request contents and restart data communications.	o		
7166H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7167H	Cannot execute a command during RUN	• A write command was designated when "Disable write during RUN" was set.	C/N	• Change the setting to "Enable write during RUN" and restart data communications.	o		
7168H		• A command that cannot be executed during RUN was designated.	C/N	• Stop the CPU and restart data communications.	o		
7169H	CPU error	• Cannot communicate normally with the CPU.	—	• If there is an error in the CPU, remove the CPU error and restart data communications.	o		

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
716BH	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
716CH							
716DH	Monitor data write error	• Monitor data was not written using QnA simplified frame / QnA (extension) frame.	PRO	• Rewrite monitor.	○		
716EH		• Monitor data was not written using A compatible frame.	PRO				
716FH	Device error	• A non-existing device was designated. • The device that cannot be designated for the corresponding command was specified.	PRO	• Check the transmission message of the external device, make correction, and restart communications.	○		
7170H	A compatible frame error	• Number of access points exceeded the range.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7171H		• A device that cannot be specified was designated.	PRO		○		
7172H		• Written number of monitoring points is incorrect. For example, [0] was designated.	PRO		○		
7173H	Monitor data write error	• Monitor data was written for a CPU other than a QnACPU using QnA simplified frame / QnA (extension) frame.	PRO	• Write the monitor data and use the A compatible frame to a CPU other than a QnACPU.	○		
7E00H	Buffer memory length error	• When EEPROM system setting write is performed, a value larger than the specified is set for on demand/sending/receiving buffer size designation of buffer memory.	—	• Set buffer memory length designation of on demand/sending/receiving of buffer memory and end address of each area to 1FFFH or less, then switch on the system setting write request again.	○	○	○
7E01H	System error	• OS of the QC24 (N) detected some error.	—	(*1)			
7E03H to 7E05H							
7E06H	Buffer memory address setting error	• Transmit/receive buffer memory addresses are in the special applications area.	—	• Change the buffer memory addresses so that they are outside the special applications area.	○		
7E07H	EEPROM specification No. error	• Description of EEPROM register/read/delete instruction area of buffer memory and Y signal request do not match.	—	• Check a value of EEPROM register/read/delete instruction area of buffer memory and switch on the EEPROM write/read request. (see section 16.4)	○	○	○
7E08H	Error during mode change processing	• The corresponding channel which mode change was made to is already in the mode change processing.	—	• After the signal turns off during mode change, execute a mode change request again.	○	○	○
7E09H	During transmission sequence initialization	• The corresponding channel which transmission sequence initialization was performed to is already in the initialization processing.	—	• After a 1s or more interval has elapsed after execution of the last transmission sequence initialization, execute transmission sequence initialization again.	○	○	○
7E0AH	Switch setting error (at mode change)	• There is an error in the requested setting description at mode change.	—	• After checking the set value and modifying, perform a mode change again.	○	○	○
7E40H	Command error	• A nonexistent command or subcommand was designated.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7E41H	Data length error	• A data length exceeding the number of points that can communicate during random read/write was designated.	PRO		○		
7E42H	Error count error	• Number of requested points exceeds the range for the command.	PRO		○		
7E43H	Device error	• A nonexistent device was designated.	PRO		○		

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7E44H	Timer 1 time-out error	• A response message was not returned within the response watchdog timer (timer 1) monitoring time.	C/N	• Make the timer 1 monitoring time longer. • When accessing another station's CPU, check if the routing parameters match.	○		
7E47H	Continuous request error	• The next request was received before a response message was returned for the preceding request.	PRO	• Do not issue continuous requests from the external device. • Set the timer 1 monitoring time to the external device time-out time.	○		
7E48H to 7E4EH	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7E4FH	Device point count error	• Access point count is incorrect.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7E50H	User frame No. designation error	• A user frame No. outside the range was designated.	PRO	• Check and correct the external device transmit message and restart data communications. • Review the frame No..	○	○	
7E51H	Unwritten user frame error	• An unwritten user frame No. was designated.	PRO	• Write the frame beforehand. • Change the frame No. and restart data communications. • Review the frame No..	○	○	
7E52H	User frame overwrite error	• A written frame No. overwrite request was issued.	PRO	• Change the write destination to an unwritten frame No. • When overwriting, delete the given No. beforehand.	○		
7E53H	User frame access data error	• A nonexistent command was designated in a subcommand. • Byte count exceeding the number of bytes that can be requested was designated.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7E54H	Modification allowed error	• The modification allowed switch was set to OFF when writing to the mode modification EEPROM.	PRO	• Set the modification allowed switch to ON and restart data communications.	○	○	○
7E55H	User frame data error	• There is an error in the user frame variable data.	PRO	• Check and correct the external device transmit message and restart data communications.	○	○	
7E56H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7E57H	EEPROM write error	• Cannot write to EEPROM normally.	—	• Re-execute the write operation. If the error is generated again, replace the module.	○		
7E58H	Mode modification error	• There was an error in the mode No. or transmission designated contents changing the mode.	PRO	• Check and correct the contents of the external device transmit message and restart data communications. • Set the QC24(N) switches to the mode and transmission specifications you want to change.	○	○	○
7E59H	Number of EEPROM write excess error	• The number of EEPROM write exceeds 1000 times.	—	• Write "0" in number of EEPROM write area of the buffer memory (address: 021FH) and recommunicate.	○	○	○

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7E70H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7E80H to 7E83H	Refer to the link dedicated instruction execution error code table, and take the corrective action. (See Section 22.1.3.)						
7E85H to 7E86H							
7E88H to 7E8AH							
7EA0H to 7EA2H							
7EA4H							
7EA6H 7EA8H 7EAAH							
7EC1H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7EC2H							
7EC3H	Double send request error	• A send request signal (Yn0 or Yn7) was turned ON while another send request was being processed.	—	• Interlock the send requests.	○	○	○

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7EC4H	Send data count error, transmit/receive buffer setting error	• The number of data larger than the transmit buffer memory size was transmitted. • The value set to the transmit/receive buffer is outside the range.	—	• Reduce the number of send data to less than the buffer memory size. • Change and increase the non procedure transmit buffer memory size. • Designate the head address and size of the transmit/receive buffer within the range of the user free area.	○	○	○
7EC5H	EEPROM access error	• Write to EEPROM was requested when the setting modification enable/disable switch (SW08) was set to OFF.	—	• When writing to EEPROM, set switch SW08 of the given interface to ON and restart the QC24.	○	○	○
7EC6H		• There is an error in the EEPROM read/write request contents.	—	• Check the read/write request data and designate the correct data.	○	○	○
7F01H	Buffer full error	• The next data was received before processing of the previous data was completed.	—	• Increase the transmission time by performing handshake with the external device, etc.	○		○
		• Multiple requests was simultaneously issued for one channel.		• Perform handshake with the request source external device.	○	○	○
7F20H	ASCII→BIN conversion error	• An ASCII code that cannot be converted to binary code was received.	PRO	• Check and correct the external device transmit message and restart data communications.		○	○
		• An odd number of bytes of data was received during data communications using ASCII→BIN conversion.		• When communicating using ASCII → BIN conversion, always transmit the data in odd number bytes units.			
7F21H	Receive header area error	• There is an error in the command (frame) part. • An ASCII code that cannot be converted to binary code was received.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7F22H	Command error	• A nonexistent command or device was designated.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7F23H	Dedicated protocol message error	• There is no data (ETX, CR-LF, etc.) following the character area, or designation was incorrect.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
7F24H	Sum check error	• The sum check calculated by the QC24(N) and the transmitted sum check are not the same.	P/S	• Review the external device sum check.	○	○	
7F25H	Data length error	• The length of the received data exceeds the receive area size.	CHn ERR.	• Correct the data length that is transmitted from the external device. • Change the "word/byte units" set by the QC24(N) to byte units. • Increase the receiving area of the QC24(N).			○
7F31H	Simultaneous transmission error	• The QC24(N) and an external device started transmitting simultaneously.	—	• Process by agreement with the external device. When necessary, change the simultaneous transmission data valid/invalid designation setting. (Set in buffer memory addresses 9BH/13BH)			○
7F40H	Timer 0 time-out error	• No reception watchdog timer (timer 0) time-out occurred.	PRO	• Check if data was dropped from the receive data. • Check if DTR control, etc. interrupted reception.	○	○	○
7F41H	Timer 1 time-out error	• Response watchdog timer (timer 1) time-out occurred.	—	• Check the status of the message transmission destination and restart data communications, as required.	○		○
7F42H	Timer 2 time-out error	• Transmit watchdog timer (timer 2) time-out occurred.	—	• Check if DTR control, etc. interrupted transmission.	○	○	○

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7F50H to 7F54H 7F61H to 7F66H	System error	• OS of the QC24(N) has detected some error.	—	(*1)			
7F67H	Overrun error	• The QC24(N) received the next data before it completed receive processing of the previous data.	SIO	• Decrease the data transmission rate and restart data communications. • Check whether a temporary stop has occurred in the station in which the QC24(N) is in installed. (For the QnACPU this can be checked using special register SD1005.) If a temporary stop has occurred, remove its cause.	○	○	○
7F68H	Framing error	• The stop bit settings do not match. • Power ON/OFF of the station at the other end caused disorder in the line. • Noise has occurred on the line. • At the time of multidrop connection, data were transmitted simultaneously from multiple devices.	SIO	• Match the setting of the QC24(N) with that of the external device. • Issue the error information initialization request (YnE/YnF) to clear the error information. At the time of communications using the non procedure protocol, discard unnecessary data. • Take measures against noise. • At the time of multidrop connection, provide interlocks so that data are not transmitted simultaneously from multiple devices.	○	○	○
7F69H	Parity error	• The parity bit settings do not match. • Power ON/OFF of the station at the other end caused disorder in the line. • Noise has occurred on the line. • At the time of multidrop connection, data were transmitted simultaneously from multiple devices.	P/S	• Match the setting of the QC24(N) with that of the external device. • Issue the error information initialization request (YnE/YnF) to clear the error information. At the time of communications using the non procedure protocol, discard unnecessary data. • Take measures against noise. • At the time of multidrop connection, provide interlocks so that data are not transmitted simultaneously from multiple devices.	○	○	○
7F6AH	Buffer full error	• OS receive buffer overflowed and receive data was skipped.	SIO	• Use DTR and DC control and perform data communications so that the buffer does not become full. Perform RS · CS control when the modem function is used. • If the Read Request signal was turned ON, execute read immediately.	○	○	○
7F6BH	CD signal control error	• Data was received when CD signal is OFF when "CD terminal check enabled" was designated.	CHn ERR.	• Check the CD signal control of the external device. (Send while the CD signal is ON.) • Set "no CD terminal checking" and perform communication.	○	○	○
7F6CH	Transmission error	• Data cannot be sent because the line is not connected.	CHn ERR.	• Transmit data after line connection processing on the interface side that uses the modem function.	○	○	○
7F91H to 7FBCH 7FC8H to 7FCFH	System error	• OS of the QC24(N) has detected some error.	—	(*1)			

Error code (Hexa-decimal)	Error	Error contents	Indi-cator LED	Corrective action	Protocol		
					Dedi-cated	Non proce-dure	Bidirec tional
7FD0H to 7FE5H	Refer to the error code list while modem function is used, and take the corrective action. (See Section 22.1.4.)						
7FF5H	Processing cancelled due to mode switching, transmission sequence initialization, etc.	• The processing in operation was cancelled due to execution of the following: <Mode switching, transmission sequence initialization, reception data clear, user frame use enable/disable designation, PLC CPU information clear>	—	• Do not execute these functions during any other processing.	○	○	○
F000H to FFFFH	—	[Errors detected by the MELSECNET/10 network system]	—	• Take corrective action by referring to Section 10 of the QnA corresponding MELSECNET/10 network system reference manual.	○		

*1 Perform measures in the following procedures.

①Check that the QC24(N), power supply module, CPU module are properly installed on the base unit.

②Check that the operating environment of the QC24(N) is within the general specification of the CPU module.

③Check that the power capacity is sufficient.

④Check that the hardware of QC24(N), CPU module, and base unit is normal referring to a manual of each unit, or check operation by replacing a unit.

In case a fault is found, contact your local Mitsubishi representative to request repair.

⑤If the above measures do not solve problems, consult your local Mitsubishi representative with detailed description on fault.

22.1.2 A compatible frame communications error code table

The following table lists the error code, error contents, and corrective action for errors generated during A compatible frame communications.

Error code (Hexadecimal)	Error	Error contents	Indicator LED	Corrective action	Protocol		
					Dedicated	Non procedure	Bidirectional
00H	Disable during RUN	• A write command was designated when "Disable write during RUN" was set. • Parameter or sequence program was written during RUN.	C/N	• Change the setting to "Enable write during RUN" and restart data communications. • Stop the CPU and restart data communications.	○		
01H	Parity error	• The data does not match the parity bit setting.	P/S	• Match the QC24(N) and external device settings.	○		
02H	Sum check error	• The sum check calculated by the QC24(N) and the transmitted sum check are not the same.	P/S	• Check the external device sum check.	○		
03H	Protocol error	• Data communications were performed with a control procedure different from the control procedure set in the mode switch. The control procedure is partially different from the designated control procedure.	PRO	• Check and correct the external device transmit message and restart data communications.	○		
04H	Framing error	• The data does not match the stop bit setting.	SIO	• Match the QC24(N) and external device settings.	○		
05H	Overrun error	• The next data was received before the QC24(N) received all the preceding data.	SIO	• Decrease the transmission rate and restart data communications.	○		
06H	Character area error	• Designation method error in part of a message. • A command that does not exist was designated. • The number of processing points is outside the range for the command. • A device that does not exist was designated.	PRO	• Check and correct the external device transmit message and restart data transmission.	○		
08H	PLC access error	• The CPU cannot communicate with the QC24(N).	C/N	• Replace the CPU with a CPU that can communicate with the QC24.	○		
10H	PLC No. error	• The PLC No. is not "FF", or a station No. set in the network parameters.	C/N	• Check and correct the external device transmit message and restart data communications.	○		
42H	Other errors	*See POINT.			○		

POINT

- If an error occurs during A compatible frame communications, the QC24(N) adds a 2-character error code (00H to 10H, 42H) to the "NAK" code and returns the "NAK" code to the external device and stores the error code (equivalent to QnA (extension) frame error code) to buffer memory address 25AH (CH1) or 26AH (CH2).
  The exact error contents can be checked by reading the value stored to the buffer memory.
  See Section 22.1.1 "QnA (extension) frame communications error code table" for a detailed description of the error codes.

22.1.3 Link dedicated instruction execution error code table

The following table lists the error codes, error contents, and corrective action for errors generated while a QnACPU is using a link dedicated instruction to communicate with other stations through a QC24(N). The error code is stored to the device designated by "End status" by send/receive instruction.

Error code (Hexadecimal)	Error contents	Corrective action
7E80H	A channel that is busy transmitting was used.	• Increase the time. • Check if local station/multiple stations issued multiple requests for the same target station channel.
7E81H	A busy channel was used.	• Increase the time. • Check if local station/multiple stations issued multiple requests for the same target station channel.
7E82H	Arrival monitoring time lapsed. (When number of retransmissions is 0.)	• If this error is generated in a RECV instruction, and another station can execute a SEND instruction, make the arrival monitoring time longer. • If local station is the instruction execution station, make the arrival monitoring time longer. If an error is still generated, check the network and target station.
7E83H	Communication was not made even if the designated number of retransmission was performed.	• Make the arrival monitoring time longer. If this error is still generated, check the network and target station.
7E85H	System error	(*1)
7E86H	Local station was designated the target station.	• Designate a target station No. other than local station No.
7E88H	System error	(*1)
7E89H		
7E8AH		
7EA0H	A number other than 0 is designated to the target station network No.	• Designate 0 to a target station network No.
7EA1H	Any other than 0 was specified for the target station No.	• Specify 0 for the target station No.
7EA2H	Transmission destination station No. error (Transmission destination station No. is outside the designated range.)	• Correct the transmission destination group No.
7EA4H	Transmission destination CPU error (Transmission destination hardware error)	• Check the transmission destination CPU.
7EA6H	Number of relay stations error (A transmission destination outside the relay range (8 stations or more) was designated.)	• Set a station within the relay range. Check the system.
7EA8H	Receiving network No. error (The receive network No. is incorrect.)	• Check the network No.
7EAAH	Response wait time-out	• Wait, then try again.

*1 Perform measures in the following procedures.

① Check that the QC24(N), power supply module, CPU module are properly installed on the base unit.

② Check that the operating environment of the QC24(N) is within the general specification of the CPU module.

③ Check that the power capacity is sufficient.

④ Check that the hardware of QC24(N), CPU module, and base unit is normal referring to a manual of each unit, or check operation by replacing a unit.
In case a fault is found, contact your local Mitsubishi representative to request repair.

⑤ If the above measures do not solve problems, consult your local Mitsubishi representative with detailed description on fault.

22.1.4 Error code list while modem function is used

The following table shows the error codes, description and corrective actions for errors (including errors at the abnormal completion) that may occur while the QC24N modem function is used.

The error codes for the modem function are stored in the modem function error code storage area (address : 221H(545)) of the buffer memory.

Error code (Hexadecimal)	Error	Error contents	Indicator LED	Corrective action	Reference section
7F25H	Data length error	The received "data length" has exceeded the receive area size.	CHn ERR.	• Correct the "data length" to be transmitted from the external device side. • Change the "word/byte unit" setting set by the QC24(N) to byte unit. • Increase the QC24(N)'s reception area.	
7F6BH	CD signal control error	When it is set to "perform CD terminal check," data was received while the CD signal is OFF.		• Review the CD signal control on the external device side. (Send while the CD signal is ON.) • Perform an exchange after setting "do not perform CD terminal check."	
7F6CH	Transmission error	Cannot transmit because the line is disconnected.		First perform line connection processing of the interface that uses the modem function, then start transmission.	
7FD0H	Modem function error	There is an error in the designation of the notification execution.		Set 0 to 1 to the notification execution designation.	Section 21.3.4
7FD1H		There is an error in the designation of the number of connection retries.		Set the number of connection retries in the range of 1 to 5.	
7FD2H		There is an error in the designation of the connection retry interval.		Set the connection retry interval in the range of 90 to 300 seconds.	
7FD3H		There is an error in the initialization/ connection time-out designation.		Set the initialization/connection time-out in the range of 1 to 60 seconds.	
7FD4H		There is an error in the designation of the number of initialization retries.		Set the number of initialization retries in the range of 1 to 5.	
7FD5H		There is an error in the designation of the data number for initialization.		Designate the registered data number for initialization, or set 0.	Section 21.3.4 Section 21.4.7
7FD6H		There is an error in the data for connection designated by the data number for connection.		Recheck the pager receiver designation.	Section 21.4.6
7FD7H				Recheck the dialing number of the external line.	
7FD8H				Recheck the telephone number designation.	
7FD9H		The line to the destination is being connected. Alternatively, modem initialization is not yet complete.		After completion of modem initialization, connect the line or notify when the line to the destination is not connected.	Section 21.4.8 Section 21.4.9
7FDAH		There is an error in the designation of the data number for connection.		Designate a registered number for the data for connection.	Section 21.3.4 Section 21.4.8
7FDBH		There is an error in the designation of the Q6TEL connection.		Set 0 to 1 to the Q6TEL connection designation.	Section 21.3.4
7FDCH		There is an error in the data for connection designated by the data number for connection.		Recheck the waiting time for the notification-message part of the message transmission.	Section 21.4.6
7FDDH		A connection time-out error occurred.		• Recheck the telephone number in the data for connection. • Check if the destination is ready for a connection. • Recheck the set value of the connection time-out. • Recheck the initialization command.	Section 21.3.4 Section 21.4.5 Section 21.4.6

Error code (Hexadecimal)	Error	Error contents	Indicator LED	Corrective action	Reference section
7FDEH	Modem function error	Connection to the modem/TA was unsuccessful, or the modem is not connected.		• Check if there is any problem with the modem/TA by seeing the operation manual of the modem/TA. • Connect the modem/TA to the QC24N. • Check the connection cable by seeing the operation manual of the modem/TA.	Section 21.2
7FDFH		Modem connection channel number is not designated.	—	Set 1 to 2 to the modem connection channel designation.	Section 21.3.4
7FE0H		Designated modem connection channel number is incorrect.			
7FE1H		There is an error in the designation of the user registration frame number.	CHn ERR.	• Recheck the user registration frame number. • Designate the registered user registration frame number. • Register the designated data for initialization.	Section 21.4.5 Section 21.4.6 Section 21.4.7
		There is an error in the designation of the output head pointer.		• Designate the output head pointer in the range of 1 to 100. • Designate the position (n-th position) where the data for initialization number is designated. • Designate the data for initialization number at the designated position (n-th position).	Section 21.4.7
7FE2H		There is an error in the designation of the output frame number.		Designate a registered data for initialization number within the range of the designated number of outputs from the location of the output head pointer.	Section 21.4.7
7FE3H		There is an error in the designation of the number of registered data bytes.		• Designate the data for initialization in the range of 1 to 78. • Designate 80 for the data for connection.	Section 21.4.5 Section 21.4.6
7FE4H		There is an error in the data for connection.		Recheck the message length of the message for notification.	Section 21.4.6
7FE5H		There is an error in the designation of the no-communication interval time.		Designate the no-communication interval time in the range of 0 to 120.	Section 21.3.4

22.2 Troubleshooting by Symptom

This section describes troubleshooting of trouble generated during communications between the QC24(N) and external device according to the trouble symptom.
When trouble occurs, first confirm the status of the QC24(N) and check the relevant item in the table below.

Symptom	Protocol			Reference section
	Dedicated	Non procedure	Bidirec-tional	
• "RUN" LED turned off.	○	○	○	22.2.1
• "RD" does not blink even through an external device is transmitting a message.	○	○	○	22.2.2
• An external device transmitted a message and "RD" blinked, but the QC24 did not return a response message.	○			22.2.3
• An external device transmitted a message and "RD" blinked, but the QC24 did not turn ON the read request.		○	○	22.2.4
• The "NAK" LED was turned ON.	○			22.2.5
• The "C/N" LED was turned ON.	○	○	○	22.2.6
• The "P/S" LED was turned ON.	○	○	○	22.2.7
• The "PRO" LED was turned ON.	○			22.2.8
• The "SIO" LED was turned ON.	○	○	○	22.2.9
• The "CH1 ERR." or "CH2 ERR." LED was turned ON.	○	○	○	22.2.10
• Communications are intermittently established and lost.	○	○	○	22.2.11
• Data that cannot be decoded was transmitted and received.	○	○	○	22.2.12
• Whether the cause of the communications error is in the QC24(N) or the external device is unknown.	○	○	○	22.2.13

* If an error occurs while performing data exchange using the modem function described in Chapter 21, first check the following items and confirm whether or not the error is caused by the modem/TA connection.

If an error relating to the modem function is occurring, perform necessary corrective actions for each cause according to the reference sections given below:

- Check the ON/OFF status of current I/O signals of QC24N. (See Section 21.3.3.)
- Check the storage status for error codes related to the modem function. (See Sections 21.3.4 and 22.1.4.)
- Check the ON/OFF status of the DR terminal of the modem/TA. (See Section 21.3.2 and the manual for the modem/TA.)

Remark

The following are precautionary notes when exchanging data with an external device via one of the QC24(N) interfaces.

(1) When the power supply to the QC24(N) or external device is started, the remote device that is connected may generate a reception error.

(2) If the remote device that is connected starts up while data is being transmitted, the remote device side will generate a reception error.

(3) When the QC24(N) error LED lights up because a reception error has occurred, turn off the light if necessary in accordance with Section 19.1.
Also, if a reception error has occurred on the external device side, handle the error by referring to the operating manual for the external device.

* Handle the occurrence of a reception error on the QC24(N) side using the following corrective actions.

- When communicating with the dedicated protocol
  The QC24(N) will disregard the received data or returns a response message indicating an abnormal termination if it detects a reception error after receiving the head data of the command message in the set format. If the reception error is detected before the head data of the command message in the set format is received, the received data will be disregarded.
- When communicating using non-procedure protocol
  If the QC24(N) detects a reception error, the abnormal reception detection signal (Xn4, XnB) turns ON.
  Perform procedures such as detection of reception error or clearing received data as required by following the explanations found in Sections 9.3.3, 9.3.4, 9.5 and 9.7.
- When communicating using bi-directional protocol
  When the QC24(N) detects a reception error after the head data of a communication message for bi-directional protocol is received, it returns a response message indicating an abnormal termination.
  If the reception error is detected before the head data of the communication message for bi-directional protocol is received, the received data will be disregarded.

22.2.1 Troubleshooting when "RUN" LED is turned OFF

Symptom	Cause	Corrective action	Dedicated	Bidirectional	Non procedure
• QC24(N) "RUN" LED turned off.	• A transmission specifications switch is set to an unusable position.	• Set the switch correctly and reset the CPU.	○	○	○
	• PLC CPU error.	• Remove the cause of the CPU error and reset the CPU. **Note** • During QC24(N) and external device loopback test, the minimum parameters file must be written to the CPU beforehand.	○	○	○
	• Power module 5V current capacity is insufficient.	• Calculate the 5V current drain of each installed module. If the current capacity is insufficient, check power module selection. **Note** • Whether or not the current capacity is insufficient can be checked by disconnecting the expansion base and installing only the QC24(N) to the basic base.	○	○	○
	• Extraneous noise caused the QC24(N) to abnormal operation.	• Check if the shield wire is 2-point ground. • When ground is used with other devices, ground the QC24(N) independently.	○	○	○

22.2.2 Troubleshooting when "RD" LED does not blink even through an external device is transmitting a message

Symptom	Cause	Corrective action	Dedicated	Bidirectional	Non procedure
• "RD" does not blink even through an external device is transmitting a message	• Signal lines are not connected correctly.	• Check if the QC24(N) and external RD and SD signal lines are cross connected. • Use the external device OPEN statement to check if the opened port and the cable connection port are matched.	○	○	○
	• External device transmission control signals are not turned ON.	• Connect the wiring so that the "DSR", "CS", and other transmission control signals are ready. **Note** • Since the control signal specifications depend on the device, connect the wiring by seeing the instruction manual of the device used.	○	○	○
	• If the message passes through an RS-232C ↔ RS-422 converter, modem, etc., the signal is interrupted at one of the intervening devices.	• Check the specifications of the converter and modem and recheck the settings and wiring	○	○	○

22.2.3 Troubleshooting when the QC24(N) does not return a response message even through an external device transmitted a message and the "RD" LED blinked

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• An external device transmitted a message and "RD" blinked, but the QC24(N) did not return a response message. ("NEU" remains on and "SD" does not blink)	• Mode switch is set incorrectly.	• Check if the mode switch dedicated protocol/non procedure protocol setting and format setting match. • Check if the mode was switched without using the buffer memory mode switching area. Note • The mode switch setting and current operation mode can be checked at buffer memory addresses 250H to (CH1) and 260H (CH2).	○		
	• When "Check CD terminal" is set, the CD terminal is turned OFF.	• Since the message is initialized when the CD terminal is turned OFF when "Check CD terminal" is set, change the wiring so that the CD terminal remains on all the time.	○		
	• The header byte of the message is not data needed by the set protocol and format.	• Check if the external device sent a message matched to the protocol and format. Note • The QC24(N) skips all the messages transmitted until the header byte set for each protocol and format (for example, "ENQ (05H)" for format 1) is received.	○		
	• QC24(N) station No. switch setting and message station No. designation do not match.	• Check the QC24(N) station No. switch setting and message station No. designation. Note • When the station No. designation is local station after the header byte set for each protocol and format is received, the QC24(N) performs receive processing.	○		
	• The QC24(N) data communications monitoring time is set to "infinite", or the monitoring time is too long.	• Set, or shorten, the monitoring time and retransmit the message from the external device and determine the trouble from the contents of the time-out error. Note • Error detection by watchdog timers (timer0 to timer2) is possible in the following cases. · When part of a message is skipped. · When transmission from an external device is interrupted. · When a link error was generated while accessing another station over a MELSECNET (/10, II). See Section 14.7 for a detailed description of the monitoring time.			

22.2.4 Troubleshooting when an external device transmitted a message and "RD" LED blinked, but the Read Request signal was not turned ON

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• An external device transmitted a message and "RD" blinked, but the read request signal (XnO) was not turned ON.	• Mode switch setting is incorrect.	• Check if the mode switch dedicated protocol/non procedure protocol setting and the format setting match. • Check that mode switching was not performed by using the buffer memory mode switching area. **Note** • The mode switch setting and current operating mode can be checked at buffer memory addresses 250H to (CH1) and 260H (CH2).		○	○
	• When "Check CD terminal" was set, the CD terminal was turned OFF.	• Since messages are skipped when the CD terminal is turned OFF when "Check CD terminal" is set, change the wiring so that the CD terminal remains on all the time.		○	○
	• When DC control is selected, the necessary DC codes are not transmitted.	• Check if a message is transmitted without transmitting "DC1 (11H)" after the external device transmits "DC3 (13H)" during DC1/DC3 external control. • Check if the next message is transmitted without adding "DC2 (12H)" after the external device transmits "DC4 (14H)" during DC2/DC4 control.		○	○
	• The end code was not received, or fixed length data was not received.	• Check if the end code set at the QC24(N) and the end code transmitted from the external device are the same. • Check if the external device transmitted the fixed length designated at the QC24(N). • Check if the trailer frame was transmitted during communications by user frame. **Note** • When the send data from the external device is correct, take the corrective action described in Sections 22.2.10 and 22.2.12.		○	○
	• QC24(N) setting and message format do not match.	• The data count basics, message format, etc. depend on the following settings. · ASCII-BIN conversion enable/disable · Transparent code setting · User frame setting See the relevant section for a description of operation according to the set contents and setting of each item.		○	○
	• The QC24(N) data communications monitoring time is set to "infinite", or the monitoring time is too long.	• Set, or shorten, the monitoring time and retransmit the message from the external device and determine the trouble from the contents of the time-out error. **Note** • Error can be detected with the watchdog timer (timer0 to timer2) in the following cases. · When part of a message is skipped. · When transmission from an external device is interrupted. · When a link error was generated when another station was accessed over a MELSECNET (/10, II). See Section 14.7 for a detailed description of the monitoring time.			

22.2.5 Troubleshooting when "NAK" LED turned on

<table>
<tr><th>Symptom</th><th>Cause</th><th>Corrective action</th><th>Dedicated</th><th>Bidirec-tional</th><th>Non procedure</th></tr>
<tr><td rowspan="2">"NAK" LED turned on.</td><td>• See section that describes the error LED ("C/N", "P/S", "PRO", "SIO") that are turned on simultaneously when the "NAK" LED is turned on.</td><td>Take corrective action corresponding to the contents of the error.</td><td>○</td><td></td><td></td></tr>
<tr><td colspan="5">Note
Since the error code is added to "NAK" and is transmitted from the QC24(N) to the external device when the "NAK" LED is turned on, take the corrective action described in the error code table (see Section 22.2).
Since the error code added when "NAK" is transmitted is stored to the QC24(N) buffer memory shown below, it can also be checked at the QC24(N).<table><tr><th colspan="2">Error code storage buffer memory address</th></tr><tr><td>CH1</td><td>25AH</td></tr><tr><td>CH2</td><td>26AH</td></tr></table></td></tr>
</table>

22.2.6 Troubleshooting when "C/N" LED turned on

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
"C/N" error LED turned on.	• QC24(N) cannot be installed in the CPU.	• Change to a CPU to which the QC24(N) can be installed.	○	○	○
	• PLC No. designated local station (FF), or a station other than a station No. set with the network parameters.	• Change the PLC No. to local station (FF), or a station No. set with the network parameter and restart data communications.	○		
	• Routing parameters between QC24(N) CPU and communications destination CPU are not set.	• Check the routing parameters and set them up to the communications destination CPU.	○		
	• An error was generated on the MELSECNET/10.	• Check the error contents from the state of SB and SW related to the MELSECNET with the GPP function peripheral device monitor, etc. and perform the checks and take the corrective action described in the MELSECNET/10 reference manual.	○		
	• The local station CPU on the MELSECNET/10 generated an error.				
	• Module installation address designation during communications with special function module is incorrect.	• Change the transmit message designation data.	○	○	○
	• A command that cannot be transmitted during RUN (sequence program, parameters, etc.) was transmitted, or "Disable write during RUN" is set.	• Stop the CPU and restart data communications.	○		
		• Set the "Enable/disable write during RUN" switch to "Enable" by command.	○		

22.2.7 Troubleshooting when "P/S" LED turned on

Symptom	Cause	Corrective action	Dedicated	Bidirectional	Non procedure
• "P/S" error LED turned on.	• Data does not match the parity bit setting.	• Check the QC24(N) and external device data format and match the settings.	○	○	○
	• Sum check codes do not match.	• Check if the sum check code transmitted from the external device is correct. (Recalculate)	○		
	• When CH1 and CH2 are used in the linked mode, the cable is not connected to one of the interface.	• When using CH1 and CH2 independently, check that the QC24(N) is not in the linked mode. • When using CH1 and CH2 in the linked mode, also connect the cable to CH2. **Note** If the cable is not connected to one of the interfaces when CH1 and CH2 are used in the linked mode, noise may enter and the data may be destroyed and "Data cannot be decoded" or "Communications error cause" may occur.	○	○	○

22.2.8 Troubleshooting when “PRO.” LED turned on

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• “PRO” error LED turned on.	• Communications were performed with a control procedure different from the QC24(N) mode setting.	• Check the QC24(N) mode setting and the message from the external device and match the settings, or correct the message and restart data communications.	○		
	• Some of the messages are different from the control procedure.				
	• Designated command does not exist.				
	• The device No. designation is not the character count corresponding to the command.				
	• The characters in the message include a code other than the “A to Z”, “0 to 9”, “␣“, and control codes.	• Check and correct the external device message and restart data communications. **Note** Only the codes “0 to 9” and “A to F” are handled as character area codes during communications using a dedicated protocol (ASCII mode). Therefore, when transmitting a character string as data, convert the ASCII code of the character string to 2-byte binary code. Examples) · Transmitting the character “G” The ASCII code for the character “G” is 47H and is transmitted as the two bytes 34H, 37H. · Transmitting the character “A” The ASCII code for “A” is 41H and is transmitted as the two bytes 34H, 31H. (If the ASCII code 41H for the character “A” is transmitted unchanged, QC24(N) ASCII↔BIN conversion will convert it to HA (K0) and pass it to the CPU.)	○		
	• A device No. outside the designated range was designated.	• When designating a device, check “Device setting” of the parameters written to the CPU and correct it to a device No. within the designated range and restart data communications.	○		
	• A remote RUN/STOP request was issued while remote STOP was applied from another module.	• Check if remote STOP is applied from another module and restart data communications.	○		

22.2.9 Troubleshooting when "SIO" LED turned on

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• "SIO" error LED turned on.	• Data does not match the stop bit setting.	• Check if the QC24(N) and external device settings are the same.	○	○	○
	• Transmission rate is too fast and the next data is transmitted before the QC24(N) completes processing of the receive data.	• Decrease the transmission rate and restart data communications.	○	○	○
	• Data larger than the receive buffer size was received.	• Use DTR and DC control and interrupt transmission before the buffer becomes full. Perform RS · CS control when the modem function is used. • Increase the transmission interval and provide an ample CPU read processing time. **Note** • The non procedure protocol stores the data received up to first the end code received, or fixed length data, to the non procedure receive buffer memory and turns on the Read Request signal to the CPU. If the next data is sent while the Read Request signal is ON, the data is temporarily stored to the OS receive buffer. When the OS receive buffer becomes full, the QC24(N) skips the rest of the data and turns on the "SIO" LED.		○	○
	• With a multidrop link, the external device and CPU transmitted data at the same time.	• Connect the external devices and QC24(N) in a 1:1 configuration and perform a communications test. Since data is transmitted simultaneously when normal communications among all the devices is possible, interlock the devices so that cannot transmit simultaneously.	○	○	○

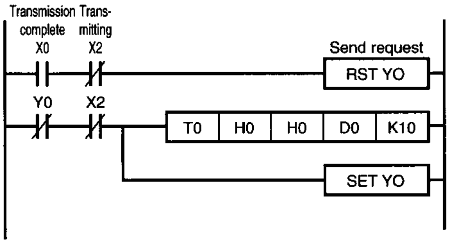
22.2.10 Troubleshooting when "CH1 ERR.", "CH2 ERR." LED turned on

<table>
<tr><th>Symptom</th><th>Cause</th><th>Corrective action</th><th>Dedicated</th><th>Bidirec-tional</th><th>Non procedure</th></tr>
<tr><td rowspan="6">• "CH1 ERR.", "CH2 ERR." error LED turned on.</td><td>• There is an error in the mode switch or transmission specifications switch setting.</td><td>• Read the error code from the buffer memory and check the error contents and change the switch setting to the correct setting.</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>• There is an error in the on-line mode switching designation.</td><td>• Read the error code from the buffer memory and check the error contents and correct the designation contents.</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>• On-demand execution generated an error.</td><td>• Read the error code from the buffer memory and check the error contents and correct the designation contents.</td><td>○</td><td></td><td></td></tr>
<tr><td>• The QC24(N) detected an error while transmitting data.</td><td>• Read the error code from the buffer memory and take the corrective action corresponding to the error contents.</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>• The QC24(N) detected an error while receiving data.</td><td>• Read the error code from the buffer memory and take the corrective action corresponding to the error contents.</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td colspan="5">Note
• When the "CH1 ERR." or "CH2 ERR." error LED is turned on, the error code is stored to the following buffer memory.
<table>
<tr><th rowspan="3">Error cause</th><th colspan="3">Error code storage buffer memory</th></tr>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th></tr>
<tr><th>CH1</th><th>CH2</th></tr>
<tr><td>Switch setting error</td><td colspan="2" rowspan="2">203H</td><td rowspan="2">Switch setting error, mode switching error storage area</td></tr>
<tr><td>Mode switching error</td></tr>
<tr><td>On-demand execution error</td><td>256H</td><td>266H</td><td>On-demand execution result storage area</td></tr>
<tr><td>Data transmission error</td><td>257H</td><td>267H</td><td>Data transmission result storage area</td></tr>
<tr><td>Data receive error</td><td>258H</td><td>268H</td><td>Data receive result storage area</td></tr>
<tr><td>Modem function error</td><td colspan="2">221H</td><td>Modem function error code storage area</td></tr>
</table>
* See Section 22.1 for a detailed description of the error codes.</td></tr>
</table>

22.2.11 Troubleshooting when "SW.ERR." LED turned on

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• "SW.ERR." error LED turned on.	• There is a switch setting error.	• Reset the CPU after correctly setting the mode settings switch, transmission specifications setting switch, and station No. setting switch.	○	○	○
	• This is a station that is not installed in the QC24(N).	• Install the QC24(N) in the QnACPU station or the MELSECNET/10 remote station.	○	○	○

22.2.12 Troubleshooting when communications is intermittently established and lost

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• Communications are intermittently established and lost.(*1)	• With a multidrop link, data was transmitted simultaneously from an external device or CPU.	• Connect the external devices and QC24(N) in a 1:1 configuration and perform a communications test. Since data is transmitted simultaneously when normal communications among all the devices is possible, interlock the external devices so that they do not transmit simultaneously.	o	o	o
	• The signal cable wiring connection is faulty.	• Replace the cable, or make the connections firm.	o	o	o
	• When "Check CD terminal" is set, the CD signal is turned ON/OFF repeatedly.	• Change the wiring so that the CD signal remains ON all the time, or change the setting to "Do not check CD terminal".	o	o	o
	• When half-duplex communications is selected, the ON/OFF timing of each signal is not matched.	• Control the external device so that the ON/OFF timing of each signal (see Section 14.5.2) is matched.		o	o
	• Program the sequence program to leave the QC24(N) I/O signals ON or OFF all the time.	• Program handshake positively in the sequence program. **Note** • The following is a sample sequence program that leaves the QC24(N) I/O signals ON or OFF all the time.  Since the send request signal Y0 is switched from OFF to ON within the same scan in the program above, END refresh is executed when the signal is "ON". Therefore, since transmission complete X0 OFF processing is not executed, the next data is not transmitted.	o	o	o

*1 The following explains how to take corrective actions when a normal exit response message cannot be received upon sending of a command message.

(a) When a response message of abnormal end is received
  1) When an external device sent a command message and received an abnormal end response message, take corrective action with the error according to the error code in the response message (see Section 22.1).
  2) When the following problem occurs at the time of access to other station CPU, clear the PLC CPU information and retry. (Refer to Section 19.6)
    - Accessible device range is narrowed. (Error code: 7140H)
    - Some of commands and/or devices cannot be used.
    (Error code: 7142H, 714DH)

(b) When response messages cannot be received
Change the setting value for the response monitoring time (timer 1, default value is 5 seconds).
(Refer to Section 14.7.2.)
If response messages still cannot be received after changing the setting value, check the communication protocol setting of the corresponding interface, the ON status of the displayed LED, and the connection cable.

(c) When the first part of a response message cannot be received
Increase the setting value of the message wait time (the default value is 0 ms).
(Refer to Section 14.7.2)
If response messages still cannot be received after increasing the setting value, it is necessary to reduce the processing time from the end of transmission processing to the start of reception processing on the external device side.

22.2.13 Troubleshooting when data that cannot be decoded is transmitted and received

Symptom	Cause	Corrective action	Dedicated	Bidirec-tional	Non procedure
• Data that cannot be decoded was transmitted and received	• With a multidrop link, data was transmitted simultaneously from an external device or the CPU.	• Connect the external devices and QC24(N) in a 1:1 configuration and perform a communications test. Since data is transmitted simultaneously when normal data communications among external devices is possible, interlock the external devices so that they do not transmit simultaneously.	○	○	○
	• Data does not match the parity bit setting.	• Match the QC24(N) and external device parity bit settings. **Note** • With the non procedure protocol, if the setting of one side is data bit length 7 bits and parity and the setting of the other side is data length 8 bits and no parity, the number of send/receive bits will be the same and the data will sent and received without generating an error.	○	○	○
	• The stop bit length settings do not match.	• Match the QC24(N) and external device number of stop bits setting. **Note** • With the non procedure protocol, if the setting of one side is data length 7 bits and stop bit 2 bits and the setting of the other side is data length 8 bits and stop bit 1 bit, the number of send/receive bits will be the same and the data will be transmitted and received without generating an error.	○	○	○
	• Transmission rate settings do not match.	• Match the QC24(N) and external device transmission rates.	○	○	○
	• With a multidrop link, the terminating resistor is not connected correctly.	• Check if the same resistance value (110Ω or 330Ω is connected to the stations at both ends of the link.	○	○	○
	• When CH1 and CH2 are used to the linked mode, the cable is not connected to one of the interfaces.	• When using CH1 and CH2 independently, check that the QC24(N) is not in the linked mode. • When using CH1 and CH2 in the linked mode, also connect the cable to 2CH. **Note** • If the cable is not connected to one of the interfaces when CH1 and CH2 are used in the linked mode, noise may enter and destroy the data and "Data cannot be decoded" or "Communication error cause" may occur.	○	○	○

22.2.14 Troubleshooting when whether the communication error cause is in the QC24(N) or an external device is unclear

Symptom	Cause	Corrective action	Dedicated	Bidirectional	Non procedure
• Whether the communications error cause is in the QC24(N) or an external device is unclear.	——	• Test the QC24(N) as described below to check where the cause is. ① Check the hardware. · The QC24(N) must be installed firmly. · The module pins must not be bent or otherwise abnormal. ② Test the QC24(N) alone. (See Section 4.6.) · ROM/RAM/switch test must not generate any errors. · Self loopback test must not generate any errors. ③ Check the state of the CPU. · There must not be any errors that stop CPU operation. **Note** • The following methods are available for testing if normal communications are possible with the QC24(N) alone. ① With one QC24(N), set CH1 and CH2 to the non procedure protocol and connect the wiring the same as for the self loopback test and transmit data from one channel and receive the transmitted data at the other channel. If the transmitted data and the received data are the same, transmit and receive processing is performed normally. ② When two QC24(N) are available, set one QC24(N) to the non procedure protocol and the other QC24(N) to a dedicated protocol and transmit a dedicated protocol message from the non procedure protocol station. If the dedicated protocol station returns the transmit message normally, transmit and receive processing is normal. This test can be performed even when there is only one QC24(N), but except for the QC24(N)-R4, an RS-232↔RS-422 converter is necessary.	○	○	○

APPENDICES

Appendix 1 Use of Previous Products Module Program and Incorporation of QC24(N) into an Existing System

Appendix 1.1 Use of computer link module program and incorporation into an existing system

Appendix 1.1.1 Use of computer link module program

Data communications and transmission control with external devices the same as those of a computer link module can also be realized with the QC24(N).
The following outlines use of a sequence program and computer program written for a computer link module with the QC24(N).

POINT

When the QC24(N) functions equivalent to the computer link module are used, there are the following major differences.
When using a computer link module program as the QC24(N) program, the parts related to these differences must be changed.

(1) QC24(N) buffer memory addresses and special applications area initialization items
(2) QC24(N) I/O signals for handshake
(3) PLC CPU dedicated instructions

1 **Initialization to buffer memory special applications area**

① The QC24(N) buffer memory special applications area addresses are different from those of the computer link module and the number of initialization items increases.
② Program the initialization sequence program of the necessary part as described in Chapter 14.
③ Change the CD terminal check setting default value to [Do not check].

2 **Data communications using a dedicated protocol**

(a) Mode switch setting

Data communications can be performed by setting the operation mode of the interfaces of a QC24(N) connected to an external device to the same format set in the mode switch of the computer link module.

(b) Command message and response message

① The messages that communicate data using the QC24(N) ASCII mode A compatible frame are the same as the computer link module messages.
② Before accessing the PLC CPU from an external device, check which commands can be used and the devices that can be accessed as described in Section 5.4.3. The PLC CPU device memory can be accessed.
The computer link/multidrop link module user's manual (computer link function, printer function) is necessary.
③ When you must access functions other than the those described in Sections 5.4.3, program a new external device program as described in Chapters 6 and 8.

(c) Other station access

① The method of accessing another station's PLC CPU over an MELSECNET/10 is different from that of the computer link module.
② When another station must be accessed, QnA (extension) frame communications must be used. Program a new external device program as described in Chapter 6.

(d) Data transmission to external device by on-demand function

① The PLC CPU program when transmitting data from PLC CPU to external device is different from that of the computer link module.
Transmit the data as described in Section 6.9.

② The data transmitted to external devices is the same as that of the computer link module.

3 **Data communication using the non procedure protocol**

(a) Data transmission and reception

① Data can be transmitted and received the same with as the computer link module.

② Before communicating data with the PLC CPU, check the QC24(N) functions, buffer memory used, and I/O signals according to Chapters 9 and 10.

③ When the PLC CPU receives data by QC24(N) default end code, the external device must transmit CR+LF (code: 0DH, 0AH) at the end of the data transmitted to the QC24(N).
When the PLC CPU receives data by arbitrary end code set at the QC24(N), data can be transmitted the same as with the computer link module.
Data reception from the QC24(N) is the same as with the computer link module.

(b) Message transmission by printer function

① Message transmission by computer link module printer function can be realized with the user frame data transmission function.

② Write and transmit messages at the PLC CPU as described in Chapters 9, 11, and 16.
With the QC24(N), the messages handled by the computer link module become user frames.

- Chapter 9 ..... Section 9.4.1 2 (b) describes the send data designation method, etc.
  Section 9.6.2 1 describes the buffer memory of the QC24(N) used.
- Chapter 11 ... Describes user frame data communications.
  Section 11.4 describes the transmission method.
- Chapter 16 ... Describes how to write user frames.

4 **Data communications using the bidirectional protocol**

(a) Setting to add sum check code to message

The setting for adding a sum check code to a message is different.

- Computer link module ..... Set by buffer memory.
- QC24(N) .... Set by transmission specifications switch (SW06).

(b) Data transmission/reception

① Data can be transmitted and received the same as with the computer link module.

② Before transmitting and receiving data with the PLC CPU, check the QC24(N) functions, buffer memory used, and I/O signals according to Chapters 12 and 13.

③ External devices can transmit and receive data the same as with the computer link module.

5 **Others**

① Except for the above, the QC24(N) has the same functions as the computer link module.

② Use the relevant functions as described in the section that covers each function.

(Examples)

- Communicating data by switching from DTR/DSR control to DC code control.... See Section 14.3.
- Communicating data by switching from full-duplex communications to half-duplex communications....See Section 14.5.
- Switching the QC24(N) mode....See Chapter 18.
- Reading the QC24(N) status and signal status after the start of data communications....See Chapter 19.

Appendix 1.1.2 Incorporating the QC24(N) into an existing system

The following describes the precautions which should be observed when incorporating the QC24(N) into a system that uses a computer link module (AJ71UC24, etc.).

1 m: n data communications

The following describes the precautions which should be observed when incorporating the QC24(N) into a system in which the external devices and PLC CPU system configuration is m: n and communicating data using a dedicated protocol.

(a) Access to PLC by binary mode

When the computer link module is connected to the line, the binary mode cannot access the PLC.

(b) Data communications between external devices

① When data communications between external devices interlocks the external devices so that data that 1:1 communications between external device and PLC CPU is possible, the external device station Nos. designated by the [station No.] and [local station No.] items in the message must be changed (80H→00H to 1FH).
It may also be necessary to make the data contents a message structure different from the dedicated protocol.

② Correspond with Section 17.2.2.

- Station No .... Designates the station No. of the transmission destination external device.
- Local station No .. Designates the station No. of the transmission source external device.
  (When A compatible frame is used, designation is unnecessary.)

(c) External device receive processing

Ignore messages transmitted and received with the link dedicated instructions described in Chapter 20, QC24(N) linked operation messages described in Section 4.3.1 *2, and messages other than those shown below, even if they are received at an external device.

- Response message transmitted in reply to a command message transmitted when a dedicated protocol is used to access the PLC CPU.
- Messages transmitted during access between external devices.

2 1: n configuration data communications

When the computer link module is connected to a line to which the external devices and PLC CPU are connected in 1: n system configuration, the binary mode cannot access the PLC.

POINT

The communication might not work correctly when the module is simply replaced, because the performance and the response speed of the QC24(N) and the computer link module are different. Be sure to check to see the normal operation when the module is replaced.

Appendix 1.2 Use of QC24 program and incorporation into an existing system

Appendix 1.2.1 Use of QC24 program

Data communication between the QnACPU and the external device, or between the QnACPUs which was executed by the QC24 can also be executed by the QC24N.

In the following section, the use of programs were designed for QC24 for the data communication with the QC24N is described.

1 **Communication programs for QC24 on the external device end and on the QnACPU (local station) end of the QC24 installed station can be utilized for QC24N.**

2 **Because internal processing speed of QC24N has been improved, the time required by QC24N for an access processing to the PLC CPU and message transmission processing to external device will be shorter than the time required by QC24. (How to use the function is the same, but the performance and response speed are different between QC24N and QC24.) When utilizing the existing QC24 communication program on the external device or on the QnACPU (local station) end, it may be required to adjust the communication timing by conducting an operation check.**

(Example of communication timing adjustment)

(a) When communicating by dedicated protocol
Increase the message wait time. Particularly, adjustment is necessary when “Scanning time of the QC24N installed station > Message wait time.”

If the message wait time is too short, the external device may not be able to receive all or the first part of a response message from the Q series C24.

① When communication is performed with the QnA frame or QnA extension frame, designate in the QC24N buffer memory (at address 11EH/1BEH).

② When communication is performed with the A compatible frame, designate in the request message transmitted from the external device.

(b) When communicating by the non procedure protocol or bidirectional protocol
Delay the data transmission timing.

- Data transmission from external device to QC24N

  Delay the data transmission timing from the external device. (Adjust on the external device end.)

- Data transmission from QC24N to external device

  When communication is performed by the non procedure protocol, delay the data transmission, controlled by the sequence program, from QC24N to external device by one scan. (When communication is performed by the bidirectional protocol, delay the timing to turn on the reception data read complete signal by one scan.)

3 **The same precautions as ones for data communication via RS-422 and RS- 422/485 interface, shown in section 3.3.3, are also applied to QC24N.**

- Countermeasures for receiving wrong data on the external device end
- Operation of the RS-422/485 interface on the QC24(N) end

4 **To execute the data communication using the functions added in QC24N (See Section 1.4), create a new program.**

Appendix 1.2.2 Incorporation of QC24N into an existing system

Incorporation of a QC24N on an existing system is described.

1 Incorporating on a multi-drop connection system

The QC24N can be incorporated on an existing system to which external devices and the PLC CPU are connected as 1:n or m:n multi-drop connection (*1).

*1 This is when the QC24 or a computer link module (such as AJ71UC24) is used as the PLC CPU module of the multi-drop connection.

2 Replacing the QC24 module with a QC24N

The QC24 can be replaced with the QC24N module, and the wiring used by the QC24 can be used as is.

POINT

For all serial communication modules discussed in this manual, all the functions can be used exactly in the same manner except for the functions that have been added to QC24N since QC24. However, the communication might not work correctly when the module is simply replaced, because the performance and the response speed of the QC24N and the QC24 are different.
Be sure to check to see the normal operation when the module is replaced.

Appendix 1.3 Precautions when replacing an old model with A1SJ71QC24N1(-R2)

The following explains precautions when replacing QC24N with A1SJ71QC24N1(-R2)

Refer to Appendix 1.1 and Appendix 1.2 for precautions when replacing a computer link module and QC24.

1 Speed up of internal processing

Faster internal processing shortens the access processing of A1SJ71QC24N1(-R2) to the PLC CPU and transmission processing time to the external device than the QC24N.

(Although the method to use function is the same, performance and response speed differ between the A1SJ71QC24N1(-R2) and QC24N.)

When utilizing a communication program for the QC24N on the external device and QnACPU (host) side, adjustment of communication timing may be necessary at operating check.

For adjustment procedure of communication timing, refer to section (2) of Appendix 1.2.1.

2 Delay in writing time to EEPROM

Writing time of the A1SJ71QC24N1(-R2) EEPROM is longer as compared to the QC24N.

(example) Processing time when 40 byte data is registered to EEPROM using PUTE instruction

· A1SJ71QC24N1(-R2) : 913ms

· QC24N other than the above : 102ms

3 When "RS-232C communication system specification" is set to half-duplex communication and "RS-232C CD terminal checking specification" is selected

The CD terminal checking functions of the A1SJ71QC24N1(-R2) are improved compared with those of the QC24N.

When data cannot be received, check the CD signal wiring again, and then change the setting as mentioned below.

· RS-232C communication system specification : Full-duplex communication
(Set 0 to buffer memory 98H.)

· RS-232C CD terminal checking specification : Do not select. (Set 1 to buffer memory 97H.)

When "RS-232C communication system specification" is set to half-duplex communication, the operation of the A1SJ71QC24N1(-R2) at data receive differs from that of the QC24N as mentioned below.

(a) A1SJ71QC24N1(-R2)
When the CD signal is OFF, the A1SJ71QC24N1(-R2) discards receive data from external devices.

When data are being sent from the A1SJ71QC24N1(-R2) with "Prioritize/not prioritize specification at simultaneous sending" being set to prioritize the sending, the A1SJ71QC24N1(-R2) discards receive data regardless of the CD signal ON/OFF status.

(b) QC24N
The QC24N receives receive data regardless of the CD signal ON/OFF status.

When data are being sent from the QC24N, the QC24N receives receive data regardless of the "Prioritize/not prioritize specification at simultaneous sending" status and the CD signal ON/OFF status.

POINT

Function and response speed differ between the A1SJ71QC24N1(-R2) and QC24N.
Always check operation after replacing a module.

Appendix 2 ASCII-Code Table

The ASCII-code table is shown below. (7-bit code)
The codes 00H to 1FH indicated by the ★ are used as QC24(N) control codes. (DC codes 11H to 14H can be changed by the user.)

	MSD	0	1	2	3	4	5	6	7
LSD		000	001	010	011	100	101	110	111
0	0000	NUL ★	DLE ★	SP	0	@	P	`	p
1	0001	SOH	DC1 ★	!	1	A	Q	a	q
2	0010	STX ★	DC2 ★	"	2	B	R	b	r
3	0011	ETX ★	DC3 ★	#	3	C	S	c	s
4	0100	EOT ★	DC4 ★	$	4	D	T	d	t
5	0101	ENQ ★	NAK ★	%	5	E	U	e	u
6	0110	ACK ★	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	/	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
A	1010	LF ★	SUB	*	:	J	Z	j	z
B	1011	VT	ESC	+	;	K	[	k	{
C	1100	FF ★	FS	,	<	L	\	l	|
D	1101	CR ★	GS	—	=	M	]	m	}
E	1110	SO	RS	.	>	N	↑	n	to
F	1111	SI	VS	\	?	O	←	o	DEL

Appendix 3 Processing Time

Appendix 3.1 PLC CPU communications time (Scan time increase)

When the PLC CPU is in the RUN state, it processes the number of processing points per communication (see Section 5.4) each time it executes an END instruction for requests sent from the QC24(N) by dedicated protocol.

The intervening time to the scan time and the number of scans required by processing at this time are shown below.

1 QnA (extension) frame command

<table>
<tr><th rowspan="3" colspan="4">Item</th><th rowspan="3">Com-mand</th><th rowspan="3">Sub-command</th><th colspan="3">Intervening time [ms] (Scan time increase)</th><th colspan="4">Number of scans required for processing</th></tr>
<tr><th colspan="2">Q3ACPU (When A38B used)</th><th rowspan="2">Number of access points ① / ②</th><th colspan="2" rowspan="2">When [Enable during RUN] set</th><th colspan="2" rowspan="2">When [Disable during RUN] set</th></tr>
<tr><th>Number of access points: ①</th><th>Number of access points: ②</th></tr>
<tr><td rowspan="15">Device memory</td><td colspan="2" rowspan="2">Batch read</td><td>Bit units</td><td rowspan="2">0401</td><td>0001</td><td>1.068</td><td>2.428</td><td>1/3952</td><td colspan="4">1</td></tr>
<tr><td>Word units</td><td>0000</td><td>0.996</td><td>3.168</td><td>1/480</td><td colspan="4">1</td></tr>
<tr><td colspan="2" rowspan="2">Batch write</td><td>Bit units</td><td rowspan="2">1401</td><td>0001</td><td>1.008</td><td>2.428</td><td>1/3952</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td>Word units</td><td>0000</td><td>0.996</td><td>3.196</td><td>1/480</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td colspan="2" rowspan="2">Random read</td><td rowspan="2">Word units</td><td rowspan="2">0403</td><td>0040</td><td>1.304</td><td>6.976</td><td rowspan="2">1/96</td><td colspan="2">3</td><td colspan="2">4</td></tr>
<tr><td>0000</td><td>1.272</td><td>7.256</td><td colspan="2">2</td><td colspan="2">3</td></tr>
<tr><td colspan="2" rowspan="2">Test
[Random write]</td><td>Bit units</td><td rowspan="2">1402</td><td>0001</td><td>1.240</td><td>9.160</td><td>1/94</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td>Word units</td><td>0000</td><td>1.156</td><td>6.764</td><td>1/80</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td colspan="2" rowspan="2">Monitor data registration</td><td rowspan="2">Word units</td><td rowspan="2">0801</td><td>0040</td><td>0.980</td><td>0.990</td><td rowspan="2">1/96</td><td colspan="4" rowspan="2">1</td></tr>
<tr><td>0000</td><td>0.948</td><td>0.950</td></tr>
<tr><td rowspan="3">Monitor</td><td>With condition</td><td rowspan="3">Word units</td><td rowspan="3">0802</td><td rowspan="3">0000</td><td>1.320</td><td>6.932</td><td rowspan="3">1/96</td><td colspan="2">Monitor condition</td><td colspan="2">Monitor condition</td></tr>
<tr><td rowspan="2">Without condition</td><td rowspan="2">1.212</td><td rowspan="2">7.256</td><td>YES</td><td>NO</td><td>YES</td><td>NO</td></tr>
<tr><td>2</td><td>1</td><td>2</td><td>1</td></tr>
<tr><td colspan="2">Multiple block batch read</td><td>Word units</td><td>0406</td><td>0000</td><td>1. 250</td><td>16.400</td><td>1/480
(*1)</td><td colspan="4">1</td></tr>
<tr><td colspan="2">Multiple block batch write</td><td>Word units</td><td>1406</td><td>0000</td><td>1. 280</td><td>13.460</td><td>1/480
(*1)</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td rowspan="2">Buffer memory</td><td colspan="3">Batch read</td><td>0613</td><td>0000</td><td colspan="2" rowspan="2">——</td><td rowspan="2">—</td><td colspan="4" rowspan="2">——</td></tr>
<tr><td colspan="3">Batch write</td><td>1613</td><td>0000</td></tr>
<tr><td rowspan="5">PLC CPU</td><td colspan="3">Remote RUN</td><td>1001</td><td>0000</td><td colspan="2">—</td><td rowspan="5">—</td><td colspan="4">1</td></tr>
<tr><td colspan="3">Remote STOP</td><td>1002</td><td>0000</td><td colspan="2">—</td><td colspan="4">1</td></tr>
<tr><td colspan="3">Remote PAUSE</td><td>1003</td><td>0000</td><td colspan="2">—</td><td colspan="4">1</td></tr>
<tr><td colspan="3">Remote latch clear</td><td>1005</td><td>0000</td><td colspan="2">—</td><td colspan="4">1</td></tr>
<tr><td colspan="3">Remote RESET</td><td>1006</td><td>0000</td><td colspan="2">—</td><td colspan="4">1</td></tr>
<tr><td rowspan="2">Drive memory</td><td colspan="3">Memory usage state read</td><td>0205</td><td>0000</td><td>1.072</td><td>2.480</td><td>1/256</td><td colspan="4">1</td></tr>
<tr><td colspan="3">Memory optimization</td><td>1207</td><td>0000</td><td colspan="2">—</td><td>—</td><td colspan="2">1</td><td colspan="2">2</td></tr>
</table>

*1 Number of blocks ① = 1, Number of blocks ② = 120

*2 Number of blocks ① = 1, Number of blocks ② = 96

Item			Command	Sub-command	Intervening time [ms] (Scan time increase)			Number of scans required for processing			
					Q3ACPU (When A38B used)		Number of access points ①/②	When [Enable during RUN] set		When [Disable during RUN] set	
					Number of access points: ①	Number of access points: ②		File No. designation		File No. designation	
								FFFFH	YES	FFFFH	YES
File	File information table read	Without header statement	0201	0000	1.104	3. 324	1/36	1			
		With header statement	0202	0000	1.192	4.132	1/16	1			
		File No. Usage State	0204	0000	1. 376		1	1			
	File information modifica-tion	Date of last updating	1204	0000	1.136		1	2	1	3	2
		File name size modification		0001	1.252		1	2	1	3	2
		Batch modification		0002	1.196		1	2	1	3	2
	File search		0203	0000	1.020		1	1			
	File contents read		0206	0000	1.164	3.228	1/960	2	1	2	1
	File creation (File name register)		1202	0000	1.376		1	1		2	
	File contents write	Arbitrary data	1203	0000	1.168	3.296	1/960	2	1	3	2
		Same data (FILL)		0001	1.200	1.336	1/960	2	1	3	2
	File lock register/clear		0808	0001	0. 996		1	2	1	3	2
				0000	1.000						
	File copy		1206	0000	1.388	1.540	1/480	1 only 2 Both 3	1	1 only 3 Both 4	2
	File delete		1205	0000	1.152		1	2	1	3	2
User entry frame	Entry data read		0610	0000	——		—	——			
	Data entry		1610	0000							
	Entry data delete			0001							
Global			1618	000□	——		—	——			
On-demand			2101	—	——		—	——			
Transmission sequence initialize (Usable in binary mode only)			1615	0000	——		—	——			
Mode switching			1612	0000							
LED OFF, error code initialize			1617	000□							
Loopback test			0619	0000							

2 A compatible frame command

Item			Command	Intervening time [ms] (Scan time increase)			Number of scans required for processing	
				Q3ACPU (When A38B used)		Number of access points ①/②	When [Enable during RUN] set	When [Disable during RUN] set
				Number of access points: ①	Number of access points: ②			
Device memory	Batch read	Bit units	BR	1.028	1.116	1/256	1	
			JR	1.032	1.132			
		Word units	WR	1.012	1.192	1/32	1	
			QR	1.040	1.128			
	Batch write	Bit units	BW	1.032	1.096	1/160	1	2
			JW	1.072	1.144			
		Word units	WW	1.024	1.104	1/10	1	2
			QW	1.028	1.044			
	Test (Random write)	Bit units	BT	1.260	2.876	1/20	1	2
			JT	1.220	2.876			
		Word units	WT	1.232	1.876	1/10	1	2
			QT	1.224	1.844			
	Monitor data registration	Bit units	BM JM	——		—	0	
		Word units	WM QM					
	Monitor	Bit units	MB	1.260	2.388	1/20	1	
			MJ	1.312	2.488			
		Word units	MN	1.260	2.452	1/20	1	
			MQ	1.240	2.448			
Extended file register	Batch read		ER	1.044	1.276	1/64	1	
	Batch write		EW	1.048	1.368	1/64	1	2
	Test (Random write)		ET	1.172	1.896	1/10	2	
	Monitor data registration		EM	——		—	——	
	Monitor		ME	1.280	2.504	1/20	1	
	Direct read	Word units	NR	0.980	1.328	1/64	1	
	Direct write	Word units	NW	1.056	1.344	1/64	1	2

3 QnA simplified frame command

Item			Command	Intervening time [ms] (Scan time increase)			Number of scans required for processing	
				Q3ACPU (When A38B used)		Number of access points ①/②	When [Enable during RUN] set	When [Disable during RUN] set
				Number of access points: ①	Number of access points: ②			
Device memory	Batch read	Bit units	1	1.068	2.428	1/3952	1	
		word units	2	0.996	3.168	1/480	1	
	Batch write	Bit units	3	1.008	2.428	1/3952	1	2
		word units	4	0.996	3.196	1/480	1	2
	Random read	word units	5	1.272	7.256	1/96	2	3
	Test	Bit units	6	1.240	9.160	1/94	1	2
		word units	7	1.156	6.764	1/80	1	2
	Monitor data registration	word units	8	0.948	0.950	1/96	1	
	Monitor	word units	9	1.212	7.256	1/96	1	1

POINT

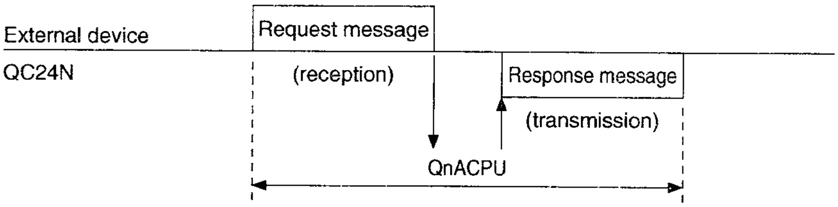
The PLC CPU can process only one of these operations with END processing. If GPP or a module accesses a given PLC CPU at the same time, one processing must wait until the other processing is completed. Therefore, the number of scans required for processing increases.

Appendix 3.2 Processing time of the PLC

When the external device accesses the local station QnACPU loaded with QC24(N) by the dedicated protocol, the processing time of the PLC is as follows when the QC24 (conventional module) and the QC24N are used.

The values listed in the following table are the processing time of the PLC when the access was performed by word under the following conditions:

- The local station QnACPU loaded with a QC24(N) is in the STOP status.
- The time from the start of the request message reception by QC24 (N) to the end of the response message transmission is reduced.
- The device to be accessed is the data register (D).
- The data communication is executed by format 1, data bit: 7, stop bit: 1, and no parity.
- The data transmission speed between the external device and the QC24(N) is as follows:



The time from the start of a request message reception by QC24N to the end of the response message transmission is reduced.

Top : 19200BPS
Bottom : 57600BPS

Access contents	Number of access points	Processing time of the PLC (unit: ms)		
		QC 24	QC 24N	
		QnA frame	QnA frame	QnA simplified frame
Batch read	1	69.2 —	29.6 14.5	22.1 12.7
	64	204.0 —	148.8 55.6	142.2 53.2
	65	204.4 —	150.6 56.2	142.8 53.9
	480	1105.1 —	936.1 324.4	926.4 322.9
Batch write	1	66.0 —	28.5 14.3	21.3 12.4
	64	318.1 —	147.1 54.4	140.2 52.9
	65	319.3 —	148.5 55.6	142.5 53.7
	480	1985.2 —	925.0 316.4	918.1 312.6

(To the next page)

(From the previous page)

Access contents	Number of access points	Processing time of the PLC (unit: ms)		
		QC 24	QC 24N	
		QnA frame	**QnA frame**	**QnA simplified frame**
Test [Random write]	1	71.1 —	29.1 14.0	21.8 13.2
	10	160.2 —	80.8 33.4	73.5 30.2
	80	1156.4 —	478.8 169.2	471.8 167.8
Random read	1	83.0 —	33.5 19.3	27.1 17.7
	96	1267.3 —	577.2 208.4	570.4 205.9
Monitor data registration	1	77.2 —	28.5 17.4	22.8 13.8
	20	230.0 —	100.2 40.8	93.9 39.0
	60	554.4 —	252.0 90.7	244.5 90.1
	96	850.0 —	387.4 138.3	380.0 135.8
Monitor	1	62.1 —	24.0 13.3	17.0 11.1
	20	99.3 —	61.4 25.9	54.5 24.9
	60	190.2 —	138.3 54.9	131.3 52.6
	96	268.0 —	208.4 80.9	201.6 78.0
Multiple block batch read	1	(No function)	32.0 15.8	(No function)
	150 (*1)		393.9 139.8	
	200 (*2)		515.6 182.5	
Multiple block batch write	1		30.9 16.3	
	150 (*1)		389.6 136.9	
	200 (*2)		511.7 178.5	

*1 When the total number of blocks for the bit device and the word device is 15.

*2 When the total number of blocks for the bit device and the word device is 20.

Appendix 3.3 Communication by non procedure protocol

Calculate the processing time of send processing and receive processing using the following formula. Note that the processing time may become further longer depending on other communication function (communication by MC protocol) and special function (ASCII-binary conversion, transmission control, etc.)

Use the value obtained from the following formula as a guideline of processing time for either sending or receiving using CH1 only.

1 Send processing time

	Formula
Communication time [ms]	T = Scan time (St) x 2 + T0 + T1
Request transmission time [ms]	T0 = Request data size [byte] x (number of bit of 1 character/transmission rate [bps] x 1000 + T2)
Internal processing time [ms] *1	T1 = Instruction execution processing time (Ta) + send completion processing time (Tb)

*1 Internal processing time

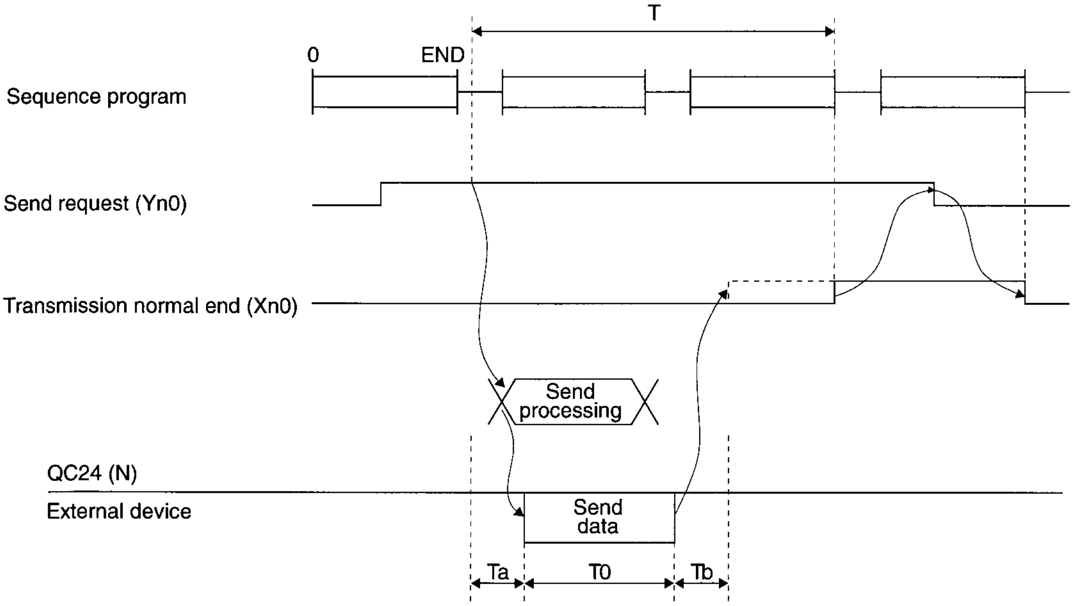
<A1SJ71QC24N1(-R2)>

The time depends on Y signal·buffer memory monitoring timing designation.
(see Section 14.12)

- "QC24N compatible setting" : T1=8.0 [ms] T2=0.07
- "high-speed setting" : T1=3.0 [ms] T2=0.07

<QC24(N) other than the above>

- ·QC24 : T1=19.0 [ms] T2=0.25
- ·QC24N : T1=8.0 [ms] T2=0.07



2 Receive processing time

	Formula
Communication time [ms]	T = Scan time (St) x 2 + request data size [byte] x T4 + T3
Internal processing time [ms] *1	T3 = Receive completion processing time

*1 Internal processing time

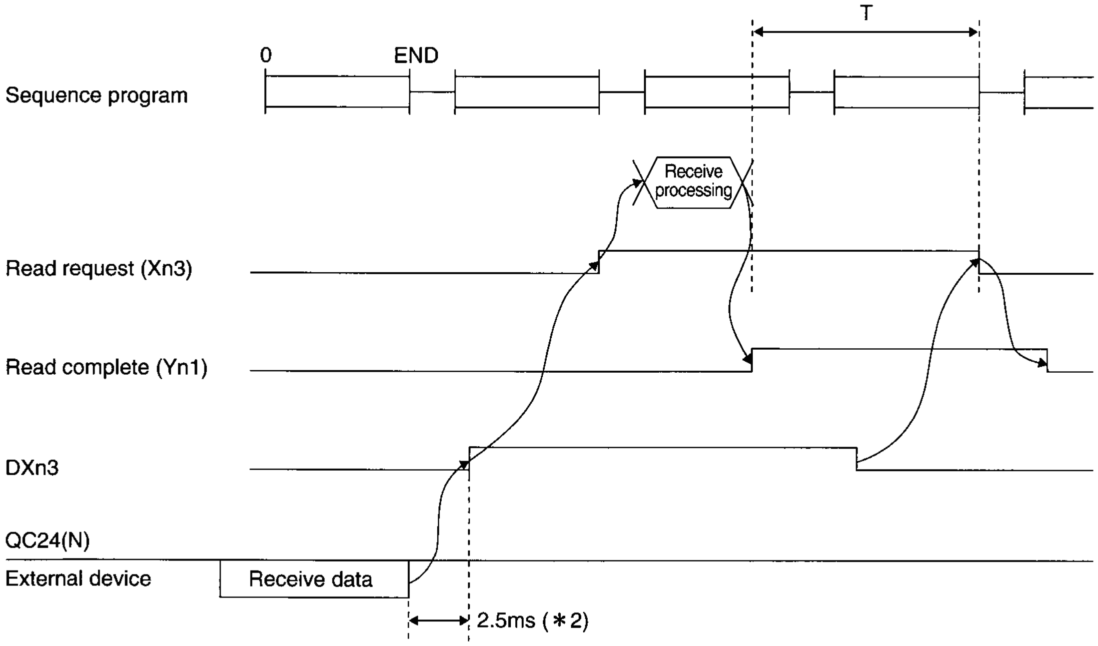
<A1SJ71QC24N1(-R2)>

It depends on Y signal·buffer memory monitoring timing designation. (see Section 14.12)

- "QC24N compatible setting" : T3=14.0 [ms] T4=0.09
- "high-speed setting" : T3=7.0 [ms] T4=0.09

<QC24(N) other than the above>

- QC24 : T3=24.0 [ms] T4=0.50
- QC24N : T3=14.0 [ms] T4=0.10



*2 It indicates a time from when the A1SJ71QC24N1(-R2) receives the data from the line until a receive read request (DXn3) turns on when only the CH side of the A1SJ71QC24N1 (-R2) is being used and data in 30 byte is being transmitted.

Appendix 4 Buffer Memory of Special Function Module and Address Range

The following shows the main modules that can be accessed and its buffer memory address range when the external equipment accesses the Special Function Module buffer memory using the device memory extension setting (See Section 6.2.11).
Access the buffer memory within the range of the buffer memory of the objective special function module.

1 Stations that can be accessed

The following special function module stations can be accessed.

① QnACPU station equipped with a QC24(N) that is connected to an external device

② Another station QnACPU accessed over the network system and QnACPU described in Section 2.2 (QnACPU only)
(Can be accessed within the range of the specifications of each system.)

2 Message [Head device] item designation

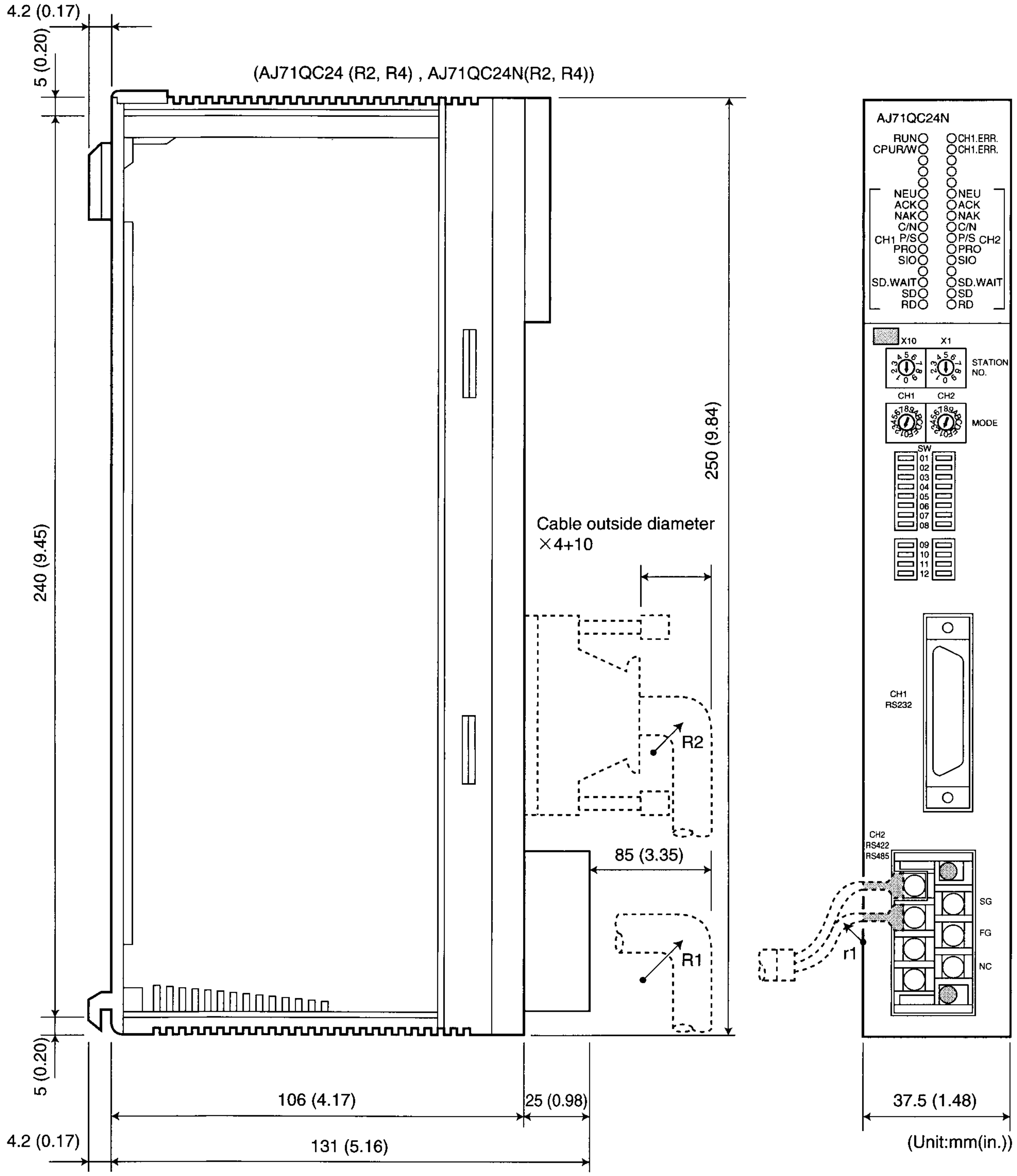
Designate the head address (same as the address designated by FROM/TO instruction) of the buffer memory range accessed by external devices in the [Head device] item in the command message that is transmitted from an external device.

3 Main modules that can be accessed and buffer memory address range

Part name	Model name	Address (Hexadecimal (decimal))		Note
		Head address	Last address	
1-axis positioning module	AD70	0H(0)	6FH(111)	—
	AD70D-S2		7EH(126)	
Positioning module	AD71(S1/S2/S7)		1EF8H(7928)	
	AD72		1EFBH(7931)	
	AD75P1/P2/P3(S3)		1BFFH (7167)	
	AD75M1/M2/M3			
Position detection module	A61LS		2CH(44)	
	A62LS-S5		2EEH(750)	
High-speed counter module	AD61	1H(1)	7H(7)	CH1
	AD61S1	21H(33)	27H(39)	CH2
A/D conversion module	A68AD	0H(0)	22H(34)	12H to 21H (18 to 33) are for K2ACPU.
	A68AD-S2		23H(35)	
	A68ADN		14H(20)	
	A616AD		17FH(383)	
Temperature/digital conversion module	A616TD		27FH(639)	—
	A68RD3		24H(36)	
	A68RD4			
D/A conversion module	A68DAV		11H(17)	
	A68DAI			
	A62DA		5H(5)	
	A62DA-S1			
	A616DAI		3FH(63)	
	A616DAV			

Part name	Model name	Address (Hexadecimal (decimal))		Note
		Head address	Last address	
Memory card Centronics interface module	AD59	0H(0)	17FFH(6143)	—
	AD59-S1			
CC-Link system master local module	AJ61BT11		FFFH(4095)	
	AJ61QBT11		2FFFH(12287)	
Computer link module (AnUCPU compatible)	AJ71UC24		DFFH(3583)	
Computer link module	AJ71C24(S3)		7FFH(2047)	
	AJ71C24-S6/S8			
Intelligent communications module	AD51-S3		BFFH(3071)	
	AD51H-S3		17FFH(6143)	
Ethernet interface module	AJ71E71(S3)		1DFFH(7679)	
	AJ71QE71(B5)		3E7FH(15999)	
Multidrop data link module	AJ71C22S1		7FFH(2047)	
MELSECNET/MINI-S3 master module	AJ71PT32-S3		1FA3H(8099)	
	AJ71T32-S3			
High-speed counter module	A1SD61		93H(147)	
	A1SD62	1H (1)	35H (53)	
	A1SD62E			
	A1SD62D (S1)			
D/A conversion module	A1S62DA	0H(0)	11H(17)	
Temperature/digital conversion module	A1S62RD3/4		24H(36)	
A/D conversion module	A1S64AD		14H(20)	
Temperature adjustment module	A1S64TCRT-S1		B4H(180)	
	A1S64TCRTBW-S1			
	A1S64TCTT-S1			
	A1S64TCTTBW-S1			
Heating/cooling temperature control module	A1S62TCRT-S2		E3H(227)	
	A1S62TCRTBW-S2			
	A1S62TCTT-S2			
	A1S62TCTTBW-S2			
CC-Link system master local module	A1SJ61BT11		FFFH(4095)	
	A1SJ61QBT11		2FFFH(12287)	
Computer link module	A1SJ71(U)C24-R2		DFFH(3583)	
	A1SJ71(U)C24-PRF			
	A1SJ71(U)C24-R4			
Ethernet interface module	A1SJ71E71-B2(S3)		1DFFH(7679)	
	A1SJ71E71-B5(S3)			
	A1SJ71QE71-B2		3E7FH(15999)	
	A1SJ71QE71-B5			
1-axis positioning module	A1SD70		6FH(111)	
Positioning module	A1SD71-S2/S7		1EF8H(7928)	
	A1SD75P1/P2/P3(S3)		1BFFH(7167)	
	A1SD75M1/M2/M3			
Analog I/O module	A1S63ADA		25H(37)	
MELSECNET/MINI master module	A1SJ71PT32-S3		1FA3H(8099)	

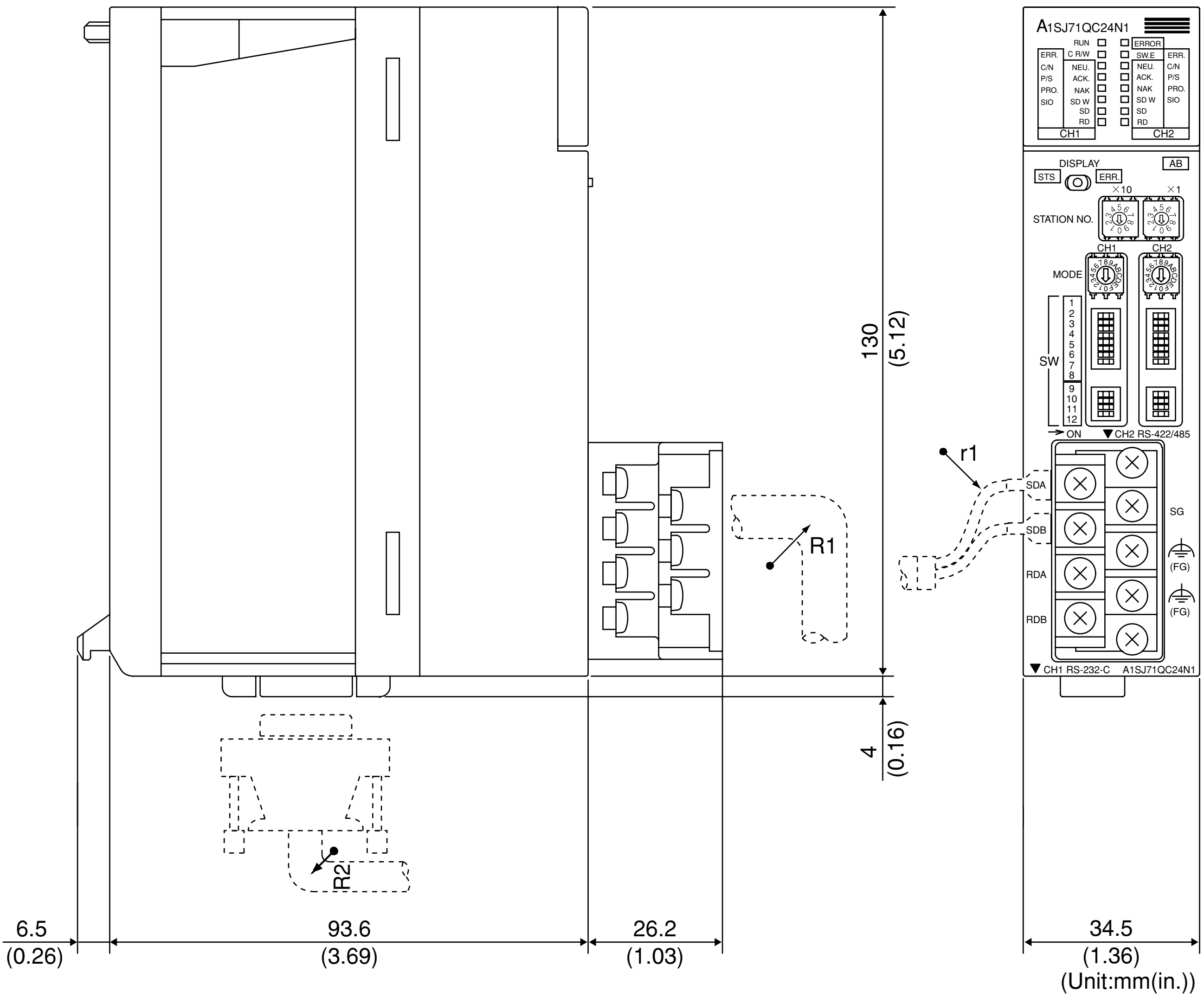
Appendix 5 Outline Dimensions



R1 (bend radius near terminal board) : Cable outside diameter x 4
R2 (bend radius near connector) : Cable outside diameter x 4
r1 (bend radius near crimp terminal) : Can be connected within the range over which bending is not excessive

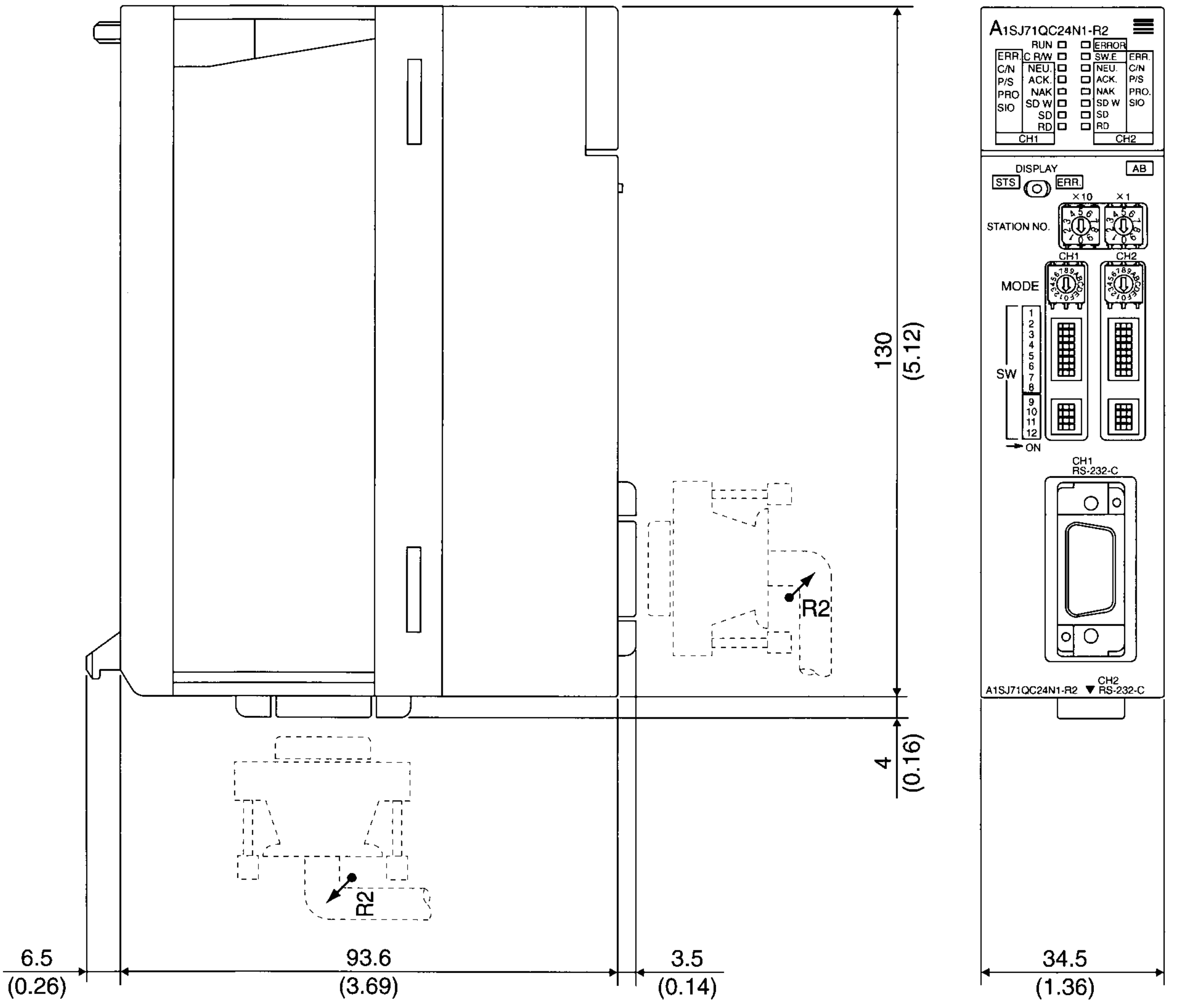
* Except for the interface section, the AJ71QC24(R2, R4), AJ71QC24N(R2, R4) outline dimensions of all six models are the same.
The illustration above shows the outline dimensions of the AJ71QC24N.

- A1SJ71QC24N1, A1SJ71QC24N, A1SJ71QC24
  The outline dimensions of the A1SJ71QC24N and A1SJ71QC24 are the same as that of the A1SJ71QC24N1 except for the model name. (see *4 of Section 4.2)



R1 (bend radius near terminal board) : Cable outside diameter × 4
R2 (bend radius near connector) : Cable outside diameter × 4
r1 (bend radius near crimp terminal) : Can be connected within the range over which bending is not excessive

- A1SJ71QC24N1-R2, A1SJ71QC24N-R2, A1SJ71QC24-R2
  The outline dimensions of the A1SJ71QC24N-R2 and A1SJ71QC24-R2 are the same as that of the A1SJ71QC24N1 except for the model name. (see *4 of Section 4.2)



(Unit:mm(in.))

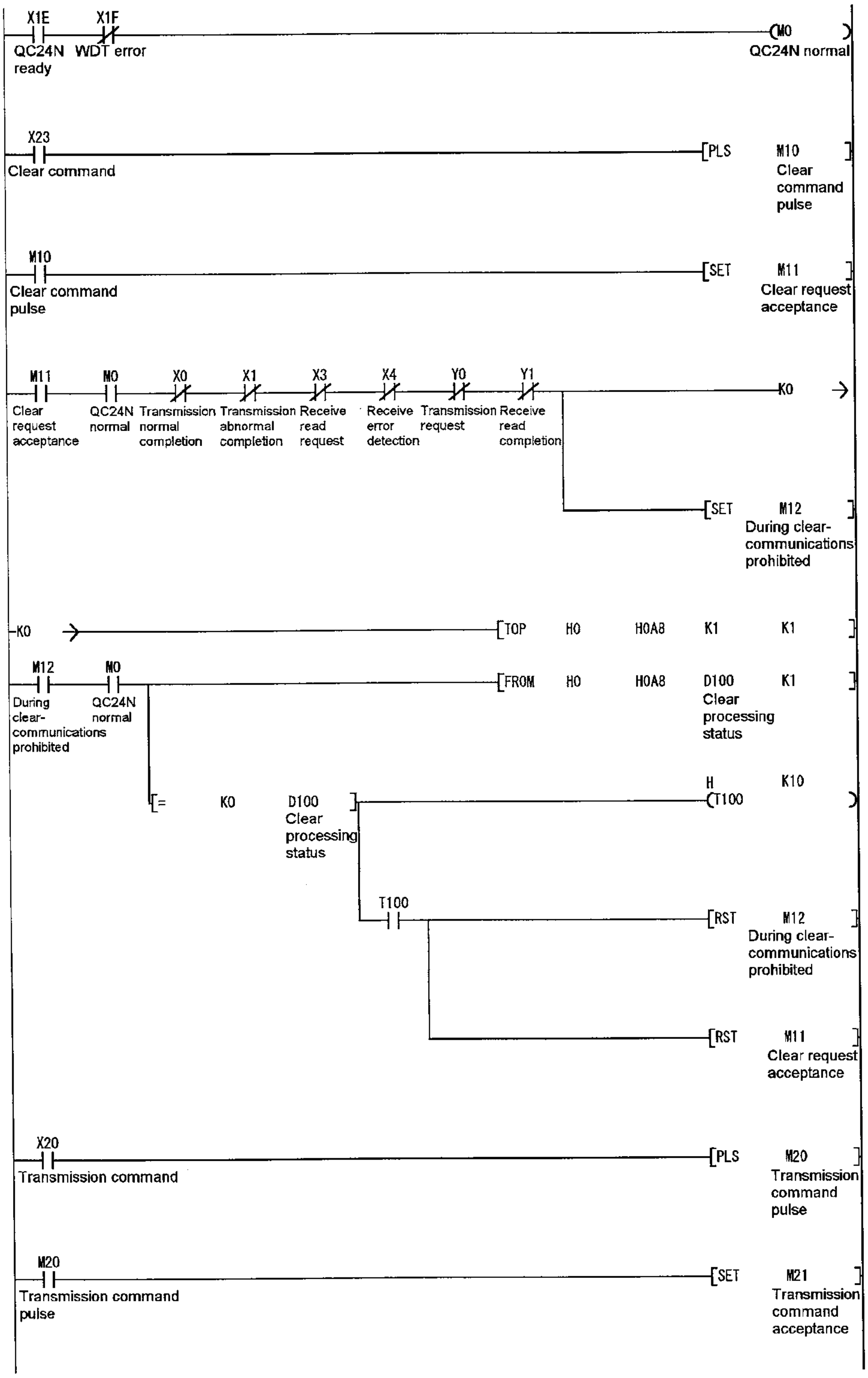
R2 (bend radius near connector) : Cable outside diameter × 4

Appendix 6 Sample Program for the Clear Processing of Reception Data

The following shows a program example that clears data received from an external device using the reception data clear request area of the buffer memory according to Section 9.3.4, when data exchange is executed using the no procedure protocol (when the QC24(N) I/O signals range from X/Y000 to X/Y01F).

The use of major devices that are used in these sample programs are listed below.

Application of device (comment list)					
Device	**Application**	**Device**	**Application**	**Device**	**Application**
X3	Reception data read request	Y0	Transmission request	M12	Clear in progress, exchange prohibited
X1E	QC24N ready	Y1	Reception data read completion	M20	Transmission command pulse
X1F	WDT error	—	—	M21	Transmission command enabled
X20	Transmission command	M0	QC24 (N) normal	M25	Transmission processing in progress
X23	Clear command	M1	Transmission enabled	—	—
—	—	M10	Clear command pulse	D100	Clear processing status
—	—	M11	Clear request enabled	—	—



Turn ON the QC24(N) accessible flag.

Input the clear command. (Convert it into pulse)

Retain the clear command.

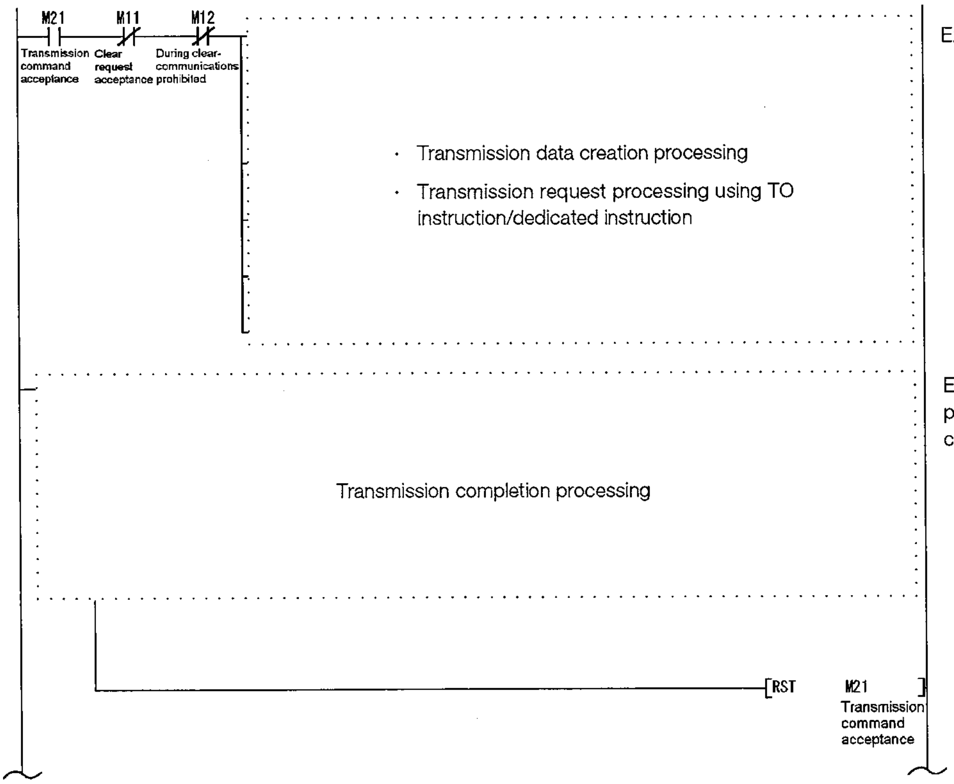
Execute the reception data clear request.

Read the clear processing status by QC24(N).

Reset the clear flag at completion of clear processing.

Input the transmission command. (Convert it into pulse)

Retain the transmission command.



Execute the transmission processing.

Execute the transmission completion processing when the transmission completion signal turns ON.

Appendix 7 Communication Support Tool (MX Component)

MX Component is an ActiveX control library that supports any types of communication paths between IBM PC/AT compatible personal computers and PLCs. It allows the users to establish communication using simple processing only, without having to know about the different communication protocols used in the individual communication.

It also supports various programming languages, allowing for a wide range of application development.

This section provides the overview of the functions provided by MX Component and explains the procedure up to creation of applications.

* See Operating Manual and Programming Manual of MX Component for the details.

Appendix 7.1 Overview of MX Component

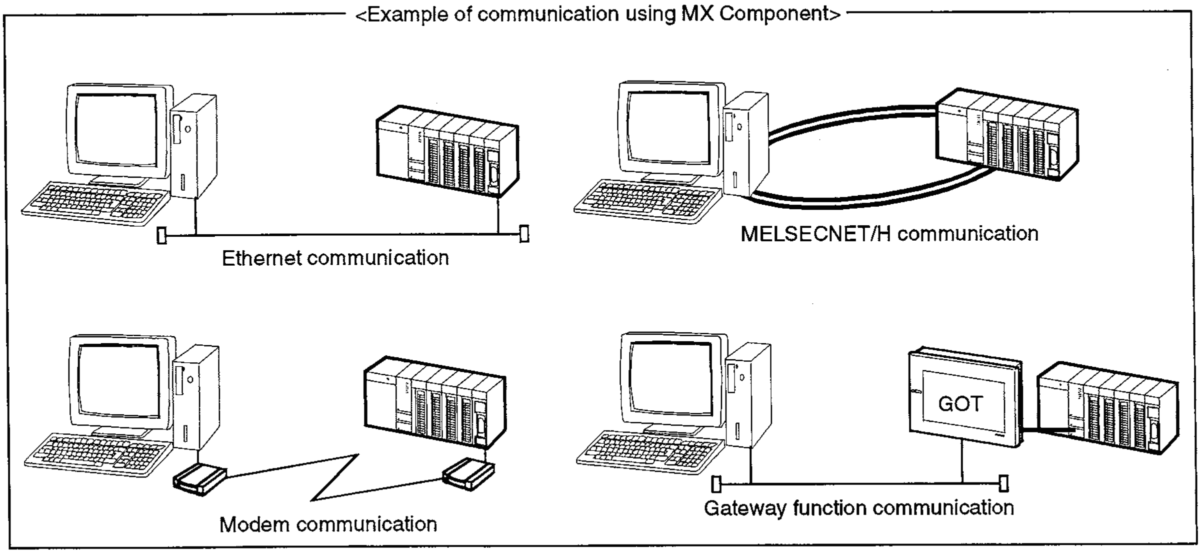
This section provides the overview of MX Component.

Different communication paths, operating systems, programming languages, and functions are supported depending on the version of MX Component used.

1 Support for a wide range of communication paths to PLCs

MX Component supports a wide range of communication paths to PLCs. It is possible to construct systems according to the needs of the users.

<Example of communication using MX Component>



2 Dramatic improvement of application development efficiency

MX Component provides wizard-style communication setting utilities.

The user only needs to select settings from menus displayed on the screen in an interactive manner to achieve the communication settings required to access the target PLC CPU.

Moreover, once the communication setting has been performed, it is possible to access the PLC CPU simply by specifying the logical station number that is stored via the communication setting utilities.

3 Support for various types of operating system

MX Component runs on the following types of DOS/V PC.

- Microsoft® Windows® 95 Operating System
- Microsoft® Windows® 98 Operating System
- Microsoft® Windows® NT Workstation Operating System Version 4.0
- Microsoft® Windows® Millennium Edition Operating System
- Microsoft® Windows® 2000 Professional Operating System
- Microsoft® Windows® XP Professional Operating System
- Microsoft® Windows® XP Home Edition Operating System
- Microsoft® Windows Vista® Home Basic Operating System
- Microsoft® Windows Vista® Home Premium Operating System
- Microsoft® Windows Vista® Business Operating System
- Microsoft® Windows Vista® Ultimate Operating System
- Microsoft® Windows Vista® Enterprise Operating System

4 Various programming languages are supported

MX Component supports the following programming languages.

Development of a wide range of applications is possible for each user.

Programming language	Development software
Visual Basic®	Microsoft® Visual Basic® 6.0, Microsoft® Visual Basic® .NET 2003, Microsoft® Visual Studio 2005 Visual Basic®
Visual C++®	Microsoft® Visual C++® 6.0, Microsoft® Visual C++® .NET 2003, Microsoft® Visual Studio 2005 Visual C++®
VBScript	Text editor and marketed HTML tool
VBA	Microsoft® Excel 2000, Microsoft® Excel 2002, Microsoft® Excel 2003, Microsoft® Excel 2007, Microsoft® Access 2000, Microsoft® Access 2002, Microsoft® Access 2003 or Microsoft® Access 2007

The shown above is information as of November 2008.

For the latest development software, refer to the MX Component Operating Manual.

5 Support for functions dedicated for data communication with PLCs

MX Component provides the functions necessary for data communication with PLCs, including functions for opening/closing communication lines and reading/writing devices. Multi-function communication programs can thus easily be developed with MX Component.

(a) When using Microsoft® Visual Basic® .NET 2003 or Microsoft® Visual C++® .NET 2003

Function name	Function
Connect	Connects a telephone line.
Open	Opens a communication line.
Close	Closes a communication line.
Disconnect	Disconnects a telephone line.
GetErrorMessage	Displays error definition and corrective action.
ReadDeviceBlock	Batch-reads data from devices. (INT type)
WriteDeviceBlock	Batch-writes data to devices. (INT type)
ReadDeviceBlock2	Batch-reads data from devices. (SHORT type)
WriteDeviceBlock2	Batch-writes data to devices. (SHORT type)
ReadDeviceRandom	Randomly reads data from devices. (INT type)
WriteDeviceRandom	Randomly writes data to devices. (INT type)
ReadDeviceRandom2	Randomly reads data from devices. (SHORT type)
WriteDeviceRandom2	Randomly writes data to devices. (SHORT type)
SetDevice	Sets one device. (INT type)
GetDevice	Acquires the data of one device. (INT type)
SetDevice2	Sets one device. (SHORT type)
GetDevice2	Acquires data of one device. (SHORT type)
ReadBuffer	Reads from buffer memory.
WriteBuffer	Writes to buffer memory.
GetClockData	Reads clock data from PLC CPU.
SetClockData	Writes clock data to PLC CPU.
GetCpuType	Reads a PLC CPU type.
SetCpuStatus	Remote RUN/STOP/PAUSE of PLC CPU
EntryDeviceStatus	Registers device status monitor.
FreeDeviceStatus	Deregisters device status monitor.
OnDeviceStatus	Announces event.

(b) When using Microsoft® Visual Basic® 6.0 or Microsoft® Visual C++® 6.0

Function name	Function
Connect	Connects a telephone line.
Open	Opens a communication line.
Close	Closes a communication line.
Disconnect	Disconnects a telephone line.
GetErrorMessage	Displays error definition and corrective action.
ReadDeviceBlock	Batch-reads data from devices. (LONG type)
WriteDeviceBlock	Batch-writes data to devices. (LONG type)
ReadDeviceBlock2	Batch-reads data from devices. (SHORT type/INT type)
WriteDeviceBlock2	Batch-writes data to devices. (SHORT type/INT type)
ReadDeviceRandom	Randomly reads data from devices. (LONG type)
WriteDeviceRandom	Randomly writes data to devices. (LONG type)
ReadDeviceRandom2	Randomly reads data from devices. (SHORT type/INT type)
WriteDeviceRandom2	Randomly writes data to devices. (SHORT type/INT type)
SetDevice	Sets one device. (LONG type)
GetDevice	Acquires the data of one device. (LONG type)
SetDevice2	Sets one device. (SHORT type/INT type)
GetDevice2	Acquires data of one device. (SHORT type/INT type)
ReadBuffer	Reads from buffer memory.
WriteBuffer	Writes to buffer memory.
GetClockData	Reads clock data from PLC CPU.
SetClockData	Writes clock data to PLC CPU.
GetCpuType	Reads a PLC CPU type.
SetCpuStatus	Remote RUN/STOP/PAUSE of PLC CPU
EntryDeviceStatus	Registers device status monitor.
FreeDeviceStatus	Deregisters device status monitor.
OnDeviceStatus	Announces event.

For details of the functions, refer to the MX Component Programming Manual.

6 Collecting data on Excel without programming

Using MX Component and MX Sheet (SWnD5C-SHEET-E) allows users to collect PLC device data on Excel with only simple setting and without any programming.

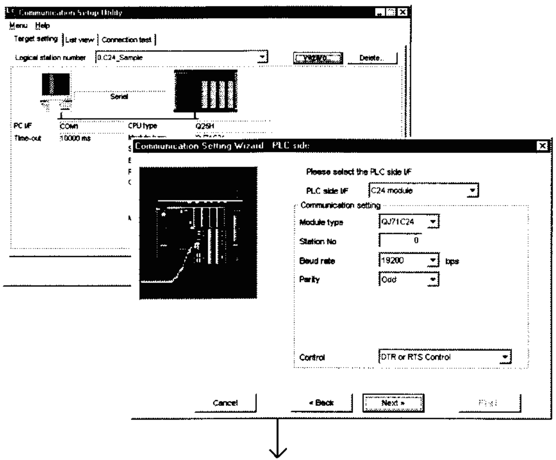
Appendix 7.2 Usage Procedure of MX Component

This section explains the procedure for creating programs and sample programs using MX Component.

1 Procedure for creating programs

The procedure for creating programs is outlined below.

The usage procedure below uses Visual Basic® as an example.



Logical station number 0.C24_Sample

PC I/F COM1

CPU type Q25H

Time-out 10000 ms

Please select the PLC side I/F

PLC side I/F C24 module

Communication setting

Module type QJ71C24

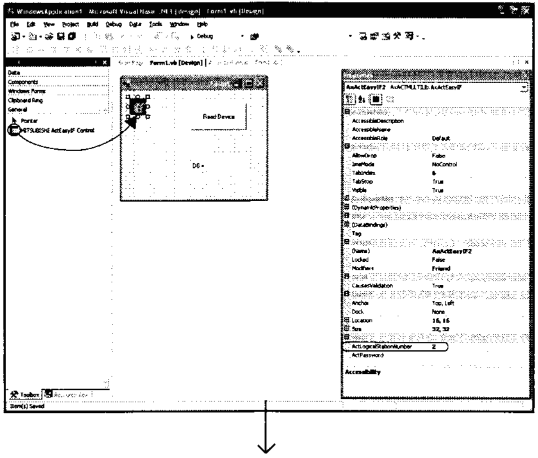
Station No 0

Baud rate 19200 bps

Parity Odd

Control DTR or RTS Control

① Perform the communication settings from a IBM PC/AT compatible personal computer to the PLC by following the wizard. (Some types of controls are set only by programs without using the wizard.)
The wizard allows the user to perform the settings required for the communication such as logical station number, connected module type, and PLC to be connected.



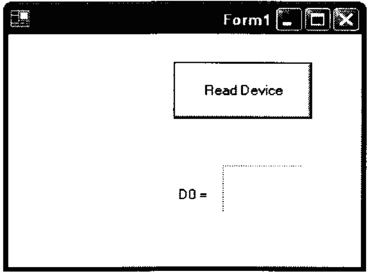
② Paste the ACT control icon onto the form and assign the logical station number set in step 1 to the property of the pasted control.

```
Private Sub Button1_Click(ByVal sender As System.Obj
    Dim rtn As Integer
    Dim iData As Integer
    rtn = AxActEasyIF1.Open()

    rtn = AxActEasyIF1.GetDevice("D0", iData)
    Label1.Text = iData

End Sub
```

③ Use the functions provided by the software to write a program that reads the device data.

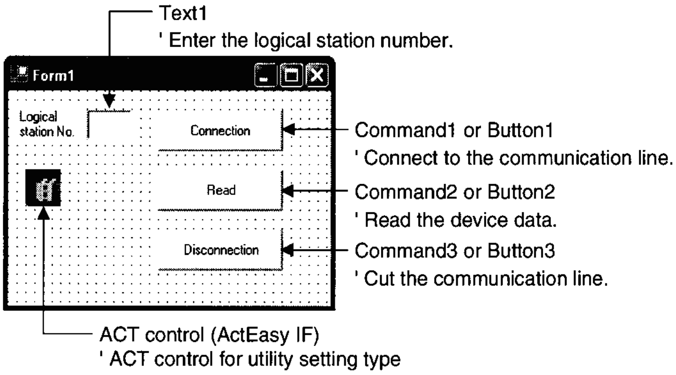


Completed

2 Sample program

The following sample program reads D0 to D4 (five points) of the target PLC using the logical station number.

(a) Screen example (Form1)



(b) Program example

For each development software, the program examples are described below.

① Visual Basic® .NET 2003
② Visual C++® .NET 2003
③ Visual Basic® 6.0
④ Visual C++® 6.0

① When Visual Basic® .NET 2003 is used

```
Private Sub Command1_Click(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles Command1.Click
'**********************************
'  Connection
'**********************************
Dim rtn As Integer

        'Get LogicalstationNumber
        AxActEasyIF1.ActLogicalStationNumber = Val(Text1.Text)

        'Connection
        rtn = AxActEasyIF1.Open()
        If rtn = 0 Then
                MsgBox("The connection was successful")
        Else
                MsgBox("Connection Error :" & Hex(rtn))
        End If

End Sub
```

```
Private Sub Command2_Click(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles Command2.Click
'***********************************
'   Read
'***********************************

Dim rtn As Integer
Dim idata(5) As Short

        D0-D4 are read
        rtn = AxActEasyIF1.ReadDeviceBlock2("D0", 5, idata(0))
        If rtn = 0 Then
                MsgBox("D0-D4 = " & idata(0) & "," & idata(1) & "," & idata(2) & "," & idata(3) & "," & idata(4))
        Else
                MsgBox("Read Error :" & Hex(rtn))
        End If

End Sub


Private Sub Command3_Click(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles Command3.Click
'***********************************
'   Disconnection
'***********************************
Dim rtn As Integer

        'Disconnection
        rtn = AxActEasyIF1.Close()
        If rtn = 0 Then
                MsgBox("The disconnection was successful")
        Else
                MsgBox("Disconnection Error :" & Hex(rtn))
        End If

End Sub
```

② When Visual C++® .NET 2003 is used

```
//**************************
//          Connection
//**************************
private: System::Void button1_Click(System::Object *  sender, System::EventArgs *  e)
{
        int iRet;

        // Get LogicalstationNumber
        axActEasyIF1->ActLogicalStationNumber=Convert::ToInt32(textBox1->Text);

        // Connection
        iRet = axActEasyIF1->Open();
        if( iRet == 0 ){
        MessageBox::Show( "The connection was successful" );
        } else {
        MessageBox::Show( String::Format( "Connection Error:0x{0:x8} [HEX]", __box(iRet) ) );
        }
}
```

```
//**************************
//          Read
//**************************
private: System::Void button2_Click(System::Object *  sender, System::EventArgs *  e)
{
        int iRet;
        short sData[5];
        String* szMessage= "";
        String* lpszarrData[];
        int iNumber;
        String* szReadData;

        // D0-D4 are read
        iRet = axActEasyIF1->ReadDeviceBlock2( "D0", 5, sData );
        if( iRet == 0 ){
                lpszarrData = new String * [ 5 ];
                lpszarrData[0] = "D0-D4 = ";

                // Storage of data to display the results
                for( iNumber = 0 ; iNumber < 5 ; iNumber++ )
                {
                        lpszarrData[ iNumber ] = sData[ iNumber ].ToString();
                }
                szReadData = String::Join(",",lpszarrData);
                MessageBox::Show(String::Format("D0-D4 = { 0} ",szReadData));
        } else {
                MessageBox::Show( String::Format( "Read Error:0x{ 0:x8} [HEX]", __box(iRet) ) );
        }
}


//**************************
//          Disconnection
//**************************
private: System::Void button3_Click(System::Object *  sender, System::EventArgs *  e)
{
        int iRet;

        // Disconnection
        iRet = axActEasyIF1->Close();
        if( iRet == 0 ){
                MessageBox::Show( "The disconnection was successful" );
        } else {
                MessageBox::Show( String::Format( "Disconnection Error:0x{0:x8} [HEX]", __box(iRet) ) );
        }
}
```

③ When Visual Basic® 6.0 is used

```
Private Sub Command1_Click()
'***********************************
' Connection
'***********************************
Dim rtn As Long

        'Get LogicalstationNumber
        ActEasyIF1.ActLogicalStationNumber = Val(Text1.Text)

        'Connection
        rtn = ActEasyIF1.Open()
        If rtn = 0 Then
                MsgBox "The connection was successful"
        Else
                MsgBox "Connection Error :" & Hex(rtn)
        End If

End Sub

Private Sub Command2_Click()
'***********************************
' Read
'***********************************
Dim rtn As Long
Dim idata(5) As Integer

        'D0-D4 are read
        rtn = ActEasyIF1.ReadDeviceBlock2("D0", 5, idata(0))
        If rtn = 0 Then
                MsgBox "D0-D5 = " & idata(0) & "," & idata(1) & "," & idata(2) & "," & idata(3) & "," & idata(4)
        Else
                MsgBox "Read Error :" & Hex(rtn)
        End If

End Sub

Private Sub Command3_Click()
'***********************************
' Disconnection
'***********************************
Dim rtn As Long

        'Disconnection
        rtn = ActEasyIF1.Close()
        If rtn = 0 Then
                MsgBox "The disconnection was successful"
        Else
                MsgBox "Disconnection Error :" & Hex(rtn)
        End If

End Sub
```

④ When Visual C++® 6.0 is used

```
//**************************
//          Connection
//**************************
void CVCDlg::OnOpen()
{
              long lRet;
              CString szMessage;

              // Reflects the logical station No. set in the text box to variables.
              UpdateData();

       //  Get LogicalstationNumber
              m_actEasyIf.SetActLogicalStationNumber( m_lLogicalStationNumber );

       // Connection
              lRet = m_actEasyIf.Open();
              if( lRet == 0 ){
                     MessageBox( "The connection was successful" );
              } else {
                     szMessage.Format( "Connection Error : %x", lRet );
                     MessageBox( szMessage );
              }
}


//**************************
//          Read
//**************************
void CVCDlg::OnRead()
{
              long lRet;
              short sData[5];
              CString szMessage;

       // D0-D4 are read
              lRet = m_actEasyIf.ReadDeviceBlock2( "D0", 5, sData );
              if( lRet == 0 ){
                     szMessage.Format( "D0-D5 = %d,%d,%d,%d,%d",
                                   sData[0],sData[1],sData[2],sData[3],sData[4] );
                     MessageBox( szMessage );
              } else {
                     szMessage.Format( "Read Error : %x", lRet );
                     MessageBox( szMessage );
              }
}
```

```
//**************************
//          Disconnection
//**************************
void CVCDlg::OnClose()
{
            long lRet;
            CString szMessage;

      // Disconnection
            lRet = m_actEasyIf.Close();
            if( lRet == 0 ){
                  MessageBox( "The disconnection was successful" );
            } else {
                  szMessage.Format( "Disconnection Error : %x", lRet );
                  MessageBox( szMessage );
            }
}
```

Index

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.

However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place. Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

Serial Communications Module
User's Manual (Modem Function Additional Version)

MODEL	A-QC24(R2/R4)-U-E
MODEL CODE	13J825
IB(NA)-66612-K(1104)MEE	

MITSUBISHI ELECTRIC CORPORATION

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