MITSUBISHI ELECTRIC

Programmable Controller

CC-Link IE TSN FPGA Module User's Manual

-NZ2GN2S-D41P01
-NZ2GN2S-D41D01
-NZ2GN2S-D41PD02
-NZ2EX2S-D41P01
-NZ2EX2S-D41D01
-NZ2EX2S-D41A01
-FPGA module configuration tool(SW1DNN-CCIETFLEXP-M)

SAFETY PRECAUTIONS

(Read these precautions before using this product.)

Before using this product, please read this manual and the relevant manuals carefully and pay full attention to safety to handle the product correctly.

If the equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.

The precautions given in this manual are concerned with this product only. For the safety precautions of the programmable controller system, refer to the user's manual for the CPU module used.

In this manual, the safety precautions are classified into two levels: "⚠ WARNING" and "⚠ CAUTION".

⚠ **WARNING**	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠ **CAUTION**	Indicates that incorrect handling may cause hazardous conditions, resulting in minor or moderate injury or property damage.

Under some circumstances, failure to observe the precautions given under "⚠ CAUTION" may lead to serious consequences.

Observe the precautions of both levels because they are important for personal and system safety.

Make sure that the end users read this manual and then keep the manual in a safe place for future reference.

[Design Precautions]

⚠ WARNING

- In the case of a communication failure in the network, data of the master station are held. Check Data link status (each station) (SW00B0 to SW00B7) and configure an interlock circuit in the program to ensure that the entire system will operate safely.
- Do not use any "use prohibited" signals as a remote input or output signal. These signals are reserved for system use. Do not write any data to the "use prohibited" areas in the remote register. If these operations are performed, an accident may occur due to an incorrect output or malfunction.
- Configure safety circuits external to the programmable controller to ensure that the entire system operates safely even when a fault occurs in the external power supply or the programmable controller. Failure to do so may result in an accident due to an incorrect output or malfunction.
  (1) Output status varies depending on the setting status of each function that controls digital output and analog output, or communication status with the CC-Link IE TSN master station. Therefore, configure settings carefully. For details on the output status, refer to Page 315 FPGA Control Function.
  (2) Signals may not be output correctly if an output element or its internal circuit has a failure. Configure an external circuit for monitoring output signals that could cause a serious accident.
- Incorporate safety circuits in a user circuit of the FPGA so that the entire system will operate safely (for instance, by holding signal output) even when an error occurs in the user circuit of the FPGA. Failure to do so may result in an accident due to an incorrect output or malfunction.
- Do not change standard circuits because the FPGA control function is incorporated in the FPGA as safety circuits.
- After verification of the FPGA design, verify actual module operations before putting the module in the system.

[Design Precautions]

⚠ CAUTION

- Do not install the communication cables together with the main circuit lines or power cables. Keep a distance of 100mm or more between them. Failure to do so may result in malfunction due to noise.
- Do not install the control lines together with the main circuit lines or power cables. Keep a distance of 150mm or more between them. Failure to do so may result in malfunction due to noise.
- At on/off of the power, a large voltage may occur or a large current may flow between output terminals for a moment. In this case, start the control after analog outputs become stable.
- During control of an inductive load such as a lamp, heater, or solenoid valve, a large current (approximately ten times greater than normal) may flow when the output is turned from off to on. Therefore, use a module that has a sufficient current rating.

[Security Precautions]

⚠ WARNING

- To maintain the security (confidentiality, integrity, and availability) of the programmable controller and the system against unauthorized access, denial-of-service (DoS) attacks, computer viruses, and other cyberattacks from external devices via the network, take appropriate measures such as firewalls, virtual private networks (VPNs), and antivirus solutions.
- Configuration data can be written to this product via a JTAG port by using a dedicated cable for FPGA download. To prevent configuration data from accidentally being written to the product, except for the purpose of FPGA download, lock the control panel so that only qualified maintenance personnel can operate it.

[Installation Precautions]

⚠ WARNING

- Shut off the external power supply (all phases) used in the system before mounting or removing a module. Failure to do so may result in electric shock or cause the module to fail or malfunction.

[Installation Precautions]

⚠ CAUTION

- Use the module in an environment that meets the descriptions of Page 32 General Specifications in this manual. Failure to do so may result in electric shock, fire, malfunction, or damage to or deterioration of the product.
- Do not directly touch any conductive parts and electronic components of the module. Doing so can cause malfunction or failure of the module.
- Securely connect the cable connectors. Poor contact may cause malfunction.
- Beware that the module could be very hot while power is on and immediately after power-off.

[Wiring Precautions]

⚠ WARNING

- Shut off the external power supply (all phases) used in the system before wiring. Failure to do so may result in electric shock or cause the module to fail or malfunction.

[Wiring Precautions]

⚠ CAUTION

- Individually ground the FG terminal of the programmable controller with a ground resistance of 100 ohms or less. Failure to do so may result in electric shock or malfunction.
- Check the rated voltage and terminal layout before wiring to the module, and connect the cables correctly. Connecting a power supply with a different voltage rating or incorrect wiring may cause a fire or failure.
- Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.
- Place the cables in a duct or clamp them. If not, dangling cables may swing or inadvertently be pulled, resulting in malfunction or damage to modules or cables. In addition, the weight of the cables may put stress on modules in an environment of strong vibrations and shocks.
- Do not install the communication cables together with the main circuit lines or power cables. Keep a distance of 100mm or more between them. Failure to do so may result in malfunction due to noise.
- Do not install the control lines together with the main circuit lines or power cables. Keep a distance of 150mm or more between them. Failure to do so may result in malfunction due to noise.
- When disconnecting the cable from the module, do not pull the cable by the cable part. For the cable with connector, hold the connector part of the cable. For the cable connected to the terminal block, pull the cable while pressing the release button using a flathead screwdriver with a tip width of 2.0 to 2.5mm. Pulling the cable without pressing the release button may result in malfunction or damage to the module or cable.
- When an overcurrent caused by an error of an external device or a failure of the programmable controller flows for a long time, it may cause smoke and fire. To prevent this, configure an external safety circuit, such as a fuse.
- Mitsubishi programmable controllers must be installed in control panels. Wiring and replacement of a module must be performed by qualified maintenance personnel with knowledge of protection against electric shock. For wiring methods, refer to Page 66 Wiring.

[Startup and Maintenance Precautions]

⚠ WARNING

- Do not touch any terminal while power is on. Doing so will cause electric shock or malfunction.
- Shut off the external power supply (all phases) used in the system before cleaning the module or retightening the terminal block screws or connector screws. Failure to do so may cause the module to fail or malfunction.

[Startup and Maintenance Precautions]

⚠ CAUTION

- Do not disassemble or modify the module. Doing so may cause failure, malfunction, injury, or a fire.
- Do not drop or apply strong shock to the module. Doing so may damage the module.
- Use any radio communication device such as a cellular phone or PHS (Personal Handy-phone System) 25cm or more away in all directions from the programmable controller. Failure to do so may cause malfunction.
- Shut off the external power supply (all phases) used in the system before mounting or removing a module. Failure to do so may cause the module to fail or malfunction.
- After the first use of the product, do not connect/remove the extension module to/from the main module, and do not mount/remove the terminal block or connector to/from the modules more than 50 times (IEC 61131-2/JIS B 3502 compliant). Exceeding the limit may cause malfunction.
- The operation of IP address/station number setting switches must be limited to 10000 times per switch. Exceeding the limit may cause malfunction.
- The operation of function setting switches must be limited to 1000 times per switch. Exceeding the limit may cause malfunction.
- Before handling the module or cables to be connected to the module, touch a conducting object such as a grounded metal to discharge the static electricity from the human body. Wearing a grounded antistatic wrist strap is recommended. Failure to discharge the static electricity may cause the module to fail or malfunction.
- Startup and maintenance of a control panel must be performed by qualified maintenance personnel with knowledge of protection against electric shock. Lock the control panel so that only qualified maintenance personnel can operate it.

[Disposal Precautions]

⚠ CAUTION

- When disposing of this product, treat it as industrial waste.

CONDITIONS OF USE FOR THE PRODUCT

(1) MELSEC programmable controller ("the PRODUCT") shall be used in conditions;
i) where any problem, fault or failure occurring in the PRODUCT, if any, shall not lead to any major or serious accident; and
ii) where the backup and fail-safe function are systematically or automatically provided outside of the PRODUCT for the case of any problem, fault or failure occurring in the PRODUCT.

(2) The PRODUCT has been designed and manufactured for the purpose of being used in general industries.
MITSUBISHI ELECTRIC SHALL HAVE NO RESPONSIBILITY OR LIABILITY (INCLUDING, BUT NOT LIMITED TO ANY AND ALL RESPONSIBILITY OR LIABILITY BASED ON CONTRACT, WARRANTY, TORT, PRODUCT LIABILITY) FOR ANY INJURY OR DEATH TO PERSONS OR LOSS OR DAMAGE TO PROPERTY CAUSED BY the PRODUCT THAT ARE OPERATED OR USED IN APPLICATION NOT INTENDED OR EXCLUDED BY INSTRUCTIONS, PRECAUTIONS, OR WARNING CONTAINED IN MITSUBISHI ELECTRIC USER'S, INSTRUCTION AND/OR SAFETY MANUALS, TECHNICAL BULLETINS AND GUIDELINES FOR the PRODUCT.
("Prohibited Application")
Prohibited Applications include, but not limited to, the use of the PRODUCT in;
- Nuclear Power Plants and any other power plants operated by Power companies, and/or any other cases in which the public could be affected if any problem or fault occurs in the PRODUCT.
- Railway companies or Public service purposes, and/or any other cases in which establishment of a special quality assurance system is required by the Purchaser or End User.
- Aircraft or Aerospace, Medical applications, Train equipment, transport equipment such as Elevator and Escalator, Incineration and Fuel devices, Vehicles, Manned transportation, Equipment for Recreation and Amusement, and Safety devices, handling of Nuclear or Hazardous Materials or Chemicals, Mining and Drilling, and/or other applications where there is a significant risk of injury to the public or property.

Notwithstanding the above restrictions, Mitsubishi Electric may in its sole discretion, authorize use of the PRODUCT in one or more of the Prohibited Applications, provided that the usage of the PRODUCT is limited only for the specific applications agreed to by Mitsubishi Electric and provided further that no special quality assurance or fail-safe, redundant or other safety features which exceed the general specifications of the PRODUCTs are required. For details, please contact the Mitsubishi Electric representative in your region.

(3) Mitsubishi Electric shall have no responsibility or liability for any problems involving programmable controller trouble and system trouble caused by DoS attacks, unauthorized access, computer viruses, and other cyberattacks.

INTRODUCTION

Thank you for purchasing the CC-Link IE TSN FPGA module (hereafter abbreviated as FPGA module).
This manual describes the procedures, system configuration, parameter settings, functions, and troubleshooting of the relevant products listed below.
Before using this product, please read this manual and the relevant manuals carefully and develop familiarity with the functions and performance of the FPGA module to handle the product correctly.
When applying the program examples provided in this manual to an actual system, ensure the applicability and confirm that it will not cause system control problems.
Note that the menu names and operating procedures may differ depending on an operating system in use and its version. When reading this manual, replace the names and procedures with the applicable ones as necessary.

Relevant products

NZ2GN2S-D41P01, NZ2GN2S-D41D01, NZ2GN2S-D41PD02, NZ2EX2S-D41A01, NZ2EX2S-D41P01, NZ2EX2S-D41D01

FPGA DEVELOPMENT SOFTWARE

For FPGA development software (Intel® Quartus Prime), use the product with the software version 20.1.1, which (its operation) has been verified by Mitsubishi Electric. (☞ Page 26 FPGA development software)

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RELEVANT MANUALS

For the latest e-Manual and manual PDF, please consult your local Mitsubishi representative.

Manual name [manual number]	Description	Available form
CC-Link IE TSN FPGA Module User's Manual [SH-082569ENG] (this manual)	Part names, specifications, procedures before operation, system configuration, installation, wiring, settings, FPGAs, functions, sample circuits, troubleshooting, remote I/O signals, remote register, remote buffer memory, and FPGA register of the FPGA module	Print book e-Manual PDF

Point

e-Manual refers to the Mitsubishi Electric FA electronic book manuals that can be browsed using a dedicated tool.

e-Manual has the following features:

- Required information can be cross-searched in multiple manuals.
- Other manuals can be accessed from the links in the manual.
- The hardware specifications of each part can be found from the product figures.
- Pages that users often browse can be bookmarked.
- Sample programs can be copied to an engineering tool.

TERMS

Unless otherwise specified, this manual uses the following terms.

Term	Description
B0 to B2	A terminal block or a circuit board of B0 to B2 for the main module
CC-Link IE TSN Class*1	A group of devices and switching hubs compatible with CC-Link IE TSN, ranked according to the functions and performance by the CC-Link Partner Association. For CC-Link IE TSN Class, refer to the CC-Link IE TSN Installation Manual (BAP-C3007ENG-001) published by the CC-Link Partner Association.
Configuration	Operation of writing configuration data to the FPGA
Configuration data	Information of the FPGA circuits
Configuration ROM	A non-volatile memory that stores configuration data
Cyclic transmission	A function by which data are periodically exchanged among stations on the same network using link devices
Data link	Communications performed by cyclic transmission and transient transmission
Dedicated instruction	An instruction that simplifies programming for using functions of intelligent function modules
Device station	A station other than a master station: a local station, a remote station
E0 to E2	A terminal block or a circuit board of E0 to E2 for the extension module
Engineering tool	A tool used for setting up programmable controllers, programming, debugging, and maintenance
Extension module	An FPGA module that cannot be used alone. The number of I/O points can be increased or analog I/O can be added by connecting an extension module to the main module.
FPGA development environment for the CC-Link IE TSN FPGA module	A set of data such as design environment (RTL), verification environment, and logic synthesis environment for the FPGA module
FPGA development software	Development software used for FPGA circuit design. Another name for Intel® Quartus Prime.
FPGA download	Operation of writing configuration data to the FPGA or the configuration ROM
FPGA download cable	A cable to connect the JTAG connector of the FPGA module to the personal computer. Access to the FPGA module from the personal computer is possible by using FPGA development software. The FPGA download cable is another name for Intel® FPGA Download Cable II (former name: USB-Blaster™ II).
FPGA Module Configuration Tool	A tool to set the parameters of the FPGA module or perform the FPGA download
FPGA parameter	A parameter to change the operation of the FPGA
FPGA register	A register for the standard circuits and the user circuit
General-purpose hub	A CC-Link IE TSN Class A switching hub authorized by CC-Link Partner Association
Link device	A device (RX, RY, RWr, or RWw) in an FPGA module
Link scan (link scan time)	Time required for all the stations on the network to transmit data. The link scan time depends on data volume and the number of transient transmission requests.
Local station	A station that performs cyclic transmission and transient transmission with the master station and other local stations

Term	Description
Main module	An FPGA module with the communication function. The main module can be used alone. One extension module can be connected to a main module.
Master station	A station that controls the entire network. This station can perform cyclic transmission and transient transmission with all stations. Only one master station can be used in a network.
Module parameter	Parameters to set the FPGA module functions except the FPGA operation
Multicast filter	A filter function that selects whether to send cyclic data of multicast mode received by the own station to the subsequent stations. Setting parameters for this function is not required because the master station automatically sets the parameters according to the system configuration.
Multicast mode	A communication mode used to send cyclic data to multiple stations
Offset binary	Signed number representations. A method where a predetermined bias value is subtracted.
Remote buffer memory	Memory in an FPGA module for storing data such as setting values and monitored values
Remote station	A station that exchanges I/O signals (bit data) and I/O data (word data) with another station by cyclic transmission. This station can perform transient transmission.
Reserved station	A station reserved for future use. This station is not actually connected, but counted as a connected station.
Sample circuit	A connection example of the user circuit and the standard circuits. The sample circuit is incorporated in the FPGA module of factory default.
SLMP	An abbreviation for Seamless Message Protocol. This protocol is used for Ethernet.
Standard circuit	A circuit block that controls the external hardware (digital I/O circuits, analog circuits) of the FPGA. The standard circuit is provided by Mitsubishi Electric Corporation and the circuit change by users is not required.
Transient transmission	A function of communication with another station, which is used when requested by a dedicated instruction or an engineering tool
TSN hub	A CC-Link IE TSN Class B switching hub authorized by the CC-Link Partner Association
User circuit	A circuit block that is designed by a user according to the application.
Verilog	A hardware description language (HDL) used to describe digital circuits

*1 The term has been changed for standardization among manuals and software applications related to CC-Link IE TSN. However, the term used in some CC-Link IE TSN related software windows may remain unchanged and may be different from the term used in this manual.
In case of inconsistency, refer to the following.

Term used in software window	Term after change
Authentication Class	CC-Link IE TSN Class

GENERIC TERMS AND ABBREVIATIONS

Unless otherwise specified, this manual uses the following generic terms and abbreviations.

Generic term/abbreviation	Description
ADC	An abbreviation for an A/D converter. The analog input part of the standard circuit controls it.
DAC	An abbreviation for a D/A converter. The analog output part of the standard circuit controls it.
FPGA module	An abbreviation for the CC-Link IE TSN FPGA module. A generic term for a main module and an extension module.
H/W	An abbreviation for hardware
REMFR	A generic term for the JP.REMFR and ZP.REMFR
REMFRD	An abbreviation for JP.REMFRD
REMFRDIP	An abbreviation for GP.REMFRDIP
REMFRIP	An abbreviation for GP.REMFRIP
REMTO	A generic term for the JP.REMTO and ZP.REMTO
REMTOD	An abbreviation for JP.REMTOD
REMTODIP	An abbreviation for GP.REMTODIP
REMTOIP	An abbreviation for GP.REMTOIP
RWr	An abbreviation for a remote register of a link device. Word data input from a device station to the master station. (For some areas in a local station, data are input in the opposite direction.)
RWw	An abbreviation for a remote register of a link device. Word data output from the master station to a device station. (For some areas in a local station, data are output in the opposite direction.)
RX	An abbreviation for remote input of a link device. Bit data input from a device station to the master station. (For some areas in a local station, data are input in the opposite direction.)
RY	An abbreviation for remote output of a link device. Bit data output from the master station to a device station. (For some areas in a local station, data are output in the opposite direction.)
S/W	An abbreviation for software
SLMPSND	A generic term for the J.SLMPSND, JP.SLMPSND, G.SLMPSND, and GP.SLMPSND

PART 1 OVERVIEW

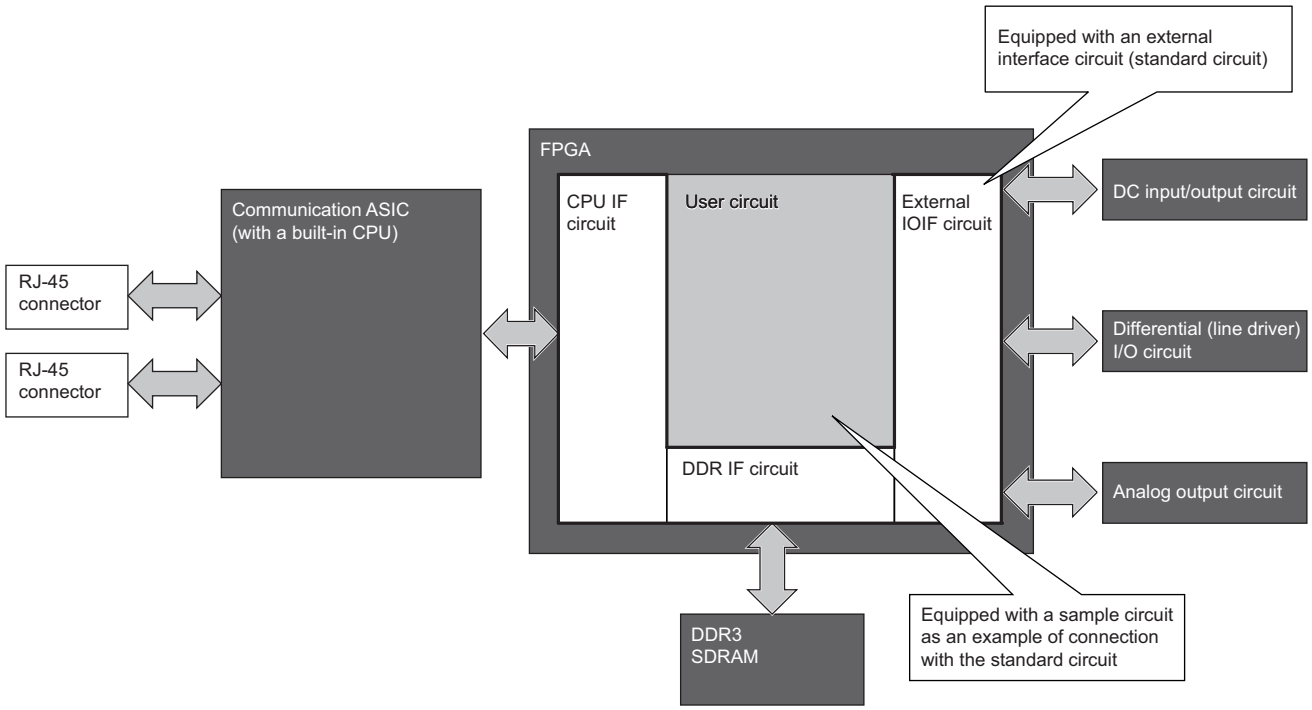
This part consists of the following chapters.

1 WHAT THIS MODULE CAN DO

The FPGA module has the following features.

No interface circuit design or verification required

Since the FPGA module is equipped with the standard circuit, users can focus on designing and verifying the user circuit.
In addition, the user circuit includes sample circuits which can be used as an example of the standard circuit connection, and this reduces the working hours required for FPGA development.

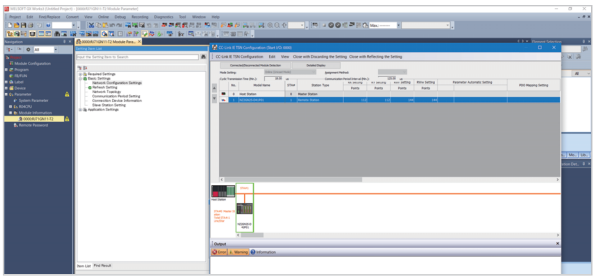


Can be operated without GX Works3

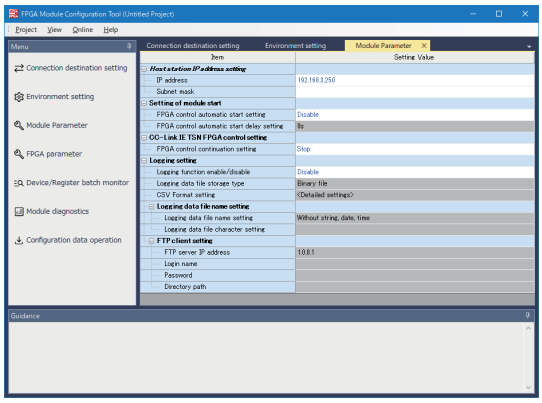
Since the FPGA Module Configuration Tool can be connected to the FPGA module standalone, the FPGA module can be operated without GX Works3.

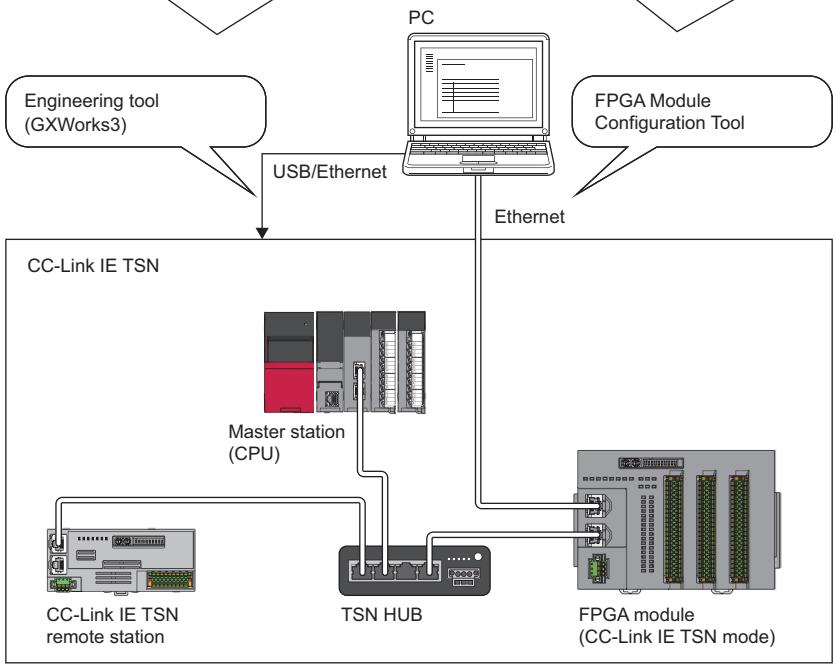
When using the FPGA Module Configuration Tool, the initial settings required for operating the FPGA module are only selection of an FPGA module and input of the IP address. In addition, the FPGA module can be operated with only simple operations without being conscious of SLMP commands.

Set the CPU, network module, and network configuration with GX Works3, and operate the FPGA module by sending and receiving SLMP commands.



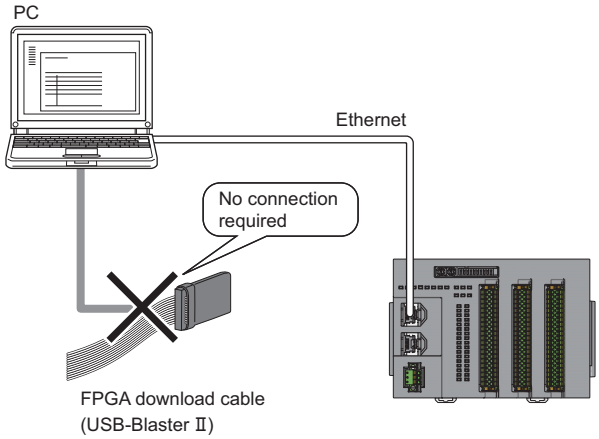
Simply select the FPGA module and input the IP address to complete the setting. The FPGA module can be operated with simple GUI operations without being conscious of SLMP commands.





Configuration data can be written to the FPGA module

The configuration data created with the FPGA development software can be written to the FPGA module by using the FPGA Module Configuration Tool. The user circuit can be updated via the network without reconnecting to the dedicated FPGA download cable. Also, the user circuit can be initialized by writing a sample circuit.



2 PRODUCT LINEUP

2.1 List of Products

Main module

Module name	Model name	Connection circuit board	Reference
CC-Link IE TSN FPGA module, DC input/output 96-point type	NZ2GN2S-D41P01	B0, B1, B2: DC input/output circuit board	Page 34 NZ2GN2S-D41P01, DC input/output: 96 points
CC-Link IE TSN FPGA module, differential input/output 51-point type	NZ2GN2S-D41D01	B0, B1, B2: Differential input/output circuit board	Page 36 NZ2GN2S-D41D01, differential input/output: 51 points
CC-Link IE TSN FPGA module, DC input/output 64-point/differential input/output 17-point type	NZ2GN2S-D41PD02	B0, B1: DC input/output circuit board B2: Differential input/output circuit board	Page 38 NZ2GN2S-D41PD02, DC input/output: 64 points/differential input/output: 17 points

Extension module

Module name	Model name	Connection circuit board	Reference
CC-Link IE TSN extension FPGA module, DC input/output 96-point type	NZ2EX2S-D41P01	E0, E1, E2: DC input/output circuit board	Page 41 NZ2EX2S-D41P01, DC input/output: 96 points
CC-Link IE TSN extension FPGA module, differential input/output 51-point type	NZ2EX2S-D41D01	E0, E1, E2: Differential input/output circuit board	Page 43 NZ2EX2S-D41D01, differential input/output: 51 points
CC-Link IE TSN extension FPGA module, analog input/output 42-point type	NZ2EX2S-D41A01	E0, E1, E2: Analog input/output circuit board	Page 46 NZ2EX2S-D41A01, analog input/output: 42 points

MEMO

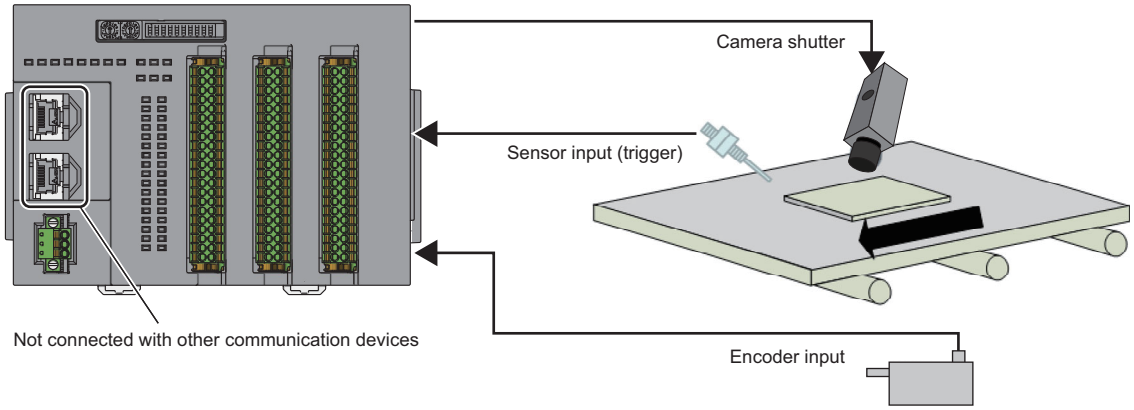
3 SYSTEM CONFIGURATION

The FPGA module has the following two modes. An image of the system configuration to be used in each mode is shown.

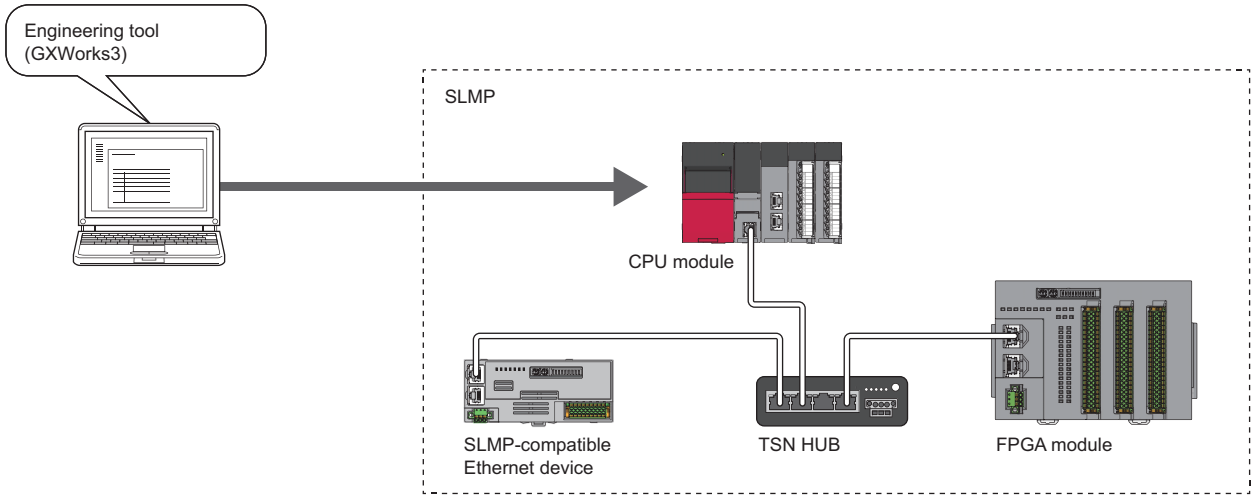
- Standalone mode
- CC-Link IE TSN communication mode

System configuration in standalone mode

In standalone mode, the system can be controlled only by the FPGA module by setting parameters in advance using the FPGA Module Configuration Tool.



Also, in standalone mode, by connecting an SLMP-compatible device, the operation of the FPGA module can be controlled by SLMP commands.



Point

When controlling the FPGA module using the CPU module, the simple CPU communication function can be used to send and receive SLMP commands to and from the FPGA module. For details on SLMP commands, refer to the following.

☞ Page 351 SLMP Communication Function

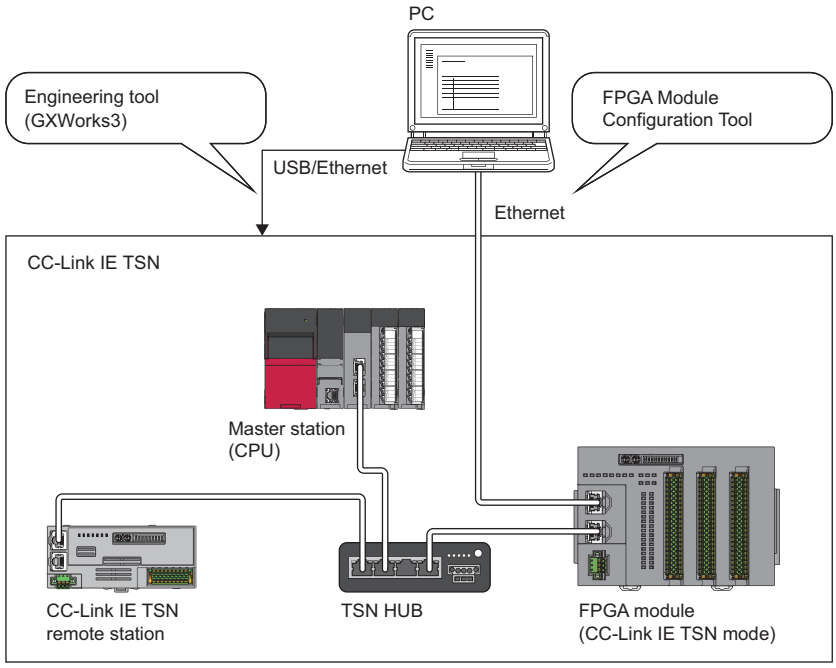
■Network configuration in standalone mode

The star connection is the only connection method that can be used in standalone mode.

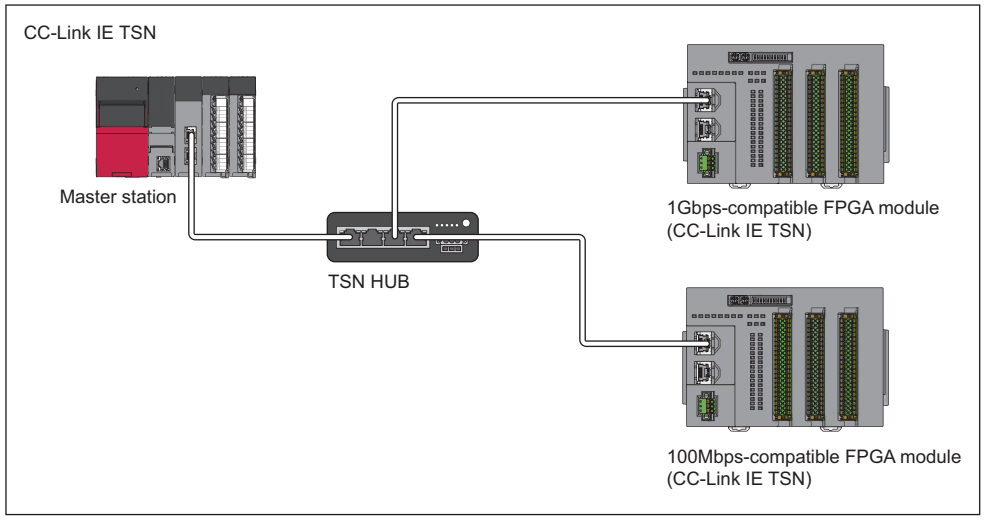
CC-Link IE TSN communication mode

In CC-Link IE TSN communication mode, the FPGA module operates as a CC-Link IE TSN remote station.

■Connection with the master station



■Connection when 1G/100Mbps compatible CC-Link IE TSN devices are mixed



Point

For connection when devices with different communication speeds or CC-Link IE TSN Classes are mixed, refer to the manual for the master module being used.

■Network configuration in CC-Link IE TSN communication mode

The connection methods that can be used in CC-Link IE TSN communication mode are shown below.

- Line topology
- Ring topology
- Star topology
- Mixture of line topology and star topology

Restriction

- The ring topology can only be connected when the CC-Link IE TSN Class is CC-Link IE TSN Class B. When a CC-Link IE TSN Class A FPGA module is connected by ring topology, data links are not established.
- In the ring topology, logging data cannot be transferred to the FTP server, so the logging function cannot be used.

3.1 Applicable Systems

Supported master station

When using the FPGA module in CC-Link IE TSN communication mode, use the following products for the master station.

Model name	Firmware version
RJ71GN11-T2	No restriction
RD78G64, RD78G32, RD78G16, RD78G8, RD78G4	
RD78GHV, RD78GHW	"05" or later

Information on "Supported master station" described above is the ones at the point when this manual was issued.
For latest information, please visit the website of CC-Link Partner Association.
www.cc-link.org

Compatible software package

The table below lists the software packages compatible with the FPGA module.

Product name	Software version
GX Works3	1.095Z or later
FPGA Module Configuration Tool	No restriction

For the FPGA Module Configuration Tool, please consult your local Mitsubishi representative.

FPGA development software

The table below lists FPGA development software that are used for FPGA design and whose operation has been verified.

Product name	Edition	Software version
Intel® Quartus Prime	Lite Edition (free)	20.1.1
	Standard Edition	20.1.1

For Intel® Quartus Prime, download it from the website below.
www.intel.com

Applicable profile

When the latest profile of the FPGA module is necessary, please consult your local Mitsubishi representative.
The profile is a setting file that stores information required for the start-up, operation, and maintenance of devices supporting the CC-Link family.
A module is added to "Module List" of the "CC-Link IE TSN Configuration" window by profile registration to the engineering tool of the master station.
For the profile registration, refer to the following.
📖 GX Works3 Operating Manual

Ethernet cables

For the specifications of the Ethernet cable, refer to the following.
📖 User's manual for the master station used

Switching hub

For compatible switching hubs, refer to the following.
📖 User's manual for the master station used

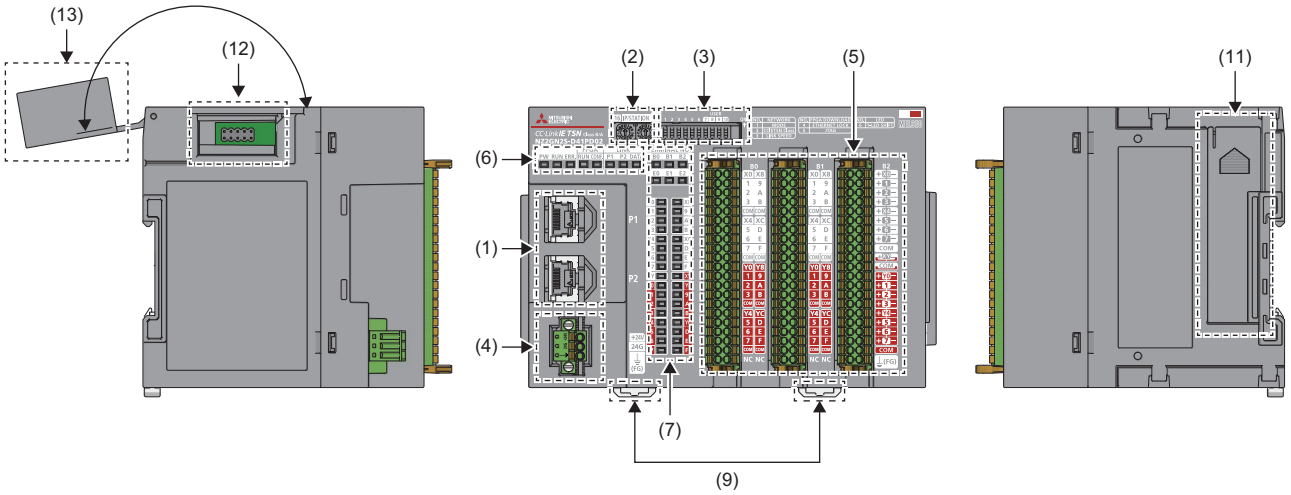
PART 2 SPECIFICATIONS

This part consists of the following chapters.

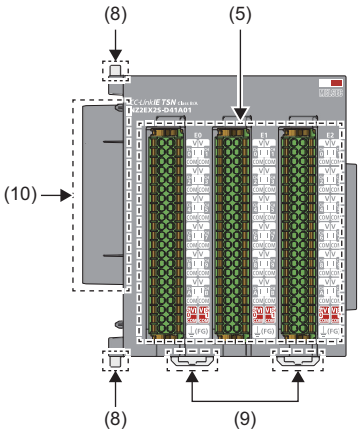
4 PART NAMES

This chapter describes the part names of the FPGA module.

Main module



Extension module



No.	Name	Description
(1)	P1	A port for the connection to a network. (RJ45 connector) Connects an Ethernet cable. (☞ Page 68 Ethernet cables) There are no restrictions on the connection order of the cables for P1 and P2. The LEDs of the Ethernet ports are always off.
	P2	Same as P1
(2)	IP address/station number setting switch	Sets the IP address fourth octet. (☞ Page 54 IP address/station number setting switch setting)
(3)	Function setting switch	Sets the operation mode and the communication speed. (☞ Page 58 Setting the function setting switches)
(4)	Terminal block for module power supply and FG	A terminal block for the connection to module power supply (24VDC) and FG. (☞ Page 66 Wiring to terminal block for module power supply and FG)
(5)	I/O terminal block	A terminal block for the connection to external devices. (☞ Page 70 Wiring to I/O terminal block)

No.	Name	Description
(6)	PW LED	Indicates the power supply status of the FPGA module. • On: Power supply ON • Off: Power supply OFF
	RUN LED	Indicates the operating status of the FPGA module. • On: Operating normally • Flashing: Operating in unit test mode, updating the firmware, or initializing the stand-alone mode IP address • Off: A major error has occurred, firmware update completed, or stand-alone mode IP address initialization completed
	ERR. LED	Indicates the error status of the FPGA module. • On: A moderate error or major error has occurred • Flashing: A minor error has occurred • Off: Operating normally
	FPGA RUN LED	Indicates the execution status of the FPGA control. • On: FPGA control being executed • Off: FPGA control stopped
	FPGA CONF. LED	Indicates the FPGA configuration status. • On: Configuration completed successfully • Flashing: FPGA download being executed • Off: Configuration incomplete or configuration error
	P1 LINK LED	Indicates the link status for PORT1. • On: Link-up • Off: Link-down
	P2 LINK LED	Indicates the link status for PORT2. • On: Link-up • Off: Link-down
	DATA LINK LED	Indicates the data link status of the FPGA module during CC-Link IE TSN communications. • On: Cyclic transmission being performed • Flashing: Cyclic transmission stopped • Off: Cyclic transmission not performed, own station disconnected, or operating in stand-alone mode
(7)	TERMINAL NO.	Indicates the terminal block whose I/O status is to be displayed.
	X0 LED to XF LED	■DC I/O terminal block Indicates the ON/OFF status of the inputs. • On: Input ON • Off: Input OFF ■Differential I/O terminal block[*1*2] Indicates the ON/OFF status of the inputs.[*3] • On: Input ON • Off: Input OFF ■Analog I/O terminal block[*4] No indication
	XY LED[*5]	■DC I/O terminal block Always off ■Differential I/O terminal block[*1*2] Indicates the ON/OFF status of the XY terminal.[*3] • On: XY terminal ON • Off: XY terminal OFF ■Analog I/O terminal block[*4] No indication
	Y0 LED to YF LED[*5]	■DC I/O terminal block Indicates the ON/OFF status of the outputs. • On: Output ON • Off: Output OFF ■Differential I/O terminal block[*1*2] Indicates the ON/OFF status of the outputs. • On: Output ON • Off: Output OFF ■Analog I/O terminal block[*4] No indication
(8)	Module joint lever	A lever to fix the connected part of the modules when connecting an extension module to the main module. (☞ Page 61 Connecting an extension module)
(9)	DIN rail hook	A hook to mount the FPGA module on a DIN rail
(10)	Extension connector	A connector to connect an extension module to the main module
(11)	Extension connector cover	A cover to protect a connector of an extension module. (☞ Page 61 Connecting an extension module)
(12)	JTAG connector	Used for writing configuration data to the FPGA module via JTAG. (☞ Page 300 FPGA Download Function)
(13)	JTAG connector cover	A protective cover for the JTAG connector

*1 The LEDs indicate the ON/OFF status of differential I/O positive (+) signals.
*2 The differential I/O terminal block has 8 points of X terminals and 8 points of Y terminals, and thus X8 to XF LEDs and Y8 to YF LEDs are always off.
*3 Depending on whether the XY terminal is used as an input terminal or an output terminal, the LED that indicates the ON/OFF status varies. When the XY terminal is used as an input terminal, the XY LED on the left indicates the ON/OFF status of the input. When the XY terminal is used as an output terminal, the XY LED on the right indicates the ON/OFF status of the output. For input/output selection of the XY terminal, refer to the following register.
· Output signal/Input output direction signal selection (B0) (ioport_iob0_dio485_osel)
· Output value/Input output direction setting (B0) (ioport_iob0_dio485_odata)
*4 For the analog I/O terminal block, the TERMINAL NO. LEDs do not turn on.
*5 The ON/OFF conditions of the output signals vary depending on the settings of Output signal selection ((B0) (oport_iob0y_osel) to (E2) (oport_ioe2y_osel)) and Output value/Input output direction setting ((B0) (ioport_iob0_dio485_odata) to (E2) (ioport_ioe2_dio485_osel)). The ON/OFF conditions of each setting are as follows.
· Register circuit output is selected: Remote output signal (RY)
· User circuit output is selected: User circuit output signal

Module status and LED status in CC-Link IE TSN communication mode

FPGA module status		LED status					
		PW LED	RUN LED	ERR. LED	FPGA RUN LED	FPGA CONF. LED	DATA LINK LED
Data link in operation		On	On	*2	*3	*4	On
Disconnected		On	On	*2	*3	*4	Off
Reserved station being set		On	On	*2	*3	*4	Flashing
Link stop		On	On	*2	*3	*4	Flashing
Network initial setting in progress*1		On	On	*2	*3	*4	Flashing
Error	Major error	On	Off	On	Off	*4	*6
	Moderate error	On	On	On	Off	*4	*6
	Minor error	On	On	Flashing	*3	*4	*6
Unit test	In progress	On	Flashing	*2	Off	*4	Off
	Completed successfully	On	On	*2	Off	*4	Off
	Completed with an error	On	On	On	Off	*4	Off
FPGA download	Download being executed	On	On	*2	Off	Flashing	*6
	Completed successfully	On	On	*2	Off	On	*6
	Completed with an error	On	On	On	Off	*5	*6
Firmware update	Update in progress	On	Flashing	*2	Off	*4	Off
	Completed (successfully/with an error)	On	Off	*2	Off	*4	Off

*1 If the master station becomes absent during network initial setting, the DATA LINK LED may flash continuously.
*2 On: A moderate error or major error has occurred
Flashing: A minor error has occurred
Off: Operating normally
*3 The LED indicates the execution status of the FPGA control.
On: FPGA control being executed
Off: FPGA control stopped
*4 On: Configuration completed successfully
Off: Configuration incomplete or configuration error
*5 Flashing: When an error occurs while configuration data is being transferred from the tool to the FPGA module
Off: When an error occurs in FPGA configuration after configuration data has been transferred from the tool to the FPGA module
*6 On: Cyclic transmission being performed
Flashing: Cyclic transmission stopped
Off: Cyclic transmission not performed or own station disconnected

Module status and LED status in stand-alone mode

FPGA module status		LED status					
		PW LED	RUN LED	ERR. LED	FPGA RUN LED	FPGA CONF. LED	DATA LINK LED
Normal operation		On	On	*1	*2	*3	Off
Error	Major error	On	Off	On	Off	*3	Off
	Moderate error	On	On	On	Off	*3	Off
	Minor error	On	On	Flashing	*2	*3	Off
Unit test	In progress	On	Flashing	*1	Off	*3	Off
	Completed successfully	On	On	*1	Off	*3	Off
	Completed with an error	On	On	On	Off	*3	Off
FPGA download	Download being executed	On	On	*1	Off	Flashing	Off
	Completed successfully	On	On	*1	Off	On	Off
	Completed with an error	On	On	On	Off	*4	Off
Firmware update	Update in progress	On	Flashing	*1	Off	*3	Off
	Completed (successfully/with an error)	On	Off	*1	Off	*3	Off
IP address initialization	Initialization in progress	On	Flashing	Off	*2	*3	Off
	Completed	On	Off	Off	*2	*3	Off

*1 On: A moderate error or major error has occurred
Flashing: A minor error has occurred
Off: Operating normally

*2 The LED indicates the execution status of the FPGA control.
On: FPGA control being executed
Off: FPGA control stopped

*3 On: Configuration completed successfully
Off: Configuration incomplete or configuration error

*4 Flashing: When an error occurs while configuration data is being transferred from the tool to the FPGA module
Off: When an error occurs in FPGA configuration after configuration data has been transferred from the tool to the FPGA module

TERMINAL NO. LEDs setting method

To set the TERMINAL NO. LEDs, use the function setting switch 6. (☞ Page 54 Setting Switches)

Operating procedure

1. Power on the FPGA module.
2. Check that the module starts up successfully, and then turn on the function setting switch 6.
3. The LED that lights up in the TERMINAL NO. changes every two seconds among 6 LEDs (B0 to E2).
4. When the LED that corresponds to a terminal block whose I/O status is to be displayed turns on, turn off the function setting switch 6.
5. This fixes the LED indication in the TERMINAL NO., and the I/O status of the selected terminal block is displayed on the I/O signal indication part.

5 SPECIFICATIONS

This chapter describes the specifications of the FPGA module.

5.1 General Specifications

<table>
<tr><th>Item</th><th colspan="6">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="6">0 to 55℃</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="6">-25 to 75℃</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="6" rowspan="2">5 to 95%RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td></tr>
<tr><td rowspan="5">Vibration resistance</td><td rowspan="5">Compliant with JIS B 3502 and IEC 61131-2</td><td>—</td><td>Frequency</td><td>Constant acceleration</td><td>Half amplitude</td><td>Number of sweeps</td></tr>
<tr><td rowspan="2">Under intermittent vibration</td><td>5 to 8.4Hz</td><td>—</td><td>3.5mm</td><td rowspan="2">10 times each in X, Y, and Z directions</td></tr>
<tr><td>8.4 to 150Hz</td><td>9.8m/s²*4</td><td>—</td></tr>
<tr><td rowspan="2">Under continuous vibration</td><td>5 to 8.4Hz</td><td>—</td><td>1.75mm</td><td rowspan="2">—</td></tr>
<tr><td>8.4 to 150Hz</td><td>4.9m/s²</td><td>—</td></tr>
<tr><td>Shock resistance</td><td colspan="6">Compliant with JIS B 3502 and IEC 61131-2 (147m/s² (15G)*4, 3 times each in X, Y, and Z directions)</td></tr>
<tr><td>Operating atmosphere</td><td colspan="6">No corrosive gases</td></tr>
<tr><td>Operating altitude*1</td><td colspan="6">0 to 2000m</td></tr>
<tr><td>Installation location</td><td colspan="6">Inside a control panel</td></tr>
<tr><td>Overvoltage category*2</td><td colspan="6">Ⅱ or less</td></tr>
<tr><td>Pollution degree*3</td><td colspan="6">2 or less</td></tr>
<tr><td>Equipment class</td><td colspan="6">Class Ⅰ</td></tr>
</table>

*1 Do not use or store the FPGA module under pressure higher than the atmospheric pressure of altitude 0m.

*2 This indicates the section of the power supply to which the equipment is assumed to be connected between the public electrical power distribution network and the machinery within premises. Category Ⅱ applies to equipment for which electrical power is supplied from fixed facilities. The surge voltage withstand level for the equipment with up to the rated voltage of 300V is 2500V.

*3 This index indicates the degree to which conductive material is generated in terms of the environment in which the equipment is used. Pollution degree 2 is when only non-conductive pollution occurs. A temporary conductivity caused by condensing must be expected occasionally.

*4 When the acceleration is set to 9.8m/s² (1G)

5.2 Performance Specifications

Common to the modules

Item		Specifications
Station type		Remote station
CC-Link IE TSN Class		CC-Link IE TSN Class B/A
Network topology		Line topology, star topology, mixture of star topology and line topology, ring topology
CC-Link IE TSN Protocol version		CC-Link IE TSN Class B: ver.1.0/2.0, CC-Link IE TSN Class A: ver.2.0
Cyclic transmission	RX/RY points	112 points
	RWr/RWw points	144 points
Maximum response time for time-managed polling (for CC-Link IE TSN Class A)		2048μs
Multicast filter		Available (☞ Page 133 Communication mode)
FTP transfer (client)	FTP server software for operation check	Microsoft IIS
	Number of settable transfer destinations	1 maximum
Communication speed		1Gbps 100Mbps
Communication cable	1Gbps	Ethernet cable (Category 5e or higher, straight cable)
	100Mbps	Ethernet cable (Category 5 or higher, straight cable)
Insulated area		Between power supply system and I/O part: Insulation Between communication system and I/O part: Insulation Between terminal blocks of I/O part: Insulation Between channels of I/O part: Non-insulation
Withstand voltage		Between power supply system and I/O part: 500VDC for 1 minute Between communication system and I/O part: 500VDC for 1 minute Between ground and I/O part: 500VDC for 1 minute
Insulation resistance		Between power supply system and I/O part: 10MΩ or higher (500VDC insulation resistance tester) Between communication system and I/O part: 10MΩ or higher (500VDC insulation resistance tester) Between ground and I/O part: 10MΩ or higher (500VDC insulation resistance tester)
Noise immunity*2		Noise voltage 500Vp-p, noise width 1μs, noise frequency 25 to 60Hz (noise simulator condition)
Protection degree		IP2X
External interface	Communication part	RJ45 connector
	Module power supply part	Spring clamp terminal block
	I/O part	Spring clamp terminal block
Applicable wire size	For module power supply	Stranded wire: 0.3 to 1.5mm² (22 to 16 AWG), terminal slot size: 2.4mm × 1.5mm
	For I/O	Stranded wire: 0.3 to 1.5mm² (22 to 16 AWG)*1
Applicable solderless terminal	Terminal block for module power supply and FG	☞ Page 66 Applicable solderless terminals
	I/O terminal block	☞ Page 70 Applicable solderless terminals
External power supply*4		24VDC (Allowable voltage range: 20.4 to 28.8VDC, ripple rate: 5% or less) Current consumption: Total current consumption of main module and extension module (☞ Page 34 Main module, Page 41 Extension module)
Incorporated FPGA	Device name	5CGXFC7D6F27I7N (Cyclone® V series manufactured by Intel®)
	Circuit capacity	LUTs = 149.5K (650K gates), block RAM = 7000K bits
Available capacity for user (recommended value)*3		LUTs = 35K (150K gates), block RAM = 4400K bits
FPGA system clock		100MHz

*1 When a solderless terminal with an insulation sleeve is used, the applicable wire size is 0.75mm² or smaller.

*2 It is the noise immunity of when the set filter value is equal to or more than the recommended value. Note that the module is easily affected by noise if a value less than the recommended value is set. The recommended value depends on the input used (24VDC input, differential (RS-422) input, or differential (RS-485) input). For details, refer to the following.
☞ Page 196 Digital input control part (di2_top)

*3 If a timing violation occurs due to the logic synthesis, correct the user circuit.

*4 For the external power supply, use a SELV (Safety Extra Low Voltage) power supply that meets LIM (Limited Energy Circuit) or UL 1310 Class 2.

Main module

NZ2GN2S-D41P01, DC input/output: 96 points

Item			Specifications
24VDC input specifications	Number of points		48 points
	Rated input voltage*3		24VDC (Ripple ratio: within 5%) (Allowable voltage range: 20.4 to 28.8VDC)
	Rated input current		4.2mA TYP. (for 24VDC)*1
	Maximum number of simultaneous input points		48 points (100%)
	ON voltage/ON current		11VDC or more/3mA or more and 5mA or less*1
	OFF voltage/OFF current		5VDC or less/1.5mA or less
	Input response time	OFF → ON	1μs or less
		ON → OFF	1μs or less
	Pulse input speed (maximum speed)		200kpps (200kHz)
	Wiring method for common		4 points/common (positive/negative common shared type)
	Filter time		0μs to 2683.6992ms*2
5 to 24VDC output specifications	Number of points		48 points
	Rated load voltage*3		5/12/24VDC (4.75 to 28.8VDC)
	Maximum load current		0.1A/point
	Maximum inrush current		0.4A, 10ms or less
	Leakage current at OFF		0.1mA or less
	Maximum voltage drop at ON		0.5VDC (maximum), 0.1A
	Output response time	OFF → ON	1μs or less
		ON → OFF	1μs or less (rated load, resistive load)
	Pulse output speed (maximum speed)		200kpps (200kHz)
	Surge suppressor		Zener diode
	Protection function		Not available
	Wiring method for common		4 points/common (sink type)
Current consumption			280mA*4
Weight			0.62kg

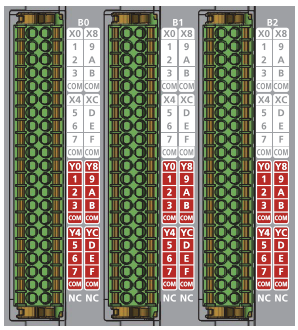
*1 Consider that the constant amount of input current of 4.2mA TYP. (3 to 5mA) flows at power-on regardless of the input voltage, when selecting connected devices and performing wiring. (☞ Page 75 Current flow in the DC input circuit)

*2 ☞ Page 196 Digital input control part (di2_top)

*3 For a device to be connected to the I/O part, use a SELV power supply that meets LIM or UL 1310 Class 2.

*4 The current consumption value (720mA) described on the rating plate and in the manual included with a product (Before Using the Product (BCN-P5999-1585)) is the maximum value for when the extension module is connected.

■I/O terminal block

I/O terminal block	B0		B1		B2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
	2	23	2	23	2	23
	3	24	3	24	3	24
	4	25	4	25	4	25
	5	26	5	26	5	26
	6	27	6	27	6	27
	7	28	7	28	7	28
	8	29	8	29	8	29
	9	30	9	30	9	30
	10	31	10	31	10	31
	11	32	11	32	11	32
	12	33	12	33	12	33
	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

B0				B1				B2			
Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name
1	X0	22	X8	1	X0	22	X8	1	X0	22	X8
2	X1	23	X9	2	X1	23	X9	2	X1	23	X9
3	X2	24	XA	3	X2	24	XA	3	X2	24	XA
4	X3	25	XB	4	X3	25	XB	4	X3	25	XB
5	X0 to X3 COM	26	X8 to XB COM	5	X0 to X3 COM	26	X8 to XB COM	5	X0 to X3 COM	26	X8 to XB COM
6	X4	27	XC	6	X4	27	XC	6	X4	27	XC
7	X5	28	XD	7	X5	28	XD	7	X5	28	XD
8	X6	29	XE	8	X6	29	XE	8	X6	29	XE
9	X7	30	XF	9	X7	30	XF	9	X7	30	XF
10	X4 to X7 COM	31	XC to XF COM	10	X4 to X7 COM	31	XC to XF COM	10	X4 to X7 COM	31	XC to XF COM
11	Y0	32	Y8	11	Y0	32	Y8	11	Y0	32	Y8
12	Y1	33	Y9	12	Y1	33	Y9	12	Y1	33	Y9
13	Y2	34	YA	13	Y2	34	YA	13	Y2	34	YA
14	Y3	35	YB	14	Y3	35	YB	14	Y3	35	YB
15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y0 to Y3 COM	36	Y8 to YB COM
16	Y4	37	YC	16	Y4	37	YC	16	Y4	37	YC
17	Y5	38	YD	17	Y5	38	YD	17	Y5	38	YD
18	Y6	39	YE	18	Y6	39	YE	18	Y6	39	YE
19	Y7	40	YF	19	Y7	40	YF	19	Y7	40	YF
20	Y4 to Y7 COM	41	YC to YF COM	20	Y4 to Y7 COM	41	YC to YF COM	20	Y4 to Y7 COM	41	YC to YF COM
21	NC	42	NC	21	NC	42	NC	21	NC	42	NC

NZ2GN2S-D41D01, differential input/output: 51 points

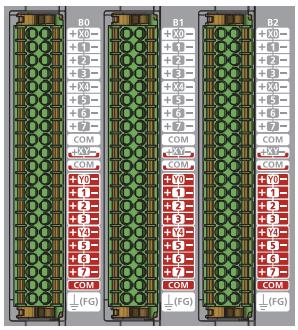
Item			Specifications
Differential (RS-422) input specifications	Number of points		24 points
	Pulse input speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps*3
	Input response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*1
Differential (RS-422) output specifications	Number of points		24 points
	Pulse output speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps
	Output response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
Differential (RS-485) input/output specifications	Number of points		3 points
	Pulse input/output speed (maximum speed)	Multiple of 1	2.5Mpps
		Multiple of 2	5Mpps
	I/O response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*1
Current consumption			510mA*2
Weight			0.62kg

*1 ☞ Page 202 Digital input control part (di2_top)

*2 The current consumption value (950mA) described on the rating plate and in the manual included with a product (Before Using the Product (BCN-P5999-1586)) is the maximum value for when the extension module is connected.

*3 When the module does not need to comply with the EMC Directive, the speed up to 16Mpps can be used.

■I/O terminal block

I/O terminal block	B0		B1		B2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
	2	23	2	23	2	23
	3	24	3	24	3	24
	4	25	4	25	4	25
	5	26	5	26	5	26
	6	27	6	27	6	27
	7	28	7	28	7	28
	8	29	8	29	8	29
	9	30	9	30	9	30
	10	31	10	31	10	31
	11	32	11	32	11	32
	12	33	12	33	12	33
	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

B0				B1				B2			
Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name
1	X0+	22	X0-	1	X0+	22	X0-	1	X0+	22	X0-
2	X1+	23	X1-	2	X1+	23	X1-	2	X1+	23	X1-
3	X2+	24	X2-	3	X2+	24	X2-	3	X2+	24	X2-
4	X3+	25	X3-	4	X3+	25	X3-	4	X3+	25	X3-
5	X4+	26	X4-	5	X4+	26	X4-	5	X4+	26	X4-
6	X5+	27	X5-	6	X5+	27	X5-	6	X5+	27	X5-
7	X6+	28	X6-	7	X6+	28	X6-	7	X6+	28	X6-
8	X7+	29	X7-	8	X7+	29	X7-	8	X7+	29	X7-
9	COM	30	COM	9	COM	30	COM	9	COM	30	COM
10	XY+	31	XY-	10	XY+	31	XY-	10	XY+	31	XY-
11	COM	32	COM	11	COM	32	COM	11	COM	32	COM
12	Y0+	33	Y0-	12	Y0+	33	Y0-	12	Y0+	33	Y0-
13	Y1+	34	Y1-	13	Y1+	34	Y1-	13	Y1+	34	Y1-
14	Y2+	35	Y2-	14	Y2+	35	Y2-	14	Y2+	35	Y2-
15	Y3+	36	Y3-	15	Y3+	36	Y3-	15	Y3+	36	Y3-
16	Y4+	37	Y4-	16	Y4+	37	Y4-	16	Y4+	37	Y4-
17	Y5+	38	Y5-	17	Y5+	38	Y5-	17	Y5+	38	Y5-
18	Y6+	39	Y6-	18	Y6+	39	Y6-	18	Y6+	39	Y6-
19	Y7+	40	Y7-	19	Y7+	40	Y7-	19	Y7+	40	Y7-
20	COM	41	COM	20	COM	41	COM	20	COM	41	COM
21	FG	42	FG	21	FG	42	FG	21	FG	42	FG

NZ2GN2S-D41PD02, DC input/output: 64 points/differential input/output: 17 points

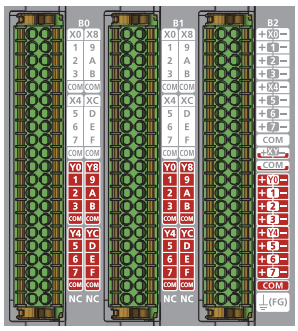
Item			Specifications
24VDC input specifications	Number of points		32 points
	Rated input voltage*3		24VDC (Ripple ratio: within 5%) (Allowable voltage range: 20.4 to 28.8VDC)
	Rated input current		4.2mA TYP. (for 24VDC)*1
	Maximum number of simultaneous input points		32 points (100%)
	ON voltage/ON current		11VDC or more/3mA or more and 5mA or less*1
	OFF voltage/OFF current		5VDC or less/1.5mA or less
	Input response time	OFF → ON	1μs or less
		ON → OFF	1μs or less
	Pulse input speed (maximum speed)		200kpps (200kHz)
	Wiring method for common		4 points/common (positive/negative common shared type)
	Filter time		0μs to 2683.6992ms*2
5 to 24VDC output specifications	Number of points		32 points
	Rated load voltage*3		5/12/24VDC (4.75 to 28.8VDC)
	Maximum load current		0.1A/point
	Maximum inrush current		0.4A, 10ms or less
	Leakage current at OFF		0.1mA or less
	Maximum voltage drop at ON		0.5VDC (maximum), 0.1A
	Output response time	OFF → ON	1μs or less
		ON → OFF	1μs or less (rated load, resistive load)
	Pulse output speed (maximum speed)		200kpps (200kHz)
	Surge suppressor		Zener diode
	Protection function		Not available
	Wiring method for common		4 points/common (sink type)
Differential (RS-422) input specifications	Number of points		8 points
	Pulse input speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps*5
	Input response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*2
Differential (RS-422) output specifications	Number of points		8 points
	Pulse output speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps
	Output response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
Differential (RS-485) input/output specifications	Number of points		1 point
	Pulse input/output speed (maximum speed)	Multiple of 1	2.5Mpps
		Multiple of 2	5Mpps
	I/O response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*2
Current consumption			360mA*4
Weight			0.62kg

*1 Consider that the constant amount of input current of 4.2mA TYP. (3 to 5mA) flows at power-on regardless of the input voltage, when selecting connected devices and performing wiring. (☞ Page 75 Current flow in the DC input circuit)

*2 ☞ Page 204 Digital input control part (di2_top)

*3 For a device to be connected to the I/O part, use a SELV power supply that meets LIM or UL 1310 Class 2.
*4 The current consumption value (800mA) described on the rating plate and in the manual included with a product (Before Using the Product (BCN-P5999-1587)) is the maximum value for when the extension module is connected.
*5 When the module does not need to comply with the EMC Directive, the speed up to 16Mpps can be used.

■I/O terminal block

I/O terminal block	B0		B1		B2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
	2	23	2	23	2	23
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	5	26	5	26	5	26
	6	27	6	27	6	27
	7	28	7	28	7	28
	8	29	8	29	8	29
	9	30	9	30	9	30
	10	31	10	31	10	31
	11	32	11	32	11	32
	12	33	12	33	12	33
	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

B0				B1				B2			
Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name
1	X0	22	X8	1	X0	22	X8	1	X0+	22	X0-
2	X1	23	X9	2	X1	23	X9	2	X1+	23	X1-
3	X2	24	XA	3	X2	24	XA	3	X2+	24	X2-
4	X3	25	XB	4	X3	25	XB	4	X3+	25	X3-
5	X0 to X3 COM	26	X8 to XB COM	5	X0 to X3 COM	26	X8 to XB COM	5	X4+	26	X4-
6	X4	27	XC	6	X4	27	XC	6	X5+	27	X5-
7	X5	28	XD	7	X5	28	XD	7	X6+	28	X6-
8	X6	29	XE	8	X6	29	XE	8	X7+	29	X7-
9	X7	30	XF	9	X7	30	XF	9	COM	30	COM
10	X4 to X7 COM	31	XC to XF COM	10	X4 to X7 COM	31	XC to XF COM	10	XY+	31	XY-
11	Y0	32	Y8	11	Y0	32	Y8	11	COM	32	COM
12	Y1	33	Y9	12	Y1	33	Y9	12	Y0+	33	Y0-
13	Y2	34	YA	13	Y2	34	YA	13	Y1+	34	Y1-
14	Y3	35	YB	14	Y3	35	YB	14	Y2+	35	Y2-
15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y3+	36	Y3-
16	Y4	37	YC	16	Y4	37	YC	16	Y4+	37	Y4-
17	Y5	38	YD	17	Y5	38	YD	17	Y5+	38	Y5-
18	Y6	39	YE	18	Y6	39	YE	18	Y6+	39	Y6-
19	Y7	40	YF	19	Y7	40	YF	19	Y7+	40	Y7-
20	Y4 to Y7 COM	41	YC to YF COM	20	Y4 to Y7 COM	41	YC to YF COM	20	COM	41	COM
21	NC	42	NC	21	NC	42	NC	21	FG	42	FG

Extension module

NZ2EX2S-D41P01, DC input/output: 96 points

Item			Specifications
24VDC input specifications	Number of points		48 points
	Rated input voltage*3		24VDC (Ripple ratio: within 5%) (Allowable voltage range: 20.4 to 28.8VDC)
	Rated input current		4.2mA TYP. (for 24VDC)*1
	Maximum number of simultaneous input points		48 points (100%)
	ON voltage/ON current		11VDC or more/3mA or more and 5mA or less*1
	OFF voltage/OFF current		5VDC or less/1.5mA or less
	Input response time	OFF → ON	1μs or less
		ON → OFF	1μs or less
	Pulse input speed (maximum speed)		200kpps (200kHz)
	Wiring method for common		4 points/common (positive/negative common shared type)
	Filter time		0μs to 2683.6992ms*2
5 to 24VDC output specifications	Number of points		48 points
	Rated load voltage*3		5/12/24VDC (4.75 to 28.8VDC)
	Maximum load current		0.1A/point
	Maximum inrush current		0.4A, 10ms or less
	Leakage current at OFF		0.1mA or less
	Maximum voltage drop at ON		0.5VDC (maximum), 0.1A
	Output response time	OFF → ON	1μs or less
		ON → OFF	1μs or less (rated load, resistive load)
	Pulse output speed (maximum speed)		200kpps (200kHz)
	Surge suppressor		Zener diode
	Protection function		Not available
	Wiring method for common		4 points/common (sink type)
Current consumption			70mA*4
Weight			0.39kg

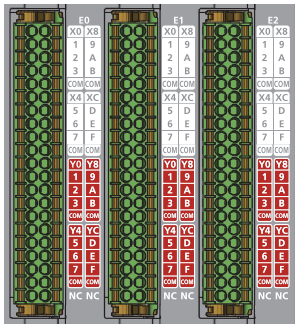
*1 Consider that the constant amount of input current of 4.2mA TYP. (3 to 5mA) flows at power-on regardless of the input voltage, when selecting connected devices and performing wiring. (☞ Page 75 Current flow in the DC input circuit)

*2 ☞ Page 204 Digital input control part (di2_top)

*3 For a device to be connected to the I/O part, use a SELV power supply that meets LIM or UL 1310 Class 2.

*4 The current consumption value is not described on the rating plate of the extension module because the maximum current consumption value for when the main module is used with the extension module is described on the rating plate of the main module.

■I/O terminal block

I/O terminal block	E0		E1		E2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
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	9	30	9	30	9	30
	10	31	10	31	10	31
	11	32	11	32	11	32
	12	33	12	33	12	33
	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

E0				E1				E2			
Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name
1	X0	22	X8	1	X0	22	X8	1	X0	22	X8
2	X1	23	X9	2	X1	23	X9	2	X1	23	X9
3	X2	24	XA	3	X2	24	XA	3	X2	24	XA
4	X3	25	XB	4	X3	25	XB	4	X3	25	XB
5	X0 to X3 COM	26	X8 to XB COM	5	X0 to X3 COM	26	X8 to XB COM	5	X0 to X3 COM	26	X8 to XB COM
6	X4	27	XC	6	X4	27	XC	6	X4	27	XC
7	X5	28	XD	7	X5	28	XD	7	X5	28	XD
8	X6	29	XE	8	X6	29	XE	8	X6	29	XE
9	X7	30	XF	9	X7	30	XF	9	X7	30	XF
10	X4 to X7 COM	31	XC to XF COM	10	X4 to X7 COM	31	XC to XF COM	10	X4 to X7 COM	31	XC to XF COM
11	Y0	32	Y8	11	Y0	32	Y8	11	Y0	32	Y8
12	Y1	33	Y9	12	Y1	33	Y9	12	Y1	33	Y9
13	Y2	34	YA	13	Y2	34	YA	13	Y2	34	YA
14	Y3	35	YB	14	Y3	35	YB	14	Y3	35	YB
15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y0 to Y3 COM	36	Y8 to YB COM	15	Y0 to Y3 COM	36	Y8 to YB COM
16	Y4	37	YC	16	Y4	37	YC	16	Y4	37	YC
17	Y5	38	YD	17	Y5	38	YD	17	Y5	38	YD
18	Y6	39	YE	18	Y6	39	YE	18	Y6	39	YE
19	Y7	40	YF	19	Y7	40	YF	19	Y7	40	YF
20	Y4 to Y7 COM	41	YC to YF COM	20	Y4 to Y7 COM	41	YC to YF COM	20	Y4 to Y7 COM	41	YC to YF COM
21	NC	42	NC	21	NC	42	NC	21	NC	42	NC

NZ2EX2S-D41D01, differential input/output: 51 points

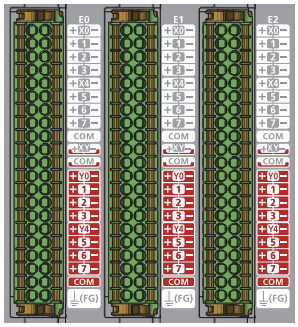
Item			Specifications
Differential (RS-422) input specifications	Number of points		24 points
	Pulse input speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps*3
	Input response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*1
Differential (RS-422) output specifications	Number of points		24 points
	Pulse output speed (maximum speed)	Multiple of 1 (1 phase/2 phases)	2.5Mpps
		Multiple of 2 (1 phase/2 phases)	5Mpps
		Multiple of 4 (2 phases)	10Mpps
	Output response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
Differential (RS-485) input/output specifications	Number of points		3 points
	Pulse input/output speed (maximum speed)	Multiple of 1	2.5Mpps
		Multiple of 2	5Mpps
	I/O response time	OFF → ON	0.2μs or less
		ON → OFF	0.2μs or less
	Filter time		0μs to 2683.6992ms*1
Current consumption			300mA*2
Weight			0.39kg

*1 ☞ Page 204 Digital input control part (di2_top)

*2 The current consumption value is not described on the rating plate of the extension module because the maximum current consumption value for when the main module is used with the extension module is described on the rating plate of the main module.

*3 When the module does not need to comply with the EMC Directive, the speed up to 16Mpps can be used.

■I/O terminal block

I/O terminal block	E0		E1		E2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
	2	23	2	23	2	23
	3	24	3	24	3	24
	4	25	4	25	4	25
	5	26	5	26	5	26
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	7	28	7	28	7	28
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	9	30	9	30	9	30
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	11	32	11	32	11	32
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	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

E0				E1				E2			
Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name	Terminal number	Signal name
1	X0+	22	X0-	1	X0+	22	X0-	1	X0+	22	X0-
2	X1+	23	X1-	2	X1+	23	X1-	2	X1+	23	X1-
3	X2+	24	X2-	3	X2+	24	X2-	3	X2+	24	X2-
4	X3+	25	X3-	4	X3+	25	X3-	4	X3+	25	X3-
5	X4+	26	X4-	5	X4+	26	X4-	5	X4+	26	X4-
6	X5+	27	X5-	6	X5+	27	X5-	6	X5+	27	X5-
7	X6+	28	X6-	7	X6+	28	X6-	7	X6+	28	X6-
8	X7+	29	X7-	8	X7+	29	X7-	8	X7+	29	X7-
9	COM	30	COM	9	COM	30	COM	9	COM	30	COM
10	XY+	31	XY-	10	XY+	31	XY-	10	XY+	31	XY-
11	COM	32	COM	11	COM	32	COM	11	COM	32	COM
12	Y0+	33	Y0-	12	Y0+	33	Y0-	12	Y0+	33	Y0-
13	Y1+	34	Y1-	13	Y1+	34	Y1-	13	Y1+	34	Y1-
14	Y2+	35	Y2-	14	Y2+	35	Y2-	14	Y2+	35	Y2-
15	Y3+	36	Y3-	15	Y3+	36	Y3-	15	Y3+	36	Y3-
16	Y4+	37	Y4-	16	Y4+	37	Y4-	16	Y4+	37	Y4-
17	Y5+	38	Y5-	17	Y5+	38	Y5-	17	Y5+	38	Y5-
18	Y6+	39	Y6-	18	Y6+	39	Y6-	18	Y6+	39	Y6-
19	Y7+	40	Y7-	19	Y7+	40	Y7-	19	Y7+	40	Y7-
20	COM	41	COM	20	COM	41	COM	20	COM	41	COM
21	FG	42	FG	21	FG	42	FG	21	FG	42	FG

NZ2EX2S-D41A01, analog input/output: 42 points

Item			Specifications			
Analog input specifications	Number of points		36 points			
	Input range*5	Voltage	-9.9 to 9.9VDC (input resistance: 800kΩ or more)			
		Current	-19.8 to 19.8mADC (input resistance: 125Ω±0.1%)			
	Digital output		16-bit signed binary value (-32768 to 32767)			
	I/O characteristics, resolution		Input range		A/D conversion value	Maximum resolution
			Voltage	-9.9 to 9.9V	-32440 to 32439	305.2μV
			Current	-19.8 to 19.8mA	-32440 to 32439	610.4nA
	Conversion accuracy*1	Voltage	Within ±0.2% (25±5℃) Within ±0.2% (0 to 55℃)			
		Current	Within ±0.3% (25±5℃) Within ±0.3% (0 to 55℃)			
	Sampling cycle (maximum speed)		4μs/36CH			
	Input band		22.5kHz (sampling cycle: 4μs)			
	Input response time*3		Voltage input: 50μs maximum (-9.9 to 9.9V) Current input: 50μs maximum (-19.8 to 19.8mA)			
	Absolute maximum input		Voltage: ±15V, current: ±30mA*2			
Analog output specifications	Number of points		6 points			
	Output range	Voltage	-9.9 to 9.9VDC (external load resistance value: 1kΩ to 1MΩ)			
		Current	0.2 to 19.8mADC (external load resistance value: 50Ω to 600Ω)			
	Digital input		16-bit unsigned binary value (0 to 65535)			
	I/O characteristics, resolution		Output range		D/A conversion value	Maximum resolution
			Voltage	-9.9 to 9.9V	328 to 65207	305.2μV
			Current	0.2 to 19.8mA	655 to 64880	305.2nA
	Conversion accuracy	Voltage	Within ±0.2% (25±5℃) Within ±0.2% (0 to 55℃)			
		Current	Within ±0.3% (25±5℃) Within ±0.3% (0 to 55℃)			
	Conversion speed (maximum speed)		6μs/6CH			
	Output response time*4		Voltage output: 50μs maximum (-9.9 to 9.9V) Current output: 50μs maximum (0.2 to 19.8mA)			
	Absolute maximum output		Voltage: ±15V, current: ±23mA			
Current consumption			440mA*6			
Weight			0.41kg			

*1 Except for the conditions under noise influence.

*2 This current value is an instantaneous value at which no breakdown occurs in the internal resistance of the module. The maximum input current value for constant application is 24mA.

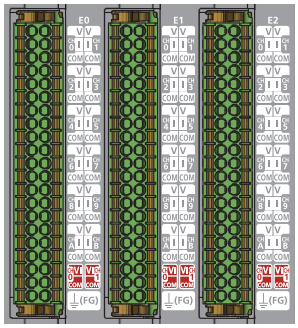
*3 Time taken from the input of an analog signal until that signal is converted to the digital value at ADC.

*4 Time taken from the start of output change of the analog output signal until 90% of the entire change is complete.

*5 For a device to be connected to the input part, use a SELV power supply that meets LIM or UL 1310 Class 2.

*6 The current consumption value is not described on the rating plate of the extension module because the maximum current consumption value for when the main module is used with the extension module is described on the rating plate of the main module.

■I/O terminal block

I/O terminal block	E0		E1		E2	
	Terminal number		Terminal number		Terminal number	
	1	22	1	22	1	22
	2	23	2	23	2	23
	3	24	3	24	3	24
	4	25	4	25	4	25
	5	26	5	26	5	26
	6	27	6	27	6	27
	7	28	7	28	7	28
	8	29	8	29	8	29
	9	30	9	30	9	30
	10	31	10	31	10	31
	11	32	11	32	11	32
	12	33	12	33	12	33
	13	34	13	34	13	34
	14	35	14	35	14	35
	15	36	15	36	15	36
	16	37	16	37	16	37
	17	38	17	38	17	38
	18	39	18	39	18	39
	19	40	19	40	19	40
	20	41	20	41	20	41
	21	42	21	42	21	42

■Signal names of I/O terminal block

E0						E1						E2					
Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name	
1	V	ADCH0	22	V	ADCH1	1	V	ADCH0	22	V	ADCH1	1	V	ADCH0	22	V	ADCH1
2	I		23	I		2	I		23	I		2	I		23	I	
3	COM		24	COM		3	COM		24	COM		3	COM		24	COM	
4	V	ADCH2	25	V	ADCH3	4	V	ADCH2	25	V	ADCH3	4	V	ADCH2	25	V	ADCH3
5	I		26	I		5	I		26	I		5	I		26	I	
6	COM		27	COM		6	COM		27	COM		6	COM		27	COM	
7	V	ADCH4	28	V	ADCH5	7	V	ADCH4	28	V	ADCH5	7	V	ADCH4	28	V	ADCH5
8	I		29	I		8	I		29	I		8	I		29	I	
9	COM		30	COM		9	COM		30	COM		9	COM		30	COM	
10	V	ADCH6	31	V	ADCH7	10	V	ADCH6	31	V	ADCH7	10	V	ADCH6	31	V	ADCH7
11	I		32	I		11	I		32	I		11	I		32	I	
12	COM		33	COM		12	COM		33	COM		12	COM		33	COM	
13	V	ADCH8	34	V	ADCH9	13	V	ADCH8	34	V	ADCH9	13	V	ADCH8	34	V	ADCH9
14	I		35	I		14	I		35	I		14	I		35	I	
15	COM		36	COM		15	COM		36	COM		15	COM		36	COM	
16	V	ADCHA	37	V	ADCHB	16	V	ADCHA	37	V	ADCHB	16	V	ADCHA	37	V	ADCHB
17	I		38	I		17	I		38	I		17	I		38	I	
18	COM		39	COM		18	COM		39	COM		18	COM		39	COM	

E0						E1						E2					
Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name		Terminal number	Signal name	
19	VI	DA CH 0	40	VI	DA CH 1	19	VI	DA CH 0	40	CH 1 VI	DA CH 1	19	VI	DA CH 0	40	CH 1 VI	DA CH 1
20	COM		41	COM		20	COM		41	CH 1 COM		20	COM		41	CH 1 COM	
21	FG		42	FG		21	FG		42	FG		21	FG		42	FG	

5.3 Ethernet Communication Specifications

This section describes the Ethernet communication specifications of the FPGA module.

Item			Description
Transmission specifications	Data transmission speed		1Gbps or 100Mbps*1
	Communication mode	1000BASE-T	Full-duplex
		100BASE-TX	
	Interface		RJ45 connector (AUTO MDI/MDI-X)
	Maximum frame size		1518 bytes
	Maximum segment length		100m*2
	Number of cascade connections	1000BASE-T	Check with the manufacturer of the switching hub to be used.
		100BASE-TX	
	IP version		IPv4

*1 The data transmission speed can be switched by using the function setting switch 3. (☞ Page 58 Setting the function setting switches)

*2 For the maximum segment length (length between switching hubs), check with the manufacturer of the switching hub to be used.

5.4 FPGA Performance

This section describes the FPGA performance of the FPGA module.

Item			Specifications
Operating frequency	Input clock		25MHz
	Internal logic operating frequency		100MHz
	External memory operating frequency (DDR3L SDRAM interface)		400MHz (maximum value)
Series	Manufacturer		Intel
	Series		Cyclone V series
	Master (frame)		5CGXFC7D6F27I7N
IP, macro (standard circuit part)			PLL SRAM DDR3 SDRAM controller (with UniPHY)
Connected device	MCU		R-IN32M4-CL3 manufactured by Renesas
	Memory for logging		DDR3L SDRAM
Input/output performance	DC input/output	Input cycle	100ns (10MHz)
		Output cycle	100ns (10MHz)
		Latency	130ns
	Differential input/output	Input cycle	10ns (100MHz)
		Output cycle	10ns (100MHz)
		Latency	90ns
	Analog input/output	Input cycle (ADC)	4μs (250KHz)
		Output cycle (DAC)	6μs (166.67KHz)
		Latency	—
	Logging	Logging cycle	1μs (1MHz)

MEMO

PART 3 START-UP PROCEDURES

This part consists of the following chapters.

6 PROCEDURES BEFORE OPERATION

This chapter describes the procedures before operation.

When using standalone mode

1. Creating configuration data

Create FPGA configuration data.

☞ Page 140 FPGA DEVELOPMENT

2. Setting the IP address/station number setting switches

Set the fourth octet of the IP address for the FPGA module.

☞ Page 54 IP address/station number setting switch setting

3. Setting the function setting switches

Set the operation mode and communication speed.

☞ Page 58 Setting the function setting switches

4. Attaching

Attach the extension module to the main module.

☞ Page 61 Connecting an extension module

5. Mounting

Mount the FPGA module onto the DIN rails.

☞ Page 63 How to mount a module on a DIN rail

6. Wiring

Wire the power supply, Ethernet cables, and external devices to the FPGA module.

☞ Page 66 Wiring to terminal block for module power supply and FG
☞ Page 68 Ethernet cables
☞ Page 70 Wiring to I/O terminal block

7. Setting FPGA module parameters

Set the parameters required for FPGA module operation with the FPGA Module Configuration Tool.

☞ Page 86 FPGA MODULE CONFIGURATION TOOL

8. FPGA download

Write the created configuration data to the FPGA module.

☞ Page 300 FPGA Download Function

Point

To replace the FPGA module, follow the procedure described below:

- Turn off the FPGA module and remove the FPGA module.
- Prepare a new FPGA module and perform steps 2 to 8.

When using CC-Link IE TSN communication mode

1. Creating configuration data

Create FPGA configuration data.

☞ Page 140 FPGA DEVELOPMENT

2. Setting the IP address/station number setting switches

Set the fourth octet of the IP address for the FPGA module.

☞ Page 54 IP address/station number setting switch setting

3. Setting the function setting switches

Set the operation mode and communication speed.

☞ Page 58 Setting the function setting switches

4. Attaching

Attach the extension module to the main module.

☞ Page 61 Connecting an extension module

5. Mounting

Mount the FPGA module onto the DIN rails.

☞ Page 63 How to mount a module on a DIN rail

6. Wiring

Wire the power supply, Ethernet cables, and external devices to the FPGA module.

☞ Page 66 Wiring to terminal block for module power supply and FG
☞ Page 68 Ethernet cables
☞ Page 70 Wiring to I/O terminal block

7. Setting network parameters

Set the network parameters of the master station to perform CC-Link IE TSN communication.

User's manual for the master module used

8. Programming

Create a program.

☞ Page 396 SAMPLE CIRCUIT IN CC-LINK IE TSN COMMUNICATION MODE

9. Setting FPGA module parameters

Set the parameters required for FPGA module operation with the FPGA Module Configuration Tool.

☞ Page 86 FPGA MODULE CONFIGURATION TOOL

10. FPGA download

Write the created configuration data to the FPGA module.

☞ Page 300 FPGA Download Function

Point

To replace the FPGA module, follow the procedure described below:

- Turn off the FPGA module and remove the FPGA module.
- Prepare a new FPGA module and perform steps 2 to 10.

7 INSTALLATION AND WIRING

This chapter describes the installation and wiring of the FPGA module.

7.1 Setting Switches

IP address/station number setting switch setting

Set the IP address fourth octet using the IP address/station number setting switches on the front of FPGA module.
The setting of IP address/station number setting switches is enabled when the FPGA module is powered on. Therefore, set this function when the module is powered off.

Point

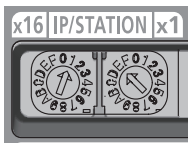
When operating the IP address/station number setting switches, use a flathead screwdriver with a tip width of 2.5mm or less.

Setting method

Set the IP address fourth octet (decimal) using ×1 and ×16 (hexadecimal) of the IP address/station number setting switches.
Combinations of ×1 and ×16 are as follows.

x16 \ x1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
A	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

Ex.
To set to 30:



Setting range

The setting value must be in the range between 1 and 254.

When a value outside the range between 1 to 254 is set, the following occurs.

- When 0 is set, the FPGA module operates with the IP address stored in the non-volatile memory of the module.
- When 255 is set, an IP address/station number setting switches out of range error (IP address) (error code: 2400H) occurs, and the ERR. LED turns on. The FPGA module operates with the IP address 192.168.3.250.

Point

- Do not change the IP address/station number setting switches while the FPGA module is on. If the IP address/station number setting switches are changed while the FPGA module is on, an IP address/station number setting switches changed error (error code: 1030H) occurs and the ERR. LED flashes. After setting the IP address/station number setting switches back to the previous setting, turn on Error clear request flag (RYA) to clear the error state and turn off the ERR. LED.
- The IP address 192.168.3.250 and the subnet mask 255.255.255.0 are set to the non-volatile memory by factory default.

■When a value in the range between 1 and 254 is set

When a value in the range between 1 and 254 is set, the IP address and subnet mask are as follows.

Operation mode	IP address		Subnet mask
	First octet to third octet	Fourth octet	
CC-Link IE TSN communication mode	Master station setting value	IP address/station number setting switch	Master station setting value
Stand-alone mode	Non-volatile memory storage value*1		Non-volatile memory storage value*1

*1 When parameters are written from the FPGA Module Configuration Tool, they are stored in the non-volatile memory of the FPGA module.

Point

- In CC-Link IE TSN communication mode, values are stored in the non-volatile memory when the FPGA module establishes a data link with the master station.
- Set a unique IP address so that it is different from IP addresses of other connected devices on the same network. Otherwise, communications cannot be performed normally.

■When 0 is set

When 0 is set, the IP address and subnet mask are as follows.

Operation mode	IP address		Subnet mask
	First octet to third octet	Fourth octet	
CC-Link IE TSN communication mode	Non-volatile memory storage value*1		Master station setting value
Stand-alone mode	Non-volatile memory storage value*2		

*1 A value stored when the FPGA module established a data link with the master module last time

*2 When parameters are written from the FPGA Module Configuration Tool, they are stored in the non-volatile memory of the FPGA module.

Point

In CC-Link IE TSN communication mode, only the subnet mask value is stored in the non-volatile memory when the FPGA module establishes a data link with the master station.

■In CC-Link IE TSN communication mode

The FPGA module operates with the following IP address and subnet mask until the module starts a data link with the master station after power-on.

IP address/station number setting switch status	IP address		Subnet mask
	First octet to third octet	Fourth octet	
255	192.168.3.250		255.255.255.0 (Fixed)
1 to 254	Non-volatile memory storage value	IP address/station number setting switch	Non-volatile memory storage value
0	Non-volatile memory storage value		

Point

- The FPGA module operates with the factory default value (excluding the IP address fourth octet) until the module establishes a data link with the master station for the first time. When connecting the FPGA Module Configuration Tool to the FPGA module that has never established a data link with the master station (a condition such as the FPGA module powered on alone, without connected to other devices), set the IP address first octet to third octet and the subnet mask to the factory default values. Note that if the FPGA module has established a data link with the master station even once, the module stores the setting values at the data link start to the non-volatile memory. Therefore, the FPGA module that has established a data link can be connected to the FPGA Module Configuration Tool while the same setting values as the master station are set for the first octet to third octet and the subnet mask.
- When the IP address first octet to third octet and the subnet mask values of the master station are changed, the FPGA module operates with the previous master station settings stored in the non-volatile memory until the module establishes a data link with the master station. Therefore, when accessing the FPGA module via the FPGA Module Configuration Tool, establish a data link between the FPGA module and the master station in advance.

■Precautions

The following table lists the IP address and the subnet mask that cannot be used for the FPGA module.

Category	Mode	Conditions of values that cannot be used
IP address	CC-Link IE TSN communication mode	• The bits of the host address (the part of subnet mask where 0 is assigned) are all "0" or all "1". • The third and fourth octet values are all 255. • Outside the range of 0.0.0.1 to 223.255.255.254*1
	Stand-alone mode	• The bits of the host address (the part of subnet mask where 0 is assigned) are all "0" or all "1". • Outside the range of 1.0.0.1 to 223.255.255.254 • The first octet is 127.
Subnet mask	—	• Outside the range of 128.0.0.0 to 255.255.255.252 • In binary notation, 1 is not assigned in the upper bits in a row and 0 is not assigned in the lower bits in a row. Acceptable example: 255.255.255.0, 255.255.0.0 Unacceptable example: 255.0.255.0, 0.255.255.0

*1 The FPGA Module Configuration Tool cannot be connected to the FPGA module because an IP address that cannot be used in the network adapter on the personal computer side and the FPGA Module Configuration Tool, such as an IP address whose first octet is 127 or 0, is included. To connect the FPGA Module Configuration Tool to the FPGA module, correct the IP address or connect the module in stand-alone mode.

Initializing IP address in stand-alone mode

In stand-alone mode, the FPGA module can initialize the IP address and the subnet mask stored in the non-volatile memory. The initialized IP address and subnet mask are as follows.

- IP address: 192.168.3.250
- Subnet mask: 255.255.255.0

Operating procedure

1. Power off the FPGA module.
2. Set the IP address/station number setting switches and function setting switches as follows.
   - IP address/station number setting switch: 255
   - Function setting switch 1: ON
   - Function setting switch 2: ON
3. Power on the FPGA module.
4. When the initialization starts, the RUN LED flashes.
5. When the initialization is complete, the RUN LED turns off.
6. Power off the FPGA module.
7. Set the IP address/station number setting switches and function setting switches as follows.
   - Function setting switch 2: OFF
   - IP address/station number setting switch: IP address fourth octet
8. Power on the FPGA module.

Setting the function setting switches

Set the following functions using the DIP switch on the front of FPGA module.

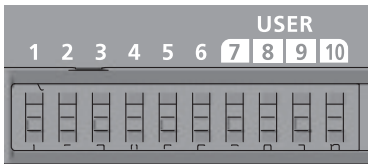
- Operation mode setting function
- CC-Link IE TSN Class setting function
- Communication speed setting function
- Lock function of FPGA download via Ethernet
- JTAG FPGA download error detection disable function
- I/O signal indication setting function
- Always write register write function

Point

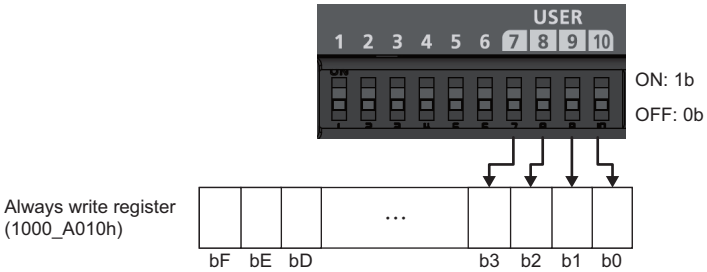
When operating the function setting switch, use a flathead screwdriver with a tip width of 1.2mm or less.

Setting method

Set each function with the function setting switch 1 to function setting switch 10.



Switch name		Function name	Setting details
Function setting switch 1	MODE	Operation mode setting function	Sets the FPGA module operation mode. • OFF: CC-Link IE TSN communication mode • ON: Stand-alone mode
Function setting switch 2	CCIETSN Class	CC-Link IE TSN Class setting function	Sets CC-Link IE TSN Class. • OFF: CC-Link IE TSN Class B • ON: CC-Link IE TSN Class A By using the function setting switch 1 and the IP address/station number setting switch together, the IP address can be initialized in unit test mode or stand-alone mode. (☞ Page 57 Initializing IP address in stand-alone mode, Page 432 MODULE DIAGNOSTICS WITH THE FPGA MODULE CONFIGURATION TOOL) For the CC-Link IE TSN Class setting status, refer to the following. ☞ Page 495 Function setting switch state monitor
Function setting switch 3	LINK SPEED	Communication speed setting function	Sets the communication speed. • OFF: 1Gbps • ON: 100Mbps For the communication speed setting status, refer to the following. ☞ Page 495 Function setting switch state monitor
Function setting switch 4	ETHERNET LOCK	Lock function of FPGA download via Ethernet	Prohibits FPGA download via Ethernet. • OFF: Enable • ON: Prohibit (lock) For details on the FPGA download function, refer to the following. ☞ Page 300 FPGA Download Function
Function setting switch 5	JTAG	JTAG FPGA download error detection disable function	Turn on the switch when performing the FPGA download via JTAG. Be sure to turn off the switch after the completion of the download. • OFF: Error detection enabled • ON: Error detection disabled For details on the FPGA download function, refer to the following. ☞ Page 300 FPGA Download Function
Function setting switch 6	T-LED SHIFT	I/O signal indication setting function	Sets the terminal block whose I/O status is to be displayed on the TERMINAL NO. • OFF: Fix LED indication terminal block. • ON: Change LED indication terminal block. (The LED corresponding to each terminal block alternately lights up in every two seconds) For details on the I/O status indicator LED setting, refer to the following. ☞ Page 31 TERMINAL NO. LEDs setting method

Switch name		Function name	Setting details
Function setting switch 7 to function setting switch 10	USER	Always write register write function	Sets the always write register 0 (usr_alwreg_00). Connect the always write register 0 (usr_alwreg_00) in the user circuit so that the operation of the user circuit can be changed by turning ON/OFF the user switch. The following shows the bit assignments of the always write register 0 (usr_alwreg_00) and the user switch.  The user switch setting is written to the always write register 0 (usr_alwreg_00) when "User switch enable/disable" of the FPGA parameter is set to "Enable". To write the setting to the always write register 0 (usr_alwreg_00) using the FPGA register access function, set "User switch enable/disable" to "Disable".

■Function setting switches 1 to 3

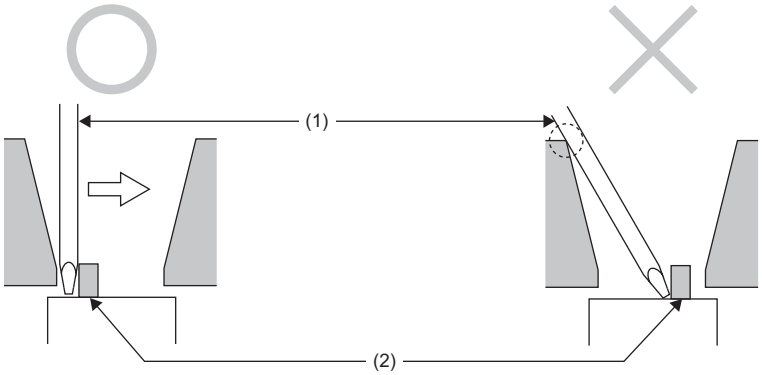
The function setting switches 1 to 3 setting is determined by the status when the FPGA module is powered on.
Do not change the switches while the FPGA module is on. If any of the switches is changed while the FPGA module is on, any of the errors from Function setting switch 1 changed error (error code: 1041H) to Function setting switch 3 changed error (error code: 1043H) occurs and the ERR. LED flashes. The operation mode, CC-Link IE TSN Class, and communication speed are not changed even if any of the switches is changed. After setting the switch back to the previous setting, turn on Error clear request flag (RYA) to clear the error state and turn off the ERR. LED.

■Function setting switches 4 to 10

The function setting switches 4 to 10 setting is determined by the status when the FPGA module is on.

Precautions

Slide one function setting switch at a time horizontally. Do not hold the screwdriver at an angle or pivot it off the edge of the case while working a function setting switch, since damage or deformation may result.



(1) Flathead screwdriver
(2) Function setting switch

7.2 Installation Environment and Installation Position

Installation environment

Installation location

Do not install the FPGA module to the following environment:

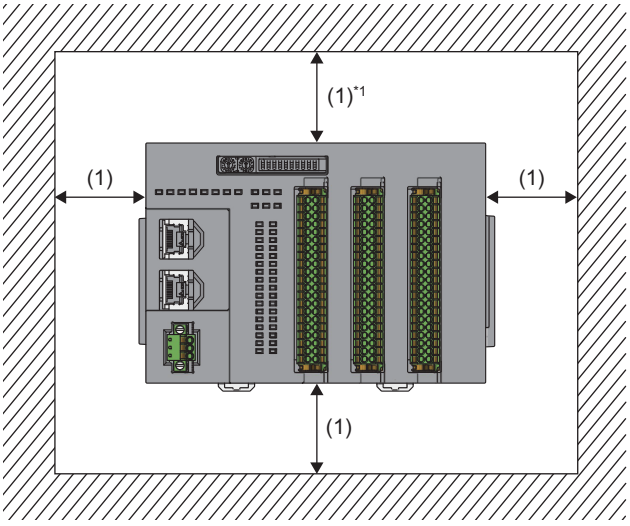
- Ambient temperature is outside the range of 0 to 55℃;
- Ambient humidity is outside the range of 5 to 95% RH;
- Condensation occurs due to rapid temperature change;
- Corrosive gas or combustible gas is present;
- There are a high level of conductive powder such as dust and iron powder, oil mist, salinity, or organic solvent;
- The FPGA module is exposed to direct sunlight;
- A strong electric field or strong magnetic field is generated; and
- The FPGA module is subject to vibration and shock.

Installation surface

Install the FPGA module on a flat surface. Unevenness on the installation surface causes application of an excessive force to the printed-circuit board, which may lead to a malfunction.

Installation position

When installing the FPGA module in a control panel, provide a clearance between the module and the sides of the control panel or other parts as shown below to ensure good ventilation and facilitate module change.



(1) 60mm or more

*1 When a JTAG connector is used, provide the clearance of 105mm or more.

Installation orientation

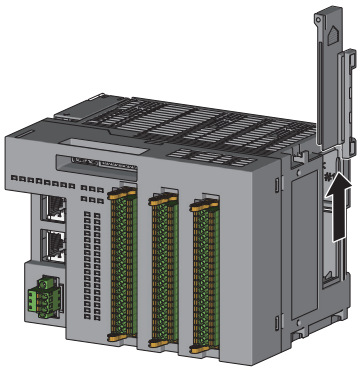
Only the horizontal installation is available. Do not use the other orientations for installing the module.

7.3 Installation

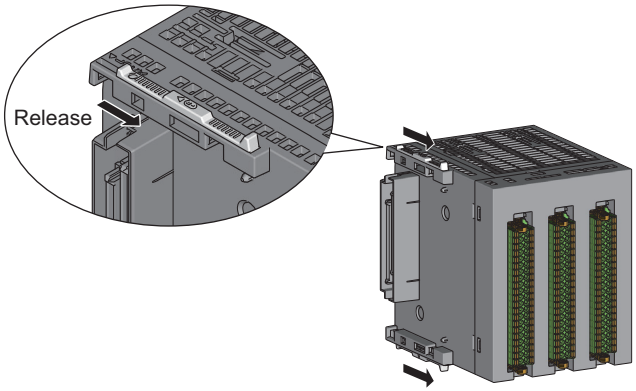
Connecting an extension module

By connecting the FPGA module to an extension module, the number of digital input points and digital output points can be increased, or analog input and analog output can be added.
Only one extension module can be connected to a main module. There are no restrictions on the combinations of a main module and an extension module. Each main module can be connected to any extension modules. Note that if an extension module is disconnected during operation, a major error occurs and the FPGA control stops.

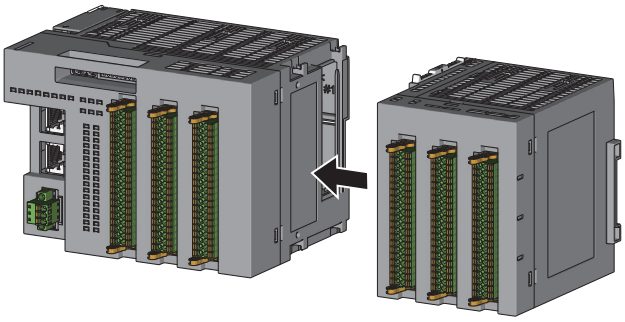
Connection procedure



1. Remove the cover on the side of the main module. Keep the removed cover, not disposing of it.



2. To release the module joint levers (two points) on the side of the extension module, slide them toward the front of the module.



3. Insert the connector of the extension module into that of the main module so that they are securely engaged.

4. To lock the module joint levers, slide them toward the rear of the module. After the levers are locked, check that the modules are securely connected. Be sure to lock the levers both on the top and bottom of the module.

Precautions

Lock the module joint levers securely. Failure to do so may cause malfunction, failure, or drop of the module.

Removal procedure

Disconnect the extension module by reversing the procedure above.

Precautions

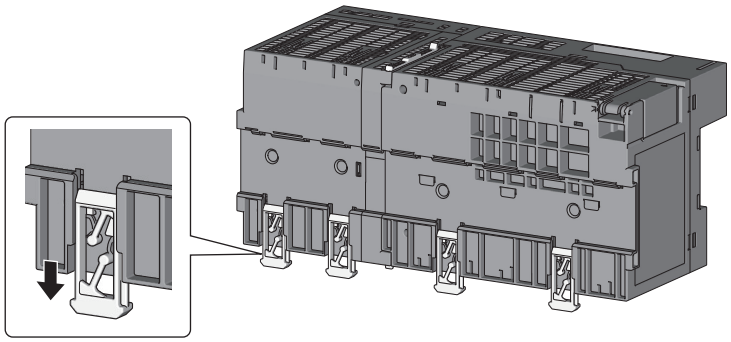
Shut off the external power supply (all phases) used in the system before connecting or removing the extension module.

How to mount a module on a DIN rail

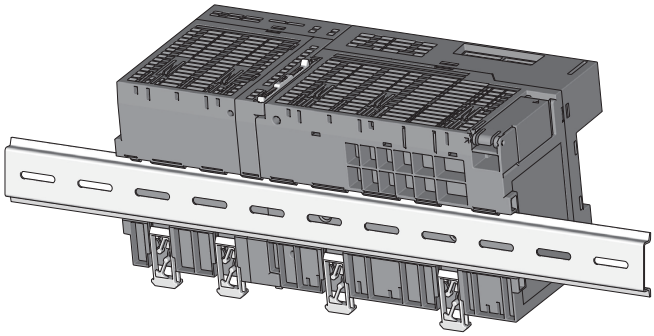
Point

The method for fixing the DIN rail stopper is an example. Fix the module in accordance with the manual for the DIN rail stopper used.

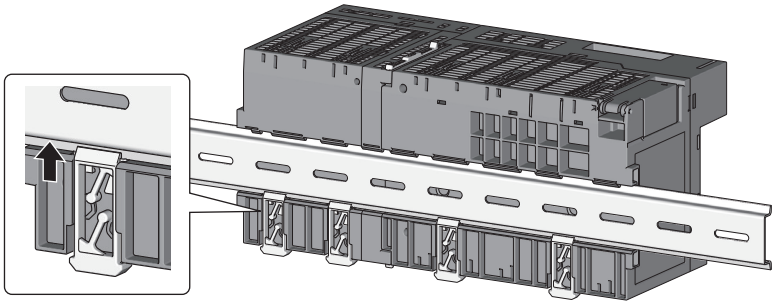
Mount procedure



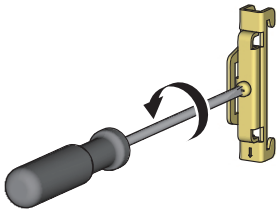
1. Pull down all DIN rail hooks on the back of the module until they click.



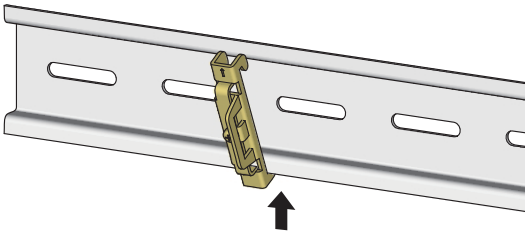
2. Hang the upper tabs of the module on the DIN rail, and push the module in position.



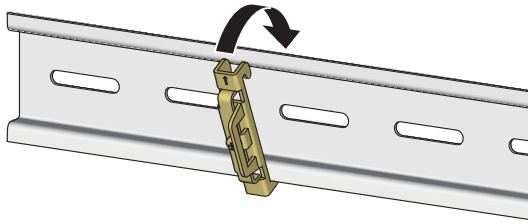
3. Lock the DIN rail hooks to the DIN rail to secure the module in position. Push each hook upward until it clicks. If the hooks are beyond the reach, use a tool such as a screwdriver.



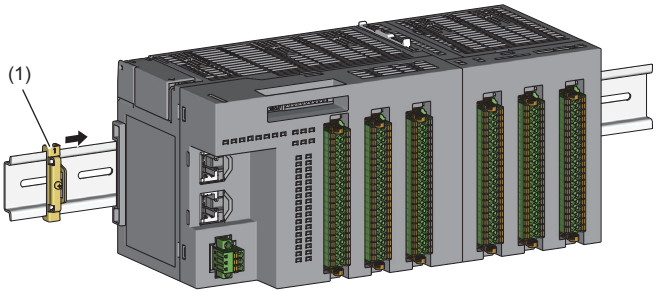
4. Loosen the screw on the DIN rail stopper.



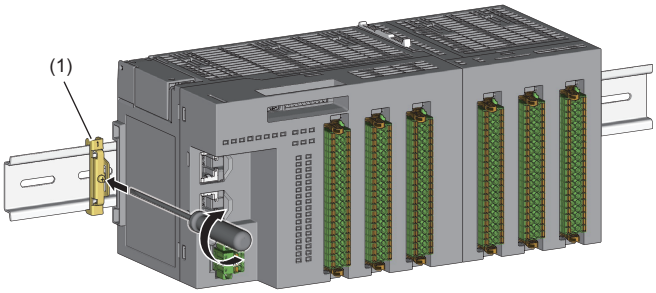
5. Hang the bottom hook of the stopper to the bottom of the DIN rail. Do not place the stopper upside down. Place it correctly by checking the arrow on the front of the stopper and referring to the figure on the left.



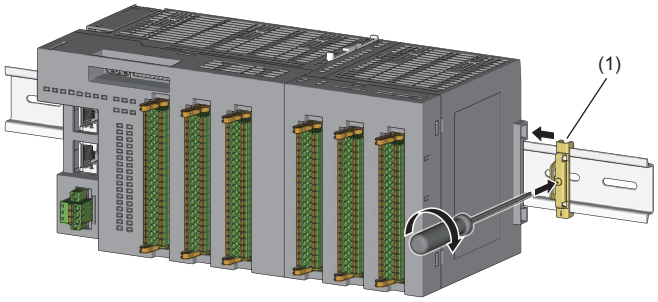
6. Hang the upper hook of the stopper to the upper of the DIN rail.



7. Slide the stopper (1) up to the left side of the module.



8. Hold the stopper (1) in the direction opposite to the arrow on the stopper and tighten the screw with a screwdriver.



9. Install another stopper on the right side of the module in the same manner. Note that the stopper must be installed upside down for the right side.

Precautions

Do not slide a module from the edge of the DIN rail when mounting it. Doing so may damage the module.

Removal procedure

Remove the module from the DIN rail by reversing the above procedure.

Applicable DIN rail model (compliant with IEC 60715)

- TH35-7.5Fe
- TH35-7.5Al

Space between DIN rail mounting screws

When installing a DIN rail, tighten the screws at intervals of 200mm or less.

DIN rail stopper

Use a stopper that can be attached to the DIN rail.

7.4 Wiring

Wiring to terminal block for module power supply and FG

Tightening torque

Tighten the terminal block mounting screws within the following tightening torque range. Overtightening the screws may damage the module case.

Screw type	Tightening torque range
Terminal block mounting screw (M2.5 screw)	0.2 to 0.3N·m

Wire to be used

The following table describes the wire to be connected to the terminal block for module power supply and FG.
When using the FPGA module as a UL listed product, use the wire listed below for wiring to the terminal block.

Applicable wire size	Type	Length	Material	Temperature rating	Strip length of wire
Stranded wire: 0.3 to 1.5mm² (22 to 16 AWG) Terminal hole size: 2.4mm × 1.5mm	Twisted pair cable	10m or shorter When a noise filter is installed, it should be placed within 3m from the module.	Copper	75℃ or more	10mm

Applicable solderless terminals

For bar solderless terminals, the products in the following table are recommended. For processing methods of the cable terminal, such as a strip length of wire, follow the specifications of the bar solderless terminal to be used. For processing, use a tool recommended by the manufacturer of the terminals. When using the FPGA module as a UL listed product, use the UL listed bar solderless terminals listed below.

Terminal shape	Model	Applicable wire size	Bar solderless terminal tool	Contact
Ferrule (with insulation sleeve)	NF 0.5-8, NF 0.5-10	0.5mm² (20 AWG)	NH-79A	NICHIFU Co., Ltd.
	NF 0.75-8, NF 0.75-10	0.5 to 0.75mm² (18 AWG)		
	AI0.34-10TQ	0.34mm² (22 AWG)	CRIMPFOX6	PHOENIX CONTACT GmbH & Co. KG
	AI0.5-10WH	0.5mm² (20 AWG)		
	AI0.75-10GY	0.75mm² (18 AWG)		
Ferrule (without insulation sleeve)	A0.5-10	0.5mm² (20 AWG)		
	A0.75-10	0.75mm² (18 AWG)		
	A1-10	1.0mm² (18 AWG)		
	A1.5-10	1.5mm² (16 AWG)		

Installing and removing the terminal block

To remove the terminal block, loosen the terminal block mounting screws with a flathead screwdriver.
To install the terminal block, tighten the terminal block mounting screws with a flathead screwdriver.
Undertightening can cause drop of the screw, short circuit, or malfunction.

Connecting and disconnecting the cable

To connect the cable, fully insert a wire with a bar solderless terminal into a wire insertion opening.
After inserting the wire, pull it lightly to check that it is securely clamped.

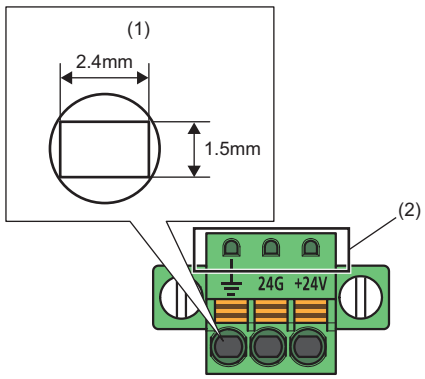
Point

Continuity can be checked with the test terminal.
Use the following test plug to check continuity.
• PHOENIX CONTACT GmbH & Co. KG test plug (ϕ1.0mm): MPS-MT 1-S4-B RD, MPS-MT 1-S

To disconnect the cable, push in the open/close button with a flathead screwdriver.
With the button pushed in, pull out the wire with a bar solderless terminal.

Precautions

- Use a bar solderless terminal for wiring to the push-in type spring clamp terminal block. If a stripped wire is inserted into a wire insertion opening, the wire cannot be securely clamped.
- For the wire strip length, follow the specifications of the bar solderless terminal used. To attach a bar solderless terminal to a wire, use a crimping tool.
- Before inserting a bar solderless terminal into a wire insertion opening (1), check the shape of the opening and the shape of the terminal, and insert the terminal paying attention to the orientation. If a bar solderless terminal larger than the wire insertion opening (1) is inserted, the terminal block may be damaged.



(1) Wire insertion opening
(2) Test terminal

Ethernet cables

Wiring method

■Installation procedure

1. Power off the FPGA module and the external device.
2. Push the Ethernet cable connector into the FPGA module until it clicks. Pay attention to the connector's orientation.
3. Power on the FPGA module.
4. Power on the external device.
5. Check that the P1 LINK LED/P2 LINK LED of the port into which the Ethernet cable is connected is on. *1*2

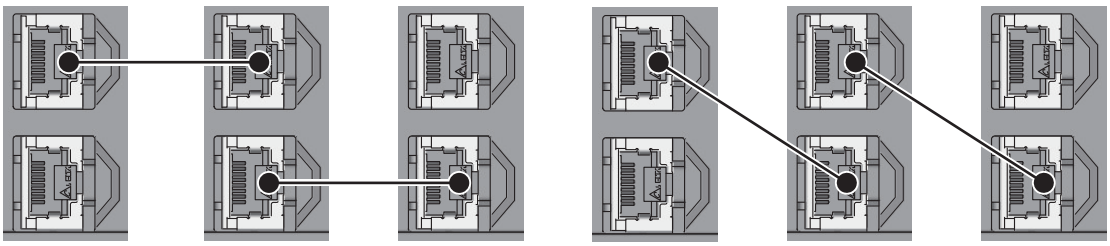
*1 The time taken for P1 LINK LED/P2 LINK LED to turn on after connection of the cable may vary. The LINK LED normally turns on in a few seconds. However, if link-up processing is repeated due to the status of a device on the line, the longer time may be required. If the P1 LINK LED/P2 LINK LED does not turn on, refer to the following and take a corrective action.
☞ Page 435 When the P1 LINK LED or P2 LINK LED turns off

*2 When connecting the FPGA module with the communication speed of 100Mbps to a device with the speed of 100Mbps, enable the auto-negotiation for that device.

Point

Both the P1 (upper) and P2 (lower) connectors can be used.

- When using one of them in a star topology, either P1 or P2 can be connected.
- When using both connectors (P1 and P2) in a line topology and a ring topology, P1-P1, P2-P2, and P1-P2 connections are possible.



■Disconnection procedure

1. Power off the FPGA module.
2. With the latch of the Ethernet cable pressed, unplug the cable.

Precautions

■Installing Ethernet cables

- Place the Ethernet cables in a duct or clamp them. If not, dangling cable may swing or inadvertently be pulled, resulting in damage to the module or cables or malfunction due to poor contact.
- Do not touch the core of the connector of the cable or the module, and protect it from dirt and dust. If any oil from your hand, or any dirt or dust sticks to the core, it can increase transmission loss, causing data link to fail.
- Check that the Ethernet cables to be used are not broken or short-circuited, and that connectors are connected securely.

■Broken cable latch

Do not use Ethernet cables with broken latches. Doing so may cause the cable to unplug or malfunction.

■Connecting and disconnecting an Ethernet cable

Hold the connector part when connecting and disconnecting the Ethernet cable. Pulling the cable connected to the module may result in damage to the module or cable or malfunction due to poor contact.

■Maximum segment length for the Ethernet cable (Maximum cable length)

The maximum segment length is 100m. However, the distance may be shorter depending on the operating environment of the cable. For details, contact the manufacturer of the cables used.

■Bending radius of an Ethernet cable

There are restrictions on the bending radius of the Ethernet cable. Check the bending radius in the specifications of the Ethernet cables used.

■Connector to which an Ethernet cable is not connected

Attach a connector cover to prevent dirt and dust from entering the FPGA module and prevent FPGA module failure and malfunction caused by static electricity.

Wiring to I/O terminal block

Wire to be used

The following table describes the wire to be connected to the I/O terminal block.

When using the FPGA module as a UL listed product, use the wire listed below for wiring to the terminal block.

Applicable wire size	Type	Length	Material	Temperature rating	Strip length of wire
Stranded wire: 0.3 to 1.5mm² (22 to 16 AWG)	Shielded cable	• DC output: Within 3m • Differential output: Within 8m • Differential input/ output: Within 10m • DC/differential input: Within 30m	Copper	75℃ or more	10mm

Applicable solderless terminals

For bar solderless terminals, the products in the following table are recommended. For processing methods of the cable terminal, such as a strip length of wire, follow the specifications of the bar solderless terminal to be used. For processing, use a tool recommended by the manufacturer of the terminals. When using the FPGA module as a UL listed product, use the UL listed bar solderless terminals listed below.

Terminal shape	Model	Applicable wire size*1	Bar solderless terminal tool	Contact
Ferrule (with insulation sleeve)	AI0.34-10TQ	0.34mm² (22 AWG)	CRIMPFOX6	PHOENIX CONTACT GmbH & Co. KG
	AI0.5-10WH	0.5mm² (20 AWG)		
	AI0.75-10GY	0.75mm² (18 AWG)		
Ferrule (without insulation sleeve)	A0.5-10	0.5mm² (20 AWG)		
	A0.75-10	0.75mm² (18 AWG)		
	A1-10	1.0mm² (18 AWG)		
	A1.5-10	1.5mm² (16 AWG)		

*1 When using a solderless terminal with an insulation sleeve, select the terminal whose applicable wire size is 0.75mm² or smaller.

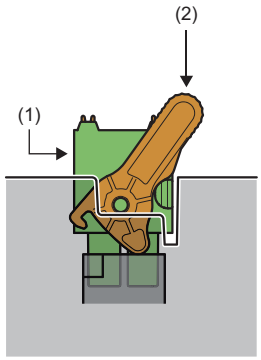
Installing and removing the I/O terminal block

The following describes how to install and remove the I/O terminal block.

■Lock and release lever positions

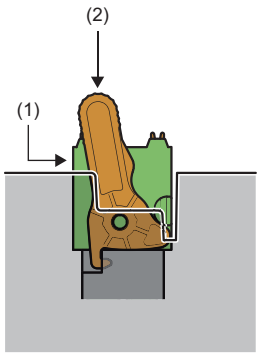
To make it easy to install and remove the I/O terminal block, a three-stage positioning stopper is attached so that the lever does not freely turn around.

When installing or removing the terminal block, turn the lever to the lock or release lever position.



1. Release lever position

This lever position (2) shows the state in which the I/O terminal block (1) has been completely pulled out from the FPGA module. Turn the lever from the lock lever position to the release lever position and lift the terminal block from the module.



2. Lock lever position

This lever position shows the state in which the I/O terminal block (1) completely fits the FPGA module. Check the lock lever position (2) and pull the terminal block lightly to check that the module completely fits the terminal block.

■Removal procedure

Turn the lever to the release lever position and remove the I/O terminal block from the FPGA module.

■Installation procedure

Turn the lever to the lock lever position and push the I/O terminal block. When the terminal block is fully pushed in, the hook of the lever hangs on the FPGA module and the module fits the terminal block.

Point

The terminal block can be inserted with the lever in positions other than the lock lever position. After insertion, check that the lever is in the lock lever position.

Signal names and wiring

For the signal names of the I/O terminal block and wiring of the external device, refer to the specifications of each module.
(☞ Page 33 Performance Specifications, Page 74 External Wiring)
Incorrect wiring can cause malfunction of or damage on the FPGA module.

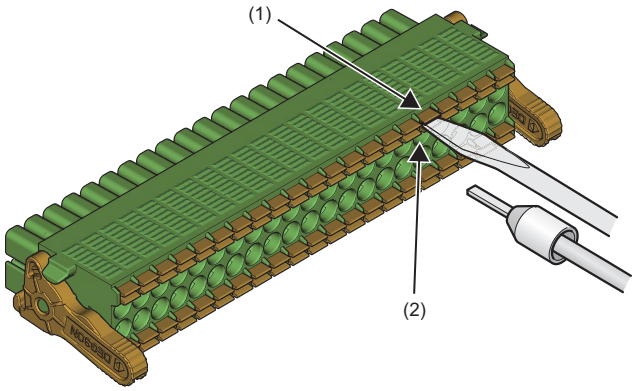
Connecting and disconnecting a cable

■Connecting the cable

Strip the cable as follows.

- Wire strip length: 10mm

Insert a wire whose tip was processed into a wire insertion opening (2) and push it all the way to the back.
If the wire cannot be inserted by this method, insert the wire while pressing the release button (1) using a flathead screwdriver with a tip width of 2.0 to 2.5mm. Once the wire is inserted all the way to the back, remove the flathead screwdriver.



Point

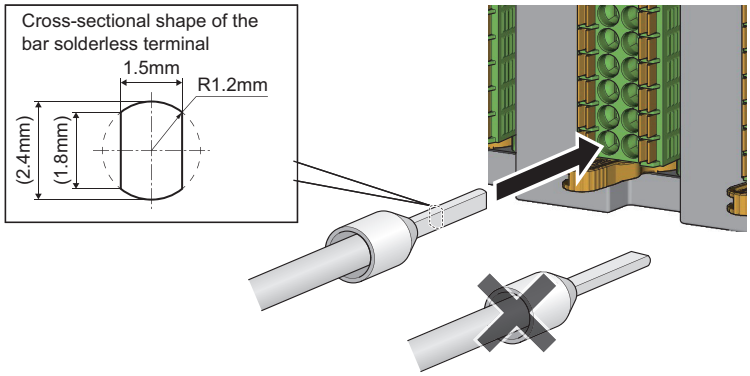
Pull the wire or bar solderless terminal lightly to check that it is securely clamped.

■Disconnecting the cable

Pull the wire while pressing the release button using a flathead screwdriver with a tip width of 2.0 to 2.5mm.

Precautions

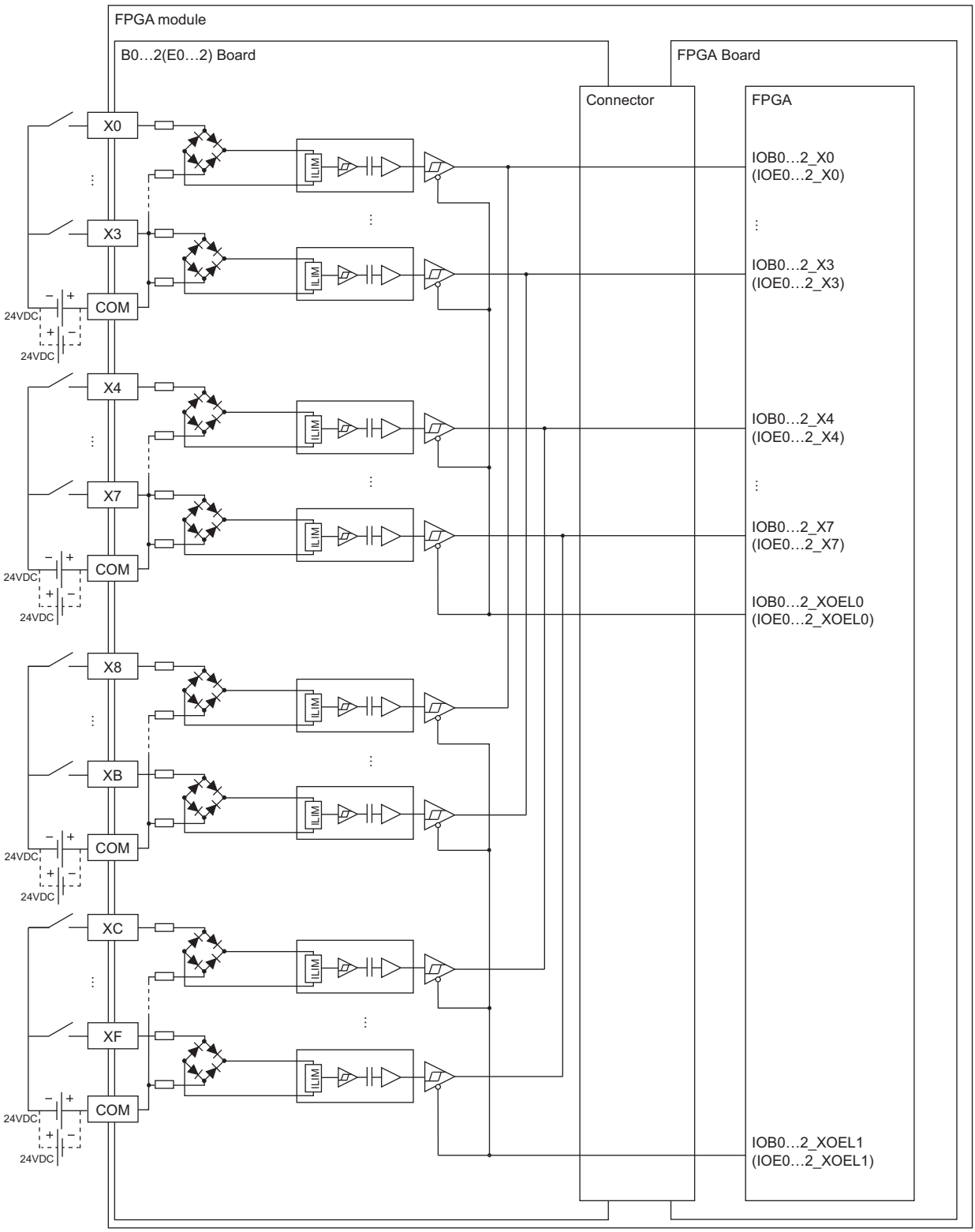
- Use a bar solderless terminal for the wiring to the I/O terminal block. If a stripped wire is inserted to a wire insertion opening, the wire cannot be clamped securely.
- Use a crimping tool to connect a bar solderless terminal to a wire. (☞ Page 70 Applicable solderless terminals)
- When inserting a bar solderless terminal, check that the size of the terminal and its insertion direction are correct to prevent the terminal from getting stuck in or damage to the terminal block. When using a bar solderless terminal other than the applicable solderless terminals, make sure that the cross-sectional shape of the terminal after processing (the size includes an error in processing) is smaller than the size shown below. For the correct terminal insertion direction, refer to the figure below.



7.5 External Wiring

DC input wiring

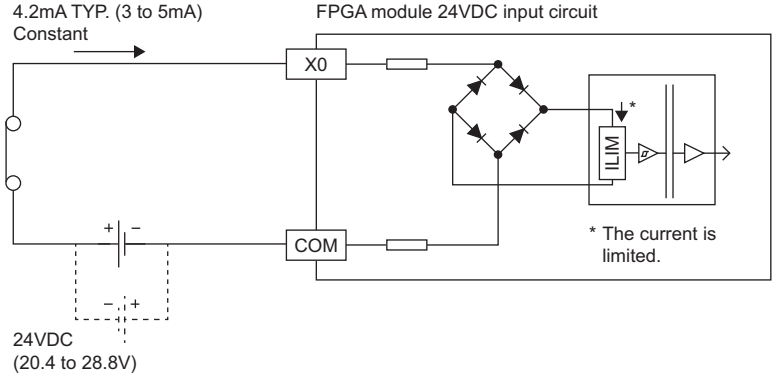
This section describes the wiring to the DC input terminal. The polarity of the common can be either way, as the signal is input through the diode bridge. Note that the common terminal is common to each of four points. (Example: X0 to X3)
Consider that the constant amount of input current of 4.2mA TYP. (3 to 5mA) flows at power-on regardless of the input voltage, when selecting connected devices and performing wiring.



Precautions

■Current flow in the DC input circuit

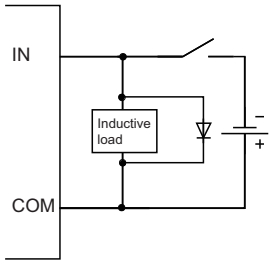
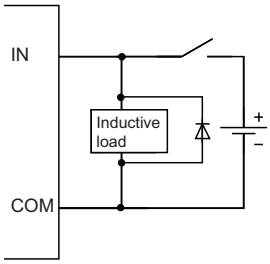
The input current at power-on is controlled to be a certain current value by the internal circuit, and thus the constant amount of current of 4.2mA TYP. (3 to 5mA) flows regardless of the input voltage. Consider this, and select connected devices and perform wiring.



■Measures against counter-electromotive force

When connecting an inductive load, connect a diode in parallel with the load. Use the diode that satisfies the following conditions:

- A reverse breakdown voltage is ten times as high as the circuit voltage or more.
- A forward current is twice as high as the load current or more.

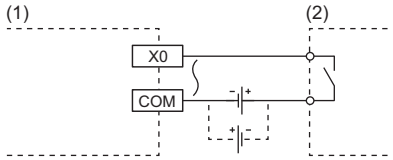
Positive common	Negative common
	

Wiring example

The following show examples of wiring between the DC input terminal and a connectable DC input device (DC output type).

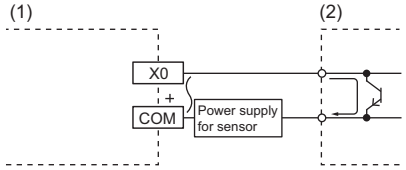
■Contact output type

The following shows an example of wiring between the DC input terminal (1) and the contact output type (2).



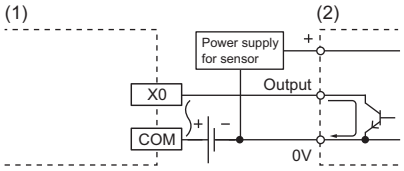
■DC two-wire type

The following shows an example of wiring between the DC input terminal (1) and the DC two-wire type (2).

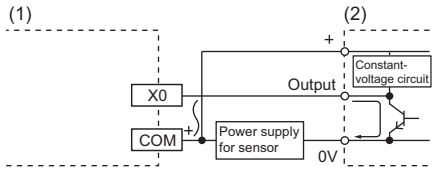


■Transistor output type

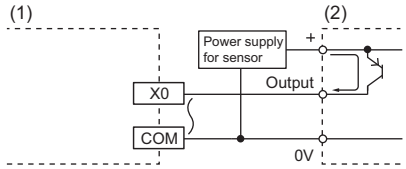
The following shows an example of wiring between the DC input terminal (1) and the NPN open collector output type (2).



The following shows an example of wiring between the DC input terminal (1) and the NPN current output type (2).

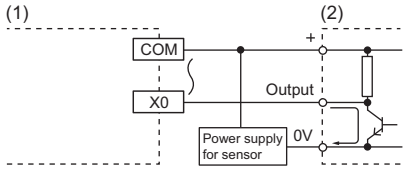


The following shows an example of wiring between the DC input terminal (1) and the PNP current output type (2).



■Voltage output type

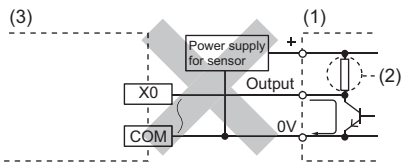
The following shows an example of wiring between the DC input terminal (1) and the voltage output type (2).



Point

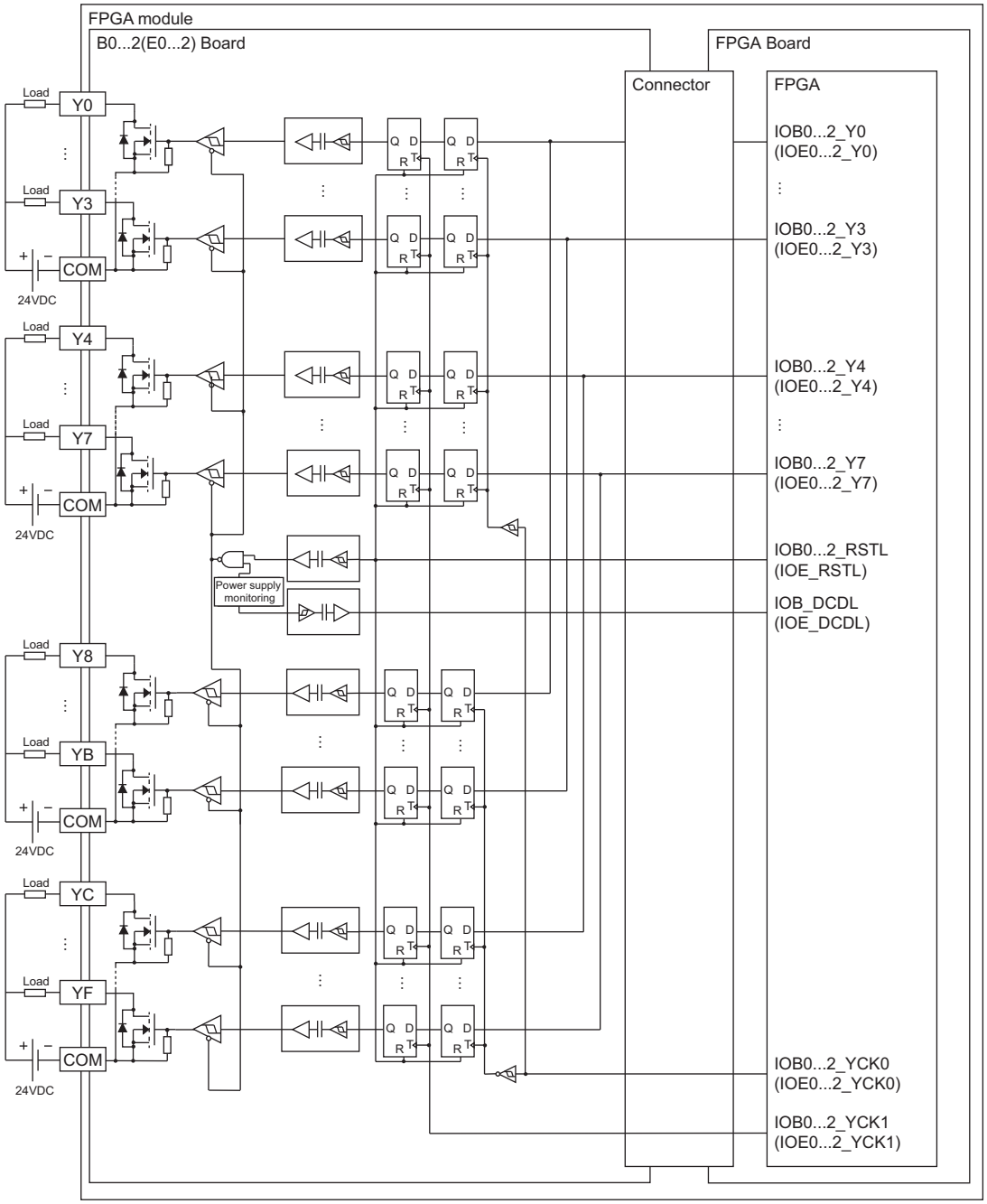
When connecting the DC input terminal to a sensor of voltage output type (1), do not perform the wiring as shown below.

Doing so will cause the current to flow to the DC input terminal through the sensor pull-up resistor (2). As a result, the input current may not satisfy the ON current to the DC input terminal (3) and the input signal may not turn on.



Transistor output wiring

This is the sink output type that the current flows into the output terminal when the output element (FET) is turned on.
There is a common terminal at intervals of four points. (Example: Y0 to Y3)



Precautions

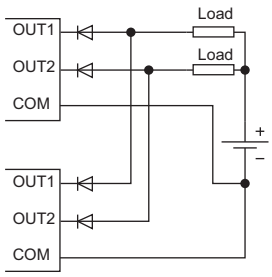
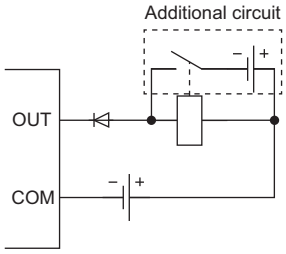
■Short-circuit protection

To prevent burnout or damage of the external devices and module if a load short-circuit occurs in the output circuit, install a fuse for each point of external terminal. The following lists the fuses whose operation has been verified by Mitsubishi Electric.

Model name	Rated current	Contact
312.750	0.75A	Littelfuse, Inc.
216.800	0.8A	

■Measures against reverse current

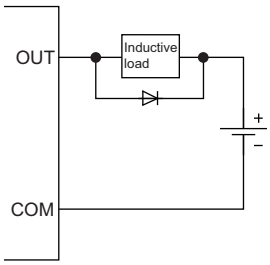
In the following connections, a reverse current flows to the output element, which can cause failure.
When wiring, install diodes as shown in the figures below.

Parallel connection to one load	When configuring another circuit in parallel
	

■Counter-electromotive force

When connecting an inductive load, connect a diode in parallel with the load.
Use the diode that satisfies the following conditions:

- A reverse breakdown voltage is ten times as high as the circuit voltage or more.
- A forward current is twice as high as the load current or more.



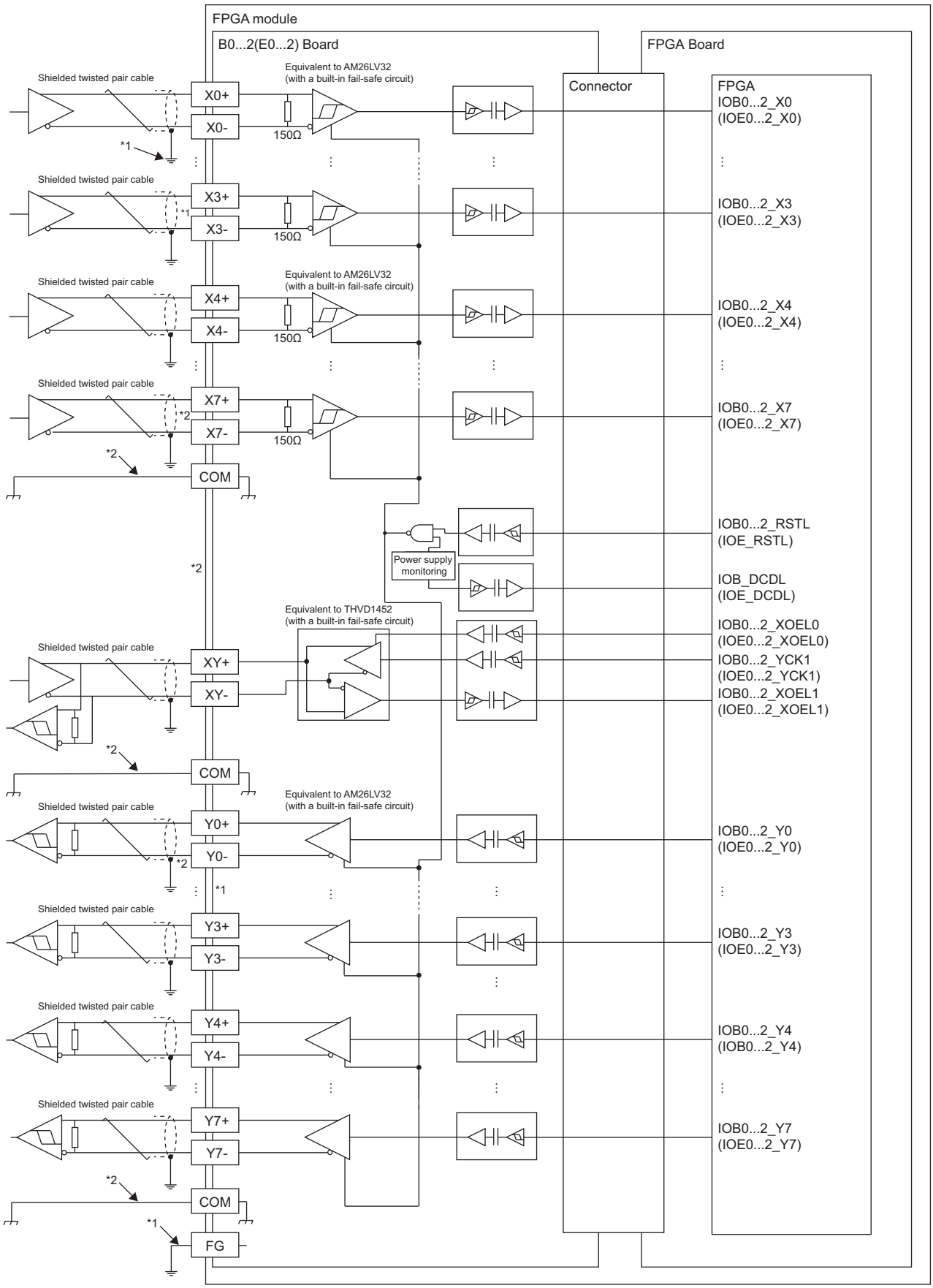
■Transistor output terminal element protection

If excessive noise affects the transistor output terminals, the output may be turned on to protect the output element.
Adjust the voltage between the transistor output terminals not to exceed the operating load voltage range by taking measures such as the following:

- When an inductive load such as a relay is used, a surge suppressor is required on the load side as well. Take appropriate measures referring to the measures against the counter-electromotive force.
- To prevent excessive noise, avoid installing power cables together with I/O cables.

Differential input/output wiring

The differential input/output has receivers and transceivers that satisfy the requirements of the TIA/EIA-422-B and TIA/EIA-485-A standards.
When an external device has a common terminal, connecting the common terminal is recommended because a potential difference between the common of external device and the common of module can cause the module to fail or malfunction.
There is a common terminal for input terminals and output terminals at intervals of eight points and a common terminal for I/O shared terminals at intervals of one point.

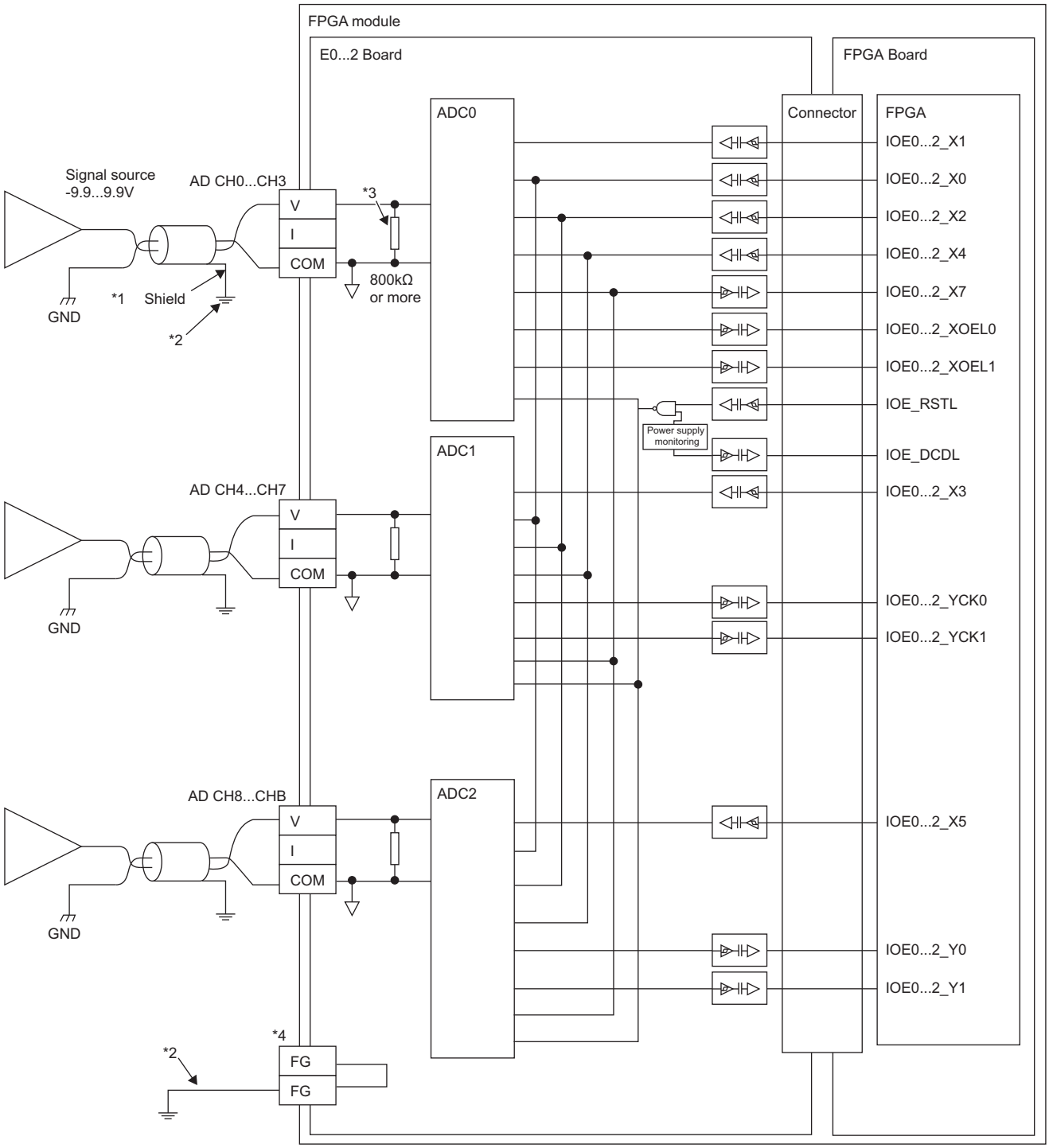


*1 Ground the shielded cable of a wire for each channel as well as the FG terminal.

*2 When a potential difference is found between the COM terminal and the GND of an external device, connect the COM terminal to the GND of the external device.

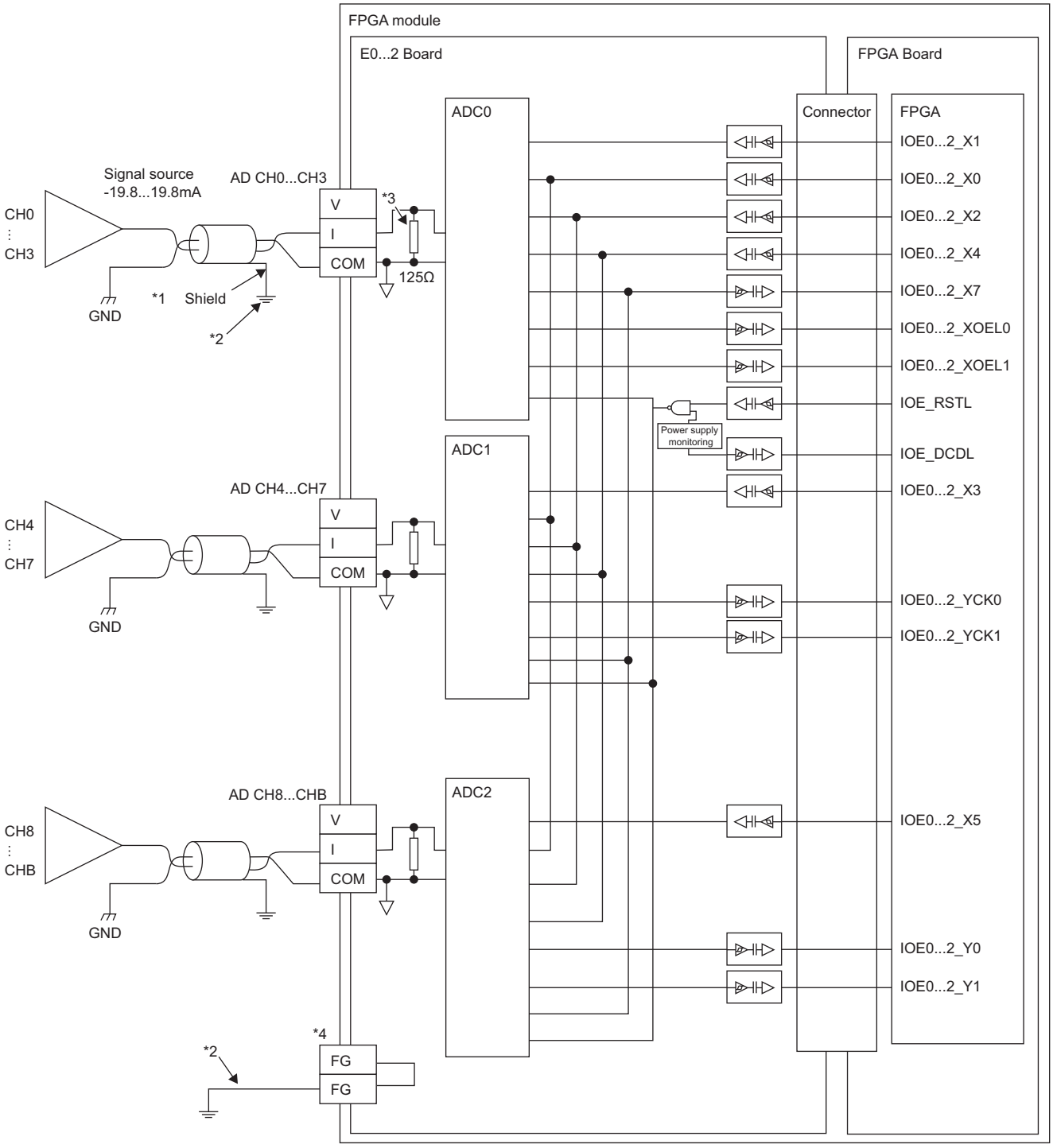
Analog input wiring

Using a voltage input signal



*1 For the cable, use the 2-core shielded twisted pair cable.
*2 Ground the shielded cable of a wire for each channel as well as the FG terminal.
*3 Indicates the internal input resistance of the NZ2EX2S-D41A01.
*4 The FG terminal is common to analog input and analog output.

Using a current input signal



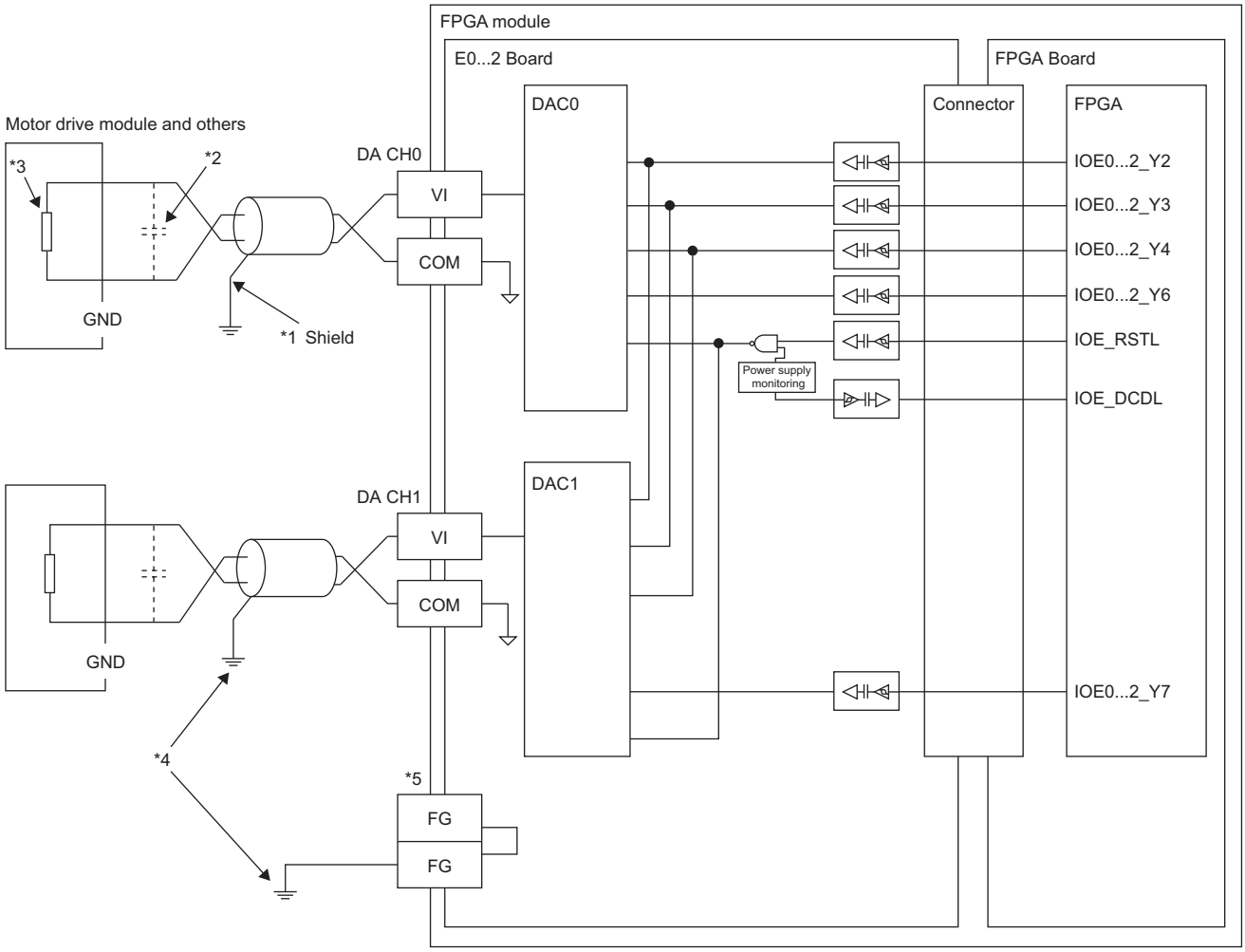
*1 For the cable, use the 2-core shielded twisted pair cable.
*2 Ground the shielded cable of a wire for each channel as well as the FG terminal.
*3 Indicates the internal input resistance of the NZ2EX2S-D41A01.
*4 The FG terminal is common to analog input and analog output.

Precautions

To obtain the maximum performance from the A/D conversion function and improve the system reliability, external wiring that is noise resistant is required. Precautions for external wiring are as follows.

- Use separate cables for the AC control circuit and the external input signals of the analog input terminal to avoid effects of the AC side surges or induction.
- Do not install cables near or bundle cables with any main circuit lines, high voltage lines, or load cables for equipment other than the programmable controller. Doing so may cause the system to be susceptible to noise, surges, or induction.
- Ground shielded wires or shielded cables based on single-point ground. However, depending on the external noise conditions, it may be better to ground them externally.
- If A/D conversion is enabled while terminals of unused channels are open, an undefined digital value may be output. To prevent this, short-circuit the COM terminal and the input terminal (V or I) of the unused channels.

Analog output wiring



*1 For the cable, use the 2-core shielded twisted pair cable.

*2 If there is noise or ripples in the external wiring, connect a 0.1 to 0.47μF capacitor (25V or higher voltage-resistant product) to the input terminal of the external device.

*3 The external load resistance values are as follows:
Voltage output: 1kΩ to 1MΩ
Current output: 50Ω to 600Ω

*4 Ground the shielded cable of a wire for each channel as well as the FG terminal.

*5 The FG terminal is common to analog input and analog output.

Precautions

To obtain the maximum performance from the D/A conversion function and improve the system reliability, external wiring that is noise resistant is required. Precautions for external wiring are as follows.

- Use separate cables for the AC control circuit and the external output signals of the analog output terminal or the external power supply to avoid effects of the AC side surges or induction.
- Do not install cables near or bundle cables with any main circuit lines, high voltage lines, or load cables for equipment other than the programmable controller. Doing so may cause the system to be susceptible to noise, surges, or induction.
- Ground shielded wires or shielded cables based on single-point ground. However, depending on the external noise conditions, it may be better to ground them externally.

PART 4 SETTINGS

This part consists of the following chapters.

8 FPGA MODULE CONFIGURATION TOOL

This chapter describes the FPGA Module Configuration Tool used to write to the FPGA module.
For the FPGA Module Configuration Tool, please consult your local Mitsubishi representative.

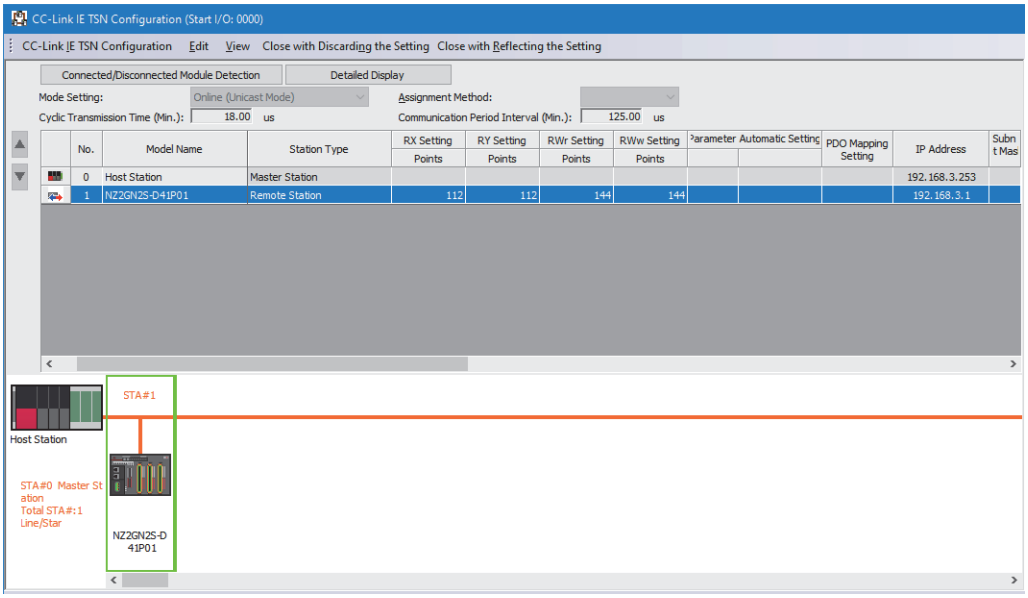
8.1 Starting Up and Finishing

When using CC-Link IE TSN communication mode

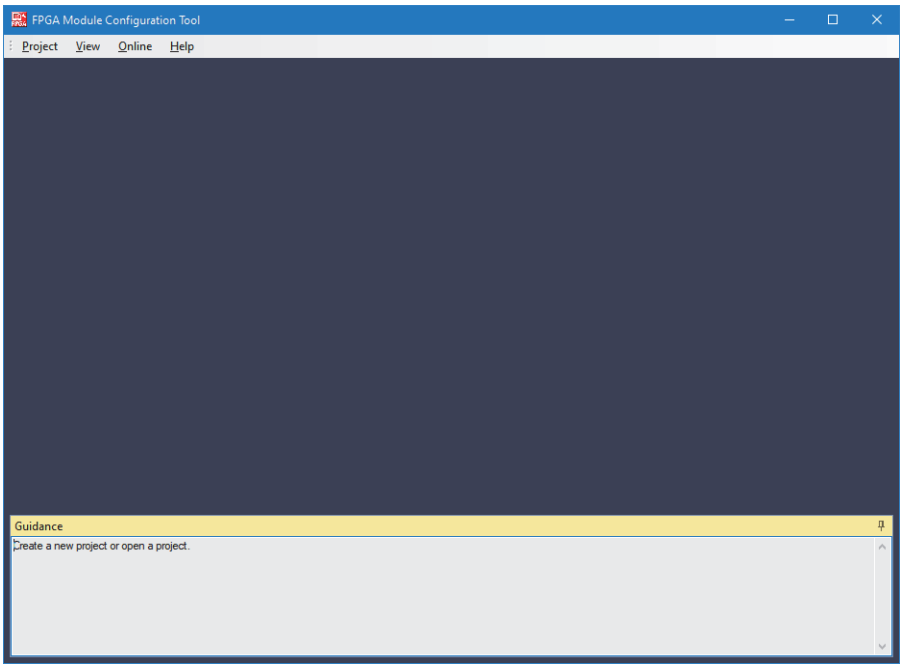
The following describes the startup method when using CC-Link IE TSN communication mode.

Operating procedure

1. Display the CC-Link IE TSN Configuration window and double-click the target module.



2. The FPGA Module Configuration Tool will start.

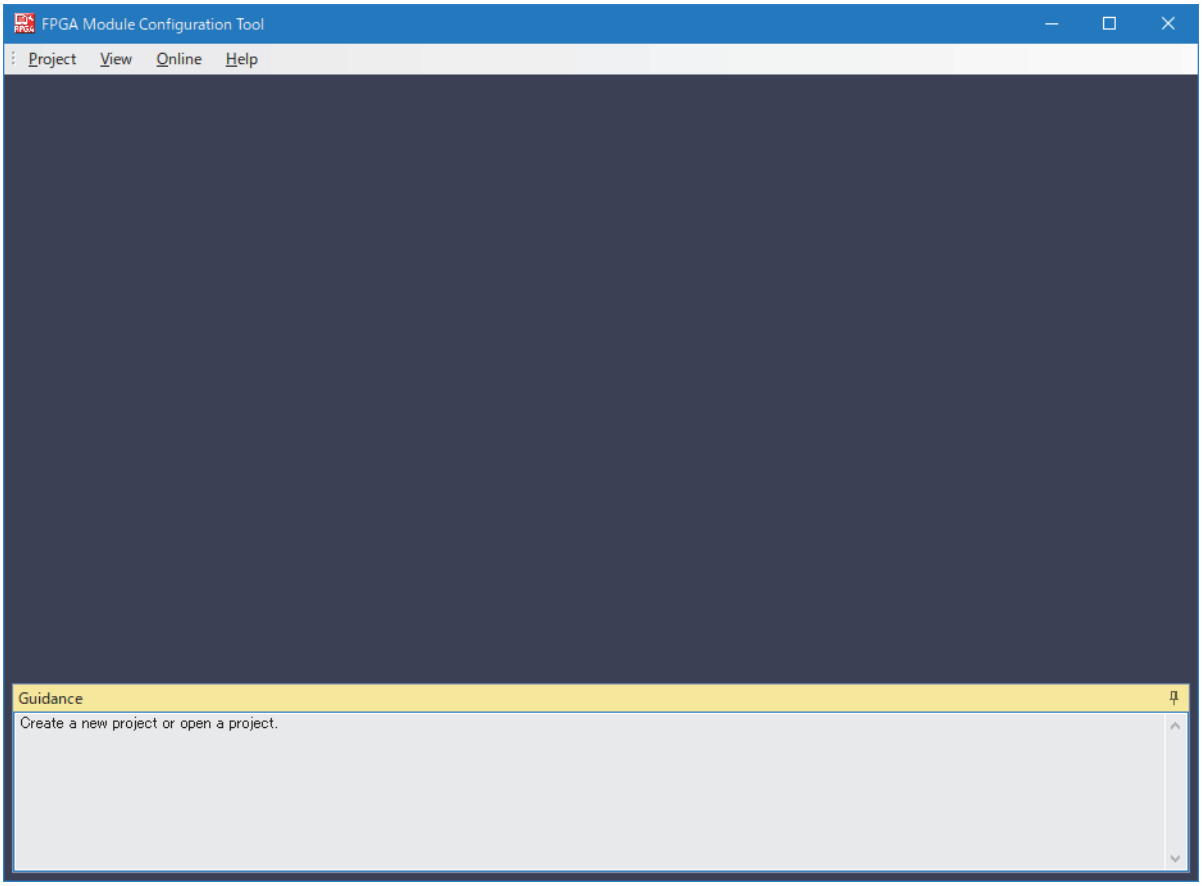


When using standalone mode

Here is how to start when using standalone mode.

Operating procedure

1. Start FPGAUnitSettingTool from "MELSOFT" in the Windows Start menu.
2. The FPGA Module Configuration Tool will start.

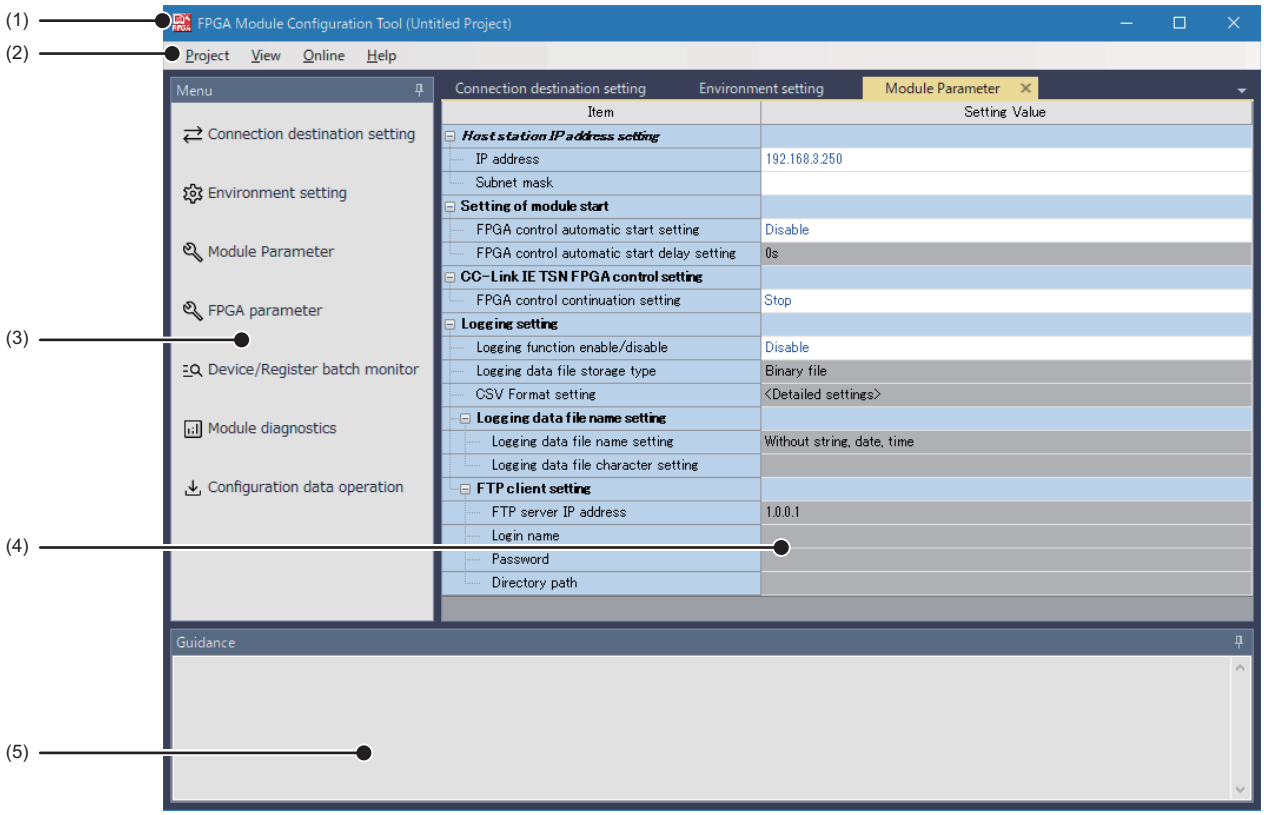


Exit

In the FPGA Module Configuration Tool, select [Project] ⇨ [Exit].

8.2 Window Configuration

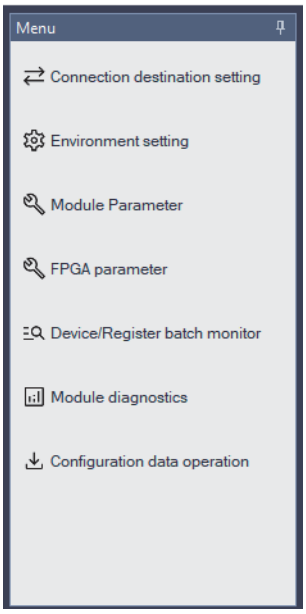
The overall window configuration is shown below.



No.	Window	Reference
(1)	Title bar	—
(2)	Menu bar	Page 91 FPGA Module Configuration Tool Menu List
(3)	Menu window	Page 89 Menu window
(4)	Work window	Page 90 Work window
(5)	Guidance window	Page 90 Guidance window

Menu window

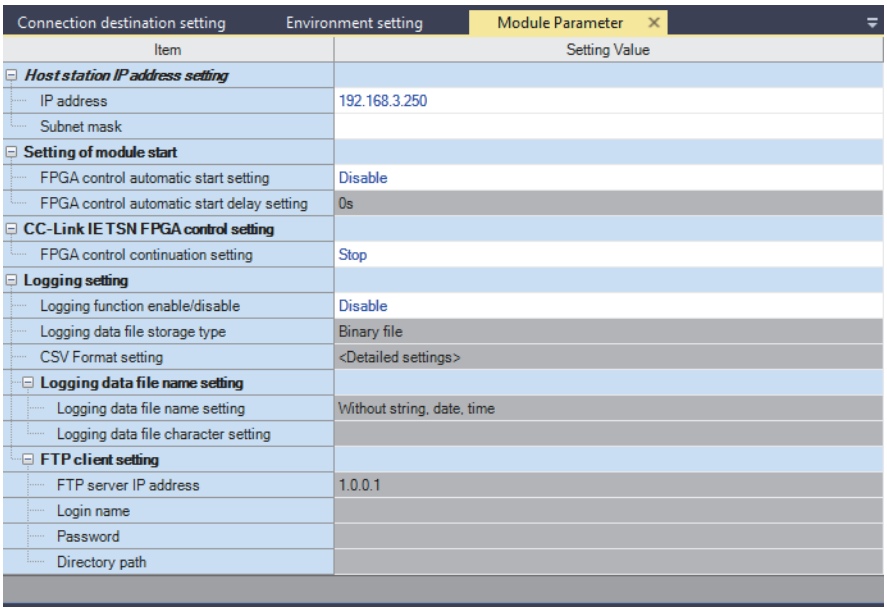
The Menu window displays a navigation menu allowing execution of each function.



Item	Description	Reference
Connection destination setting	Set the connection destination FPGA module.	Page 113 Connection destination setting
Environment setting	Set the communication settings, timeout time, and other settings on the personal computer side.	Page 127 Environment setting
Module parameter	Set the module parameters.	Page 95 Module parameters
FPGA parameter	Set the FPGA parameters.	Page 98 FPGA parameters
Device/Register batch monitor	Displays the contents of link devices, remote buffers, or FPGA register areas.	Page 117 Batch monitor display
Module diagnostics	Displays basic information about the FPGA module, such as the status of LEDs and the status of errors, which is displayed collectively.	Page 121 Module diagnostics
Configuration data operation	Verifies or downloads the configuration data created using the FPGA development software to the configuration ROM in the FPGA module.	Page 124 Configuration data operation

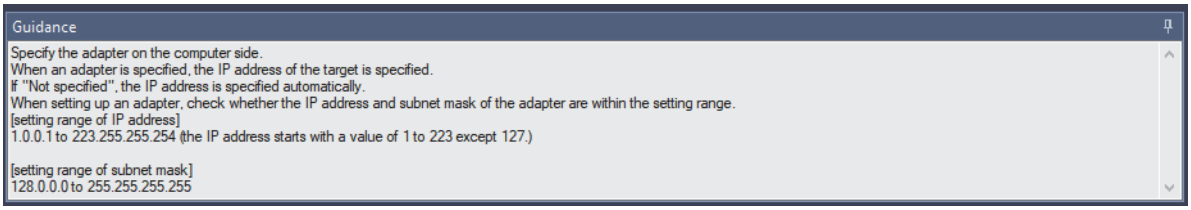
Work window

This window is used when performing various settings and module operations. The window to be operated will switch when an item is selected in the menu window. The window can also be switched by pressing the ▼ button at the top right of the window.



Guidance window

Displays an explanation for the item selected in the Work window.



8.3 FPGA Module Configuration Tool Menu List

[Project] menu

Menu	Reference
[Project] ⇨ [New]	Page 92 Creating new projects
[Project] ⇨ [Open]	Page 93 Opening a project
[Project] ⇨ [Close]	—
[Project] ⇨ [Save]	Page 93 Save project
[Project] ⇨ [Save as]	Page 93 Save project as
[Project] ⇨ [Exit]	Page 87 Exit

[View] menu

Menu	Reference
[View] ⇨ [Switch Display Language]	Page 94 Display language switching

[Online] menu

Menu	Reference
[Online] ⇨ [Parameter write (Memory)]	Page 116 Parameter writing
[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]	
[Online] ⇨ [Parameter read (Memory)]	Page 116 Parameter read
[Online] ⇨ [Parameter read (Non-volatile memory)]	

[Help] menu

Menu	Reference
[Help] ⇨ [Version information]	Page 128 Checking the version of the FPGA Module Configuration Tool

8.4 Project Function

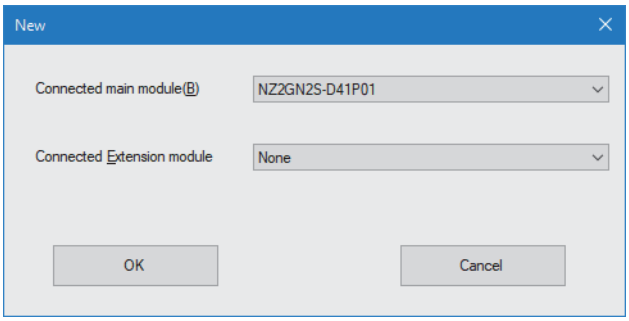
Creating new projects

A new project is created as described below.

Operating procedure

1. From "New", select "Connected main module" or "Connected Extension module".

[Project] ⇨ [New]



Item	Setting range
Connected main module	• NZ2GN2S-D41D01 • NZ2GN2S-D41P01 • NZ2GN2S-D41PD02
Connected Extension module	• None • NZ2EX2S-D41A01 • NZ2EX2S-D41D01 • NZ2EX2S-D41P01

2. Click the [OK] button.

Opening a project

The following describes how to load a project saved on the personal computer's hard disk or other storage media.

Operating procedure

1. Open the "Open" window.

[Project] ⇨ [Open]

2. Select the project to be opened and click the [Open] button.

Saving the project

How to save a project file to the hard disk of your personal computer.

Save project

Saves the currently open project.

Operating procedure

[Project] ⇨ [Save]

Save project as

Saves the project being edited under a new file name.

Operating procedure

[Project] ⇨ [Save as]

8.5 Display Function

Display language switching

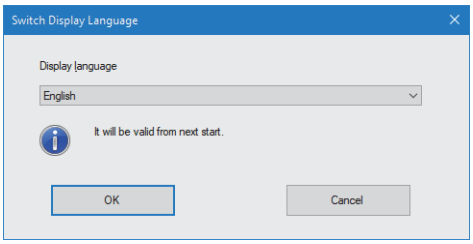
The display language of the FPGA Module Configuration Tool can be selected from the following three.

- Japanese
- English
- Chinese (Simplified)

Operating procedure

1. The display language is switched from "Switch Display Language".

[View] ⇨ [Switch Display Language]



2. Select the display language and click the [OK] button.

8.6 Parameter Setting Function

This section describes how to set the module parameters and FPGA parameters.

Module parameters

Set the module parameters.

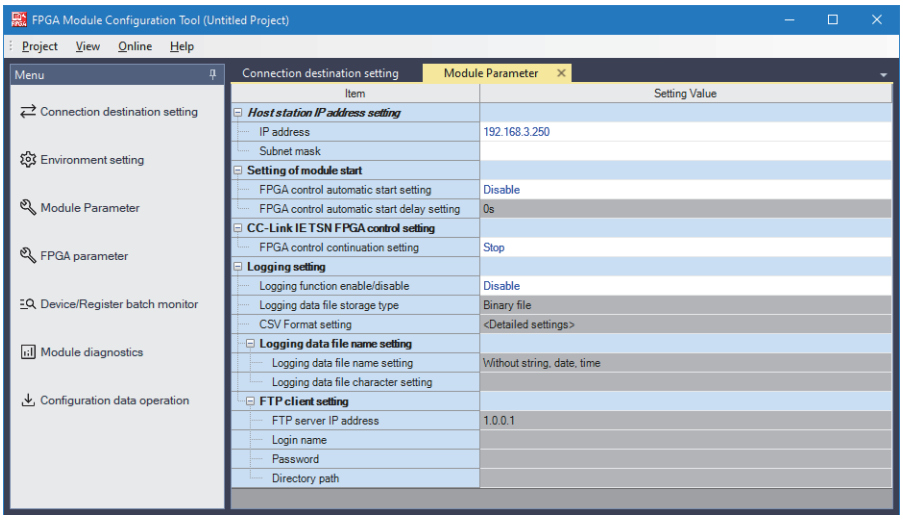
Point

By selecting the setting value on the Work window and selecting the initialization menu by right-clicking, the setting value can be initialized.

Operating procedure

1. It is done from "Module Parameter".

[Menu] ⇨ [Module Parameter]

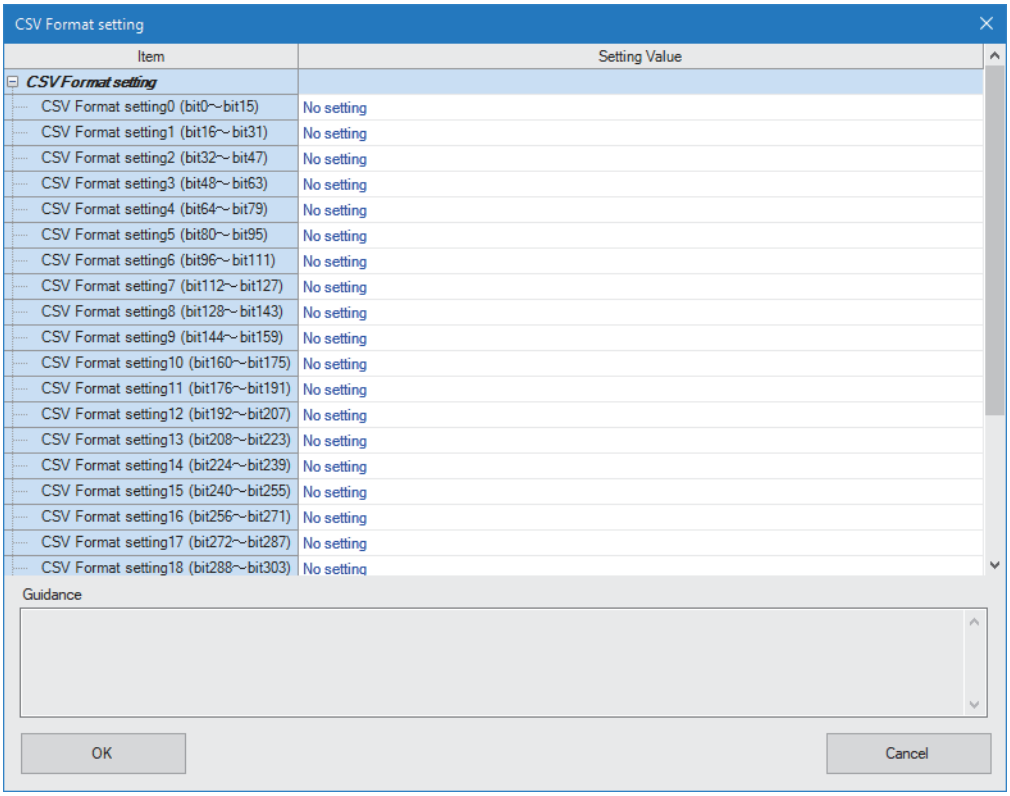


Item		Description	Setting range	Default
Host station IP address setting	IP address	Sets the IP address of your own station in standalone mode.	1.0.0.1 to 223.255.255.254 (The beginning of the IP address must start with a value between 1 and 223, excluding 127.)	192.168.3.250
	Subnet mask	Sets the subnet mask of the host station in standalone mode.	• Blank • 128.0.0.0 to 255.255.255.252	Blank
Setting of module start	FPGA control automatic start setting	Sets whether to automatically start FPGA control after configuration is complete.	• Disable • Enable	Disable
	FPGA control automatic start delay setting*1	Sets the time from configuration completion until the automatic start of FPGA control.	0 to 255	0
CC-Link IE TSN FPGA control setting	FPGA control continuation setting	Sets whether to stop or continue FPGA control when the data link with the CPU module and master station is broken during module operation in CC-Link TSN communication mode.	• Stop • Continue	Stop
Logging setting	Logging function enable/disable	Enables or disables the logging function.	• Disable • Enable	Disable
	Logging data file storage type*2	Sets the format of the saved data when transferring the collected logging data to the FTP server. When the logging data time division setting is time division mode, this setting is fixed to binary file.	• Binary file • CSV file	Binary file
	CSV Format setting*3	☞ Page 97 CSV Format setting		

Item		Description	Setting range	Default
Logging data file name setting	Logging data file name setting*2	Sets whether or not to add the date, time, and character string at the time of transfer to the file name of logging data transferred to the FTP server.	• Without string, date, time • With date • With time • With date, time • With string • With string, date • With string, time • With string, date, time	Without string, date, time
	Logging data file character setting*4	Sets the character string to be added to the file name of the logging data transferred to the FTP server.	The maximum number that can be set for this setting changes depending on the logging data file name setting. • With string: 1 to 51 characters • With string, date: 1 to 42 characters • With string, time: 1 to 44 characters • With string, date, time: 1 to 35 characters One-byte alphanumeric characters and single-byte symbols can be set. However, \ / : * ? < > | " cannot be used.	Blank
FTP client setting	FTP server IP address*2	Sets the IP address of the FTP server to be used for communication.	1.0.0.1 to 223.255.255.254 (The beginning of the IP address must start with a value between 1 and 223, excluding 127.)	1.0.0.1
	Login name*2	Sets the login name to be used when transferring files (logging in) to the FTP server.	1 to 32 characters (one-byte alphanumeric characters and one-byte symbols)	Blank
	Password*2	Sets the password for transferring files (login) to the FTP server.	0 to 32 characters (one-byte alphanumeric characters and one-byte symbols)	Blank
	Directory path*2	Sets the directory path for transferring files to the FTP server.	0 to 64 characters (one-byte alphanumeric characters and one-byte symbols) However, * ? < > | " cannot be used.	Blank

*1 This can be set when "FPGA control automatic start setting" is set to "Enable". When set to "Disable", it is masked and cannot be set.
*2 This can be set when "Logging function enable/disable" is set to "Enable". When set to "Disable", it is masked and cannot be set.
*3 This can be set when "Logging data file storage type" is set to "CSV file". When set to "Binary file", it is masked and cannot be set.
*4 It can be set when "Logging data file name setting" is set to "With string", "With string, date", "With string, time", or "With string, date, time". With other settings it is masked and cannot be set.

■CSV Format setting



Item		Description	Setting range	Default
CSV Format setting	CSV Format setting 0 (bit0~bit15) to CSV Format setting 26 (bit416~bit431)	Sets the format to use when saving logging data in CSV file format.	• No setting • Bit, binary format • Word [Signed], decimal format • Word [Unsigned], decimal format • Word [Unsigned], hexadecimal format • Double Word [Signed], decimal format • Double Word [Unsigned], decimal format • Double Word [Unsigned], hexadecimal format	No setting

FPGA parameters

Set the FPGA parameters.

Point

- The items that can be set differ depending on the module selected.
- The E0 terminal block, E1 terminal block, and E2 terminal block can be set when an Extension module is connected. Masked if no Extension module is connected.
- By selecting the setting value on the Work window and selecting the initialization menu by right-clicking, the setting value can be initialized.

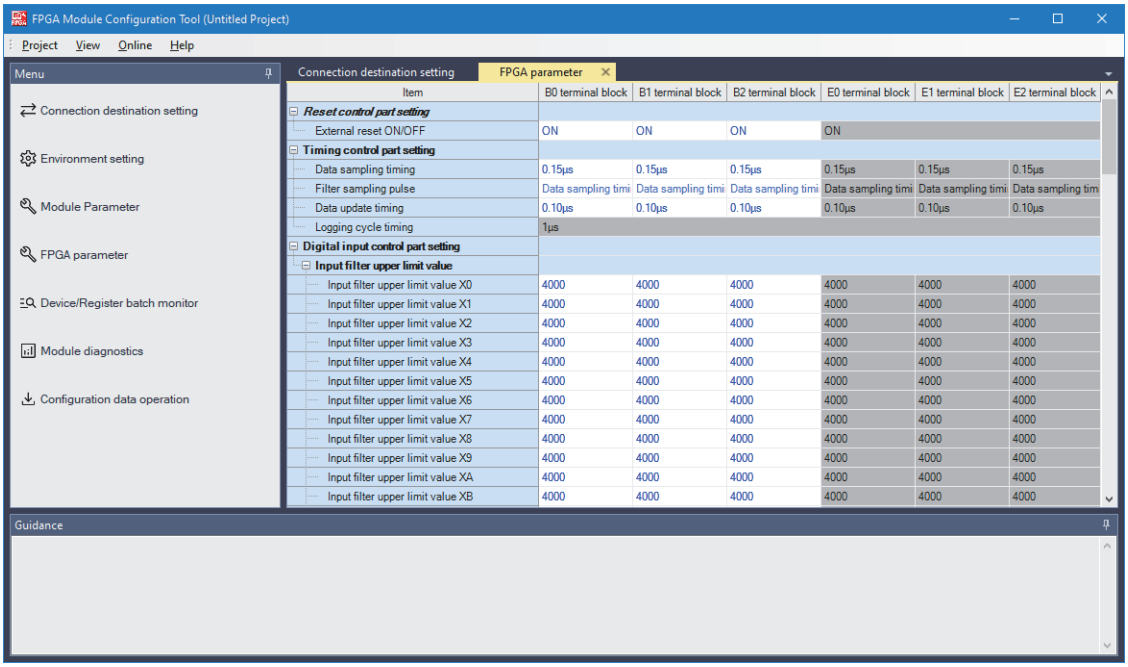
Operating procedure

1. Do it from "FPGA parameter".

[Menu] ⇨ [FPGA parameter]

Ex.

For NZ2GN2S-D41P01



■NZ2GN2S-D41P01

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing	Sets the timing (cycle) for sampling the DC input.	0.10 to 655.36μs (set in units of 0.01μs)	0.15μs
	Filter sampling pulse	Sets the operation cycle of the digital filter. For the DC I/O board, this setting is fixed to the data sampling timing.	Data sampling timing (fixed)	Data sampling timing
	Data update timing	Sets the output timing (cycle) of the DC output.	0.10 to 655.36μs (set in units of 0.01μs)	0.10μs
	Logging cycle timing*1	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value XF	Sets the DC input filter upper limit value.	0 to 4095	4000
Digital output control part setting	Output signal selection Y0 to Output signal selection YF	Sets the signal to output to the DC output.	• Register setting value (RY) • User circuit output	Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7	It is masked and cannot be set.		CLEAR (fixed to H)
Digital I/O control part setting	Select output signal or I/O direction signal	It is masked and cannot be set.		Register setting value (RY or I/O direction)
	I/O direction setting	It is masked and cannot be set.		Input
	Input filter upper limit value	It is masked and cannot be set.		4000
	Differential output HOLD/CLEAR	It is masked and cannot be set.		CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	Cannot be set.		
	ADC range setting CH0 to ADC range setting CHB	Cannot be set.		
	ADC offset value CH0 to ADC offset value CHB	Cannot be set.		
	Select A/D conversion timing	Cannot be set.		
	ADC oversampling ratio setting	Cannot be set.		
Analog output control part setting	D/A conversion enable/disable setting CH0, D/A conversion enable/disable setting CH1	Cannot be set.		
	DAC range setting CH0, DAC range setting CH1	Cannot be set.		
	DAC offset value CH0, DAC offset value CH1	Cannot be set.		
	Select D/A conversion value	Cannot be set.		
	Select D/A conversion timing	Cannot be set.		
	Select DAC LDAC signal	Cannot be set.		

Item		Description	Setting range	Default
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*2	When "Logging operation mode setting" is set to "Trigger operation mode", this sets the number of logging times after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/ disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.

*2 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

■NZ2GN2S-D41D01

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing	Sets the timing (cycle) for sampling the differential (RS-422/RS-485) input.	0.01μs	0.01μs
	Filter sampling pulse	Sets the operation cycle of the digital filter. The data sampling timing cannot be set for the differential I/O board. The same value as this setting is set for the data sampling timing.	• 0.01μs • 0.02μs • 0.04μs • 0.08μs • 0.10μs • 0.14μs • 0.16μs • 0.20μs • 0.32μs • 0.40μs • 0.50μs • 1.00μs • 2.00μs • 10.00μs • 100.00μs	0.01μs
	Data update timing	Sets the output timing (cycle) for differential (RS-422/RS-485) output.	0.01μs to 655.36μs (set in units of 0.01μs)	0.01μs
	Logging cycle timing*1	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value X7*2	Sets the filter upper limit value of the differential (RS-422) input digital filter.	0 to 4095	1500
Digital output control part setting	Output signal selection Y0 to Output signal selection Y7*3	Sets the signal output to the differential (RS-422) output.	• Register setting value (RY) • User circuit output	Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7*4	Sets the differential (RS-422) output value when FPGA control is stopped for a differential I/O board.	• CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)
Digital I/O control part setting	Select output signal or I/O direction signal	Select the input/output direction signal.	• Register setting value (RY or I/O direction) • User circuit output	Register setting value (RY or I/O direction)
	I/O direction setting*6	When "Select output signal or I/O direction signal" is set to "Register setting value (RY or I/O direction)". Sets the input and output direction of differential (RS-485) input/output.	• Input • Output	Input
	Input filter upper limit value	Sets the filter upper limit value of the differential (RS-485) input digital filter.	0 to 4095	1500
	Differential output HOLD/CLEAR*5	Sets the differential (RS-485) output value when FPGA control stops.	• CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	Cannot be set.		
	ADC range setting CH0 to ADC range setting CHB	Cannot be set.		
	ADC offset value CH0 to ADC offset value CHB	Cannot be set.		
	Select A/D conversion timing	Cannot be set.		
	ADC oversampling ratio setting	Cannot be set.		

Item		Description	Setting range	Default
Analog output control part setting	D/A conversion enable/disable setting CH0, D/A conversion enable/disable setting CH1	Cannot be set.		
	DAC range setting CH0, DAC range setting CH1	Cannot be set.		
	DAC offset value CH0, DAC offset value CH1	Cannot be set.		
	Select D/A conversion value	Cannot be set.		
	Select D/A conversion timing	Cannot be set.		
	Select DAC LDAC signal	Cannot be set.		
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*7	Sets the number of times logging occurs after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.
*2 The input filter upper limit values X8 to XF are masked and cannot be set.
*3 Output signal selection Y8 to YF are masked and cannot be set.
*4 This can be set when "External reset ON/OFF" is set to "OFF". "ON" is masked and cannot be set.
*5 This can be set when "External reset ON/OFF" is set to "OFF" and "Select output signal or I/O direction signal" is set to "User circuit output". Otherwise it is masked and cannot be set.
*6 When "Select output signal or I/O direction signal" is set to "User circuit output", it is masked and cannot be set.
*7 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

■NZ2GN2S-D41PD02

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing	Sets the sampling timing (cycle) for DC input and differential (RS-422/RS-485) input.	■B0 terminal block, B1 terminal block 0.10μs to 655.36μs (set in units of 0.01μs) ■B2 terminal block 0.01μs to 655.36μs (set in units of 0.01μs)	■B0 terminal block, B1 terminal block 0.15μs ■B2 terminal block 0.01μs
	Filter sampling pulse	Sets the operation cycle of the digital filter. For the DC I/O board, this setting is fixed to the data sampling timing. The data sampling timing cannot be set for the differential I/O board. The same value as this setting is set for the data sampling timing.	■B0 terminal block, B1 terminal block Data sampling timing (fixed) ■B2 terminal block • 0.01μs • 0.02μs • 0.04μs • 0.08μs • 0.10μs • 0.14μs • 0.16μs • 0.20μs • 0.32μs • 0.40μs • 0.50μs • 1.00μs • 2.00μs • 10.00μs • 100.00μs	■B0 terminal block, B1 terminal block Data sampling timing ■B2 terminal block 0.01μs
	Data update timing	Sets the output timing (cycle) for DC output and differential (RS-422/RS-485) output.	■B0 terminal block, B1 terminal block 0.10μs to 655.36μs (set in units of 0.01μs) ■B2 terminal block 0.01μs to 655.36μs (set in units of 0.01μs)	■B0 terminal block, B1 terminal block 0.10μs ■B2 terminal block 0.01μs
	Logging cycle timing[*1]	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value XF[*2]	Sets the filter upper limit value of the digital filter for DC input and differential (RS-422) input.	0 to 4095	■B0 terminal block, B1 terminal block 4000 ■B2 terminal block 1500
Digital output control part setting	Output signal selection Y0 to Output signal selection YF[*3]	Sets the signal to be output to the DC output and differential (RS-422) output.	• Register setting value (RY) • User circuit output	Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7[*4]	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block Sets the differential (RS-422) output value when FPGA control is stopped for a differential I/O board.	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block • CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)

Item		Description	Setting range	Default
Digital I/O control part setting	Select output signal or I/O direction signal	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block Select the input/output direction signal.	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block • Register setting value (RY or I/O direction) • User circuit output	Register setting value (RY or I/O direction)
	I/O direction setting*6	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block When "Select output signal or I/O direction signal" is set to "Register setting value (RY or I/O direction)", this item sets the input and output direction of differential (RS-485) input/output.	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block • Input • Output	Input
	Input filter upper limit value	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block Sets the filter upper limit value of the differential (RS-485) input digital filter.	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block 0 to 4095	■B0 terminal block, B1 terminal block 4000 ■B2 terminal block 1500
	Differential output HOLD/CLEAR*5	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block Sets the differential (RS-485) output value when FPGA control stops.	■B0 terminal block, B1 terminal block It is masked and cannot be set. ■B2 terminal block • CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	Cannot be set.		
	ADC range setting CH0 to ADC range setting CHB	Cannot be set.		
	ADC offset value CH0 to ADC offset value CHB	Cannot be set.		
	Select A/D conversion timing	Cannot be set.		
	ADC oversampling ratio setting	Cannot be set.		
Analog output control part setting	D/A conversion enable/disable setting CH0, D/A conversion enable/disable setting CH1	Cannot be set.		
	DAC range setting CH0, DAC range setting CH1	Cannot be set.		
	DAC offset value CH0, DAC offset value CH1	Cannot be set.		
	Select D/A conversion value	Cannot be set.		
	Select D/A conversion timing	Cannot be set.		
	Select DAC LDAC signal	Cannot be set.		

Item		Description	Setting range	Default
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*7	When "Logging operation mode setting" is set to "Trigger operation mode", this sets the number of logging times after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.
*2 The input filter upper limit values X8 to XF of the B2 terminal block are masked and cannot be set.
*3 Output signal selections Y8 to YF on the B2 terminal block are masked and cannot be set.
*4 Only with the B2 terminal block, they can be set when "External reset ON/OFF" is set to "OFF". "ON" is masked and cannot be set.
*5 Can be set when "External reset ON/OFF" on the B2 terminal block is "OFF" and "Select output signal or I/O direction signal" is "User circuit output". Otherwise it is masked and cannot be set.
*6 When "Select output signal or I/O direction signal" is set to "User circuit output", it is masked and cannot be set.
*7 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

■NZ2EX2S-D41P01

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing	Sets the timing (cycle) for sampling the DC input.	0.10 to 655.36μs (set in units of 0.01μs)	0.15μs
	Filter sampling pulse	Sets the operation cycle of the digital filter. For the DC I/O board, this setting is fixed to the data sampling timing.	Data sampling timing (fixed)	Data sampling timing
	Data update timing	Sets the output timing (cycle) of the DC output.	0.10 to 655.36μs (set in units of 0.01μs)	0.10μs
	Logging cycle timing*1	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value XF	Sets the filter upper limit value of the DC input digital filter.	0 to 4095	4000
Digital output control part setting	Output signal selection Y0 to Output signal selection YF	Sets the signal to output to the DC output.	• Register setting value (RY) • User circuit output	Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7	It is masked and cannot be set.		CLEAR (fixed to H)
Digital I/O control part setting	Select output signal or I/O direction signal	It is masked and cannot be set.		Register setting value (RY or I/O direction)
	I/O direction setting	It is masked and cannot be set.		Input
	Input filter upper limit value	It is masked and cannot be set.		4000
	Differential output HOLD/CLEAR	It is masked and cannot be set.		CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	It is masked and cannot be set.		Conversion-disable
	ADC range setting CH0 to ADC range setting CHB	It is masked and cannot be set.		-9.9V to 9.9V
	ADC offset value CH0 to ADC offset value CHB	It is masked and cannot be set.		0
	Select A/D conversion timing	It is masked and cannot be set.		Data sampling timing
	ADC oversampling ratio setting	It is masked and cannot be set.		No setting
Analog output control part setting	D/A conversion enable/disable setting CH0, D/A conversion enable/disable setting CH1	It is masked and cannot be set.		Conversion-disable
	DAC range setting CH0, DAC range setting CH1	It is masked and cannot be set.		-9.9V to 9.9V
	DAC offset value CH0, DAC offset value CH1	It is masked and cannot be set.		0
	Select D/A conversion value	It is masked and cannot be set.		Register setting value
	Select D/A conversion timing	It is masked and cannot be set.		Data update timing
	Select DAC LDAC signal	It is masked and cannot be set.		Fixed to Low

Item		Description	Setting range	Default
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*2	Sets the number of times logging occurs after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.

*2 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

■NZ2EX2S-D41D01

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing	Sets the timing (cycle) for sampling differential (RS-422/RS-485) input and analog input.	0.01 to 0.01μs	0.01μs
	Filter sampling pulse	Sets the operation cycle of the digital filter. The data sampling timing cannot be set for the differential I/O board. The same value as this setting is set for the data sampling timing.	• 0.01μs • 0.02μs • 0.04μs • 0.08μs • 0.10μs • 0.14μs • 0.16μs • 0.20μs • 0.32μs • 0.40μs • 0.50μs • 1.00μs • 2.00μs • 10.00μs • 100.00μs	0.01μs
	Data update timing	Sets the output timing (cycle) for differential (RS-422/RS-485) output.	0.01μs to 655.36μs (set in units of 0.01μs)	0.01μs
	Logging cycle timing[*1]	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value X7[*2]	Sets the filter upper limit value of the differential (RS-422) input digital filter.	0 to 4095	1500
Digital output control part setting	Output signal selection Y0 to Output signal selection Y7[*3]	Sets the signal output to the differential (RS-422) output.	• Register setting value (RY) • User circuit output	Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7[*4]	Sets the differential (RS-422) output value when FPGA control is stopped for a differential I/O board.	• CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)
Digital I/O control part setting	Select output signal or I/O direction signal	Select the input/output direction signal.	• Register setting value (RY or I/O direction) • User circuit output	Register setting value (RY or I/O direction)
	I/O direction setting[*5]	When "Select output signal or I/O direction signal" is set to "Register setting value (RY or I/O direction)", this item sets the input and output direction of differential (RS-485) input/output.	• Input • Output	Input
	Input filter upper limit value	Sets the filter upper limit value of the differential (RS-485) input digital filter.	0 to 4095	1500
	Differential output HOLD/CLEAR[*6]	When "External reset ON/OFF" is set to "OFF" and "Select output signal or I/O direction signal" is set to "User circuit output", this sets the differential (RS-485) output value when FPGA control is stopped.	• CLEAR (fixed to L) • CLEAR (fixed to H) • HOLD	CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	It is masked and cannot be set.		Conversion-disable
	ADC range setting CH0 to ADC range setting CHB	It is masked and cannot be set.		-9.9V to 9.9V
	ADC offset value CH0 to ADC offset value CHB	It is masked and cannot be set.		0
	Select A/D conversion timing	It is masked and cannot be set.		Data sampling timing
	ADC oversampling ratio setting	It is masked and cannot be set.		No setting

Item		Description	Setting range	Default
Analog output control part setting	D/A conversion enable/ disable setting CH0, D/A conversion enable/ disable setting CH1	It is masked and cannot be set.		Conversion-disable
	DAC range setting CH0, DAC range setting CH1	It is masked and cannot be set.		-9.9V to 9.9V
	DAC offset value CH0, DAC offset value CH1	It is masked and cannot be set.		0
	Select D/A conversion value	It is masked and cannot be set.		Register setting value
	Select D/A conversion timing	It is masked and cannot be set.		Data update timing
	Select DAC LDAC signal	It is masked and cannot be set.		Fixed to Low
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*7	Sets the number of times logging occurs after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.
*2 The input filter upper limit values X8 to XF are masked and cannot be set.
*3 Output signal selection Y8 to YF are masked and cannot be set.
*4 This can be set when "External reset ON/OFF" is set to "OFF". "ON" is masked and cannot be set.
*5 When "Select output signal or I/O direction signal" is set to "User circuit output", it is masked and cannot be set.
*6 This can be set when "External reset ON/OFF" is set to "OFF" and "Select output signal or I/O direction signal" is set to "User circuit output". Otherwise it is masked and cannot be set.
*7 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

■NZ2EX2S-D41A01

Item		Description	Setting range	Default
Reset control part setting	External reset ON/OFF	Sets ON/OFF of the reset issued to the board when FPGA control is stopped.	• ON • OFF	ON
Timing control part setting	Data sampling timing[*5]	Sets the sampling timing (cycle) for DC input, differential (RS-422/RS-485) input, and analog input.	4.00μs to 655.36μs (set in units of 0.01μs)	4.00μs
	Filter sampling pulse	It is masked and cannot be set.		Data sampling timing
	Data update timing[*6]	Sets the output timing (cycle) for DC output, differential (RS-422/RS-485) output, and analog output.	6.00μs to 655.36μs (set in units of 0.01μs)	6.00μs
	Logging cycle timing[*1]	Sets the logging cycle.	1μs to 32768μs (set in units of 1μs)	1μs
Digital input control part setting	Input filter upper limit value X0 to Input filter upper limit value XF	It is masked and cannot be set.		4000
Digital output control part setting	Output signal selection Y0 to Output signal selection YF	It is masked and cannot be set.		Register setting value (RY)
	Differential output HOLD/CLEAR Y0 to Differential output HOLD/CLEAR Y7	It is masked and cannot be set.		CLEAR (fixed to H)
Digital I/O control part setting	Select output signal or I/O direction signal	It is masked and cannot be set.		Register setting value (RY or I/O direction)
	I/O direction setting	It is masked and cannot be set.		Input
	Input filter upper limit value	It is masked and cannot be set.		4000
	Differential output HOLD/CLEAR	It is masked and cannot be set.		CLEAR (fixed to H)
Analog input control part setting	A/D conversion enable/disable setting	Enables or disables A/D conversion.	• Conversion-disable • Conversion-enable	Conversion-disable
	ADC range setting CH0 to ADC range setting CHB[*2]	Sets the ADC range.	• -19.8mA to 19.8mA • -9.9V to 9.9V	-9.9V to 9.9V
	ADC offset value CH0 to ADC offset value CHB[*2]	Sets the ADC offset value.	-128 to 127	0
	Select A/D conversion timing[*2]	Select the ADC A/D conversion timing.	• Data sampling timing • User circuit output	Data sampling timing
	ADC oversampling ratio setting[*2]	Sets the ADC oversampling ratio.	• No setting • Double • 4x • 8x • 16x • 32x • 64x • 128x • 256x	No setting
Analog output control part setting	D/A conversion enable/disable setting CH0, D/A conversion enable/disable setting CH1	Enables or disables D/A conversion.	• Conversion-disable • Conversion-enable	Conversion-disable
	DAC range setting CH0, DAC range setting CH1[*3]	Sets the DAC range.	• -9.9V to 9.9V • 0.2mA to 19.8mA	-9.9V to 9.9V
	DAC offset value CH0, DAC offset value CH1[*3]	Sets the DAC offset value.	-32768 to 32767	0
	Select D/A conversion value[*3]	Select the D/A conversion value to output to DAC.	• Register setting value • User circuit output	Register setting value
	Select D/A conversion timing[*3]	Select the DAC D/A conversion timing.	• Data update timing • User circuit output	Data update timing
	Select DAC LDAC signal[*3]	Select the LDAC signal to output to the DAC.	• Fixed to Low • User circuit output	Fixed to Low

Item		Description	Setting range	Default
Logging part setting	Logging operation mode setting*1	Select the logging operation mode.	• Storage operation mode • Trigger operation mode	Storage operation mode
	Buffer operation setting*1	Select linear buffer operation or ring buffer operation.	• Linear buffer operation • Ring buffer operation	Linear buffer operation
	Select logging start control*1	Select the logging start signal.	• User circuit output • Register setting value (RY3)	User circuit output
	Select sampling pulses*1	Select the logging cycle.	• Logging cycle timing • User circuit output	Logging cycle timing
	Logging data size setting*1	Logging data size setting	• 256 records • 512 records • 1024 records • 2048 records • 4096 records • 8192 records • 16384 records • 32768 records • 65536 records • 131072 records • 262144 records • 524288 records	4096 records
	Set number of sampling after trigger*4	When "Logging operation mode setting" is set to "Trigger operation mode", this sets the number of logging times after trigger input.	1 to (number of records in logging data size setting -1)	1
User circuit part setting	Logging data time division setting*1	Sets Non-Time division mode and Time division mode.	• Non-Time division mode • Time division mode	Non-Time division mode
	USER switch function enable/disable	Enables or disables function setting switches 7 to 10.	• Disable • Enable	Disable
	User circuit part parameter setting	☞ Page 112 User circuit part parameter setting		

*1 This can be set when "Logging function enable/disable" in "Logging setting" of "Module Parameter" is set to "Enable". When set to "Disable", it is masked and cannot be set.

*2 Can be set when "A/D conversion enable/disable setting" is set to "Conversion-enable". With "Conversion-disable" it is masked and cannot be set.

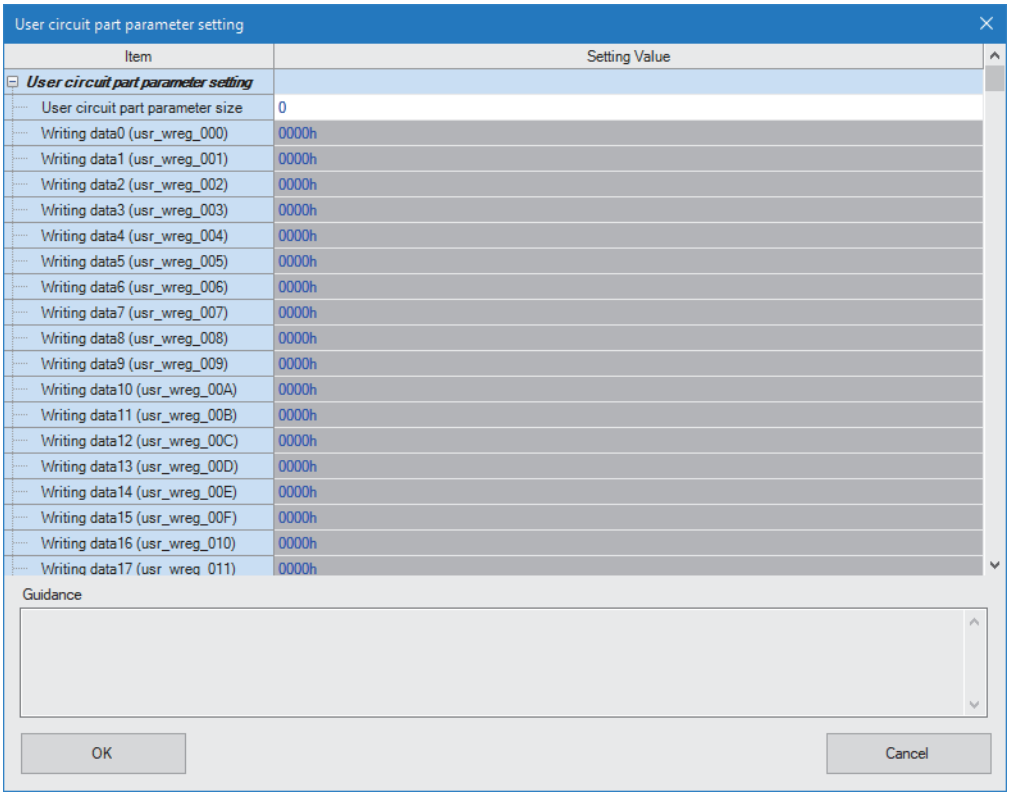
*3 This can be set when "D/A conversion enable/disable setting" is set to "Conversion-enable". With "Conversion-disable" it is masked and cannot be set.

*4 Can be set when "Logging operation mode setting" is set to "Trigger operation mode". When set to "Storage operation mode", it is masked and cannot be set.

*5 This can be set when "A/D conversion enable/disable setting" is set to "Conversion-enable" and "Select A/D conversion timing" is set to "Data sampling timing". Otherwise it is masked and cannot be set.

*6 Can be set when "D/A conversion enable/disable setting" is set to "Conversion-enable" and "Select D/A conversion timing" is set to "Data update timing". Otherwise it is masked and cannot be set.

■User circuit part parameter setting



Item	Description	Setting value
User circuit part parameter size	From the start address of the FPGA register writing data (transient area) in the user circuit part, set the size of FPGA parameters to be saved in non-volatile memory, in word units.	0 to 384 (Default: 0)
Writing data0 (usr_wreg_000) to Writing data383 (usr_wreg_17F)*1	Set when changing the initial value of the User circuit part writing data (transient area) (usr_wreg_000 to 17F) from 0000h.	0000h to FFFFh (Default: 0000h)

*1 Masking is canceled by the input value of "User circuit part parameter size".

8.7 Online Functions

The online functions are described in the following.

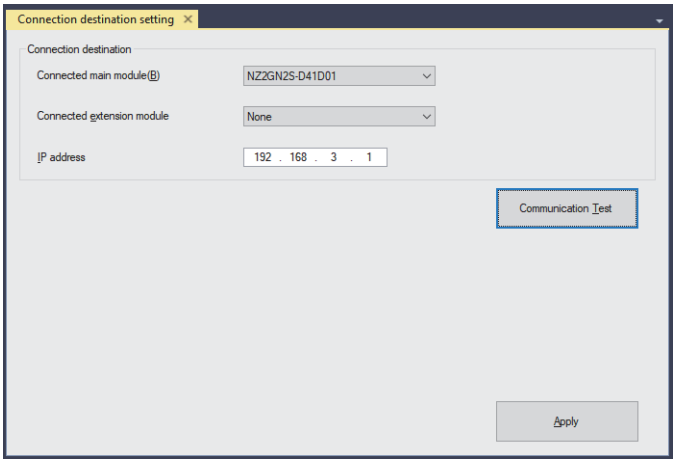
Connection destination setting

Settings for a newly created Main module, changes for an Extension module, and IP address settings are made as follows.

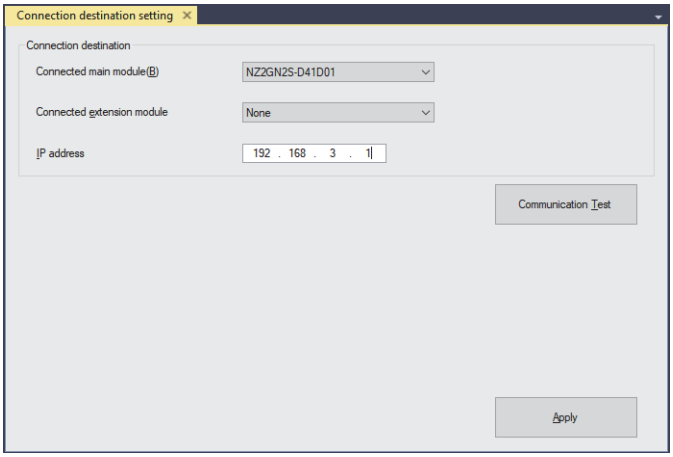
Operating procedure

1. The contents set in "New" are displayed.

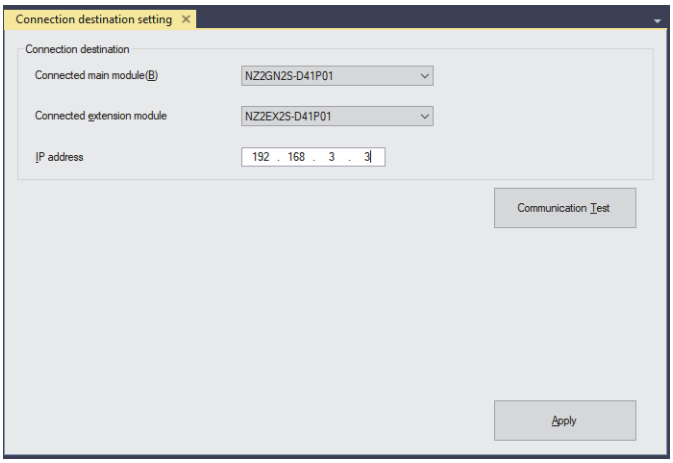
[Menu] ⇨ [Connection destination setting]



2. Redo the settings for items to be changed on the main module and extension module.



3. Set the IP address of the connected FPGA module.



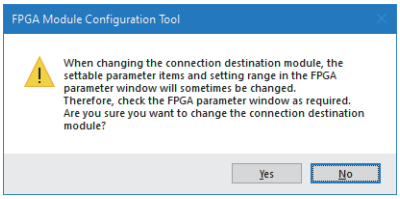
Item	Setting range
IP address	1.0.0.1 to 223.255.255.254

Point

The IP address must start with a value between 1 and 223, excluding 127.

4. Click the [Apply] button.

5. If there is no problem with the changes, click the [Yes] button.



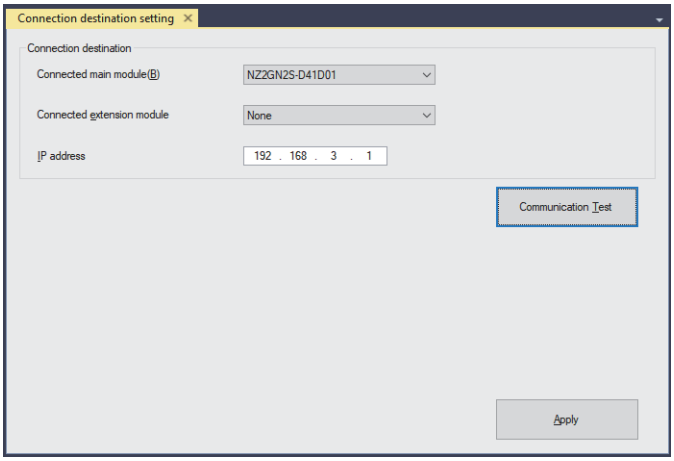
Communication test

Allows for checking whether communication using the set IP address is possible.

Operating procedure

1. Display the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]



2. Click the [Communication Test] button.

3. Click the [OK] button.

Point

The setting is not reflected if only a communication test is performed. Click the [Apply] button to have the settings be reflected.

Parameter writing

This section describes how to write Module parameters and FPGA parameters to the FPGA module.
There are two types of write destinations for parameters: memory and non-volatile memory. Writing can be performed only to memory or to both memory and non-volatile memory. Parameters written to nonvolatile memory are read back into memory when the power is turned on, so control can be started without redoing settings. However, since 10000 is the limit on the number of writes that can be made to the non-volatile memory, it is recommended that different write destinations be used as follows.

Write destination	Setting values after the FPGA module is powered off	Application
Memory	Not saved.	When adjusting the setting value
Memory + Non-volatile memory	Saved in non-volatile memory.	When wishing to use the set values the next time the FPGA module power is turned on

Point

The IP address and subnet mask are saved in non-volatile memory regardless of whether the parameter write destination is memory or memory + non-volatile memory.

Operating procedure

1. Select the write method according to the write destination.

[Online] ⇨ [Parameter write (Memory)] or [Parameter write (Memory + Non-volatile memory)]

Parameter read

Reads Module parameters and FPGA parameters from the FPGA module.

Read destination	Description
Memory	Read Module parameters and FPGA parameters from memory.
Memory + Non-volatile memory	Read Module parameters and FPGA parameters from non-volatile memory.

Operating procedure

1. Select the reading method.

[Online] ⇨ [Parameter read (Memory)] or [Parameter read (Memory + Non-volatile memory)]

Batch monitor display

Displays the contents of link devices, remote buffers, or FPGA register areas.
By manipulating cells on the grid, values can be changed and written.

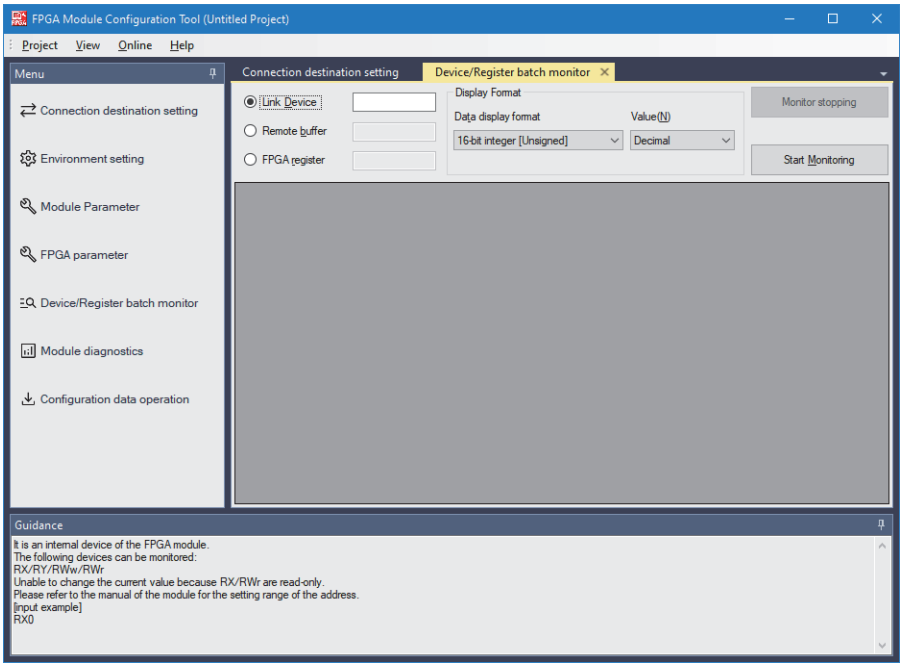
Point

Link devices (RX/RY) can only be monitored in units of 16 points, and FPGA register areas can only be monitored in units of even numbers.

Operating procedure

1. Displays the "Device/Register batch monitor" window.

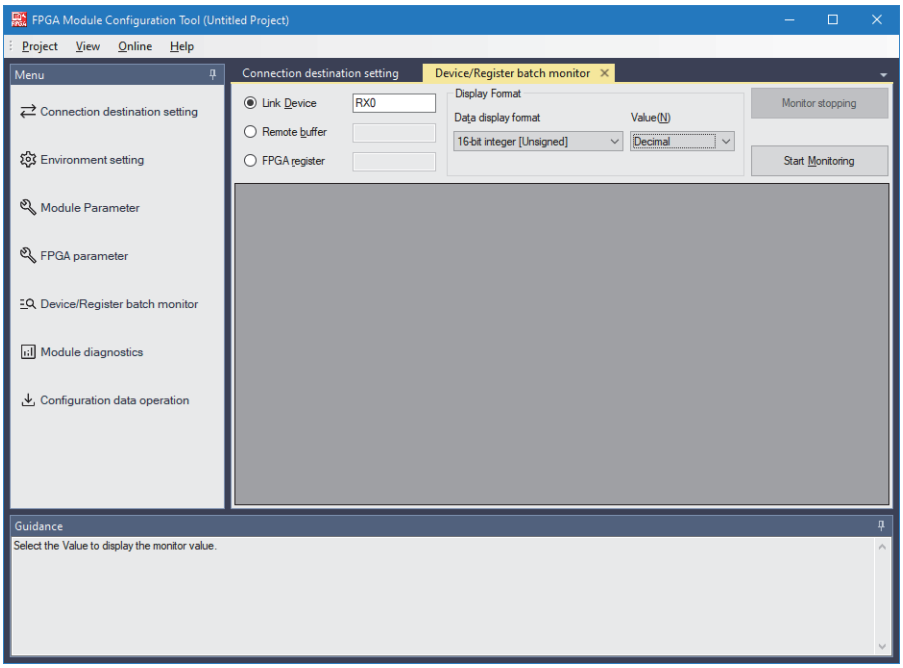
[Menu] ⇨ [Device/Register batch monitor]



2. Select either Link device, Remote buffer, or FPGA register as the type to display.

3. Enter the address to display.

4. Select Data display format and Value under Display Format.



Data display format	Value	Display content
16-bit integer [Unsigned]	Decimal	Displays the current value in the range of 0 to 65535.
	Hexadecimal	Displays the current value in four hexadecimal digits.
32-bit integer [Unsigned]	Decimal	Displays the current value in the range of 0 to 4294967295. The current value is displayed with the displayed top address as the base point, and when scrolled, the current value is recalculated and displayed with the displayed top address as the base point.
	Hexadecimal	Displays the current value in 8 hexadecimal digits. The current value is displayed with the displayed top address as the base point, and when scrolled, the current value is recalculated and displayed with the displayed top address as the base point.
16-bit integer [Signed]	Decimal	Displays the current value in the range of -32768 to 32767.
	Hexadecimal	Displays the current value in four hexadecimal digits.
32-bit integer [Signed]	Decimal	Displays the current value in the range of -2147483648 to 2147483647. The current value is displayed with the displayed top address as the base point, and when scrolled, the current value is recalculated and displayed with the displayed top address as the base point.
	Hexadecimal	Displays the current value in 8 hexadecimal digits. The current value is displayed with the displayed top address as the base point, and when scrolled, the current value is recalculated and displayed with the displayed top address as the base point.

5. Click the [Start Monitoring] button.

Changing current values

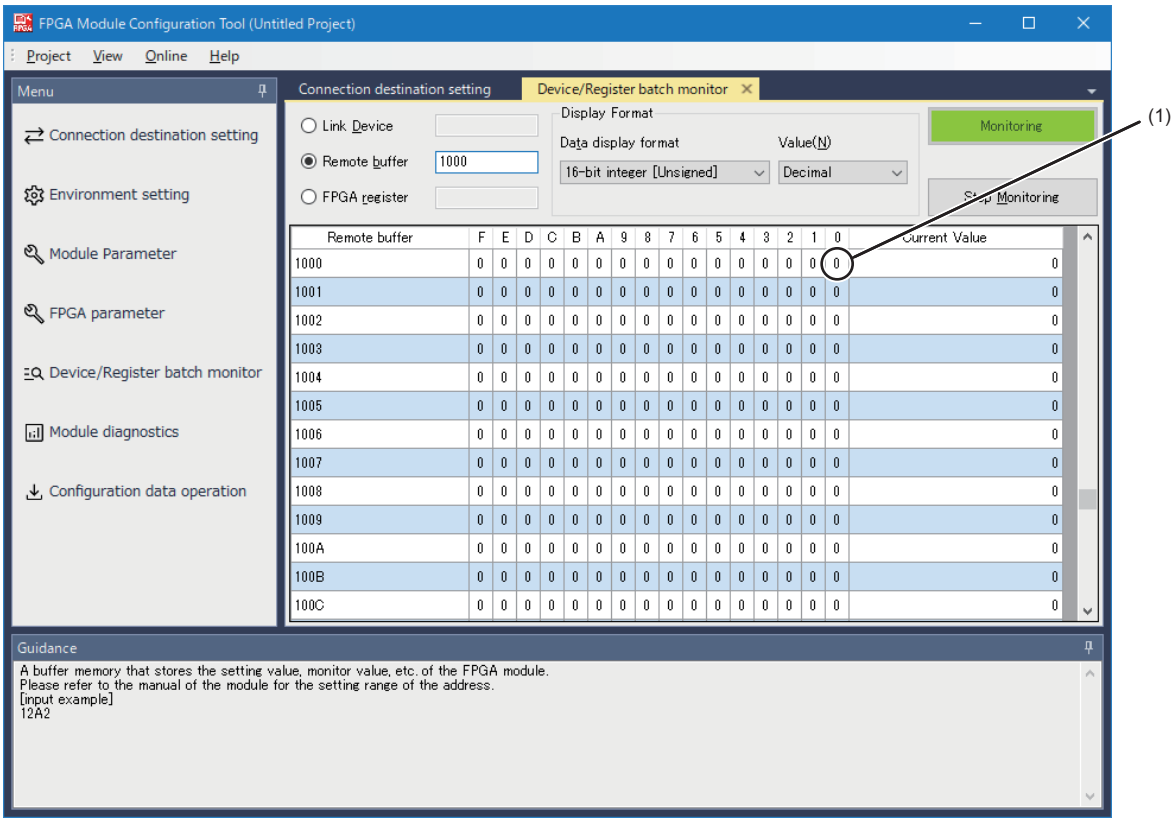
The current values of link devices (RY/RWw), remote buffers, and FPGA register areas can be changed as follows.

Restriction

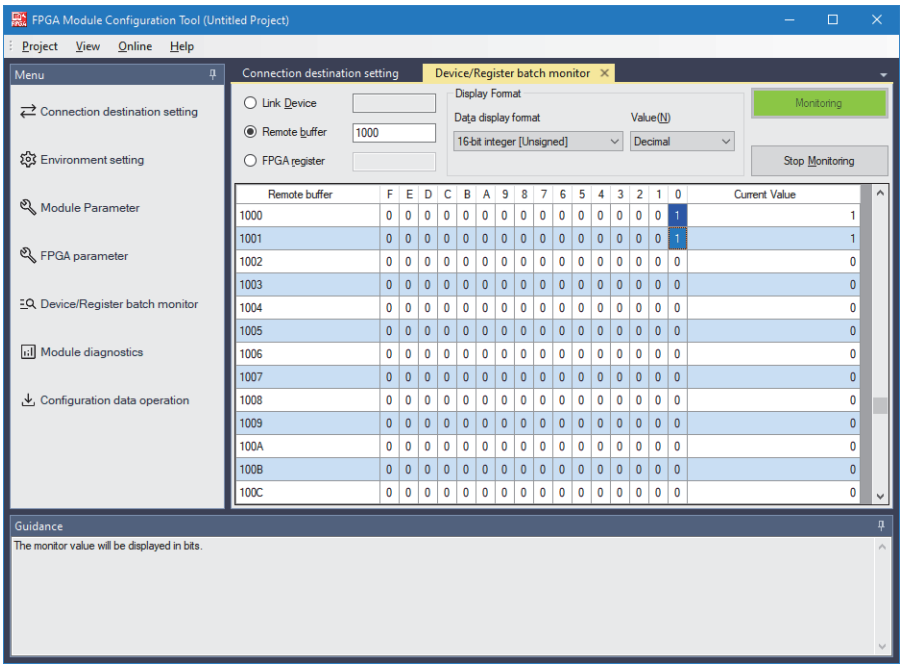
- The current value of Link devices (RX/RWr) cannot be changed.
- In CC-Link IE TSN communication mode, the current value of link devices (RY/RWw) cannot be changed.

Operating procedure

1. Double-click a cell in grid (1) or press the Enter key.



2. The bit value will be highlighted, allowing the current value to be changed.



Point

The current value can also be changed by right-clicking a grid cell and selecting the change current value menu.

Automatic monitor stop

- When creating a project with "New"
- When the project is opened with "Open"
- When "Parameter read (Memory)" is executed
- When executing "Parameter write (Memory)" or "Parameter write (Memory + Non-volatile memory)"
- When the setting contents are changed in "Connection destination setting"
- When the setting contents are changed in "Environment setting"
- If any other menu is selected (The monitor is paused. However, when returned to the monitor window, the monitor will automatically resume.)
- If a communication error, SLMP timeout, or data read error occurs during monitoring

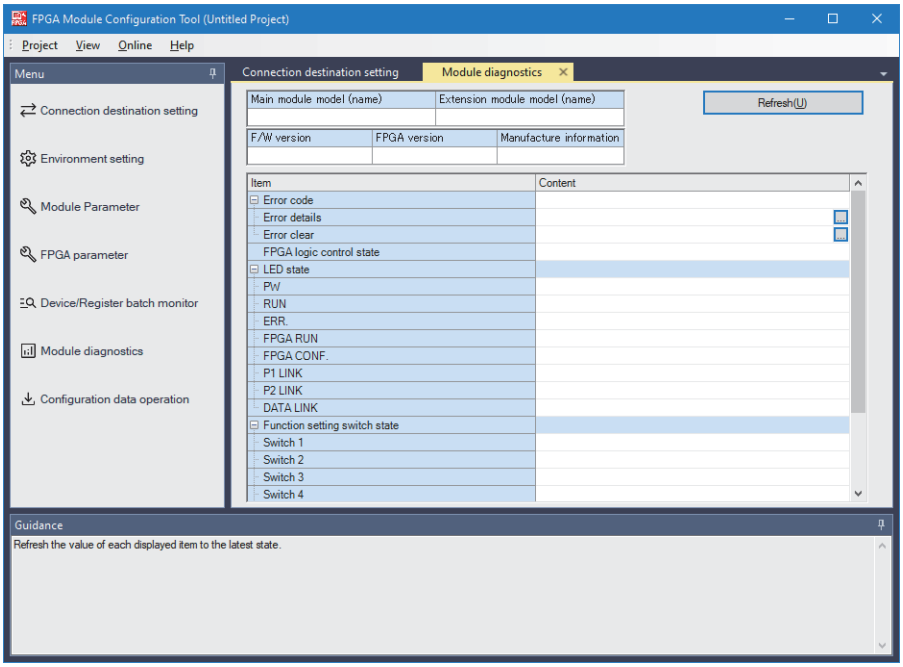
Module diagnostics

Displays basic information, the status of LEDs, and the status of errors of the FPGA module collectively.

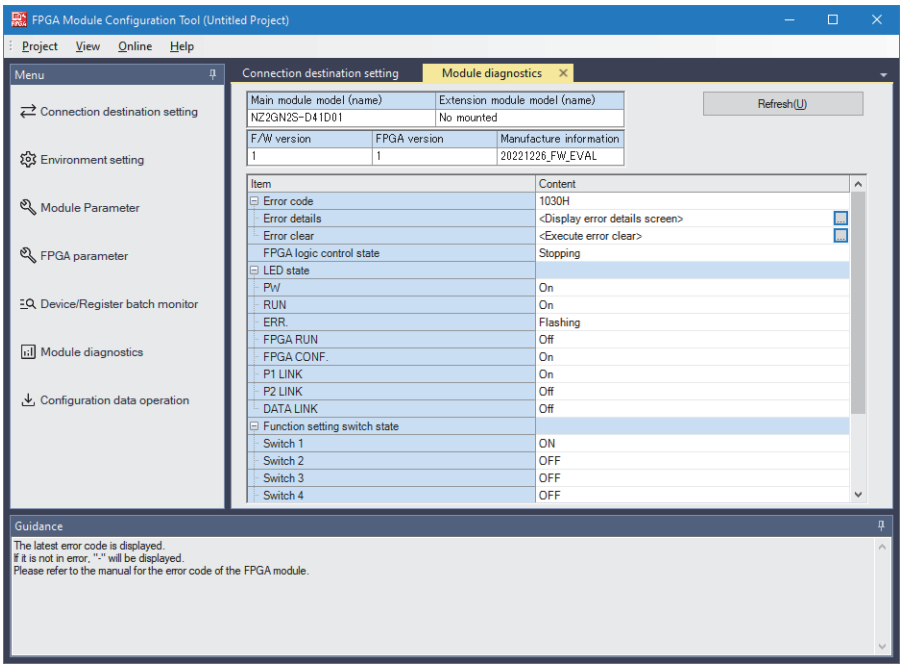
Operating procedure

1. Display the "Module diagnostics" window.

[Menu] ⇨ [Module diagnostics]



2. To get the latest information, click the [Refresh] button.



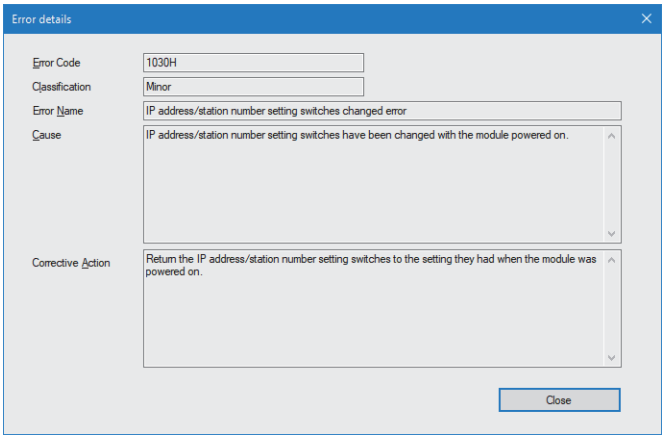
Item	Display content
Main module model (name)	Displays the model name of the Main module.
Extension module model (name)	Displays the model name of the Extension module.
F/W version	Shows the firmware version.
FPGA version	Displays the FPGA version.
Manufacture information	Displays manufacturing information for the module.
Error code	Displays the latest error code occurring in the module. If no error has occurred "—" is displayed.
FPGA logic control state	Displays the FPGA logic control state.
LED state	The lighting state of the module operation status indicator LED is stored.
Function setting switch state	The ON/OFF statuses of the function setting switches are stored. • Function setting switches 1 to 3: Status of the function setting switches when the power is turned on • Function setting switches 4 to 10: Current status of the function setting switches

Error details window

The following describes how to check the details of an error that has occurred.

Operating procedure

1. Double-click <Display error details screen>.
2. The "Error details" window is displayed.



Executing error clear

The method for executing error clear is shown below.

1. Eliminate the cause of the error.
2. Double-click <Execute error clear>.
3. Click the [Yes] button.
4. Click the [OK] button.

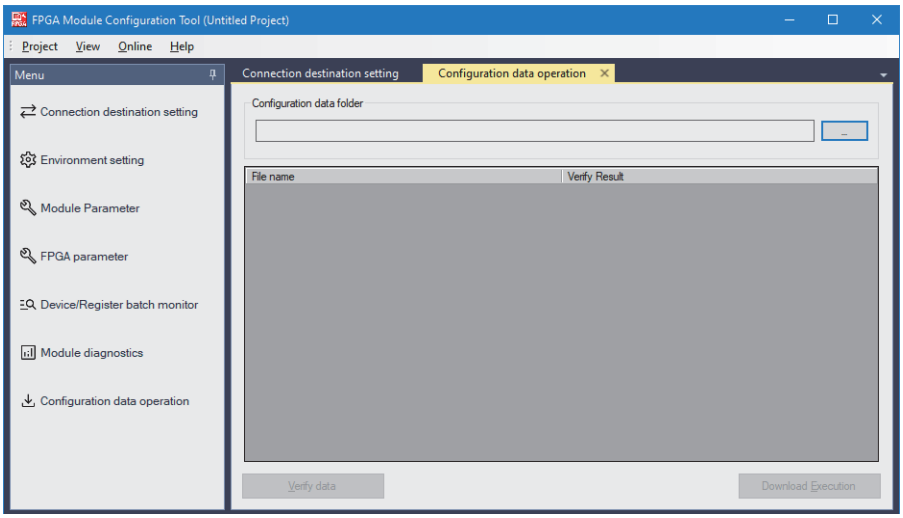
Configuration data operation

Verifies or downloads the configuration data created using the FPGA development software to the configuration ROM in the FPGA module.

Operating procedure

1. Display the "Configuration data operation" window.

[Menu] ⇨ [Configuration data operation]

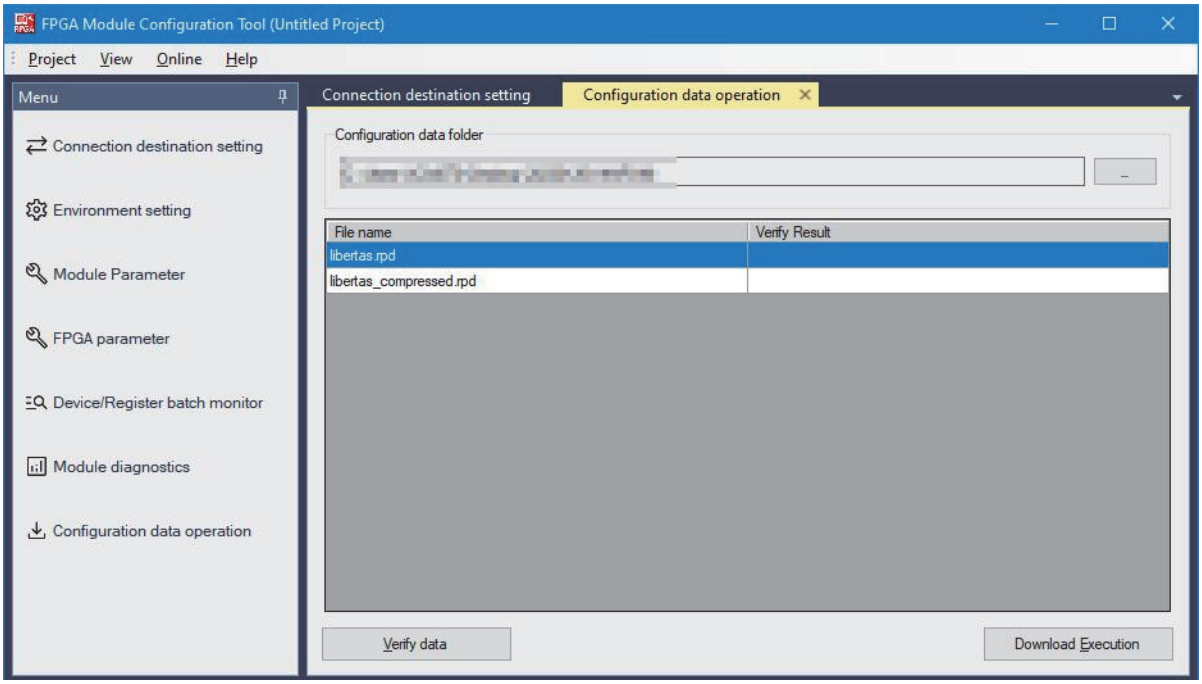


Data verification

Verifies the configuration data created using the FPGA development software and the configuration ROM in the FPGA module.

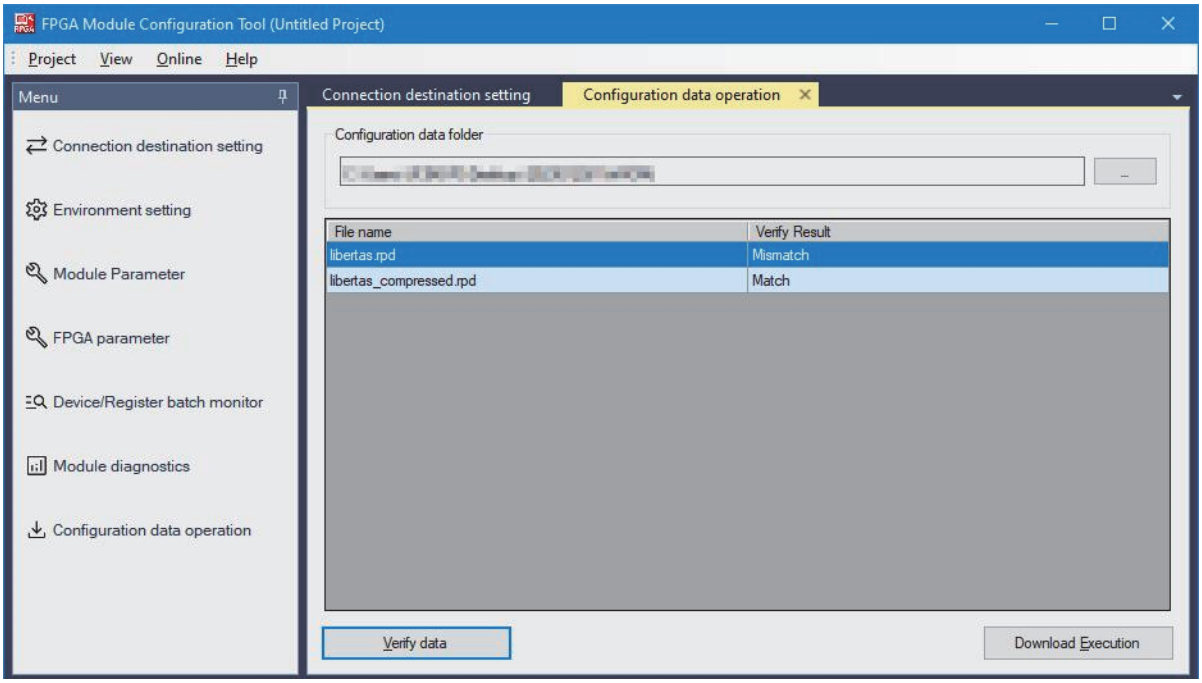
Operating procedure

1. Select the configuration data folder.
2. The configuration data files in the selected folder are displayed.



3. Click the [Verify data] button.
4. The verification results are displayed.

Match or Mismatch is displayed in the verification results.

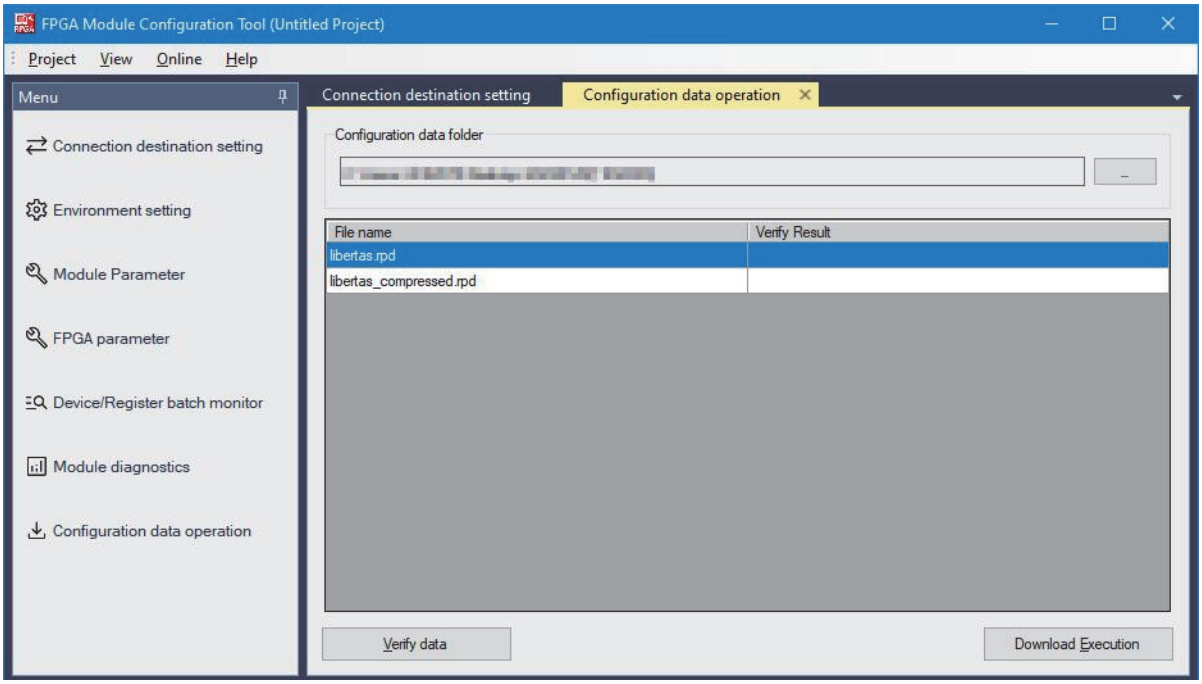


Download execution

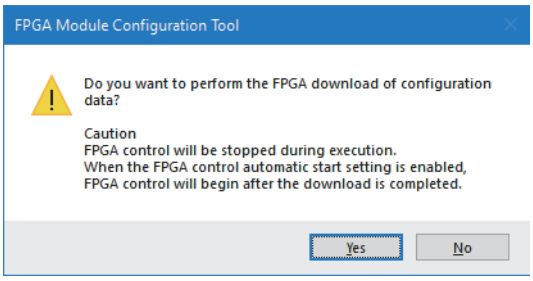
Downloads the configuration data created using the FPGA development software to the configuration ROM in the FPGA module.

Operating procedure

1. Select the configuration data folder.
2. The configuration data files in the selected folder are displayed.



3. Select the file to be downloaded.
4. Click the [Download Execution] button.
5. Click the [Yes] button.



8.8 Optional Functions

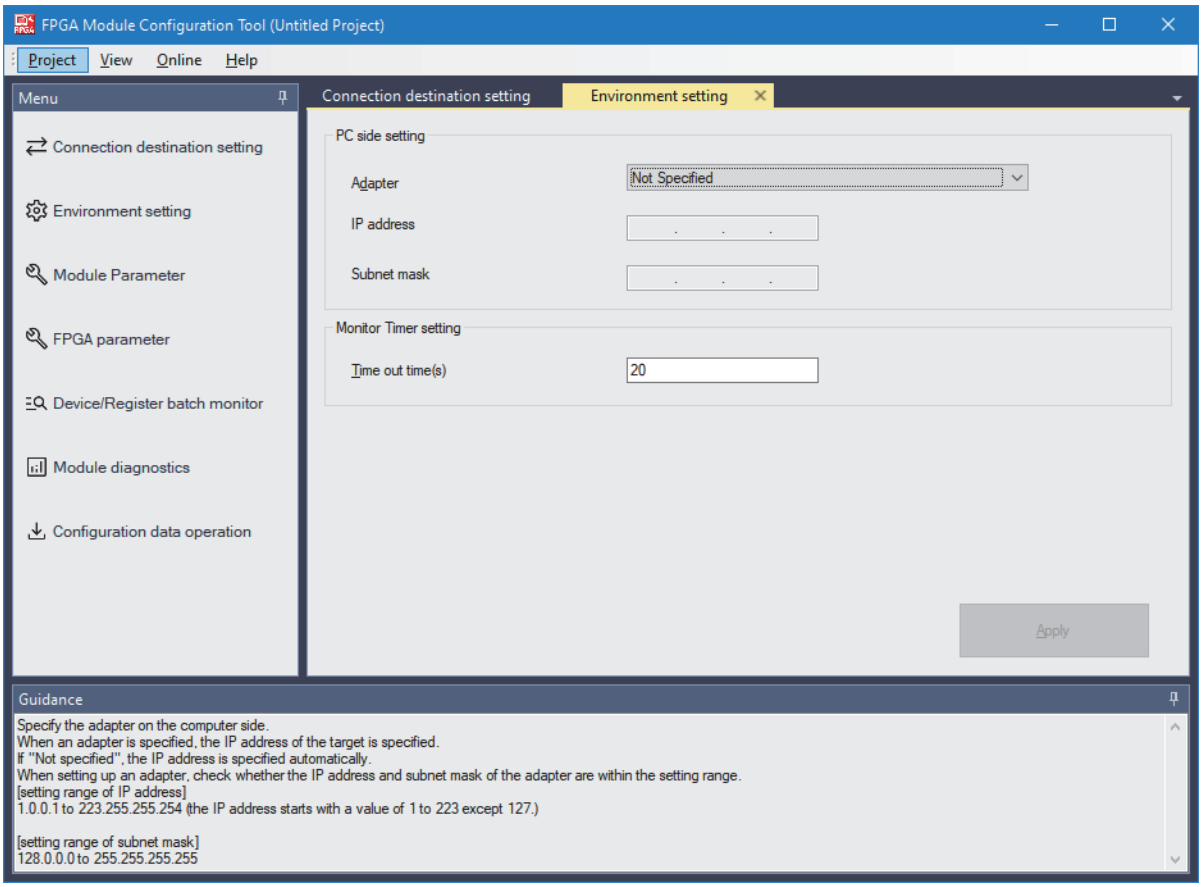
Environment setting

The following describes how to configure settings such as communication settings and timeout time on the personal computer side.

Operating procedure

1. Set the value in the "Environment setting" window.

[Menu] ⇨ [Environment setting]



Item		Setting range
PC side setting	Adapter	—
	IP address	1.0.0.1 to 223.255.255.254 (The beginning of the IP address must start with a value between 1 and 223, excluding 127.)
	Subnet mask	128.0.0.0 to 255.255.255.255
Monitor Timer setting	Time out time	1 to 30

2. Click the [Apply] button.

8.9 Help Function

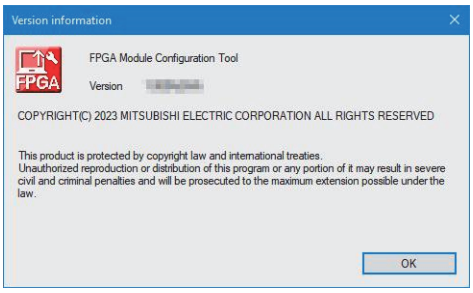
A check of the version of the FPGA Module Configuration Tool is provided as a help function.

Checking the version of the FPGA Module Configuration Tool

Perform the following to check the version of the FPGA Module Configuration Tool.

Operating procedure

[Help] ⇨ [Version information]



9 PARAMETER SETTING

Use the FPGA Module Configuration Tool for setting the parameters of the FPGA module.
For instructions on how to install the FPGA Module Configuration Tool, refer to the following.
FPGA Module Configuration Tool Installation Instructions

About the parameters

The parameters of the FPGA module are of the following two types.

- Module parameters (Page 95 Module parameters)
- FPGA parameters (Page 98 FPGA parameters)

9.1 For Standalone Mode

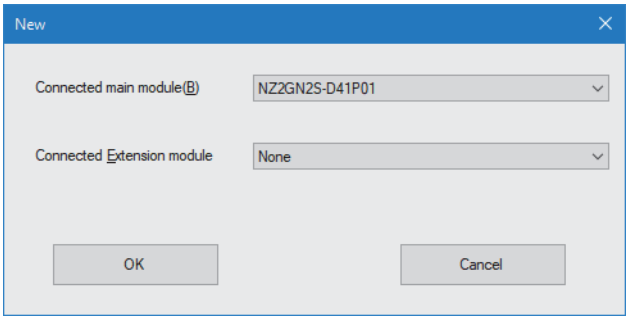
Set the parameter values in the FPGA Module Configuration Tool.

Setting method

Operating procedure

1. Start the FPGA Module Configuration Tool.
2. From "New", select "Connected main module" or "Connected Extension module".

[Project] ⇨ [New]

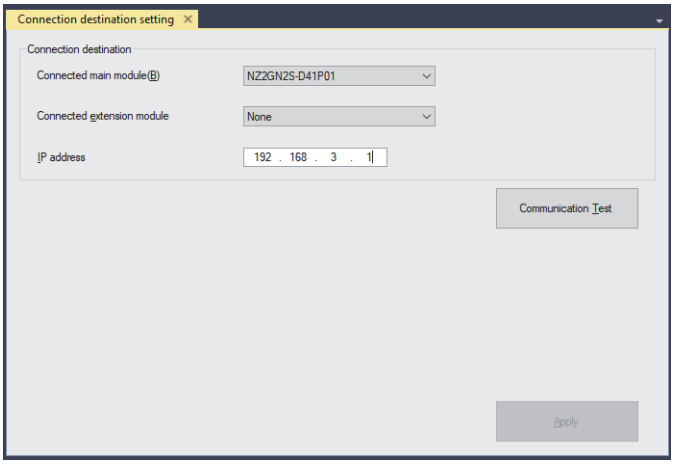


Item	Setting range
Connected main module	• NZ2GN2S-D41D01 • NZ2GN2S-D41P01 • NZ2GN2S-D41PD02
Connected Extension module	• None • NZ2EX2S-D41A01 • NZ2EX2S-D41D01 • NZ2EX2S-D41P01

3. Click the [OK] button.

4. Enter the IP address of the connected FPGA module from "Connection destination setting".

[Menu] ⇨ [Connection destination setting]



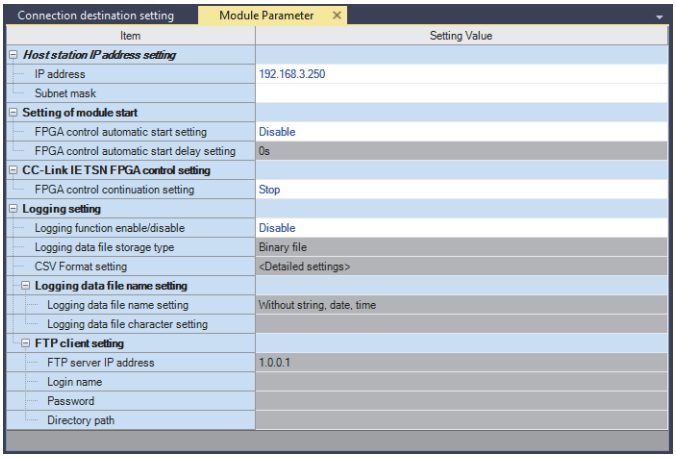
5. Click the [Communication Test] button.

6. Click the [OK] button.

7. Click the [Apply] button.

8. Set the parameter value in "Module Parameter".

[Menu] ⇨ [Module Parameter]



9. Set the values of the FPGA parameters in "FPGA parameter".

[Menu] ⇨ [FPGA parameter]

Connection destination setting | Module Parameter | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.15μs	0.15μs	0.15μs	0.15μs	0.15μs	0.15μs
Filter sampling pulse	Data sampling timin	Data sampling timin	Data sampling timin	Data sampling timin	Data sampling timin	Data sampling timin
Data update timing	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs
Logging cycle timing	1μs					
Digital input control part setting						
Input filter upper limit value						
Input filter upper limit value X0	4000	4000	4000	4000	4000	4000
Input filter upper limit value X1	4000	4000	4000	4000	4000	4000
Input filter upper limit value X2	4000	4000	4000	4000	4000	4000
Input filter upper limit value X3	4000	4000	4000	4000	4000	4000
Input filter upper limit value X4	4000	4000	4000	4000	4000	4000
Input filter upper limit value X5	4000	4000	4000	4000	4000	4000
Input filter upper limit value X6	4000	4000	4000	4000	4000	4000
Input filter upper limit value X7	4000	4000	4000	4000	4000	4000
Input filter upper limit value X8	4000	4000	4000	4000	4000	4000
Input filter upper limit value X9	4000	4000	4000	4000	4000	4000
Input filter upper limit value XA	4000	4000	4000	4000	4000	4000
Input filter upper limit value XB	4000	4000	4000	4000	4000	4000
Input filter upper limit value XC	4000	4000	4000	4000	4000	4000
Input filter upper limit value XD	4000	4000	4000	4000	4000	4000
Input filter upper limit value XE	4000	4000	4000	4000	4000	4000
Input filter upper limit value XF	4000	4000	4000	4000	4000	4000

10. Write the Module parameter and FPGA parameters to the FPGA module.

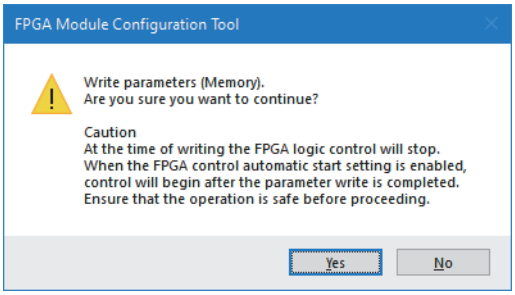
[Online] ⇨ [Parameter write (Memory)] or [Parameter write (Memory + Non-volatile memory)]

Write destination	Setting values after the FPGA module is powered off	Application
Memory	Not saved.	When adjusting the setting value
Memory + Non-volatile memory	Saved in non-volatile memory.	When wishing to use the set values the next time the FPGA module power is turned on

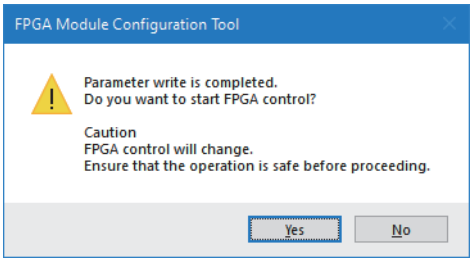
Point

The IP address and subnet mask are saved in non-volatile memory regardless of whether the parameter write destination is memory or memory + non-volatile memory.

11. Click the [Yes] button.



12. Click the [Yes] button.



9.2 For CC-Link IE TSN Communication Mode

Assure that the network parameters have been written to the CPU module of the master station. For the setting procedure for the master station, refer to the following.

User's manual for the master station used

Communication cycle interval setting

When using the FPGA module in CC-Link IE TSN communication mode, set the communication cycle interval as follows.

■When the CC-Link IE TSN Class of the FPGA module is CC-Link IE TSN Class B

Communication speed		Value that can be set
Master station	FPGA module	
1Gbps	1Gbps	■When the value is set in increments of 1μs 125.00μs to 10000.00μs ■When the value is not set in increments of 1μs One of the following values 31.25μs, 62.5μs, 125.00μs, 250.00μs, 500.00μs, 1000.00μs, 2000.00μs, 4000.00μs, or 8000.00μs
	100Mbps*1*3	■When the value is set in increments of 1μs 125.00μs to 625.00μs ■When the value is not set in increments of 1μs One of the following values 125.00μs, 250.00μs, 500.00μs
100Mbps	100Mbps*2	■When the value is set in increments of 1μs 500.00μs to 10000.00μs and a value divisible by 2μs ■When the value is not set in increments of 1μs One of the following values 500.00μs, 1000.00μs, 2000.00μs, 4000.00μs, or 8000.00μs

*1 When using the FPGA module in this combination, set the "Communication Period Setting" of the FPGA module to "Low-Speed".

*2 When using the FPGA module in this combination, set the "Communication Period Setting" of the FPGA module to "Basic Period" or "Normal-Speed".

*3 Use a TSN hub when communicating between Master station and FPGA module with different communication speeds.

■When the CC-Link IE TSN Class of the FPGA module is CC-Link IE TSN Class A

The Basic Period of the FPGA module (communication cycle interval setting) should be set to a value with a multiplier that results in a value that is 2.5ms or more and 1.28s or less.

Item	Description
Basic period (Communication period interval setting)	Setting values of the communication period interval setting of master station parameters
Magnification	Magnification that is determined by the following master station parameters • Setting values of the communication period setting for network configuration setting • Setting values of the multiple period setting for master station parameters

If the communication speed of the master station is 1Gbps and the communication speed of the FPGA module is 100Mbps, set the communication period setting of the FPGA module to "Low-Speed".

Ex.

When the communication period setting of the FPGA module is set to "Low-Speed" in the network structure settings, and "16x" is set for "Low-Speed" in the multiple period setting of the master station parameter

The range of the basic cycle that satisfies the conditions (the value of the communication cycle interval setting of the parameter of the master station) is 156.25μs to 80ms.

Point

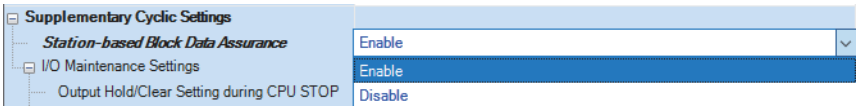
If an FPGA module that satisfies the following conditions does not establish a data link even if the above value is set for the communication cycle interval setting, check multiples of CC-Link IE TSN Class A (low speed) in the buffer memory of the master station (buffer memory address: 1294304).

- The CC-Link IE TSN Class setting is CC-Link IE TSN Class A
- The communication period setting is "Low-Speed"

If multiples of CC-Link IE TSN Class A (low speed) (buffer memory address: 1294304) are 6 or more, the basic cycle (communication cycle interval setting) × magnification × CC-Link IE TSN Class A (low speed) multiple (buffer memory address: 1294304) should be between 2.5ms and 6.4s.

Station-based block data assurance

When using the FPGA module, be sure to set "Station-based Block Data Assurance" to "Enable". If "Disable" is specified, the function as an FPGA module cannot be guaranteed.



Network topology setting

When using the FPGA module in CC-Link IE TSN communication mode, set the network topology setting as follows.

- Line/Star
- Ring

Point

The ring topology can only be connected when the CC-Link IE TSN Class is CC-Link IE TSN Class B. When a CC-Link IE TSN Class A FPGA module is connected by ring topology, data links are not established.

Communication mode

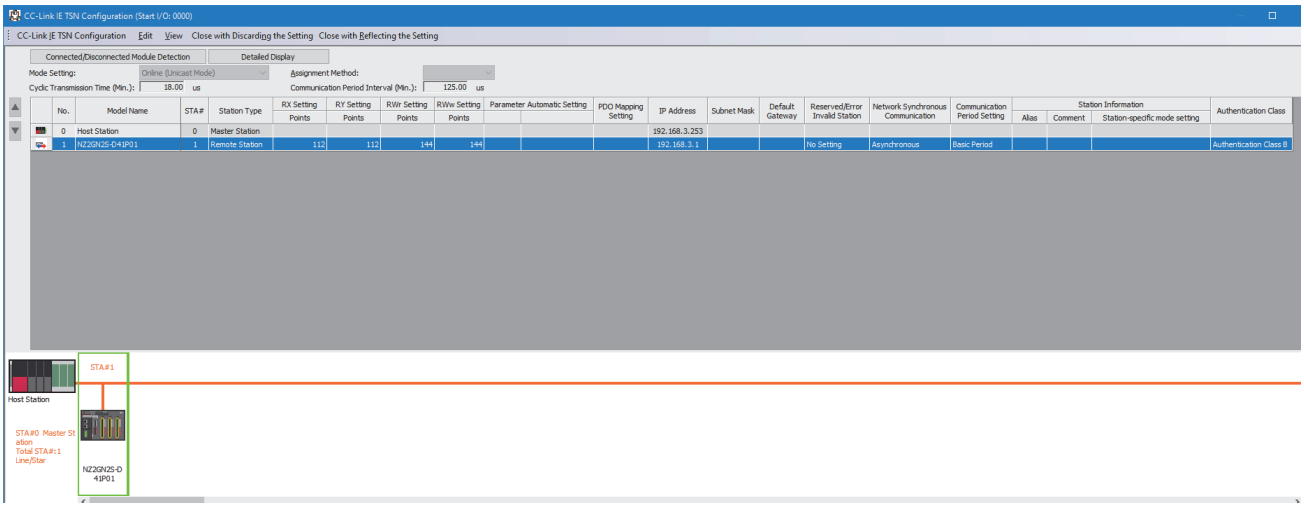
- Unicast
- Multicast

Point

When an Ethernet device (or CC-Link IE TSN Class A remote station) is connected to the FPGA module in multicast mode, the Ethernet device (or CC-Link IE TSN Class A remote station) connected to the FPGA module will not be relayed multicast cyclic frames.

CC-Link IE TSN structure

Window



In this manual, "Authentication Class" is described as "CC-Link IE TSN Class".

Displayed items

Item		Description	Setting range
RX Setting, RY Setting	Points	Set the assignment of RX/RY points.	0 to 112 (Default value: 112)
	Start	The RX/RY start number is displayed.	—
	End	The RX/RY end number is displayed.	—
RWr Setting, RWw Setting	Points	Set the assignment of RWr/RWw points.	0 to 144 (Default value: 144)
	Start	The RWr/RWw start number is displayed.	—
	End	The RWr/RWw end number is displayed.	—
IP Address		Set the IP address of the FPGA module to be connected. If the set IP address is different from the IP address set with the IP address/station number setting switch, cyclic transmission with the master station cannot be performed and data link will not be established. (☞ Page 54 IP address/station number setting switch setting)	0.0.01 to 223.255.255.254
Network Synchronous Communication Setting		Sets whether to use the CC-Link IE TSN Network synchronous communication function.	• Do not Synchronize (Default) • Synchronize
Communication Period Setting		Sets the cycle of the FPGA module when setting multiple communication cycles. If the master station and FPGA module have different communication speeds, there are restrictions on the setting range. (☞ Page 132 Communication cycle interval setting)	• Basic Period • Normal-Speed • Low-Speed
CC-Link IE TSN Class		Sets the CC-Link IE TSN Class of the FPGA module. Make the same settings as the CC-Link IE TSN Class set on the FPGA module. (☞ Page 58 Setting the function setting switches)	• CC-Link IE TSN Class B • CC-Link IE TSN Class A

Point

If the CC-Link IE TSN Class set by function setting switch 2 and the CC-Link IE TSN Class set in the network configuration settings are set to different values, event code 00C81H will be recorded in the event history of the master station and the FPGA module will not establish a data link.

Network Configuration Setting

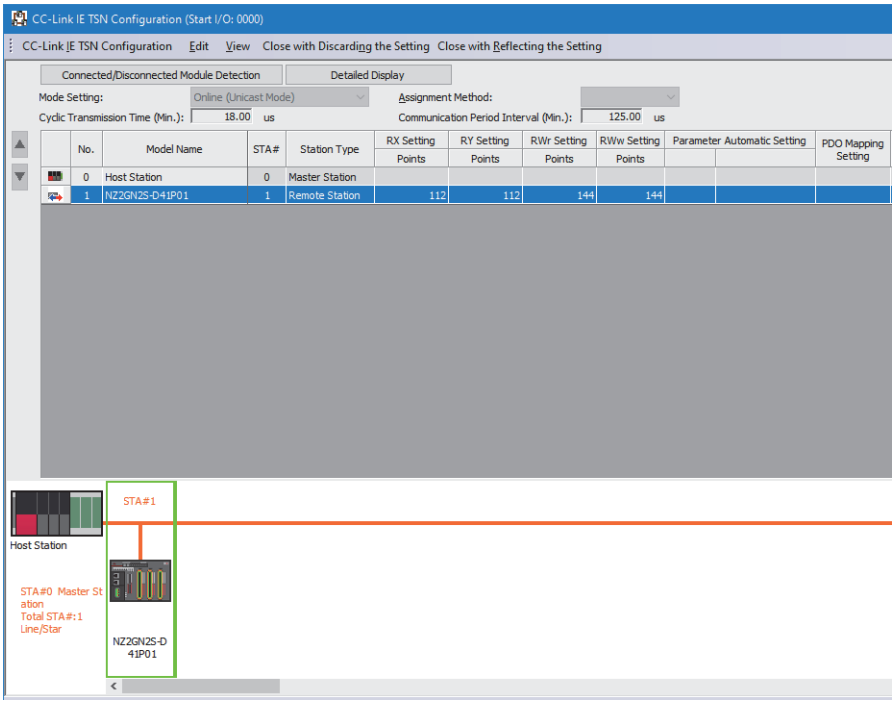
Operating procedure

1. Display the "CC-Link IE TSN Configuration" window.

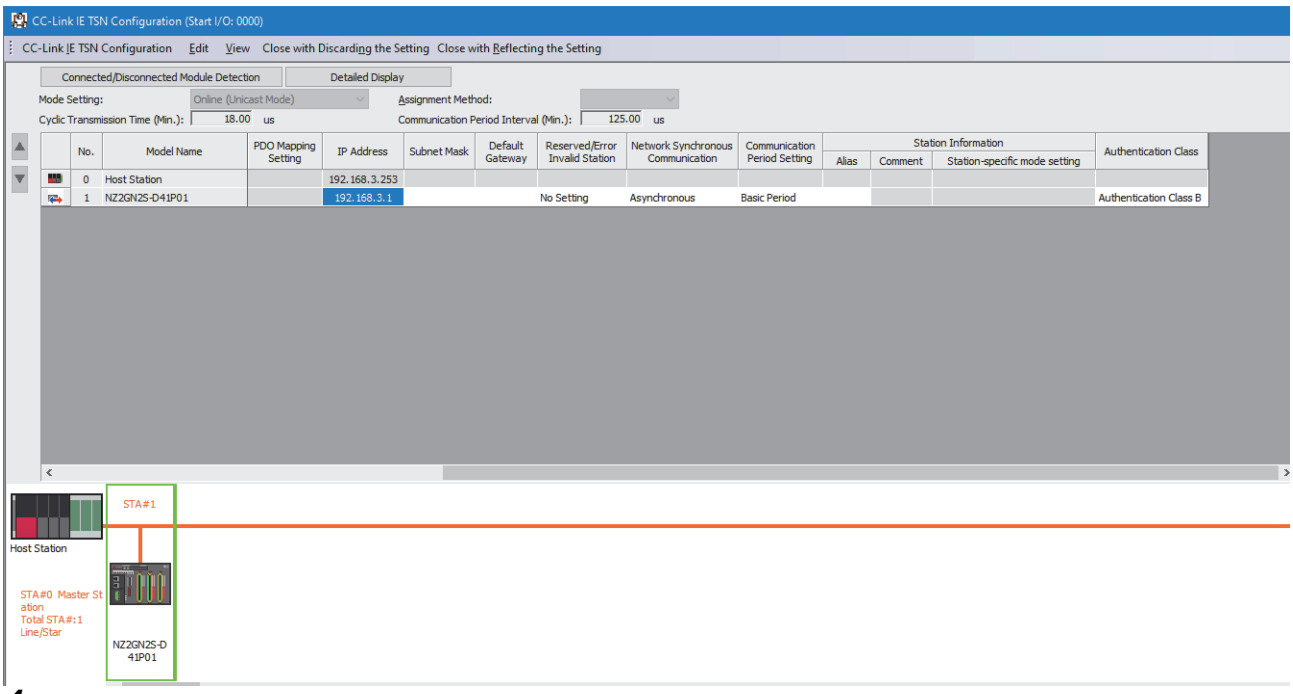
[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ Model ⇨ [Basic Setting] ⇨ [Network Configuration Settings]

2. Select the Main module of the FPGA modules from the "Module List" and drag and drop it onto the station list or network structure diagram.

"Station Type", "RX/RY setting" and "RWw/RWr setting" are automatically set to Input. Change the value as necessary. Extension module settings are not required.



3. Enter the IP address of the FPGA module.



4. Select [Close with Reflecting the Setting] to close the "CC-Link IE TSN Configuration" window.

5. Click the [Apply] button.

6. Write the set parameters to the CPU module of the master station and reset the CPU module of the master station, or turn off and on the power supply of the programmable controller.

[Online] ⇨ [Write to PLC]

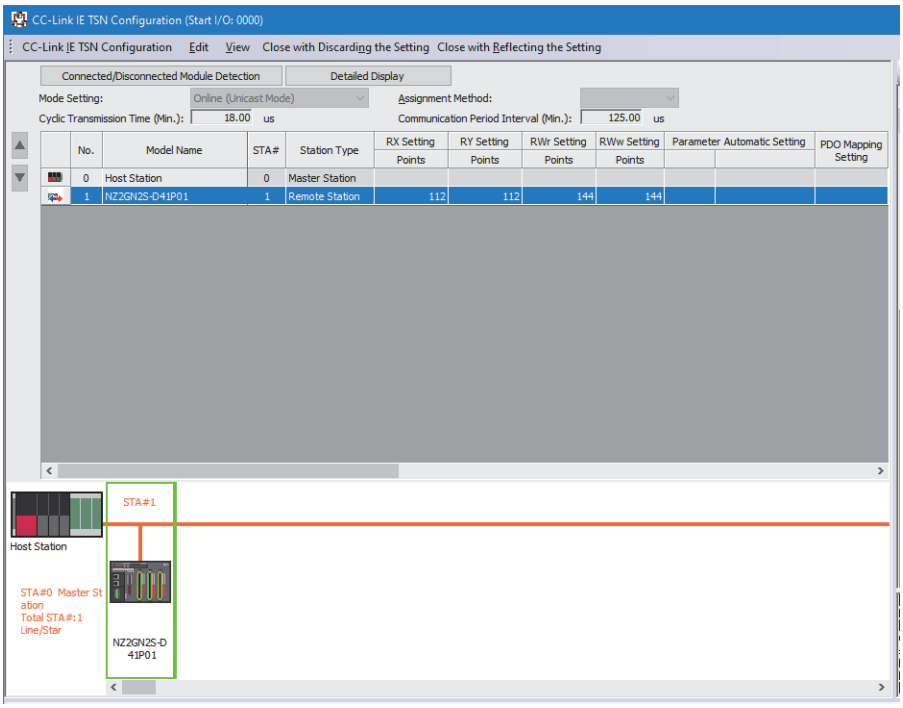
7. Set the CPU module of the master station to RUN, and check that the DATA LINK LED of the FPGA module is turned on.

Parameter setting

Operating procedure

1. Display the "CC-Link IE TSN Configuration" window.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ Model ⇨ [Basic Setting] ⇨ [Network Configuration Settings]



2. Double-click the FPGA module to start the FPGA Module Configuration Tool.

3. All steps after step 3 are the same as in standalone mode.

☞ Page 129 For Standalone Mode

MEMO

PART 5 FPGAs

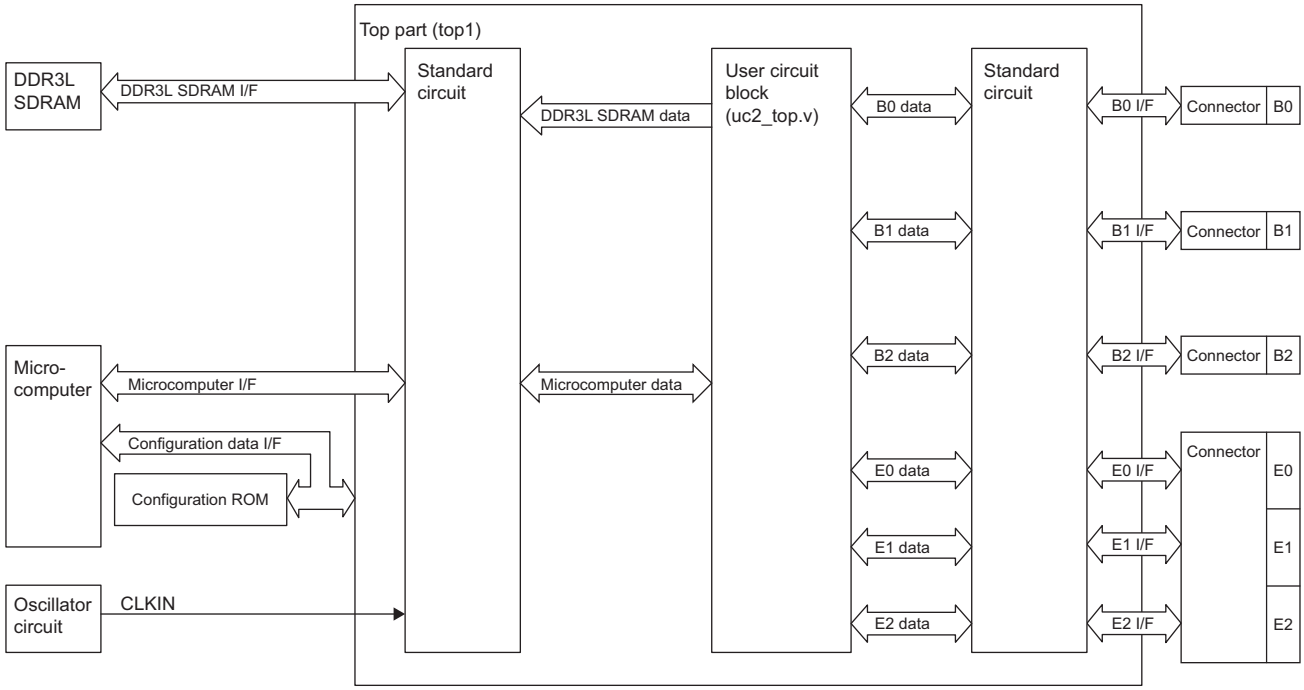
This part consists of the following chapters.

10 FPGA DEVELOPMENT

A sample circuit is written in the configuration ROM of the factory-shipped FPGA module. This chapter shows an example of changing the sample circuit.

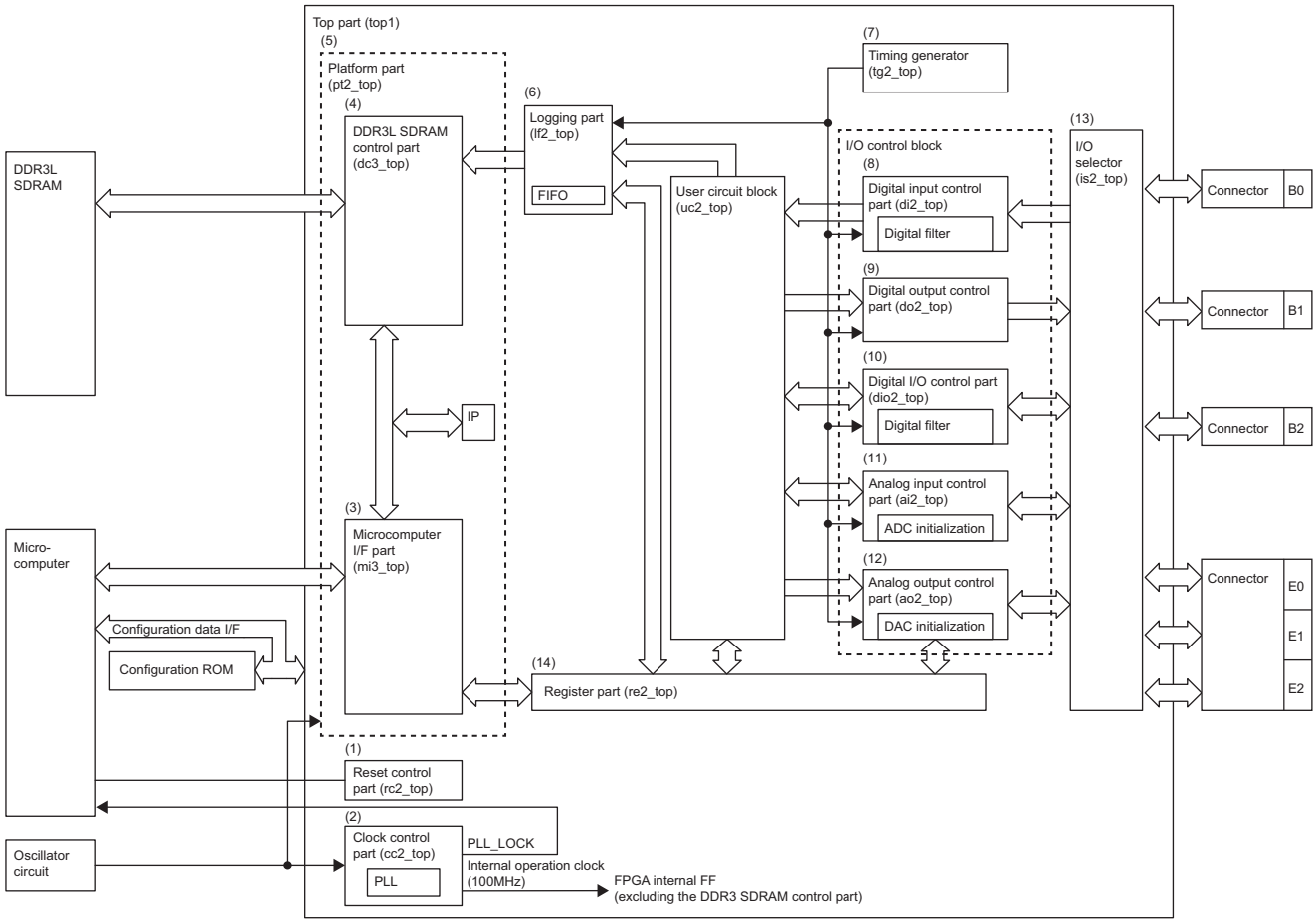
10.1 FPGA Development Procedures

The only block that requires to be developed (design/verification) is the user circuit block (uc2_top.v). Do not modify the circuit description of the standard circuit. If the standard circuit is modified, the operation of various functions cannot be guaranteed. The FPGA configuration of the FPGA module is shown below.



Standard circuit block

The configuration of the standard circuit block is shown below.



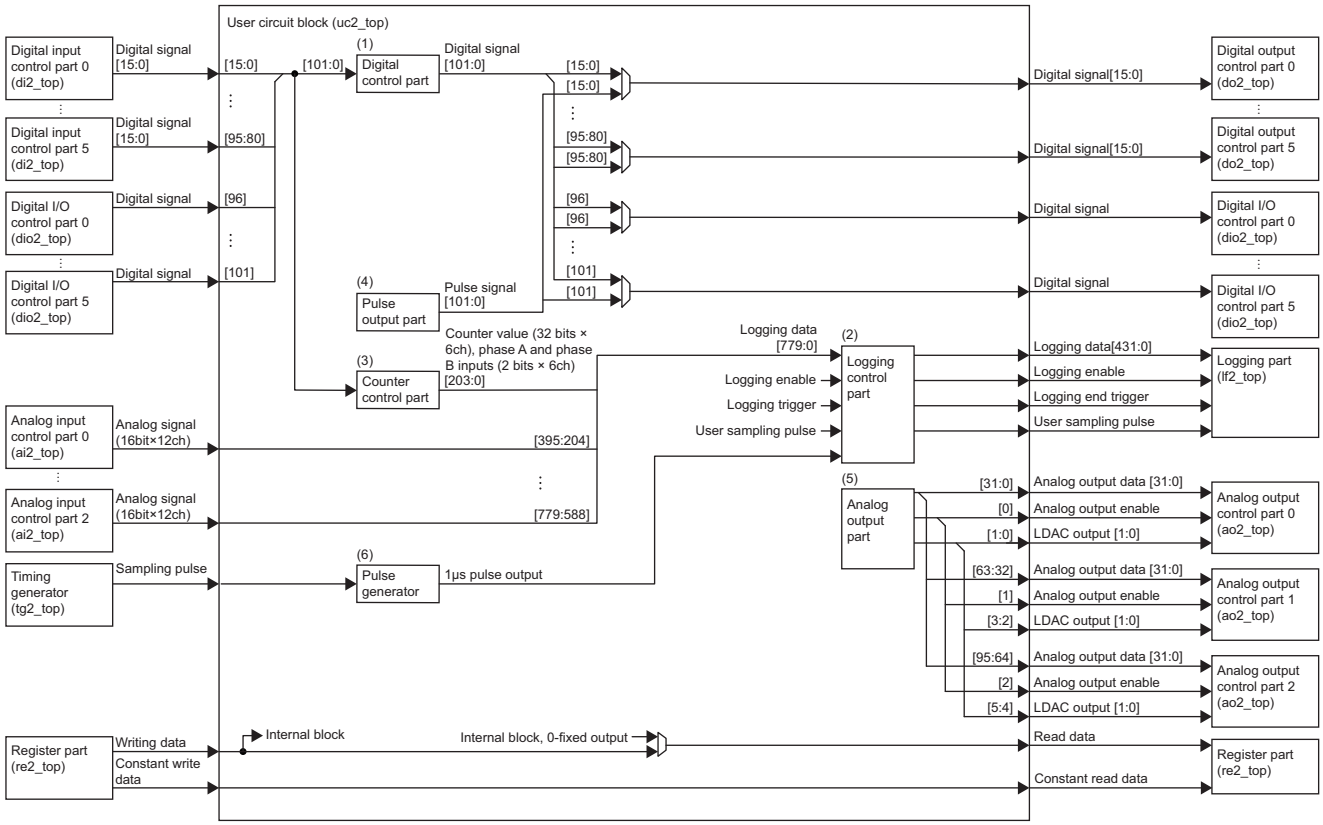
No.	Function block	Function
(1)	Reset control part (rc2_top.v)	Controls the reset inside the FPGA. The reset signal from the microcomputer is connected to all register areas in the FPGA.
(2)	Clock control part (cc2_top.v)	Generates the system clock used inside the FPGA. The system clock is 100MHz.
(3)	Microcomputer I/F part (mi3_top.v)	Controls register access/memory access from the microcomputer. It controls the 16-bit data bus.
(4)	DDR3L SDRAM control part (dc3_top.v)	Write the logging data output from the logging part to DDR3L SDRAM. In addition, logging data is read from DDR3L SDRAM by a read request from the microcomputer I/F part.
(5)	Platform part (pt2_top.v)	Implements Intel® FPGA Avalon® interface and connects the FPGA internal IP and the microcomputer I/F part. This function block has a program ROM, WorkRAM, and DPRAM for output value storage, which are equipped as peripheral circuits for FPGA internal CPU (Nios® Ⅱ/e). The platform part implements following functions. • Function to control writing of logging data to DDR3L SDRAM • The microcomputer I/F part and Nios® Ⅱ/e control read/write to DDR3L SDRAM.
(6)	Logging part (lf2_top.v)	The output signal of the user circuit block is stored in the internal memory (FIFO) for each logging cycle timing pulse output from the timing generator. The data is also stored in DDR3L SDRAM via the platform part. The logging part implements the following functions. • User circuit block I/F • Platform part I/F • Logging data sampling • Logging operation (trigger operation mode) • Logging operation (storage operation mode) • DDR3L SDRAM control • User sampling pulse cycle monitoring • Time control

No.	Function block	Function
(7)	Timing generator (tg2_top.v)	Generates input/output timing between the input/output control block and the user circuit block. The following four timing signals are generated. • Sampling pulse for digital input filter • Digital/analog data sampling pulse • Digital/analog data update pulse • Logging cycle timing pulse
(8)	Digital input control part (di2_top.v)	Removes noise and outputs signals to the circuits (register part, user circuit block) in the subsequent stage. The digital input control part implements the following functions. • Digital filter function • Function to digital-filter signals to output to the register part and user circuit block
(9)	Digital output control part (do2_top.v)	Outputs signals from the register part and user circuit block to the outside of the FPGA via the input/output selection part. Also, when the FPGA has stopped operating, the value that was output immediately before the stop is held (HOLD) or cleared (CLEAR). The digital output control part implements the following functions. • Digital output signal selection function • HOLD/CLEAR function
(10)	Digital input/output control part (dio2_top.v)	Removes noise and outputs signals to the circuits (register part, user circuit block) in the subsequent stage. Outputs signals from the register part and user circuit block to the outside of the FPGA via the input/output selection part. Also, when the FPGA has stopped operating, the value that was output immediately before the stop is held (HOLD) or cleared (CLEAR). The digital input/output control part implements the following functions. • Digital filter function • Function to digital-filter signals to output to the register part and user circuit block • Digital output signal selection function • HOLD/CLEAR function
(11)	Analog input control part (ai2_top.v)	Controls the ADC connected to the outside of the FPGA and captures analog values. The analog input control part implements the following functions. • Signal generation for clock synchronous serial IF • ADC initialization • Function to output the A/D conversion value to the register part and user circuit block for each data sampling pulse
(12)	Analog output control part (ao2_top.v)	Controls the DAC connected to the outside of the FPGA and outputs analog values to devices connected to the module. The analog output control part implements the following functions. • Signal generation for clock synchronous serial IF • DAC initialization • Function to select and output the D/A conversion value from the register part or user circuit block at each data update timing.
(13)	Input/output selector (is2_top.v)	Uses the module type signal to switch the input/output of FPGA external terminals. The input/output selector implements the I/O terminal switching function.
(14)	Register part (re2_top.v)	Implements the register inside the FPGA. The register part implements the following functions. • Function to notify FPGA setting values internal to the FPGA and to notify the microcomputer of signals (monitored) inside the FPGA. • FPGA version register*1

*1 The FPGA version register is the version of the provided standard circuit and sample circuit.

User circuit block

The configuration of the user circuit block at the time of shipment from the factory is shown below.



No.	Function block	Function
(1)	Digital control part	Inverts digital signals input from the digital input control part and digital input/output control part, and controls output enable/disable.
(2)	Logging control part	Selects and outputs the logging data to be logged and the signal that controls the logging part. The logging control part implements the following functions. • Logging data selection • Logging enable selection • Logging end trigger selection • User sampling pulse selection
(3)	Counter control part	Implements the following counters that operate with the signal from the digital input control part. • 32-bit ring counter (2-phase multiple of 4) • 32-bit ring counter (1-phase multiple of 1)
(4)	Pulse output part	Outputs the following pulses to the digital output control part/digital input/output control part. • 0 degree pulse • 90 degree pulse • 180 degree pulse • 270 degree pulse The pulse can be set in units of 10ns.
(5)	Analog output part	Generates the following DAC signals to be connected to the FPGA by register settings. • D/A conversion value • D/A conversion value enable • LDAC
(6)	Pulse generator	Generates a 1µs pulse for logging data generation.
(7)	Other connections	The following functions are implemented as other connections. • HOLD/CLEAR of digital signals • User interrupt output • Connection control of various signals

When not modifying the user circuit block

If the user circuit block is not modified, the configuration ROM can be used without modification. For usage examples, refer to the following.

☞ Page 298 FUNCTIONS
☞ Page 366 SAMPLE CIRCUIT IN STANDALONE MODE

When developing the FPGA with a modified user circuit block

The following products are required for FPGA development with a modified user circuit block.

Product name	Application	Remarks
Intel® FPGA download cableII	Configuration data write	—
FPGA development environment for the CC-Link IE TSN FPGA module	Development environment construction	A generation environment (a set of data such as design environment (RTL), verification environment, and logic synthesis environment) of configuration data written in the factory default FPGA module. Use this data to develop the FPGA. Please consult your local Mitsubishi representative.
Intel® Quartus Prime	Logic synthesis	Install this product from the website of Intel Corporation. www.intel.com
ModelSim-Intel® FPGA STARTER EDITION	Verification (HDL simulator running on a personal computer)	This product is included in the Lite Edition of Intel® Quartus Prime.

Point

The source code of the FPGA development environment for the CC-Link IE TSN FPGA module is written in Verilog.

Procedures for editing the user circuit block

The procedures for editing the user circuit block are shown below.

1. Checking FPGA information

Check the FPGA terminal information and FPGA input/output timing.

☞ Page 141 Standard circuit block
☞ Page 143 User circuit block

2. FPGA design and coding

Perform the design and coding based on the information required for the system.

3. FPGA verification

Perform FPGA verification from the top layer including the user circuit. The verification patterns of the sample circuit are included in the provided verification environment. Use them as samples.

☞ Page 146 FPGA Verification Procedure

4. FPGA logic synthesis

Perform FPGA logic synthesis from the top layer including the user circuit block. By using the provided FPGA logic synthesis environment, restrictions are imposed on the top terminal of the FPGA. If a new restriction is required, add the restriction.

☞ Page 174 FPGA Logic Synthesis Procedures

10.2 FPGA Design Procedures

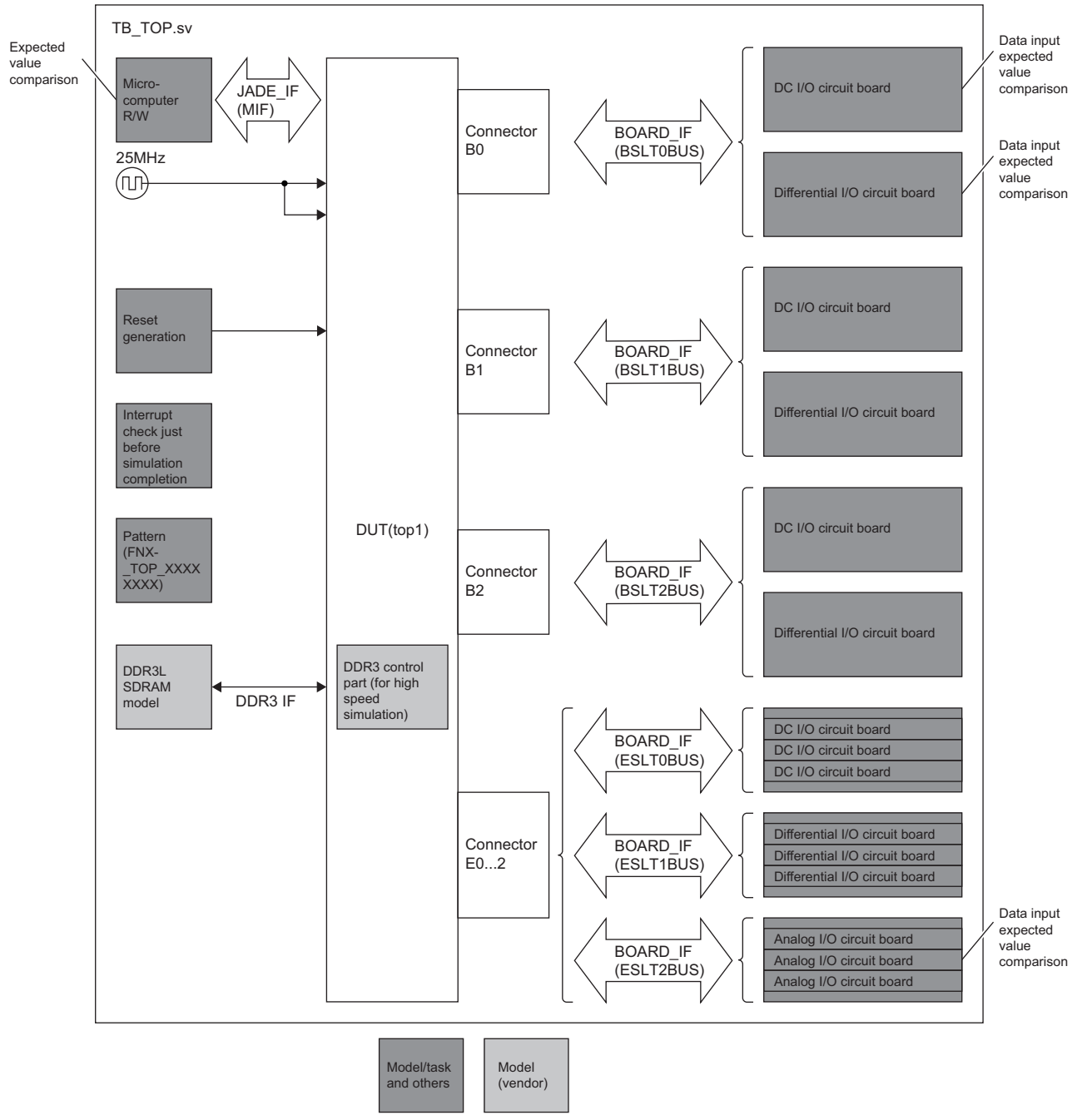
When editing the user circuit block, change the RTL of the synthesis environment ($HOME\RTL\TOP\UC). For input/output (terminal list, timing) connected to the user circuit block, refer to the following.

☞ Page 218 Connection block list
☞ Page 610 List of User Circuit Block Terminals
☞ Page 220 Module common interface

10.3 FPGA Verification Procedure

Verification environment

The verification environment for the sample circuit and the configuration of the verification environment are shown below.
○: Need to be changed according to the user circuit block, △: Need to be changed according to the development environment, ×: Do not change



No.	Directory					Description	Changeability
(1)	$HOME	—				Simulation top folder	×
(2)		RTL	—			RTL storage directory	×
(3)			TOP	—		RTL storage directory (top layer)	×
(4)				UC/		RTL storage directory (UC) (user circuit block)	△
(5)				*/		RTL storage directory (TOP, each block) (standard circuit)	×
(6)		vendormod	—			Vendor model (outside the FPGA) storage directory	×
(7)			DDR3			DDR3L SDRAM model storage directory	×
(8)		SIM_TOP	—			TOP verification environment	×
(9)			log/			Storage directory for the simulation execution log	×
(10)			wave/			Waveform storage directory	×
(11)			pat/	—		Simulation pattern storage directory	×
(12)				FNx_TOP_XXXXXX.sv		Simulation pattern	○
(13)			sim/	—		Simulation execution directory	×
(14)				scr	—	Storage directory for simulation execution scripts	×
(15)					00_RTL_build.do	RTL compilation script	△
(16)					02_VMD_build.do	Vendor model compilation script	×
(17)					50_SimGo.do	Execution script for single/all simulation(s)	△
(18)					param.do	Simulation setting file, which specifies the FPGA development software installation directory.	△
(19)					wave.do	Dump signal specification file	×
(20)				inc	—	Storage directory for TB_TOP.sv include files	×
(21)					glb_set.sv	Common variables, microcomputer/slot I/F, microcomputer R/W tasks	×
(22)					tb_common.sv	Common tasks, clock/reset, Sim termination display, timeout processing	×
(23)					dut_inst.sv	Test target signal declaration, instances, comparison function for slot output signals	×
(24)					model_set.sv	Connection selection from DDR3L SDRAM model, DC and differential input/output circuit board models	×
(25)					board.sv	Circuit board models (DC input/output circuit board, differential input/output circuit board, analog input/output circuit board)	×
(26)				TB_TOP.sv		Test bench top	×
(27)				run_sim.bat		ModelSim path specification, and batch execution of single/all simulation(s)	△
(28)		lib				Simulation library storage directory for FPGA design software	△

Procedure for executing verification environment

The execution procedure of the provided verification environment is shown below.

1. Open (27) run_sim.bat in the configuration of the verification environment and modify the description of MODELSIM_DIR to match the Model-sim installation folder.
2. Open (18) param.do in the configuration of the verification environment and modify the description of QUARTUS_INSTALL_DIR to match the FPGA development software installation folder.
3. Store the modified RTL in (4) UC/ in the configuration of the verification environment.
4. Open (15) 00_RTL_build.do in the configuration of the verification environment and modify the description of vlog ${RTLDIR}/UC/*.v. For example, when writing in VHDL, change it to vcom ${RTLDIR}/UC/*.vhd. If any change is not required, no modification is necessary.
5. Store the simulation library stored in the FPGA design software into (28) lib in the configuration of the verification environment. The sample circuit can be simulated by storing the libraries shown below.

220model.v
altera_lnsim.sv
altera_mf.v
altera_primitives.v
cyclonev_atoms.v
cyclonev_atoms_ncrypt.v
cyclonev_hmi_atoms_ncrypt.v
cyclonev_hssi_atoms_ncrypt.v
cyclonev_pcie_hip_atoms.v
cyclonev_pcie_hip_atoms_ncrypt.v
sgate.v

6. Check the difference between the */ file of (5) in the configuration for the verification environment and the RTL of the FPGA development environment for the CC-Link IE TSN FPGA module. If there is any difference, store the file downloaded again from the Mitsubishi Electric FA site.
7. After modifying the provided patterns stored in (12) FNx_TOP_XXXXXX.sv in the configuration of the verification environment, store them in the same location.
8. Open (17) 50_SimGo.do in the configuration of the verification environment and modify the description of TBLIST with simulation pattern names.
9. Go to (13) sim/ in the configuration of the verification environment and enter the command to execute the pattern. The command to be input is as follows.

- To execute all patterns described in step 8: $ ./run_sim.bat
- To execute a single pattern: $ ./run_sim.bat FNA_TOP_xxxxxxxx

10. Open the waveform file output to (10) wave/ in the configuration of the verification environment and check whether it has the intended input.
11. Open the log file output to (9) log/ in the configuration of the verification environment and check that ERROR is 0 and TOTAL TIME is other than 0.

Verification item

Verification items for the provided patterns are shown below. Check the reference for details on the validation patterns.

Validation pattern name	Item	Verification item	Reference
FNA_TOP_01010101	DC input/output check	■Purpose To perform inversion control and output control for the DC input of DC input/output circuit boards, and to check that it is output as the DC output of the DC input/output circuit boards ■Check item Perform inversion control and output control for the DC input of DC input/output circuit boards, and check that it is output as the DC output of the DC input/output circuit boards. (Check the above for each of circuit boards B0, B1, B2, E0, E1, and E2.)	Page 150 DC input/ output check
FNA_TOP_01010102	Differential input/ output check	■Purpose To perform inversion control and output control for the differential input of differential input/ output circuit boards, and to check that it is output to the differential output of the differential input/output circuit boards ■Check item Perform inversion control and output control for the differential input of differential input/ output circuit boards, and check that it is output to the differential output of the differential input/output circuit boards. (Check the above for each of circuit boards B0, B1, B2, E0, E1, and E2.)	Page 152 Differential input/ output check
FNA_TOP_01010103	Pulse output check	■Purpose To check that the pulse output of the user circuit block is output to the differential output of differential input/output circuit boards ■Check item Check the operation of the pulse output of the user circuit block. (B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)	Page 154 Pulse output check
FNA_TOP_01010104	Counter operation check	■Purpose To check that 32-bit ring counters (2-phase multiple of 4)/32-bit ring counters (1-phase multiple of 1) implemented in the user circuit block count against differential inputs from differential input/output circuit boards ■Check item Check the operation of 32-bit ring counters (2-phase multiple of 4)/32-bit ring counters (1-phase multiple of 1) in the user circuit block. (B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)	Page 157 Counter operation check
FNA_TOP_01010105	Logging (non-time division mode) check	■Purpose To check that the differential input of differential input/output circuit boards is logged to DDR3L SDRAM ■Check item Perform logging for the differential input of differential input/output circuit boards and 32-bit ring counters (2-phase multiple of 4), and check that data is logged to DDR3L SDRAM. Logging is performed in trigger operation mode. (B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)	Page 162 Logging (non-time division mode) check
FNA_TOP_01010106	Analog output check	■Purpose To check that analog outputs (analog data, enable, LDAC) are performed according to the register settings of the user circuit block ■Check item Check that analog outputs (analog data, enable, LDAC) are performed according to the register settings of the user circuit block. (B0, B1, and B2 do not connect, while E0, E1, and E2 connect to analog input/output circuit boards.)	Page 165 Analog output check
FNA_TOP_01010107	Analog input and logging (time division mode) check	■Purpose To check that the analog input of analog input/output circuit boards is logged to DDR3L SDRAM ■Check item Check that the analog input of analog input/output circuit boards is logged to DDR3L SDRAM in a time division manner. Logging is performed in trigger operation mode. (B0, B1, and B2 do not connect, while E0, E1, and E2 connect to analog input/output circuit boards.)	Page 166 Analog input and logging (time division mode) check
FNA_TOP_01010108	Logging (automatic transfer mode) check	■Purpose To check that logging can be performed normally when b0 of Logging control part automatic transfer mode setting (usr_wreg_095) (FPGA register address: 1000_B12AH) is set to Enable (1) ■Check item Check that, when b0 of Logging control part automatic transfer mode setting (usr_wreg_095) (FPGA register address: 1000_B12AH) is set to Enable (1), the logging enable signal (logging start) is output according to the logging control trigger and that data is written to DDR3L SDRAM normally.	Page 168 Logging (automatic transfer mode) check

DC input/output check

■Validation pattern name

FNA_TOP_01010101

■Purpose

To perform inversion control and output control for the DC input of DC input/output circuit boards, and to check that it is output as the DC output of the DC input/output circuit boards

■Check item

Perform inversion control and output control for the DC input of DC input/output circuit boards, and check that it is output as the DC output of the DC input/output circuit boards. (Check the above for each of circuit boards B0, B1, B2, E0, E1, and E2)

■Procedure

Configuration: B0 to B2 DC input/output circuit boards and E0 to E2 DC input/output circuit boards, without verification model connection of DDR3L SDRAM

1. Reset the sequence. (Set Initialization completed signal (init_done) to 1.)
2. Set the register areas for B0 to B2 DC input/output circuit boards and E0 to E2 DC input/output circuit boards. Also, set the related register areas as shown in the table below.

Register name	Setting value	Reference
Filter sampling pulse (B0) (tim_iob0x_samp)	0000H	Page 523 Filter sampling pulse
Filter sampling pulse (B1) (tim_iob1x_samp)	0000H	
Filter sampling pulse (B2) (tim_iob2x_samp)	0000H	
Filter sampling pulse (E0) (tim_ioe0x_samp)	0000H	
Filter sampling pulse (E1) (tim_ioe1x_samp)	0000H	
Filter sampling pulse (E2) (tim_ioe2x_samp)	0000H	
Data sampling timing (B0) (tim_iob0x_en)	0009H	Page 524 Data sampling timing (B□)
Data sampling timing (B1) (tim_iob1x_en)	0013H	
Data sampling timing (B2) (tim_iob2x_en)	001DH	
Data sampling timing (E0) (tim_ioe0x_en)	0009H	Page 525 Data sampling timing (E□)
Data sampling timing (E1) (tim_ioe1x_en)	0013H	
Data sampling timing (E2) (tim_ioe2x_en)	001DH	
Data update timing (B0) (tim_iob0x_conv)	0009H	Page 526 Data update timing
Data update timing (B1) (tim_iob1x_conv)	0013H	
Data update timing (B2) (tim_iob2x_conv)	001DH	
Data update timing (E0) (tim_ioe0x_conv)	0009H	
Data update timing (E1) (tim_ioe1x_conv)	0013H	
Data update timing (E2) (tim_ioe2x_conv)	001DH	
Input filter upper limit value (IOB0_X0) (B0) (iport_iob0_0_filcnt_upper) to Input filter upper limit value (IOB0_XF) (B0) (iport_iob0_f_filcnt_upper)	0000H	Page 528 Input filter counter upper limit
Input filter upper limit value (IOB1_X0) (B1) (iport_iob1_0_filcnt_upper) to Input filter upper limit value (IOB1_XF) (B1) (iport_iob1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOB2_X0) (B2) (iport_iob2_0_filcnt_upper) to Input filter upper limit value (IOB2_XF) (B2) (iport_iob2_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE0_X0) (E0) (iport_ioe0_0_filcnt_upper) to Input filter upper limit value (IOE0_XF) (E0) (iport_ioe0_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE1_X0) (E1) (iport_ioe1_0_filcnt_upper) to Input filter upper limit value (IOE1_XF) (E1) (iport_ioe1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE2_X0) (E2) (iport_ioe2_0_filcnt_upper) to Input filter upper limit value (IOE2_XF) (E2) (iport_ioe2_f_filcnt_upper)	0000H	

3. Perform the preprocessing of internal operation start.

4. To check B0, set the register areas as shown in the table below.

When setting the register areas, set b0 of Internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Stop (0). When b0 is set to Stop (0), FPGA external reset (IOB0_RSTL, IOE_RSTL) becomes 0. When b0 is set to Start (1), FPGA external reset (IOB0_RSTL, IOE_RSTL) becomes 1. The writing data register is reflected by writing Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H).

Register name	Setting value	Reference
Output signal selection (B0) (oport_iob0y_osel)	FFFFH	Page 530 Output signal selection
Digital output control digital output selection (B0) (usr_wreg_078)	0000H	Page 576 Digital output control digital output selection

5. Input 1 for 0.5μs and then 0 for 0.5μs to Input signal monitor register (B0) (iport_iob0x_monitor) (FPGA register address: 1000_3100H).

Check that 0 is output from b0 (IOB0_Y0) of Output signal monitor (B0) (iport_iob0y_monitor) (FPGA register address: 1000_4020H).

6. Switch the register setting value as shown in the table below and perform step 5.

When the setting value is 0001H, check that the input value to IOB0_X0 is output from IOB0_Y0. When the setting value is 0003H, check that the inverted input value to IOB0_X0 is output from IOB0_Y0.

Register name	Setting value	Reference
Digital control part enable/disable control register (IOB0_X0 B0) (usr_wreg_000)	0000H→0001H→0003H	Page 573 Digital control part enable/disable control register

7. Read the checked terminal X0 as X1 to XF to perform steps 5 and 6. Use the following table instead in step 6.

Check that the values are output where each value is obtained by replacing Y0 in steps 5 and 6 with Y1 to YF.

Register name	Setting value	Reference
Digital control part enable/disable control register (IOB0_X1 B0) (usr_wreg_001)	0000H→0001H→0003H	Page 573 Digital control part enable/disable control register
Digital control part enable/disable control register (IOB0_X2 B0) (usr_wreg_002)		
Digital control part enable/disable control register (IOB0_X3 B0) (usr_wreg_003)		
Digital control part enable/disable control register (IOB0_X4 B0) (usr_wreg_004)		
Digital control part enable/disable control register (IOB0_X5 B0) (usr_wreg_005)		
Digital control part enable/disable control register (IOB0_X6 B0) (usr_wreg_006)		
Digital control part enable/disable control register (IOB0_X7 B0) (usr_wreg_007)		
Digital control part enable/disable control register (IOB0_X8 B0) (usr_wreg_008)		
Digital control part enable/disable control register (IOB0_X9 B0) (usr_wreg_009)		
Digital control part enable/disable control register (IOB0_XA B0) (usr_wreg_00A)		
Digital control part enable/disable control register (IOB0_XB B0) (usr_wreg_00B)		
Digital control part enable/disable control register (IOB0_XC B0) (usr_wreg_00C)		
Digital control part enable/disable control register (IOB0_XD B0) (usr_wreg_00D)		
Digital control part enable/disable control register (IOB0_XE B0) (usr_wreg_00E)		
Digital control part enable/disable control register (IOB0_XF B0) (usr_wreg_00F)		

8. Read B0 as B1, B2, and E0 to E2 and perform steps 4 to 7.

Check that the values are output where each value is obtained by replacing B0 in steps 5 to 7 with B1, B2, and E0 to E2.

Differential input/output check

■Validation pattern name

FNA_TOP_01010102

■Purpose

To perform inversion control and output control for the differential input of differential input/output circuit boards, and to check that it is output to the differential output of the differential input/output circuit boards

■Check item

Perform inversion control and output control for the differential input of differential input/output circuit boards, and check that it is output to the differential output of the differential input/output circuit boards. (Check the above for each of circuit boards B0, B1, B2, E0, E1, and E2)

■Procedure

Configuration: B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, without verification model connection of DDR3L SDRAM

1. Reset the sequence.

2. Set the register areas for B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards. Also, set the related register areas as shown in the table below.

Register name	Setting value	Reference
Filter sampling pulse (B0) (tim_iob0x_samp)	0000H	Page 523 Filter sampling pulse
Filter sampling pulse (B1) (tim_iob1x_samp)	0000H	
Filter sampling pulse (B2) (tim_iob2x_samp)	0000H	
Filter sampling pulse (E0) (tim_ioe0x_samp)	0000H	
Filter sampling pulse (E1) (tim_ioe1x_samp)	0000H	
Filter sampling pulse (E2) (tim_ioe2x_samp)	0000H	
Data update timing (B0) (tim_iob0x_conv)	0000H	Page 526 Data update timing
Data update timing (B1) (tim_iob1x_conv)	0000H	
Data update timing (B2) (tim_iob2x_conv)	0000H	
Data update timing (E0) (tim_ioe0x_conv)	0000H	
Data update timing (E1) (tim_ioe1x_conv)	0000H	
Data update timing (E2) (tim_ioe2x_conv)	0000H	
Input filter upper limit value (IOB0_X0) (B0) (iport_iob0_0_filcnt_upper) to Input filter upper limit value (IOB0_XF) (B0) (iport_iob0_f_filcnt_upper)	0000H	Page 528 Input filter counter upper limit
Input filter upper limit value (IOB1_X0) (B1) (iport_iob1_0_filcnt_upper) to Input filter upper limit value (IOB1_XF) (B1) (iport_iob1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOB2_X0) (B2) (iport_iob2_0_filcnt_upper) to Input filter upper limit value (IOB2_XF) (B2) (iport_iob2_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE0_X0) (E0) (iport_ioe0_0_filcnt_upper) to Input filter upper limit value (IOE0_XF) (E0) (iport_ioe0_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE1_X0) (E1) (iport_ioe1_0_filcnt_upper) to Input filter upper limit value (IOE1_XF) (E1) (iport_ioe1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE2_X0) (E2) (iport_ioe2_0_filcnt_upper) to Input filter upper limit value (IOE2_XF) (E2) (iport_ioe2_f_filcnt_upper)	0000H	

3. Perform the preprocessing of internal operation start.

4. To check B0, set the register areas as shown in the table below. Also set b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

Register name	Setting value	Reference
Output signal/Input output direction signal selection (B0) (ioport_iob0_dio485_osel)	0003H	Page 536 Select output signal or I/O direction signal
Digital input/output control digital output selection (usr_wreg_086)	003EH→001FH	Page 578 Digital I/O control digital output selection
Digital input/output control input/output control register (B0) (usr_wreg_080)	0000H→0001H→0003H→0005H	Page 577 Digital I/O control I/O control register

5. After starting the internal operation, input 1 for 0.5μs and then 0 for 0.5μs to IOB0_DIO485_I.

When the internal operation is set to Stop, IOB0-2_RSTL/IOE_RSTL becomes 0. When it is set to Start, IOB0-2_RSTL/IOE_RSTL becomes 1.

Check that 0 is output from IOB0_DIO485_O and IOB0_DIO485_EN.

6. Switch the setting value of the Digital input/output control input/output control register according to the table in step 4, and then perform step 5.

Check that the following values are output.

If the setting value is 0001H, check that the input value from IOB0_DIO485_O to IOB0_DIO485_I is output and 0 is output from IOB0_DIO485_EN. If the setting value is 0003H, check that the inverted input value from IOB0_DIO485_O to IOB0_DIO485_I is output and 0 is output from IOB0_DIO485_EN. If the setting value is 0005H, check that the input value from IOB0_DIO485_O to IOB0_DIO485_I is output and 1 is output from IOB0_DIO485_EN.

7. Read B0 as B1, B2, and E0 to E2 and perform steps 4 to 6.

Check that the values are output where each value is obtained by replacing B0 in steps 5 and 6 with B1, B2, and E0 to E2.

Pulse output check

■Validation pattern name

FNA_TOP_01010103

■Purpose

To check that the pulse output of the user circuit block is output to the differential output of differential input/output circuit boards

■Check item

Check the operation of the pulse output of the user circuit block. (Circuit boards B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)

■Procedure

Configuration: B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, without verification model connection of DDR3L SDRAM

1. Reset the sequence.
2. Set the register areas as shown in the table below.

Register name	Setting value	Reference
Data update timing (B0) (tim_iob0x_conv)	0000H	Page 526 Data update timing
Data update timing (B1) (tim_iob1x_conv)	0000H	
Data update timing (B2) (tim_iob2x_conv)	0000H	
Data update timing (E0) (tim_ioe0x_conv)	0000H	
Data update timing (E1) (tim_ioe1x_conv)	0000H	
Data update timing (E2) (tim_ioe2x_conv)	0000H	
Output signal selection (B0) (oport_iob0y_osel)	FFFFH	Page 530 Output signal selection
Output signal selection (B1) (oport_iob1y_osel)	FFFFH	
Output signal selection (B2) (oport_iob2y_osel)	FFFFH	
Output signal selection (E0) (oport_ioe0y_osel)	FFFFH	
Output signal selection (E1) (oport_ioe1y_osel)	FFFFH	
Output signal selection (E2) (oport_ioe2y_osel)	FFFFH	
Output signal/Input output direction signal selection (B0) (ioport_iob0_dio485_osel)	0003H	Page 536 Select output signal or I/O direction signal
Output signal/Input output direction signal selection (B1) (ioport_iob1_dio485_osel)	0003H	
Output signal/Input output direction signal selection (B2) (ioport_iob2_dio485_osel)	0003H	
Output signal/Input output direction signal selection (E0) (ioport_ioe0_dio485_osel)	0003H	
Output signal/Input output direction signal selection (E1) (ioport_ioe1_dio485_osel)	0003H	
Output signal/Input output direction signal selection (E2) (ioport_ioe2_dio485_osel)	0003H	
Digital output control digital output selection (B0) (usr_wreg_078)	FFFFH	Page 576 Digital output control digital output selection
Digital output control digital output selection (B1) (usr_wreg_079)	FFFFH	
Digital output control digital output selection (B2) (usr_wreg_07A)	FFFFH	
Digital output control digital output selection (E0) (usr_wreg_07B)	FFFFH	
Digital output control digital output selection (E1) (usr_wreg_07C)	FFFFH	
Digital output control digital output selection (E2) (usr_wreg_07D)	FFFFH	
Digital input/output control digital output selection (usr_wreg_086)	003FH	Page 578 Digital I/O control digital output selection

Register name	Setting value	Reference
Pulse output part pulse width upper limit value (lower side) (B0) (usr_wreg_110)	0003H	Page 587 Pulse output part pulse width upper limit value
Pulse output part pulse width upper limit value (upper side) (B0) (usr_wreg_111)	0000H	
Pulse output part pulse width upper limit value (lower side) (B1) (usr_wreg_115)	0003H	
Pulse output part pulse width upper limit value (upper side) (B1) (usr_wreg_116)	0000H	
Pulse output part pulse width upper limit value (lower side) (B2) (usr_wreg_11A)	0003H	
Pulse output part pulse width upper limit value (upper side) (B2) (usr_wreg_11B)	0000H	
Pulse output part pulse width upper limit value (lower side) (E0) (usr_wreg_11F)	0003H	
Pulse output part pulse width upper limit value (upper side) (E0) (usr_wreg_120)	0000H	
Pulse output part pulse width upper limit value (lower side) (E1) (usr_wreg_124)	0003H	
Pulse output part pulse width upper limit value (upper side) (E1) (usr_wreg_125)	0000H	
Pulse output part pulse width upper limit value (lower side) (E2) (usr_wreg_129)	0003H	
Pulse output part pulse width upper limit value (upper side) (E2) (usr_wreg_12A)	0000H	
Pulse output part output pulse count upper limit value (lower side) (B0) (usr_wreg_112)	0064H	Page 588 Pulse output part output pulse count upper limit value
Pulse output part output pulse count upper limit value (upper side) (B0) (usr_wreg_113)	0000H	
Pulse output part output pulse count upper limit value (lower side) (B1) (usr_wreg_117)	0064H	
Pulse output part output pulse count upper limit value (upper side) (B1) (usr_wreg_118)	0000H	
Pulse output part output pulse count upper limit value (lower side) (B2) (usr_wreg_11C)	0064H	
Pulse output part output pulse count upper limit value (upper side) (B2) (usr_wreg_11D)	0000H	
Pulse output part output pulse count upper limit value (lower side) (E0) (usr_wreg_121)	0064H	
Pulse output part output pulse count upper limit value (upper side) (E0) (usr_wreg_122)	0000H	
Pulse output part output pulse count upper limit value (lower side) (E1) (usr_wreg_126)	0064H	
Pulse output part output pulse count upper limit value (upper side) (E1) (usr_wreg_127)	0000H	
Pulse output part output pulse count upper limit value (lower side) (E2) (usr_wreg_12B)	0064H	
Pulse output part output pulse count upper limit value (upper side) (E2) (usr_wreg_12C)	0000H	
Pulse output part pulse output enable (B0) (usr_wreg_1B8)	0001H	Page 597 Pulse output part pulse output enable
Pulse output part pulse output enable (B1) (usr_wreg_1B9)	0001H	
Pulse output part pulse output enable (B2) (usr_wreg_1BA)	0001H	
Pulse output part pulse output enable (E0) (usr_wreg_1BB)	0001H	
Pulse output part pulse output enable (E1) (usr_wreg_1BC)	0001H	
Pulse output part pulse output enable (E2) (usr_wreg_1BD)	0001H	
Pulse output part pulse output selection 0 (B0) (usr_wreg_130)	E4E4H	Page 589 Pulse output part pulse output selection
Pulse output part pulse output selection 1 (B0) (usr_wreg_131)	E4E4H	
Pulse output part pulse output selection 2 (B0) (usr_wreg_132)	0000H	
Pulse output part pulse output selection 0 (B1) (usr_wreg_133)	E4E4H	
Pulse output part pulse output selection 1 (B1) (usr_wreg_134)	E4E4H	
Pulse output part pulse output selection 2 (B1) (usr_wreg_135)	0000H	
Pulse output part pulse output selection 0 (B2) (usr_wreg_136)	E4E4H	
Pulse output part pulse output selection 1 (B2) (usr_wreg_137)	E4E4H	
Pulse output part pulse output selection 2 (B2) (usr_wreg_138)	0000H	
Pulse output part pulse output selection 0 (E0) (usr_wreg_139)	E4E4H	
Pulse output part pulse output selection 1 (E0) (usr_wreg_13A)	E4E4H	
Pulse output part pulse output selection 2 (E0) (usr_wreg_13B)	0000H	
Pulse output part pulse output selection 0 (E1) (usr_wreg_13C)	E4E4H	
Pulse output part pulse output selection 1 (E1) (usr_wreg_13D)	E4E4H	
Pulse output part pulse output selection 2 (E1) (usr_wreg_13E)	0000H	
Pulse output part pulse output selection 0 (E2) (usr_wreg_13F)	E4E4H	
Pulse output part pulse output selection 1 (E2) (usr_wreg_140)	E4E4H	
Pulse output part pulse output selection 2 (E2) (usr_wreg_141)	0000H	

Register name	Setting value	Reference
Pulse output part pulse output mask 0 (B0) (usr_wreg_142)	FFFFH	Page 590 Pulse output part pulse output mask
Pulse output part pulse output mask 1 (B0) (usr_wreg_143)	0001H	
Pulse output part pulse output mask 0 (B1) (usr_wreg_144)	FFFFH	
Pulse output part pulse output mask 1 (B1) (usr_wreg_145)	0001H	
Pulse output part pulse output mask 0 (B2) (usr_wreg_146)	FFFFH	
Pulse output part pulse output mask 1 (B2) (usr_wreg_147)	0001H	
Pulse output part pulse output mask 0 (E0) (usr_wreg_148)	FFFFH	
Pulse output part pulse output mask 1 (E0) (usr_wreg_149)	0001H	
Pulse output part pulse output mask 0 (E1) (usr_wreg_14A)	FFFFH	
Pulse output part pulse output mask 1 (E1) (usr_wreg_14B)	0001H	
Pulse output part pulse output mask 0 (E2) (usr_wreg_14C)	FFFFH	
Pulse output part pulse output mask 1 (E2) (usr_wreg_14D)	0001H	

3. Set b1 and b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

4. After the preprocessing of the internal operation start, start the internal operation.

5. Check that 100 pulses with the width of 0.04μs are output from IOB0_Y0 and IOB0_DIO485_O. Also, check that the phases between the channels are shifted by 90 degrees.

6. Read Y0 as Y1 to Y7 and perform step 5.

Check that the values are output where each value is obtained by replacing Y0 in step 5 with Y1 to Y7.

7. Read B0 as B1, B2, and E0 to E2, and perform steps 5 and 6.

Check that the values are output where each value is obtained by replacing B0 in steps 5 and 6 with B1, B2, and E0 to E2.

Counter operation check

■Validation pattern name

FNA_TOP_01010104

■Purpose

To check that 32-bit ring counters (2-phase multiple of 4)/32-bit ring counters (1-phase multiple of 1) implemented in the user circuit block count against differential inputs from differential input/output circuit boards

■Check item

Check the operation of 32-bit ring counters (2-phase multiple of 4)/32-bit ring counters (1-phase multiple of 1) in the user circuit block. (Circuit boards B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)

■Procedure

Configuration: B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, without verification model connection of DDR3L SDRAM

1. Reset the sequence.
2. Set the register areas as shown in the table below.

Register name	Setting value	Reference
Filter sampling pulse (B0) (tim_iob0x_samp)	0000H	Page 523 Filter sampling pulse
Filter sampling pulse (B1) (tim_iob1x_samp)	0000H	
Filter sampling pulse (B2) (tim_iob2x_samp)	0000H	
Filter sampling pulse (E0) (tim_ioe0x_samp)	0000H	
Filter sampling pulse (E1) (tim_ioe1x_samp)	0000H	
Filter sampling pulse (E2) (tim_ioe2x_samp)	0000H	
Data sampling timing (B0) (tim_iob0x_en)	0000H	Page 524 Data sampling timing (B□)
Data sampling timing (B1) (tim_iob1x_en)	0000H	
Data sampling timing (B2) (tim_iob2x_en)	0000H	
Data sampling timing (E0) (tim_ioe0x_en)	0000H	Page 525 Data sampling timing (E□)
Data sampling timing (E1) (tim_ioe1x_en)	0000H	
Data sampling timing (E2) (tim_ioe2x_en)	0000H	
Input filter upper limit value (IOB0_X0) (B0) (iport_iob0_0_filcnt_upper) to Input filter upper limit value (IOB0_X7) (B0) (iport_iob0_7_filcnt_upper)	0000H	Page 528 Input filter counter upper limit
Input filter upper limit value (IOB1_X0) (B1) (iport_iob1_0_filcnt_upper) to Input filter upper limit value (IOB1_X7) (B1) (iport_iob1_7_filcnt_upper)	0000H	
Input filter upper limit value (IOB2_X0) (B2) (iport_iob2_0_filcnt_upper) to Input filter upper limit value (IOB2_X7) (B2) (iport_iob2_7_filcnt_upper)	0000H	
Input filter upper limit value (IOE0_X0) (E0) (iport_ioe0_0_filcnt_upper) to Input filter upper limit value (IOE0_X7) (E0) (iport_ioe0_7_filcnt_upper)	0000H	
Input filter upper limit value (IOE1_X0) (E1) (iport_ioe1_0_filcnt_upper) to Input filter upper limit value (IOE1_X7) (E1) (iport_ioe1_7_filcnt_upper)	0000H	
Input filter upper limit value (IOE2_X0) (E2) (iport_ioe2_0_filcnt_upper) to Input filter upper limit value (IOE2_X7) (E2) (iport_ioe2_7_filcnt_upper)	0000H	
Input filter upper limit value (IOB0_DIO485_I) (B0) (iport_iob0_dio485_filcnt_upper)	0000H	Page 534 Input filter counter upper limit
Input filter upper limit value (IOB1_DIO485_I) (B1) (iport_iob1_dio485_filcnt_upper)	0000H	
Input filter upper limit value (IOB2_DIO485_I) (B2) (iport_iob2_dio485_filcnt_upper)	0000H	
Input filter upper limit value (IOE0_DIO485_I) (E0) (iport_ioe0_dio485_filcnt_upper)	0000H	
Input filter upper limit value (IOE1_DIO485_I) (E1) (iport_ioe1_dio485_filcnt_upper)	0000H	
Input filter upper limit value (IOE2_DIO485_I) (E2) (iport_ioe2_dio485_filcnt_upper)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B0) (usr_wreg_188)	0000H	Page 593 Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B1) (usr_wreg_18B)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B2) (usr_wreg_18E)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E0) (usr_wreg_191)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E1) (usr_wreg_194)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E2) (usr_wreg_197)	0000H	

Register name	Setting value	Reference
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0) (usr_wreg_189)	0000H	Page 594 Counter control part 32-bit ring counter (2-phase multiple of 4) preset data
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0) (usr_wreg_18A)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B1) (usr_wreg_18C)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B1) (usr_wreg_18D)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B2) (usr_wreg_18F)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B2) (usr_wreg_190)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E0) (usr_wreg_192)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E0) (usr_wreg_193)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E1) (usr_wreg_195)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E1) (usr_wreg_196)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E2) (usr_wreg_198)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E2) (usr_wreg_199)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0) (usr_wreg_0A3)	0064H	Page 583 Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0) (usr_wreg_0A4)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B1) (usr_wreg_0AB)	0064H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B1) (usr_wreg_0AC)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B2) (usr_wreg_0B3)	0064H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B2) (usr_wreg_0B4)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E0) (usr_wreg_0BB)	0064H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E0) (usr_wreg_0BC)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E1) (usr_wreg_0C3)	0064H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E1) (usr_wreg_0C4)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E2) (usr_wreg_0CB)	0064H	
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E2) (usr_wreg_0CC)	0000H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	0201H	Page 584 Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) (usr_wreg_0AD)	0201H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) (usr_wreg_0B5)	0201H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) (usr_wreg_0BD)	0201H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) (usr_wreg_0C5)	0201H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) (usr_wreg_0CD)	0201H	

Register name	Setting value	Reference
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B0) (usr_wreg_1A0)	0001H	Page 595 Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B1) (usr_wreg_1A3)	0001H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B2) (usr_wreg_1A6)	0001H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E0) (usr_wreg_1A9)	0001H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E1) (usr_wreg_1AC)	0001H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E2) (usr_wreg_1AF)	0001H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B0) (usr_wreg_1A1)	0032H	Page 596 Counter control part 32-bit ring counter (1-phase multiple of 1) preset data
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B0) (usr_wreg_1A2)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B1) (usr_wreg_1A4)	0032H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B1) (usr_wreg_1A5)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B2) (usr_wreg_1A7)	0032H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B2) (usr_wreg_1A8)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E0) (usr_wreg_1AA)	0032H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E0) (usr_wreg_1AB)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E1) (usr_wreg_1AD)	0032H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E1) (usr_wreg_1AE)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E2) (usr_wreg_1B0)	0032H	
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E2) (usr_wreg_1B1)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B0) (usr_wreg_0D3)	0064H	Page 585 Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B0) (usr_wreg_0D4)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B1) (usr_wreg_0DB)	0064H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B1) (usr_wreg_0DC)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B2) (usr_wreg_0E3)	0064H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B2) (usr_wreg_0E4)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E0) (usr_wreg_0EB)	0064H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E0) (usr_wreg_0EC)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E1) (usr_wreg_0F3)	0064H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E1) (usr_wreg_0F4)	0000H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E2) (usr_wreg_0FB)	0064H	
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E2) (usr_wreg_0FC)	0000H	

Register name	Setting value	Reference
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) (usr_wreg_0D5)	0403H	Page 586 Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) (usr_wreg_0DD)	0403H	
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) (usr_wreg_0E5)	0403H	
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) (usr_wreg_0ED)	0403H	
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) (usr_wreg_0F5)	0403H	
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) (usr_wreg_0FD)	0403H	

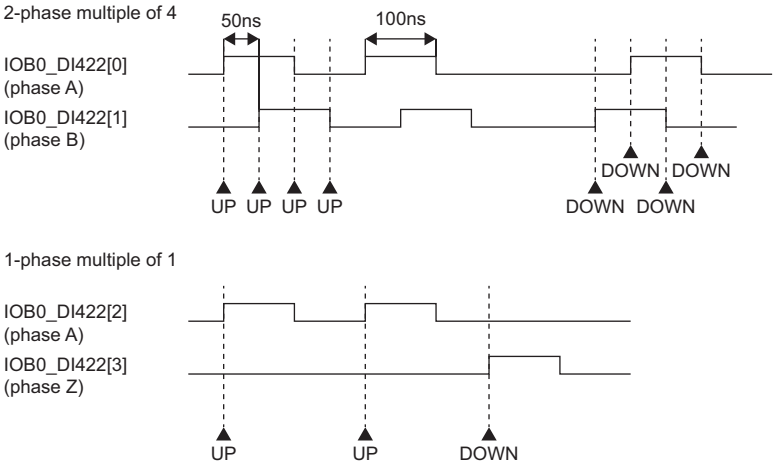
3. Set b1 and b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register: 1000_A000H) to 3.

4. After the preprocessing of the internal operation start, start the internal operation.

5. Set Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B0) (usr_wreg_1A0) (FPGA register address: 1000_B340H) to Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E2) (usr_wreg_1AF) (FPGA register address: 1000_B35EH) to 0 for all circuit boards.

6. Set b1 of Write/read data control register (usr_wrdat_ctrl) (FPGA register: 1000_A000H) to 1.

7. Input IO[B|E][0-2]_DI422_I[3:0] 24 times according to UPs in the figure below.



8. Set b9 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

9. Read Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B0) (usr_rreg_1B3) (FPGA register address: 1000_BB66H) to Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E2) (usr_rreg_1BE) (FPGA register address: 1000_BB7CH) and Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B0) (usr_rreg_1BF) (FPGA register address: 1000_BB7EH) and Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E2) (usr_rreg_1CA) (FPGA register address: 1000_BB94H). Check that the counter value corresponds to 96 for 2-phase multiple of 4 and 24 (+ preset) for 1-phase multiple of 1.

10. Input IO[B|E][0-2]_DI422_I[3:0] 23 times according to DOWNs in the figure shown in step 7.

11. Set b9 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

12. Read Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B0) (usr_rreg_1B3) (FPGA register address: 1000_BB66H) to Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E2) (usr_rreg_1BE) (FPGA register address: 1000_BB7CH) and Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B0) (usr_rreg_1BF) (FPGA register address: 1000_BB7EH) and Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E2) (usr_rreg_1CA) (FPGA register address: 1000_BB94H). Check that the counter value (corresponds to 4 for 2-phase multiple of 4 and 1 (+ preset) for 1-phase multiple of 1.

Logging (non-time division mode) check

■Validation pattern name

FNA_TOP_01010105

■Purpose

To check that the differential input of differential input/output circuit boards is logged to DDR3L SDRAM

■Check item

Perform logging for the differential input of differential input/output circuit boards and 32-bit ring counters (2-phase multiple of 4), and check that data is logged to DDR3L SDRAM. Logging is performed in trigger operation mode. (Circuit boards B0, B1, B2, E0, E1, and E2 connect to differential input/output circuit boards.)

■Procedure

Configuration: B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, with verification model connection of DDR3L SDRAM

1. Reset the sequence.
2. Set the register areas for B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, and the related register areas as shown in the table below. Set b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register: 1000_A000H) to 1.

Register name	Setting value	Reference
Logging operation control register (lgdw_ctrl)	1100H	Page 550 Logging operation control register
Logging data size setting (lgdw_area)	0001H	Page 553 Logging data size setting
Set number of sampling after trigger (lower side) (lgdw_triggered_lsample)	0080H	Page 555 Set number of sampling after trigger
Set number of sampling after trigger (upper side) (lgdw_triggered_usample)	0000H	
Filter sampling pulse (B0) (tim_iob0x_samp)	0000H	Page 523 Filter sampling pulse
Filter sampling pulse (B1) (tim_iob1x_samp)		
Filter sampling pulse (B2) (tim_iob2x_samp)		
Filter sampling pulse (E0) (tim_ioe0x_samp)		
Filter sampling pulse (E1) (tim_ioe1x_samp)		
Filter sampling pulse (E2) (tim_ioe2x_samp)		
Input filter upper limit value (IOB0_X0) (B0) (iport_iob0_0_filcnt_upper) to Input filter upper limit value (IOB0_X7) (B0) (iport_iob0_7_filcnt_upper)	0000H	Page 528 Input filter counter upper limit
Input filter upper limit value (IOB1_X0) (B1) (iport_iob1_0_filcnt_upper) to Input filter upper limit value (IOB1_X7) (B1) (iport_iob1_7_filcnt_upper)		
Input filter upper limit value (IOB2_X0) (B2) (iport_iob2_0_filcnt_upper) to Input filter upper limit value (IOB2_X7) (B2) (iport_iob2_7_filcnt_upper)		
Input filter upper limit value (IOE0_X0) (E0) (iport_ioe0_0_filcnt_upper) to Input filter upper limit value (IOE0_X7) (E0) (iport_ioe0_7_filcnt_upper)		
Input filter upper limit value (IOE1_X0) (E1) (iport_ioe1_0_filcnt_upper) to Input filter upper limit value (IOE1_X7) (E1) (iport_ioe1_7_filcnt_upper)		
Input filter upper limit value (IOE2_X0) (E2) (iport_ioe2_0_filcnt_upper) to Input filter upper limit value (IOE2_X7) (E2) (iport_ioe2_7_filcnt_upper)		
Logging cycle timing (tim_log_cyc)	0000H	Page 527 Logging cycle timing
User circuit logging mode selection (usr_logmode_sel)	0000H	Page 565 User circuit logging mode selection
Logging control part end trigger signal selection (usr_wreg_092)	0015H	Page 580 Logging control part end trigger signal selection
Logging control part logging enable mode setting (usr_wreg_094)	0000H	Page 582 Logging control part logging enable mode setting

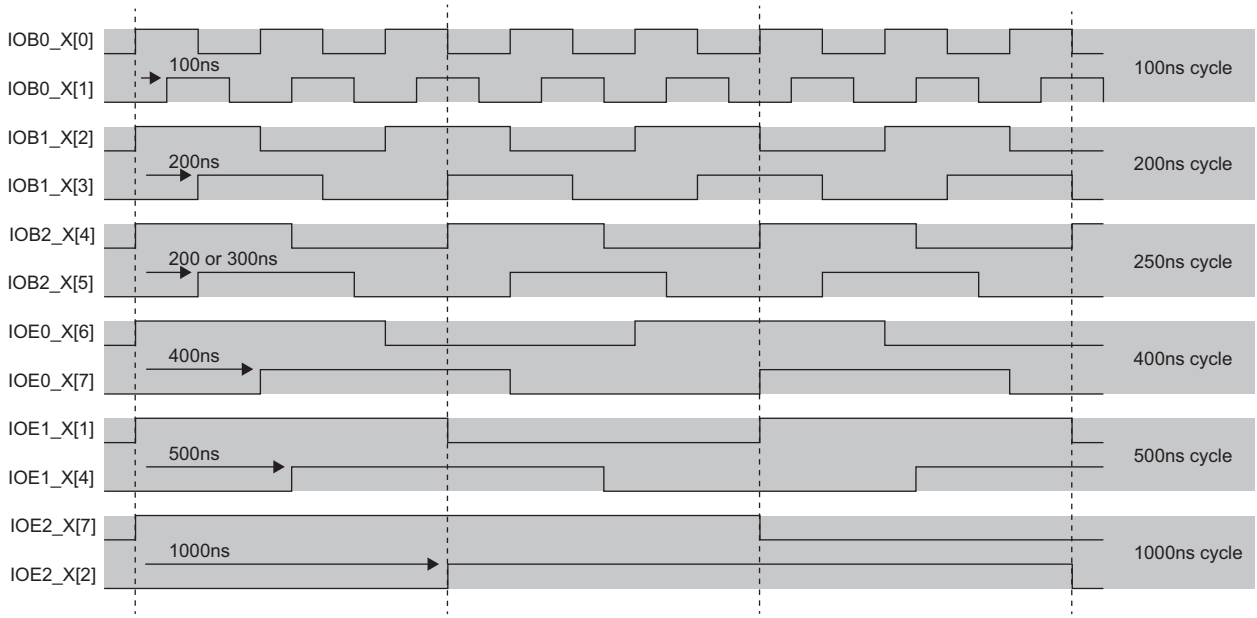
Register name	Setting value	Reference
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	0201H	Page 584 Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) (usr_wreg_0AD)	0403H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) (usr_wreg_0B5)	0605H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) (usr_wreg_0BD)	0807H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) (usr_wreg_0C5)	0502H	
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) (usr_wreg_0CD)	0308H	

3. After the preprocessing of the internal operation start, start the internal operation.

When the internal operation is set to Stop, IOB0-2_RSTL/IOE_RSTL becomes 0. When it is set to Start, IOB0-2_RSTL/IOE_RSTL becomes 1. Also, exp_IO[B|E][0-2]_Y[0-7] and exp_IO[B|E][0-2]_YCK1 become to 0.

4. Set b0 of Logging operation control register (lgdw_ctrl) (FPGA register: 1000_9000H) to 1, and start write logging. Input differential signals while logging. Refer to the table and chart below for input values.

Terminal name	Setting value	Terminal name	Setting value
IOB0_X[0]	Refer to the following chart.	IOE0_X[0]	0000H
IOB0_X[1]	Refer to the following chart.	IOE0_X[1]	0000H
IOB0_X[2]	0000H	IOE0_X[2]	0000H
IOB0_X[3]	0000H	IOE0_X[3]	0000H
IOB0_X[4]	0000H	IOE0_X[4]	0000H
IOB0_X[5]	0000H	IOE0_X[5]	0000H
IOB0_X[6]	0000H	IOE0_X[6]	Refer to the following chart.
IOB0_X[7]	0000H	IOE0_X[7]	Refer to the following chart.
IOB1_X[0]	0000H	IOE1_X[0]	0000H
IOB1_X[1]	0000H	IOE1_X[1]	Refer to the following chart.
IOB1_X[2]	Refer to the following chart.	IOE1_X[2]	0000H
IOB1_X[3]	Refer to the following chart.	IOE1_X[3]	0000H
IOB1_X[4]	0000H	IOE1_X[4]	Refer to the following chart.
IOB1_X[5]	0000H	IOE1_X[5]	0000H
IOB1_X[6]	0000H	IOE1_X[6]	0000H
IOB1_X[7]	0000H	IOE1_X[7]	0000H
IOB2_X[0]	0000H	IOE2_X[0]	0000H
IOB2_X[1]	0000H	IOE2_X[1]	0000H
IOB2_X[2]	0000H	IOE2_X[2]	Refer to the following chart.
IOB2_X[3]	0000H	IOE2_X[3]	0000H
IOB2_X[4]	Refer to the following chart.	IOE2_X[4]	0000H
IOB2_X[5]	Refer to the following chart.	IOE2_X[5]	0000H
IOB2_X[6]	0000H	IOE2_X[6]	0000H
IOB2_X[7]	0000H	IOE2_X[7]	Refer to the following chart.



5. After 4μs has elapsed, set b1 of Logging control part user logging control (usr_wreg_180) (FPGA register address: 1000_B300H) to 1, and b1 of Write/read data control register (usr_wrdat_ctrl) (FGA register address: 1000_A000H) to 1, and input the end trigger.

B1 of Logging control part user logging control (usr_wreg_180) (FPGA register address: 1000_B300H) has a rising edge detection circuit, so b1 must be set to 0 after set to 1.

6. Wait for 128μs.

After waiting, check that CPU_INTPL[2] is asserted.

7. Read the register areas shown in the table below.

Check that the expected values shown in the table below are read for the register areas.

Register name	Expected value	Reference
Logging state register (lgdw_sts)	0500H	Page 551 Logging state register
Logging system flag (lgdw_sys_sts)	0004H	Page 552 Logging system flag
Number of samplings (lower side) (lgdw_sample_lcount)	0084H	Page 556 Number of samplings
Number of samplings (upper side) (lgdw_sample_ucount)	0000H	

8. Read the logging data shown in the table below from the microcomputer.

Check that data according to logging data bit assignment is read by the number of times of 64 bytes × (4+128). For details, refer to the following.

☞ Page 714 Logging Data Bit Assignment

Area	CS	Address		Remarks
		b29, b28	b27-b0	
DDR (1) area (1)	CS1	0000H	000_0000H	—
DDR (1) area (1)	CS1	0000H	000_7FFFH	32KB

Analog output check

■Validation pattern name

FNA_TOP_01010106

■Purpose

To check that analog outputs (analog data, enable, LDAC) are performed according to the register settings of the user circuit block

■Check item

Check that analog outputs (analog data, enable, LDAC) are performed according to the register settings of the user circuit block. (B0, B1, and B2 do not connect, while E0, E1, and E2 connect to analog input/output circuit boards.)

■Procedure

Use a configuration in which B0 to B2 do not connect and E0 to E2 connect to analog input/output circuit boards, with no DDR3L SDRAM verification model connected.

1. Reset the sequence.
2. Set the register areas for E0 to E2 analog input/output circuit boards, and set the related register areas as shown in the table below.

Register name	Setting value	Reference
Data update timing (E0) (tim_ioe0x_conv)	FFFFH	Page 526 Data update timing
Data update timing (E1) (tim_ioe1x_conv)	FFFFH	
Data update timing (E2) (tim_ioe2x_conv)	FFFFH	

3. After the preprocessing of the internal operation start, start the internal operation.
4. Set D/A conversion enable/disable setting (aoport_da_start) (FPGA register address: 1000_7000H) to 003FH so that conversion is enabled for all channels on all circuit boards.
5. To check CH0 of E0, set the register areas as shown in the table below. Also set b1 and b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

Register name	Setting value	Reference
Select D/A conversion value (aoport_da_data_sel)	0001H to 0020H	Page 546 D/A conversion value selection
Select D/A conversion timing (aoport_da_cyc_sel)	0001H, 0002H, 0004H	Page 547 D/A conversion timing selection
Analog output part D/A conversion value CH0 (E0) (usr_wreg_1C0)	Any	Page 597 Analog output part D/A conversion value
DAC LDAC signal selection (aoport_da_ldac_sel)	0001H to 0020H	Page 548 DAC LDAC signal selection
Analog output part LDAC output selection (usr_wreg_160)	0017H, 001DH, 0035H	Page 591 Analog output part LDAC output selection

6. Set b0 of Analog output part D/A conversion value enable (usr_wreg_1C6) (FPGA register address: 1000_B38CH) to 1, and b1 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1. After writing, start analog output.

b0 of Analog output part D/A conversion value enable (usr_wreg_1C6) (FPGA register address: 1000_B38CH) has a rising edge detection circuit, so b0 must be set to 0 after set to 1.

Check that data set to Analog output part D/A conversion value CH0 (E0) (usr_wreg_1C0) (FPGA register address: 1000_B380H) is output as the analog output of E0 CH0 and that the output of CH1 is all 0s. Also, check that the E0 LDAC output is 11 while E0 CH0 is being output.

7. Perform steps 5 and 6 for E0 CH1.

Check that the values are output where each value is obtained by swapping CH0 and CH1 in step 6.

8. Read E0 as E1 and E2 and perform steps 5 to 7.

Check that the values are output where each value is obtained by replacing E0 in steps 6 and 7 with E1 and E2.

Analog input and logging (time division mode) check

■Validation pattern name

FNA_TOP_01010107

■Purpose

To check that the analog input of analog input/output circuit boards is logged to DDR3L SDRAM

■Check item

Check that the analog input of analog input/output circuit boards is logged to DDR3L SDRAM in a time division manner. Logging is performed in trigger operation mode. (B0, B1, and B2 do not connect, while E0, E1, and E2 connect to analog input/output circuit boards.)

■Procedure

Use a configuration in which B0 to B2 do not connect and E0 to E2 connect to analog input/output circuit boards, with the DDR3L SDRAM verification model connected.

1. Reset the sequence.

2. Set the register areas for E0 to E2 analog input/output circuit boards, and set the related register areas as shown in the table below. After register setting, set b1 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

Register name	Setting value	Reference
Logging operation control register (lgdw_ctrl)	3100H	Page 550 Logging operation control register
Logging data size setting (lgdw_area)	0002H	Page 553 Logging data size setting
Set number of sampling after trigger (lower side) (lgdw_triggered_lsample)	0080H	Page 555 Set number of sampling after trigger
Set number of sampling after trigger (upper side) (lgdw_triggered_usample)	0000H	
Logging cycle timing (tim_log_cyc)	0003H	Page 527 Logging cycle timing
Data sampling timing (E0) (tim_ioe0x_en)	018FH	Page 525 Data sampling timing (E□)
Data sampling timing (E1) (tim_ioe1x_en)	031FH	
Data sampling timing (E2) (tim_ioe2x_en)	04AFH	
Select A/D conversion timing (aiport_ad_cyc_sel)	0000H	Page 540 A/D conversion timing selection
User circuit logging mode selection (usr_logmode_sel)	0001H	Page 558 User circuit logging mode selection
Logging control part end trigger signal selection (usr_wreg_092)	0015H	Page 580 Logging control part end trigger signal selection
Logging control part sampling pulse signal selection (usr_wreg_093)	0015H	Page 581 Logging control part sampling pulse signal selection

3. After the preprocessing of the internal operation start, start the internal operation.

When the internal operation is set to Stop, IOB0-2_RSTL/IOE_RSTL becomes 0. When the internal operation is set to Start, IOB0-2_RSTL/IOE_RSTL becomes 1.

4. Set E0, E1, and E2 to change from Conversion-disable to Conversion-enable.

Check that E0, E1, and E2 ADCs are initialized when the settings are changed.

5. After ADC initialization processing is completed, set b0 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 1, and start logging.

Input any value from the ADC during logging.

6. After 8μs has elapsed, set b1 of Logging control part user logging control (usr_wreg_180) (FPGA register address: 1000_B300H) to 1, and b1 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1, and input the end trigger.

B1 of Logging control part user logging control (usr_wreg_180) (FPGA register address: 1000_B300H) has a rising edge detection circuit, so b1 must be set to 0 after set to 1.

7. After 8μs has elapsed, read the register areas shown in the table below.

Check that the expected values shown in the table below are read for the register areas.

Register name	Expected value	
	Value	Reference
Logging state register (lgdw_sts)	0410H	Page 551 Logging state register
Logging system flag (lgdw_sys_sts)	0004H	Page 552 Logging system flag
Number of samplings (lower side) (lgdw_sample_lcount)	0006H	Page 556 Number of samplings
Number of samplings (upper side) (lgdw_sample_ucount)	0000H	

8. Wait for 256μs.

After waiting, check that CPU_INTPL[2] is asserted.

9. Read the register areas shown in the table below.

Check that the expected values shown in the table below are read for the register areas.

Register name	Expected value	
	Value	Reference
Logging state register (lgdw_sts)	0500H	Page 551 Logging state register
Logging system flag (lgdw_sys_sts)	0004H	Page 552 Logging system flag
Number of samplings (lower side) (lgdw_sample_lcount)	0082H	Page 556 Number of samplings
Number of samplings (upper side) (lgdw_sample_ucount)	0000H	

10. Read the logging data shown in the table below from the microcomputer.

Check that data according to logging data bit assignment is read by the number of times of 64 bytes × (2+128). For details, refer to the following.

☞ Page 714 Logging Data Bit Assignment

Area	CS	Address		Remarks
		b29, b28	b27 to b0	
DDR (1) area (1)	CS1	0000H	000_0000H	—
DDR (1) area (1)	CS1	0000H	000_FFFFH	64KB

Logging (automatic transfer mode) check

■Validation pattern name

FNA_TOP_01010108

■Purpose

To check that logging can be performed normally when b0 of Logging control part automatic transfer mode setting (usr_wreg_095) (FPGA register address: 1000_B12AH) is set to Enable (1)

■Check item

Check that, when b0 of Logging control part automatic transfer mode setting (usr_wreg_095) (FPGA register address: 1000_B12AH) is set to Enable (1), the logging enable signal (logging start) is output according to the logging control trigger and that data is written to DDR3L SDRAM normally.

■Procedure

Use a configuration in which B0 to B2 connect to differential input/output circuit boards and E0 to E2 connect to differential input/output circuit boards, with the DDR3L SDRAM verification model connected.

1. Reset the sequence.
2. Set the register areas for B0 to B2 differential input/output circuit boards and E0 to E2 differential input/output circuit boards, and the related register areas as shown in the table below. After setting, set b1 and b0 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) to 1.

Register name	Setting value	Reference
Filter sampling pulse (B0) (tim_iob0x_samp)	0000H	Page 523 Filter sampling pulse
Filter sampling pulse (B1) (tim_iob1x_samp)	0000H	
Filter sampling pulse (B2) (tim_iob2x_samp)	0000H	
Filter sampling pulse (E0) (tim_ioe0x_samp)	0000H	
Filter sampling pulse (E1) (tim_ioe1x_samp)	0000H	
Filter sampling pulse (E2) (tim_ioe2x_samp)	0000H	
Data sampling timing (B0) (tim_iob0x_en)	0000H	Page 524 Data sampling timing (B□)
Data sampling timing (B1) (tim_iob1x_en)	0000H	
Data sampling timing (B2) (tim_iob2x_en)	0000H	
Data sampling timing (E0) (tim_ioe0x_en)	0000H	Page 525 Data sampling timing (E□)
Data sampling timing (E1) (tim_ioe1x_en)	0000H	
Data sampling timing (E2) (tim_ioe2x_en)	0000H	
Data update timing (B0) (tim_iob0x_conv)	0000H	Page 526 Data update timing
Data update timing (B1) (tim_iob1x_conv)	0000H	
Data update timing (B2) (tim_iob2x_conv)	0000H	
Data update timing (E0) (tim_ioe0x_conv)	0000H	
Data update timing (E1) (tim_ioe1x_conv)	0000H	
Data update timing (E2) (tim_ioe2x_conv)	0000H	
Input filter upper limit value (IOB0_X0) (B0) (iport_iob0_0_filcnt_upper) to Input filter upper limit value (IOB0_XF) (B0) (iport_iob0_f_filcnt_upper)	0000H	Page 528 Input filter counter upper limit
Input filter upper limit value (IOB1_X0) (B1) (iport_iob1_0_filcnt_upper) to Input filter upper limit value (IOB1_XF) (B1) (iport_iob1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOB2_X0) (B2) (iport_iob2_0_filcnt_upper) to Input filter upper limit value (IOB2_XF) (B2) (iport_iob2_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE0_X0) (E0) (iport_ioe0_0_filcnt_upper) to Input filter upper limit value (IOE0_XF) (E0) (iport_ioe0_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE1_X0) (E1) (iport_ioe1_0_filcnt_upper) to Input filter upper limit value (IOE1_XF) (E1) (iport_ioe1_f_filcnt_upper)	0000H	
Input filter upper limit value (IOE2_X0) (E2) (iport_ioe2_0_filcnt_upper) to Input filter upper limit value (IOE2_XF) (E2) (iport_ioe2_f_filcnt_upper)	0000H	
Logging operation control register (lgdw_ctrl)	2400H	Page 550 Logging operation control register
Logging data size setting (lgdw_area)	0000H	Page 553 Logging data size setting
Logging control part logging enable signal selection (usr_wreg_091)	0001H	Page 579 Logging control part logging enable signal selection

Register name	Setting value	Reference
Logging control part sampling pulse signal selection (usr_wreg_093)	0002H	Page 581 Logging control part sampling pulse signal selection
Logging control part automatic transfer mode setting (usr_wreg_095)	0001H	Page 582 Logging control part automatic transfer mode setting

3. After the preprocessing of the internal operation start, start the internal operation.

When the internal operation is set to Stop, IOB0-2_RSTL/IOE_RSTL becomes 0. When the internal operation is set to Start, IOB0-2_RSTL/IOE_RSTL becomes 1. Also, exp_IO[B|E][0-2]_Y[0-7] and exp_IO[B|E][0-2]_YCK1 become 0.

4. Input 1 to IOB0_X0 and set b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 1.

5. Input a value in the order of 0, 1, 0 to IOB0_X1.

6. Input 0 to IOB0_X0 and set b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 0.

Logging system flag (lgdw_sys_sts) (FPGA register address: 1000_9004H), and Constant read register 14 (usr_alwreg_0E) (FPGA register address: 1000_A04CH) are initialized by writing each bit of Flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H), and Constant write register 14 (usr_alwreg_0E) with 1. After checking the status of each register, the initialization is performed by writing each bit of Flag clear register (lgdw_flag_clr) and Constant write register 14 (usr_alwreg_0E) (FPGA register address: 1000_A02CH) with 1.

After setting b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 0, check that the register areas have the value shown in the table below.

Register name	Expected value	Reference
b8 of Logging state register (lgdw_sts)	0	Page 551 Logging state register
b13 of Logging system flags (lgdw_sys_sts)	0	Page 552 Logging system flag
b14 of Logging system flags (lgdw_sys_sts)		
b0 of Constant read register 14 (usr_alwreg_0E)	1	Page 571 Always read register 14
b1 of Constant read register 14 (usr_alwreg_0E)		

7. After setting b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 1, input 1 to IOB0_X0.

8. Input a value in the order of 0, 1, 0 to IOB0_X1. (1clk pulse)

9. Wait until b8 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) becomes 1.

10. Set b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to 0 and input 0 to IOB0_X0.

After inputting 0 to IOB0_X0, check that the register areas have the value shown in the table below.

Register name	Expected value	Reference
b8 of Logging state register (lgdw_sts)	1	Page 551 Logging state register
b13 of Logging system flags (lgdw_sys_sts)	0	Page 552 Logging system flag
b14 of Logging system flags (lgdw_sys_sts)		
b15 of Logging system flags (lgdw_sys_sts)	1	
b0 of Constant read register 14 (usr_alwreg_0E)	0	Page 571 Always read register 14
b1 of Constant read register 14 (usr_alwreg_0E)		

Verification details

This section describes the tasks and parameters included in the provided patterns.

Precautions

- Since the firmware automatically controls the parts that use the private register to control the FPGA, set the public register according to the provided patterns.
- For the initial values of the FPGA register implemented in the FPGA, refer to the following.

☞ Page 502 FPGA register

- Perform verification using the provided verification environment and create a report file ($HOME\SIM_TOP\log). At that time, a warning will be output as a result of executing the sample circuit and a provided pattern, but there is no problem. For warnings, refer to the following.

☞ Page 712 Provided pattern warning list

■Tasks included in provided patterns

File name	Task name	Description
inc/dut_inst.sv	task T_INITSIG;	Input the initial value. Set IOB/E_DCDL to 1. Other values are set by model_set.sv and other files.
inc/glb_set.sv	task MICON_WR; input int cs_num; input [31:0] addr; input [15:0] wr_data;	Perform write access from the microcomputer. Write the data (specified by wr_data) to the address (specified by addr) of the chip select (specified by cs_num). • cs_num: Chip select number (0 to 2) • addr: Access address • wr_data: Writing data
inc/glb_set.sv	task MICON_RD; input int cs_num; input [31:0] addr; input [15:0] rd_data;	Perform read access from the microcomputer. Reading data from the address (specified by addr) of the chip select (specified by cs_num) and compare it with rd_data. • cs_num: Chip select number (0 to 2) • addr: Access address • rd_data: Expected value of reading data
inc/tb_common.sv	task T_UNITDISP;	Display the identification string of the circuit board connected to each slot. Call the string at the beginning of a pattern and display it in a log. • No argument
inc/tb_common.sv	task T_RSTSEQ;	Change the external reset from input to cancel and wait until the internal reset is canceled. • No argument
inc/tb_common.sv	task T_SIMEND(input int nochk=0);	Perform the Sim termination processing. When performed, check system error interrupts and display the Sim time/final error count. Be sure to call the task at the pattern end position. • nochk: System error interrupt check off (default: 0) 0: With system error interrupt check 1: Without system error interrupt check Also, by specifying PATNAME inside a pattern, the pattern name will be displayed in the simulation execution log. For usage, refer to each provided pattern. An example is shown below. initial PATNAME="FNA_TOP_01010101";
inc/tb_common.sv	task automatic T_CMP(input chksig, input exp, input string signame, input int msglv = 0);	Compare the signal of chksig with exp when chksig is called. • chksig: 1-bit signal to be compared • exp: Expected value of a signal with which to be compared (if the value is 1'bx, do not compare.) • signame: String for identification when displaying the comparison result (optional) • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK

File name	Task name	Description
inc/tb_common.sv	task T_TIMFILSET(int slt, int mode, int dir=0);	Set the normal timing register/filter register. Set the register corresponding to the slot number specified by slt. • slt: Specify a slot number. 0d: B0 1d: B1 2d: B2 3d: E0 4d: E1 5d: E2 • mode: DC/differential input/output switching 0d: DC input/output circuit board 1d: Differential input/output circuit board • dir: Setting range (default: 0) 0: Input and output setting 1: Input setting only 2: Output setting only
inc/tb_common.sv	task T_PRESET(input bit[1:0] ddrsta=0, input int rom1st=1);	Preprocess the internal operation start. • ddrsta: 2-bit expected value of the DDR status (default: 0) • rom1st: Specify the range of the interrupt unmasking (default: 1) 1: System error. Cancel only data update. Other than 1: Unmask all
inc/tb_common.sv	task T_MDCTLR2(input bit strt);	Set internal operation start/stop. • strt: Value to be written to the internal operation start/stop bit 0: Stop 1: Start

inc/dut_inst.sv	task T_IOB0INIT();
	task T_IOB1INIT();
	task T_IOB2INIT();
	task T_IOEINIT();
		Set the expected value of each slot after reset cancellation. Automatically determine the module to be connected within the task.
		• No argument

inc/board.sv	task T_SETX(input logic [15:0] xval, input int msglv = 0);	Task for DC input/output circuit boards Control DC input [15:0]. • xval: Divide the DC input [15:0] into the lower side ([7:0]) and upper side ([15:8]) and input them to the FPGA in a time division manner. • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK
inc/board.sv	task T_SET422(input logic [7:0] xval, input int msglv = 0);	Task for differential input/output circuit boards Control the differential (RS-422) input [7:0]. • xval: Input the differential (RS-422) input [7:0] to the FPGA. • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK
inc/board.sv	task T_SET485(input logic xval, input int msglv = 0);	Task for differential input/output circuit boards Control the differential (RS-485) input. • xval: Input the differential (RS-485) input to the FPGA. • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK
inc/board.sv	task T_422OCMP(input bit [7:0] exp, input int msglv = 0);	Task for differential input/output circuit boards Generate the expected value of the differential (RS-422) output [7:0]. • exp: Expected value of the differential (RS-422) output [7:0] • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK
inc/board.sv	task T_485OCMP(input bit exp, input int msglv = 0);	Task for differential input/output circuit boards Generate the expected value of the differential (RS-485) output. • exp: Expected value of the differential (RS-485) output • msglv: Message display level (default: 0) 0: Display only on error 1 or greater: Display even if OK
inc/board.sv	task T_ADC_CONVST(input int delay=3, input int width=10);	Task for analog input/output circuit boards Control the CONVST and BUSY signals to the ADC. • delay: Delay time from the rising edge of IOE[2-0]_CONVST to the rising edge of IOE[2-0]_AD_BUSY • width: Delay time from the rising edge to falling edges of IOE[2-0]_AD_BUSY

File name	Task name	Description
inc/board.sv	task automatic T_ADC_SPI(input bit[2:0] csl, input bit[15:0] sdi, input bit[15:0] do_0a = '0, input bit[15:0] do_0b = '0, input bit[15:0] do_1a = '0, input bit[15:0] do_1b = '0, input bit[15:0] do_2a = '0, input bit[15:0] do_2b = '0);	Task for analog input/output circuit boards Perform ADC SPI communication. • csl: Chip select number (0 to 2) • sdi: ADC serial data output • do_0a: ADC0 cha data • do_0b: ADC0 chb data • do_1a: ADC1 cha data • do_1b: ADC1 chb data • do_2a: ADC2 cha data • do_2b: ADC2 chb data
inc/board.sv	task T_ADC_SPI_REG_WR(input bit[2:0] csl, input bit[5:0] adr, input bit[7:0] dat);	Task for analog input/output circuit boards Execute ADC register write. • csl: Chip select number (0 to 2) • adr: Access address • dat: Writing Data
inc/board.sv	task T_ADC_SPI_REG_RD(input bit[2:0] csl, input bit[5:0] adr, input bit[7:0] dat, input bit mode=0);	Task for analog input/output circuit boards Execute ADC register read. • csl: Chip select number (0 to 2) • adr: Access address • dat: Expected value data • mode: Select the ADC mode. 0b: ADC register read 1b: Change the mode in which the A/D conversion value is acquired periodically from the ADC to ADC register read mode.
inc/board.sv	task T_ADC_SPI_CONV_RD(input bit[15:0] ADC0_V[1:8], input bit[15:0] ADC1_V[1:8], input bit[15:0] ADC2_V[1:8]);	Task for analog input/output circuit boards Read the A/D conversion value from the ADC. Perform SPI communication after CONVST rises. • ADC0_V: Set the expected value of the current/voltage input from the ADC. (ADC0_V[1,3,5,7] current input, ADC0_V[2,4,6,8] voltage input) • ADC1_V: Set the expected value of the current/voltage input from the ADC. (ADC1_V[1,3,5,7] current input, ADC1_V[2,4,6,8] voltage input) • ADC2_V: Set the expected value of the current/voltage input from the ADC. (ADC2_V[1,3,5,7] current input, ADC2_V[2,4,6,8] voltage input)
inc/board.sv	task T_ADC_INITSEQ (input bit[2:0] csl, input bit mode[0:3], input bit[3:0] range[0:3]='{4{'h3}}, input bit[7:0] oversamp='0, input bit[5:0] gain[0:3]='{4{'h00}}, input bit[7:0] offset[0:3]='{4{'h80}}, input bit[7:0] phase[0:3]='{4{'h0}});	Task for analog input/output circuit boards Initialize the ADC. • csl: chip select number 110b: ADC0 101b: ADC1 011b: ADC2 • mode: Select current or voltage 0: Current 1: Voltage • range: ADC range setting 0001b: ±5V single-ended 0010b: ±10V single-ended • oversamp: ADC oversampling setting • gain: Setting prohibited (fixed to 0) • offset: ADC offset setting • phase: Setting prohibited (fixed to 0)
inc/board.sv	task T_DAC_SPI(input bit [31:0] di);	Task for analog input/output circuit boards Perform DAC SPI communication. • di: DAC serial data
inc/board.sv	task T_DAC_SPI_CONV_WR(input bit[1:0] dut_adr, input bit[15:0] dat);	Task for analog input/output circuit boards Output the D/A conversion value. • dut_adr: DUT address 00: ch0 01: ch1 • dat: D/A conversion value

■Parameters included in provided patterns

File name	Parameter name	Description
inc/tb_common.sv	parameter P_BSLT0	Determine the FPGA external connection (Connector (B0)). 0: No connection 1: DC input/output circuit board 2: Differential input/output circuit board 3 or greater: No connection The defparam statement is used to declare the connection in each pattern.
inc/tb_common.sv	parameter P_BSLT1	Determine the FPGA external connection (Connector (B1)). 0: No connection 1: DC input/output circuit board 2: Differential input/output circuit board 3 or greater: No connection
inc/tb_common.sv	parameter P_BSLT2	Determine the FPGA external connection (Connector (B2)). 0: No connection 1: DC input/output circuit board 2: Differential input/output circuit board 3 or greater: No connection
inc/tb_common.sv	parameter P_ESLT	Determine the FPGA external connection (Connector (E)). 0: No connection 1: DC input/output circuit board 2: Differential input/output circuit board 3: Analog input/output circuit board 4 or greater: No connection
inc/tb_common.sv	parameter P_DDR_SET	Set the connection for the DDR3L SDRAM verification model. 0: Without DDR3L SDRAM verification model connection 1: With DDR3L SDRAM verification model connection 2: Without DDR3L SDRAM verification model connection
inc/tb_common.sv	string PATNAME	Specify the pattern name. The string set with this parameter is displayed in the simulation execution log.

10.4 FPGA Logic Synthesis Procedures

Logic synthesis environment

The logic synthesis environment for the provided sample circuit is shown below. Modify this environment and execute logic synthesis.

○: Need to be changed according to the user circuit block, ×: Do not change

No.	Directory				Description	Changeability
(1)	$HOME	—			Logic synthesis top folder	×
(2)		RTL	—		RTL storage directory	×
(3)			TOP	—	RTL storage directory (top layer)	×
(4)				UC	RTL storage directory (UC) (user circuit block)	○
(5)				*/	RTL storage directory (TOP, each block) (standard circuit)	×
(6)		Layout	—		Logic synthesis folder	×
(7)			top.qpf		Project file for the FPGA development software	×
(8)			top.qsf		Restrictions file for the FPGA development software	○
(9)			top.sdc		Restrictions file for logic synthesis	×
(10)			top_jtag.sdc		Restrictions file for logic synthesis (for JTAG)	×
(11)			conv_···.cof		jic file, rpd file generation script	×
(12)		SAMPLE_CONFIGURATION_DATA	—		Storage directory for sample configuration data	×
(13)			top_compressed.jic		Sample configuration data file (JIC format)	×
(14)			top_compressed.rpd		Sample configuration data file (RPD format)	×
(15)			top.sof		Sample configuration data file (SOF format)	×

Procedure for logic synthesis execution

■Execution procedure

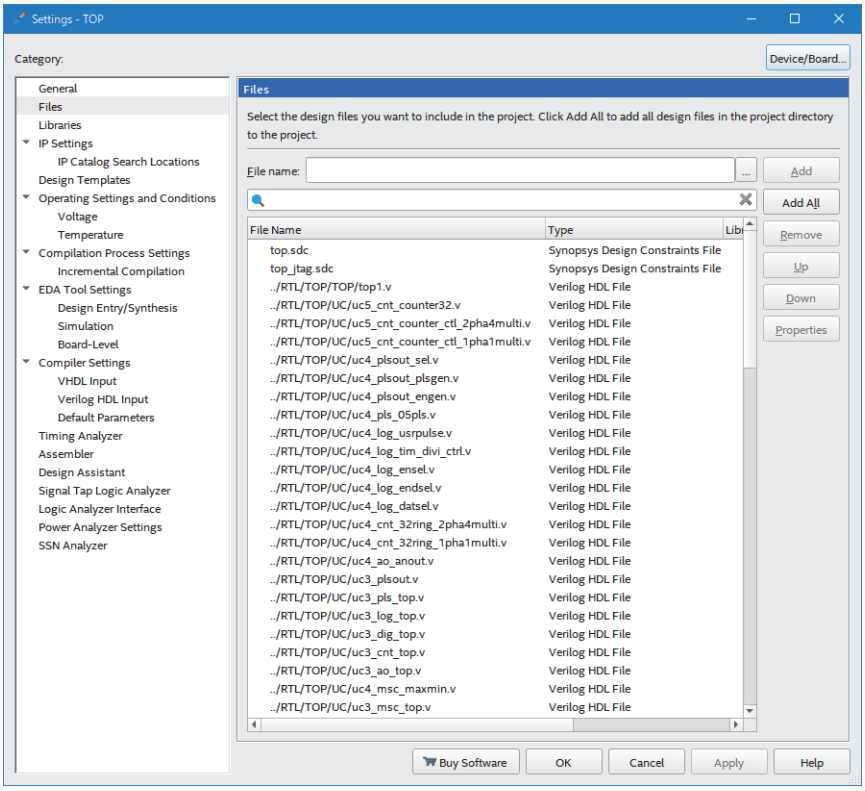
The following is the execution procedure for provided sample circuits logic synthesis environment.

1. Double-click the (7)top.qpf file for the logic synthesis environment to start FPGA development software.
2. Set files in (4)UC and (5)*/ folders for the logic synthesis environment to FPGA development software.

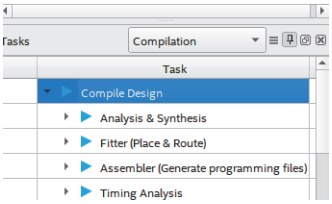
When setting the files to FPGA development software, if restrictions on the logic synthesis need to be added, create a logic synthesis restrictions file apart from (9)top.sdc and (10)top_jtag.sdc files for the logic synthesis environment, and set the file with FPGA development software. When addition of restrictions on the logic synthesis is not required, the setting of the logic synthesis restrictions file is not required. The step 3 shows how to set the files.

3. Specify created RTL files and logic synthesis restrictions file in "File name".

[Assignments] ⇨ [Settings]



4. Click the [OK] button.
5. Check the difference between the */ file of (5) in the configuration for the logic synthesis environment and RTL of FPGA development environment for CC-Link IE TSN FPGA module. When the differences have been found, store the file that is re-downloaded from Mitsubishi Electric FA Global Website.
6. Double-click "Compile Design" to execute the compilation on FPGA development software.



7. When the compilation has been completed, a report file is output to the (6) folder for the logic synthesis environment. Check the contents of the file to confirm that there is no problem.

■Notes and restrictions

The following table lists notes and restrictions when executing logic synthesis.

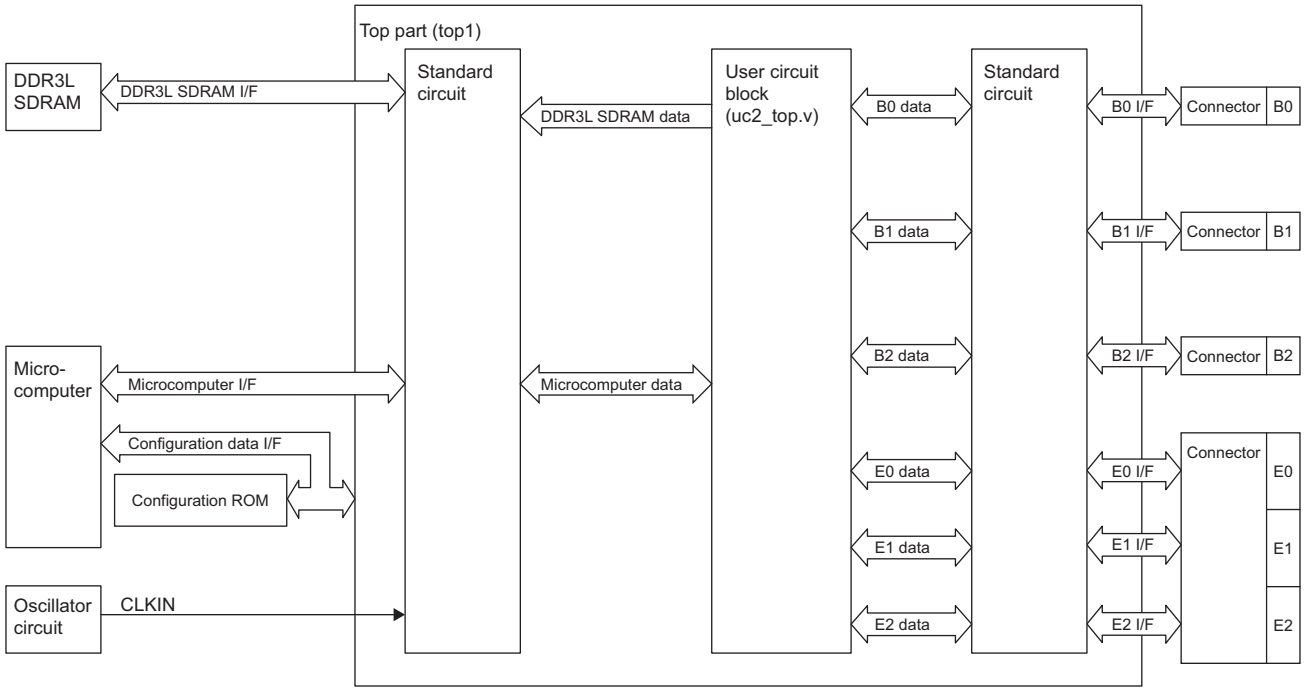
Item	Description
Initial logic synthesis procedure	Execute logic synthesis using the provided logic synthesis environment and create a report file. The report file is created in the logic synthesis environment (6) folder. There is no problem with warnings and deleted register areas in the sample circuit. If RTL (user circuit block) is modified, analyze the parts other than the above warnings and deleted register areas. As a result of the analysis, if needed, modify the environment. Refer to the following for details on warnings. ☞ Page 693 Sample circuit warning list
Restrictions file for logic synthesis	Do not modify the logic synthesis environment (7), (9), and (10) files because they describe the logic synthesis restrictions (FPGA external input/output restrictions) of the standard circuit. If modified, the standard circuit will not be covered by the warranty. If logic synthesis restrictions are required in the RTL with which the user circuit block is modified, add a restriction file for the logic synthesis restrictions to the logic synthesis environment (6) folder.
Timing Violation in the standard circuit	If a Timing Violation occurs in the standard circuit, review the modified RTL (user circuit block). The following are examples of review targets. • Circuit scale • Interface of uc2_top.v • Fanout of FF If the logic synthesis environment (7), (9), or (10) file is modified, the standard circuit will not be covered by the warranty.
Verification debug procedure	If unintended behavior occurs when using the file after logic synthesis to verify the actual machine, review the verification environment according to the procedures shown below. ■Checking on a personal computer • Check if the standard circuit block has been modified. Check the difference between the RTL downloaded from the Mitsubishi Electric FA site (logic synthesis environment (5) file) and the RTL with which logic synthesis was performed. • Check the FPGA design of the user circuit block. Check if there is any problem with the circuit of the user circuit block. • Check the FPGA verification of the user circuit block. Check if the verification covers all conditions. • Check the result of logic synthesis including the user circuit block. Check Timing Violation and Warning/Error in each report. ■Checking on the actual machine • Check the operation using the actual machine. When checking the operation, use a tool such as the Signal Tap logic analyzer that is included in the FPGA development software. For information on how to use the tool, contact Intel® Corporation.

11 FPGA INTERNAL CIRCUIT

The circuit mounted on the FPGA of the factory default FPGA module is shown below.

11.1 Overview

The FPGA structure of the factory default FPGA module is shown below. The only block that needs development is the user circuit block (uc2_top.v). Do not change the RTL of the standard circuit. If the standard circuit is modified, the operation of various functions cannot be guaranteed.



FPGA peripheral circuit structure

The FPGA connects one of the following to each connector (B0, B1, B2, E0, E1, E2). Change and use the connection inside the FPGA for each connected circuit board.

- DC input/output circuit board
- Differential input/output circuit board
- Analog input/output circuit board

For details on the DC/differential input circuit, DC/differential output circuit, and ADC/DAC circuit, refer to the following.

☞ Page 74 External Wiring

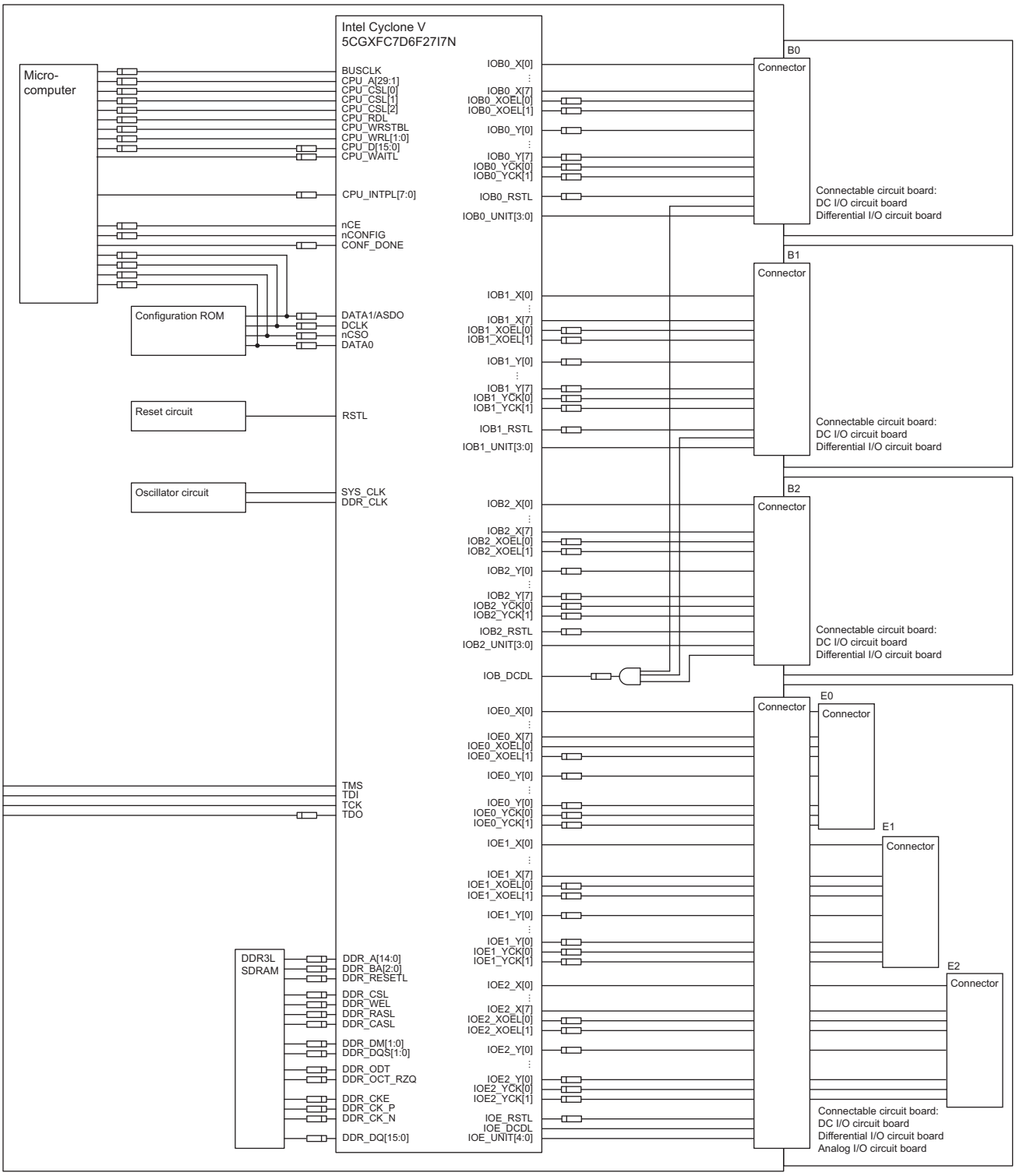
For details on the external terminals of the FPGA, refer to the following.

☞ Page 651 A List of FPGA External Terminals

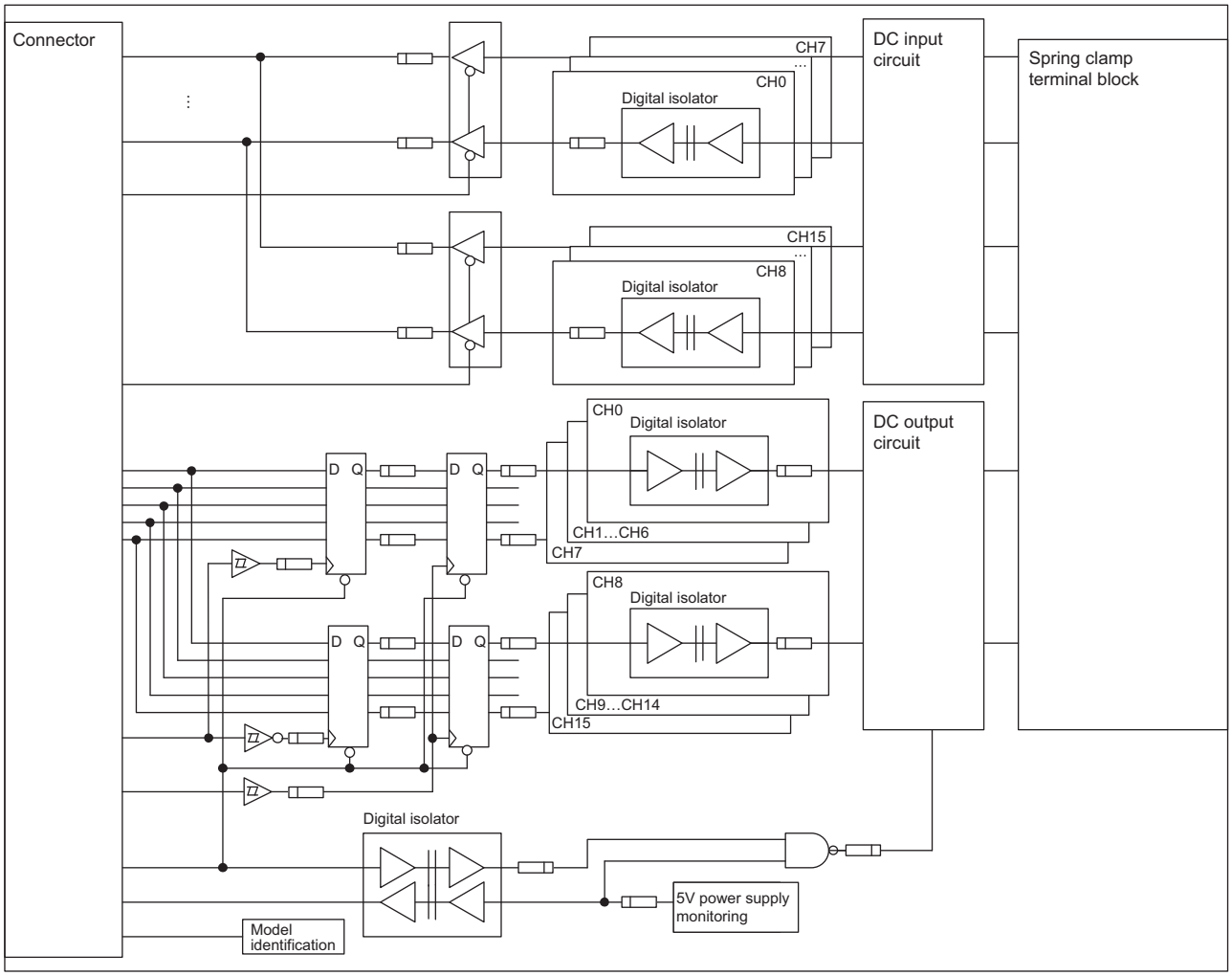
FPGA peripheral circuit connection

The peripheral circuit connection of the FPGA is shown below.

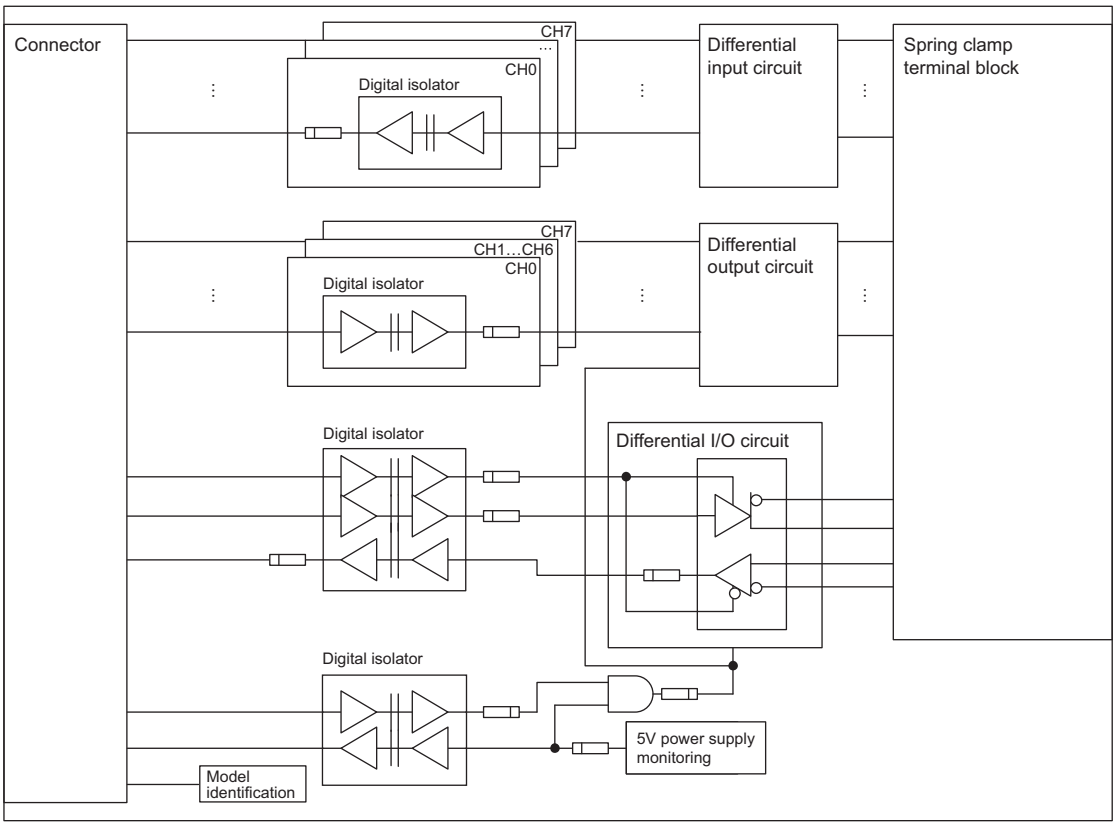
■FPGA circuit board



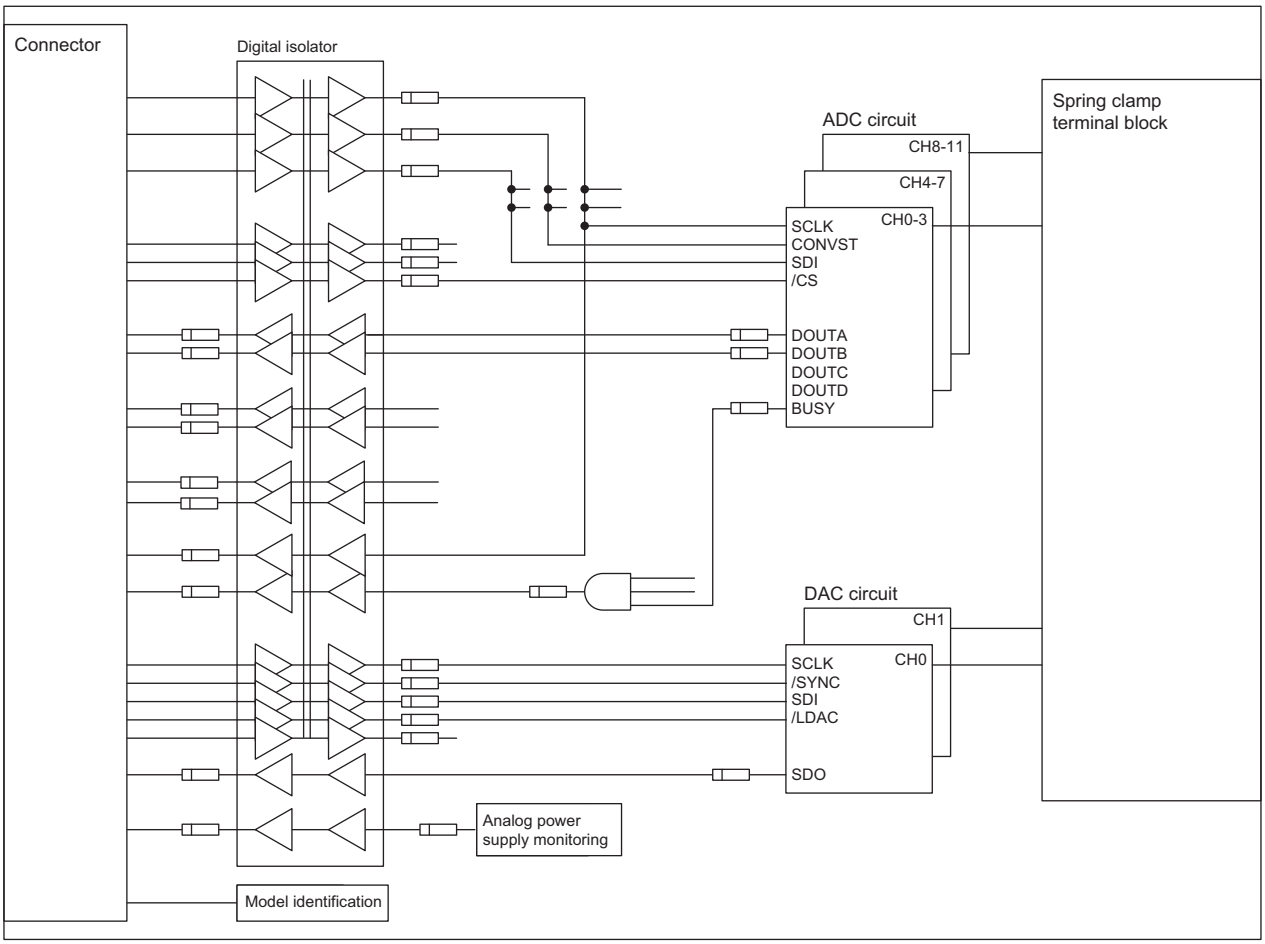
■DC input/output circuit board



■Differential input/output circuit board



■Analog input/output circuit board



■Prefix

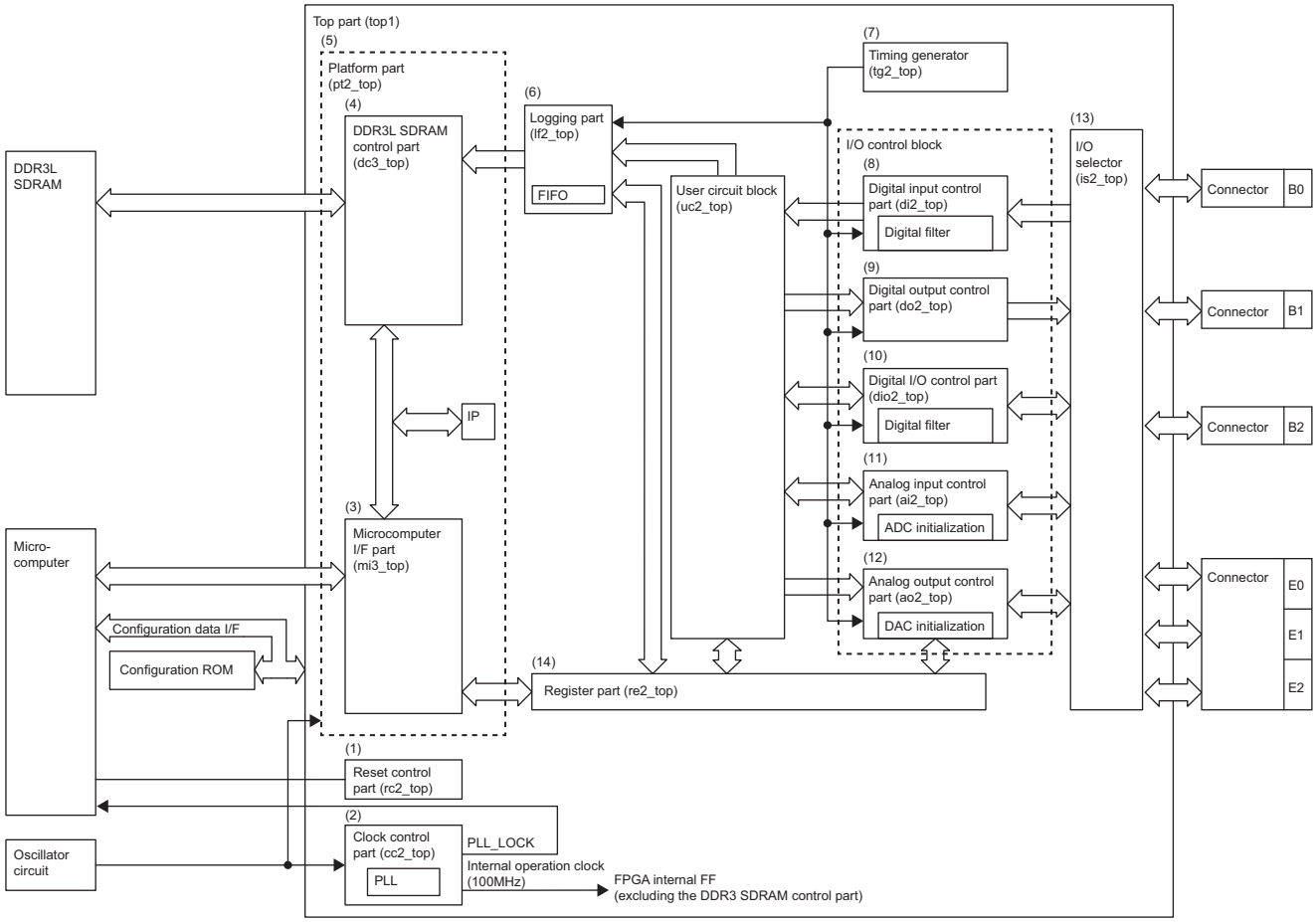
The prefix of an external terminal name is already determined for each connector. Terminal prefixes are shown below.

Target connector	Corresponding signal (prefix)
Common from B0 to B2	IOB_
B0	IOB0_
B1	IOB1_
B2	IOB2_
Common from E0 to E2	IOE_
E0	IOE0_
E1	IOE1_
E2	IOE2_

Function blocks

Standard circuit

Do not change the standard circuit. If the standard circuit is modified, the operation of various functions cannot be guaranteed.



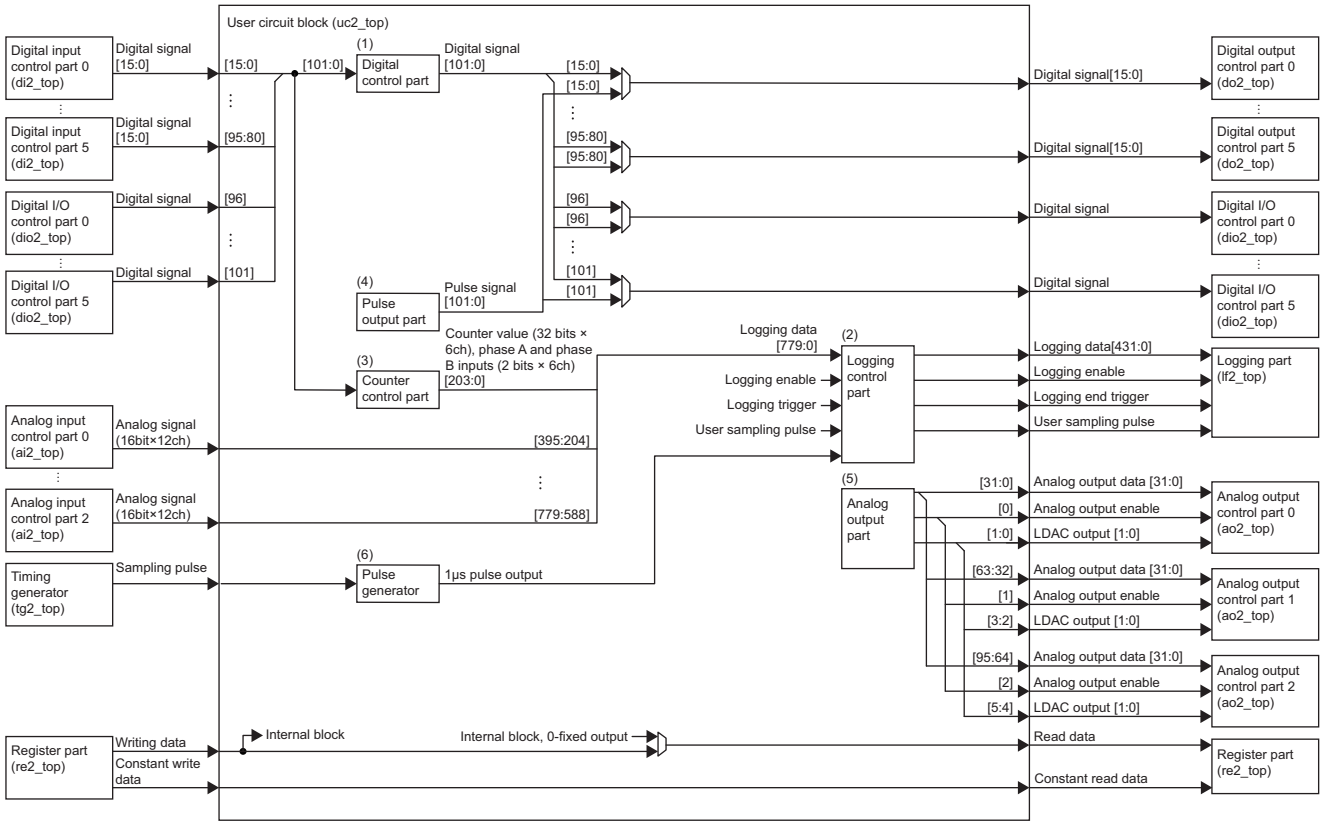
No.	Function blocks	Function	Classification	Reference
(1)	Reset control part	Controls the reset inside the FPGA. The reset from the MCU is connected to all register areas in the FPGA.	Module common circuit	Page 188 Reset control part (rc2_top)
(2)	Clock control part	Generates the system clock used inside the FPGA. The system clock is 100MHz.	Module common circuit	Page 189 Clock control part (cc2_top)
(3)	Microcomputer I/F part	Controls register access/memory access from the MCU. It controls the 16-bit data bus.	Module common circuit	Page 190 Platform part (pt2_top)
(4)	DDR3L SDRAM control part	Writes the logging data output from the logging block to DDR3L SDRAM. In addition, logging data is read from DDR3L SDRAM by a read request from the microcomputer I/F part	Module common circuit	
(5)	Platform part	Implements Intel® FPGA Avalon® interface and connects the IP inside the FPGA and the microcomputer I/F part. FPGA internal CPU (Nios® Ⅱ/e) is equipped with a program ROM, WorkRAM, and DPRAM for output value storage as peripheral circuits. The following functions are implemented in the platform part. • Controls writing of logging data to DDR3L SDRAM. • Microcomputer I/F part, Nios® Ⅱ/e controls reading/writing to DDR3L SDRAM.	Module common circuit	

No.	Function blocks	Function	Classification	Reference
(6)	Logging part	Stores the output signal of user circuit block in the internal memory (FIFO) for each logging cycle timing pulse of the timing generator output. The data is stored in DDR3L SDRAM via the platform block. The logging part implements the following functions. • User circuit part I/F • Platform part I/F • Logging data sampling • Logging operation (trigger operation mode) • Logging operation (storage operation mode) • DDR3L SDRAM control • User sampling pulse cycle monitoring • Time control	Module common circuit	Page 191 Logging part (lf2_top)
(7)	Timing generator	Generates input/output timing between the input/output control block and the user circuit block. The following four timing signals are generated. • Sampling pulse for digital input filter • Digital/analog data sampling pulse • Digital/analog data update pulse • Logging cycle timing pulse	Module common circuit	Page 193 Timing generator (tg2_top)
(8)	Digital input control part	Removes noise and outputs to the circuit (register block, user circuit block) in the level immediately below. The digital input control part implements the following functions. • Digital filter function • Outputs the signal after digital filtering to the register block and user circuit block	Module specific circuit • NZ2GN2S-D41P01 • NZ2GN2S-D41D01 • NZ2GN2S-D41PD02 • NZ2EX2S-D41P01 • NZ2EX2S-D41D01	Page 196 Digital input control part (di2_top)
(9)	Digital output control part	Outputs signals from the register block or user circuit block to the outside of the FPGA via the input/output selector. Also, when the FPGA has stopped operating, the output value that was output immediately before is held (HOLD) or cleared (CLEAR). The digital output control part implements the following functions. • Digital output signal selection function • HOLD/CLEAR function	Module specific circuit • NZ2GN2S-D41P01 • NZ2GN2S-D41D01 • NZ2GN2S-D41PD02 • NZ2EX2S-D41P01 • NZ2EX2S-D41D01	Page 199 Digital output control part (do2_top)
(10)	Digital input/output control part	Removes noise and outputs to the circuit (register block, user circuit block) in the level immediately below. Outputs signals from the register block or user circuit block to the outside of the FPGA via the input/output selector. Also, when the FPGA has stopped operating, the output value that was output immediately before is held (HOLD) or cleared (CLEAR). The digital input/output control part implements the following functions. • Digital filter function • Outputs the signal after digital filtering to the register part and user circuit block • Digital output signal selection function • HOLD/CLEAR function	Module specific circuit • NZ2GN2S-D41D01 • NZ2GN2S-D41PD02 • NZ2EX2S-D41D01	Page 202 Digital input/output control part (dio2_top)
(11)	Analog input control part	Controls the ADC connected to the outside of the FPGA and captures analog values. The analog input control part implements the following functions. • Generates signals for clock synchronous serial IF • Initializes ADC • Function to output the A/D conversion value to the register part and user circuit block for each data sampling pulse	Module specific circuit • NZ2EX2S-D41A01	Page 205 Analog input control part (ai2_top)
(12)	Analog output control part	Controls the DAC connected to the outside of the FPGA and outputs analog values to the device connected to the module. The analog output control part implements the following functions. • Generates signals for clock synchronous serial IF • Initializes DAC • Selects and outputs the D/A conversion value from the register block or user circuit block at each data update timing.	Module specific circuit • NZ2EX2S-D41A01	Page 211 Analog output control part (ao2_top)
(13)	Input/output selector	Switches the input/output of the external terminal of the FPGA from the model identification signal. The input/output selector implements the I/O terminal switching function.	Module common circuit	Page 194 Input/output selector (is2_top)
(14)	Register part	Mounts register areas inside the FPGA. The register part implements the following functions. • Notifies the FPGA setting value to the inside of the FPGA. It also notifies the signal (monitor) inside the FPGA to the MCU. • FPGA version register*1		Page 195 Register part (re2_top)

*1 The FPGA version register is the version of the provided standard circuit and sample circuit.

User circuit block (sample circuit)

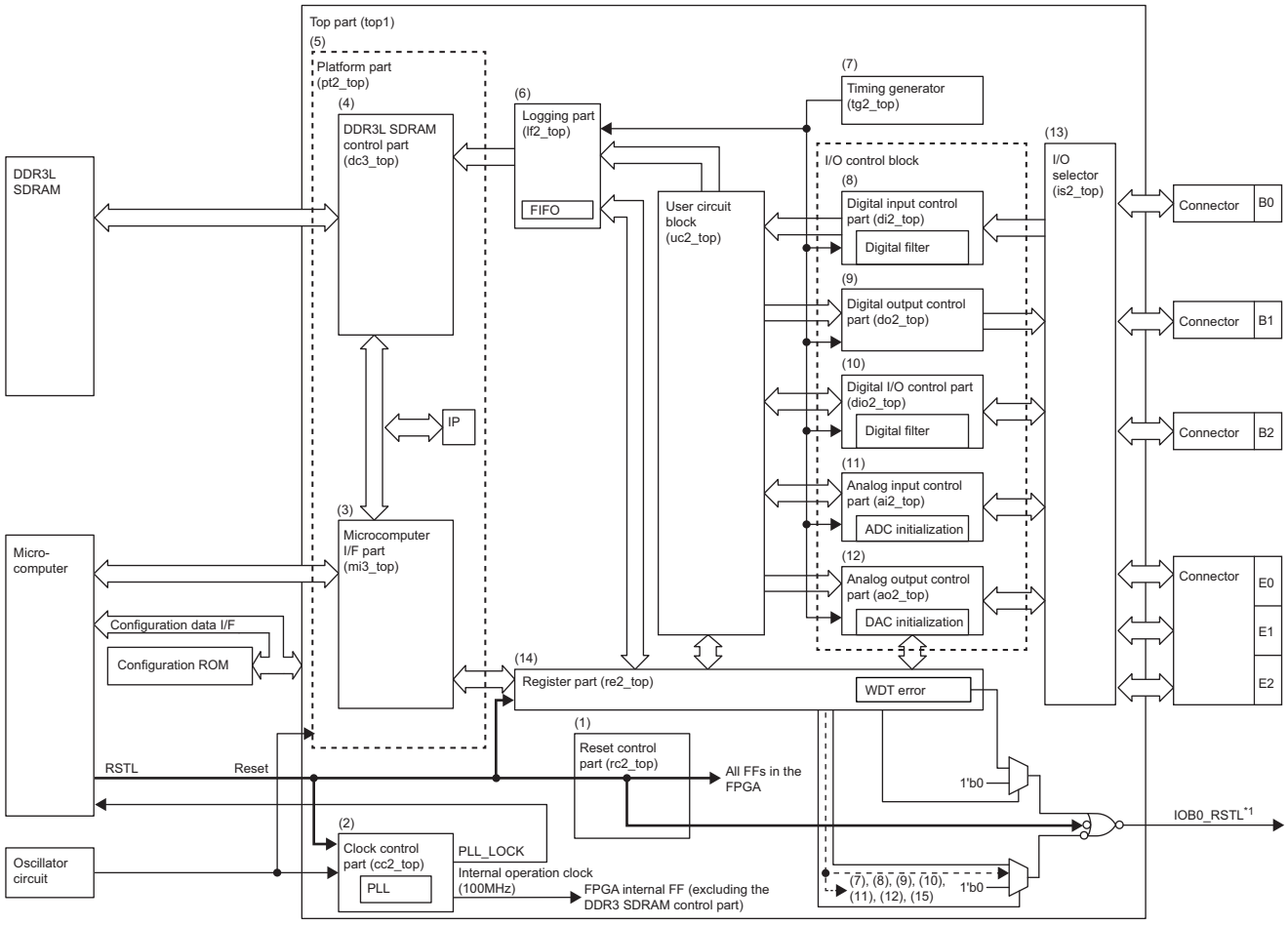
The structure of the factory default user circuit block (sample circuit) is shown below.



No.	Function blocks	Function	Reference
(1)	Digital control part	Inverts digital signals input from the digital input control part and digital input/output control part, and enables/disables output.	Page 246 Digital control part (uc3_dig_top)
(2)	Logging control part	Selects and outputs data to be logged and the signal that controls the logging part. The logging control part implements the following functions. • Logging data selection • Logging enable selection • Logging end trigger selection • User sampling pulse selection	Page 271 Logging control part (uc3_log_top)
(3)	Counter control part	Implements the following counters that operate with the signal from the digital input control part. • 32-bit ring counter (2-phase multiple of 4) • 32-bit ring counter (1-phase multiple of 1)	Page 256 Counter control part (uc3_cnt_top)
(4)	Pulse output part	Outputs the following pulses to the digital output control part/digital input/output control part. • 0 degree pulse • 90 degree pulse • 180 degree pulse • 270 degree pulse The pulse can be set in units of 10ns.	Page 249 Pulse output part (uc3_plsout)
(5)	Analog output part	Generates the following DAC signals to be connected to the FPGA by register settings. • D/A conversion value • D/A conversion value enable • LDAC	Page 266 Analog output block (uc3_ao_top)
(6)	Pulse generator	Generates 1µs pulse for logging data generation.	Page 265 Pulse generator (uc3_pls_top)
(7)	Other connections	The following functions are implemented as other connections. • Executes HOLD/CLEAR of digital signals. • Outputs a user interrupt. • Controls connection of various signals.	—

Reset system diagram

The reset system diagram is shown below.



Internal operation start/stop

Reset

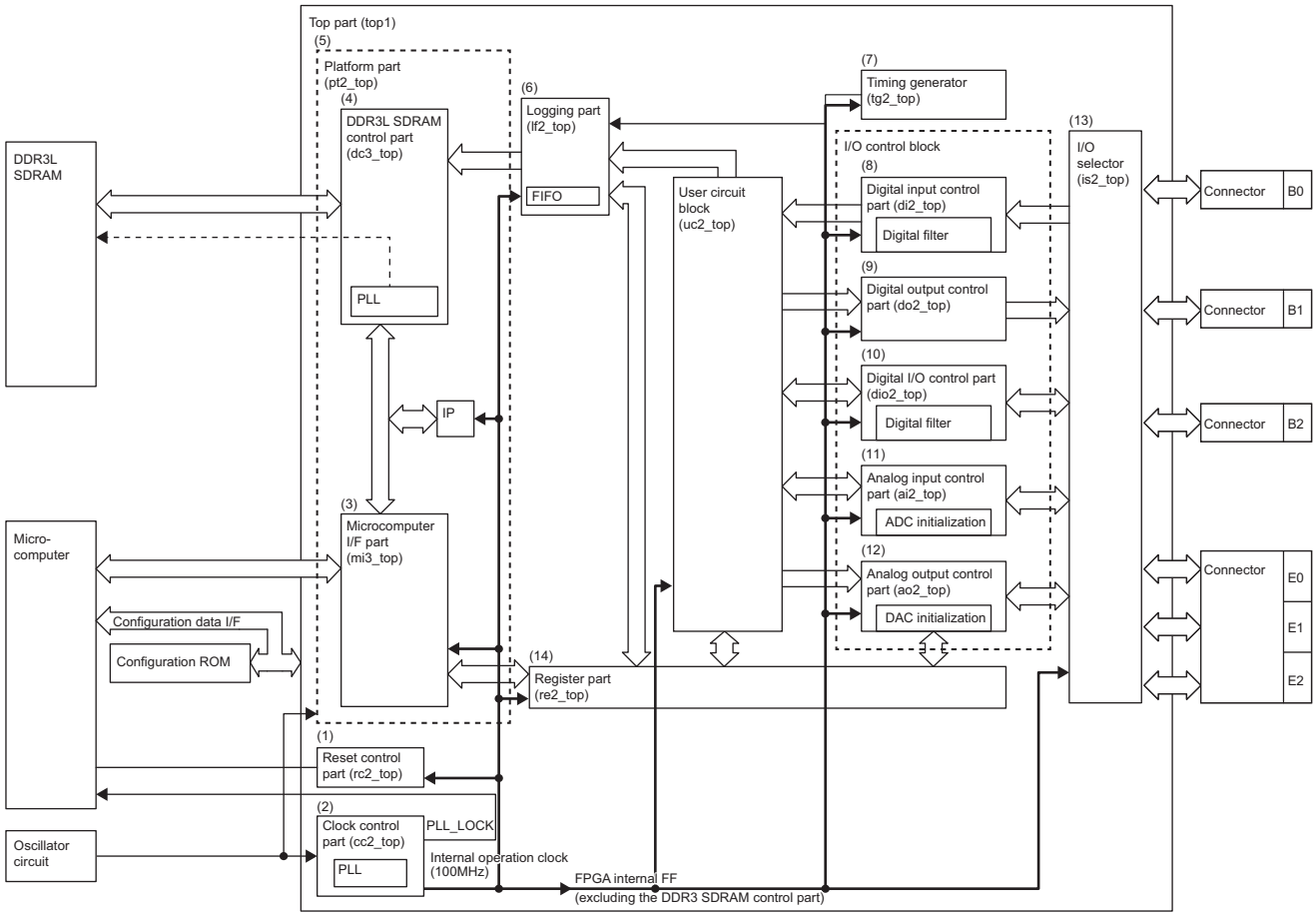
*1 IOB1_RSTL, IOB2_RSTL, and IOE_RSTL have the same structure.

For details on the reset system, refer to the following.

☞ Page 188 Reset control part (rc2_top)

Clock system diagram

The clock system diagram is shown below.



For details on the clock system, refer to the following.

☞ Page 189 Clock control part (cc2_top)

FPGA external terminal list

For the list of FPGA external terminals, refer to the following. In addition, the external terminal connected to the connector recognizes the connected circuit board type inside the FPGA and automatically connects to the appropriate block.

☞ Page 651 A List of FPGA External Terminals

FPGA memory map

For the FPGA memory map, refer to the following.

☞ Page 321 FPGA Register Access Function

Register

For details on the FPGA, refer to the following.

☞ Page 502 FPGA register

11.2 Details

The FPGA internal circuit changes and uses the following input/output control part block connections for each module.

- Digital input control part (di2_top)
- Digital output control part (do2_top)
- Digital input/output control part (dio2_top)
- Analog input control part (ai2_top)
- Analog output control part (ao2_top)

This section describes the details on the module common circuit used by all modules and the module specific circuit used for each module. The module specific circuit used for each module is shown below.

Module category	Model	Connection circuit board	Target input/output control part block
Main module	NZ2GN2S-D41P01	B0, B1, B2: DC input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top)
	NZ2GN2S-D41D01	B0, B1, B2: Differential input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top) Digital input/output control part (dio2_top)
	NZ2GN2S-D41PD02	B0, B1: DC input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top)
		B2: Differential input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top) Digital input/output control part (dio2_top)
Extension module	NZ2EX2S-D41P01	E0, E1, E2: DC input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top)
	NZ2EX2S-D41D01	E0, E1, E2: Differential input/output circuit board	Digital input control part (di2_top) Digital output control part (do2_top) Digital input/output control part (dio2_top)
	NZ2EX2S-D41A01	E0, E1, E2: Analog input/output circuit board	Analog input control part (ai2_top) Analog output control part (ao2_top)

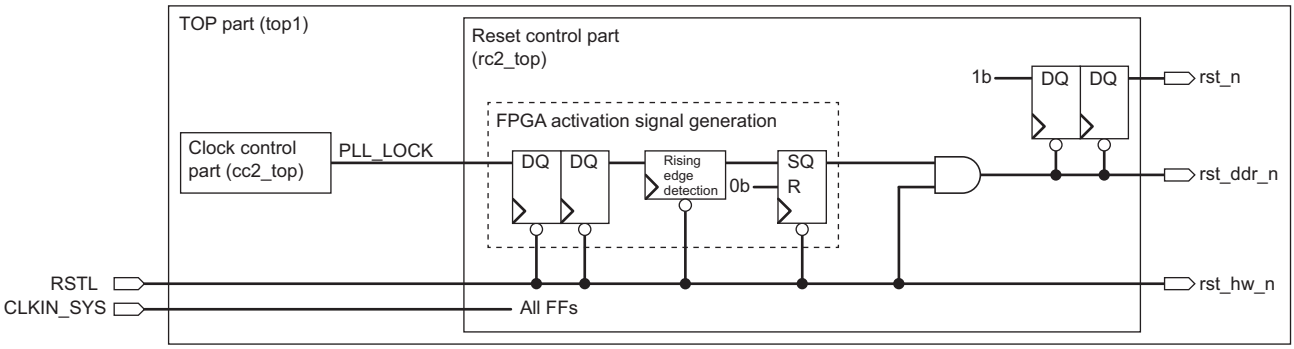
11.3 Standard Circuit

Do not change the standard circuit. If the standard circuit is modified, the operation of various functions cannot be guaranteed.

Module common circuit

Reset control part (rc2_top)

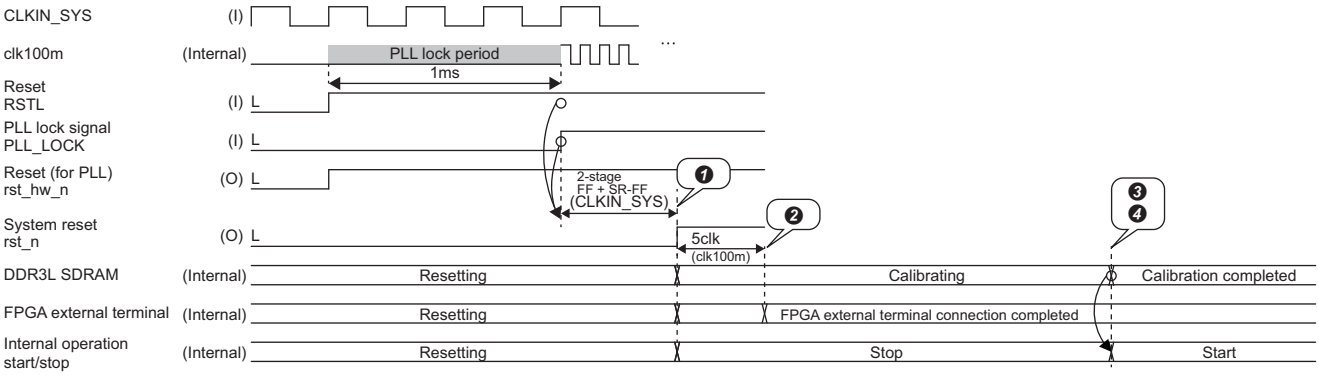
All register areas inside the FPGA are reset by a reset (RSTL) input from the MCU until the state transition of the FPGA or module is established, such as during configuration. In addition, the circuit in the FPGA can be started/stopped at any timing on the program.



Reset signal	Overview	Target
rst_n	System reset	Other than DDR3L SDRAM IF
rst_ddr_n	Reset for DDR3L SDRAM IF	DDR3L SDRAM IF
rst_hw_n	Reset (for PLL))	PLL

The reset is output as is for the PLL. (rst_hw_n: Reset (for PLL))

Also, for other resets (rst_n: system reset, rst_ddr_n: DDR3L SDRAM IF reset), the status remains as reset during the PLL unlock period.



❶ After the reset is released, the inside of the FPGA is reset (rst_re_hw_n=0, rst_n=0) during the PLL lock period.
❷ After the reset inside the FPGA, the connection of the external terminal is switched according to the type of circuit board to be connected.
❸ DDR3L SDRAM calibration is executed and the end of calibration is notified to the MCU.
❹ When the MCU sets internal operation start/stop to Start(1), the internal operation of the FPGA is started.

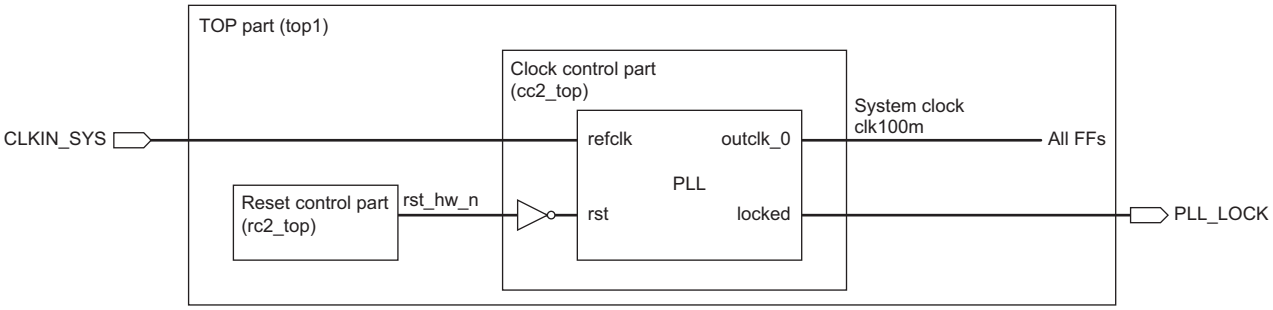
■Reset target list

The reset target list is shown below.

Reset cause	Reset function
Reset (RSTL) • Initializing at power-on • Configurating	Sets all FPGA register areas until the FPGA circuit is established.
Internal operation start/stop • FPGA control start request (RY0): start • FPGA control stop request (RY1): stop For details, refer to the following. ☞ Page 315 FPGA Control Function	Shows the processing content of each block as below when internal operation start/stop is stop. ■Timing generator Resets the internal circuit and is fixed at 0 without outputting pulses to the circuit in the level immediately below. ■Digital input control part Resets the internal circuit and fixes the output to the circuit in the level immediately below to 0. ■Digital output control part Holds (HOLD) or clears (CLEAR) the value that was output until just before. (☞ Page 315 FPGA Control Function) ■Digital input/output control part • Input side: Same as digital input control part • Output side: Same as digital output control part • I/O direction setting signal: Not applicable ■Analog input control part Stops A/D conversion. If it stops during conversion processing, the A/D conversion value is discarded. ■Analog output control part Stops D/A conversion. If it stops during conversion processing, it will stop after D/A conversion end. ■User circuit block Resets the internal circuit and outputs an inactive signal (0) to the circuit in the level immediately below. (It will be processed in the sample circuit. If the RTL is modified, the behavior will change.)
WDT error	The watchdog timer (WDT) monitors and detects hardware failure. A WDT error occurs when access to the FPGA from the MCU is interrupted for a long time due to a hardware failure. When a WDT error occurs, the value that was output immediately before is held (HOLD) or cleared (CLEAR) in the same way as when FPGA control stops. For details, refer to the following. ☞ Page 315 FPGA Control Function If the MCU can detect a WDT error, a hardware error (error code: 3C00H) is generated, and a reset is issued from the MCU to the FPGA. (WDT errors may not be detected due to hardware failures that occur.)

Clock control part (cc2_top)

PLL is used to generate system clock (clk100m). Other than IP, it operates with the system clock.



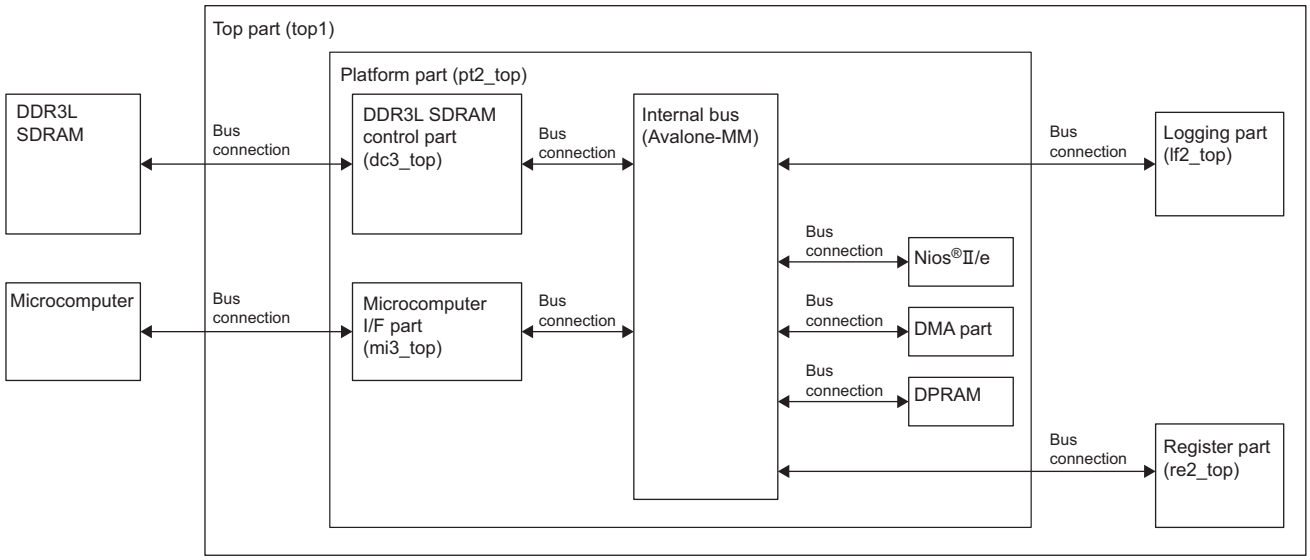
■Clock list

Clock signal	Function	Frequency	Origin	Where to use
clk100m	System clock	100MHz	FPGA internal PLL	• Timing generator • Microcomputer I/F part • Logging part • Digital/analog input/output function block input/output selector • Platform part • User circuit block*1

*1 Input signals to the user circuit block are synchronized with the system clock and input.

Platform part (pt2_top)

The platform part is a block that implements IP using Platform Designer included in the FPGA design software. This circuit performs FPGA internal register access from the MCU and DDR3L SDRAM access from the logging module.

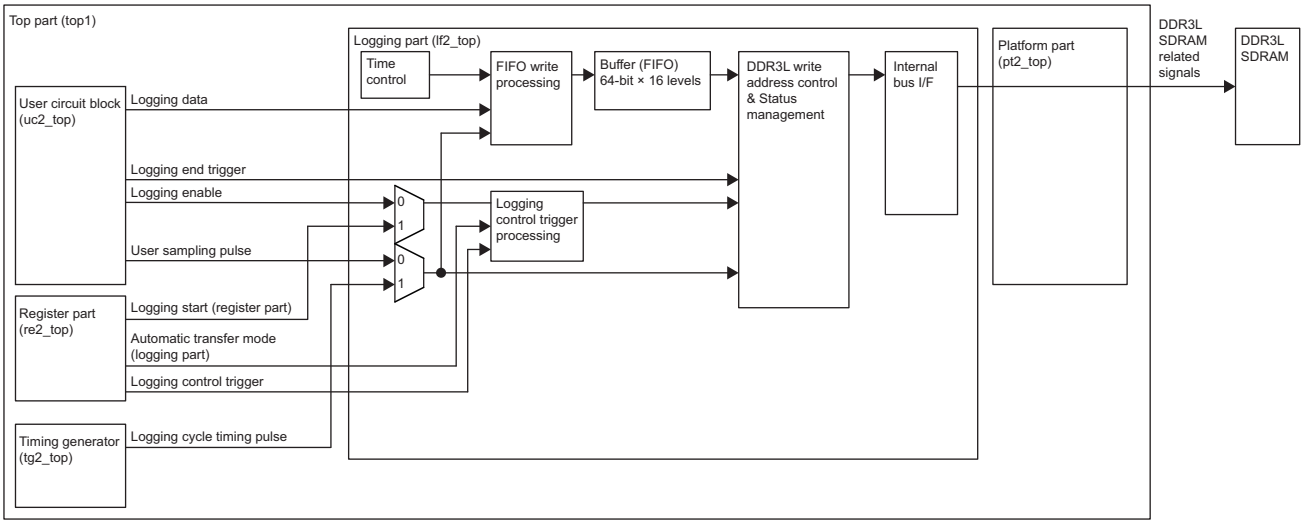


Item	IP name	Remarks
DDR3L SDRAM control part	DDR3 SDRAM Controller with UniPHY Intel® FPGA IP	—
Nios® Ⅱ/e part	Nios® Ⅱ/e(economy)	—
DMA part	Modular Scatter-Gather DMA Intel® FPGA IP	—
DPRAM part	On-Chip Memory (RAM or ROM) Intel® FPGA IP	—
Microcomputer I/F part	—	It is not IP. It is a bridge circuit that connects the MCU to the inside of the FPGA.

*1 Since the IP is used by the MCU, it cannot be used by the user circuit block.

Logging part (lf2_top)

It temporarily saves the time information and logging data output from the user circuit block in a buffer (FIFO 64-bit × 16 levels) for each logging cycle timing pulse of the timing generator output. Then, they are written to DDR3L SDRAM.
Logging starts with a signal that is selected as the logging start signal for the user circuit block or register part according to the setting value of the logging operation control register [12]. Also, logging is performed by synchronizing the user sampling pulse of the user circuit block or the logging cycle timing pulse of the timing generator with the selected signal according to the setting value of the logging operation control register [13].

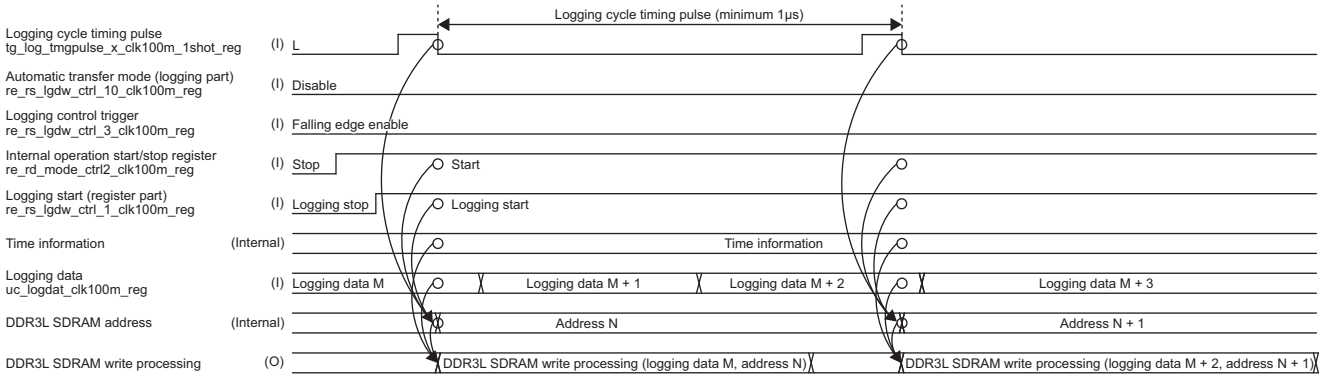


■Function List

Item	Operation	Remarks
FIFO write process	Receives the logging cycle timing pulse from the user circuit block or timing generator, and writes the logging data (432 bits) output from the user circuit block and the time information (80 bits) generated by the logging part to the FIFO. The data is divided into 64 bits and stored in the FIFO.	—
Buffer (FIFO) 64-bit × 16 levels	64-bit × 16-level FIFO	—
DDR3L SDRAM write address control state management	The operation modes of the logging part are shown below. • Storage operation mode • Trigger operation mode The DDR3L SDRAM area used for logging can be set by the logging data size setting of the register. The addresses are generated up to the set area and logging is performed via the platform part.	The maximum area of DDR3L SDRAM used for logging is set in the logging data size setting. The area start address is fixed at 0000_0000H. For an overview of the storage operation mode and trigger operation mode, refer to the following. ☞ Page 327 Logging Function
Internal bus I/F	Implements the light master interface of Intel® FPGA Avalon® interface.	—
Time control	Adds time information of calendar (Western calendar), month, day, hour, minute, second, ms, and μs to the logging data.	—
Automatic transfer mode (logging part)	In the automatic transfer mode, the firmware uses the logging control trigger to notify the FPGA of the period during which logging is possible, and operates according to the notification content. If the notification is not followed, the logging operation (during logging, or when logging stops) is maintained and continues.	—

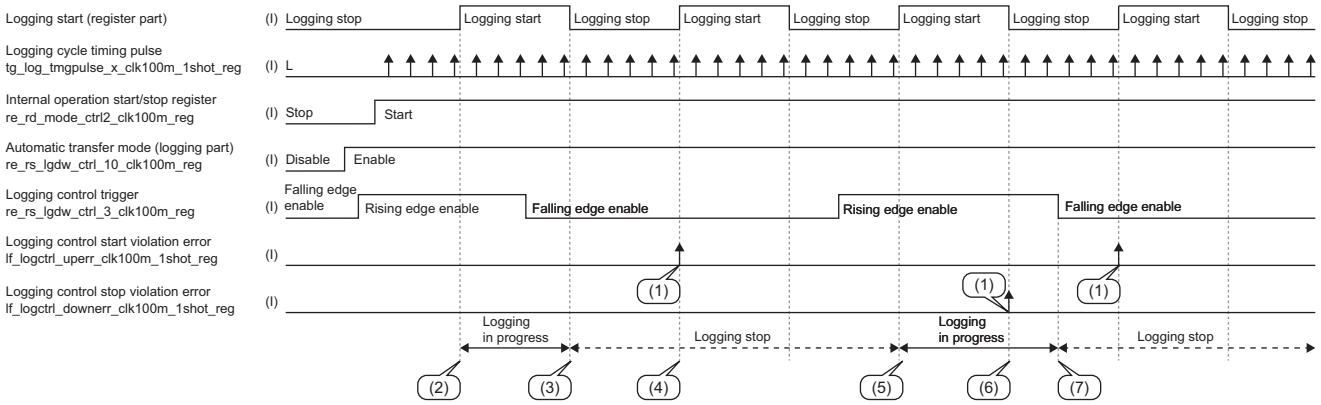
■Timing chart

Logging starts when the internal operation start/stop is Start and the logging start signal (logging start (register part), signal with logging enable selected) is Start (1). After logging starts, when the logging cycle timing (logging cycle timing, signal with user sampling pulse selected) is enabled (1), the DDR3L SDRAM address is generated and the logging data and time information are written to the DDR3L SDRAM.



■Automatic transfer mode

In this mode, the firmware uses the logging control trigger to notify the FPGA of the period during which logging is possible, and operates according to the notification content. If the content of the notification is not followed, the logging operation (logging in progress, or when logging stops) will be maintained and will continue.



(1) Minor error
(2) Automatic transfer mode (logging part) = Enable && Logging control trigger = Rising edge enable, so logging starts
(3) Automatic transfer mode (logging part) = Enable && Logging control trigger = Falling edge enable, so logging stops.
(4) Automatic transfer mode (logging part) = Enable && Logging control trigger = Falling edge enable, so logging does not start.

State transitions and conditions of logging during automatic transfer mode are shown below.

- Automatic transfer mode (logging part): Enable
- Internal operation start/stop register: Start

Logging control trigger	Logging start (register part)	Current state	Next state	Logging control start violation error	Logging control stop violation error
Rising edge enable	During rising edge	During logging*1	During logging	None	None
	During rising edge	Logging stop*2	During logging	None	None
	When L	During logging*1	During logging	None	Minor error*3
	When L	Logging stop*2	Logging stop	None	Minor error*3
Falling edge enable	During rising edge	During logging*1	During logging	Minor error	None
	During rising edge	Logging stop*2	Logging stop	Minor error	None
	When L	During logging*1	Logging stop	None	None
	When L	Logging stop*2	Logging stop	None	None
Others			Hold previous state	None	None

*1 Writing from FPGA to DDR3L-SDRAM
*2 No access from FPGA to DDR3L-SDRAM
*3 Only when the logging start (register part) is falling edge, a logging control stop violation error is output.

Timing generator (tg2_top)

After setting internal operation start/stop to Start (1), this block generates the timing pulse used in each function block. A list of timing pulses used in each block is shown below.

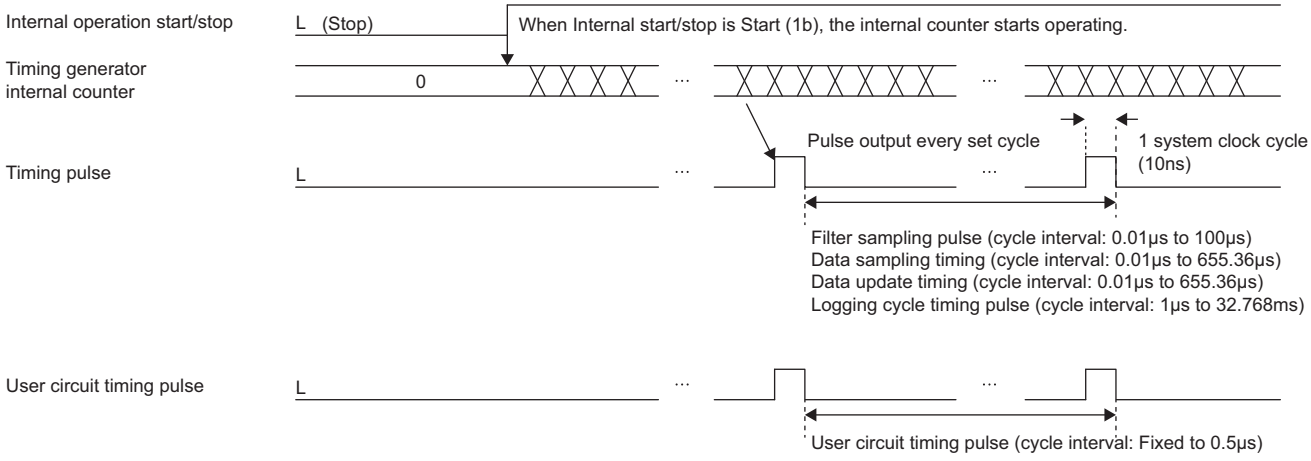
Item	Connection destination	Signal name	Description	Remarks
Filter sampling pulse	• Digital input control part • Digital input/output control part (input side)	tg_fil_tmgpulse_x_clk100m_1shot_reg*2	Generates timing pulse for digital filter. (100MHz (0.01μs) to 10KHz (100μs) can be selected.)	Set the cycle interval with the filter sampling pulse (B/E0 to E2).
Data sampling timing	• Digital input control part • Digital input/output control part (input side) • Analog input control part	tg_sampling_tmgpulse_x_clk100m_1shot_reg*2	Generates the timing pulse signal for determining the external input signal. (0.01μs to 655.36μs can be selected.)*1	Set the cycle interval with the data sampling timing (B/E0 to E2).
Data update timing	• Digital output control part • Digital input/output control part (output side) • Analog output control part • Register part	tg_datout_tmgpulse_x_clk100m_1shot_reg*2	Generates the timing pulse signal for determining the external output signal. (0.01μs to 655.36μs can be selected.)*1	Set the cycle interval with the data update timing (B/E0 to E2).
Logging cycle timing pulse	Logging part	tg_log_tmgpulse_clk100m_1shot_reg	Generates timing pulses for writing data to DDR3L SDRAM. (1μs to 32.768ms can be selected.)	Set the cycle interval with the logging cycle timing.
User circuit timing pulse	User circuit block	tg_05us_tmgpulse_clk100m_1shot_reg	Generates timing pulses for user circuit synchronization. (Fixed at 0.5μs)	Cycle interval output is fixed at 0.5μs.

*1 The minimum pulse interval differs for each connected circuit board. The minimum setting values for each circuit board are shown below.
DC input/output circuit board: 0.1μs
Differential input/output circuit board: 0.01μs
Analog input/output circuit board: Data sampling timing (4μs), data update timing (6μs) (The minimum setting value of the data sampling timing changes depending on the ADC oversampling ratio setting.)

*2 x=0, 1, 2, 3, 4, 5 (B0=0, B1=1, B2=2, E0=3, E1=4, E2=5)

■Timing chart

A schematic timing chart of the timing pulse output from the timing generator is shown below.



Input/output selector (is2_top)

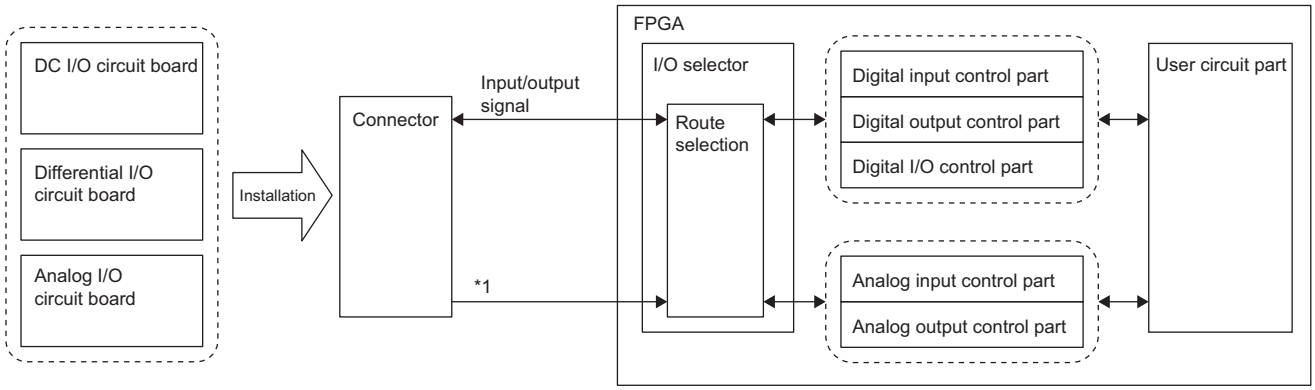
Each connector is connected to one of the following.

- DC input/output circuit board
- Differential input/output circuit board
- Analog input/output circuit board

The connector determines the circuit board based on the connected module type (IOB0_UNIT, IOB1_UNIT, IOB2_UNIT, IOE_UNIT).

The input/output selector uses the determined module type information to connect to the following function blocks and to output signals to the user circuit block via each function block.

- Digital input control part
- Digital output control part
- Digital input/output control part
- Analog input control part
- Analog output control part



*1 IOB1_UNIT, IOB2_UNIT, and IOE_UNIT have the same structure.

■Function List

A list of input/output selector functions is shown below.

Item	Operation
I/O terminal switching	Module type signals (IOB□_UNIT[3:0], IOE_UNIT[4:0]) are used as the basis for I/O terminal switching and FPGA internal connection.*1

*1 □: Indicates 0, 1, 2.

■Decoding result

The decoding result for each module type is shown below. Depending on each decoding result, the connection destination block in FPGA operates effectively.

- Main module connection circuit board

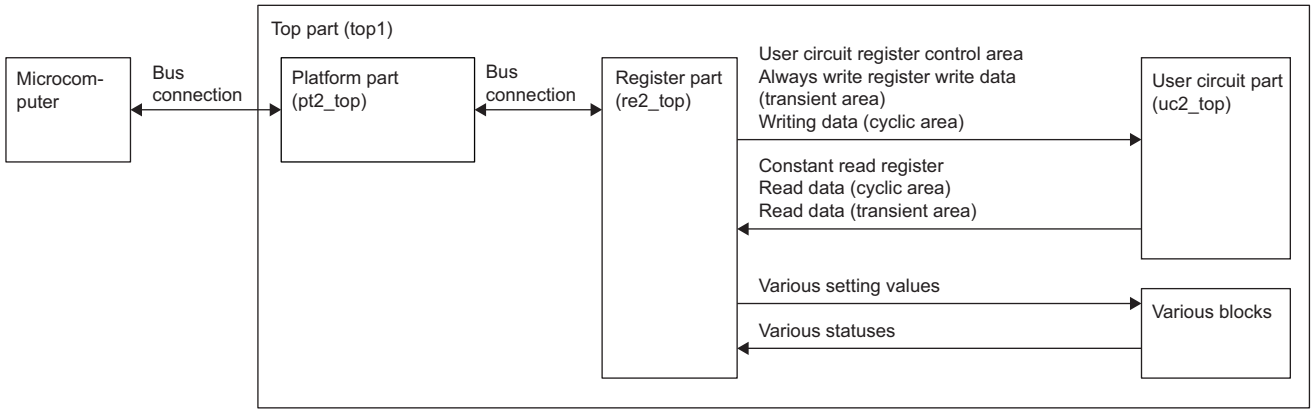
IOB0 to 2_UNIT[3:0]	Connection circuit board
0001b	DC input/output circuit board
0010b	Differential input/output circuit board

- Extension module connection circuit board

IOE_UNIT[4:0]	Connector (E0)	Connector (E1)	Connector (E2)
0_0001b	DC input/output circuit board	DC input/output circuit board	DC input/output circuit board
0_0010b	Differential input/output circuit board	Differential input/output circuit board	Differential input/output circuit board
0_0011b	Analog input/output circuit board	Analog input/output circuit board	Analog input/output circuit board
0_1111b	No connection circuit board	No connection circuit board	No connection circuit board

Register part (re2_top)

This block notifies the setting values inside the FPGA via the platform part from the MCU.



■Function List

Item	Operation
Notification of setting values to user circuit block	Notifies the user circuit block of the setting values (user circuit register control area, constant write area, write data (transient area), write data (cyclic area)) from the MCU.
Loading status information from user circuit block	Notifies the MCU of the status in the user circuit block (constant read area, read data (cyclic area), read data (transient area)).
Notification of setting values to each block	Notifies each block of the setting value notified from the MCU.
Loading status information of each block	Notifies the MCU of the status in each block.

■Connection and setting value notification timing

The connection between the register part and the user circuit block, and the setting value notification timing are shown below.

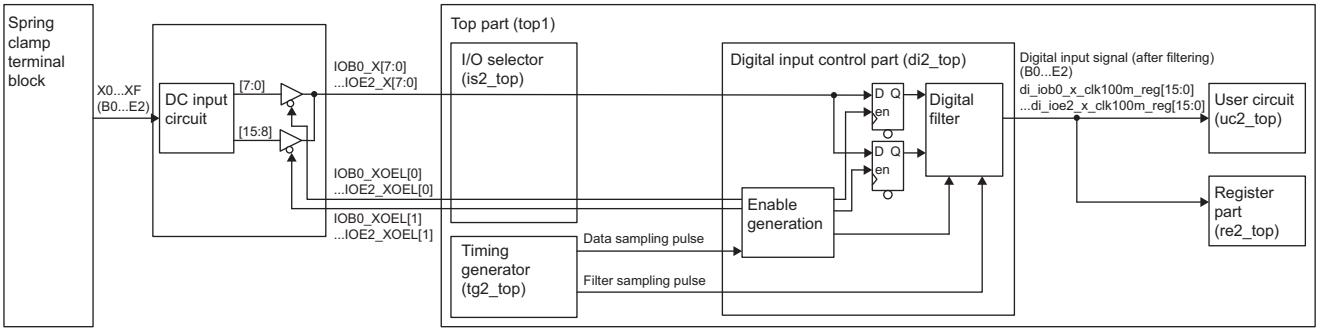
FPGA address	Register name	Register overview	User circuit signal name	Setting value notification timing
1000_A000H	usr_wrdat_ctrl	Write/read data control register	No connection	—
1000_A002H	usr_logmode_sel	User circuit logging mode selection	re_rs_usr_logmode_sel_1_0_clk100m_reg	Constant notification
1000_A004H	usr_micon_syserr	MCU system error notification	re_rd_usr_micon_syserr_clk100m_reg	Constant notification
1000_0010H to 1000_A02FH	usr_alwreg_00 to usr_alwreg_0F	Always write register	re_rs_usr_alwreg_00_clk100m_reg to re_rs_usr_alwreg_00_clk100m_reg	Constant notification
1000_A030H to 1000_A04FH	usr_alrreg_00 to usr_alrreg_0F	Always read register	uc_rs_usr_alrreg_00_clk100m_reg to uc_rs_usr_alrreg_0f_clk100m_reg	Constant notification
1000_B000H to 1000_B2FFH	usr_wreg_000 to usr_wreg_17F	Write data (transient area)	re_rs_usr_wreg_000_clk100m_reg to re_rs_usr_wreg_17f_clk100m_reg	When 1 is set to Write/read data control register [0]
1000_B300H to 1000_B3FFH	usr_wreg_180 to usr_wreg_1FF	Writing data (cyclic area)	re_rs_usr_wreg_180_clk100m_reg to re_rs_usr_wreg_1ff_clk100m_reg	When 1 is set to Write/read data control register [1]
1000_B800H to 1000_BAFFH	usr_rreg_000 to usr_rreg_17F	Read data (transient area)	uc_rs_usr_rreg_000_clk100m_reg to uc_rs_usr_rreg_17f_clk100m_reg	When 1 is set to Write/read data control register [8]
1000_BB00H to 1000_BBFFH	usr_rreg_180 to usr_rreg_1FF	Read data (cyclic area)	uc_rs_usr_rreg_180_clk100m_reg to uc_rs_usr_rreg_1ff_clk100m_reg	When 1 is set to Write/read data control register [9]

Module specific circuit (NZ2GN2S-D41P01)

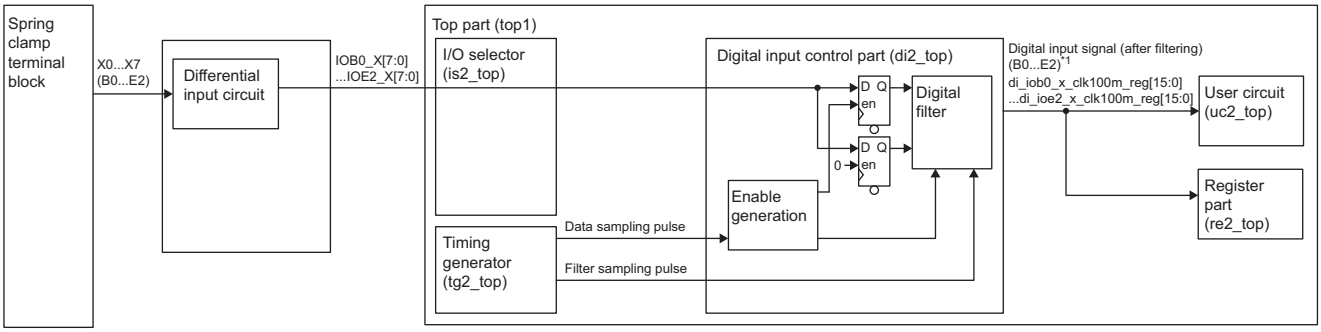
Digital input control part (di2_top)

The input signal from the input/output selector is loaded into the digital input control part.

For the DC input circuit board, the 16-bit digital signal is multiplexed into the lower 8 bits and the upper 8 bits on the DC input/output circuit board, and loaded in units of 8 bits into the digital input control part.



For the differential input/output circuit board, only 8 bits are loaded. To reduce the external noise of the loaded input signal, it is output to the user circuit block via a digital filter.



*1 [15:8] is fixed to 0.

■Function List

Item	Operation	Remarks
Demultiplexer module	■Demultiplexing circuit Demultiplexes data multiplexed outside the FPGA and generates DC input output enable (IOB/Ex_XOEL[1:0]) for the tri-state buffer outside the FPGA.	The timing for multiplexing and demultiplexing is set by the data sampling timing (B0 to E2). Also, for DC input/output, the data sampling pulse setting needs to be set to 0.1μs or more.
Digital filter	■Digital filter circuit The digital filter implements a 12-bit up/down counter, and the filter time can be changed by setting the register areas below. • Filter sampling pulse • Input filter counter upper limit ■Filter time formula Filter time = Filter sampling pulse*1 × Input filter counter upper limit For the outline operation of the digital filter, refer to the following. ☞ Page 197 Digital filter	The filter sampling pulse is set by the filter sampling pulse (B/E0 to E2). The input filter counter upper limit is set by the input filter counter upper limit upper (IOB0_X0 to IOE0_XF). Also, set the filter sampling pulse to the same setting as the data sampling pulse. For details on the FPGA register areas, refer to the following. ☞ Page 502 FPGA register

*1 The data sampling pulse can be selected as the filter sampling pulse according to the register setting value.

■Monitor register

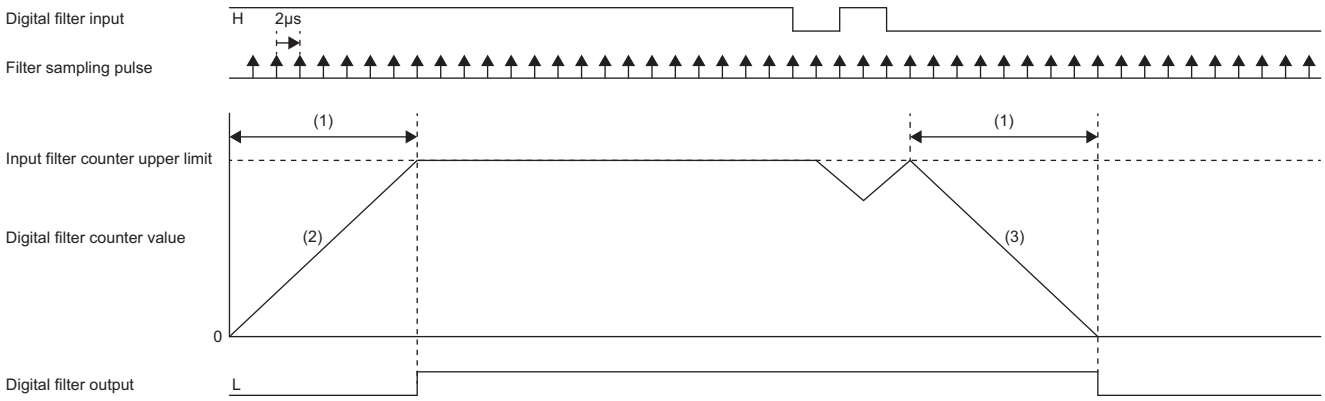
For the monitor register of the digital input control part, refer to the following.

☞ Page 504 Digital input control part

■Digital filter

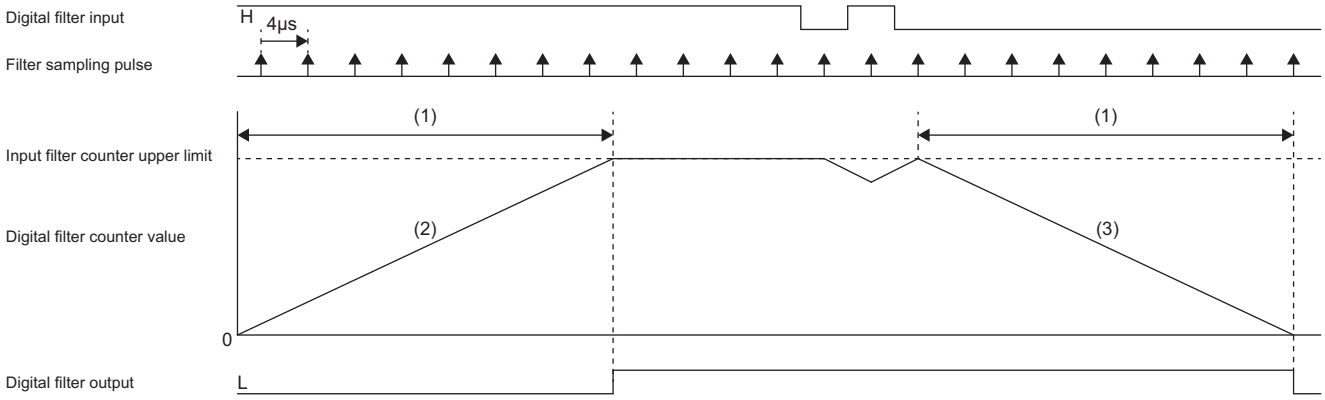
A conceptual diagram of a digital filter is shown below. For the filter time, the input filter counter upper limit (IOB/E□_X□) and filter sampling pulse (B/E□) can be set.

- Filter sampling pulse: 2μs



(1) Filter time
(2) Count-up
(3) Countdown

- Filter sampling pulse: 4μs



(1) Filter time
(2) Count-up
(3) Countdown

■Filter time

Recommended values for the filter time are shown below.

Circuit board type	Register		
	Data sampling timing (B/E0 to E2)	Filter sampling pulse (B/E0 to E2)	Input filter counter upper limit (IOB/E0 to E2_X0 to EF) (B/E0 to E2)
DC input/output circuit board	9H(100ns)	FH (data sampling timing)	AH
Differential input/output circuit board (differential input)	0H(10ns)	0H(10ns)	5H
Differential input/output circuit board (differential input/output)	0H(10ns)	0H(10ns)	6H

■Timing chart

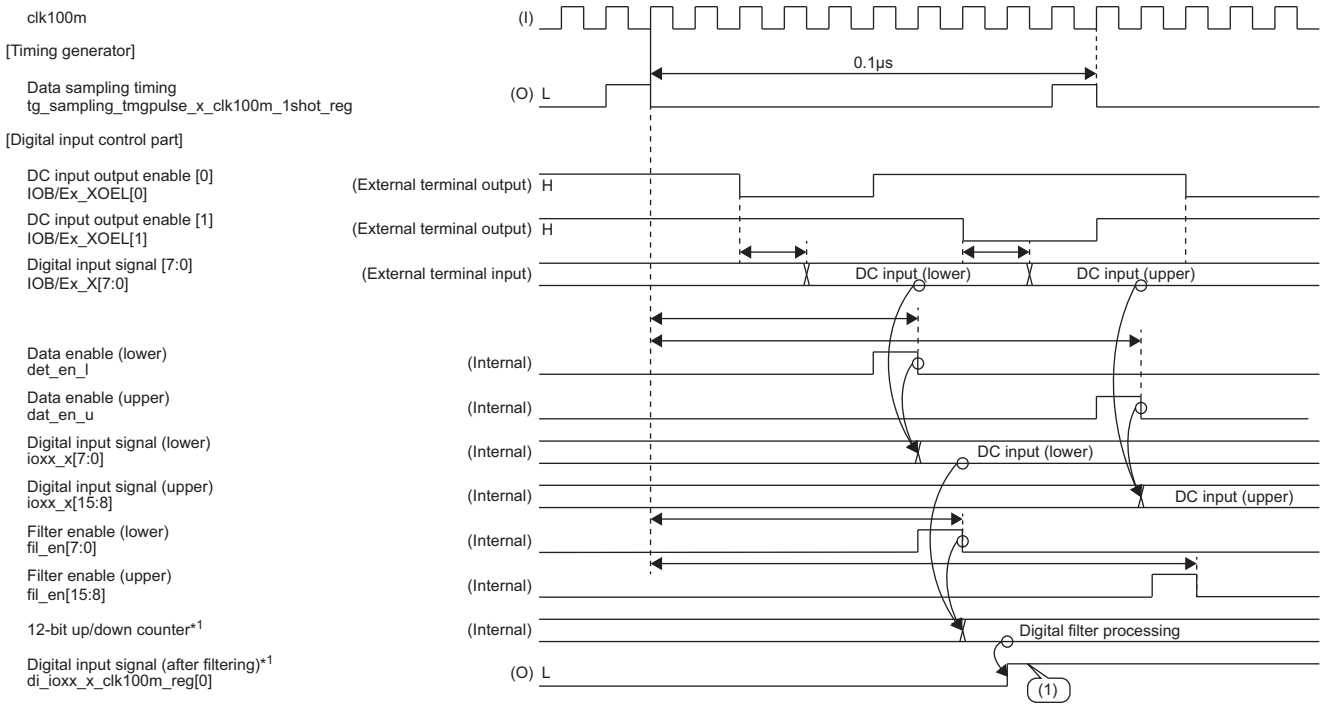
The selection of the timing pulse of the digital filter differs between the DC input/output circuit board and the differential input/output circuit board.

The DC input/output circuit board performs digital filtering in synchronization with the data sampling timing.

The differential input/output circuit board sets the filter sampling pulse, generates the timing pulse, and implements the digital filter. The timing chart of the digital input control part is shown below.

• DC input/output circuit board

Filter sampling pulse setting register: FH

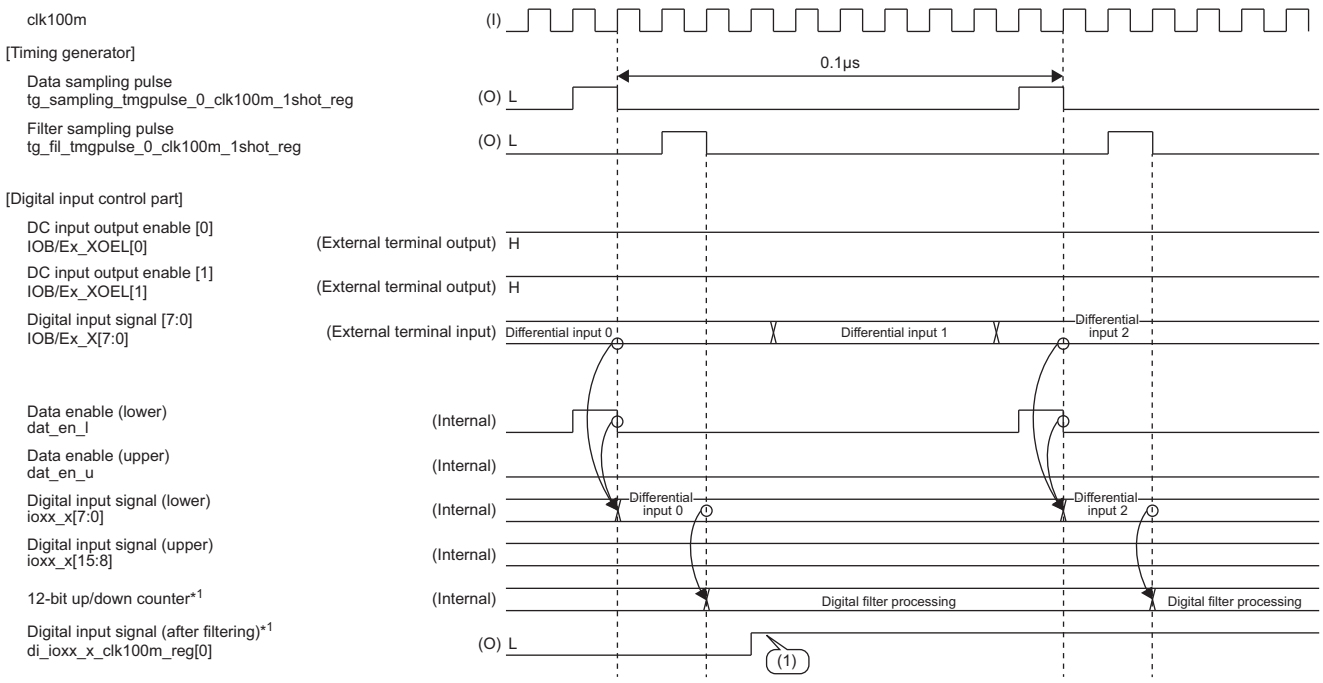


(1) After match comparison, output in one level of FF.

*1 1 bit is indicated. [15:1] has the same process.

• Differential input/output circuit board

Filter sampling pulse setting register: Other than FH



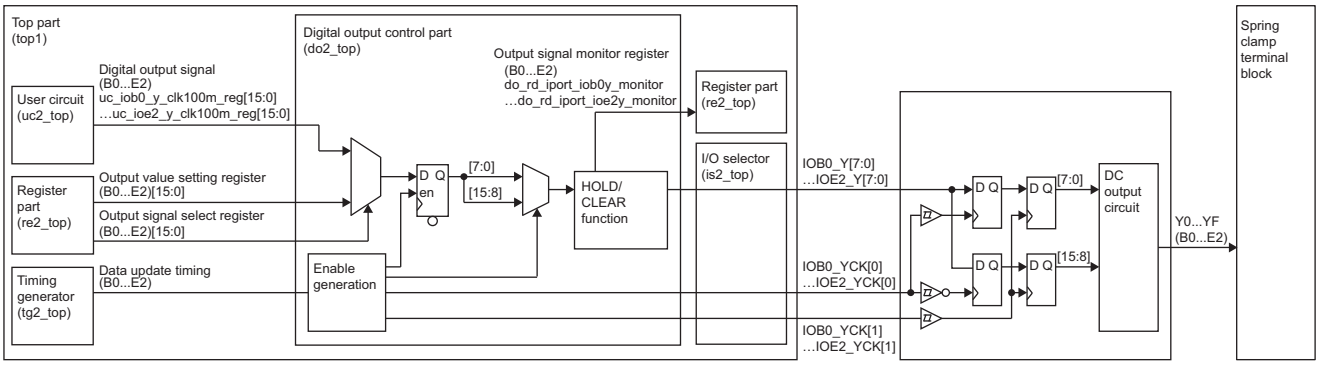
(1) After match comparison, output in one level of FF.

*1 1 bit is indicated.

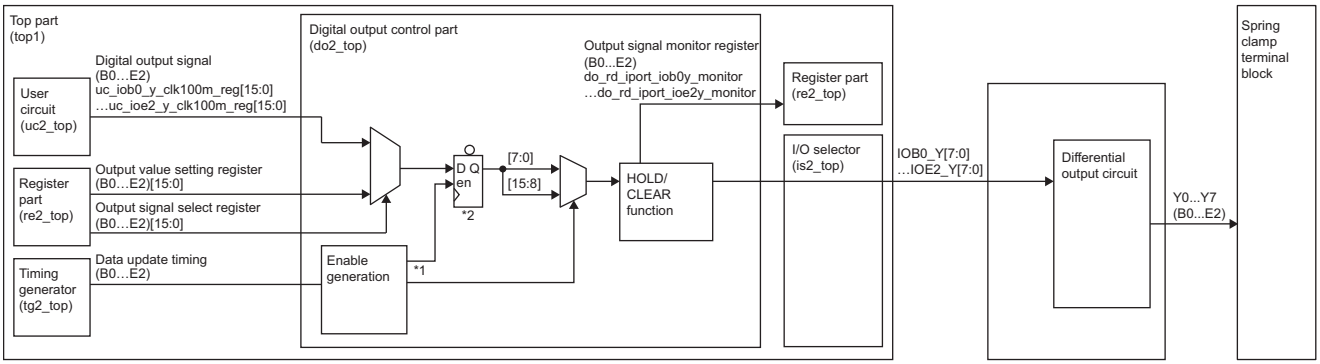
Digital output control part (do2_top)

A digital signal in the user circuit block or register part is selected by output signal selection register, and the digital signal is output to the outside of the FPGA via the input/output selector. The output timing is synchronized with the timing pulse signal from the timing generator.

For the DC input/output circuit board, the digital signal (16 bits) is multiplexed, output to the outside of the FPGA in the order of the lower 8 bits and then the upper 8 bits, and demultiplexed outside the FPGA. Output occurs when data is updated.



The differential input/output circuit board outputs an 8-bit digital signal when data is updated.



*1 Select and output only [7:0].

*2 Through output occurs when the internal operation start/stop is Stop.

Also, with the use of the register setting, the digital output signal output immediately before the internal operation stopped can be held (HOLD) or cleared (CLEAR).

■Function List

Item	Operation	Remarks
Digital signal selection	■Digital signal selection circuit The digital signal to be output is selected from the digital signal [15:0] of the user circuit block and the output value setting register (B□) or output value setting register (E□) [15:0] according to the setting of the output signal selection (B□) or output signal selection (E□), and the selected digital signal is output.	—
Multiplexer module	■Multiplex circuit In addition to multiplexing digital signals for demultiplexing outside the FPGA, it generates DC output enable (IOB/E□_YCK[1:0]) for loading digital signals outside the FPGA.	The timing to perform demultiplexing and multiplexing is set by data update timing (B0 to B2) and data update timing (E0 to E2). For DC input/output circuit board, the cycle interval of data sampling pulse needs to be 0.1μs or more.

Item	Operation	Remarks
HOLD/CLEAR function	■HOLD/CLEAR circuit By the register setting, HOLD/CLEAR is executed when the internal operation stops. The HOLD/CLEAR processing for each circuit board is shown below. • DC input/output circuit board When CLEAR is set: The board outputs the digital signal values with all 0.*1 When HOLD is set: The digital signal is held. • Differential input/output circuit board When CLEAR is set: The board selects all 0 or all 1 according to the register setting value and outputs the digital signal values with the selected ones. When HOLD is set: The digital signal is held.	HOLD/CLEAR for the DC input/output circuit board sets the external reset ON/OFF setting. HOLD/CLEAR for differential input/output circuit board sets the differential output HOLD/CLEAR (B0 to B2, E0 to E2). For details, refer to the following. ☞ Page 315 FPGA Control Function

*1 Issue the FPGA external reset (IOB0_RSTL, IOB1_RSTL, IOB2_RSTL, IOE_RSTL) to reset the FPGA external circuit.

■Monitor register

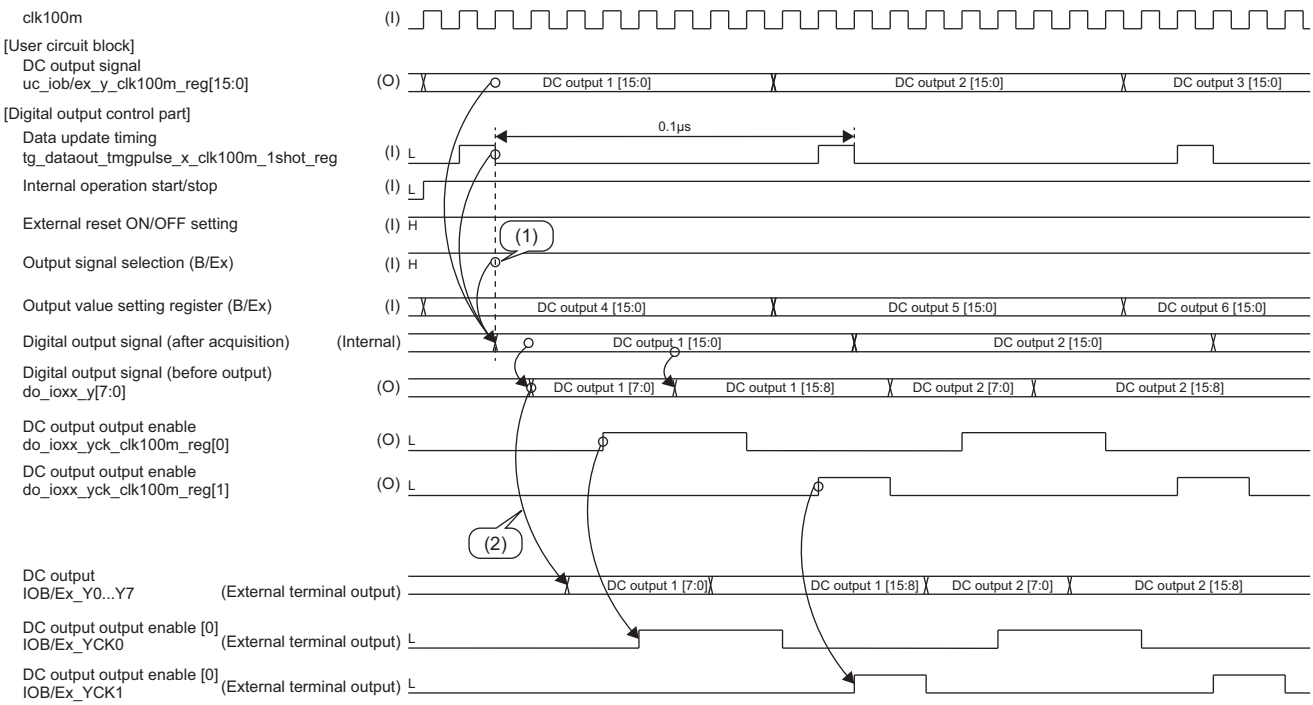
For the monitor register of the digital output control part, refer to the following.

☞ Page 506 Digital output control part

■Operation

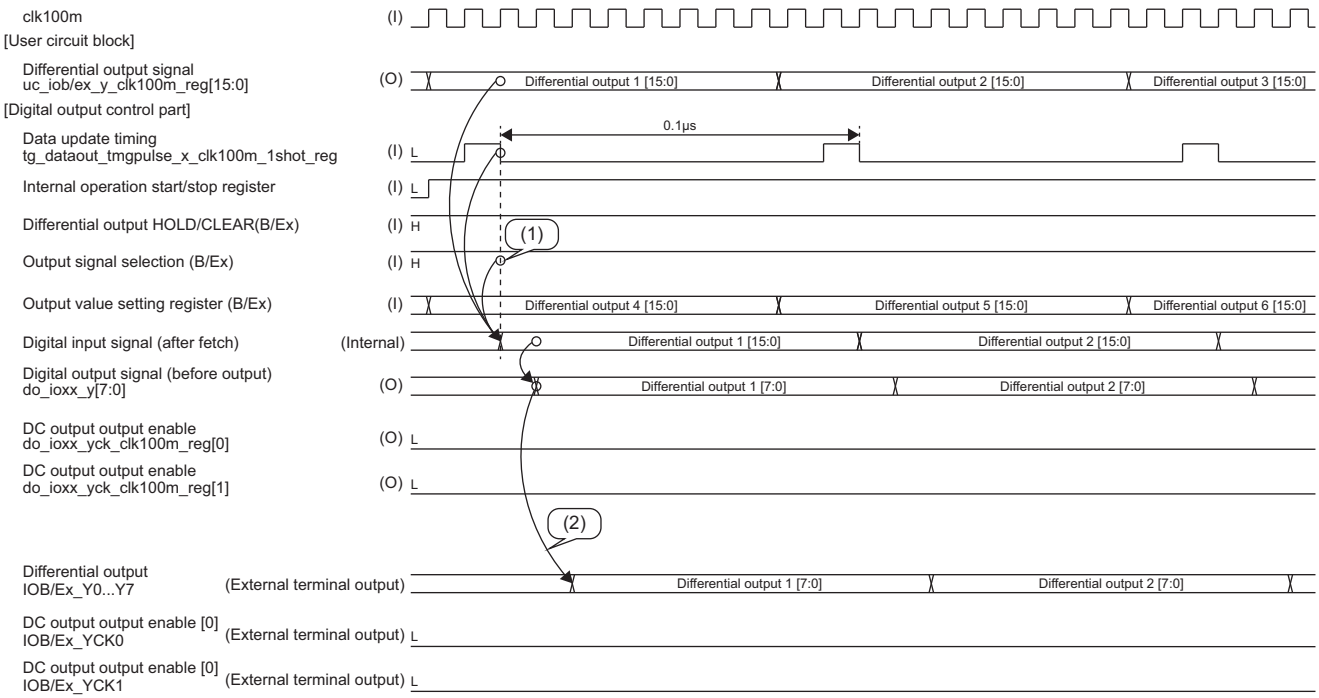
The output timing of the digital output control part varies depending on the DC input/output circuit board and the differential input/output circuit board. A timing chart is shown below.

- DC input/output circuit board



(1) By setting the output signal selection register, select the digital input from the user circuit block and register part, and load it into the digital output control part.
(2) Output to external terminal in one level of FF.

- Differential input/output circuit board



(1) By setting the output signal selection register, select the digital input from the user circuit block and register part, and load it into the digital output control part.
(2) Output to external terminal in one level of FF.

Module specific circuit (NZ2GN2S-D41D01)

Digital input control part (di2_top)

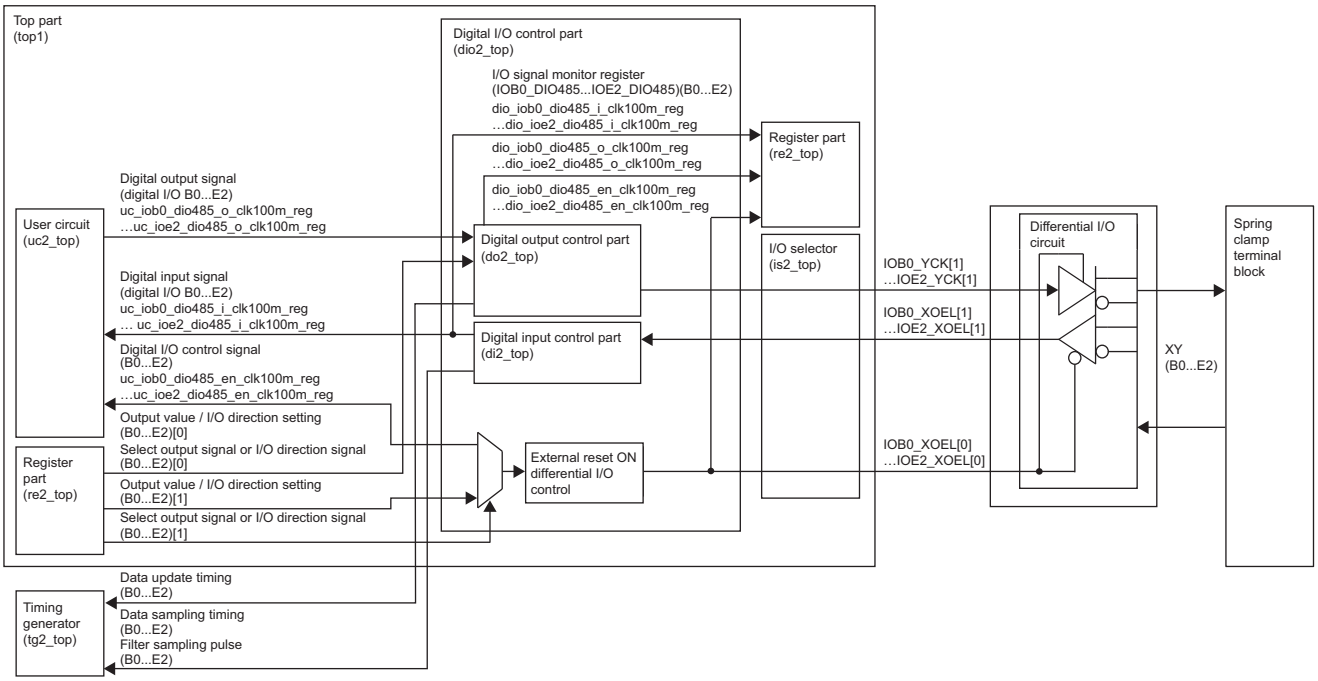
Same as NZ2GN2S-D41P01 (☞ Page 196 Digital input control part (di2_top))

Digital output control part (do2_top)

Same as NZ2GN2S-D41P01 (☞ Page 199 Digital output control part (do2_top))

Digital input/output control part (dio2_top)

Controls the bi-directional buffer when a differential input/output circuit board is connected. It generates the 1-bit bidirectional buffer digital input signal, digital output signal, and input/output direction signal that controls the digital input/output.
The digital input signal and digital output signal have the same functions as the digital input control part and digital output control part. The input/output direction signal that controls digital input/output selects and outputs the signal in the user circuit block or the register part.



■Function List

Item	Operation
Digital input	Same as the digital input control part
Digital output	Same as the digital output control part
Digital input/output control	■Digital input/output control circuit According to the setting values of output signal/input output direction signal selection (B0) to output signal/input output direction signal selection (B2), and output signal/input output direction signal selection (E0) to output signal/input output direction signal selection (E2), this function selects and outputs the user circuit block digital output or the register part output. Also, the external reset ON/OFF setting controls the input/output of the differential input/output circuit when the internal operation start/stop is Stop(0). • When the external reset ON/OFF setting is set to ON: Outputs with 0 fixed. (The differential input/output circuit is fixed to the input direction.) • When the external reset ON/OFF setting is set to OFF: Outputs the signal selected by the setting value of the output signal or I/O direction signal selection (B0 to E2).

■List of monitor register areas

Register name	Connection signal name
I/O signal monitor (IOB0_DIO485)B0) (ioport_iob0_dio485_monitor)	dio_iob0_dio485_i_clk100m_reg dio_iob0_dio485_o_clk100m_reg dio_iob0_dio485_en_clk100m_reg
I/O signal monitor (IOB1_DIO485)B1) (ioport_iob1_dio485_monitor)	dio_iob1_dio485_i_clk100m_reg dio_iob1_dio485_o_clk100m_reg dio_iob1_dio485_en_clk100m_reg
I/O signal monitor (IOB2_DIO485)B2) (ioport_iob2_dio485_monitor)	dio_iob2_dio485_i_clk100m_reg dio_iob2_dio485_o_clk100m_reg dio_iob2_dio485_en_clk100m_reg
I/O signal monitor (IOE0_DIO485)E0) (ioport_ioe0_dio485_monitor)	dio_ioe0_dio485_i_clk100m_reg dio_ioe0_dio485_o_clk100m_reg dio_ioe0_dio485_en_clk100m_reg
I/O signal monitor (IOE1_DIO485)E1) (ioport_ioe1_dio485_monitor)	dio_ioe1_dio485_i_clk100m_reg dio_ioe1_dio485_o_clk100m_reg dio_ioe1_dio485_en_clk100m_reg
I/O signal monitor (IOE2_DIO485)E2) (ioport_ioe2_dio485_monitor)	dio_ioe2_dio485_i_clk100m_reg dio_ioe2_dio485_o_clk100m_reg dio_ioe2_dio485_en_clk100m_reg

If the external wiring of the differential input/output circuit board is disconnected, the input signals dio_iob0_dio485_i_clk100m_reg to dio_ioe2_dio485_i_clk100m_reg become H(1). Also, the input signals dio_iob0_dio485_i_clk100m_reg to dio_ioe2_dio485_i_clk100m_reg in the output direction become H(1).

Module specific circuit (NZ2GN2S-D41PD02)

Digital input control part (di2_top)

Same as NZ2GN2S-D41P01 (☞ Page 196 Digital input control part (di2_top))

Digital output control part (do2_top)

Same as NZ2GN2S-D41P01 (☞ Page 199 Digital output control part (do2_top))

Digital input/output control part (dio2_top)

Same as NZ2GN2S-D41D01 (☞ Page 202 Digital input/output control part (dio2_top))

Module specific circuit (NZ2EX2S-D41P01)

Digital input control part (di2_top)

Same as NZ2GN2S-D41P01 (☞ Page 196 Digital input control part (di2_top))

Digital output control part (do2_top)

Same as NZ2GN2S-D41P01 (☞ Page 199 Digital output control part (do2_top))

Module specific circuit (NZ2EX2S-D41D01)

Digital input control part (di2_top)

Same as NZ2GN2S-D41P01 (☞ Page 196 Digital input control part (di2_top))

Digital output control part (do2_top)

Same as NZ2GN2S-D41P01 (☞ Page 199 Digital output control part (do2_top))

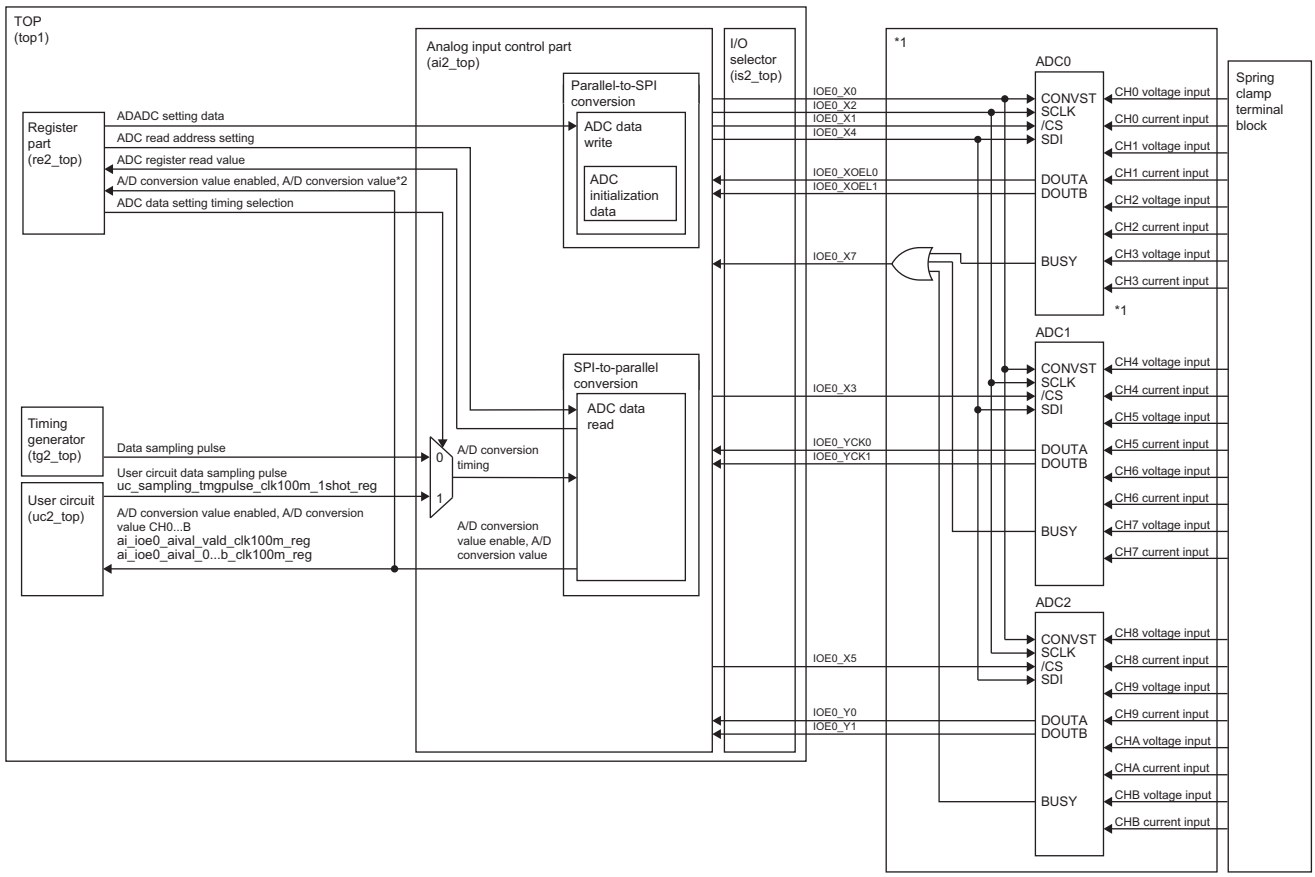
Digital input/output control part (dio2_top)

Same as NZ2GN2S-D41D01 (☞ Page 202 Digital input/output control part (dio2_top))

Module specific circuit (NZ2EX2S-D41A01)

Analog input control part (ai2_top)

When E0 to E2 are analog input/output circuit boards, it controls the ADC (three elements on one circuit board). Communication with the ADC uses SPI (Serial Peripheral Interface). In addition, the serial clock output and serial data output signals are common and the chip select signal is used to control ADC0 to ADC2 individually. ADC register write and read are sequentially controlled to ADC0, ADC1, and ADC2. A/D conversion controls ADC0 to ADC2 in parallel.



*1 It becomes an analog input/output circuit board. It is described in IOE0. IOE1 and IOE2 have the same structure.

*2 ai_ioe0_aival_0 to b_clk100m_reg

■Function List

Item	Operation	Remarks
A/D conversion enable/disable	Sets whether to enable or disable A/D conversion for each circuit board.	—
ADC setting	■ADC setting circuit After setting the A/D conversion enable/disable setting to Enable(1), set the ADC (rewrite all ADC register areas). The following functions can be used depending on the ADC setting. • ADC range setting: Sets the analog input range. • ADC offset: Outputs the A/D conversion value with the ADC offset value added/subtracted. • ADC oversampling ratio setting: After the data sampling pulse is input, the results of sampling by multiples of the ADC oversampling ratio setting are averaged and output as A/D conversion value.	The processing indicated on the left is performed at the rising edge of the A/D conversion enable/disable setting.
A/D conversion processing	■A/D conversion cycle The conversion cycle timing pulse can be selected from the user circuit block or data sampling timing by A/D conversion timing selection. • A/D conversion value: Outputs to the user circuit block and register part. The A/D conversion value is output in 2's complement. • A/D conversion start: After ADC initialization end, A/D conversion is started by writing 1 to the A/D conversion start register.	When A/D conversion enable/disable setting (A/D conversion enable/disable setting (E0 to E2)) is set to Enable, the A/D conversion enable/disable setting (A/D conversion start E0 to E2) is set to Start. After that, A/D conversion processing is performed. The A/D conversion cycle is set by the data sampling timing (B0) to data sampling timing (B2) and data sampling timing (E0) to data sampling timing (E2) of the timing control part.

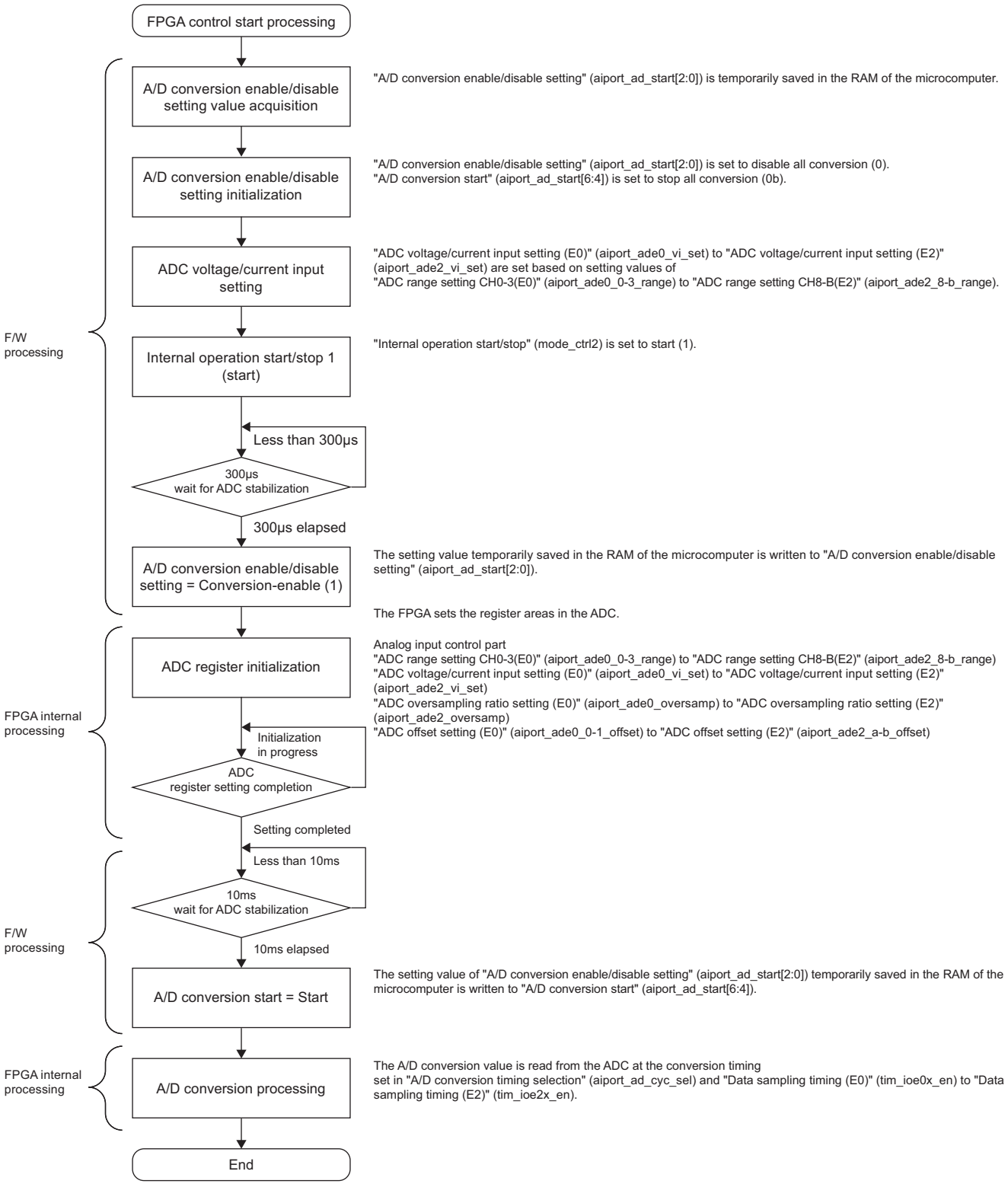
■Monitor register

For information on the monitor register of the analog input control part, refer to the following.

☞ Page 507 Analog input control part

■Process

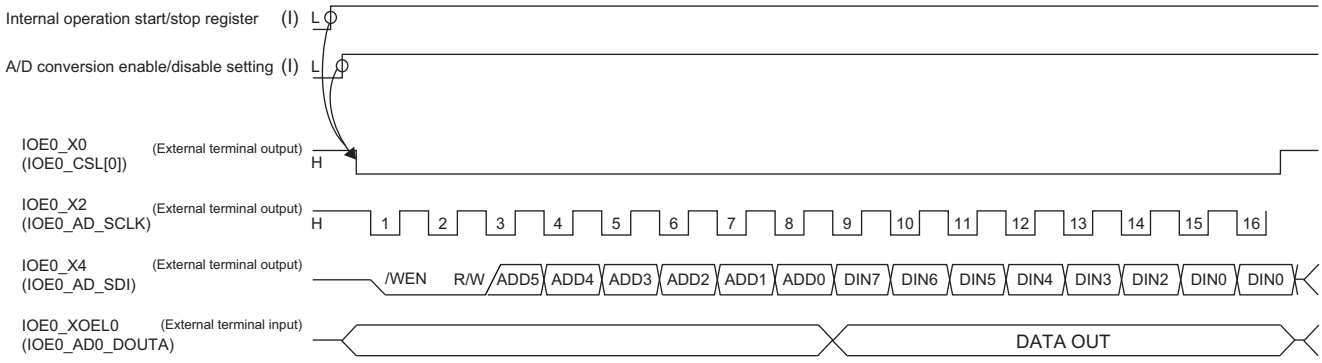
The analog input control part performs the following processing.



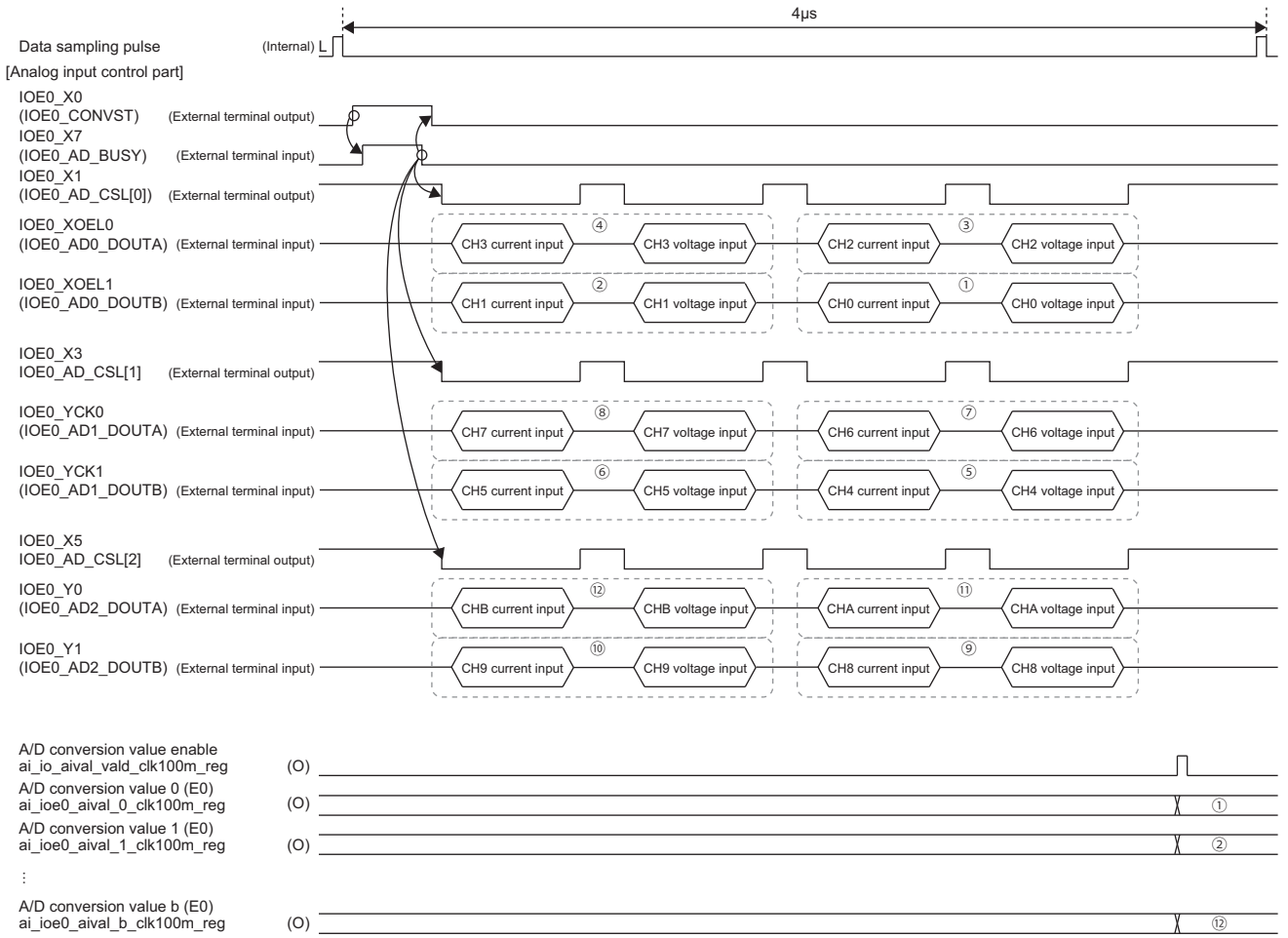
■Operation

The analog input control part performs the ADC register settings, ADC register initialization and ADC register setting end, and A/D conversion processing that reads A/D conversion values from the ADC. ADC register initialization and ADC register setting end set register areas in the ADC when the internal operation start/stop is Start and A/D conversion enable/disable setting is set to Enable (1). For A/D conversion processing, by setting the A/D conversion start to Start(1), the A/D conversion value is read from the ADC in synchronization with the data sampling pulses that are input at constant cycle from the timing generator. Both current and voltage A/D conversion values are input from the ADC, and A/D conversion values set by the ADC range setting (aiport_ade0_0-3_range to aiport_ade2_8-b_range) are output to the user circuit block. The analog input control part outputs the 12-bit A/D conversion values (ai_ioe0_aival_0_clk100m_reg to ai_ioe0_aival_b_clk100m_reg) to the user circuit block at the same time as the A/D conversion value enable (ai_io_aival_vald_clk100m_reg). The A/D conversion value connected to the FPGA is a 16-bit 2's complement.

• ADC register initialization, ADC register end



• A/D conversion processing



■Configurable functions

The configurable functions of the ADC are shown below.

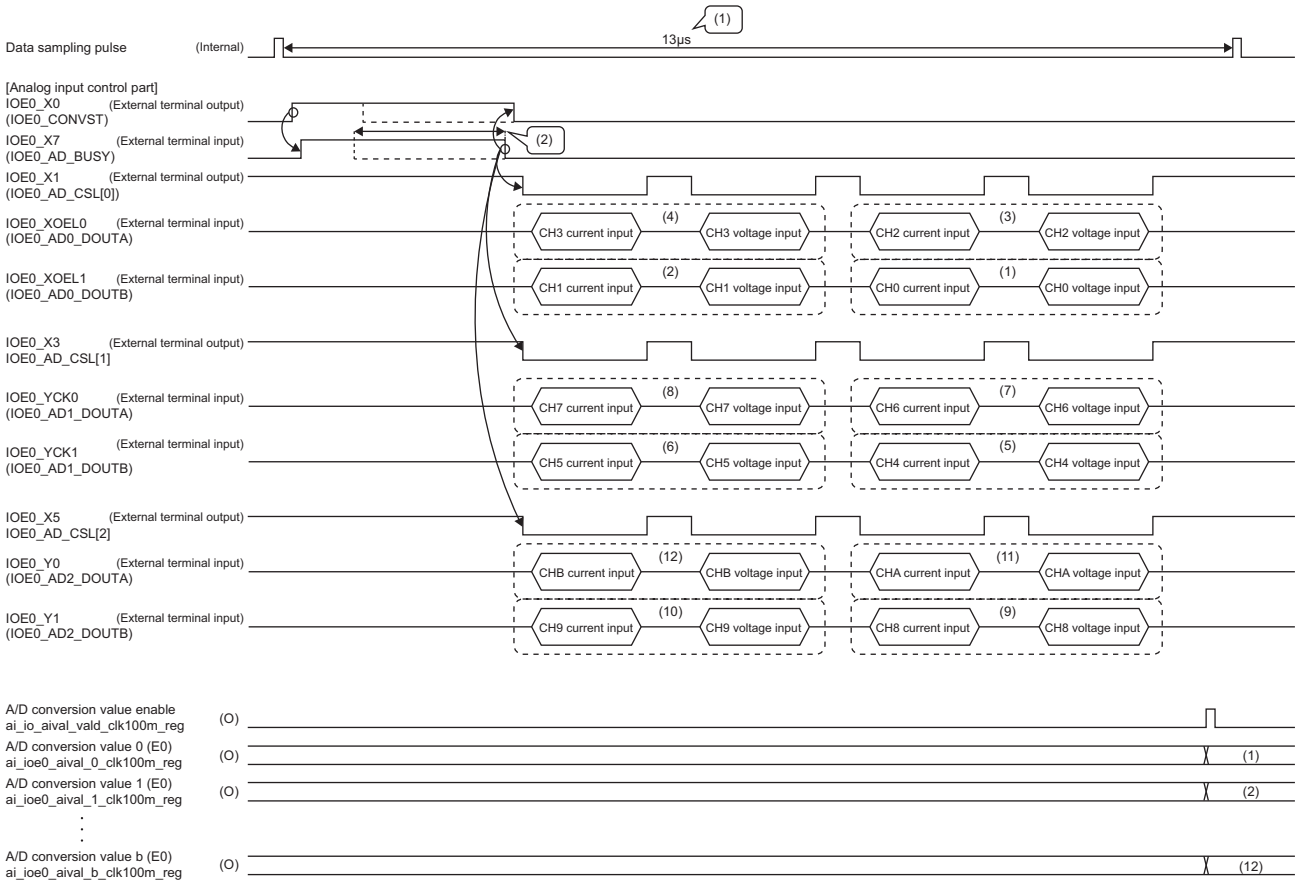
- Oversampling function
- Offset function

■Oversampling function

The ADC oversampling function performs digital averaging. Digitally averaging applies to the amount equal to the number of times set in "ADC oversampling ratio setting". Therefore, the falling edge timing of the IOE0 to E2_AD_BUSY signals is delayed by the amount of time to execute digital averaging. The following shows the timing chart when "ADC oversampling ratio setting" is set and the restriction on the minimum cycle interval of data sampling pulses.

Ex.

When "ADC oversampling ratio setting" is set to "8x"



(1) ADC oversampling ratio setting: For 8x, set the data sampling timing so that the interval is 13µs or more.

(2) The setting of the ADC oversampling ratio setting register delays the IOE0_AD_BUSY signal because A/D conversion is performed eight times. Get the average value of the 8 times as A/D conversion value.

ADC oversampling ratio setting	Data sampling timing minimum cycle interval constraint
No Setting	4µs
2×	6µs
4×	8µs
8×	13µs
16×	24µs
32×	44µs
64×	84µs
128×	165µs
256×	328µs

■Offset function

Offset errors caused by external factors of ADC can be compensated by the ADC offset value for each channel.
Regarding the ADC offset setting value CH0 to 1 (E0) (aiport_ade0_0-1_offset) (FPGA register address: 1000_6160H) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset) (FPGA register address: 1000_6182H), depending on their settings, up to 128 resolutions can be automatically added or subtracted for each channel.
The resolution for the ADC input current range and input voltage range is shown below.

ADC range setting CH0 to CHB (E0 to E2)	Resolution
-9.9 to 9.9V	305μV
-19.8 to 19.8mA	0.610μA

The formula for calculating the analog input value is shown below.

- Analog input value = Resolution × (Digital input for A/D conversion + ADC offset value)

The ADC offset value is the offset binary set at ADC offset setting value CH0 to 1 (E0) (aiport_ade0_0-1_offset) (FPGA register address: 1000_6160H) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset) (FPGA register address: 1000_6182H) (Initial value: 80H)

■ADC offset value

Regarding the ADC offset setting value CH0 to 1 (E0)(aiport_ade0_0-1_offset) (FPGA register address: 1000_6160H) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset) (FPGA register address: 1000_6182H), the ADC offset values for the values set in them are shown below.

Regarding the ADC offset setting value CH0 to 1 (E0) (aiport_ade0_0-1_offset) (FPGA register address: 1000_6160H) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset) (FPGA register address: 1000_6182H)	ADC offset value (setting value from FPGA Module Configuration Tool)
00H	-128
01H	-127
⋮	⋮
80H	0
81H	1
⋮	⋮
FFH	127

Ex.

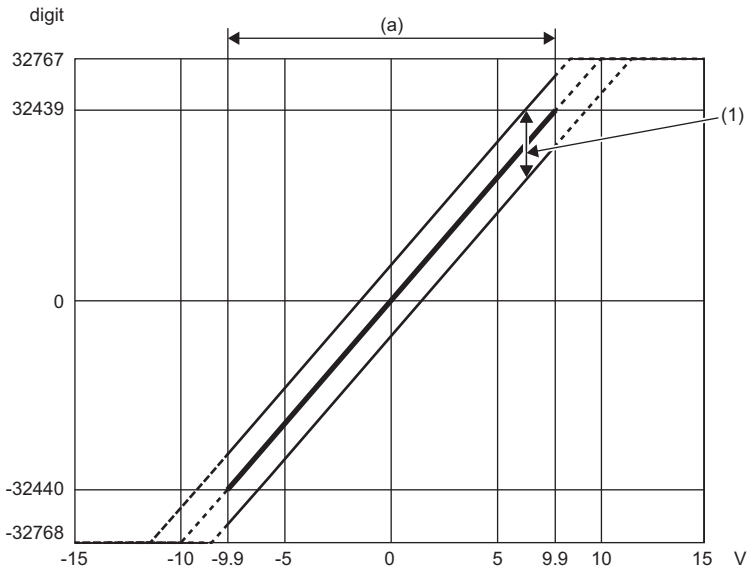
Regarding the ADC range setting CH0 to 3 (E0) (aiport_ade0_0-3_range) (FPGA register address: 1000_6100H) to ADC range setting CH8 to B (E2) (aiport_ade2_8-B_range) (FPGA register address: 1000_6110H), if their setting is ±9.9V with 9mV offset error, for the ADC offset setting value CH0 to 1 (E0) (aiport_ade0_0-1_offset) (FPGA register address: 1000_6160H) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset) (FPGA register address: 1000_6182H), set them to 62H.

- Set 80H-1EH(9mV)=305μV×-30=62H.

■I/O conversion characteristics using the offset function

The I/O conversion characteristics using the offset function are shown below. Slope characteristics and scaling are not possible with the standard circuit. Add them in the user circuit block if necessary.

Use them within the practical analog input range. If a value is out of the range, the maximum resolution and accuracy may not fall within the range of performance specifications. (Avoid using the dotted line section of the graph.)



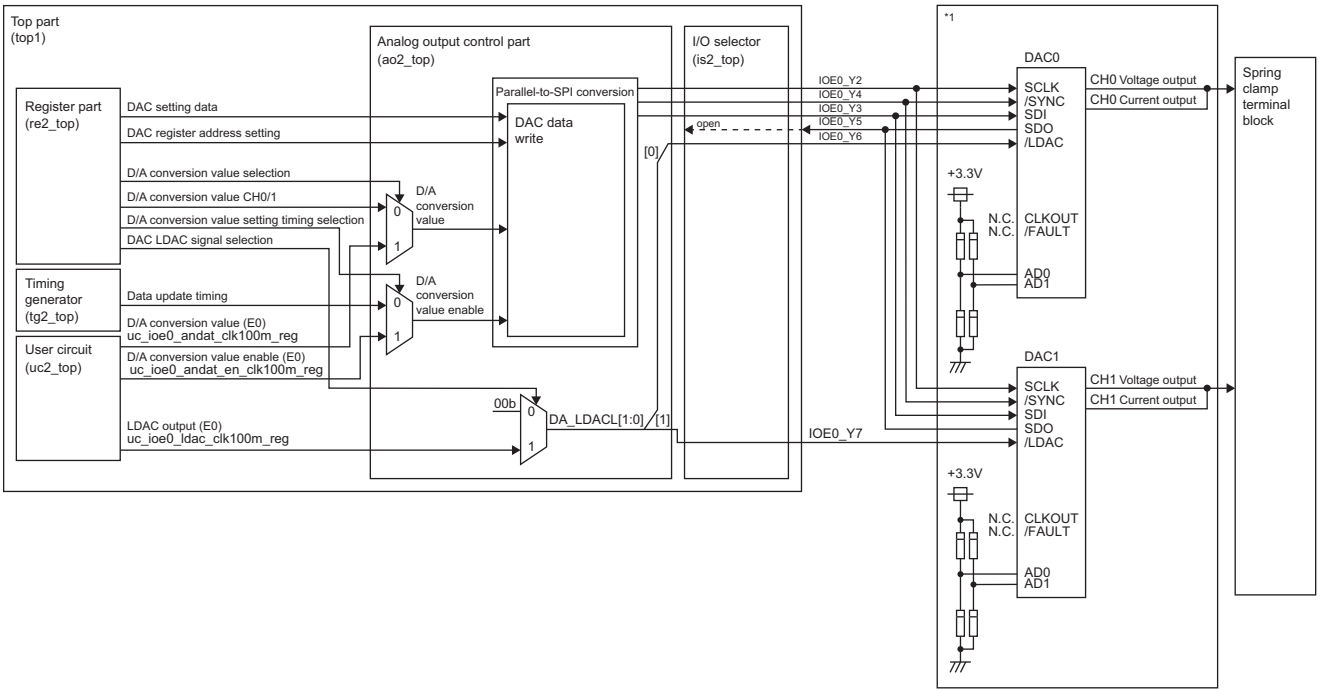
digit: A/D conversion value
V: Analog input voltage (V)
(1) Offset value
(a) Practical analog input range

Analog output control part (ao2_top)

If E0 to E2 are analog input/output circuit boards, it controls the DAC (two elements on one circuit board). Communication with the DAC uses SPI (Serial Peripheral Interface).

In addition, the serial clock output, serial data output signal, and chip select signal are common, and an address (2 bits) for each chip is used to control the DAC individually.

Synchronization between channels can be performed by controlling the /LDAC signal with the user circuit block.



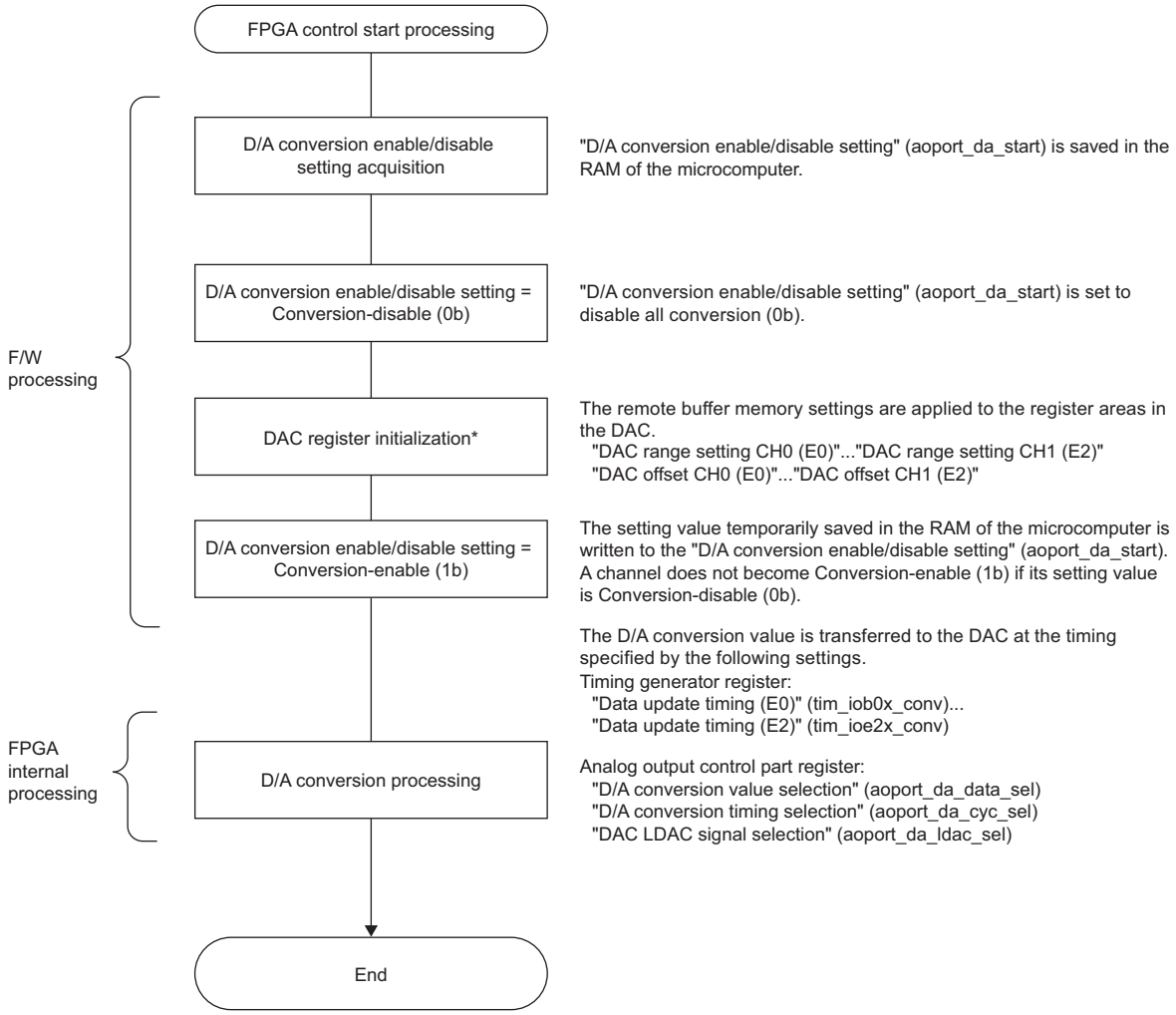
*1 This is an analog input/output circuit board. It is described in IOE0. IOE1 and IOE2 have the same structure.

■Function List

Item	Operation	Remarks
D/A conversion enable/ disable	Enable/disable D/A conversion for each channel.	—
DAC setting	■DAC setting circuit Set the DAC (set the register inside the DAC).	F/W controls the DAC setting circuit during the FPGA control start processing.
D/A conversion processing	■D/A conversion cycle The D/A conversion cycle timing pulse can be selected from "User circuit output" or "Data update timing" by "Select D/A conversion timing". ■D/A conversion value D/A conversion value can be selected from "User circuit output" or "Register setting value" by "Select D/A conversion value". (The D/A conversion value is output in offset binary.) ■LDAC signal selection Control of the /LDAC signal by the user circuit block can be enabled or disabled (fixed to low).	D/A conversion processing is performed when "D/A conversion enable/disable setting" is enabled. The D/A conversion cycle is set by "Data update timing".

■Processing flow

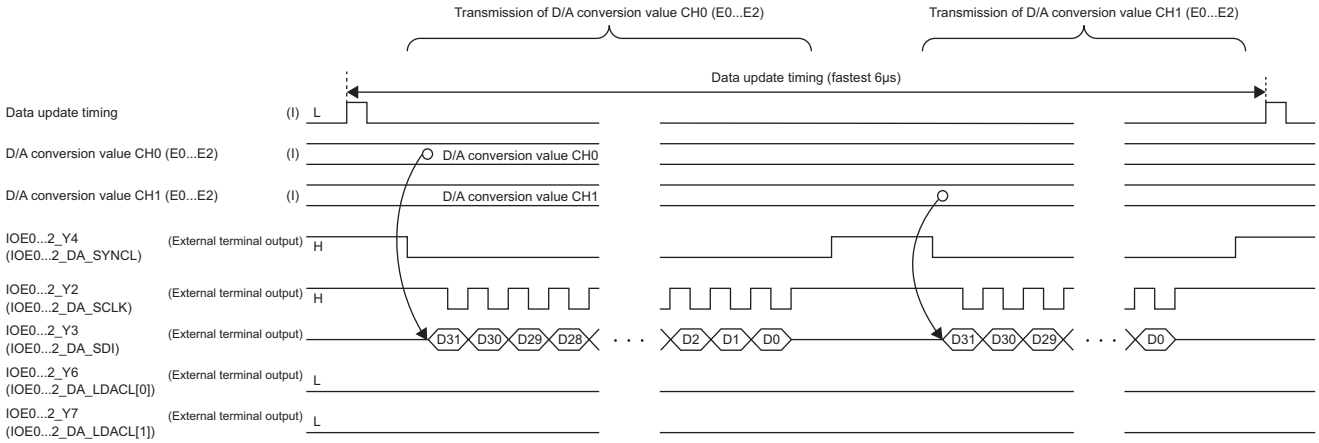
The processing flow of the analog output control part is shown below. From the MCU, set the analog output control part register mounted on the FPGA. After setting the analog output control register, transfer the D/A conversion value to the DAC at each data update timing cycle.



*1 If the external reset ON/OFF setting (ioport_set) (FPGA register address: 1000_0020H) is reset OFF(1), the DAC is not set. However, if any of the following is changed and the FPGA control has started, DAC is set.
·External reset ON/OFF setting (ioport_set) (FPGA register address: 1000_0020H)
·DAC range setting CH0 (E0) (remote buffer memory address: 0602H) to DAC range setting CH1 (E2) (remote buffer memory address: 0616H)
·DAC offset CH0 (E0) (remote buffer memory address: 0601H) to DAC offset CH1 (E2) (remote buffer memory address: 0615H)
Analog output during DAC setting is 0V/0mA.

■Operation

The analog output control part performs D/A conversion processing to transfer the D/A conversion value to the DAC.
The analog output control part register setting is performed by firmware. After analog output control part register setting end, follow the analog output control register ("Select D/A conversion value" (aoport_da_data_sel), "Select D/A conversion timing" (aoport_da_cyc_sel), and "Select DAC LDAC signal" (aoport_da_ldac_sel)) to transfer the D/A conversion values CH0 to CH1 (E0 to E2) to the DAC in synchronization with the data update timing that is input at constant cycle from the timing generator. The timing chart for D/A conversion processing is shown below.



■Correspondence between D/A conversion values and analog output values

The DAC connected to this FPGA outputs 16-bit offset binary when setting the voltage, and 16-bit straight binary when setting the current. The table below shows the correspondence between D/A conversion values and analog output values.

• Specifications for current output (0.2 to 19.8mA)

D/A conversion value	Analog output value (typical)	Analog output value (maximum)	Analog output value (minimum)
64880	19.79980469mA	19.85920410mA	19.74040527mA
64879	19.79949951mA	19.85889801mA	19.74010101mA
⋮	⋮	⋮	⋮
657	0.200500488mA	0.20110199mA	0.199898987mA
656	0.200195313mA	0.20079590mA	0.199594727mA
655	0.199890137mA	0.200489807mA	0.199290466mA

• Voltage output specification (-9.9 to 9.9V)

D/A conversion value	Analog output value (typical)	Analog output value (maximum)	Analog output value (minimum)
65207	9.899597168V	9.919396362V	9.879797974V
65206	9.899291992V	9.919090576V	9.879493408V
⋮	⋮	⋮	⋮
330	-9.899291992V	-9.919090576V	-9.879493408V
329	-9.899597168V	-9.919396362V	-9.879797974V
328	-9.899902344	-9.919702148V	-9.880102539V

■Configurable functions

The function that can be set is shown below.

• Offset function

■Offset function

Offset errors caused by external factors of DAC can be compensated by the DAC offset value for each channel.
DAC offset channel△ (E□)(remote buffer memory address: 0601H, 0605H, 0609H, 060DH, 0611H, 0615H), setting it can automatically add or subtract up to 32768 resolutions for each channel.
The resolution for the DAC output voltage range is shown below.

DAC output current/voltage range	Resolution
-9.9 to 9.9V	305μV
0.2 to 19.8mA	0.305μA

The formula for calculating the analog output value is shown below.

• Analog output value = Resolution × (Digital input for D/A conversion + DAC offset value)

The DAC offset value is the offset binary (initial value: 8000H) set by DAC offset CH△ (E□)(remote buffer memory address: 0601H, 0605H, 0609H, 060DH, 0611H, 0615H).

Point

Set the digital input for D/A conversion + DAC offset value within the following range.

• If the DAC range setting CH△ (E□)(remote buffer memory address: 0602H, 0606H, 060AH, 060EH, 0612H, 0616H) setting is ± 9.9V

328 ≤ Digital input for D/A conversion + DAC offset value ≤ 65207

• If the DAC range setting CH△ (E□)(remote buffer memory address: 0602H, 0606H, 060AH, 060EH, 0612H, 0616H) setting is 0.2 to 19.8mA

655 ≤ Digital input for D/A conversion + DAC offset value ≤ 64880

■DAC offset value

DAC offset channel△ (E□)(remote buffer memory address: 0601H, 0605H, 0609H, 060DH, 0611H, 0615H), the DAC offset values corresponding to the values set in it are shown below.

DAC offset channel△ (E□)(remote buffer memory address: 0601H, 0605H, 0609H, 060DH, 0611H, 0615H)	DAC offset value (setting value from FPGA Module Configuration Tool)
0000H	-32768
0001H	-32767
⋮	⋮
8000H	0
8001H	1
⋮	⋮
FFFFH	32767

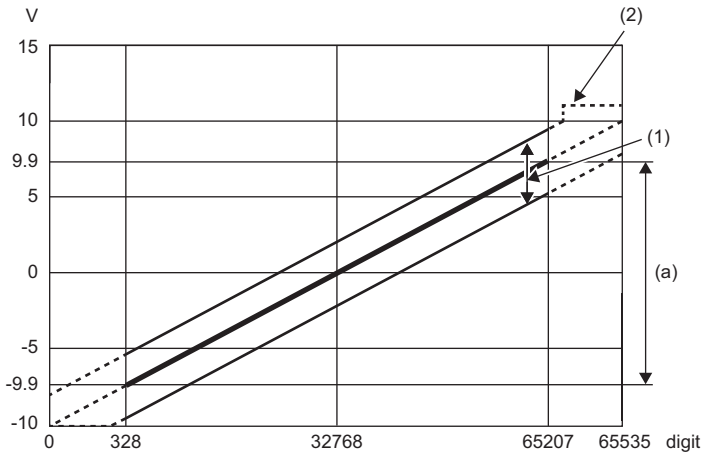
Ex.

If the DAC range setting CH△ (E□)(remote buffer memory address: 0602H, 0606H, 060AH, 060EH, 0612H, 0616H) is an offset of ±9.9V and 9mV, the DAC offset CH△ (E□)(remote buffer memory address: 0601H, 0605H, 0609H, 060DH, 0611H, 0615H) is set to 7FE2H.

• Set 8000H-001EH(9mV=305μV×-30)=7FE2H

■I/O conversion characteristics using the offset function

The I/O conversion characteristics using the offset function are shown below.



digit: D/A conversion value
V: Analog output voltage
(1) Offset value
(2) If the digital input for D/A conversion + DAC offset value > 65535 digits, it varies in the range of 10 to 15V.
(a) Analog output practical range

Notes and restrictions

Notes and restrictions for the standard circuit are shown below.

- Set "Data sampling timing" and "Filter sampling pulse" to be the same.
- Stop the logging operation before accessing DDR3L SDRAM from the MCU.
- Enable logging start after performing all necessary settings such as the operation of the timing generator.
- When the DC input/output circuit board and analog input/output circuit board are connected, the setting of "Differential output HOLD/CLEAR" becomes invalid.

11.4 User Circuit Block

The user circuit block is a block written in RTL according to the application. This section describes the following.

- Connection block list
- Terminal list
- Interface specification
- Circuit implemented in the sample circuit provided

When creating a new user circuit block, or when partially or completely reusing it, refer to the following and perform the development.

- When creating a new user circuit(☞ Page 218 Connection block list, Page 219 Terminal list, Page 220 Module common interface)
- When partially or completely a user circuit (☞ Page 218 Connection block list, Page 219 Terminal list, Page 220 Module common interface, Page 238 Sample circuit)

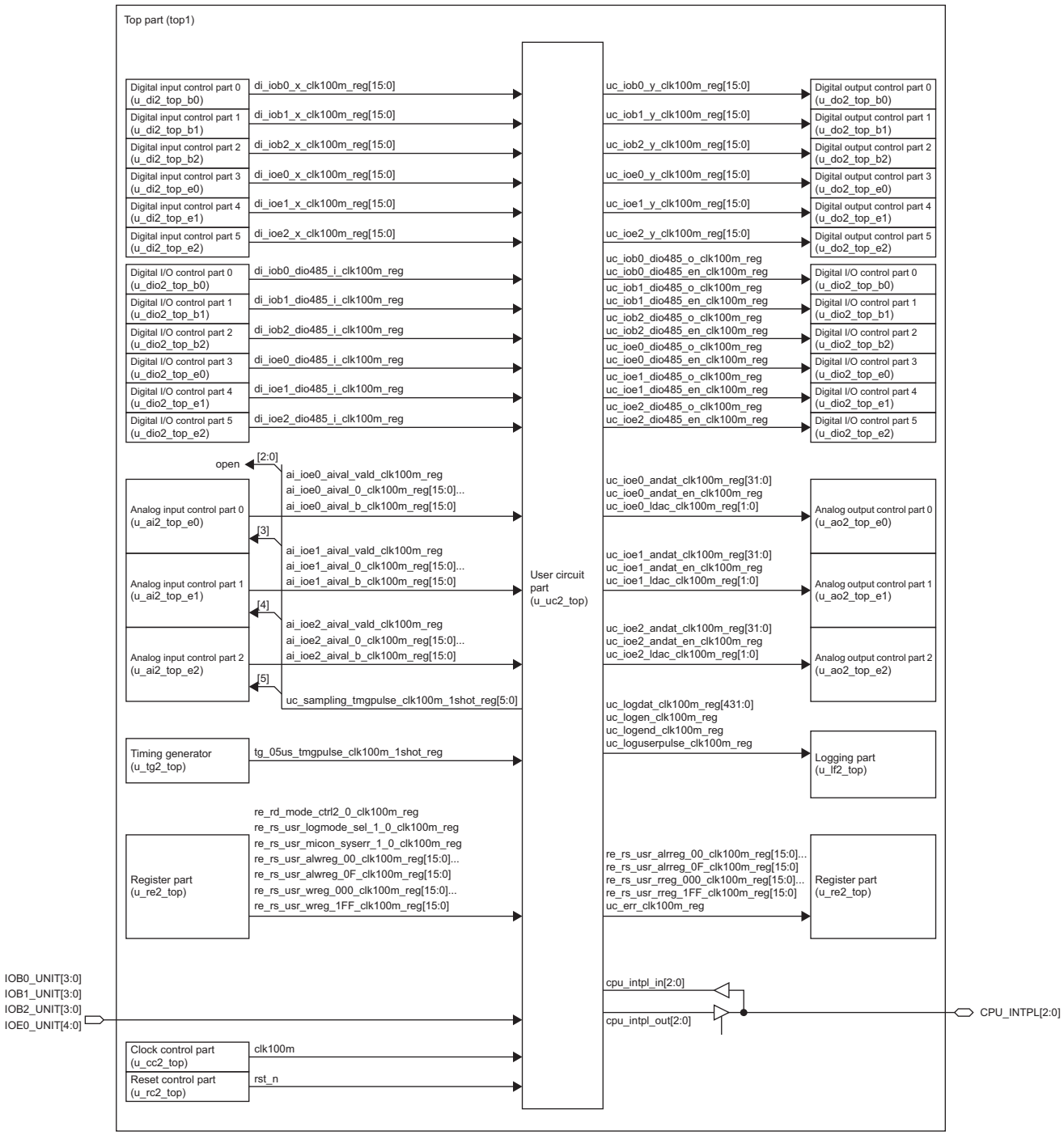
Connection block list

Blocks connected to the input/output selector are enabled or disabled depending on the model. The connected blocks are shown below.

- Digital input control part
- Digital output control part
- Digital input/output control part
- Analog input control part
- Analog output control part

If a block is enabled, the active signal and inactive signal of the external terminal are notified to the user circuit block via the block. If a block is disabled, it will not operate. The input signals will be inactive and output signals ignored.

The connection diagram of the user circuit block and effective blocks for each model are shown below.



Model	Module category	Connection circuit board	Effective block*1
NZ2GN2S-D41P01	Main module	B0, B1, B2: DC input/output circuit board	u_di2_top_b0, u_di2_top_b1, u_di2_top_b2, u_do2_top_b0, u_do2_top_b1, u_do2_top_b2
NZ2GN2S-D41D01		B0, B1, B2: Differential input/output circuit board	u_di2_top_b0, u_di2_top_b1, u_di2_top_b2, u_do2_top_b0, u_do2_top_b1, u_do2_top_b2, u_dio2_top_b0, u_dio2_top_b1, u_dio2_top_b2
NZ2GN2S-D41PD02		B0, B1: DC input/output circuit board	u_di2_top_b0, u_di2_top_b1, u_do2_top_b0, u_do2_top_b1
		B2: Differential input/output circuit board	u_di2_top_b2, u_do2_top_b2, u_dio2_top_b2
NZ2EX2S-D41P01	Extension module	E0, E1, E2: DC input/output circuit board	u_di2_top_e0, u_di2_top_e1, u_di2_top_e2, u_do2_top_e0, u_do2_top_e1, u_do2_top_e2
NZ2EX2S-D41D01		E0, E1, E2: Differential input/output circuit board	u_di2_top_e0, u_di2_top_e1, u_di2_top_e2, u_do2_top_e0, u_do2_top_e1, u_do2_top_e2, u_dio2_top_e0, u_dio2_top_e1, u_dio2_top_e2
NZ2EX2S-D41A01		E0, E1, E2: Analog input/output circuit board	u_ai2_top_e0, u_ai2_top_e1, u_ai2_top_e2, u_ao2_top_e0, u_ao2_top_e1, u_ao2_top_e2

*1 It is described using the RTL instance name. (u_module name)

Terminal list

For the terminal list of the user circuit block, refer to the following.

☞ Page 610 List of User Circuit Block Terminals

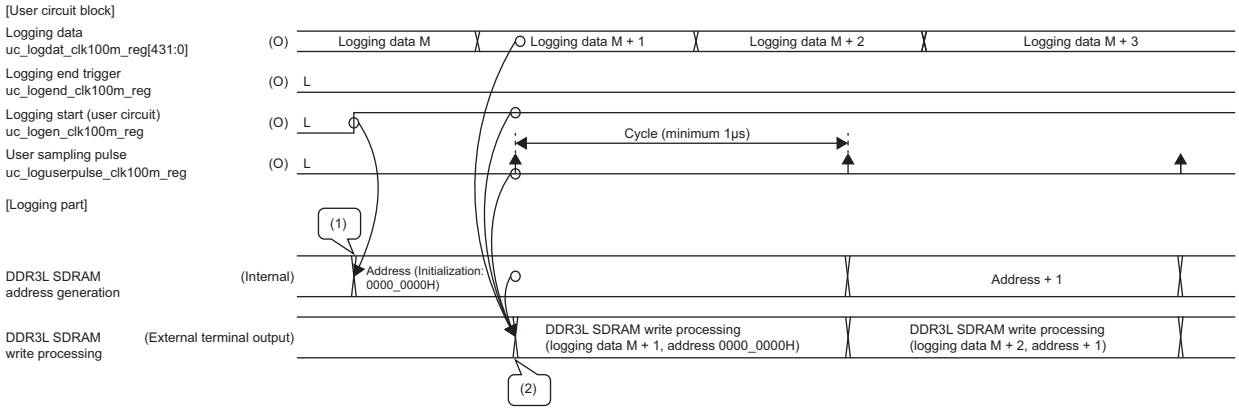
Logging control (output)

The timing chart when using the logging control (output) is shown below.

Ex.

If the FPGA register is set as follows:

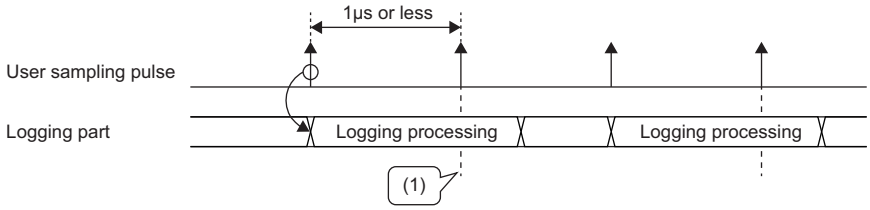
FPGA register	Setting value	Remarks
Logging cycle timing (tim_log_cyc) (FPGA register address: 1000_2200H)	0001H	1μs
Logging data size setting (lgdw_area)(FPGA register address: 1000_9008H)	0H	256 records (16kB)
Set number of sampling after trigger (lower side) (lgdw_triggered_lsample) (FPGA register address: 1001_9000H)	0200H	512
Set number of sampling after trigger (upper side) (lgdw_triggered_usample) (FPGA register address: 1001_9002H)	0H	
Logging state register (lgdw_sts)(Address: 1000_9002H)	—	For monitoring logging status
Number of samplings (lower) (lgdw_sample_lcount)(address: 1001_9004H)	—	For monitoring the number of times logged
Number of samplings (upper)(lgdw_sample_ucount)(address: 1001_9006H)	—	



(1) Initialize the address (0000_0000H) at the start of logging.
(2) Issue a user sampling pulse from the user circuit block and write logging data to DDR3L SDRAM.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start(1).
2	Enables(1) the logging enable (uc_logen_clk100m_reg), and enables (1) the user sampling pulse (uc_loguserpulse_clk100m_reg).
3	Writes one record (data with time information (80 bits) and logging data (432 bits) as one unit) to DDR3L SDRAM.
3-1	■Storage operation mode (linear buffer mode) Enables (1) the logging enable (uc_logen_clk100m_reg), and stops the operation when user sampling pulses are sent for the number of times set in the logging data size setting (lgdw_area) (FPGA register address: 1000_9008H). To perform logging again, it is necessary to set logging enable (uc_logen_clk100m_reg) from Enable (1) to Disable (0) and then Enable (1). For DDR3L SDRAM sampling count (lower) (lgdw_sample_lcount) (FPGA register address: 1001_9004H) and number of samplings (upper) (lgdw_sample_ucount) (FPGA register address: 1001_9006H), they are initialized when logging enable (uc_logen_clk100m_reg) is set to Enable (1H).
3-2	■Storage operation mode (ring buffer mode) Enables (1) Logging enable (uc_logen_clk100m_reg), and initializes the DDR3L SDRAM address to 0000_0000H when user sampling pulses are sent for the number of times set in the logging data size setting (lgdw_area) (FPGA register address: 1000_9008H). To stop logging, set logging enable (uc_logen_clk100m_reg) to Disable (0). To perform logging again, it is necessary to set logging enable (uc_logen_clk100m_reg) to Enable (1). For DDR3L SDRAM sampling count (lower) (lgdw_sample_lcount)(FPGA register address: 1001_9004H) and number of samplings (upper) (lgdw_sample_ucount) (FPGA register address: 1001_9006H), they are initialized when logging enable (uc_logen_clk100m_reg) is set to Enable (1H).
3-3	■In trigger operation mode If the logging end trigger is enabled while operating in the storage operation mode (ring buffer mode), the operation will stop when logging data is sent for the number of times set in the post-trigger sampling count. To perform logging again, it is necessary to set Logging enable (uc_logen_clk100m_reg) from Enable (1) to Disable (0) and then Enable(1). For DDR3L SDRAM sampling count (lower) (lgdw_sample_lcount)(FPGA register address: 1001_9004H) and number of samplings (upper) (lgdw_sample_ucount) (FPGA register address: 1001_9006H), they are initialized when logging enable (uc_logen_clk100m_reg) is set to Enable (1H).

If the user sampling pulse (uc_loguserpulse_clk100m_reg) is smaller than the minimum setting value of the logging cycle timing below, it will not work properly. (☞ Page 193 Timing generator (tg2_top))
After enabling (1) the user sampling pulse (uc_loguserpulse_clk100m_reg), logging processing is performed in the logging part. During logging processing, even if the user sampling pulse (uc_loguserpulse_clk100m_reg) is enabled (1), it is ignored by the logging part. The operation when the pulse interval is set below the minimum setting value is shown below.



(1) Ignores user sampling pulses because logging is in progress.

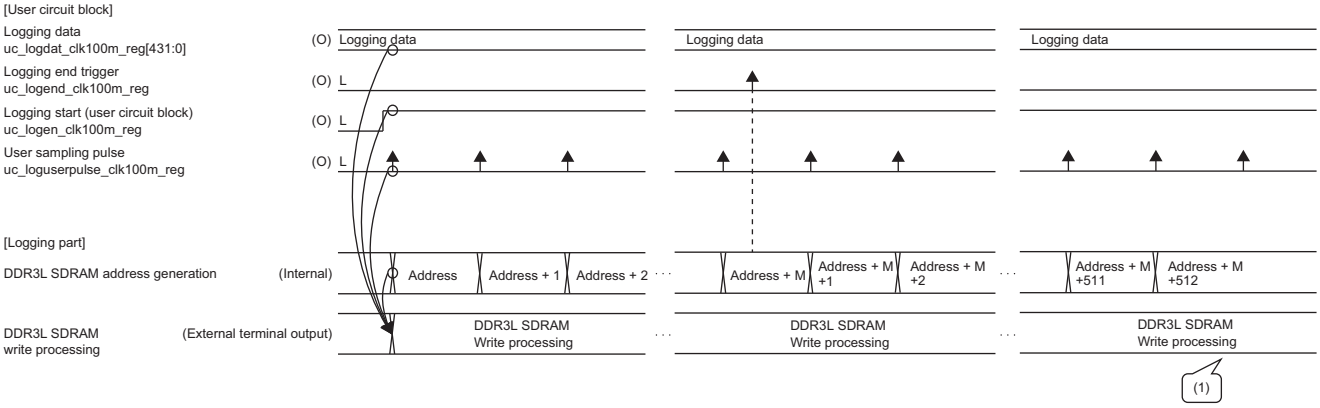
■Automatic transfer mode

The logging control operates using the automatic transfer mode of the logging part. In the automatic transfer mode, logging start (user circuit block) needs to be output according to the logging control trigger input to the user circuit block.

If b3 of the logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) is set to Rising for logging start allowed (1), the rising edge of logging start (user circuit block) is detected and logging starts. Also, to stop logging which is in progress, set b3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) to Falling for logging start allowed (0), so that the falling edge of Logging enable (uc_logen_clk100m_reg) is detected and logging stops.

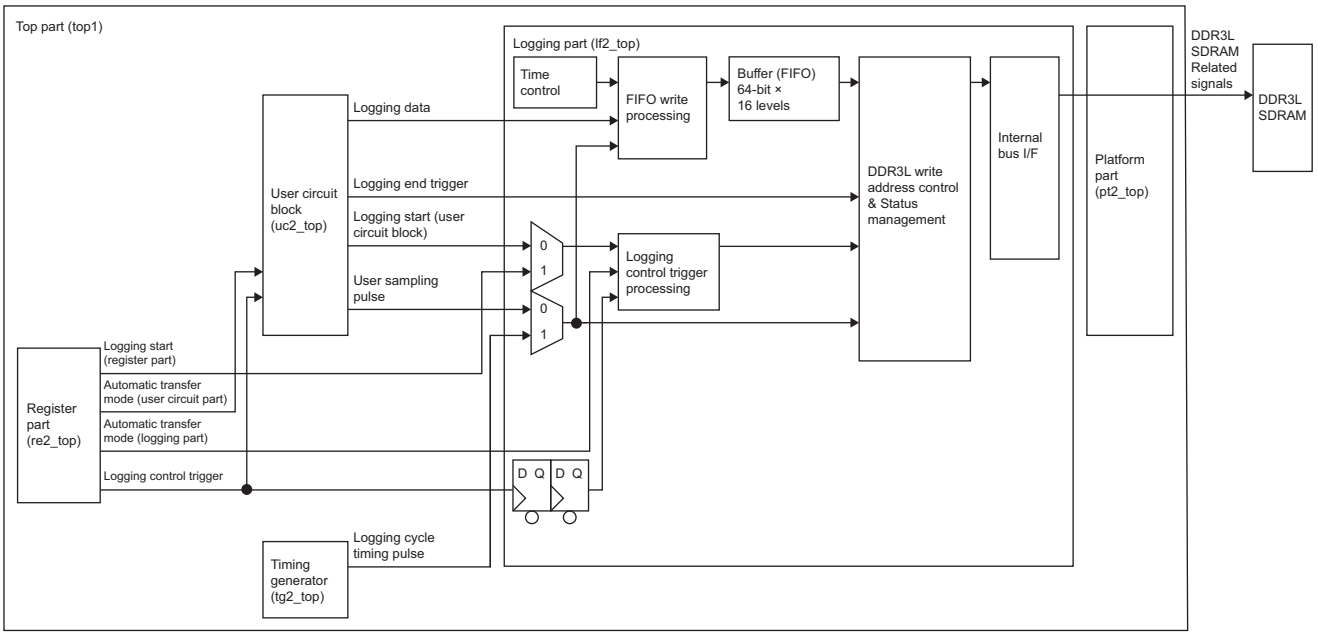
Logging can also be stopped by using the logging end trigger. The method is shown below.

- Trigger control

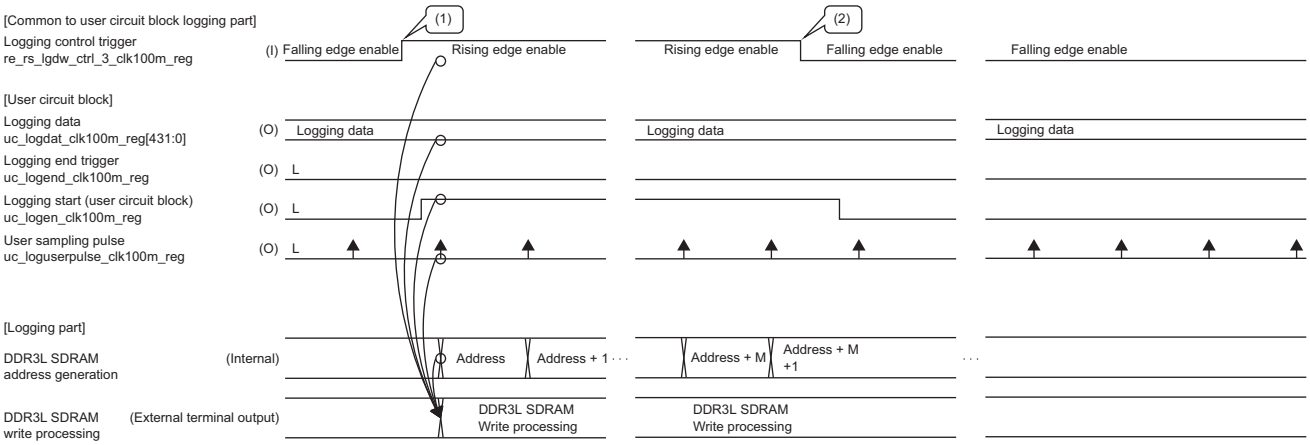


(1) After the logging end trigger is input, logging is stopped by writing for the number of times set for "Set number of sampling after trigger (upper/lower side)".

Logging using the automatic transfer mode is shown below.



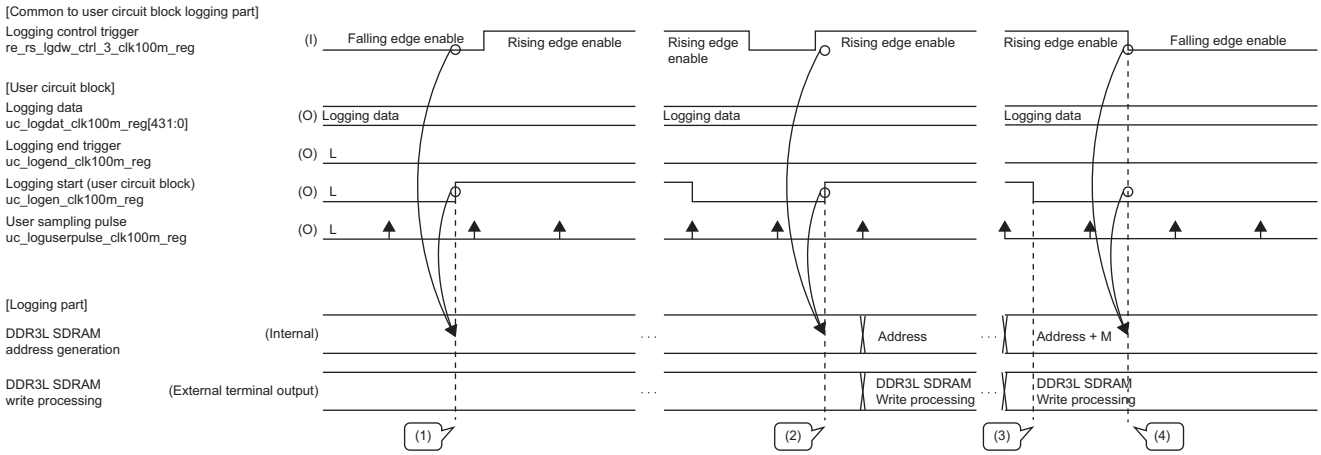
• Automatic transfer mode (normal operation)



(1) Logging is started by enabling (1) logging enable (uc_logen_clk100m_reg) when the logging control trigger is Rising edge enable.
(2) Logging is stopped by disabling (0) the logging enable (uc_logen_clk100m_reg) when the logging control trigger is Falling edge enable.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2)(FPGA register address: 1000_0002H) to Start (1).
2	If Bit 3 of Logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) is set to Rising edge enable (1), after Logging enable (uc_logen_clk100m_reg) is set to Enable (1), User sampling pulse (uc_loguserpulse_clk100m_reg) is set to Enable (1).
3	Writes one record (data with time information (80 bits) and logging data (432 bits) as one unit) to DDR3L SDRAM. (Writes one record for each user sampling pulse output.)
4	Sets Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg) to Falling edge enable (1), and Logging start (user circuit block) (uc_logen_clk100m_reg) to Disable (0).
5	Writes the record currently being written to DDR3L SDRAM and stops logging.

• Automatic transfer mode (faulty operation)



(1) Even if Logging start (user circuit block) is enabled while the logging control trigger is Falling edge enable, logging in the logging block will not start. (A minor error occurs.)
(2) Logging starts because Logging start (user circuit block) is enabled while the logging control trigger is rising edge enable.
(3) Even if Logging start (user circuit block) is disabled (0) while the logging control trigger is rising edge enable, logging in the logging block will not stop. (A minor error occurs.)
(4) Logging stops because the logging control trigger is Falling edge enable and Logging start (user circuit block) is disabled.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1).
2	Sets Logging start (user circuit block) (uc_logen_clk100m_reg) to Enable (1), Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg) to Rising edge enable (1), and then User sampling pulse (uc_loguserpulse_clk100m_reg) to Enable (1b, 1 pulse output (clk100m)).
3	Raises a minor error. (Error code: 1430H)
4	Sets Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg) to Rising edge enable (1), Logging start (user circuit block) (uc_logen_clk100m_reg) to Enable (1), and then User sampling pulse (uc_loguserpulse_clk100m_reg) to Enable (1b, 1 pulse output (clk100m)).
5	Writes one record (data with time information (80 bits) and logging data (432 bits) as one unit) to DDR3L SDRAM. (One record is written for each user sampling pulse output.)
6	Sets Logging start (user circuit block) (uc_logen_clk100m_reg) to Disable (1), Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg) to Falling edge enable (1), and then User sampling pulse (uc_loguserpulse_clk100m_reg) to Enable (1b, 1 pulse output (clk100m)).
7	Raises a minor error. (Error code: 1431H) Writes one record (data with time information (80 bits) and logging data (432 bits) as one unit) to DDR3L SDRAM. (One record is written for each user sampling pulse output.) *Continues logging without stopping.

Register

Notifies the setting values from the MCU to the user circuit and notifies the user circuit status to the MCU. For the signal names of the user circuit part and the register part, as well as the notification timing, refer to the following.

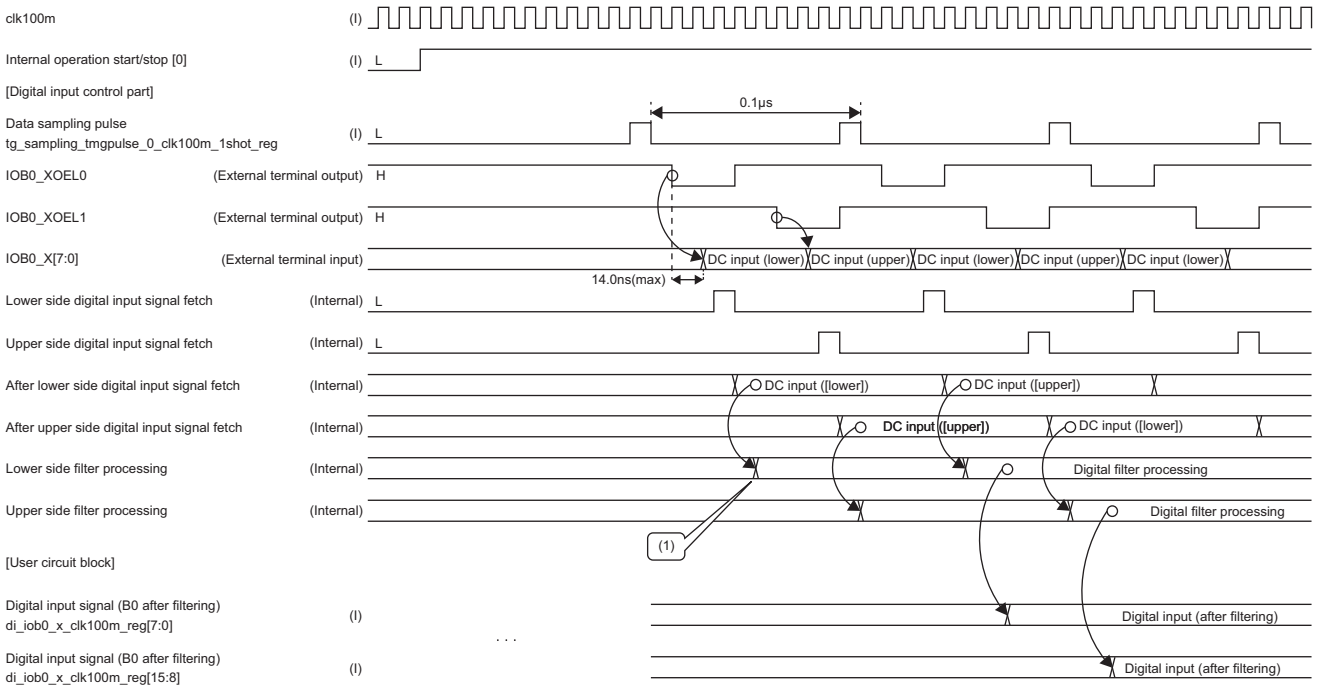
☞ Page 195 Connection and setting value notification timing

DC input/output circuit board (input)

The user circuit block timing chart when using the DC input/output circuit board is shown below. In addition, the setting values of the digital input control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	Filter sampling pulse (B0)	FH	Data sampling pulse
2	Data sampling timing (B0)	9H	0.1μs cycle
3	Input filter counter upper limit (IOB0_X0) (B0) to input filter counter upper limit (IOB0_XF) (B0)	2H each	—

■Timing chart example



(1) Filter sampling pulse (B0) = FH, so digital filtering is performed in synchronization with the data sampling timing.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start(1).
2	The data sampling timing becomes Enable (1) at each cycle set in "Data sampling timing (B0)", and the digital input control part operates.
3	DC input [7:0] and DC input [15:8] are input from outside the FPGA in time division.
4	A digital input signal that has passed through a digital filter is input to the user circuit block.

*1 B0 is explained at the circuit board. B1, B2, E0, E1, and E2 have the same structure.

*2 Changing the filter sampling pulse (B0) and data sampling timing (B0) changes the input timing of the digital input signal (B0 after filtering) (di_iob0_x_clk100m_reg[15:0]). For details, refer to the following.

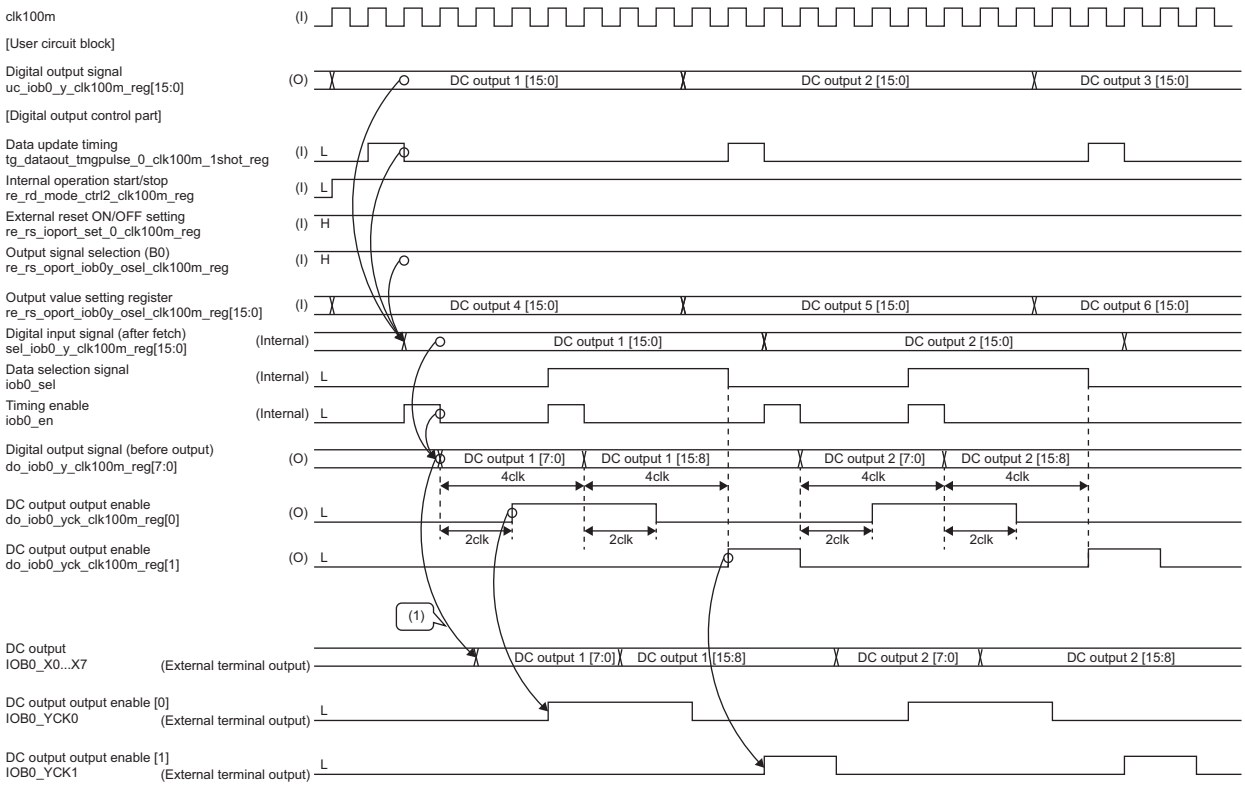
☞ Page 193 Timing generator (tg2_top)
☞ Page 195 Connection and setting value notification timing

DC input/output circuit board (output)

The user circuit block timing chart when using the DC input/output circuit board (output) is shown below. The setting values of the digital output control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	External reset ON/OFF setting	0000H	Reset ON
2	Data update timing (B0)	0009H	0.1μs cycle
3	Output signal selection (B0)	0001H	Selects user circuit output.
4	Output value setting (B0)	0000H	Setting is not required (because user circuit output is selected in No.3).
5	Output signal monitor (B0)	—	Register for monitoring IOB0_Y[0] to IOB0_Y[15]

■Timing chart example



(1) Output to external terminal in one level of FF.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1).
2	The data update timing becomes Enable (1) at each cycle set in Data update timing (B0), and the digital output control part operates.
3	The digital output signal (uc_iob0_y_clk100m_reg[15:0]) of the user circuit block is output in time division from the DC output (IOB0_X0 to X7).

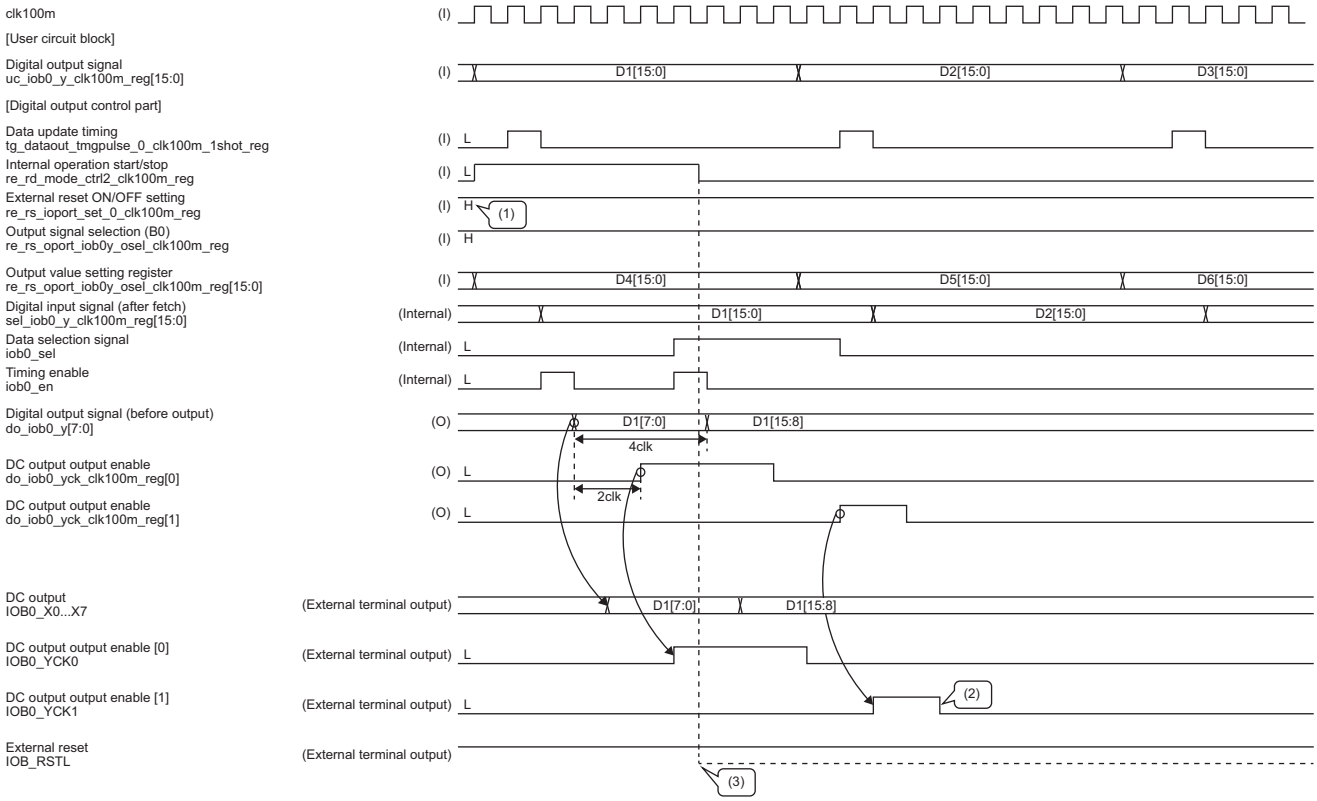
*1 B0 is explained at the circuit board. B1, B2, E0, E1, and E2 have the same structure.

*2 Although 8 bits are output to the outside of the FPGA in time division, the structure in which 16 bits are output at the same timing outside the FPGA is constructed.

*3 Changing the data update timing (B0) changes the output timing of the DC output (IOB_Y0 to Y7). For details, refer to the following.
☞ Page 193 Timing generator (tg2_top)

*4 Even if "Internal operation start/stop" is set to Stop (0) during DC output, the DC output signal being output will be output. After the DC output signal is output, the operation differs depending on the HOLD/CLEAR setting. See below for a HOLD/CLEAR timing chart.
☞ Page 227 Timing chart (HOLD) example
☞ Page 227 Timing chart (CLEAR) example

■Timing chart (HOLD) example

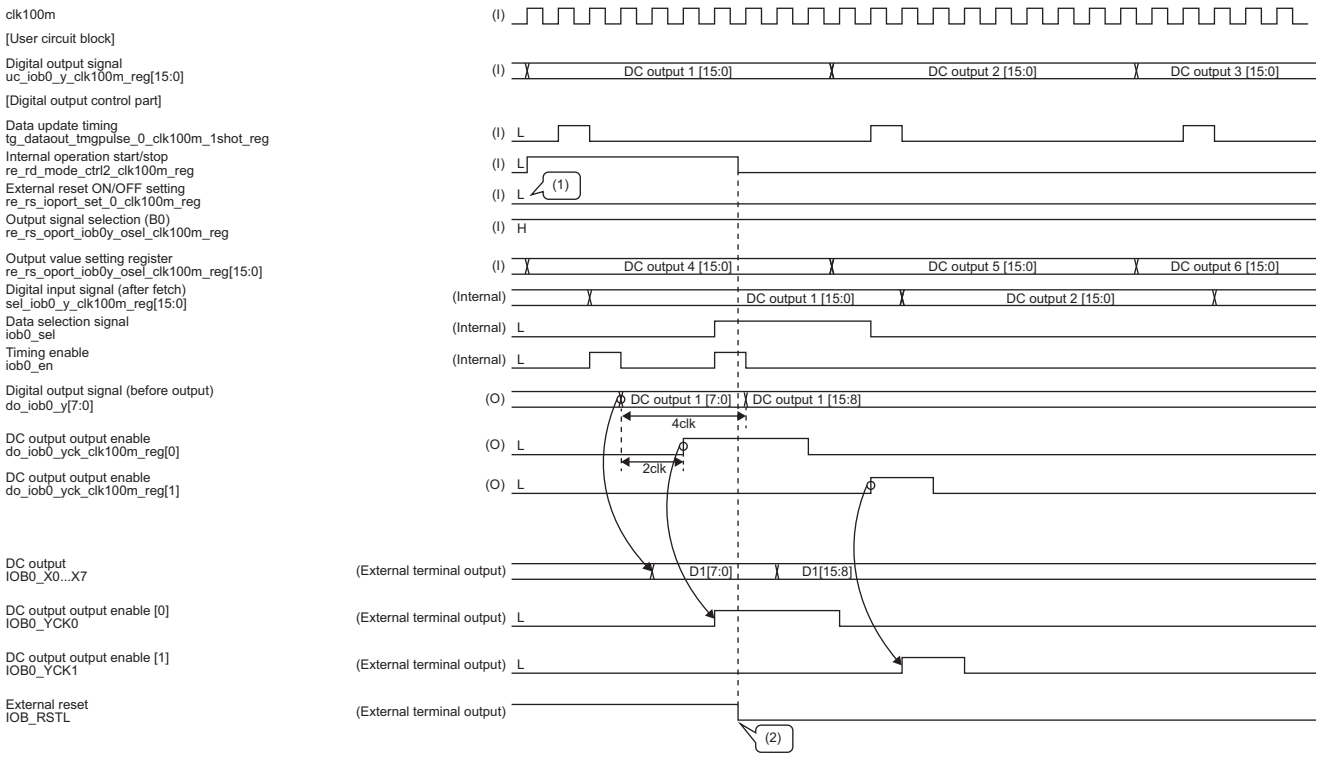


(1) HOLD setting

(2) Completes the output process of the signal being output. The subsequent data is not output.

(3) If the terminal setting for internal stop is HOLD, no reset is issued to the FPGA external circuit.

■Timing chart (CLEAR) example



(1) CLEAR setting

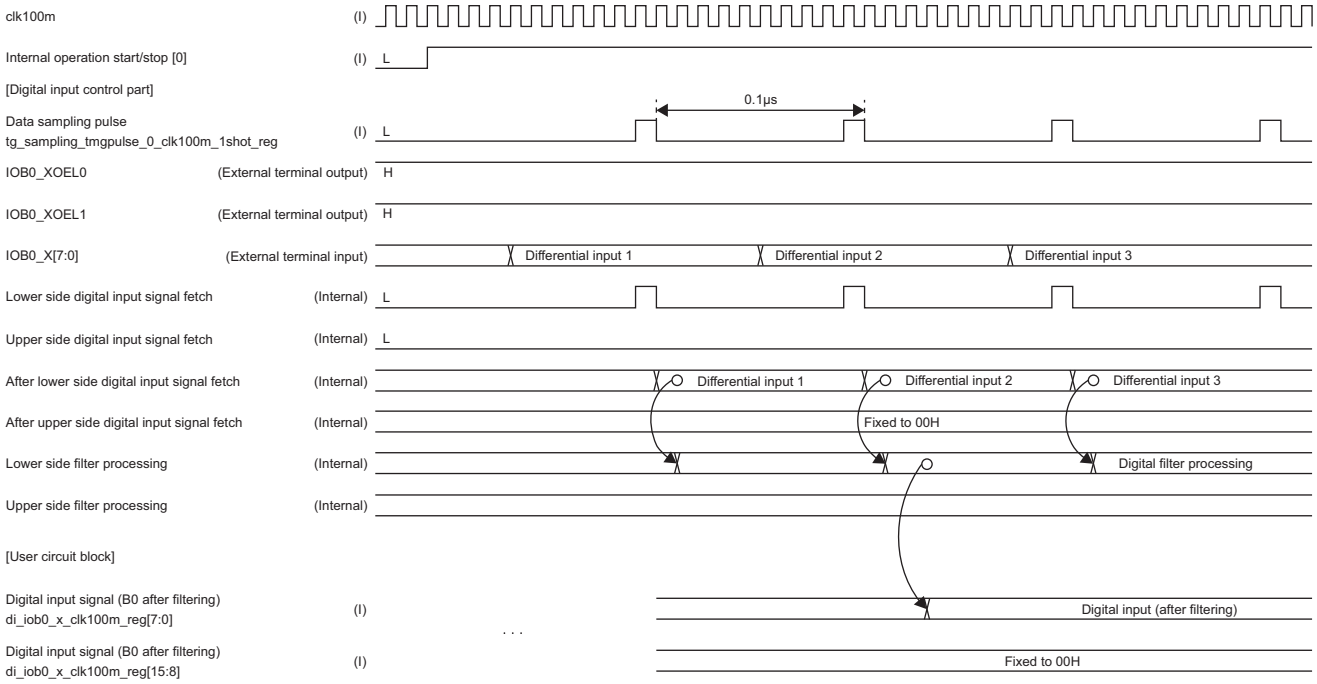
(2) If the terminal setting during internal stop is CLEAR, a reset is issued to the FPGA external circuit.

Differential input/output circuit board (input)

The user circuit timing chart when using the differential input/output circuit board is shown below. In addition, the setting values of the digital input control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	Filter sampling pulse (B0)	4H	0.10μs
2	Data sampling timing (B0)	9H	0.1μs cycle
3	Input filter counter upper limit (IOB0_X0) (B0) to input filter counter upper limit (IOB0_XF) (B0)	2H each	—

■Timing chart example



No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1).
2	The data sampling timing becomes Enable (1) at each cycle set in Data sampling timing (B0), and the digital input control part operates.
3	Differential input [7:0] is input from outside the FPGA.
4	The data sampling timing becomes Enable (1) at each cycle set in Data sampling timing (B0), and the digital input control part operates.

*1 B0 is explained at the circuit board. B1, B2, E0, E1, and E2 have the same structure.

*2 Changing the filter sampling pulse (B0) and data sampling timing (B0) changes the input timing of the digital input signal (B0 after filtering) (di_iob0_x_clk100m_reg[15:0]). For details, refer to the following.

☞ Page 193 Timing generator (tg2_top)
☞ Page 195 Connection and setting value notification timing

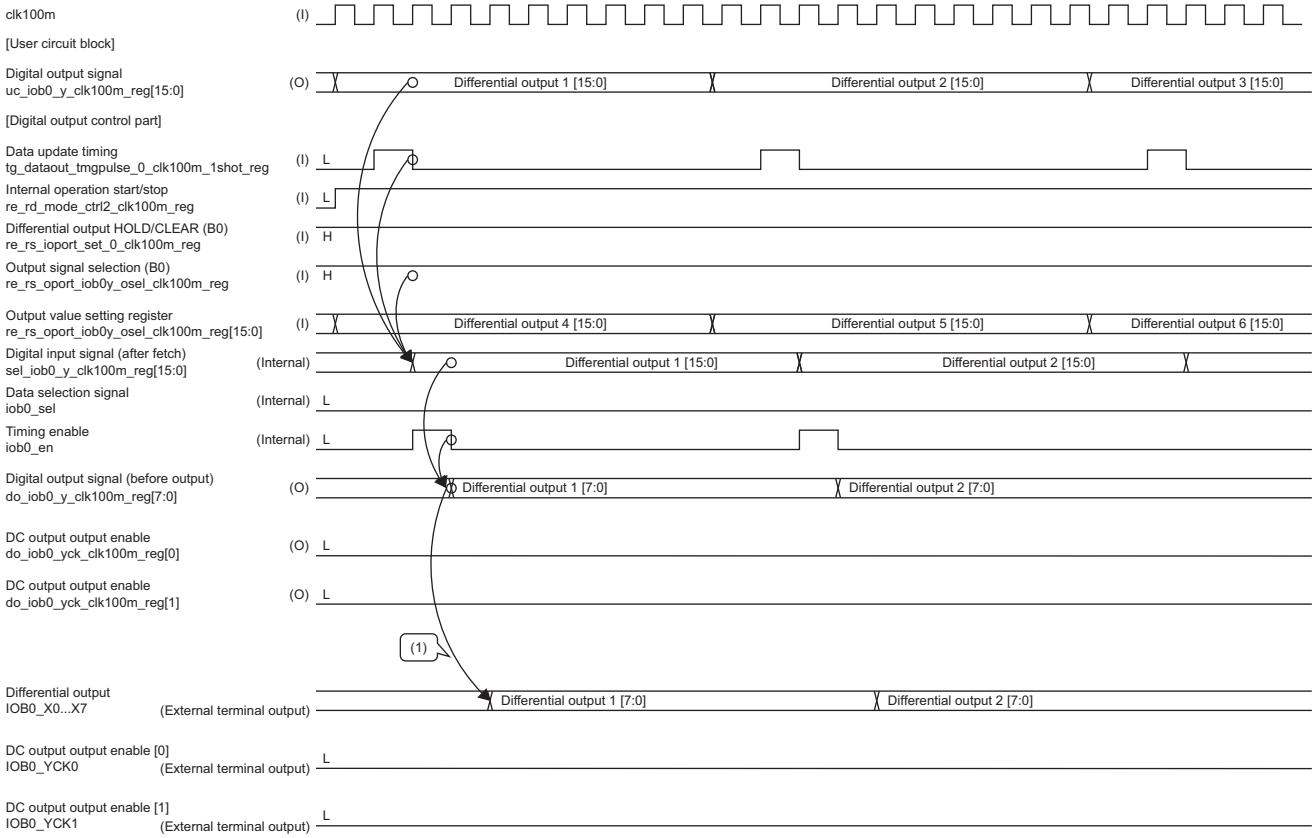
*3 The same structure is used when using the digital input/output control part as an input (dio_iob0 to b2_dio485_i_clk100m_reg, dio_ioe0 to e2_dio485_i_clk100m_reg). When using the digital input/output control part for digital input control, set dio_iob0 to b2_dio485_en_clk100m_reg to 0b.

Differential input/output circuit board (output)

The user circuit block timing chart when using the differential input/output circuit board (output) is shown below. The setting values of the digital output control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	Data update timing (B0)	0009H	0.1μs cycle
2	Output signal selection (B0)	0001H	Selects user circuit output.
3	Output value setting (B0)	0000H	Setting is not required (because user circuit output is selected in No.2).
4	Differential output HOLD/CLEAR (B0)	0000H	CLEAR (0b fixed)
5	Output signal monitor (B0)	—	Register for monitoring IOB0_Y[0] to IOB0_Y[7]

■Timing chart example



(1) Output to external terminal in one level of FF.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1).
2	The data update timing becomes Enable (1) at each cycle set in Data update timing (B0), and the digital output control part operates.
3	The digital output signal (uc_iob0_y_clk100m_reg[7:0]) of the user circuit block is output from the differential output (IOB0_X0 to X7).

*1 B0 is explained at the circuit board. B1, B2, E0, E1, and E2 have the same structure.

*2 Changing the data update timing (B0) (tim_iob0x_conv) (FPGA register address: 1000_2110H) changes the output timing of the differential output (IOB_Y0 to Y7). For details, refer to the following.

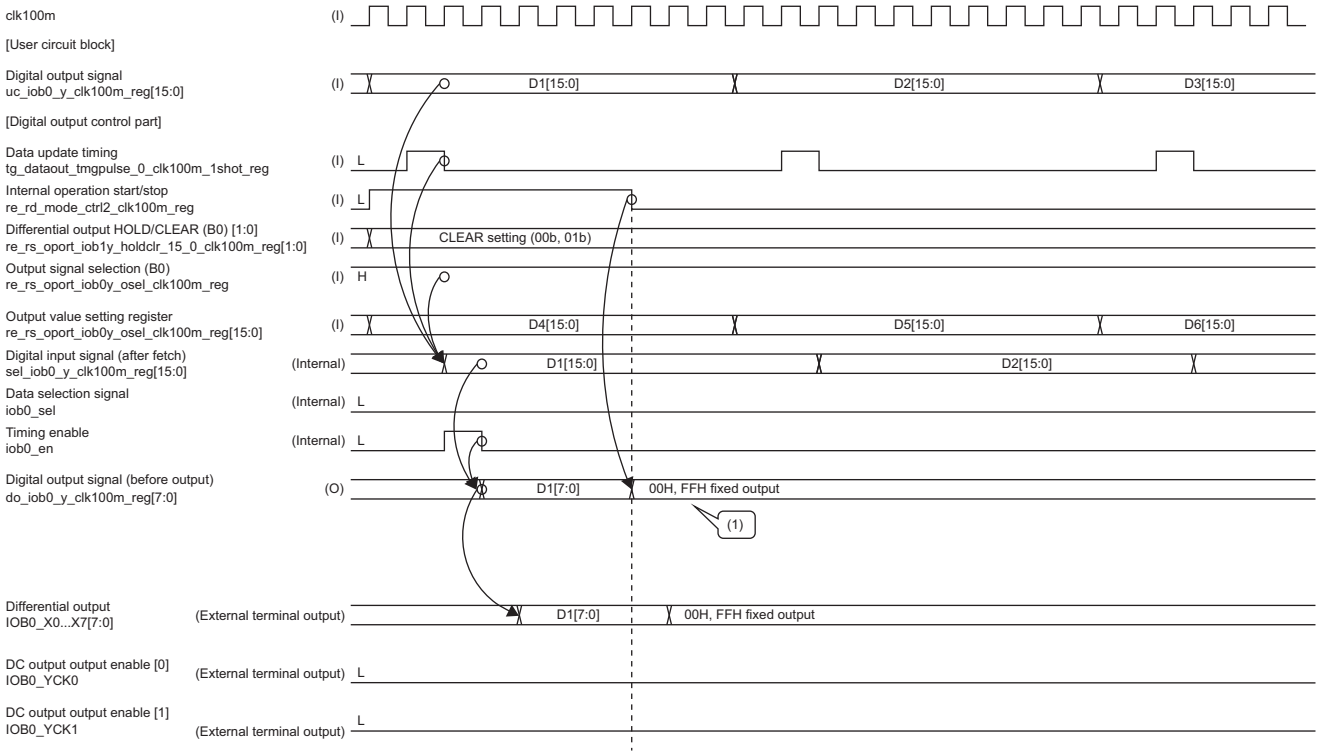
☞ Page 193 Timing generator (tg2_top)

*3 The same structure is used when using the digital input/output control part as an output (dio_iob0 to b2_dio485_o_clk100m_reg, dio_ioe0 to e2_dio485_o_clk100m_reg). When using the digital input/output control part for digital output control, set dio_iob0 to b2_dio485_en_clk100m_reg to 1b.

*4 Even if "Internal operation start/stop" is set to Stop (0) during differential output, the differential output signal being output is output. After the differential output signal is output, the operation differs depending on the HOLD/CLEAR setting. See below for a HOLD/CLEAR timing chart.

☞ Page 230 Timing chart (HOLD/CLEAR) example

■Timing chart (HOLD/CLEAR) example



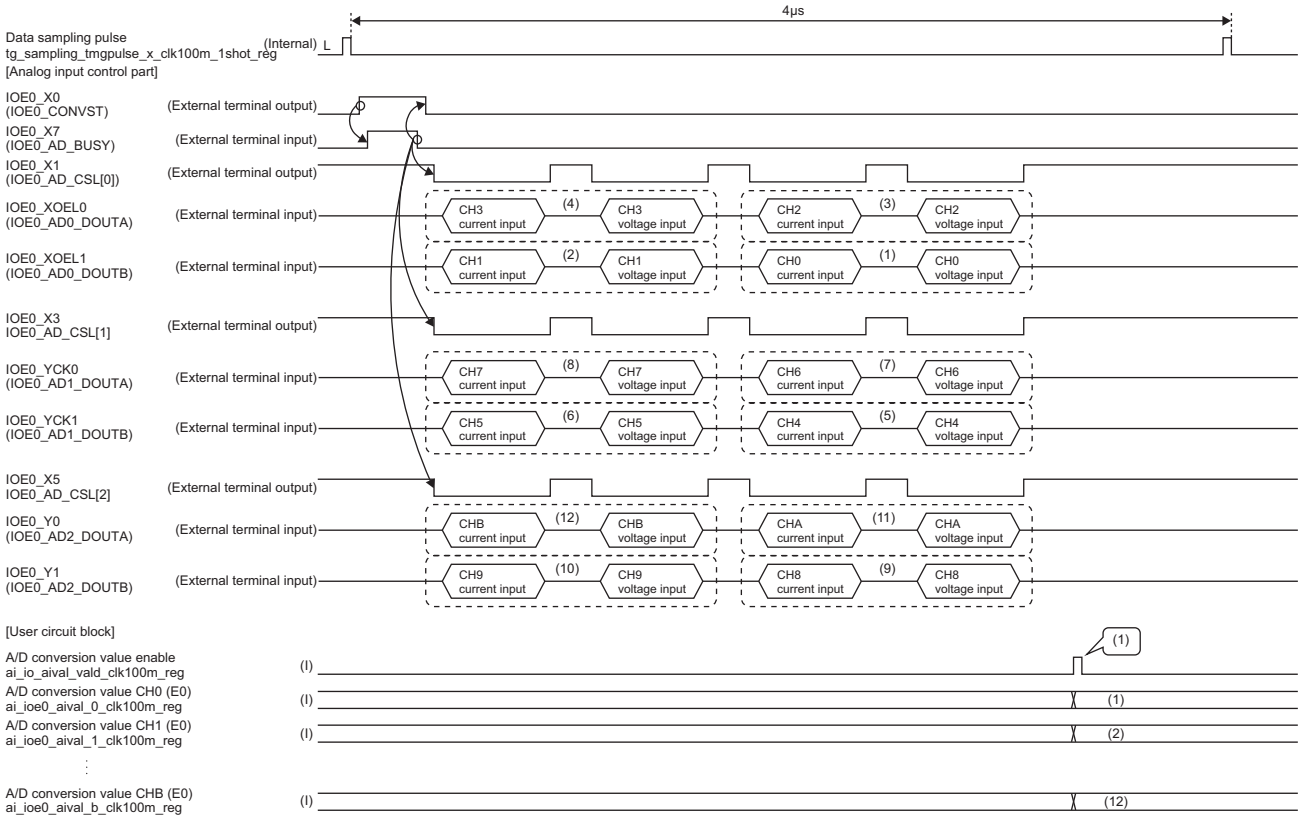
(1) Differential output HOLD/CLEAR (B0)[1:0]:
00b setting: 0 fixed output, 01b setting: 1 fixed output
10b, 11b settings: Previous value held

Analog input/output circuit board (input)

The user circuit block timing chart when using the analog input/output circuit board is shown below. The setting values for the analog input control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	Data sampling timing (E0)	18FH	4μs cycle
2	A/D conversion enable/disable setting	0001H	CH0 to CHB of E0: A/D conversion enable
3	A/D conversion timing selection	0000H	Select data sampling timing
4	ADC range setting CH0-3 (E0)	3333H	CH0 to CHB of E0: -9.9 to 9.9V range
5	ADC range setting CH4-7 (E0)	3333H	
6	ADC range setting CH8-B (E0)	3333H	
7	ADC oversampling ratio setting (E0)	0000H	Oversampling setting is not required.
8	ADC offset value CH0-1 (E0)	8080H	ADC offset value CHm-n (E0) Lower byte: Offset value of CHm Upper byte: Offset value of CHn
9	ADC offset value CH2-3 (E0)	8080H	
10	ADC offset value CH4-5 (E0)	8080H	
11	ADC offset value CH6-7 (E0)	8080H	
12	ADC offset value CH8-9 (E0)	8080H	
13	ADC offset value CHA-B (E0)	8080H	
14	A/D conversion value CH0 (E0) to A/D conversion value CHB (E0)	—	Monitor register areas that store A/D conversion values

■Timing chart example



(1) Input A/D conversion value enable and A/D conversion value CH0 to CHB at the same time.

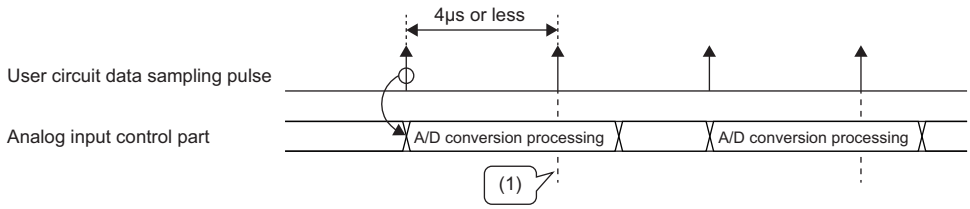
No.	Description
1	Sets Internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1), A/D Conversion-enable/disable setting of A/D Conversion-enable/disable setting (aiport_ad_start) (FPGA register address: 1000_6000H) to Conversion-enable (1), and A/D conversion start to Start (1). (After startup, ADC register initialization is performed inside the FPGA. ☞ Page 232 Timing chart example is the operation after the ADC register is initialized.)
2	The data sampling timing becomes Enable (1) at each cycle set in Data sampling timing (E0), and the analog input control part operates.
3	Outputs the A/D conversion start signal (IOE0_CONVST) from the FPGA. After the BUSY signal (IOE0_AD_BUSY) from the ADC falls, the A/D conversion value is input to the FPGA using SPI (Serial Peripheral Interface). (The BUSY signal (IOE0_AD_BUSY) of the ADC output remains active until all conversion processing ends.)
4	After A/D conversion values of 12CH are input to the FPGA, the A/D conversion values CH0 to B (E0) (ai_io_aival_0_clk100m_reg to ai_io_aival_b_clk100m_reg) are input to the user circuit block together with the A/D conversion value enable signal (ai_io_aival_vald_clk100m_reg).

*1 E0 is explained at the circuit board. E1 and E2 have the same structure.

*2 While the ADC register areas are being initialized, A/D conversion processing is not executed even if a data sampling pulse is input (☞ Page 232 Timing chart example operation is not performed).

*3 Changing the A/D conversion timing selection (aiport_ad_cyc_sel) (FPGA register address: 1000_6002H) changes the input timing of the A/D conversion value enable signal and A/D conversion values 0 to b (E0). For details, refer to the following.
☞ Page 208 Oversampling function

*4 When operating at the customer's timing, change the data sampling pulse in the timing chart example to the user circuit block data sampling pulse (uc_sampling_tmgpulse_clk100m_1shot_reg) and output the changed pulse from the user circuit block. However, if it is smaller than the minimum setting value of ☞ Page 193 Timing generator (tg2_top) data sampling timing, it will not work properly. After setting the user circuit block data sampling pulse to Enable (1), A/D conversion processing is performed in the analog input control part. During A/D conversion processing, even if the user circuit block data sampling pulse is enabled, it is ignored by the analog input control part. The operation when the pulse interval is set below the minimum setting value is described below.



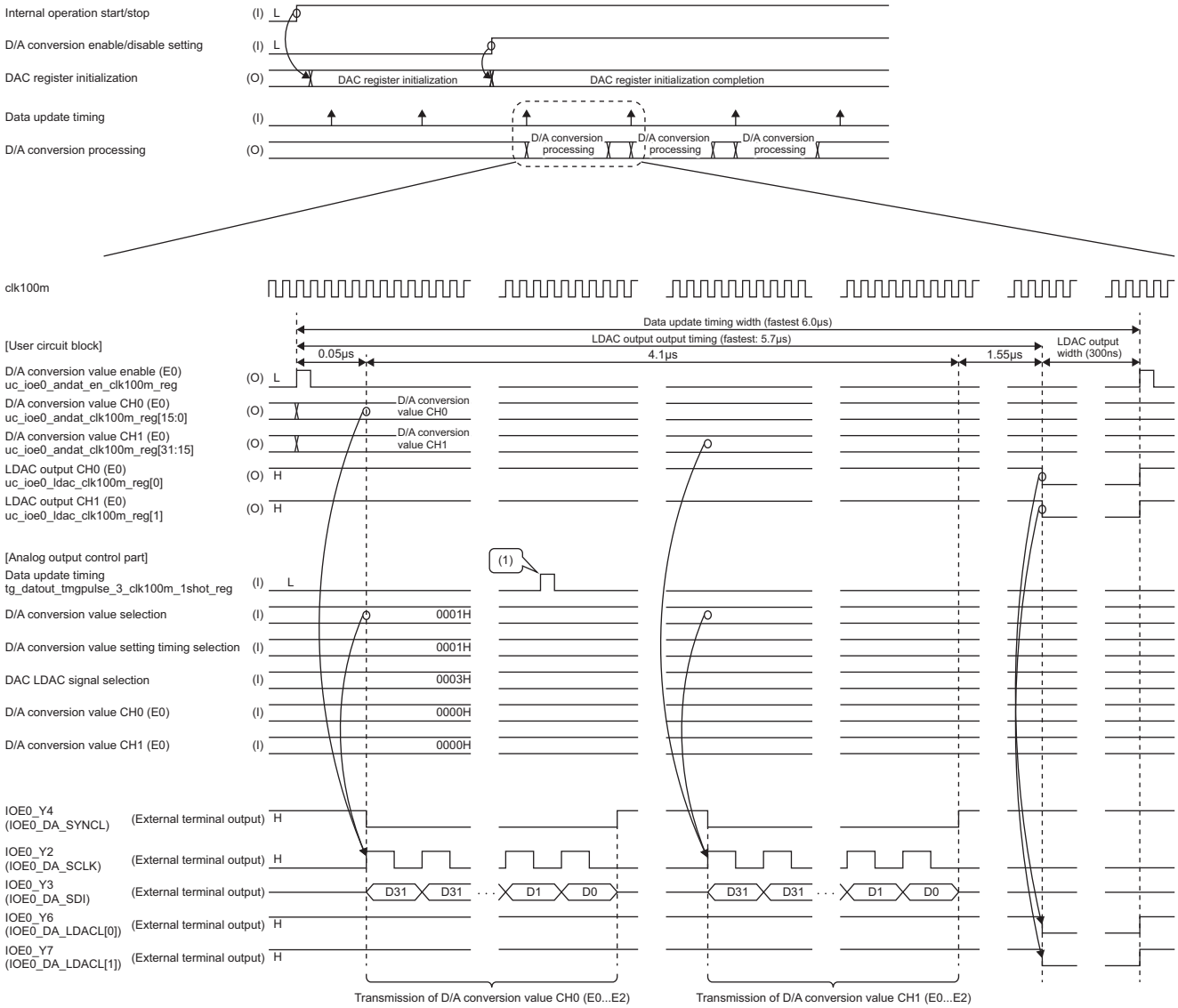
(1) The user circuit block data sampling pulse is ignored because A/D conversion processing is in progress.

Analog input/output circuit board (output)

The user circuit block timing chart when using the analog input/output circuit board (output) is shown below. Also, the setting values of the analog output control part in this timing chart are shown below.

No.	Target register	Setting value	Remarks
1	External reset ON/OFF setting	0000H	Reset ON
2	Data update timing (E0)	0257H	6μs cycle
3	D/A conversion enable/disable setting	0001H	CH0: Conversion enable CH1: Conversion-disable
4	D/A conversion value selection	0001H	Selects user circuit output.
5	D/A conversion timing selection	0001H	Selects user circuit output.
6	DAC LDAC signal selection	0001H	Selects user circuit output.
7	D/A conversion value CH0 (E0)	0000H	Setting is not required (because user circuit output is selected in No.4).
8	D/A conversion value CH1 (E0)	0000H	Setting is not required (because of D/A conversion disable)

■Timing chart example



(1) No processing is performed because the user circuit block is selected in D/A conversion value setting timing selection.

No.	Description
1	Sets the internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) to Start (1) and initializes the DAC register. (After startup, DAC register initialization is performed by F/W.)
2	The data update timing becomes Enable (1) at each cycle set in Data update timing (E0), and the analog output control part operates. (In the timing chart example, the setting becomes disabled because the user circuit block is selected.)

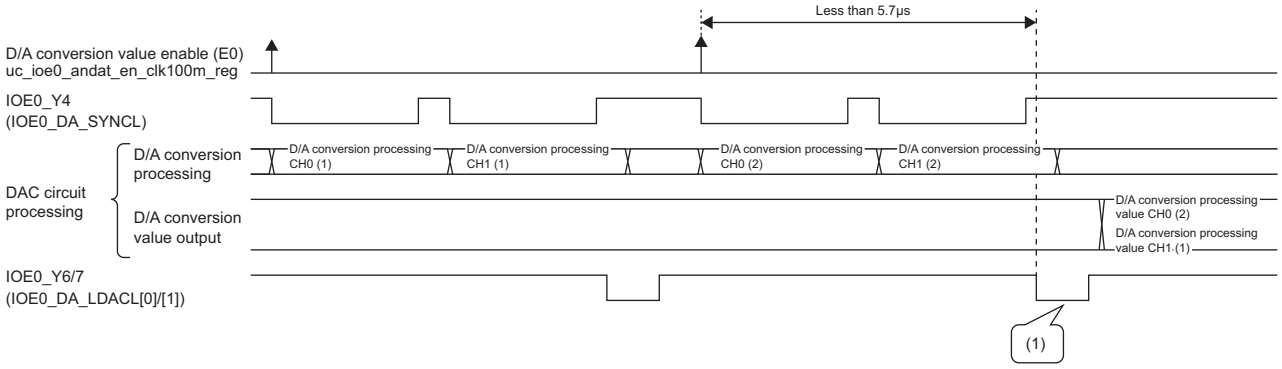
No.	Description
3	Sets the output data to D/A conversion value CH0 (E0) (uc_ioe0_andat_clk100m_reg[15:0]), D/A conversion value CH1 (E0) (uc_ioe0_andat_clk100m_reg[31:16]), and D/A conversion value enable (E0) (uc_ioe0_andat_en_clk100m_reg) to Enable (1).
4	Set D/A conversion value enable (E0) (uc_ioe0_andat_en_clk100m_reg) to Enable(1) when synchronizing between DAC channels, and, after 5.70μs, sets LDAC output CH0-1 (E0) (uc_ioe0_ldac_clk100m_reg) to enable (0) for 300ns.
5	FPGA performs analog output to DAC (IOE0_DA_SYNCL, IOE0_DA_SCLK, IOE0_DA_SDI, IOE0_DA_LDACL[0], IOE0_DA_LDACL[1]).

*1 E0 is explained at the circuit board. E1 and E2 have the same structure.

*2 Changing the data update timing (E0) (tim_ioe0x_conv) (FPGA register address: 1000_2118H) changes the output timing of the analog output (IOE0_DA_SYNCL, IOE0_DA_SCLK, IOE0_DA_SDI, IOE0_DA_LDACL[0], IOE0_DA_LDACL[1]). (For details, refer to ☞ Page 193 Timing generator (tg2_top).)

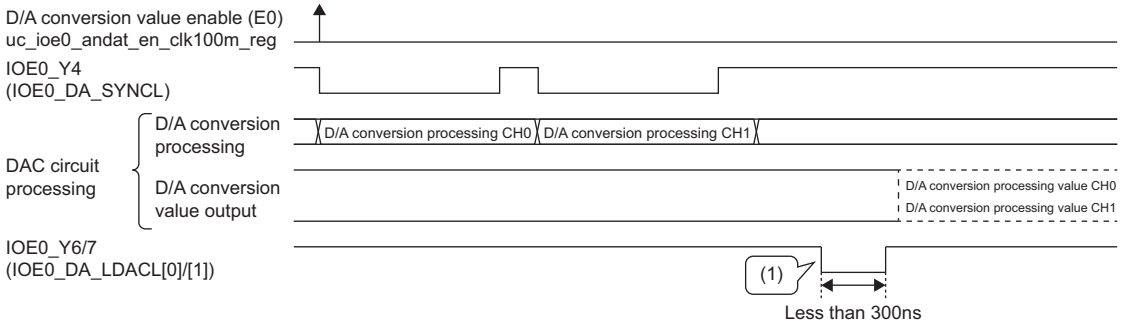
*3 When synchronization between channels is not performed, set LDAC output CH0 (E0) and LDAC output CH1 (E0) to 0 fixed output. When performing inter-channel synchronization, as shown in ☞ Page 231 Analog input/output circuit board (input), set the width between Enable (1) of D/A conversion value enable (E0) and Enable(0b) of LDAC output CH0-1 (E0) to 5.7μs or more. Also, set the effective period of LDAC output CH0-1 (E0) to 300ns or more.

■Operation when D/A conversion enable (E0) to LDAC output CH0-1 (E0) period constraint is violated



(1) Since the D/A conversion processing of the DAC circuit has not been completed, the previous data (D/A conversion processing CH1(1)) may be output.

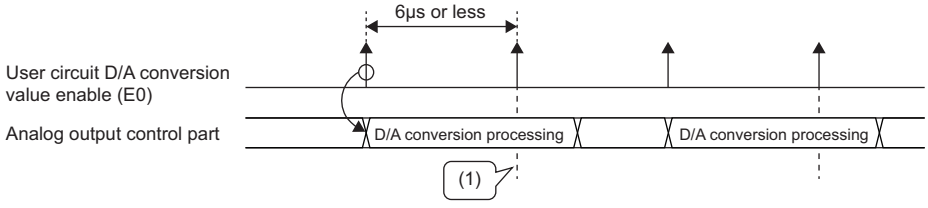
■Operation when LDAC output CH0 (E0) period constraint is violated



(1) The D/A conversion processing value may not be output because the DAC circuit does not recognize the LDAC signal.

*1 If the user circuit block D/A conversion value enable (E0) (uc_ioe0_andat_en_clk100m_reg) is smaller than the minimum setting value of ☞ Page 193 Timing generator (tg2_top)'s data update timing, it will not work properly. After setting the user circuit block D/A conversion value enable (E0) to Enable (1), the analog output control part performs D/A conversion processing. During D/A conversion processing, even if the user circuit block D/A conversion value enable (E0) is enabled, it is ignored by the analog output control part. The operation when the pulse interval is set below the minimum setting value is described below.

■Operation when user circuit D/A conversion value enable (E0) constraint is violated



(1) User circuit D/A conversion value enable (E0) is ignored because D/A conversion processing is in progress.

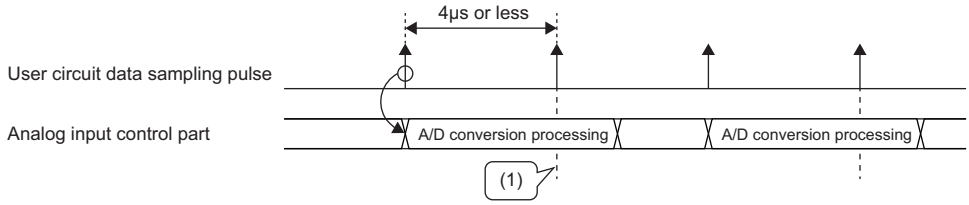
IF specification notes/restrictions

The user circuit IF specification notes/restrictions are shown below.

No.	Description
1	Input/output (input/output declarations inside the RTL, input/output signal names) of the user circuit (uc2_top.v) must not be changed. Set terminals that are not used as input OPEN/output non-dominant fixed.
2	The logging target is 512 bits, but the time information (80 bits) is given in the logging part. Output 432 bits for the logging target output from the user circuit. Set unused bits to 0 fixed output. For details on assigning logging targets output from the sample circuit, refer to the following. ☞ Page 714 Logging Data Bit Assignment
3	For user circuit data sampling pulse, D/A conversion value enable (E0 to E2), and user sampling pulse, do not set them to less than the minimum value described in ☞ Page 193 Timing generator (tg2_top). Otherwise, it will not work properly. The constraint conditions are shown below. • H-significant 1-pulse signal • 1b • The minimum pulse interval is the same as ☞ Page 193 Timing generator (tg2_top). The user circuit data sampling pulse has the same constraints as the analog input/output circuit board for the data sampling timing. D/A conversion enable (E0 to E2) has the same constraints as the analog input/output circuit board for the data update timing. The user sampling pulse has the same constraints as the logging cycle timing pulse. For details, refer to the following. ☞ Page 231 Analog input/output circuit board (input) ☞ Page 220 Logging control (output) Operation when constraint conditions are not met is shown in ☞ Page 236 Operation when pulse interval constraint is violated.
4	Set the width from Enable (1) of D/A conversion value enable (E0) to Enable(0) of LDAC output CH0-1 (E0) to 5.7μs or more. Also, set the effective period of LDAC output CH0-1 (E0) to 300ns or more. Operation when constraint conditions are not met is shown in ☞ Page 236 Operation when LDAC constraint is violated.
5	Set all outputs to the outside of the user circuit to flip-flop output.
6	Use the system clock (clk100m). When generating and using a clock in the user circuit, synchronize the output signal with the system clock (clk100m). Asynchronous processing is not implemented in the standard circuit.
7	Start the operation of the user circuit after activating "Internal operation start/stop". Since the module specific circuit of the standard circuit does not operate while "Internal operation start/stop" is stopped, the signal from the user circuit is ignored. The reset sequence is shown in ☞ Page 237 Reset sequence.
8	When the DC input/output circuit board is selected, the FPGA loads the lower ([7:0]) and upper ([15:8]) of the digital signal ([15:0]) in time division. Note that there is a 100ns lag between the upper and lower parts of the digital signal loading timing.
9	When the differential input/output circuit board is connected, if "Internal operation start/stop" is set to Stop, the output value of the digital signal ([7:0]) that is output to the outside of the FPGA can be specified. Set the output from the user circuit and "Differential output HOLD/CLEAR" according to the device to be connected externally, and output the signal to the outside of the FPGA. Example: When the initial value of the externally connected device is 1b • Set the output of the user circuit part to 1b. • Set "Differential output HOLD/CLEAR" to 1b (CLEAR (1b fixed)).
10	Use the logging control part in the fixed automatic transfer mode by F/W. When designing the user circuit part, output the logging start signal (user circuit part) according to Logging control trigger signal (re_rs_lgdw_ctrl_3_clk100m_reg).

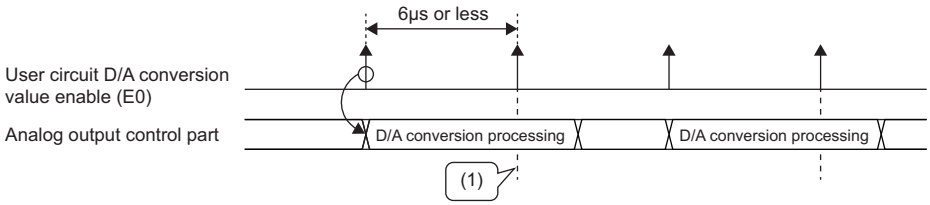
Operation when pulse interval constraint is violated

■For user circuit data sampling pulse



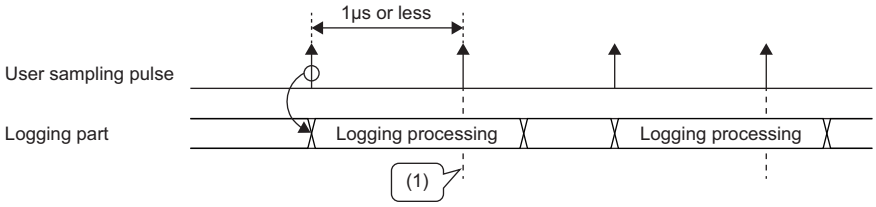
(1) The user circuit data sampling pulse is ignored because A/D conversion processing is in progress.

■For user circuit D/A conversion value enable



(1) User circuit D/A conversion value enable (E0) is ignored because D/A conversion processing is in progress.

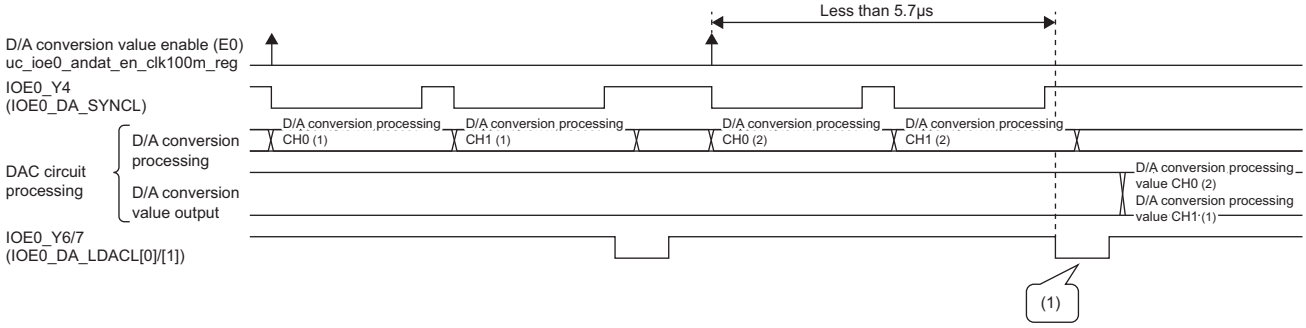
■For user sampling pulse



(1) Ignores user sampling pulses because logging is in progress.

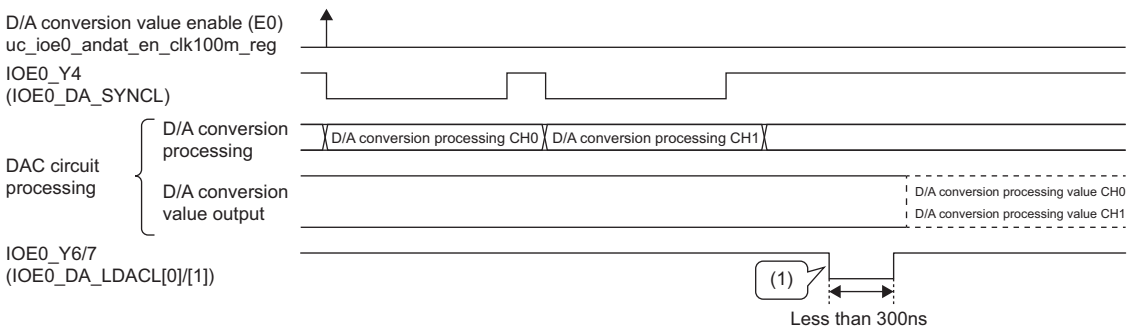
Operation when LDAC constraint is violated

■If the width from D/A conversion value enable(1) to LDAC output enable(0) is less than 5.7µs



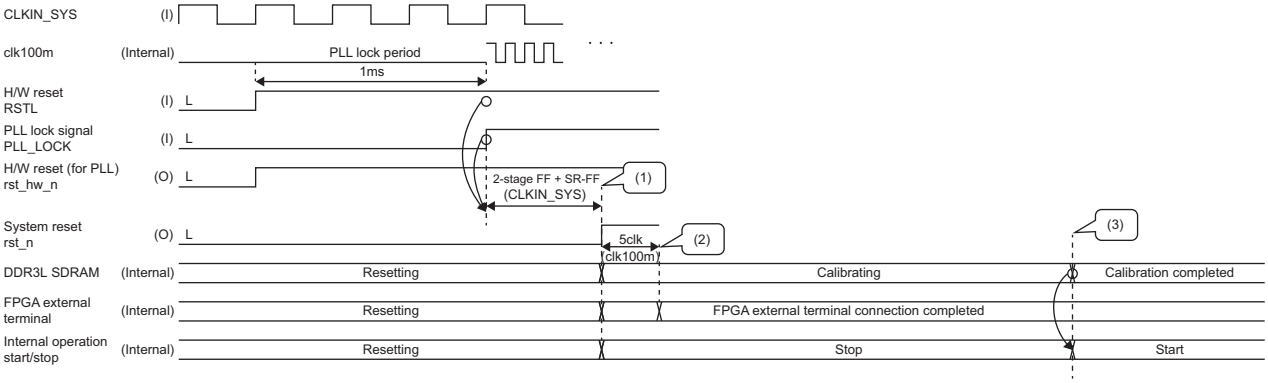
(1) Since the D/A conversion processing of the DAC circuit has not been completed, the previous data (D/A conversion processing CH1(1)) may be output.

■If the LDAC output effective period is less than 300ns



(1) The D/A conversion processing value may not be output because the DAC circuit does not recognize the LDAC signal.

Reset sequence



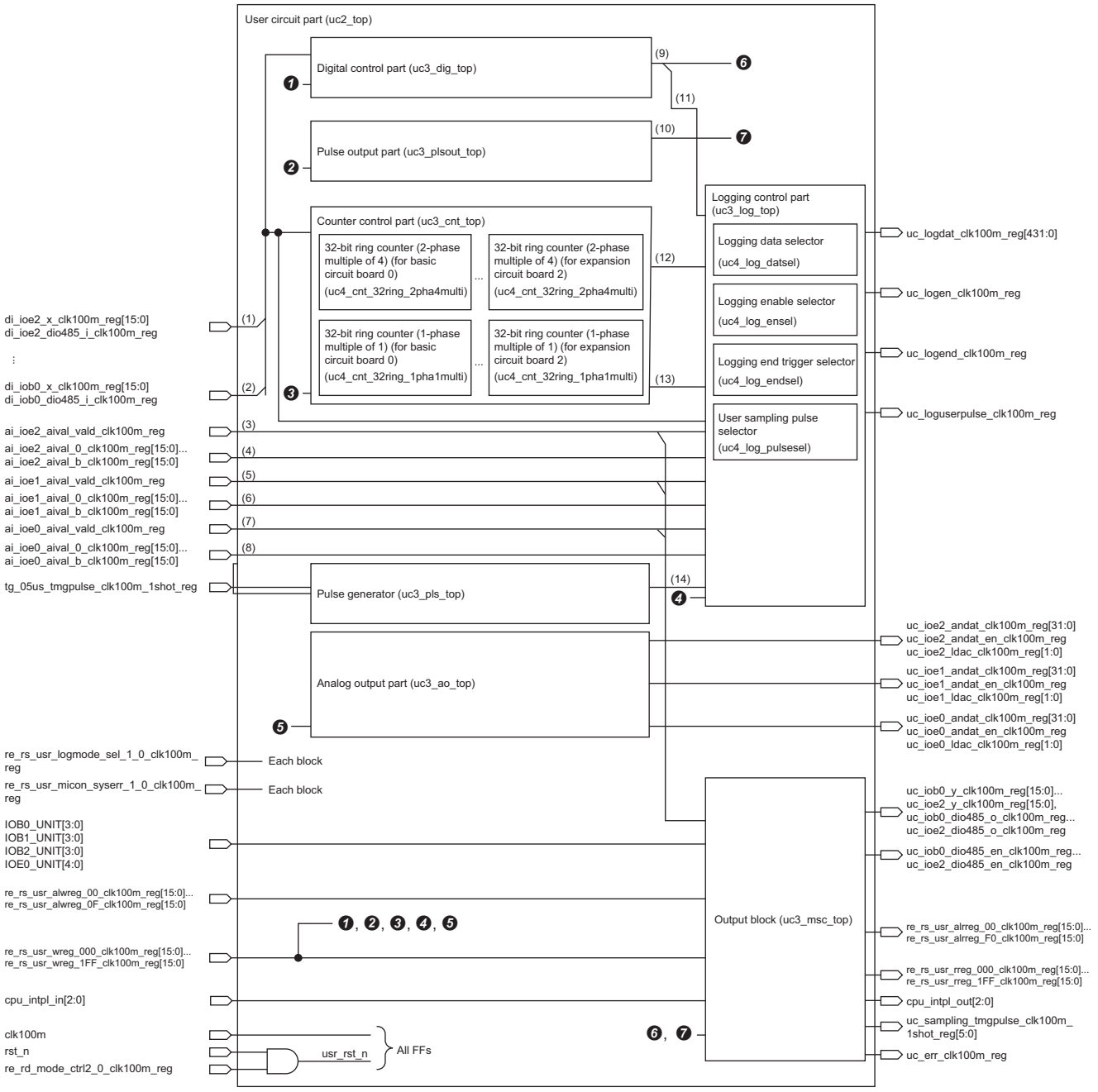
(1) After the H/W reset is released, the reset is executed until the PLL lock becomes enabled. Circuits other than the PLL do not operate.
(2) Switch the connection of the FPGA external terminal inside the FPGA according to the type of circuit board to be connected.
(3) The MCU is notified of the DDR3L SDRAM calibration end. The MCU sets internal operation start/stop to Start(1) and then starts the operation.

Sample circuit

Sample circuit operation details

Sample circuit user circuit block diagram is shown below. Also, the register connections (1) to (6) are shown below.

■Block Diagram



No.	Function classification	Description
❶	Pulse generator (uc3_pls_top)	Generates 1μs pulses for the logging control part. It starts count-up when "Internal operation start/stop" is set to Start (1), and implements a ring counter of the upper limit(1). Count-up starts when a 0.5μs pulse is received from the timing generator. One pulse (clk100m) is output at the upper limit(1).

No.	Function classification	Description
❷	Digital control part[*1] (uc3_dig_top)	Implements the following for the digital signal input from the digital input control part. • Inversion process When the "Digital control part enable/disable control register (IOB0_X0 B0) [1]" is set to Enable (1), the digital signal is inverted and output. If it is set to Disable (0), the signal will be output without inversion. • Digital output enable/disable control When the "Digital control part enable/disable control register (IOB0_X0 B0) [0]" is set to Enable (1), the digital signal after inversion processing is output. If it is set to Disable (0), 0b fixed output will occur.
❸	Counter control part (uc3_cnt_top)	A 32-bit ring counter is implemented. The types of ring counters are as follows. 1. 32-bit ring counter (2-phase multiple of 4) 2. 32-bit ring counter (1-phase multiple of 1) Phase A, Phase B, and Phase Z signals can be set by register areas.
❹	Logging control part (uc3_log_top)	The following functions are implemented to perform logging in the logging part. • Logging data Selects and outputs data to be stored in DDR3L-SDRAM. For data selection, it selects and outputs various counters or analog input from "User circuit logging mode selection [0]". When analog input is selected, 864 bits are output to 432 bits in time division. • Logging start Selects and outputs the logging start signal. The logging start signal is selected and output as 1 bit according to the value set in "Logging control part logging start signal selection". • Logging end trigger Outputs one pulse (clk100m) of the trigger to end logging. 1 bit is selected and output according to the value set in "Logging control part end trigger signal selection".[*2] • User sampling pulse Outputs one pulse (clk100m) of the logging timing. For the selection of the user sampling pulse, 1 bit is selected and output according to the value set in "Logging control part user sampling pulse signal selection".
❺	Pulse output part (uc3_plsout_top)	Sets the pulse width and pulse output count and generates a reference pulse with a constant cycle. Based on the reference pulse, 0, 90, 180, and 270 degree pulses are generated and output to the digital output control part and digital input/output control part.
❻	Analog output part (uc3_ao_top)[*1]	The functions of the analog output part are shown below. • D/A conversion value generation "Analog output part D/A conversion value CH0 (E0)" is output as the D/A conversion value. In addition, the D/A conversion value is output with the previous value held (HOLD) and 0 fixed output (CLEAR) by "MCU system error notification" and "Analog output part HOLD/CLEAR". • D/A conversion value enable generation Detects the rising edge of "Analog output part D/A conversion value valid generation [0]" and outputs D/A conversion value enable (E0). At the same timing, D/A conversion value enable (E0) is notified to the digital input/output control. • Digital input/output control Generates the LDAC signal for inter-channel synchronization. It receives D/A conversion value enable (E0) and generates enable pulse of 300ns (0b enable pulse). The 300ns enable pulse is output from the second pulse of D/A conversion value enable (E0) after reset release. Also, 11b, 00b fixed output is possible by "Analog output part LDAC output selection [1:0]".
❼	Output block part (uc3_msc_top)	■Read data output Controls the signal connected to "Read data (transient area), (cyclic area)". The connection is made by enabling or disabling the setting of "Test mode setting" and selecting the status inside the FPGA and "Write data (transient area), (cyclic area)". The following shows the connection when the test mode setting is enabled/disabled. • Disable Connects "Write data (transient area)" to "Read Data (transient area)". Connects the status of the user circuit to "Read data (transient area)". • Enable Connects writing data (transient area) to read data (transient area). Connects writing data (cyclic area) to read data (cyclic area). ■Always read register output Connects the always write register to the always read register. ■Error signal output Outputs "User circuit error signal generation register [0]". (Output in one flip-flop level (clk100m)) ■Digital output control Selects the pulse output from the pulse output part or the digital output signal from the digital control part and outputs as a digital signal. ■Digital input/output control Selects and outputs the digital control output signal or pulse generation signal from "Digital input/output control digital output selection (B0 to B2, E0 to E2)". ■General-purpose I/O Outputs general-purpose input (cpu_intpl_in) by general-purpose output (cpu_intpl_out)(output in one flip-flop level (clk100m)).[*3] ■Analog control data sampling pulse generation Outputs the signal that detects the rising edge of "Analog control data sampling pulse generation". ■A/D conversion value enable status When an analog input/output circuit board is connected to an extension module (E0, E1, E2), the signal is set by the A/D conversion value enable signal from the analog input control part, and reset when "Internal operation start/stop" is set to Stop(1). The set/reset signal is connected to the read data.

*1 Only CH0 is explained. The same functions are implemented for number of channels for each circuit board. The number of channels to implement multiple is shown below.

No.	Function name	Number of channels	Breakdown
1	Digital control part	102CH	Digital input/output (DC input/output circuit board/differential input/output circuit board): 6 circuit boards × 16 channels Digital input/output (differential input/output circuit board): 6 circuit boards × 1 channel
2	Analog output part	6CH	Analog input/output (analog input/output circuit board): 3 circuit boards × 2 channels

*2 The logging end trigger signal is enabled only in the trigger operation mode. Any input to the logging part in the storage operation mode will be ignored.

*3 The general-purpose I/O is a function for future extension. Output it with 1 fixed.

■User circuit block diagram connection list

No.	Block diagram No.	Connection signal name	Register address
1	❶	re_rs_usr_wreg_000_clk100m_reg[1:0]	1000_B000H
2	❶	re_rs_usr_wreg_001_clk100m_reg[1:0]	1000_B002H
3	❶	re_rs_usr_wreg_002_clk100m_reg[1:0]	1000_B004H
4	❶	re_rs_usr_wreg_003_clk100m_reg[1:0]	1000_B006H
5	❶	re_rs_usr_wreg_004_clk100m_reg[1:0]	1000_B008H
6	❶	re_rs_usr_wreg_005_clk100m_reg[1:0]	1000_B00AH
7	❶	re_rs_usr_wreg_006_clk100m_reg[1:0]	1000_B00CH
8	❶	re_rs_usr_wreg_007_clk100m_reg[1:0]	1000_B00EH
9	❶	re_rs_usr_wreg_008_clk100m_reg[1:0]	1000_B010H
10	❶	re_rs_usr_wreg_009_clk100m_reg[1:0]	1000_B012H
11	❶	re_rs_usr_wreg_00a_clk100m_reg[1:0]	1000_B014H
12	❶	re_rs_usr_wreg_00b_clk100m_reg[1:0]	1000_B016H
13	❶	re_rs_usr_wreg_00c_clk100m_reg[1:0]	1000_B018H
14	❶	re_rs_usr_wreg_00d_clk100m_reg[1:0]	1000_B01AH
15	❶	re_rs_usr_wreg_00e_clk100m_reg[1:0]	1000_B01CH
16	❶	re_rs_usr_wreg_00f_clk100m_reg[1:0]	1000_B01EH
17	❶	re_rs_usr_wreg_014_clk100m_reg[1:0]	1000_B028H
18	❶	re_rs_usr_wreg_015_clk100m_reg[1:0]	1000_B02AH
19	❶	re_rs_usr_wreg_016_clk100m_reg[1:0]	1000_B02CH
20	❶	re_rs_usr_wreg_017_clk100m_reg[1:0]	1000_B02EH
21	❶	re_rs_usr_wreg_018_clk100m_reg[1:0]	1000_B030H
22	❶	re_rs_usr_wreg_019_clk100m_reg[1:0]	1000_B032H
23	❶	re_rs_usr_wreg_01a_clk100m_reg[1:0]	1000_B034H
24	❶	re_rs_usr_wreg_01b_clk100m_reg[1:0]	1000_B036H
25	❶	re_rs_usr_wreg_01c_clk100m_reg[1:0]	1000_B038H
26	❶	re_rs_usr_wreg_01d_clk100m_reg[1:0]	1000_B03AH
27	❶	re_rs_usr_wreg_01e_clk100m_reg[1:0]	1000_B03CH
28	❶	re_rs_usr_wreg_01f_clk100m_reg[1:0]	1000_B03EH
29	❶	re_rs_usr_wreg_020_clk100m_reg[1:0]	1000_B040H
30	❶	re_rs_usr_wreg_021_clk100m_reg[1:0]	1000_B042H
31	❶	re_rs_usr_wreg_022_clk100m_reg[1:0]	1000_B044H
32	❶	re_rs_usr_wreg_023_clk100m_reg[1:0]	1000_B046H
33	❶	re_rs_usr_wreg_028_clk100m_reg[1:0]	1000_B050H
34	❶	re_rs_usr_wreg_029_clk100m_reg[1:0]	1000_B052H
35	❶	re_rs_usr_wreg_02a_clk100m_reg[1:0]	1000_B054H
36	❶	re_rs_usr_wreg_02b_clk100m_reg[1:0]	1000_B056H
37	❶	re_rs_usr_wreg_02c_clk100m_reg[1:0]	1000_B058H
38	❶	re_rs_usr_wreg_02d_clk100m_reg[1:0]	1000_B05AH
39	❶	re_rs_usr_wreg_02e_clk100m_reg[1:0]	1000_B05CH
40	❶	re_rs_usr_wreg_02f_clk100m_reg[1:0]	1000_B05EH
41	❶	re_rs_usr_wreg_030_clk100m_reg[1:0]	1000_B060H
42	❶	re_rs_usr_wreg_031_clk100m_reg[1:0]	1000_B062H
43	❶	re_rs_usr_wreg_032_clk100m_reg[1:0]	1000_B064H
44	❶	re_rs_usr_wreg_033_clk100m_reg[1:0]	1000_B066H
45	❶	re_rs_usr_wreg_034_clk100m_reg[1:0]	1000_B068H
46	❶	re_rs_usr_wreg_035_clk100m_reg[1:0]	1000_B06AH
47	❶	re_rs_usr_wreg_036_clk100m_reg[1:0]	1000_B06CH
48	❶	re_rs_usr_wreg_037_clk100m_reg[1:0]	1000_B06EH
49	❶	re_rs_usr_wreg_03c_clk100m_reg[1:0]	1000_B078H
50	❶	re_rs_usr_wreg_03d_clk100m_reg[1:0]	1000_B07AH
51	❶	re_rs_usr_wreg_03e_clk100m_reg[1:0]	1000_B07CH

No.	Block diagram No.	Connection signal name	Register address
52	❶	re_rs_usr_wreg_03f_clk100m_reg[1:0]	1000_B07EH
53	❶	re_rs_usr_wreg_040_clk100m_reg[1:0]	1000_B080H
54	❶	re_rs_usr_wreg_041_clk100m_reg[1:0]	1000_B082H
55	❶	re_rs_usr_wreg_042_clk100m_reg[1:0]	1000_B084H
56	❶	re_rs_usr_wreg_043_clk100m_reg[1:0]	1000_B086H
57	❶	re_rs_usr_wreg_044_clk100m_reg[1:0]	1000_B088H
58	❶	re_rs_usr_wreg_045_clk100m_reg[1:0]	1000_B08AH
59	❶	re_rs_usr_wreg_046_clk100m_reg[1:0]	1000_B08CH
60	❶	re_rs_usr_wreg_047_clk100m_reg[1:0]	1000_B08EH
61	❶	re_rs_usr_wreg_048_clk100m_reg[1:0]	1000_B090H
62	❶	re_rs_usr_wreg_049_clk100m_reg[1:0]	1000_B092H
63	❶	re_rs_usr_wreg_04a_clk100m_reg[1:0]	1000_B094H
64	❶	re_rs_usr_wreg_04b_clk100m_reg[1:0]	1000_B096H
65	❶	re_rs_usr_wreg_050_clk100m_reg[1:0]	1000_B0A0H
66	❶	re_rs_usr_wreg_051_clk100m_reg[1:0]	1000_B0A2H
67	❶	re_rs_usr_wreg_052_clk100m_reg[1:0]	1000_B0A4H
68	❶	re_rs_usr_wreg_053_clk100m_reg[1:0]	1000_B0A6H
69	❶	re_rs_usr_wreg_054_clk100m_reg[1:0]	1000_B0A8H
70	❶	re_rs_usr_wreg_055_clk100m_reg[1:0]	1000_B0AAH
71	❶	re_rs_usr_wreg_056_clk100m_reg[1:0]	1000_B0ACH
72	❶	re_rs_usr_wreg_057_clk100m_reg[1:0]	1000_B0AEH
73	❶	re_rs_usr_wreg_058_clk100m_reg[1:0]	1000_B0B0H
74	❶	re_rs_usr_wreg_059_clk100m_reg[1:0]	1000_B0B2H
75	❶	re_rs_usr_wreg_05a_clk100m_reg[1:0]	1000_B0B4H
76	❶	re_rs_usr_wreg_05b_clk100m_reg[1:0]	1000_B0B6H
77	❶	re_rs_usr_wreg_05c_clk100m_reg[1:0]	1000_B0B8H
78	❶	re_rs_usr_wreg_05d_clk100m_reg[1:0]	1000_B0BAH
79	❶	re_rs_usr_wreg_05e_clk100m_reg[1:0]	1000_B0BCH
80	❶	re_rs_usr_wreg_05f_clk100m_reg[1:0]	1000_B0BEH
81	❶	re_rs_usr_wreg_064_clk100m_reg[1:0]	1000_B0C8H
82	❶	re_rs_usr_wreg_065_clk100m_reg[1:0]	1000_B0CAH
83	❶	re_rs_usr_wreg_066_clk100m_reg[1:0]	1000_B0CCH
84	❶	re_rs_usr_wreg_067_clk100m_reg[1:0]	1000_B0CEH
85	❶	re_rs_usr_wreg_068_clk100m_reg[1:0]	1000_B0D0H
86	❶	re_rs_usr_wreg_069_clk100m_reg[1:0]	1000_B0D2H
87	❶	re_rs_usr_wreg_06a_clk100m_reg[1:0]	1000_B0D4H
88	❶	re_rs_usr_wreg_06b_clk100m_reg[1:0]	1000_B0D6H
89	❶	re_rs_usr_wreg_06c_clk100m_reg[1:0]	1000_B0D8H
90	❶	re_rs_usr_wreg_06d_clk100m_reg[1:0]	1000_B0DAH
91	❶	re_rs_usr_wreg_06e_clk100m_reg[1:0]	1000_B0DCH
92	❶	re_rs_usr_wreg_06f_clk100m_reg[1:0]	1000_B0DEH
93	❶	re_rs_usr_wreg_070_clk100m_reg[1:0]	1000_B0E0H
94	❶	re_rs_usr_wreg_071_clk100m_reg[1:0]	1000_B0E2H
95	❶	re_rs_usr_wreg_072_clk100m_reg[1:0]	1000_B0E4H
96	❶	re_rs_usr_wreg_073_clk100m_reg[1:0]	1000_B0E6H
103	❶	re_rs_usr_wreg_080_clk100m_reg[2:0]	1000_B100H
104	❶	re_rs_usr_wreg_081_clk100m_reg[2:0]	1000_B102H
105	❶	re_rs_usr_wreg_082_clk100m_reg[2:0]	1000_B104H
106	❶	re_rs_usr_wreg_083_clk100m_reg[2:0]	1000_B106H
107	❶	re_rs_usr_wreg_084_clk100m_reg[2:0]	1000_B108H
108	❶	re_rs_usr_wreg_085_clk100m_reg[2:0]	1000_B10AH
112	❹	re_rs_usr_wreg_091_clk100m_reg[7:0]	1000_B122H
113	❹	re_rs_usr_wreg_092_clk100m_reg[7:0]	1000_B124H

No.	Block diagram No.	Connection signal name	Register address
114	❹	re_rs_usr_wreg_093_clk100m_reg[6:0]	1000_B126H
115	❹	re_rs_usr_wreg_094_clk100m_reg[0]	1000_B128H
330	❹	re_rs_usr_wreg_095_clk100m_reg[0]	1000_B12AH
120	❸	re_rs_usr_wreg_0a3_clk100m_reg[15:0]	1000_B146H
121	❸	re_rs_usr_wreg_0a4_clk100m_reg[15:0]	1000_B148H
122	❸	re_rs_usr_wreg_0a5_clk100m_reg[5:0]	1000_B14AH
123	❸	re_rs_usr_wreg_0a5_clk100m_reg[13:8]	1000_B14AH
127	❸	re_rs_usr_wreg_0ab_clk100m_reg[15:0]	1000_B156H
128	❸	re_rs_usr_wreg_0ac_clk100m_reg[15:0]	1000_B158H
129	❸	re_rs_usr_wreg_0ad_clk100m_reg[5:0]	1000_B15AH
130	❸	re_rs_usr_wreg_0ad_clk100m_reg[13:8]	1000_B15AH
134	❸	re_rs_usr_wreg_0b3_clk100m_reg[15:0]	1000_B166H
135	❸	re_rs_usr_wreg_0b4_clk100m_reg[15:0]	1000_B168H
136	❸	re_rs_usr_wreg_0b5_clk100m_reg[5:0]	1000_B16AH
137	❸	re_rs_usr_wreg_0b5_clk100m_reg[13:8]	1000_B16AH
141	❸	re_rs_usr_wreg_0bb_clk100m_reg[15:0]	1000_B176H
142	❸	re_rs_usr_wreg_0bc_clk100m_reg[15:0]	1000_B178H
143	❸	re_rs_usr_wreg_0bd_clk100m_reg[5:0]	1000_B17AH
144	❸	re_rs_usr_wreg_0bd_clk100m_reg[13:8]	1000_B17AH
148	❸	re_rs_usr_wreg_0c3_clk100m_reg[15:0]	1000_B186H
149	❸	re_rs_usr_wreg_0c4_clk100m_reg[15:0]	1000_B188H
150	❸	re_rs_usr_wreg_0c5_clk100m_reg[5:0]	1000_B18AH
151	❸	re_rs_usr_wreg_0c5_clk100m_reg[13:8]	1000_B18AH
155	❸	re_rs_usr_wreg_0cb_clk100m_reg[15:0]	1000_B196H
156	❸	re_rs_usr_wreg_0cc_clk100m_reg[15:0]	1000_B198H
157	❸	re_rs_usr_wreg_0cd_clk100m_reg[5:0]	1000_B19AH
158	❸	re_rs_usr_wreg_0cd_clk100m_reg[13:8]	1000_B19AH
162	❸	re_rs_usr_wreg_0d3_clk100m_reg[15:0]	1000_B1A6H
163	❸	re_rs_usr_wreg_0d4_clk100m_reg[15:0]	1000_B1A8H
164	❸	re_rs_usr_wreg_0d5_clk100m_reg[5:0]	1000_B1AAH
165	❸	re_rs_usr_wreg_0d5_clk100m_reg[13:8]	1000_B1AAH
169	❸	re_rs_usr_wreg_0db_clk100m_reg[15:0]	1000_B1B6H
170	❸	re_rs_usr_wreg_0dc_clk100m_reg[15:0]	1000_B1B8H
171	❸	re_rs_usr_wreg_0dd_clk100m_reg[5:0]	1000_B1BAH
172	❸	re_rs_usr_wreg_0dd_clk100m_reg[13:8]	1000_B1BAH
176	❸	re_rs_usr_wreg_0e3_clk100m_reg[15:0]	1000_B1C6H
177	❸	re_rs_usr_wreg_0e4_clk100m_reg[15:0]	1000_B1C8H
178	❸	re_rs_usr_wreg_0e5_clk100m_reg[5:0]	1000_B1CAH
179	❸	re_rs_usr_wreg_0e5_clk100m_reg[13:8]	1000_B1CAH
183	❸	re_rs_usr_wreg_0eb_clk100m_reg[15:0]	1000_B1D6H
184	❸	re_rs_usr_wreg_0ec_clk100m_reg[15:0]	1000_B1D8H
185	❸	re_rs_usr_wreg_0ed_clk100m_reg[5:0]	1000_B1DAH
186	❸	re_rs_usr_wreg_0ed_clk100m_reg[13:8]	1000_B1DAh
190	❸	re_rs_usr_wreg_0f3_clk100m_reg[15:0]	1000_B1E6h
191	❸	re_rs_usr_wreg_0f4_clk100m_reg[15:0]	1000_B1E8H
192	❸	re_rs_usr_wreg_0f5_clk100m_reg[5:0]	1000_B1EAH
193	❸	re_rs_usr_wreg_0f5_clk100m_reg[13:8]	1000_B1EAH
197	❸	re_rs_usr_wreg_0fb_clk100m_reg[15:0]	1000_B1F6H
198	❸	re_rs_usr_wreg_0fc_clk100m_reg[15:0]	1000_B1F8H
199	❸	re_rs_usr_wreg_0fd_clk100m_reg[5:0]	1000_B1FAH
200	❸	re_rs_usr_wreg_0fd_clk100m_reg[13:8]	1000_B1FAH
206	❷	re_rs_usr_wreg_110_clk100m_reg[15:0]	1000_B220H
207	❷	re_rs_usr_wreg_111_clk100m_reg[15:0]	1000_B222H

No.	Block diagram No.	Connection signal name	Register address
208	❷	re_rs_usr_wreg_112_clk100m_reg[15:0]	1000_B224H
209	❷	re_rs_usr_wreg_113_clk100m_reg[15:0]	1000_B226H
211	❷	re_rs_usr_wreg_115_clk100m_reg[15:0]	1000_B22AH
212	❷	re_rs_usr_wreg_116_clk100m_reg[15:0]	1000_B22CH
213	❷	re_rs_usr_wreg_117_clk100m_reg[15:0]	1000_B22EH
214	❷	re_rs_usr_wreg_118_clk100m_reg[15:0]	1000_B230H
216	❷	re_rs_usr_wreg_11a_clk100m_reg[15:0]	1000_B234H
217	❷	re_rs_usr_wreg_11b_clk100m_reg[15:0]	1000_B236H
218	❷	re_rs_usr_wreg_11c_clk100m_reg[15:0]	1000_B238H
219	❷	re_rs_usr_wreg_11d_clk100m_reg[15:0]	1000_B23AH
221	❷	re_rs_usr_wreg_11f_clk100m_reg[15:0]	1000_B23EH
222	❷	re_rs_usr_wreg_120_clk100m_reg[15:0]	1000_B240H
223	❷	re_rs_usr_wreg_121_clk100m_reg[15:0]	1000_B242H
224	❷	re_rs_usr_wreg_122_clk100m_reg[15:0]	1000_B244H
226	❷	re_rs_usr_wreg_124_clk100m_reg[15:0]	1000_B248H
227	❷	re_rs_usr_wreg_125_clk100m_reg[15:0]	1000_B24AH
228	❷	re_rs_usr_wreg_126_clk100m_reg[15:0]	1000_B24CH
229	❷	re_rs_usr_wreg_127_clk100m_reg[15:0]	1000_B24EH
231	❷	re_rs_usr_wreg_129_clk100m_reg[15:0]	1000_B252H
232	❷	re_rs_usr_wreg_12a_clk100m_reg[15:0]	1000_B254H
233	❷	re_rs_usr_wreg_12b_clk100m_reg[15:0]	1000_B256H
234	❷	re_rs_usr_wreg_12c_clk100m_reg[15:0]	1000_B258H
236	❷	re_rs_usr_wreg_130_clk100m_reg[15:0]	1000_B260H
237	❷	re_rs_usr_wreg_131_clk100m_reg[15:0]	1000_B262H
238	❷	re_rs_usr_wreg_132_clk100m_reg[1:0]	1000_B264H
239	❷	re_rs_usr_wreg_133_clk100m_reg[15:0]	1000_B266H
240	❷	re_rs_usr_wreg_134_clk100m_reg[15:0]	1000_B268H
241	❷	re_rs_usr_wreg_135_clk100m_reg[1:0]	1000_B26AH
242	❷	re_rs_usr_wreg_136_clk100m_reg[15:0]	1000_B26CH
243	❷	re_rs_usr_wreg_137_clk100m_reg[15:0]	1000_B26EH
244	❷	re_rs_usr_wreg_138_clk100m_reg[1:0]	1000_B270H
245	❷	re_rs_usr_wreg_139_clk100m_reg[15:0]	1000_B272H
246	❷	re_rs_usr_wreg_13a_clk100m_reg[15:0]	1000_B274H
247	❷	re_rs_usr_wreg_13b_clk100m_reg[1:0]	1000_B276H
248	❷	re_rs_usr_wreg_13c_clk100m_reg[15:0]	1000_B278H
249	❷	re_rs_usr_wreg_13d_clk100m_reg[15:0]	1000_B27AH
250	❷	re_rs_usr_wreg_13e_clk100m_reg[1:0]	1000_B27CH
251	❷	re_rs_usr_wreg_13f_clk100m_reg[15:0]	1000_B27EH
252	❷	re_rs_usr_wreg_140_clk100m_reg[15:0]	1000_B280H
253	❷	re_rs_usr_wreg_141_clk100m_reg[1:0]	1000_B282H
254	❷	re_rs_usr_wreg_142_clk100m_reg[15:0]	1000_B284H
255	❷	re_rs_usr_wreg_143_clk100m_reg[0]	1000_B286H
256	❷	re_rs_usr_wreg_144_clk100m_reg[15:0]	1000_B288H
257	❷	re_rs_usr_wreg_145_clk100m_reg[0]	1000_B28AH
258	❷	re_rs_usr_wreg_146_clk100m_reg[15:0]	1000_B28CH
259	❷	re_rs_usr_wreg_147_clk100m_reg[0]	1000_B28EH
260	❷	re_rs_usr_wreg_148_clk100m_reg[15:0]	1000_B290H
261	❷	re_rs_usr_wreg_149_clk100m_reg[0]	1000_B292H
262	❷	re_rs_usr_wreg_14a_clk100m_reg[15:0]	1000_B294H
263	❷	re_rs_usr_wreg_14b_clk100m_reg[0]	1000_B296H
264	❷	re_rs_usr_wreg_14c_clk100m_reg[15:0]	1000_B298H
265	❷	re_rs_usr_wreg_14d_clk100m_reg[0]	1000_B29AH
273	❺	re_rs_usr_wreg_160_clk100m_reg[5:0]	1000_B2C0H

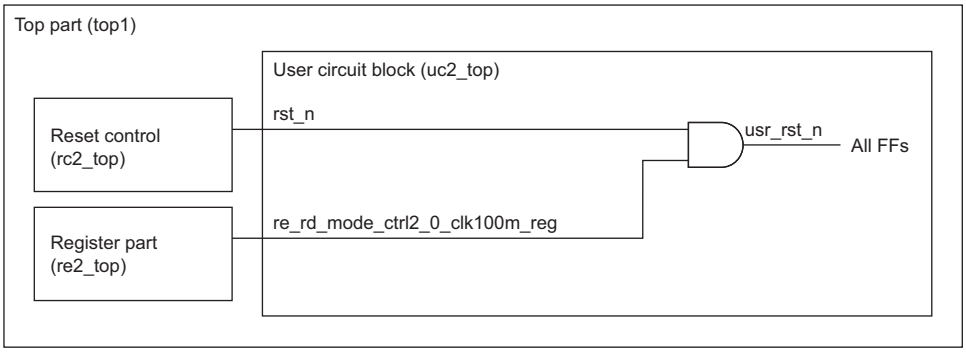
No.	Block diagram No.	Connection signal name	Register address
274	❺	re_rs_usr_wreg_168_clk100m_reg[0]	1000_B2D0H
277	❹	re_rs_usr_wreg_180_clk100m_reg[1:0]	1000_B300H
278	❹	re_rs_usr_wreg_181_clk100m_reg[0]	1000_B302H
279	❸	re_rs_usr_wreg_188_clk100m_reg[0]	1000_B310H
280	❸	re_rs_usr_wreg_189_clk100m_reg[15:0]	1000_B312H
281	❸	re_rs_usr_wreg_18a_clk100m_reg[15:0]	1000_B314H
282	❸	re_rs_usr_wreg_18b_clk100m_reg[0]	1000_B316H
283	❸	re_rs_usr_wreg_18c_clk100m_reg[15:0]	1000_B318H
284	❸	re_rs_usr_wreg_18d_clk100m_reg[15:0]	1000_B31AH
285	❸	re_rs_usr_wreg_18e_clk100m_reg[0]	1000_B31CH
286	❸	re_rs_usr_wreg_18f_clk100m_reg[15:0]	1000_B31EH
287	❸	re_rs_usr_wreg_190_clk100m_reg[15:0]	1000_B320H
288	❸	re_rs_usr_wreg_191_clk100m_reg[0]	1000_B322H
289	❸	re_rs_usr_wreg_192_clk100m_reg[15:0]	1000_B324H
290	❸	re_rs_usr_wreg_193_clk100m_reg[15:0]	1000_B326H
291	❸	re_rs_usr_wreg_194_clk100m_reg[0]	1000_B328H
292	❸	re_rs_usr_wreg_195_clk100m_reg[15:0]	1000_B32AH
293	❸	re_rs_usr_wreg_196_clk100m_reg[15:0]	1000_B32CH
294	❸	re_rs_usr_wreg_197_clk100m_reg[0]	1000_B32EH
295	❸	re_rs_usr_wreg_198_clk100m_reg[15:0]	1000_B330H
296	❸	re_rs_usr_wreg_199_clk100m_reg[15:0]	1000_B332H
297	❸	re_rs_usr_wreg_1a0_clk100m_reg[0]	1000_B340H
298	❸	re_rs_usr_wreg_1a1_clk100m_reg[15:0]	1000_B342H
299	❸	re_rs_usr_wreg_1a2_clk100m_reg[15:0]	1000_B344H
300	❸	re_rs_usr_wreg_1a3_clk100m_reg[0]	1000_B346H
301	❸	re_rs_usr_wreg_1a4_clk100m_reg[15:0]	1000_B348H
302	❸	re_rs_usr_wreg_1a5_clk100m_reg[15:0]	1000_B34AH
303	❸	re_rs_usr_wreg_1a6_clk100m_reg[0]	1000_B34CH
304	❸	re_rs_usr_wreg_1a7_clk100m_reg[15:0]	1000_B34EH
305	❸	re_rs_usr_wreg_1a8_clk100m_reg[15:0]	1000_B350H
306	❸	re_rs_usr_wreg_1a9_clk100m_reg[0]	1000_B352H
307	❸	re_rs_usr_wreg_1aa_clk100m_reg[15:0]	1000_B354H
308	❸	re_rs_usr_wreg_1ab_clk100m_reg[15:0]	1000_B356H
309	❸	re_rs_usr_wreg_1ac_clk100m_reg[0]	1000_B358H
310	❸	re_rs_usr_wreg_1ad_clk100m_reg[15:0]	1000_B35AH
311	❸	re_rs_usr_wreg_1ae_clk100m_reg[15:0]	1000_B35CH
312	❸	re_rs_usr_wreg_1af_clk100m_reg[0]	1000_B35EH
313	❸	re_rs_usr_wreg_1b0_clk100m_reg[15:0]	1000_B360H
314	❸	re_rs_usr_wreg_1b1_clk100m_reg[15:0]	1000_B362H
315	❷	re_rs_usr_wreg_1b8_clk100m_reg[0]	1000_B370H
316	❷	re_rs_usr_wreg_1b9_clk100m_reg[0]	1000_B372H
317	❷	re_rs_usr_wreg_1ba_clk100m_reg[0]	1000_B374H
318	❷	re_rs_usr_wreg_1bb_clk100m_reg[0]	1000_B376H
319	❷	re_rs_usr_wreg_1bc_clk100m_reg[0]	1000_B378H
320	❷	re_rs_usr_wreg_1bd_clk100m_reg[0]	1000_B37AH
321	❺	re_rs_usr_wreg_1c0_clk100m_reg[15:0]	1000_B380H
322	❺	re_rs_usr_wreg_1c1_clk100m_reg[15:0]	1000_B382H
323	❺	re_rs_usr_wreg_1c2_clk100m_reg[15:0]	1000_B384H
324	❺	re_rs_usr_wreg_1c3_clk100m_reg[15:0]	1000_B386H
325	❺	re_rs_usr_wreg_1c4_clk100m_reg[15:0]	1000_B388H
326	❺	re_rs_usr_wreg_1c5_clk100m_reg[15:0]	1000_B38AH
327	❺	re_rs_usr_wreg_1c6_clk100m_reg[2:0]	1000_B38CH

Clock system

The user circuit clock is a single system clock (clk100m).

Reset system

The reset system diagram of the user circuit is shown below.



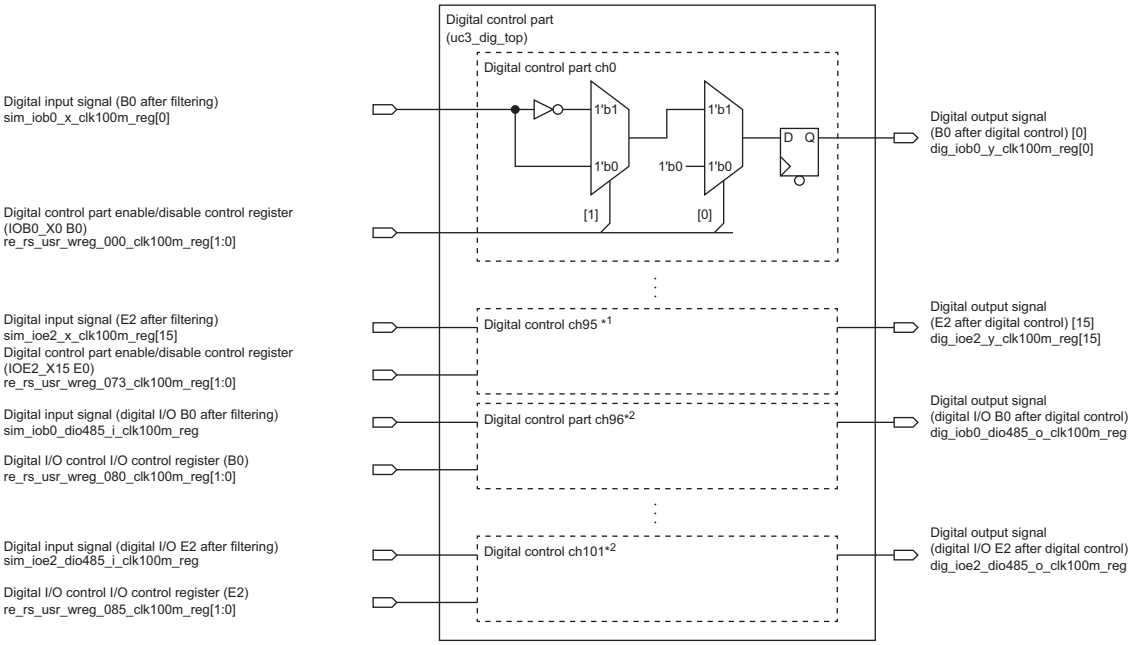
As shown in the diagram, two resets are input. The application range is as follows.

- rst_n: Reset
- re_rd_mode_ctrl2_0_clk100m_reg: Internal operation start/stop

Digital control part (uc3_dig_top)

This module controls inversion processing and enable/disable of digital output for the digital input signal (after filtering) that is input from the digital input control part. The block diagram, function list, and terminal list of the digital input control part are shown below.

■Digital control part block diagram



*1 Digital control part ch1 to ch95 have the same structure as digital control part ch0. They are output to the output block part and the logging control part.

*2 Digital control part ch96 to ch101 have the same structure as digital control part ch0. They are output to the output block part and the logging control part.

■Digital control part function list

No.	Function	Overview	Remarks
1	Inversion process	Inverts the digital input signal (after filtering) and outputs it to Digital output enable/disable control. When "Digital control part enable/disable control register (IOB0_X0 B0)" [1] is set to Enable (1), the digital input signal (after filtering) is inverted. If it is set to Disable (0), through output occurs at Digital output enable/disable control.	—
2	Digital output enable/disable control	Selects whether or not to output the inverted digital input signal (after filtering) to the digital output signal (after digital control). When "Digital control part enable/disable control register (IOB0_X0B0)" [0] is set to Enable (1), the inverted digital input signal after inversion processing (after filtering) is directly output to the digital output signal (after digital control). When it is set to Disable (0), 0b is output to the digital output signal (after digital control).	—

■Digital control part terminal list

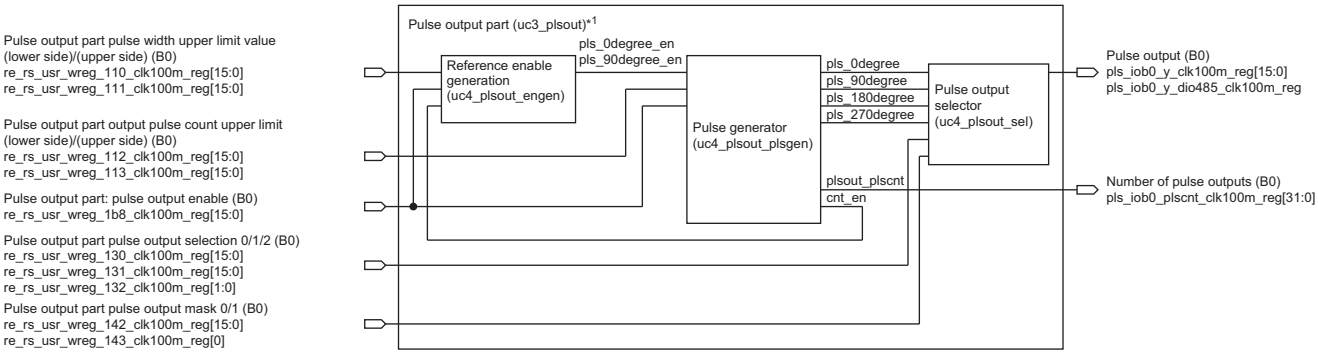
No.	Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
1	clk100m	I	—	System clock	cc2_top	—	—
2	usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	0b	—
3	sim_iob0_x_clk100m_reg[15:0]	I	—	Digital input signal (B0 after filtering)	di2_top	0000h	—
4	sim_iob1_x_clk100m_reg[15:0]	I	—	Digital input signal (B1 after filtering)	di2_top	0000h	—
5	sim_iob2_x_clk100m_reg[15:0]	I	—	Digital input signal (B2 after filtering)	di2_top	0000h	—
6	sim_ioe0_x_clk100m_reg[15:0]	I	—	Digital input signal (E0 after filtering)	di2_top	0000h	—
7	sim_ioe1_x_clk100m_reg[15:0]	I	—	Digital input signal (E1 after filtering)	di2_top	0000h	—
8	sim_ioe2_x_clk100m_reg[15:0]	I	—	Digital input signal (E2 after filtering)	di2_top	0000h	—
9	sim_iob0_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output B0)	dio2_top	0b	—
10	sim_iob1_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output B1)	dio2_top	0b	—
11	sim_iob2_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output B2)	dio2_top	0b	—
12	sim_ioe0_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output E0)	dio2_top	0b	—
13	sim_ioe1_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output E1)	dio2_top	0b	—
14	sim_ioe2_dio485_i_clk100m_reg	I	—	Digital input signal (filtered digital input/output E2)	dio2_top	0b	—
15	re_rs_usr_wreg_000_clk100m_reg[1:0] to re_rs_usr_wreg_00f_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOB0_X0 B0) to Digital control part enable/disable control register (IOB0_XF B0)	re2_top	All 0	—
28	re_rs_usr_wreg_014_clk100m_reg[1:0] to re_rs_usr_wreg_023_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOB0_X0 B1) to Digital control part enable/disable control register (IOB0_XF B1)	re2_top	All 0	—
29	re_rs_usr_wreg_028_clk100m_reg[1:0] to re_rs_usr_wreg_037_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOB2_X0 B2) to Digital control part enable/disable control register (IOB2_XF B2)	re2_top	All 0	—
30	re_rs_usr_wreg_03c_clk100m_reg[1:0] to re_rs_usr_wreg_04b_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOE0_X0 E0) to Digital control part enable/disable control register (IOE0_XF E0)	re2_top	All 0	—
31	re_rs_usr_wreg_050_clk100m_reg[1:0] to re_rs_usr_wreg_05f_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOE1_X0 E1) to Digital control part enable/disable control register (IOE1_XF E1)	re2_top	All 0	—
32	re_rs_usr_wreg_064_clk100m_reg[1:0] to re_rs_usr_wreg_073_clk100m_reg[1:0]	I	—	Digital control part enable/disable control register (IOE2_X0 E2) to Digital control part enable/disable control register (IOE2_XF E2)	re2_top	All 0	—
33	re_rs_usr_wreg_080_clk100m_reg[1:0] to re_rs_usr_wreg_085_clk100m_reg[1:0]	I	—	Digital input/output control input/output control register (B0) to Digital input/output control input/output control register (E2)	re2_top	All 0	—
16	dig_iob0_y_clk100m_reg [15:0]	O	—	Digital output signal (B0 after digital control)	Logging control part, output block part	0000h	—
17	dig_iob1_y_clk100m_reg [15:0]	O	—	Digital output signal (B1 after digital control)	Logging control part, output block part	0000h	—

No.	Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
18	dig_iob2_y_clk100m_reg [15:0]	O	—	Digital output signal (B2 after digital control)	Logging control part, output block part	0000h	—
19	dig_ioe0_y_clk100m_reg [15:0]	O	—	Digital output signal (E0 after digital control)	Logging control part, output block part	0000h	—
20	dig_ioe1_y_clk100m_reg [15:0]	O	—	Digital output signal (E1 after digital control)	Logging control part, output block part	0000h	—
21	dig_ioe2_y_clk100m_reg [15:0]	O	—	Digital output signal (E2 after digital control)	Logging control part, output block part	0000h	—
22	dig_iob0_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output B0 after digital control)	Output block part	0b	—
23	dig_iob1_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output B1 after digital control)	Output block part	0b	—
24	dig_iob2_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output B2 after digital control)	Output block part	0b	—
25	dig_ioe0_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output E0 after digital control)	Output block part	0b	—
26	dig_ioe1_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output E1 after digital control)	Output block part	0b	—
27	dig_ioe2_dio485_o_clk100m_reg	O	—	Digital output signal (digital input/output E2 after digital control)	Output block part	0b	—

Pulse output part (uc3_plsout)

This module sets the pulse width and the pulse output count, and outputs 0, 90, 180, and 270 degree pulses with a constant cycle. The block diagram, function list, and terminal list of the pulse output part are shown below.

■Pulse output part block diagram



*1 B1, B2, E0, E1, and E2 also have the same structure.

■Pulse output part function list

No.	Function	Overview	Remarks
1	Reference enable generation	Generates an enable signal that generates a pulse. A 32-bit ring counter whose upper limit is "Pulse output part pulse width upper limit value" is implemented. The following enable signals are generated based on the 32-bit ring counter. ■Enable signal • 0 degree enable Outputs when the value of the 32-bit ring counter becomes equal to the value obtained by bit-shifting (1/2 value) "Pulse output part pulse width upper limit value (B0)". (1 pulse (clk100m)) • 90 degree enable Outputs when the value of the 32-bit ring counter becomes equal to "Pulse output part pulse width upper limit value (lower side)/(upper side) (B0)". (1 pulse (clk100m))	—
2	Pulse generation	Generates 0-degree pulse and 90-degree pulse based on 0-degree enable and 90-degree enable from reference enable generation. The 0-degree pulse and 90-degree pulse are output as 180- and 270-degree pulses after being shifted with 0-degree enable and 90-degree enable. ■Output pulse • 0 degree pulse • 90 degree pulse • 180 degree pulse • 270 degree pulse In addition, the number of pulses set in "Pulse output part output pulse number upper limit (lower side)/(upper side) (B0)" is output. The number of pulses that have been output can be checked using "Pulse output part pulse output count (lower side)/(upper side) (B0)".	—
3	Pulse output selection	0, 90, 180, and 270 degree pulses are selected and output by "Pulse output part pulse output selection 0/1/2 (B0)". In addition, "Pulse output part pulse output mask (B0)" sets masking enable/disable for each channel, and outputs 0b when masking is enabled.	—

■Pulse output part terminal list

No.	Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
1	clk100m	I	—	System clock	cc2_top	—	—
2	usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
3	re_rs_usr_wreg_110_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (B0)	re2_top	0000h	—
4	re_rs_usr_wreg_111_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (B0)	re2_top	0000h	—
5	re_rs_usr_wreg_112_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (B0)	re2_top	0000h	—
6	re_rs_usr_wreg_113_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (B0)	re2_top	0000h	—
7	re_rs_usr_wreg_1b8_clk100m_reg[0]	I	—	Pulse output part pulse output enable (B0)	re2_top	0b	—
8	re_rs_usr_wreg_115_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (B1)	re2_top	0000h	—
9	re_rs_usr_wreg_116_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (B1)	re2_top	0000h	—
10	re_rs_usr_wreg_117_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (B1)	re2_top	0000h	—
11	re_rs_usr_wreg_118_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (B1)	re2_top	0000h	—
12	re_rs_usr_wreg_1b9_clk100m_reg[0]	I	—	Pulse output part pulse output enable (B1)	re2_top	0b	—
13	re_rs_usr_wreg_11a_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (B2)	re2_top	0000h	—
14	re_rs_usr_wreg_11b_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (B2)	re2_top	0000h	—
15	re_rs_usr_wreg_11c_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (B2)	re2_top	0000h	—
16	re_rs_usr_wreg_11d_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (B2)	re2_top	0000h	—
17	re_rs_usr_wreg_1ba_clk100m_reg[0]	I	—	Pulse output part pulse output enable (B2)	re2_top	0b	—
18	re_rs_usr_wreg_11f_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (E0)	re2_top	0000h	—
19	re_rs_usr_wreg_120_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (E0)	re2_top	0000h	—
20	re_rs_usr_wreg_121_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (E0)	re2_top	0000h	—
21	re_rs_usr_wreg_122_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (E0)	re2_top	0000h	—
22	re_rs_usr_wreg_1bb_clk100m_reg[0]	I	—	Pulse output part pulse output enable (E0)	re2_top	0b	—
23	re_rs_usr_wreg_124_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (E1)	re2_top	0000h	—
24	re_rs_usr_wreg_125_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (E1)	re2_top	0000h	—
25	re_rs_usr_wreg_126_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (E1)	re2_top	0000h	—
26	re_rs_usr_wreg_127_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (E1)	re2_top	0000h	—
27	re_rs_usr_wreg_1bc_clk100m_reg[0]	I	—	Pulse output part pulse output enable (E1)	re2_top	0b	—
28	re_rs_usr_wreg_129_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (lower side) (E2)	re2_top	0000h	—
29	re_rs_usr_wreg_12a_clk100m_reg[15:0]	I	—	Pulse output part pulse width upper limit value (upper side) (E2)	re2_top	0000h	—
30	re_rs_usr_wreg_12b_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (lower side) (E2)	re2_top	0000h	—
31	re_rs_usr_wreg_12c_clk100m_reg[15:0]	I	—	Pulse output part output pulse count upper limit value (upper side) (E2)	re2_top	0000h	—
32	re_rs_usr_wreg_1bd_clk100m_reg[0]	I	—	Pulse output part pulse output enable (E2)	re2_top	0b	—

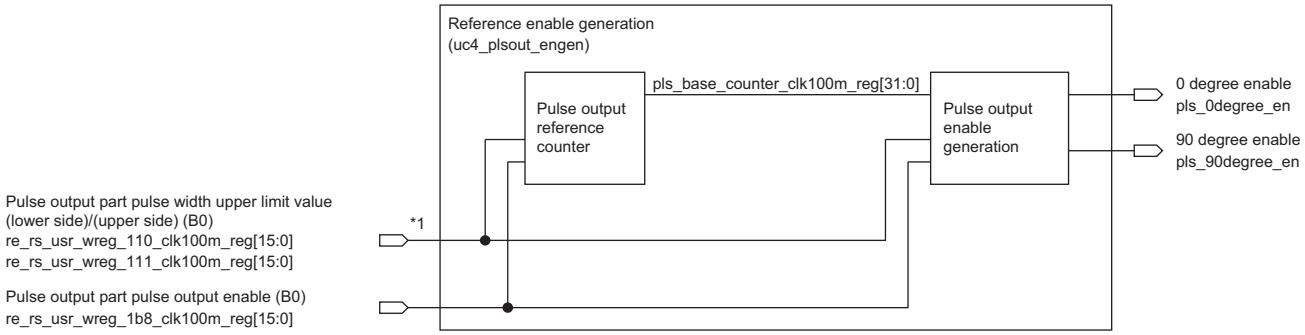
No.	Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
33	re_rs_usr_wreg_130_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (B0)	re2_top	0000h	—
34	re_rs_usr_wreg_131_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (B0)	re2_top	0000h	—
35	re_rs_usr_wreg_132_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (B0)	re2_top	0b	—
36	re_rs_usr_wreg_133_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (B1)	re2_top	0000h	—
37	re_rs_usr_wreg_134_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (B1)	re2_top	0000h	—
38	re_rs_usr_wreg_135_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (B1)	re2_top	0b	—
39	re_rs_usr_wreg_136_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (B2)	re2_top	0000h	—
40	re_rs_usr_wreg_137_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (B2)	re2_top	0000h	—
41	re_rs_usr_wreg_138_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (B2)	re2_top	0b	—
42	re_rs_usr_wreg_139_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (E0)	re2_top	0000h	—
43	re_rs_usr_wreg_13a_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (E0)	re2_top	0000h	—
44	re_rs_usr_wreg_13b_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (E0)	re2_top	0b	—
45	re_rs_usr_wreg_13c_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (E1)	re2_top	0000h	—
46	re_rs_usr_wreg_13d_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (E1)	re2_top	0000h	—
47	re_rs_usr_wreg_13e_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (E1)	re2_top	0b	—
48	re_rs_usr_wreg_13f_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 0 (E2)	re2_top	0000h	—
49	re_rs_usr_wreg_140_clk100m_reg[15:0]	I	—	Pulse output part pulse output selection 1 (E2)	re2_top	0000h	—
50	re_rs_usr_wreg_141_clk100m_reg[1:0]	I	—	Pulse output part pulse output selection 2 (E2)	re2_top	0b	—
51	re_rs_usr_wreg_142_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (B0)	re2_top	0000h	—
52	re_rs_usr_wreg_143_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (B0)	re2_top	0b	—
53	re_rs_usr_wreg_144_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (B1)	re2_top	0000h	—
54	re_rs_usr_wreg_145_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (B1)	re2_top	0b	—
55	re_rs_usr_wreg_146_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (B2)	re2_top	0000h	—
56	re_rs_usr_wreg_147_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (B2)	re2_top	0b	—
57	re_rs_usr_wreg_148_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (E0)	re2_top	0000h	—
58	re_rs_usr_wreg_149_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (E0)	re2_top	0b	—
59	re_rs_usr_wreg_14a_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (E1)	re2_top	0000h	—
60	re_rs_usr_wreg_14b_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (E1)	re2_top	0b	—
61	re_rs_usr_wreg_14c_clk100m_reg[15:0]	I	—	Pulse output part pulse output mask 0 (E2)	re2_top	0000h	—
62	re_rs_usr_wreg_14d_clk100m_reg[0]	I	—	Pulse output part pulse output mask 1 (E2)	re2_top	0b	—
63	pls_iob0_y_clk100m_reg[15:0]	O	—	Pulse output (B0)	Output block part	0000h	—
64	pls_iob0_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (B0)	Output block part	0b	—
65	pls_iob0_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (B0)	Output block part	0000_0000h	—
66	pls_iob1_y_clk100m_reg[15:0]	O	—	Pulse output (B1)	Output block part	0000h	—
67	pls_iob1_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (B1)	Output block part	0b	—

No.	Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
68	pls_iob1_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (B1)	Output block part	0000_0000h	—
69	pls_iob2_y_clk100m_reg[15:0]	O	—	Pulse output (B2)	Output block part	0000h	—
70	pls_iob2_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (B2)	Output block part	0b	—
71	pls_iob2_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (B2)	Output block part	0000_0000h	—
72	pls_ioe0_y_clk100m_reg[15:0]	O	—	Pulse output (E0)	Output block part	0000h	—
73	pls_ioe0_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (E0)	Output block part	0b	—
74	pls_ioe0_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (E0)	Output block part	0000_0000h	—
75	pls_ioe1_y_clk100m_reg[15:0]	O	—	Pulse output (E1)	Output block part	0000h	—
76	pls_ioe1_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (E1)	Output block part	0b	—
77	pls_ioe1_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (E1)	Output block part	0000_0000h	—
78	pls_ioe2_y_clk100m_reg[15:0]	O	—	Pulse output (E2)	Output block part	0000h	—
79	pls_ioe2_y_dio485_clk100m_reg	O	—	Pulse output (digital input/output) (E2)	Output block part	0b	—
80	pls_ioe2_plscnt_clk100m_reg[31:0]	O	—	Number of pulse outputs (E2)	Output block part	0000_0000h	—

Reference enable generation

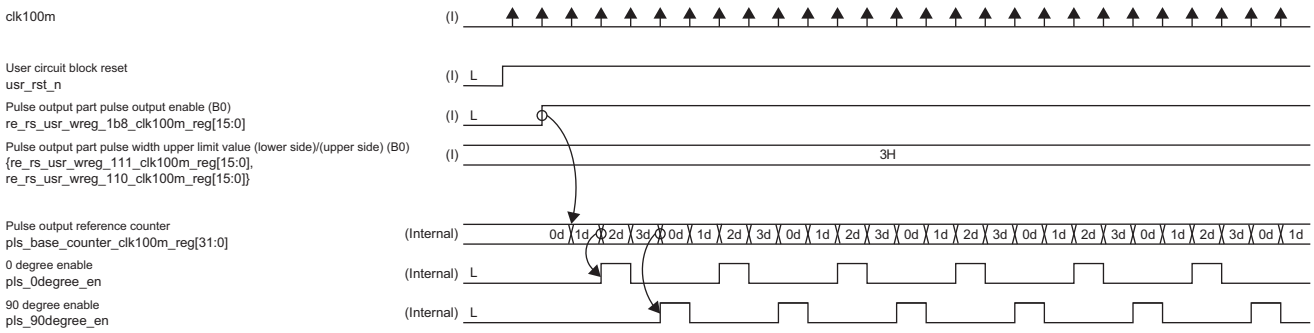
The reference enable generator implements a 32-bit ring counter with the upper limit of "Pulse output part pulse width upper limit value (lower side)/(upper side) (B0)", and outputs the 0-degree enable pulse (pls_0degree_en) for pulse generation and 90-degree enable pulse (pls_90degree_en). 0-degree enable outputs a pulse (1 pulse (clk100m)) when the bit shift (1/2) value of "Pulse output part pulse width upper limit value (lower side)/(upper side) (B0)" and the 32-bit ring counter are equal. 90-degree enable outputs a pulse (1 pulse (clk100m)) when the value of "Pulse output part pulse width upper limit value (lower side)/(upper side)" and the 32-bit ring counter are equal. The block diagram and timing chart of the reference enable generator are shown below.

■Block Diagram



*1 If 0000_0000H to 0000_0003H is input, it will be clipped to 0000_0003H.

■Timing chart



■Pulse output, reference counter

This is a 32-bit ring counter that determines the upper limit value at "Pulse output part pulse width upper limit value (lower side) (B0)" and "Pulse output part pulse width upper limit value (upper side) (B0)".

The truth values of the pulse output reference counter are shown below.

No.	usr_rst_n	*1	*2	Pulse output reference counter
1	0b (enable)	X	X	0000_0000h
2	1b (disable)	0b (disable)	X	0000_0000h
3	1b	1b (enable)	(*2) ≤ pls_base_counter_clk100m_reg	0000_0000h
4	1b	1b	(*2) > pls_base_counter_clk100m_reg	pls_base_counter_clk100m_reg+1

*1 Pulse output part pulse output enable (B0)

*2 Pulse output part pulse width upper limit value (lower side)/(upper side) (B0) (value after clipping)

■Pulse output: Enable generation

0-degree enable (pls_0degree_en) and 90 degree enable (pls_90degree_en) are generated and output from the value of the pulse output reference counter (pls_base_counter_clk100m_reg). The truth values for pulse output enable generation are shown below.

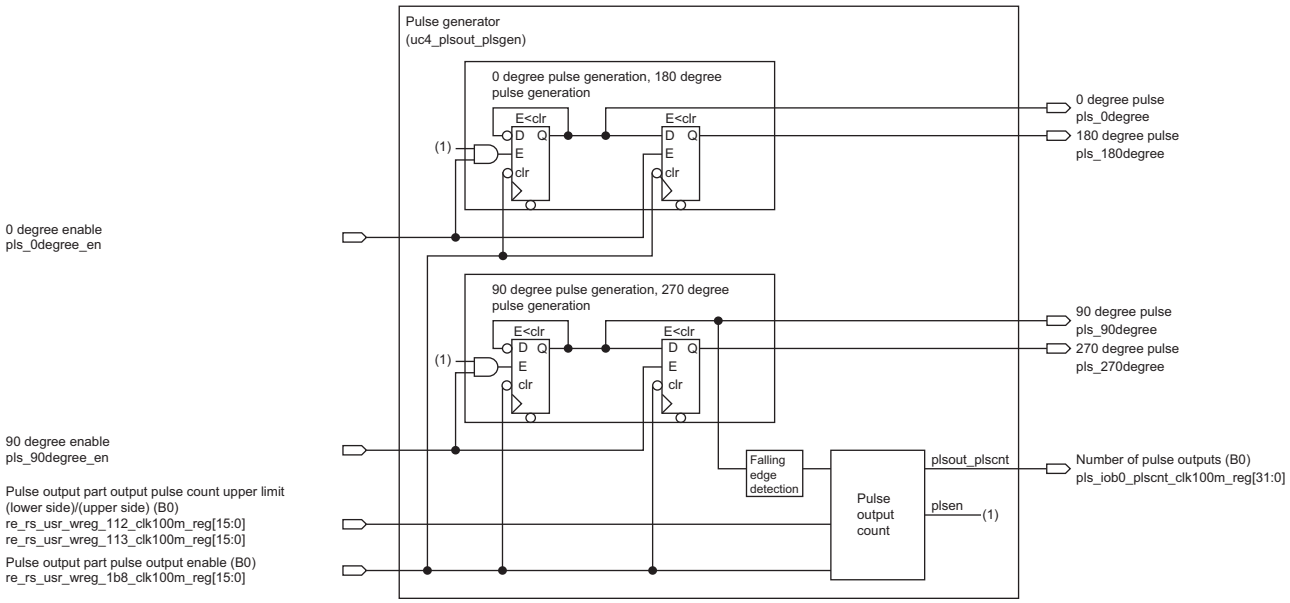
No.	usr_rst_n	*1	*2	0 degree enable (pls_0degree_en)	90 degree enable (pls_90degree_en)
1	0b (enable)	X	X	0b	0b
2	1b (disable)	0b (disable)	X	0b	0b
3	1b	1b (enable)	(*2)=pls_base_counter_clk100m_reg[31:0]	0b	1b
4	1b	1b	((*2) >> 1b)=pls_base_counter_clk100m_reg[31:0]	1b	0b
5	1b	1b	Except for that shown above	0b	0b

*1 Pulse output part pulse output enable (B0)
*2 Pulse output part pulse width upper limit value (lower side)/(upper side) (B0) (value after clipping)

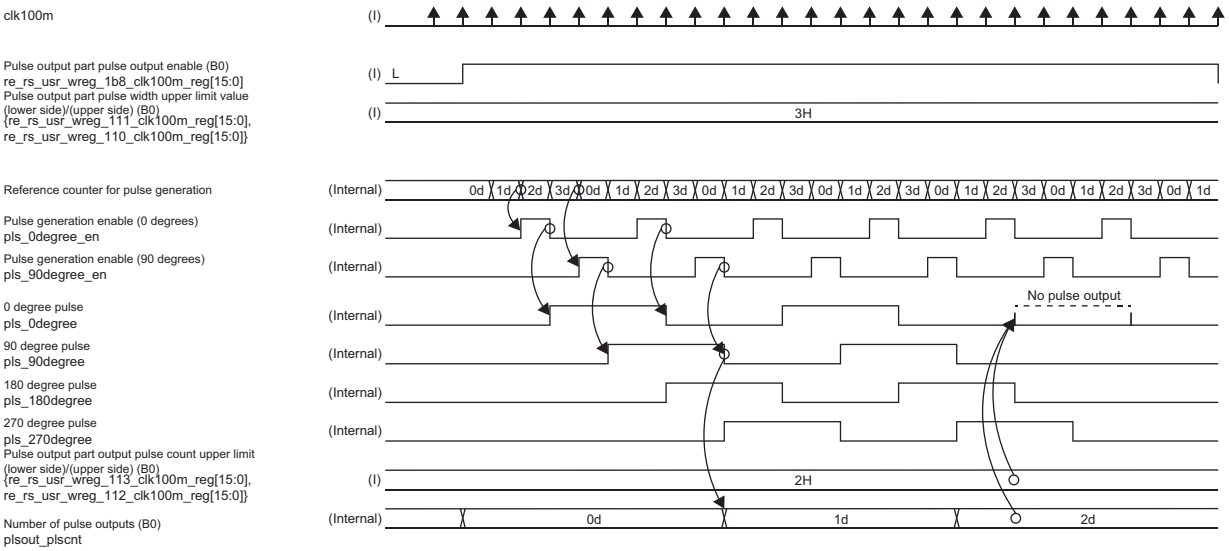
Pulse generator

The pulse generator generates 0, 90, 180, and 270 degree pulses (pls_0degree, pls_90degree, pls_180degree, pls_270degree) based on the 0 degree enable (pls_0degree_en) and 90 degree enable (pls_90degree_en) from the reference enable generator. In addition, the number of output pulses is counted, and when the count value becomes the same as "Pulse output part output pulse count upper limit value (lower side)/(upper side) (B0)", pulse output is stopped.
A block diagram and timing chart of the pulse generator are shown below.

■Pulse output pulse generation block diagram



■Pulse output: Pulse generation timing chart



■0-degree pulse generation, 180-degree pulse generation (same for 90-degree pulse generation and 270-degree pulse generation)

Receives 0-degree enable from reference enable generation, inverts the output signal, and outputs it (0-degree pulse). A 180-degree pulse is output by shifting the 0-degree pulse by one level. If "Pulse output part pulse output enable (B0)" is set to Disable (0), the 0-degree pulse and 180-degree pulse are initialized(0) and output.

The output of the 0-degree pulse is masked by the plsen signal from the pulse output count.

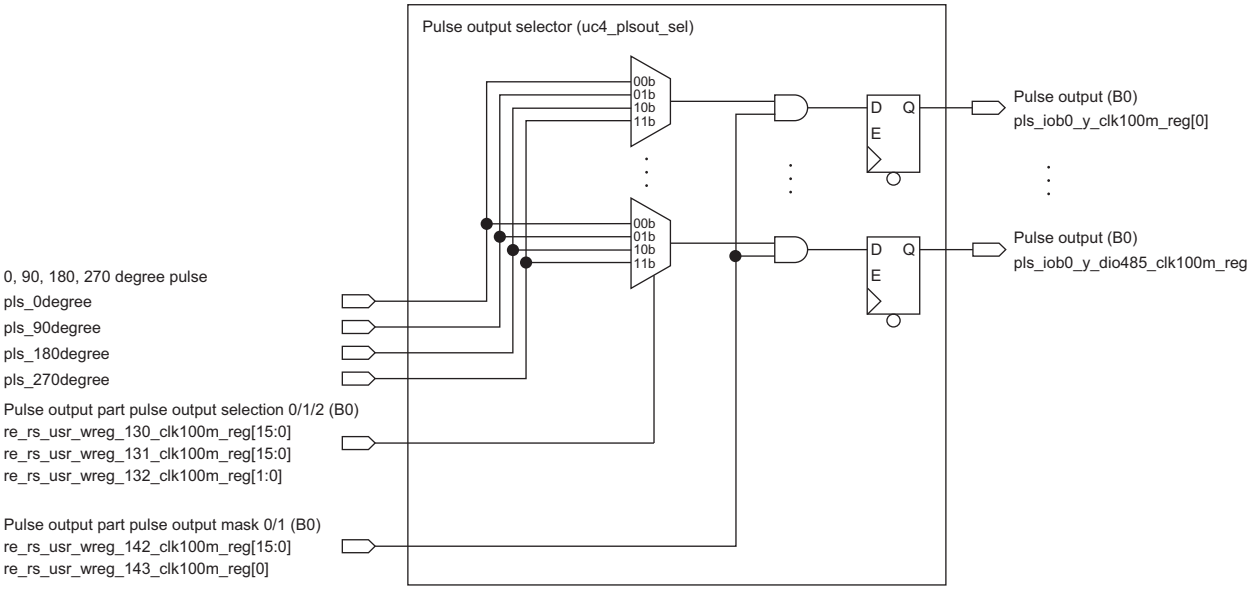
■Pulse output count

It is a 32-bit linear counter that counts according to the falling edge signal of a 90 degree pulse (pls_90degree). The plsen signal is output at 0b when the count value becomes equal to the "Pulse output part output pulse count upper limit value (lower side)/(upper side) (B0)", and then the count-up is not performed.

If "Pulse output part pulse output enable (B0)" is Disable (0), the 32-bit linear counter is initialized (0000_0000H).

Pulse output selection

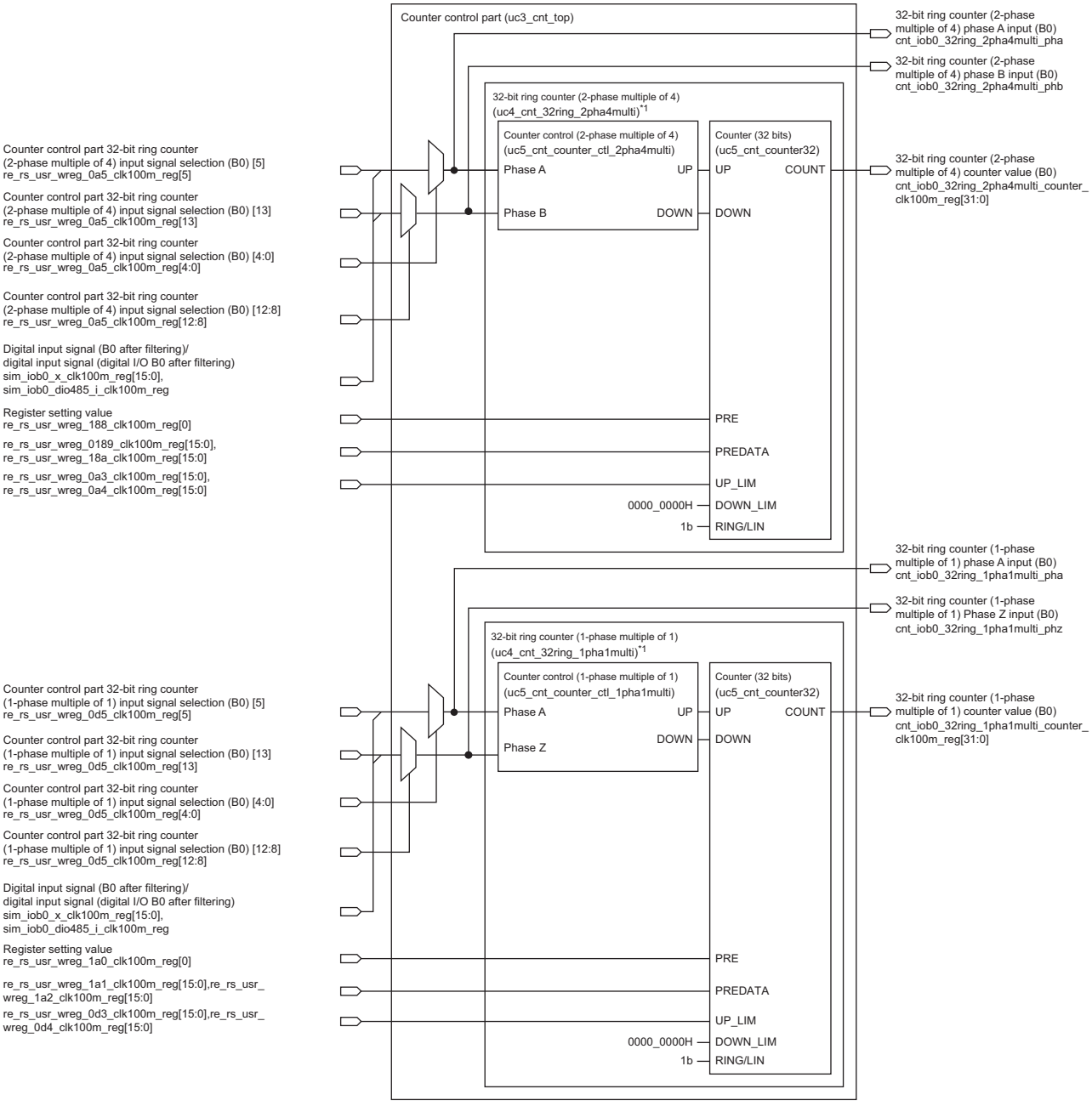
The pulse output selector selects and outputs the pulse (0-degree pulse, 90-degree pulse, 180-degree pulse, 270-degree pulse (pls_0degree, pls_90degree, pls_180degree, pls_270degree)) to be output by each channel of each circuit board. A block diagram of the pulse output selector is shown below.



Counter control part (uc3_cnt_top)

This module implements a counter controlled by digital signals input from the digital input control part. The counter implements a 32-bit ring counter (2-phase multiple of 4) and a 32-bit ring counter (1-phase multiple of 1). The block diagram, function list, and terminal list of the counter control part block are shown below.

■Counter control part block diagram



*1 B1, B2, E0, E1, and E2 also have the same structure.

■Counter control part function list

No.	Function	Overview	Remarks
1	Phase A and Phase B input selection function (2-phase multiple of 4)	From the digital input signal (B0 after filtering)/(digital input/output B0 after filtering) signal (17 bits), "Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0)" is used to select the Phase A and Phase B signals of the 32-bit ring counter (2-phase multiple of 4).	—
2	32-bit ring counter (2-phase multiple of 4) control	A 32-bit ring counter that counts up and down in 2-phase multiple of 4. Control is performed with the preset, Phase A, and Phase B inputs. • Phase A, Phase B input: Counts up/down. • Preset input: Executes preset. If the count value is the same as the counter upper limit value -1 and the count-up condition is met, the value becomes 0000_0000h. Also, if the count value is 0000_0000h and the countdown condition is met, the value becomes counter upper limit value -1. (Priority of input signal is PRE > Phase A = Phase B)	—
3	Phase A, Phase Z input selection function (1-phase multiple of 1)	This is the same as the Phase A, Phase B input selection function (2-phase multiple of 4).	—
4	32-bit ring counter (1-phase multiple of 1) control	A 32-bit ring counter that counts up and down with 1-phase multiple of 1. It changes to the same structure as 32-bit ring counter (2-phase multiple of 4) and count-up of 1-phase multiple of 1.	—

■Counter control part terminal list

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
clk100m	I	—	System clock	cc2_top	—	—
usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
sim_iob0_x_clk100m_reg[15:0]	I	—	Digital input signal (B0 after filtering)	di2_top	0000h	—
sim_iob1_x_clk100m_reg[15:0]	I	—	Digital input signal (B1 after filtering)	di2_top	0000h	—
sim_iob2_x_clk100m_reg[15:0]	I	—	Digital input signal (B2 after filtering)	di2_top	0000h	—
sim_ioe0_x_clk100m_reg[15:0]	I	—	Digital input signal (E0 after filtering)	di2_top	0000h	—
sim_ioe1_x_clk100m_reg[15:0]	I	—	Digital input signal (E1 after filtering)	di2_top	0000h	—
sim_ioe2_x_clk100m_reg[15:0]	I	—	Digital input signal (E2 after filtering)	di2_top	0000h	—
sim_iob0_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B0 after filtering)	dio2_top	0b	—
sim_iob1_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B1 after filtering)	dio2_top	0b	—
sim_iob2_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B2 after filtering)	dio2_top	0b	—
sim_ioe0_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E0 after filtering)	dio2_top	0b	—
sim_ioe1_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E1 after filtering)	dio2_top	0b	—
sim_ioe2_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E2 after filtering)	dio2_top	0b	—
re_rs_usr_wreg_188_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B0)	re2_top	0b	—
re_rs_usr_wreg_189_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_18a_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0a3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0a4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0a5_clk100m_reg [4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) Phase A input selection	re2_top	00h	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
re_rs_usr_wreg_0a5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0a5_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0a5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_18b_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B1)	re2_top	0b	—
re_rs_usr_wreg_18c_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_18c_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0ab_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0ac_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0ad_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0ad_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0ad_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0ad_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_18e_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B2)	re2_top	0b	—
re_rs_usr_wreg_18f_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_190_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0b3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0b4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0b5_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0b5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0b5_clk100m_reg [5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0b5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_191_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E0)	re2_top	0b	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
re_rs_usr_wreg_192_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_193_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0bb_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0bc_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0bc_clk100m_reg [4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0bc_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0bd_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0bd_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_194_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E1)	re2_top	0b	—
re_rs_usr_wreg_195_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_196_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0c3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0c4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0c5_clk100m_reg [4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0c5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0c5_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0c5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_197_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E2)	re2_top	0b	—
re_rs_usr_wreg_198_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_199_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_0cb_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (E2)	re2_top	0000h	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
re_rs_usr_wreg_0cc_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_0cd_clk100m_reg [4:0]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0cd_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) Phase B input selection	re2_top	00h	—
re_rs_usr_wreg_0cd_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0cd_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) Phase B register input	re2_top	0b	—
re_rs_usr_wreg_1a0_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B0)	re2_top	0b	—
re_rs_usr_wreg_1a1_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_1a2_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0d3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0d4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B0)	re2_top	0000h	—
re_rs_usr_wreg_0d5_clk100m_reg [4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0d5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) Phase Z input selection	re2_top	00h	—
re_rs_usr_wreg_0d5_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0d5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) Phase Z register input	re2_top	0b	—
re_rs_usr_wreg_1a3_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B1)	re2_top	0b	—
re_rs_usr_wreg_1a4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_1a5_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0db_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0dc_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B1)	re2_top	0000h	—
re_rs_usr_wreg_0dd_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0dd_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) Phase Z input selection	re2_top	00h	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
re_rs_usr_wreg_0dd_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0dd_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) Phase Z register input	re2_top	0b	—
re_rs_usr_wreg_1a6_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B2)	re2_top	0b	—
re_rs_usr_wreg_1a7_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_1a8_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0e3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0e4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B2)	re2_top	0000h	—
re_rs_usr_wreg_0e5_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0e5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) Phase Z input selection	re2_top	00h	—
re_rs_usr_wreg_0e5_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0e5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) Phase Z register input	re2_top	0b	—
re_rs_usr_wreg_1a9_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E0)	re2_top	0b	—
re_rs_usr_wreg_1aa_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_1ab_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0eb_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0ec_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E0)	re2_top	0000h	—
re_rs_usr_wreg_0ed_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0ed_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) Phase Z input selection	re2_top	00h	—
re_rs_usr_wreg_0ed_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0ed_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) Phase Z register input	re2_top	0b	—
re_rs_usr_wreg_1ac_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E1)	re2_top	0b	—
re_rs_usr_wreg_1ad_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E1)	re2_top	0000h	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
re_rs_usr_wreg_1ae_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0f3_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0f4_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E1)	re2_top	0000h	—
re_rs_usr_wreg_0f5_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0f5_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) Phase Z input selection	re2_top	00h	—
re_rs_usr_wreg_0f5_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0f5_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) Phase Z register input	re2_top	0b	—
re_rs_usr_wreg_1af_clk100m_reg[0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E2)	re2_top	0b	—
re_rs_usr_wreg_1b0_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_1b1_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_0fb_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_0fc_clk100m_reg[15:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E2)	re2_top	0000h	—
re_rs_usr_wreg_0fd_clk100m_reg[4:0]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) Phase A input selection	re2_top	00h	—
re_rs_usr_wreg_0fd_clk100m_reg[12:8]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) Phase Z input selection	re2_top	00h	—
re_rs_usr_wreg_0fd_clk100m_reg[5]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) Phase A register input	re2_top	0b	—
re_rs_usr_wreg_0fd_clk100m_reg[13]	I	—	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) Phase Z register input	re2_top	0b	—
cnt_iob0_32ring_2pha4multi_counter_clk100m_reg[31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (B0)	Output block part	0000_0000h	—
cnt_iob0_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (B0)	Output block part	0000_0000h	—
cnt_iob1_32ring_2pha4multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (B1)	Output block part	0000_0000h	—
cnt_iob1_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (B1)	Output block part	0000_0000h	—
cnt_iob2_32ring_2pha4multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (B2)	Output block part	0000_0000h	—
cnt_iob2_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (B2)	Output block part	0000_0000h	—
cnt_ioe0_32ring_2pha4multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (E0)	Output block part	0000_0000h	—

Signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
cnt_ioe0_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (E0)	Output block part	0000_0000h	—
cnt_ioe1_32ring_2pha4multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (E1)	Output block part	0000_0000h	—
cnt_ioe1_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (E1)	Output block part	0000_0000h	—
cnt_ioe2_32ring_2pha4multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (2-phase multiple of 4) counter value (E2)	Output block part	0000_0000h	—
cnt_ioe2_32ring_1pha1multi_counter_clk100m_reg [31:0]	O	—	32-bit ring counter (1-phase multiple of 1) counter value (E2)	Output block part	0000_0000h	—
cnt_iob0_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B0)	Logging control part	0b	—
cnt_iob0_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B0)	Logging control part	0b	—
cnt_iob1_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B1)	Logging control part	0b	—
cnt_iob1_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B1)	Logging control part	0b	—
cnt_iob2_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B2)	Logging control part	0b	—
cnt_iob2_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B2)	Logging control part	0b	—
cnt_ioe0_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E0)	Logging control part	0b	—
cnt_ioe0_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E0)	Logging control part	0b	—
cnt_ioe1_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E1)	Logging control part	0b	—
cnt_ioe1_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E1)	Logging control part	0b	—
cnt_ioe2_32ring_2pha4multi_pha	O	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E2)	Logging control part	0b	—
cnt_ioe2_32ring_2pha4multi_phb	O	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E2)	Logging control part	0b	—

■Counter control (32-bit ring counter (2-phase multiple of 4))

It detects the rising edge and falling edge of Phase A and Phase B, and outputs the counter UP and DOWN signals in one pulse (clk100m). The truth table of the UP output and DOWN output is shown below.

usr_rst_n	clk100m	Phase A	Phase B	UP	DOWN
0b (enable)	X	X	X	0b (disable)	0b (disable)
1b (disable)	↑	↑	0b	1b (enable)	0b
1b	↑	↑	1b	0b	1b (enable)
1b	↑	↓	0b	0b	1b
1b	↑	↓	1b	1b	0b
1b	↑	0b	↑	0b	1b
1b	↑	1b	↑	1b	0b
1b	↑	0b	↓	1b	0b
1b	↑	1b	↓	0b	1b
Except for that shown above				0b	0b

■Counter (32 bits)

The truth table of the 32-bit counter is shown below. Ring/Linear is input as a ring-fixed value, and the counter lower limit value is input as a 0000_0000h fixed value.

usr_rst_n	clk100m	PRE	RING/LIN	UP	DOWN	UP_LIM[31:0]	DOWN_LIM[31:0]	COUNT[31:0]
0b (enable)	X	X	X	X	X	X	X	0000_0000h
1b (disable)	↑	1b (enable)	X	X	X	X	X	PRE_DATA
1b	↑	0b (disable)	1b(RING)	0b (disable)	0b (disable)	X	X	Hold
1b	↑	0b	1b	1b (enable)	0b	COUNT=UP_LIM-1	X	DONW_LIM
1b	↑	0b	1b	1b	0b	Except for that shown above	X	COUNT+1
1b	↑	0b	1b	0b	1b (enable)	X	COUNT=DOWN_LIM	UP_LIM-1
1b	↑	0b	1b	0b	1b	X	Except for that shown above	COUNT-1
1b	↑	0b	1b	1b	1b	X	X	Hold
1b	↑	0b	0b(LIN)	0b	0b	X	X	Hold
1b	↑	0b	0b	1b	0b	COUNT=UP_LIM	X	Hold
1b	↑	0b	0b	1b	0b	Except for that shown above	X	COUNT+1
1b	↑	0b	0b	0b	1b	X	COUNT=DOWN_LIM	Hold
1b	↑	0b	0b	0b	1b	X	Except for that shown above	COUNT-1
1b	↑	0b	0b	1b	1b	X	X	Hold

Point

The 32-bit counter is used in common for the 32-bit ring counter (2-phase multiple of 4) and the 32-bit ring counter (1-phase multiple of 1).

■Counter control (32-bit ring counter (1-phase multiple of 1))

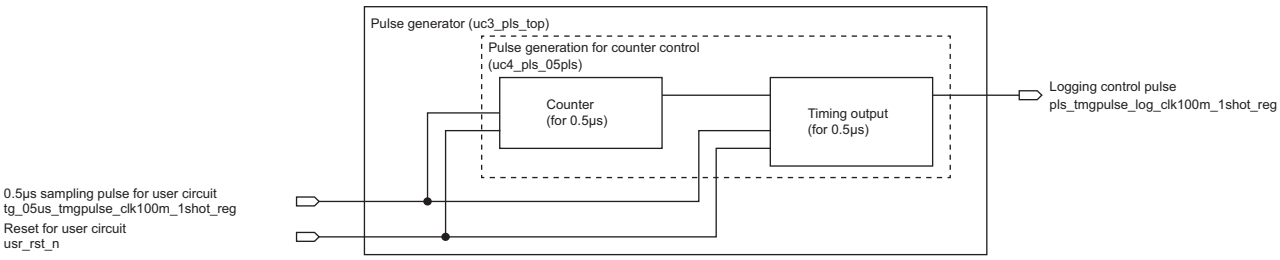
It detects the rising edge of Phase A and Phase Z, and outputs the UP signal and DOWN signal in one pulse. The truth table of the UP/DOWN output is shown below.

usr_rst_n	clk100m	Phase A	Phase Z	UP	DOWN
0b (enable)	X	X	X	0b	0b
1b (disable)	↑	↑	X	1b	0b
1b	↑	X	↑	0b	1b
1b	↑	↑	↑	1b	1b

Pulse generator (uc3_pls_top)

This module generates the sampling pulse for use in the logging control part, from the 0.5µs sampling pulse for user circuit which is input from the timing generator. The block diagram, function list, and terminal list of the pulse generator are shown below.

■Pulse generator block diagram



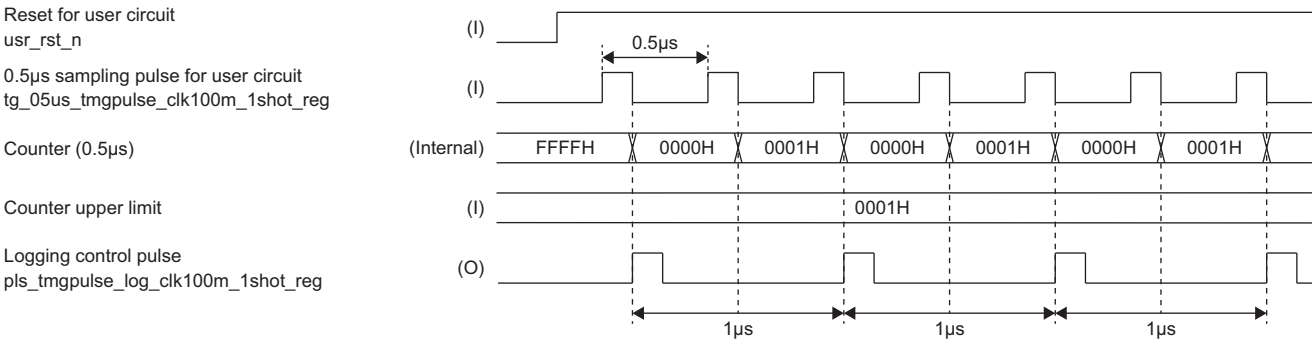
■Pulse generator function list

No.	Function	Overview	Remarks
1	0.5µs counter	A 16-bit ring counter that counts at the 0.5µs pulse input from timing generation. When "Internal operation start/stop" from the register control part starts, counting starts (1). When "Internal operation start/stop" stops (0), the counter is initialized (0000h). The upper limit value is 0001h and it counts from 0000h to 0001h.	—
2	0.5µs data update timing output	Generates a sampling pulse (1 pulse (clk100m)) in 1µs unit from the 0.5µs counter value and 0.5µs pulse.	—

■Pulse generator terminal list

No.	Module signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
1	clk100m	I	—	System clock	cc2_top	—	—
2	usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
3	tg_05us_tmgpulse_clk100m_1shot_reg	I	H	0.5µs sampling pulse for user circuit	tg2_top	0b	1shot@clk100m
4	pls_tmgpulse_log_clk100m_1shot_reg	O	H	Pulse for logging control	Logging control part	1b	1shot@clk100m

■Pulse generator timing chart



■Counter (0.5μs)

Implements a 16-bit ring counter that counts up with the 0.5μs sampling pulse (tg_05us_tmgpulse_clk100m_1shot_reg) for user circuit. The upper limit of the counter is fixed at 0001H and count up is done at every 0.5μs. The truth value of the counter (0.5μs) is shown below.

No.	usr_rst_n	clk100m	tg_05us_tmgpulse_clk100m_1shot_reg	Counter (0.5us) (count_05us)	Counter (0.5us) (count_05us)
1	0b (enable)	X	X	X	0000h
2	1b (disable)	↑	0b (disable)	X	Hold
3	1b	↑	1b (enable)	0001H ≤ count_05us	0000h
4	1b	↑	1b	0001H > count_05us	count_05us+1

■Timing output (for 0.5μs)

Generates the logging control pulse (pls_tmgpulse_log_clk100m_1shot_reg) used inside the user circuit according to the 0.5μs sampling pulse (tg_05us_tmgpulse_clk100m_1shot_reg) for user circuit and the count value (count_05μs) of the counter (0.5μs).

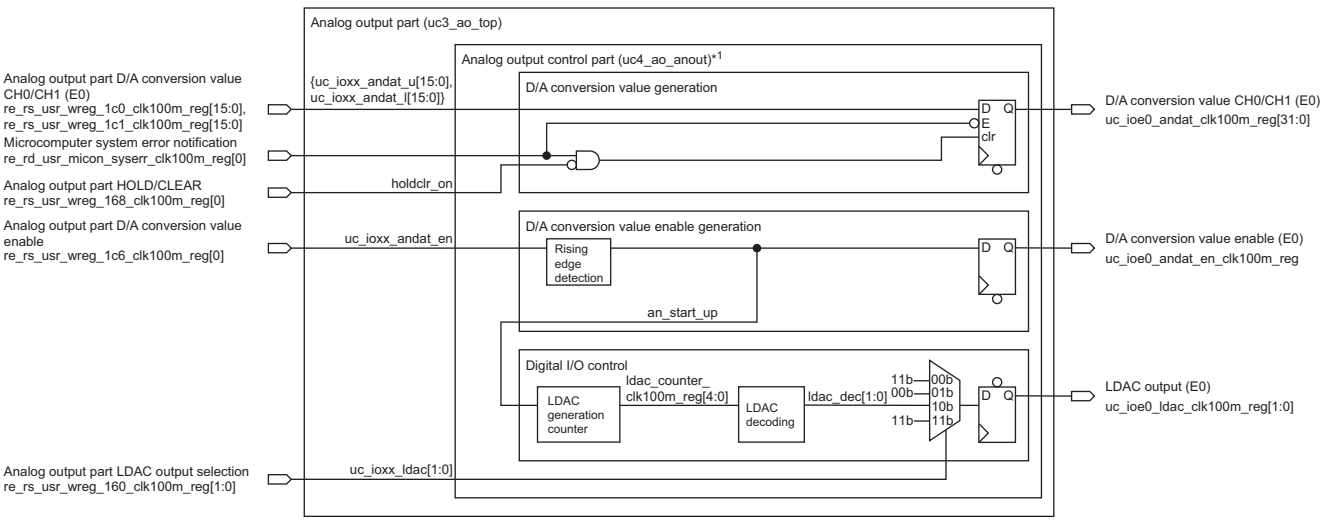
The truth table for pulse generation is shown below.

No.	usr_rst_n	clk100m	tg_05us_tmgpulse_clk100m_1shot_reg	Counter (0.5us) (count_05us)	Pulse for logging control (pls_tmgpulse_log_ clk100m_1shot_reg)
1	0b (enable)	X	X	X	0b
2	1b (disable)	↑	0b (disable)	X	0b
3	1b	↑	1b (enable)	0001h = count_05us	1b
4	1b	↑	1b	Except for that shown above	0b

Analog output block (uc3_ao_top)

This module outputs the D/A conversion value to the analog output control part of the standard circuit according to the register setting value and the register setting timing. The block diagram, function list, and terminal list of the analog output control part are shown below.

■Analog output control part block diagram



*1 E1 and E2 have the same structure.

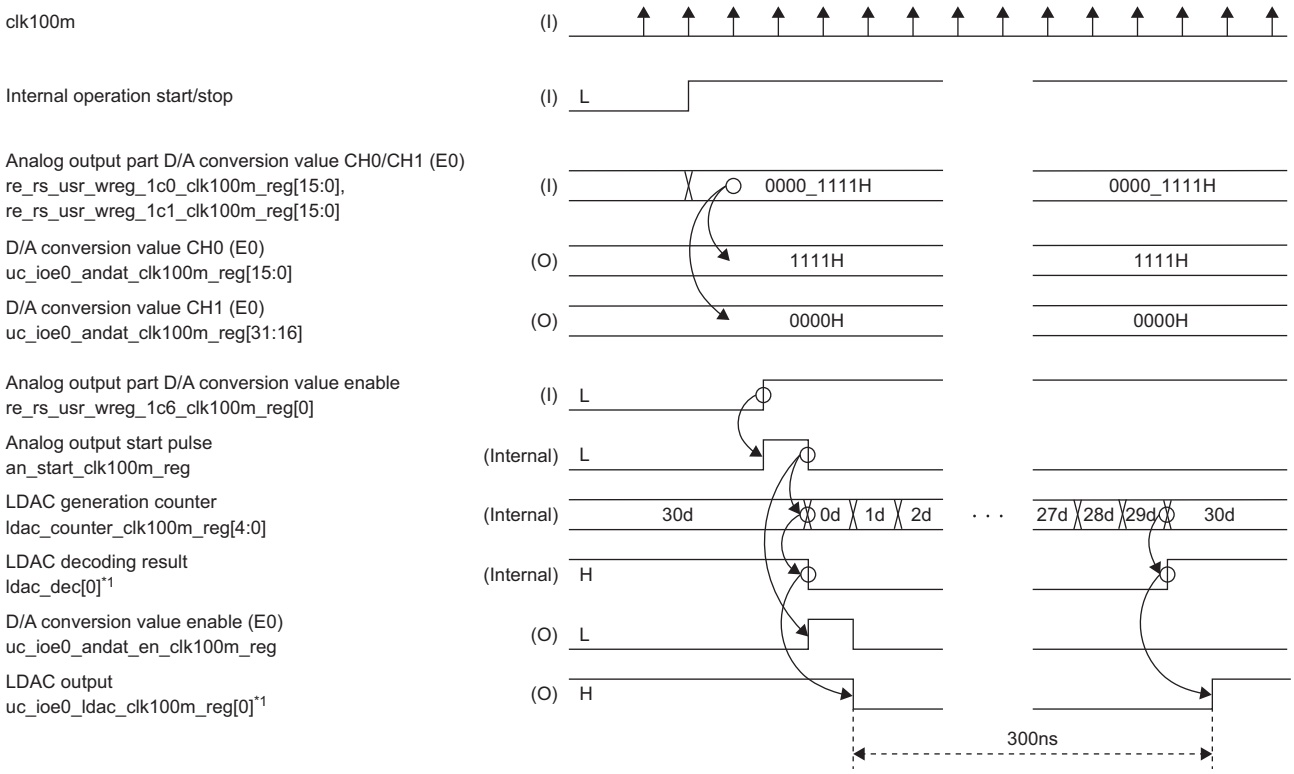
■Analog output control part function list

No.	Function	Overview	Remarks
1	D/A conversion value generation	D/A conversion value CH0/CH1 (E0) is generated by MCU system error notification and Analog output part HOLD/CLEAR. The output combinations of D/A conversion values CH0/CH1 (E0) are shown below. • MCU system error notification = 0b (no error), Analog output part HOLD/CLEAR = 0b (CLEAR), and Analog control D/A conversion value CH0/CH1 (E0) is output. • MCU system error notification = 1b (error present), Analog output part HOLD/CLEAR = 0b (CLEAR), and 0000_0000h is output. • MCU system error notification = 0b (no error), Analog output part HOLD/CLEAR = 1b (HOLD), and Analog control D/A conversion value CH0/CH1 (E0) is output. • MCU system error notification = 1b (error found), Analog output part HOLD /CLEAR = 1b (HOLD), and the previous value is held.	—
2	D/A conversion value enable	Analog control: Detects the rising edge of D/A conversion value enable (E0) and outputs D/A conversion value enable (E0). At the same timing, D/A conversion value enable (E0) is notified to the digital input/output control.	—
3	Digital input/ output control	Generates the following LDAC output (E0). The output combinations are shown below. • Analog output part LDAC output selection = 0h, 3h Outputs 11b • Analog output part LDAC output selection = 1h Outputs 00b • Analog output part LDAC output selection = 2h Outputs the LDAC signal for inter-channel synchronization. ■LDAC signal for inter-channel synchronization Receives D/A conversion value enable (E0) and outputs a 300ns pulse (0b enable pulse). A 300ns pulse is output from the second pulse of D/A conversion value enable (E0) after reset release.	—

■Analog output part terminal list

No.	Module signal name	I/O	Logic	Function	Connection destination	Initial value	Pulse signal
1	clk100m	I	—	System clock	cc2_top	—	—
2	usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
3	re_rs_usr_wreg_1c0_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH0 (E0)	re2_top	0000h	—
4	re_rs_usr_wreg_1c1_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH1 (E0)	re2_top	0000h	—
5	re_rs_usr_wreg_1c2_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH0 (E1)	re2_top	0000h	—
6	re_rs_usr_wreg_1c3_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH1 (E1)	re2_top	0000h	—
7	re_rs_usr_wreg_1c4_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH0 (E2)	re2_top	0000h	—
8	re_rs_usr_wreg_1c5_clk100m_reg[15:0]	I	—	Analog output part D/A conversion value CH1 (E2)	re2_top	0000h	—
9	re_rs_usr_wreg_1c6_clk100m_reg[2:0]	I	—	Analog output part D/A conversion value enable	re2_top	0h	—
10	re_rs_usr_wreg_160_clk100m_reg[5:0]	I	—	Analog output part LDAC output selection	re2_top	00h	—
11	re_rs_usr_wreg_168_clk100m_reg[0]	I	—	Analog output part HOLD/CLEAR	re2_top	0b	—
12	re_rs_usr_micon_syserr_clk100m_reg	I	—	MCU system error notification	re2_top	0b	—
13	uc_ioe0_andat_clk100m_reg[31:0]	O	—	D/A conversion value CH0/CH1 (E0)	ao2_top	0000_0000h	—
14	uc_ioe0_andat_en_clk100m_reg	O	H	D/A conversion value enable (E0)	ao2_top	0b	1shot@clk100m
15	uc_ioe0_ldac_clk100m_reg[1:0]	O	—	LDAC output (E0)	ao2_top	3h	—
16	uc_ioe1_andat_clk100m_reg[31:0]	O	—	D/A conversion value (E1)	ao2_top	0000_0000h	—
17	uc_ioe1_andat_en_clk100m_reg	O	H	D/A conversion value enable (E1)	ao2_top	0b	1shot@clk100m
18	uc_ioe1_ldac_clk100m_reg[1:0]	O	—	LDAC output (E1)	ao2_top	3h	—
19	uc_ioe2_andat_clk100m_reg[31:0]	O	—	D/A conversion value (E2)	ao2_top	0000_0000h	—
20	uc_ioe2_andat_en_clk100m_reg	O	H	D/A conversion value enable (E2)	ao2_top	0b	1shot@clk100m
21	uc_ioe2_ldac_clk100m_reg[1:0]	O	—	LDAC output (E2)	ao2_top	3h	—

■Analog output part schematic timing chart



*1 *1 [1] outputs the same signal as [0].

■D/A conversion value generation

In D/A conversion value generation, D/A conversion value is generated by "Analog output part HOLD/CLEAR", "Microcomputer system error notification", and "Analog output part D/A conversion value CH0/CH1 (E0)". The truth table for D/A conversion value generation is shown below.

No.	usr_rst_n	clk100m	MCU system error notification	Analog output part HOLD/ CLEAR	uc_ioe0_andat_clk100m_reg
1	0b (enable)	X	X	X	0000_0000h
2	1b (disable)	↑	0b (disable)	0b(CLEAR)	{re_rs_usr_wreg_1c1_clk100m_reg, re_rs_usr_wreg_1c0_clk100m_reg,}
3	1b	↑	0b	1b(HOLD)	{re_rs_usr_wreg_1c1_clk100m_reg, re_rs_usr_wreg_1c0_clk100m_reg,}
4	1b	↑	1b (enable)	0b	0000_0000h
5	1b	↑	1b	1b	Previous value held

■D/A conversion value enable generation

D/A conversion value enable (E0) (uc_ioe0_andat_en_clk100m_1shot_reg) detects the rising edge (an_start_up) of "Analog output part D/A conversion value enable" and outputs it in one level of flip-flop.

■Digital input/output control

Implements an LDAC generation counter (ldac_counter_clk100m_reg[4:0]) with an upper limit value of 30d, and decodes this counter to output a 300ns enable pulse (L enable pulse) as an LDAC signal. The LDAC generation counter and the decoding conditions for the LDAC output signal are shown below.

• Digital input/output control counter truth table

No.	usr_rst_n	clk100m	an_start_up	ldac_counter_clk100m_reg[4:0]	LDAC generation counter (ldac_counter_clk100m_reg[4:0])
1	0b (enable)	X	X	X	1Eh
2	1b (disable)	↑	1b (enable)	X	00h
3	1b	↑	0b (disable)	ldac_counter_clk100m_reg < 1Eh	ldac_counter_clk100m_reg+1
4	1b	↑	0b	ldac_counter_clk100m_reg ≥ 1Eh	1Eh

• LDAC output signal decoding condition

No.	usr_rst_n	clk100m	re_rs_usr_wreg_160_clk100m_reg[1:0]	ldac_counter_clk100m_reg[4:0]	LDAC output signal (uc_ioe0_ldac_clk100m_reg[1:0])
1	0b (enable)	X	X	X	11b
2	1b (disable)	↑	00b or 11b	X	11b
3	1b	↑	01b	X	00b
4	1b	↑	10b	ldac_counter_clk100m_reg < 1Eh	00b
5	1b	↑	10b	ldac_counter_clk100m_reg ≥ 1Eh	11b

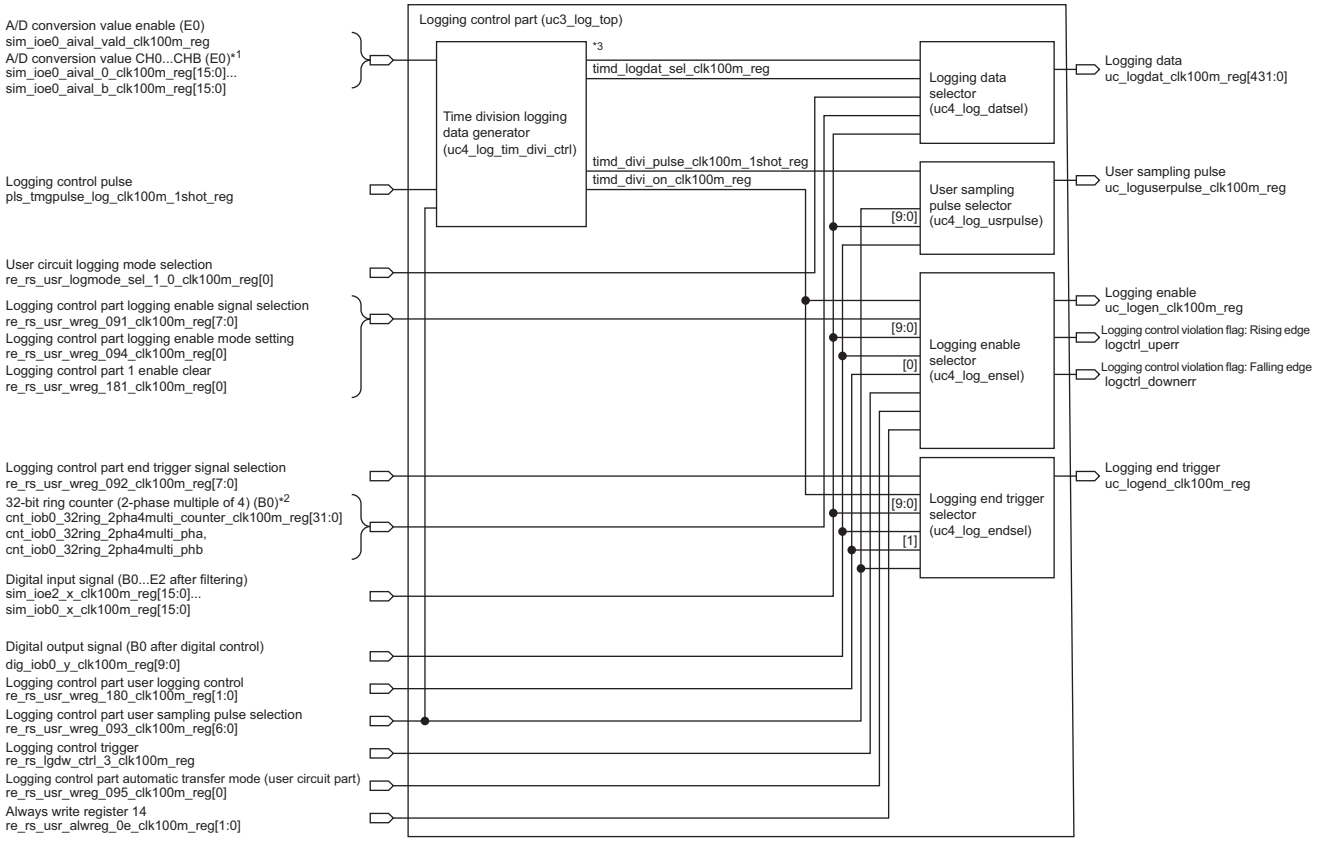
Point

If "Microcomputer system error notification" occurs, output D/A conversion value enable (E0 to E2) and the LDAC output signal (E0 to E2) at least once. Since IOB_RSTL is not output externally, the DAC value needs to be pseudo overwritten.

Logging control part (uc3_log_top)

This module provides the logging control part with logging data (logging target data), logging enable (logging start signal), logging end trigger (logging end pulse during trigger operation mode), and user sampling pulse (logging data sampling). The block diagram, function list, and terminal list of the logging control part are shown below.

■Block Diagram



*1 E1 and E2 are connected in the same way.

*2 B1, B2, E0, E1, and E2 are connected in the same way.

*3 The following signals are connected.

·A/D conversion value (E0): timd_ioe0_aival_0_clk100m_reg[15:0] to timd_ioe0_aival_b_clk100m_reg[15:0]

·A/D conversion value (E1): timd_ioe1_aival_0_clk100m_reg[15:0] to timd_ioe1_aival_b_clk100m_reg[15:0]

·A/D conversion value (E2): timd_ioe2_aival_0_clk100m_reg[15:0] to timd_ioe2_aival_b_clk100m_reg[15:0]

■Logging control part function list

Function		Description
Time division logging data generation	Enable selection	It operates when "A/D conversion value enable (E0, E1, E2)" is selected from the "Logging control part user sampling pulse signal selection" setting. It receives the selected "A/D conversion value enable (E0, E1, E2)" and resets when the next logging control pulse is received. After reset, it outputs an enable signal to the level immediately below.
	Data latch	The A/D conversion value is latched by the signal output from enable selection.
	User sampling pulse output	Outputs the logging control pulse twice after receiving the pulse from the enable selection. It generates a time division logging ON signal. When the user circuit logging mode selection [0]" is enabled (1) and the upper/lower logging data is being logged, the time division logging ON signal becomes enabled (1).
Logging data selector		The user circuit has the following two modes. Use "User circuit logging mode selection" to select a mode. • Time division mode Receives the sampling pulses that have been input, and outputs the logging data. The first sampling pulse outputs [431:0] for logging. The second sampling pulse outputs [943:512] for logging. • Non-time division mode Continues to output [431:0] regardless of timing.

Function		Description
Logging enable selector	Logging enable selection	Selects logging enable (logging start) in the logging control part and then outputs it. 1 bit is selected and output from "Logging control part logging enable signal selection".
	Enable output processing	■(1) The logging enable's output mode is determined by "Logging control part logging enable mode setting". The output modes are shown below. 0: Multiple-enable mode 1: One-enable mode In the multiple-enable mode, the signal selected by logging enable selection is output through. In the one-enable mode, the signal selected by logging enable selection is output only the first time. To output the next logging enable, set "Logging control part 1 enable clear" to Enable (1). While the setting is enabled, the signal selected by logging enable selection is output through. ■(2) When the automatic transfer mode (user circuit) is set to Enable (1) Logging enable is controlled by the logging control trigger and output to the level immediately below. The output conditions for logging enable are as follows. • Logging enable output condition Set condition: Logging control trigger = 1 (logging start rising edge enabled) & logging enable rising edge detected Reset condition: Logging control trigger = 0 (Falling for logging start allowed) & logging enable falling edge detected If any other conditions are met: Outputs the logging control violation flag. The logging control violation flag output conditions are as follows. • Logging control violation flag rising edge output condition Set condition: Logging control trigger = 0 (Falling for logging start allowed) & logging enable rising edge detected Reset condition: Logging control violation flag rising edge clear = 1 • Logging control violation flag falling edge output condition Set condition: Logging control trigger = 1 (logging start rising edge enabled) & logging enable falling edge detected Reset condition: Logging control violation flag falling edge clear = 1 ■(3) When time division mode is enabled When "User circuit logging mode selection [0]" is set to Enable (1), logging enable for time division mode is generated. The generation conditions for logging enable for time division mode are as follows. • Logging enable in time division mode Set condition: Time division logging ON signal = 0 & signal selected by (1)(2) = 1 Reset condition: Time division logging ON signal = 0 & signal selected by (1)(2) = 0
Logging end trigger selector		■(1) Logging end trigger selection Selects the logging end trigger to be output to the logging control part. 1 bit is selected and output from "Logging control part end trigger signal selection". ■(2) When time division mode is enabled The operation when the time division mode is enabled is shown below. When "User circuit logging mode selection [0]" is set to Enable (1), a logging end trigger for time division mode is generated. The conditions for generating a logging end trigger in time division mode are as follows. • Logging end trigger in time division mode Set condition: Time division logging ON signal = 0 & signal selected by (1) = 1 Reset condition: Time division logging ON signal = 0 & signal selected by (1) = 0
User sampling pulse selector		Selects the user sampling pulse to be output to the logging control part. Selects and outputs 1 bit from "Logging control part sampling pulse signal selection".

■Logging control part terminal list

Module signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
clk100m	I	—	System clock	cc2_top	—	—
usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
sim_ioe0_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E0)	ai2_top	0b	1shot@clk100m
sim_ioe0_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E0)	ai2_top	0000H	—
sim_ioe0_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E0)	ai2_top	0000H	—
sim_ioe0_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E0)	ai2_top	0000H	—
sim_ioe0_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E0)	ai2_top	0000H	—
sim_ioe0_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E0)	ai2_top	0000H	—
sim_ioe0_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E0)	ai2_top	0000H	—
sim_ioe0_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E0)	ai2_top	0000H	—
sim_ioe0_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E0)	ai2_top	0000H	—
sim_ioe0_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E0)	ai2_top	0000H	—
sim_ioe0_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E0)	ai2_top	0000H	—
sim_ioe0_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E0)	ai2_top	0000H	—
sim_ioe0_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E0)	ai2_top	0000H	—
sim_ioe1_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E1)	ai2_top	0b	1shot@clk100m
sim_ioe1_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E1)	ai2_top	0000H	—
sim_ioe1_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E1)	ai2_top	0000H	—
sim_ioe1_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E1)	ai2_top	0000H	—
sim_ioe1_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E1)	ai2_top	0000H	—
sim_ioe1_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E1)	ai2_top	0000H	—
sim_ioe1_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E1)	ai2_top	0000H	—
sim_ioe1_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E1)	ai2_top	0000H	—
sim_ioe1_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E1)	ai2_top	0000H	—
sim_ioe1_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E1)	ai2_top	0000H	—
sim_ioe1_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E1)	ai2_top	0000H	—
sim_ioe1_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E1)	ai2_top	0000H	—
sim_ioe1_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E1)	ai2_top	0000H	—
sim_ioe2_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E2)	ai2_top	0b	1shot@clk100m
sim_ioe2_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E2)	ai2_top	0000H	—
sim_ioe2_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E2)	ai2_top	0000H	—
sim_ioe2_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E2)	ai2_top	0000H	—
sim_ioe2_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E2)	ai2_top	0000H	—
sim_ioe2_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E2)	ai2_top	0000H	—
sim_ioe2_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E2)	ai2_top	0000H	—
sim_ioe2_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E2)	ai2_top	0000H	—
sim_ioe2_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E2)	ai2_top	0000H	—
sim_ioe2_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E2)	ai2_top	0000H	—
sim_ioe2_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E2)	ai2_top	0000H	—
sim_ioe2_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E2)	ai2_top	0000H	—
sim_ioe2_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E2)	ai2_top	0000H	—
pls_tmgpulse_log_clk100m_1shot_reg	I	H	Pulse for logging control	Pulse generator	0b	1shot@clk100m
cnt_iob0_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B0)	Counter control part	0000_0000H	—
cnt_iob0_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B0)	Counter control part	0b	—
cnt_iob0_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B0)	Counter control part	0b	—
cnt_iob1_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B1)	Counter control part	0000_0000H	—

Module signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
cnt_iob1_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B1)	Counter control part	0b	—
cnt_iob1_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B1)	Counter control part	0b	—
cnt_iob2_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B2)	Counter control part	0000_0000H	—
cnt_iob2_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (B2)	Counter control part	0b	—
cnt_iob2_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (B2)	Counter control part	0b	—
cnt_ioe0_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E0)	Counter control part	0000_0000H	—
cnt_ioe0_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E0)	Counter control part	0b	—
cnt_ioe0_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E0)	Counter control part	0b	—
cnt_ioe1_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E1)	Counter control part	0000_0000H	—
cnt_ioe1_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E1)	Counter control part	0b	—
cnt_ioe1_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E1)	Counter control part	0b	—
cnt_ioe2_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E2)	Counter control part	0000_0000H	—
cnt_ioe2_32ring_2pha4multi_pha	I	H	32-bit ring counter (2-phase multiple of 4) Phase A input (E2)	Counter control part	0b	—
cnt_ioe2_32ring_2pha4multi_phb	I	H	32-bit ring counter (2-phase multiple of 4) Phase B input (E2)	Counter control part	0b	—
sim_iob0_x_clk100m_reg[15:0]	I	—	Digital input signal (B0 after filtering)	di2_top	0000H	—
sim_iob1_x_clk100m_reg[15:0]	I	—	Digital input signal (B1 after filtering)	di2_top	0000H	—
sim_iob2_x_clk100m_reg[15:0]	I	—	Digital input signal (B2 after filtering)	di2_top	0000H	—
sim_ioe0_x_clk100m_reg[15:0]	I	—	Digital input signal (E0 after filtering)	di2_top	0000H	—
sim_ioe1_x_clk100m_reg[15:0]	I	—	Digital input signal (E1 after filtering)	di2_top	0000H	—
sim_ioe2_x_clk100m_reg[15:0]	I	—	Digital input signal (E2 after filtering)	di2_top	0000H	—
dig_iob0_y_clk100m_reg[9:0]	I	—	Digital output signal (B0 after digital control)	Digital control part	000H	—
re_rs_usr_wreg_180_clk100m_reg[1:0]	I	—	Logging control part user logging control	re2_top	0H	—
re_rs_usr_wreg_091_clk100m_reg[7:0]	I	—	Logging control part logging enable signal selection	re2_top	00H	—
re_rs_usr_wreg_092_clk100m_reg[7:0]	I	—	Logging control part end trigger signal selection	re2_top	00H	—
re_rs_usr_wreg_093_clk100m_reg[6:0]	I	—	Logging control part sampling pulse signal selection	re2_top	00H	—
re_rs_usr_wreg_094_clk100m_reg[0]	I	—	Logging control part logging enable mode setting	re2_top	0b	—
re_rs_usr_wreg_181_clk100m_reg[0]	I	H	Logging control part 1 enable clear	re2_top	0b	—
re_rs_usr_logmode_sel_1_0_clk100m_reg[0]	I	H	User circuit logging mode selection	re2_top	0b	—
uc_logdat_clk100m_reg[431:0]	O	—	Logging data	lf2_top	432(0)	—
uc_logen_clk100m_reg	O	—	Logging enable	lf2_top	0b	—
uc_logend_clk100m_reg	O	—	Logging end trigger	lf2_top	0b	1shot@clk100m
uc_loguserpulse_clk100m_reg	O	—	User sampling pulse	lf2_top	0b	1shot@clk100m
re_rs_usr_alwreg_0e_clk100m_reg[1:0]	I	—	Always write register 14 (logging control violation flag falling edge/ rising edge)	re2_top	0H	—
re_rs_usr_wreg_095_clk100m_reg[0]	I	H	Logging control part automatic transfer mode (user circuit part)	re2_top	0b	—
re_rs_lgdw_ctrl_3_clk100m_reg	I	H	Logging control trigger	re2_top	0b	—

Module signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
logctrl_uperr	O	H	Logging control violation flag rising edge	Output block part	0b	—
logctrl_downerr	O	H	Logging control violation flag falling edge	Output block part	0b	—

Time division logging data generator

The time division logging data generator performs the following operations.

- Loads A/D conversion value (E0), A/D conversion value (E1), A/D conversion value (E2)

Loads the following signals into the time division logging data generator.

A/D conversion value (E0): sim_ioe0_aival_0_clk100m_reg to sim_ioe0_aival_b_clk100m_reg

A/D conversion value (E1): sim_ioe1_aival_0_clk100m_reg to sim_ioe1_aival_b_clk100m_reg

A/D conversion value (E2): sim_ioe2_aival_0_clk100m_reg to sim_ioe2_aival_b_clk100m_reg

- Generates logging data by A/D conversion value enable (E0), A/D conversion value enable (E1), A/D conversion value enable (E2), and logging control pulse (pls_tmgpulse_log_clk100m_1shot_reg)

Loads logging data by using the following signals.

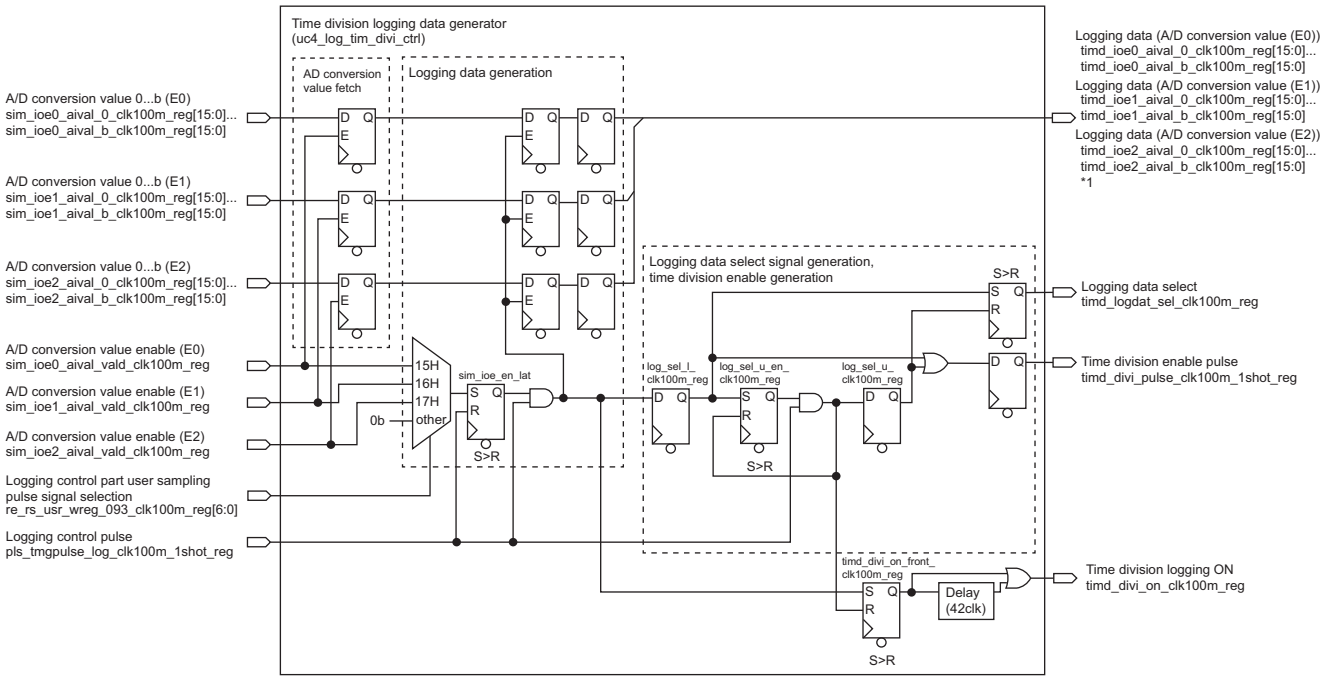
A/D conversion value enable (E0): sim_ioe0_aival_vald_clk100m_reg

A/D conversion value enable (E1): sim_ioe1_aival_vald_clk100m_reg

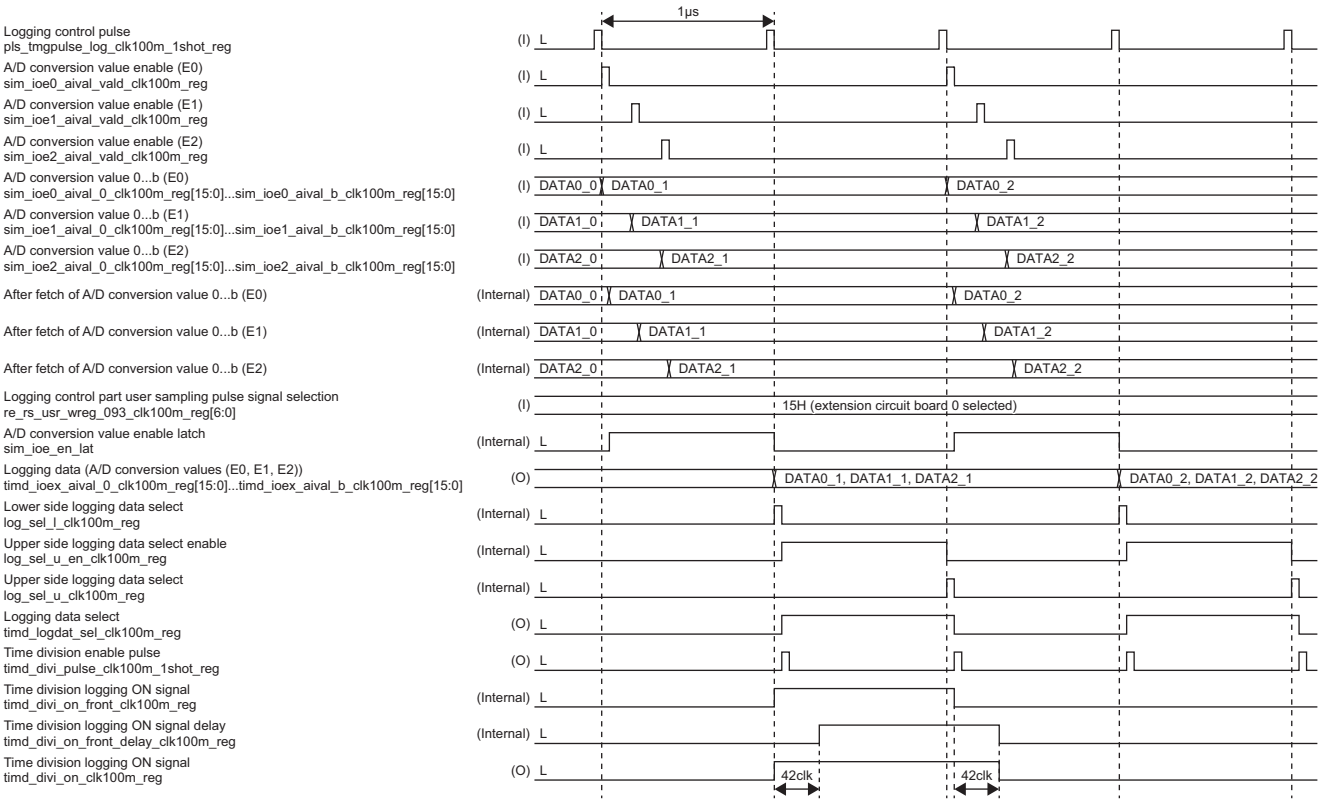
A/D conversion value enable (E2): sim_ioe2_aival_vald_clk100m_reg

- Generates logging data lower/upper selection signal
- Generates enable pulses for time sharing

The block diagram and timing chart of the time division logging data generator are shown below.



*1 A/D conversion value bit assignment is timd_ioe2_aival_b_clk100m_reg, timd_ioe2_aival_a_clk100m_reg····, timd_ioe0_aival_1_clk100m_reg, timd_ioe0_aival_0_clk100m_reg.


1µs
Logging control pulse
pls_tmgpulse_log_clk100m_1shot_reg
(I) L
A/D conversion value enable (E0)
sim_ioe0_aival_vald_clk100m_reg
(I) L
A/D conversion value enable (E1)
sim_ioe1_aival_vald_clk100m_reg
(I) L
A/D conversion value enable (E2)
sim_ioe2_aival_vald_clk100m_reg
(I) L
A/D conversion value 0...b (E0)
sim_ioe0_aival_0_clk100m_reg[15:0]...sim_ioe0_aival_b_clk100m_reg[15:0]
(I) DATA0_0 DATA0_1 DATA0_2
A/D conversion value 0...b (E1)
sim_ioe1_aival_0_clk100m_reg[15:0]...sim_ioe1_aival_b_clk100m_reg[15:0]
(I) DATA1_0 DATA1_1 DATA1_2
A/D conversion value 0...b (E2)
sim_ioe2_aival_0_clk100m_reg[15:0]...sim_ioe2_aival_b_clk100m_reg[15:0]
(I) DATA2_0 DATA2_1 DATA2_2
After fetch of A/D conversion value 0...b (E0)
(Internal) DATA0_0 DATA0_1 DATA0_2
After fetch of A/D conversion value 0...b (E1)
(Internal) DATA1_0 DATA1_1 DATA1_2
After fetch of A/D conversion value 0...b (E2)
(Internal) DATA2_0 DATA2_1 DATA2_2
Logging control part user sampling pulse signal selection
re_rs_usr_wreg_093_clk100m_reg[6:0]
(I) 15H (extension circuit board 0 selected)
A/D conversion value enable latch
sim_ioe_en_lat
(Internal) L
Logging data (A/D conversion values (E0, E1, E2))
timd_ioex_aival_0_clk100m_reg[15:0]...timd_ioex_aival_b_clk100m_reg[15:0]
(O) DATA0_1, DATA1_1, DATA2_1 DATA0_2, DATA1_2, DATA2_2
Lower side logging data select
log_sel_l_clk100m_reg
(Internal) L
Upper side logging data select enable
log_sel_u_en_clk100m_reg
(Internal) L
Upper side logging data select
log_sel_u_clk100m_reg
(Internal) L
Logging data select
timd_logdat_sel_clk100m_reg
(O) L
Time division enable pulse
timd_divi_pulse_clk100m_1shot_reg
(O) L
Time division logging ON signal
timd_divi_on_front_clk100m_reg
(Internal) L
Time division logging ON signal delay
timd_divi_on_front_delay_clk100m_reg
(Internal) L
Time division logging ON signal
timd_divi_on_clk100m_reg
(O) L
42clk
42clk

■Loading A/D conversion value

The A/D conversion value is loaded at "A/D conversion value enable". The data corresponding to loading is shown below.

A/D conversion value enable (loaded if (1))	A/D conversion value target signal	Signal after loading A/D conversion value	Remarks
sim_ioe0_aival_vald_clk100m_reg	sim_ioe0_aival_0_clk100m_reg to sim_ioe0_aival_b_clk100m_reg	sim_ioe0_aival_0_d1_clk100m_reg to sim_ioe0_aival_b_d1_clk100m_reg	E0
sim_ioe1_aival_vald_clk100m_reg	sim_ioe1_aival_0_clk100m_reg to sim_ioe1_aival_b_clk100m_reg	sim_ioe1_aival_0_d1_clk100m_reg to sim_ioe1_aival_b_d1_clk100m_reg	E1
sim_ioe2_aival_vald_clk100m_reg	sim_ioe2_aival_0_clk100m_reg to sim_ioe2_aival_b_clk100m_reg	sim_ioe2_aival_0_d1_clk100m_reg to sim_ioe2_aival_b_d1_clk100m_reg	E2

■Generating logging data

Select an extension module (E0, E1, E2) targeted for logging timing, and generate logging data synchronized with "A/D conversion value enable" of the selected extension module. For the extension module targeted for logging timing, select it from "Logging control part user sampling pulse signal selection (re_rs_usr_wreg_093_clk100m_reg)". Latch (sim_ioe_en_lat) it with enable signals of the selected "A/D conversion enable (sim_ioe0_aival_vald_clk100m_reg)", "A/D conversion enable (sim_ioe1_aival_vald_clk100m_reg)", and "A/D conversion enable (sim_ioe2_aival_vald_clk100m_reg)". Generate the following logging data from the latched enable signal and the periodically input "Logging control pulse (pls_tmgpulse_log_clk100m_1shot_reg)".

timd_ioe0_aival_0_clk100m_reg, timd_ioe0_aival_b_clk100m_reg, timd_ioe1_aival_0_clk100m_reg, timd_ioe1_aival_b_clk100m_reg, timd_ioe2_aival_0_clk100m_reg, timd_ioe2_aival_b_clk100m_reg

Target enable selection, target enable signal latch, and logging data generation are shown below.

• Target enable selection

Logging control part: User sampling pulse signal selection (re_rs_usr_wreg_093_clk100m_reg[6:0])	Selection signal (sim_ioe_en)	Remarks
15h	sim_ioe0_aival_vald_clk100m_reg	Select E0.
16h	sim_ioe1_aival_vald_clk100m_reg	Select E1.
17h	sim_ioe2_aival_vald_clk100m_reg	Select E2.
Except for that shown above	Fixed to 0.	No selection

• Target enable signal latch

usr_rst_n	clk100m	Selection signal (sim_ioe_en)	Logging control pulse (pls_tmgpulse_log_clk100m_1shot_reg)	Select signal enable signal latch (sim_ioe_en_lat)
0b (enable)	×	×	×	0b (enable)
1b (disable)	↑	1b	×	1b (disable)
1b	↑	0b	1b	0b

• Generation of logging data

usr_rst_n	clk100m	Select signal enable signal latch (sim_ioe_en_lat)	Logging control pulse (pls_tmgpulse_log_clk100m_1shot_reg)	A/D conversion value (E0) (timd_ioe0_aival_0_clk100m_reg[15:0] to timd_ioe0_aival_b_clk100m_reg[15:0])*1
0b (enable)	×	×	×	Outputs all 0s.
1b (disable)	↑	0b (disable)	×	Holds the previous value.
1b	↑	1b (enable)	1b	sim_ioe0_aival_0_d1_clk100m_reg to sim_ioe0_aival_b_d1_clk100m_reg

*1 E1 and E2 have the same structure.

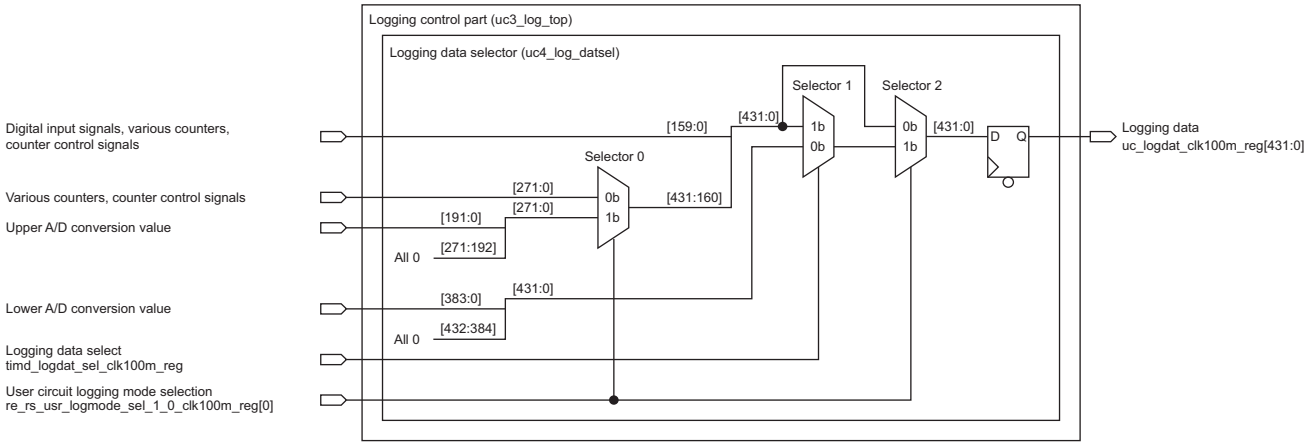
■Logging data select signal generation, time division enable pulse generation, time division logging ON signal generation

Generates "Logging data select (timd_logdat_sel_clk100m_reg)" and "Time division enable pulse (timd_divi_pulse_clk100m_1shot_reg)" that select the upper and lower A/D conversion values. The time division enable pulse is output twice at "Logging control pulse receive (pls_tmgpulse_log_clk100m_1shot_reg)" after A/D conversion value is loaded (sim_ioe_en_lat=1 (enabled)). For the output timing, refer to the timing chart. The logging data select is output by a flip-flop that is set (selects the upper logging data) with the first time division enable pulse and reset (selects the lower logging data) with its second time. Time division logging ON is generated by SR-FF, which is set at the first time division enable pulse and reset at the second time, and the generated signal is expanded by 42 cycles and then output. For the output timing, refer to the timing chart.

Logging data selector

Logging data is structured with various counters, counter control signals, and A/D conversion values. "User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])" selects whether to enable or disable time division.
When time division is enabled, the logging data is output alternately between upper and lower sections by logging data selection. A block diagram of the logging data selector is shown below. For bit assignment of logging data, refer to the following.

☞ Page 714 Logging Data Bit Assignment



■Selector 0

Selects the logging data by "User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])".
(Assignment of [431:0] of [1023:0] in time division mode)

User circuit logging mode selection	Bit assignment
0b	{48{0b}, cnt_ioe2_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_ioe2_32ring_2pha4multi_phb, cnt_ioe2_32ring_2pha4multi_pha, cnt_ioe1_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_ioe1_32ring_2pha4multi_phb, cnt_ioe1_32ring_2pha4multi_pha, cnt_ioe0_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_ioe0_32ring_2pha4multi_phb, cnt_ioe0_32ring_2pha4multi_pha, cnt_iob2_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_iob2_32ring_2pha4multi_phb, cnt_iob2_32ring_2pha4multi_pha, cnt_iob1_32ring_2pha4multi_counter_clk100m_reg[31:0]}
1b	{80{0b}, timd_ioe0_aival_b_clk100m_reg[15:0], timd_ioe0_aival_a_clk100m_reg[15:0], timd_ioe0_aival_9_clk100m_reg[15:0], timd_ioe0_aival_8_clk100m_reg[15:0], timd_ioe0_aival_7_clk100m_reg[15:0], timd_ioe0_aival_6_clk100m_reg[15:0], timd_ioe0_aival_5_clk100m_reg[15:0], timd_ioe0_aival_4_clk100m_reg[15:0], timd_ioe0_aival_3_clk100m_reg[15:0], timd_ioe0_aival_2_clk100m_reg[15:0], timd_ioe0_aival_1_clk100m_reg[15:0], timd_ioe0_aival_0_clk100m_reg[15:0]}

■Selector 1

Selects the logging data by "Logging data select (timd_logdat_sel_clk100m_reg)". (Assignment of [943:512] of [1023:0] in time division mode)

Logging data select	Bit assignment
0b	{48{0b}, timd_ioe2_aival_b_clk100m_reg[15:0], timd_ioe2_aival_a_clk100m_reg[15:0], timd_ioe2_aival_9_clk100m_reg[15:0], timd_ioe2_aival_8_clk100m_reg[15:0], timd_ioe2_aival_7_clk100m_reg[15:0], timd_ioe2_aival_6_clk100m_reg[15:0], timd_ioe2_aival_5_clk100m_reg[15:0], timd_ioe2_aival_4_clk100m_reg[15:0], timd_ioe2_aival_3_clk100m_reg[15:0], timd_ioe2_aival_2_clk100m_reg[15:0], timd_ioe2_aival_1_clk100m_reg[15:0], timd_ioe2_aival_0_clk100m_reg[15:0], timd_ioe1_aival_b_clk100m_reg[15:0], timd_ioe1_aival_a_clk100m_reg[15:0], timd_ioe1_aival_9_clk100m_reg[15:0], timd_ioe1_aival_8_clk100m_reg[15:0], timd_ioe1_aival_7_clk100m_reg[15:0], timd_ioe1_aival_6_clk100m_reg[15:0], timd_ioe1_aival_5_clk100m_reg[15:0], timd_ioe1_aival_4_clk100m_reg[15:0], timd_ioe1_aival_3_clk100m_reg[15:0], timd_ioe1_aival_2_clk100m_reg[15:0], timd_ioe1_aival_1_clk100m_reg[15:0], timd_ioe1_aival_0_clk100m_reg[15:0]}
1b	{selector 0 result, 14{0b}, cnt_iob1_32ring_2pha4multi_phb, cnt_iob1_32ring_2pha4multi_pha, cnt_iob0_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_iob0_32ring_2pha4multi_phb, cnt_iob0_32ring_2pha4multi_pha, sim_ioe2_x_clk100m_reg[15:0], sim_ioe1_x_clk100m_reg[15:0], sim_ioe0_x_clk100m_reg[15:0], sim_iob2_x_clk100m_reg[15:0], sim_iob1_x_clk100m_reg[15:0], sim_iob0_x_clk100m_reg[15:0]}

■Selector 2

Selects the logging data by "User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])". (Assignment of [943:512] of [1023:0] in time division mode)

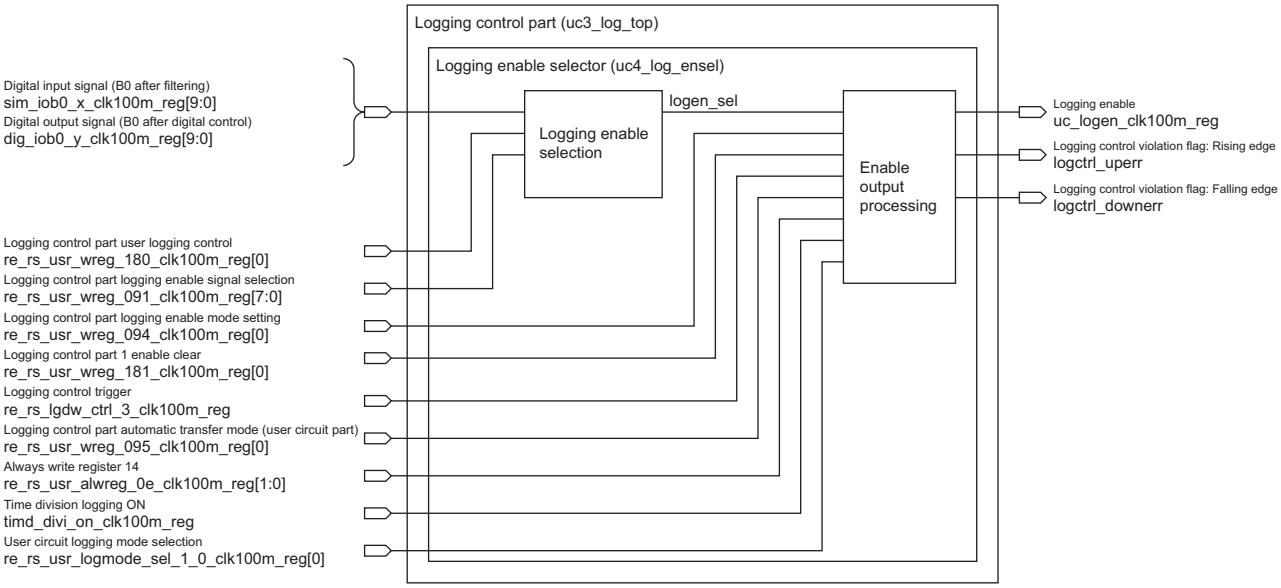
User circuit logging mode selection	Bit assignment
0b	{selector 0 result, 14{0b}, cnt_iob1_32ring_2pha4multi_phb, cnt_iob1_32ring_2pha4multi_pha, cnt_iob0_32ring_2pha4multi_counter_clk100m_reg[31:0], 14{0b}, cnt_iob0_32ring_2pha4multi_phb, cnt_iob0_32ring_2pha4multi_pha, sim_ioe2_x_clk100m_reg[15:0], sim_ioe1_x_clk100m_reg[15:0], sim_ioe0_x_clk100m_reg[15:0], sim_iob2_x_clk100m_reg[15:0], sim_iob1_x_clk100m_reg[15:0], sim_iob0_x_clk100m_reg[15:0]}
1b	Selector 1 result

Logging enable selector

The logging enable selector outputs logging enable (logging start) to the logging block. It selects and outputs the logging enable signal from the digital input signal (B0 after filtering), digital input signal (B0 after digital control), and "Logging control part user logging control" by "Logging control part logging enable signal selection". In addition, "Logging control part logging enable mode setting" controls whether the logging enable signal is output multiple times (multiple-enable mode) or only once (one-enable mode).

After these operations, an automatic transfer mode is implemented to control the rising edge and falling edge of logging enable by firmware. When "Logging control part automatic transfer mode (user circuit part)" is set to Enable (1), logging enable is output by "Logging control trigger".

A block diagram of the logging enable selector is shown below.



■Logging enable selection

According to the value set in "Logging control part logging enable signal selection (re_rs_usr_wreg_091_clk100m_reg[7: 0])", it selects the signal (logen_sel) to be output to the level immediately below. Logging enable signal selection is shown below.

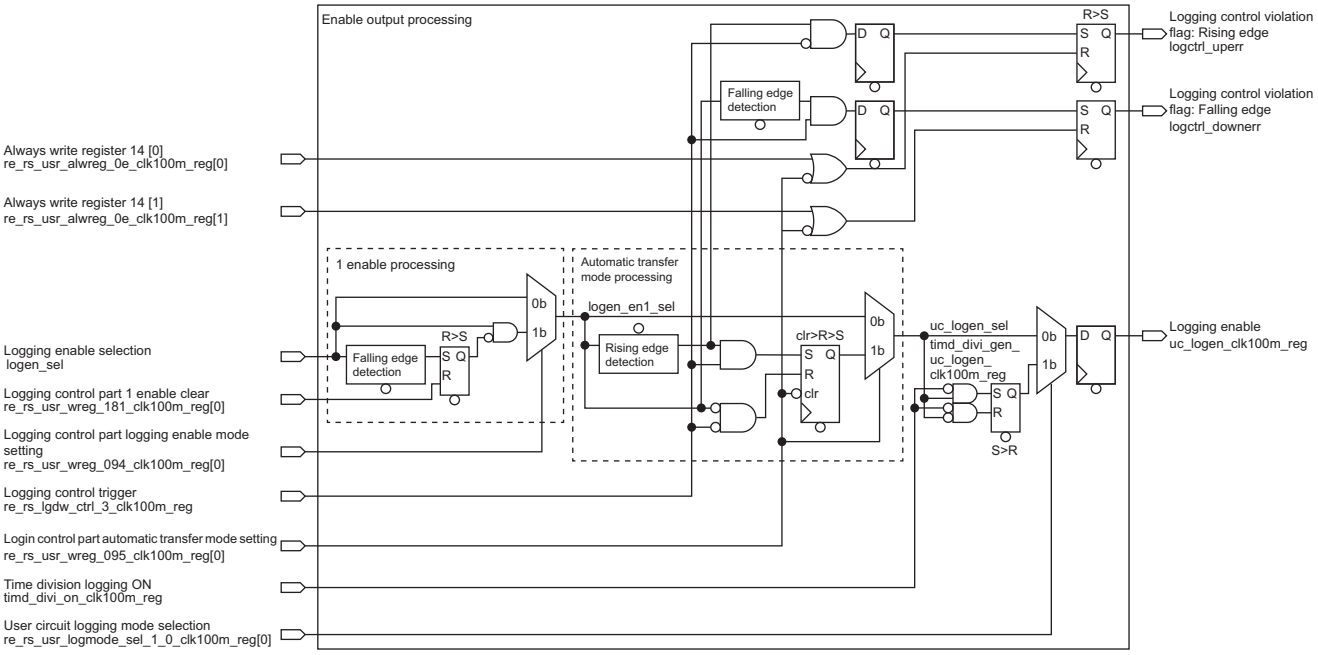
Logging control part logging enable signal selection	logen_sel	Description
01H	sim_iob0_x_clk100m_reg[0]	Digital input signal of IOB0_X[0] (B0 after filtering)
02H	sim_iob0_x_clk100m_reg[1]	Digital input signal of IOB0_X[1] (B0 after filtering)
03H	sim_iob0_x_clk100m_reg[2]	Digital input signal of IOB0_X[2] (B0 after filtering)
04H	sim_iob0_x_clk100m_reg[3]	Digital input signal of IOB0_X[3] (B0 after filtering)
05H	sim_iob0_x_clk100m_reg[4]	Digital input signal of IOB0_X[4] (B0 after filtering)
06H	sim_iob0_x_clk100m_reg[5]	Digital input signal of IOB0_X[5] (B0 after filtering)
07H	sim_iob0_x_clk100m_reg[6]	Digital input signal of IOB0_X[6] (B0 after filtering)
08H	sim_iob0_x_clk100m_reg[7]	Digital input signal of IOB0_X[7] (B0 after filtering)
09H	sim_iob0_x_clk100m_reg[8]	Digital input signal of IOB0_X[8] (B0 after filtering)
0AH	sim_iob0_x_clk100m_reg[9]	Digital input signal of IOB0_X[9] (B0 after filtering)
0BH	dig_iob0_y_clk100m_reg[0]	Digital output signal of IOB0_Y[0] (B0 after digital control)
0CH	dig_iob0_y_clk100m_reg[1]	Digital output signal of IOB0_Y[1] (B0 after digital control)
0DH	dig_iob0_y_clk100m_reg[2]	Digital output signal of IOB0_Y[2] (B0 after digital control)
0EH	dig_iob0_y_clk100m_reg[3]	Digital output signal of IOB0_Y[3] (B0 after digital control)
0FH	dig_iob0_y_clk100m_reg[4]	Digital output signal of IOB0_Y[4] (B0 after digital control)
10H	dig_iob0_y_clk100m_reg[5]	Digital output signal of IOB0_Y[5] (B0 after digital control)
11H	dig_iob0_y_clk100m_reg[6]	Digital output signal of IOB0_Y[6] (B0 after digital control)
12H	dig_iob0_y_clk100m_reg[7]	Digital output signal of IOB0_Y[7] (B0 after digital control)
13H	dig_iob0_y_clk100m_reg[8]	Digital output signal of IOB0_Y[8] (B0 after digital control)
14H	dig_iob0_y_clk100m_reg[9]	Digital output signal of IOB0_Y[9] (B0 after digital control)
15H	re_rs_usr_wreg_180_clk100m_reg[0]	Logging control part: User logging control [0]
Except for that shown above	0b	Fixed to 0.

■Enable output processing

The enable output processing part performs one-enable processing and automatic transfer mode processing.

One-enable processing determines the output mode of "Logging enable (uc_logen_clk100m_reg)" according to the setting of "Logging control part logging enable mode setting". The operation and RTL diagram for each output mode are shown below.

Logging control part logging enable mode setting	Mode name	Mode description
0b	Multiple-enable mode	Outputs through the signal selected by logging enable selection.
1b	One-enable mode	Outputs the signal selected by logging enable selection the first time. (Output H only once.) To output the next logging enable, switch "Logging control part 1 enable clear (re_rs_usr_wreg_181_clk100m_reg[0])" in the order of Disable (0), Enable (1), and Disable (0). Also, It can also be output by switching "usr_rst_n" to Enable (0) and Disable (1) in that order.



Automatic transfer mode processing selects whether to output the logging enable output from one-enable processing in the automatic transfer mode or through output.

When "Logging control part automatic transfer mode setting (re_rs_usr_wreg_095_clk100m_reg)" is Automatic transfer mode enabled (1), Logging enable is selected at the rising/falling edge output from one-enable processing according to the setting value of "Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg)". The truth table of "Logging enable selection signal (uc_logen_sel)" is shown below.

Logging control part automatic transfer mode setting (re_rs_usr_wreg_095_clk100m_reg[0])	Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg)	One-enable processing output signal (logen_en1_sel)	Logging enable selection signal (uc_logen_sel)	Remarks
0b (disable)	—	—	logen_en1_sel	Through output
1b (enable)	0b (falling edge enable)	0b	0b	—
1b	0b	Rising edge	Holds the previous value.	—
1b	1b (rising edge enabled)	0b	Holds the previous value.	—
1b	1b	Rising edge	1b	—
Except for that shown above			Holds the previous value.	—

Also, if the logging enable output condition is not met, the logging control violation flag is output. The truth table of the logging control violation flag is shown below.

Logging control part automatic transfer mode setting (re_rs_usr_wreg_095_clk100m_reg[0])	Always write register 14 (re_rs_usr_alwreg_0e_clk100m_reg)		Logging control trigger (re_rs_lgdw_ctrl_3_clk100m_reg)	One-enable processing output signal (logen_en1_sel)	Always read register 14 (re_rs_usr_alrreg_0e_clk100m_reg)	
	[1]	[0]			[1]	[0]
0b (disable)	—	—	—	—	0b	0b
1b (enable)	1b	1b	—	—	0b	0b
1b	1b	0b	0b (falling edge enable)	Rising edge	0b	1b
1b	1b	0b	0b	Falling edge	0b	Holds the previous value.
1b	1b	0b	1b (rising edge enabled)	Rising edge	0b	Holds the previous value.
1b	1b	0b	1b	Falling edge	0b	Holds the previous value.
1b	0b	1b	0b	Rising edge	Holds the previous value.	0b
1b	0b	1b	0b	Falling edge	Holds the previous value.	0b
1b	0b	1b	1b	Rising edge	Holds the previous value.	0b
1b	0b	1b	1b	Falling edge	1b	0b
1b	0b	0b	0b	Rising edge	Holds the previous value.	1b
1b	0b	0b	0b	Falling edge	Holds the previous value.	Holds the previous value.
1b	0b	0b	1b	Rising edge	Holds the previous value.	Holds the previous value.
1b	0b	0b	1b	Falling edge	1b	Holds the previous value.
Except for that shown above					Holds the previous value.	Holds the previous value.

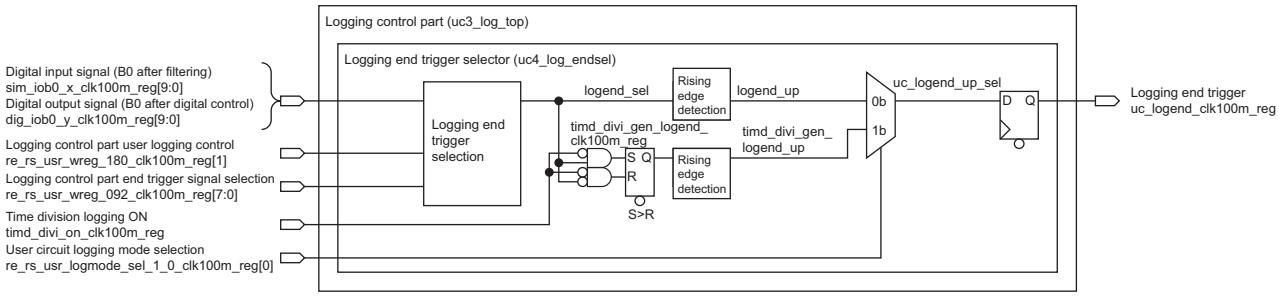
In addition, "Logging enable (uc_logen_clk100m_reg)" is generated by combining "User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])" and "Time division logging ON (timd_divi_on_clk100m_reg)". The logging enable truth table is shown below.

User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])	Time division logging ON (timd_divi_on_clk100m_reg)	Logging enable selection signal (uc_logen_sel)	Logging enable (uc_logen_clk100m_reg)	Remarks
0b (disable)	—	—	uc_logen_sel	Through output
1b (enable)	1b (enable)	—	Holds the previous value.	—
1b	0b (disable)	1b	1b	—
1b	0b	0b	0b	—

Logging end trigger selector

The logging end trigger selector outputs the logging end trigger to be output to the logging part. It selects "Digital input signal (B0 after filtering)" and "Digital output signal (B0 after digital control)" from "Logging control part end trigger signal selection", and selects "Logging end trigger" from "Logging control part user logging control". It detects the rising edge of the selected signal and outputs 1 pulse (clk100m).

A block diagram of the logging end trigger selector is shown below.



■Logging end trigger selection

According to the value set in "Logging control part end trigger signal selection (re_rs_usr_wreg_092_clk100m_reg[7: 0])", it selects the signal (logend_sel) to be output to the level immediately below. The signals to select are shown below. Also, the selected signal is detected on its rising edge and output to the level immediately below.

Logging control part end trigger signal selection (re_rs_usr_wreg_092_clk100m_reg[7:0])	logen_sel	Description
01H	sim_iob0_x_clk100m_reg[0]	Digital input signal of IOB0_X[0] (B0 after filtering)
02H	sim_iob0_x_clk100m_reg[1]	Digital input signal of IOB0_X[1] (B0 after filtering)
03H	sim_iob0_x_clk100m_reg[2]	Digital input signal of IOB0_X[2] (B0 after filtering)
04H	sim_iob0_x_clk100m_reg[3]	Digital input signal of IOB0_X[3] (B0 after filtering)
05H	sim_iob0_x_clk100m_reg[4]	Digital input signal of IOB0_X[4] (B0 after filtering)
06H	sim_iob0_x_clk100m_reg[5]	Digital input signal of IOB0_X[5] (B0 after filtering)
07H	sim_iob0_x_clk100m_reg[6]	Digital input signal of IOB0_X[6] (B0 after filtering)
08H	sim_iob0_x_clk100m_reg[7]	Digital input signal of IOB0_X[7] (B0 after filtering)
09H	sim_iob0_x_clk100m_reg[8]	Digital input signal of IOB0_X[8] (B0 after filtering)
0AH	sim_iob0_x_clk100m_reg[9]	Digital input signal of IOB0_X[9] (B0 after filtering)
0BH	dig_iob0_y_clk100m_reg[0]	Digital output signal of IOB0_Y[0] (B0 after digital control)
0CH	dig_iob0_y_clk100m_reg[1]	Digital output signal of IOB0_Y[1] (B0 after digital control)
0DH	dig_iob0_y_clk100m_reg[2]	Digital output signal of IOB0_Y[2] (B0 after digital control)
0EH	dig_iob0_y_clk100m_reg[3]	Digital output signal of IOB0_Y[3] (B0 after digital control)
0FH	dig_iob0_y_clk100m_reg[4]	Digital output signal of IOB0_Y[4] (B0 after digital control)
10H	dig_iob0_y_clk100m_reg[5]	Digital output signal of IOB0_Y[5] (B0 after digital control)
11H	dig_iob0_y_clk100m_reg[6]	Digital output signal of IOB0_Y[6] (B0 after digital control)
12H	dig_iob0_y_clk100m_reg[7]	Digital output signal of IOB0_Y[7] (B0 after digital control)
13H	dig_iob0_y_clk100m_reg[8]	Digital output signal of IOB0_Y[8] (B0 after digital control)
14H	dig_iob0_y_clk100m_reg[9]	Digital output signal of IOB0_Y[9] (B0 after digital control)
15H	re_rs_usr_wreg_180_clk100m_reg[1]	Logging control part: User logging control [1]
Except for that shown above	0b	Fixed to 0.

The combination of "Time division logging ON (timd_divi_on_clk100m_reg)" generates "Time division logging end trigger signal (timd_divi_gen_logend_clk100m_reg)". The truth table of the time division logging end trigger signal is shown below.

Time division logging ON (timd_divi_on_clk100m_reg)	Logging end trigger selection signal (uc_logend_sel)	Time division logging end trigger signal (timd_divi_gen_logend_clk100m_reg)
1b (enable)	—	Hold the previous value.
0b (disable)	1b	1b
0b	0b	0b

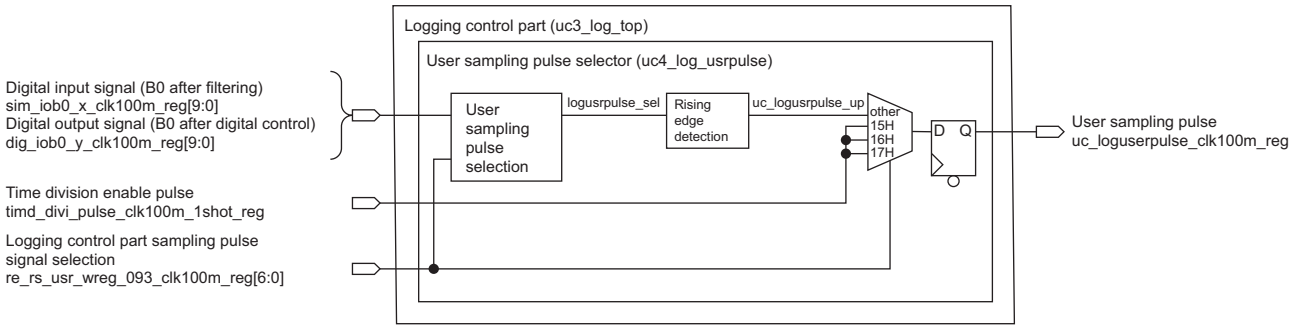
In addition, the logging end trigger is selected and output by "User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])". The truth table of the logging end trigger signal is shown below.

User circuit logging mode selection (re_rs_usr_logmode_sel_1_0_clk100m_reg[0])	Logging end trigger signal (uc_logend_clk100m_reg)
0b	Detects and outputs the rising edge of logend_sel.
1b	Detects and outputs the rising edge of timd_divi_gen_logend_clk100m_reg.

User sampling pulse selector

The user sampling pulse selector outputs the user sampling pulse to the logging block. It selects "Digital input signal (B0 after filtering)" and "Digital input signal (B0 after digital control)" from "Logging control part sampling pulse signal selection", and selects "User sampling pulse" from "Logging control part sampling pulse signal selection". It outputs 1 pulse (clk100m) when the rising edge of the selected signal is detected.

A block diagram of the user sampling pulse selector is shown below.



■Select sampling pulses

The signal (logusrpulse_sel) to be output to the level immediately below is selected according to the value set in "Logging control part sampling pulse signal selection (re_rs_usr_wreg_093_clk100m_reg[6:0])". After the rising edge of the selected signal is detected, it is output to the level immediately below.

If the value of "Logging control part sampling pulse signal selection (re_rs_usr_wreg_093_clk100m_reg)" is 15H, 16H, or 17H, "Time division enable pulse (timd_divi_pulse_clk100m_1shot_reg)" is selected. Otherwise, the logusrpulse_sel rising edge detection signal is selected and output.

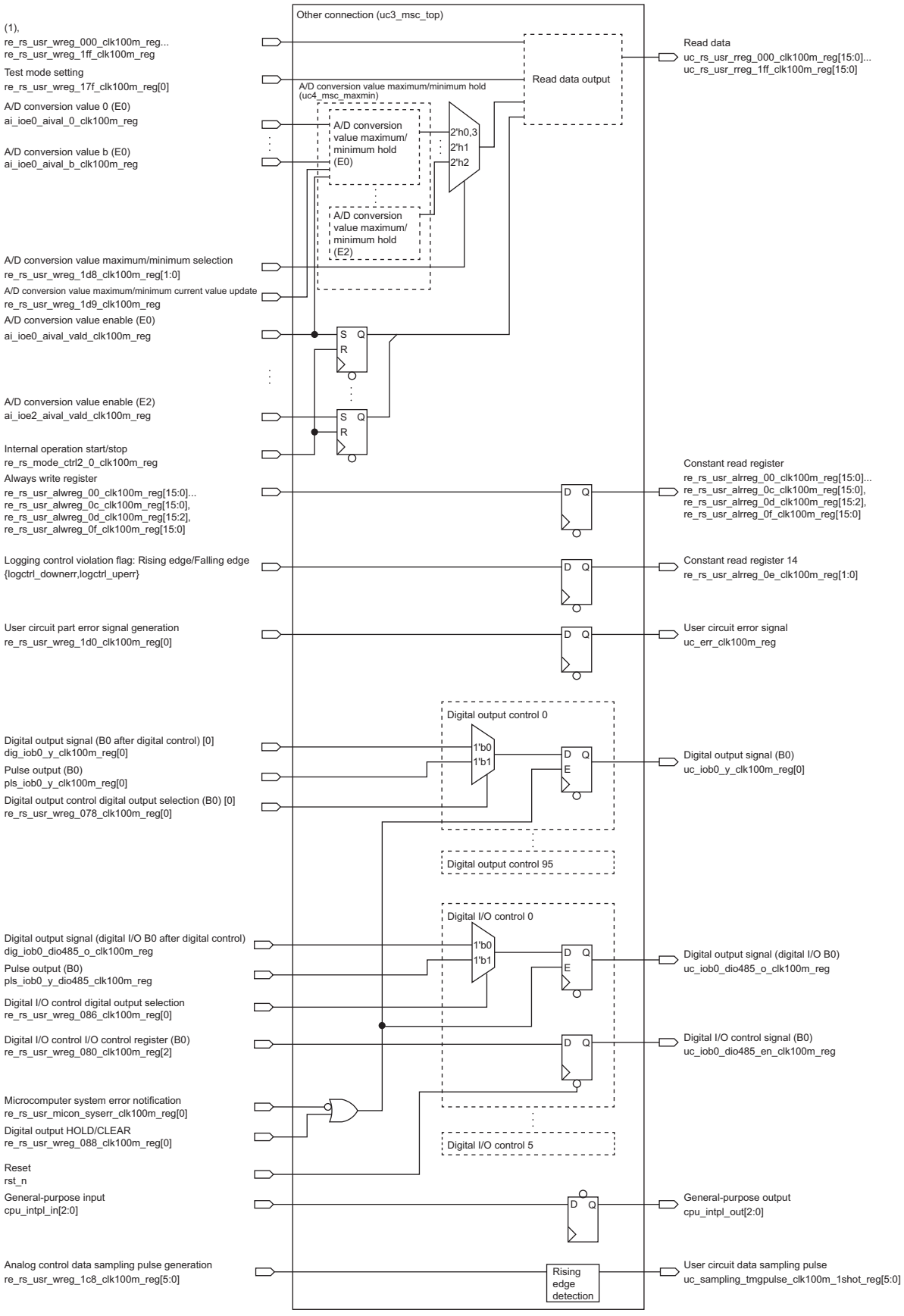
The signals to be selected are shown below.

Logging control part sampling pulse signal selection (re_rs_usr_wreg_093_clk100m_reg[6:0])	logusrpulse_sel	Description
01H	sim_iob0_x_clk100m_reg[0]	Digital input signal of IOB0_X[0] (B0 after filtering)
02H	sim_iob0_x_clk100m_reg[1]	Digital input signal of IOB0_X[1] (B0 after filtering)
03H	sim_iob0_x_clk100m_reg[2]	Digital input signal of IOB0_X[2] (B0 after filtering)
04H	sim_iob0_x_clk100m_reg[3]	Digital input signal of IOB0_X[3] (B0 after filtering)
05H	sim_iob0_x_clk100m_reg[4]	Digital input signal of IOB0_X[4] (B0 after filtering)
06H	sim_iob0_x_clk100m_reg[5]	Digital input signal of IOB0_X[5] (B0 after filtering)
07H	sim_iob0_x_clk100m_reg[6]	Digital input signal of IOB0_X[6] (B0 after filtering)
08H	sim_iob0_x_clk100m_reg[7]	Digital input signal of IOB0_X[7] (B0 after filtering)
09H	sim_iob0_x_clk100m_reg[8]	Digital input signal of IOB0_X[8] (B0 after filtering)
0AH	sim_iob0_x_clk100m_reg[9]	Digital input signal of IOB0_X[9] (B0 after filtering)
0BH	dig_iob0_y_clk100m_reg[0]	Digital output signal of IOB0_Y[0] (B0 after digital control)
0CH	dig_iob0_y_clk100m_reg[1]	Digital output signal of IOB0_Y[1] (B0 after digital control)
0DH	dig_iob0_y_clk100m_reg[2]	Digital output signal of IOB0_Y[2] (B0 after digital control)
0EH	dig_iob0_y_clk100m_reg[3]	Digital output signal of IOB0_Y[3] (B0 after digital control)
0FH	dig_iob0_y_clk100m_reg[4]	Digital output signal of IOB0_Y[4] (B0 after digital control)
10H	dig_iob0_y_clk100m_reg[5]	Digital output signal of IOB0_Y[5] (B0 after digital control)
11H	dig_iob0_y_clk100m_reg[6]	Digital output signal of IOB0_Y[6] (B0 after digital control)
12H	dig_iob0_y_clk100m_reg[7]	Digital output signal of IOB0_Y[7] (B0 after digital control)
13H	dig_iob0_y_clk100m_reg[8]	Digital output signal of IOB0_Y[8] (B0 after digital control)
14H	dig_iob0_y_clk100m_reg[9]	Digital output signal of IOB0_Y[9] (B0 after digital control)
Except for that shown above	0b	Fixed to 0.

Output block part (uc3_msc_top)

This module controls signal output to each block. The output signals are shown below.

■Block Diagram



(1) Various statuses

■Function List

Function	Description
Read data output	Outputs various statuses to check the internal status of the user circuit. Also, it selects and connects the FPGA internal status, "Write data (transient area)", and "Write data (cyclic area)" by setting "Test mode setting". For details, refer to the following. ☞ Page 592 Test mode setting
Always read register output	Connects the always write register 0 to C15 to always read register 0 to 15 in one flip-flop level (clk100m). Connections for exceptions are shown below. Always write register 14[0]: Logging control violation flag rising edge clear Always write register 14[1]: Logging control violation flag falling edge clear Always read register 14[0]: Logging control violation flag rising edge Always read register 14[1]: Logging control violation flag falling edge
Error signal output	"User circuit part error signal generation [0]" is output in one flip-flop level (clk100m).
Digital output control	Selects the signal from the pulse output part or digital control part and outputs it as a digital signal. Also, depending on the setting value of "Digital output HOLD/CLEAR", "Microcomputer system error notification" is set to Enable (1) and the output value is HOLD/CLEAR.
Digital input/output control	"Digital input/output control input/output control register (B0) [3:2]" is output in one flip-flop level (clk100m). Also, depending on the setting value of "Digital output HOLD/CLEAR", "Microcomputer system error notification" is set to Enable (1) and the output value is HOLD/CLEAR.
General-purpose output	Outputs general-purpose input (cpu_intpl_in). (Outputs in one flip-flop level (clk100m))
Data sampling pulse output	Outputs the signal that detected the rising edge of "Analog control data sampling pulse generation (re_rs_usr_wreg_1c8_clk100m_reg)".
ADC conversion enable status	Sets when A/D conversion value enable (E0), (E1), (E2) from extension module (E0, E1, E2) is set to Enable (1), and resets when internal operation start/stop is Stop (1). The set/reset signal is connected to the read data.
A/D conversion value maximum/minimum hold	Holds the maximum and minimum A/D conversion values of the extension module (E0, E1, E2). The maximum initial value is set to 8000H and the minimum initial value is set to 7FFFH, and when "A/D conversion value enable" is set to Enable (1), they are compared with the A/D conversion value and held. Also, at the rising edge of "Analog control A/D conversion value maximum/minimum current value update", "A/D conversion value maximum/minimum" is updated to the current value. When this happens, priority is given in descending order of analog control A/D conversion value maximum/minimum current value update and analog input enable.

■Terminal list

Signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
clk100m	I	—	System clock	cc2_top	—	—
usr_rst_n	I	L	Reset for user circuit (the AND between reset and internal operation start/stop)	uc2_top	1b	—
dig_iob0_y_clk100m_reg[15:0]	I	—	Digital output signal (B0 after digital control)	Digital control part	0000H	—
dig_iob1_y_clk100m_reg[15:0]	I	—	Digital output signal (B1 after digital control)	Digital control part	0000H	—
dig_iob2_y_clk100m_reg[15:0]	I	—	Digital output signal (B2 after digital control)	Digital control part	0000H	—
dig_ioe0_y_clk100m_reg[15:0]	I	—	Digital output signal (E0 after digital control)	Digital control part	0000H	—
dig_ioe1_y_clk100m_reg[15:0]	I	—	Digital output signal (E1 after digital control)	Digital control part	0000H	—
dig_ioe2_y_clk100m_reg[15:0]	I	—	Digital output signal (E2 after digital control)	Digital control part	0000H	—
dig_iob0_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output B0 after digital control)	Digital control part	0b	—
dig_iob1_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output B1 after digital control)	Digital control part	0b	—
dig_iob2_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output B2 after digital control)	Digital control part	0b	—
dig_ioe0_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output E0 after digital control)	Digital control part	0b	—
dig_ioe1_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output E1 after digital control)	Digital control part	0b	—
dig_ioe2_dio485_o_clk100m_reg	I	—	Digital output signal (digital input/output E2 after digital control)	Digital control part	0b	—

Signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
pls_iob0_y_clk100m_reg[15:0]	I	—	Pulse output (B0)	Pulse output part	0000H	—
pls_iob0_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (B0)	Pulse output part	0b	—
pls_iob1_y_clk100m_reg[15:0]	I	—	Pulse output (B1)	Pulse output part	0000H	—
pls_iob1_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (B1)	Pulse output part	0b	—
pls_iob2_y_clk100m_reg[15:0]	I	—	Pulse output (B2)	Pulse output part	0000H	—
pls_iob2_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (B2)	Pulse output part	0b	—
pls_ioe0_y_clk100m_reg[15:0]	I	—	Pulse output (E0)	Pulse output part	0000H	—
pls_ioe0_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (E0)	Pulse output part	0b	—
pls_ioe1_y_clk100m_reg[15:0]	I	—	Pulse output (E1)	Pulse output part	0000H	—
pls_ioe1_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (E1)	Pulse output part	0b	—
pls_ioe2_y_clk100m_reg[15:0]	I	—	Pulse output (E2)	Pulse output part	0000H	—
pls_ioe2_y_dio485_clk100m_reg	I	—	Pulse output (digital input/output) (E2)	Pulse output part	0b	—
cpu_intpl_in[2:0]	I	—	General-purpose input	top1	0H	—
re_rs_usr_micon_syserr_clk100m_reg	I	H	MCU system error notification	re2_top	0b	—
re_rs_usr_wreg_080_clk100m_reg[2]	I	—	Digital input/output control input/output control register (B0)	re2_top	0b	—
re_rs_usr_wreg_081_clk100m_reg[2]	I	—	Digital input/output control input/output control register (B1)	re2_top	0b	—
re_rs_usr_wreg_082_clk100m_reg[2]	I	—	Digital input/output control input/output control register (B2)	re2_top	0b	—
re_rs_usr_wreg_083_clk100m_reg[2]	I	—	Digital input/output control input/output control register (E0)	re2_top	0b	—
re_rs_usr_wreg_084_clk100m_reg[2]	I	—	Digital input/output control input/output control register (E1)	re2_top	0b	—
re_rs_usr_wreg_085_clk100m_reg[2]	I	—	Digital input/output control input/output control register (E2)	re2_top	0b	—
re_rs_usr_wreg_086_clk100m_reg[5:0]	I	—	Digital input/output control part digital input/output selection	re2_top	00H	—
re_rs_usr_wreg_088_clk100m_reg[0]	I	—	Digital output HOLD/CLEAR	re2_top	0b	—
re_rs_usr_wreg_1D0_clk100m_reg[0]	I	H	User circuit part error signal generation	re2_top	1b	—
IOB0_UNIT[3:0]	I	—	Module type (B0) (usr_rreg_180[3:0])	top1	0H	—
IOB1_UNIT[3:0]	I	—	Module type (B1) (usr_rreg_180[7:4])	top1	0H	—
IOB2_UNIT[3:0]	I	—	Module type (B2) (usr_rreg_180[11:8])	top1	0H	—
IOE_UNIT[4:0]	I	—	Module type (E0 to E2) (usr_rreg_181[5:0])	top1	00H	—
di_iob0_x_clk100m_reg[15:0]	I	—	Digital input signal (B0 after filtering) (usr_rreg_182[15:0])	di2_top	0000H	—
dio_iob0_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B0 after filtering) (usr_rreg_183[0])	dio2_top	0b	—
di_iob1_x_clk100m_reg[15:0]	I	—	Digital input signal (B1 after filtering) (usr_rreg_184[15:0])	di2_top	0000H	—
dio_iob1_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B1 after filtering) (usr_rreg_185[0])	dio2_top	0b	—
di_iob2_x_clk100m_reg[15:0]	I	—	Digital input signal (B2 after filtering) (usr_rreg_186[15:0])	di2_top	0000H	—
dio_iob2_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output B2 after filtering) (usr_rreg_187[0])	dio2_top	0b	—

Signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
di_ioe0_x_clk100m_reg[15:0]	I	—	Digital input signal (E0 after filtering) (usr_rreg_188[15:0])	di2_top	0000H	—
dio_ioe0_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E0 after filtering) (usr_rreg_189[0])	dio2_top	0b	—
di_ioe1_x_clk100m_reg[15:0]	I	—	Digital input signal (E1 after filtering) (usr_rreg_18A[15:0])	di2_top	0000H	—
dio_ioe1_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E1 after filtering) (usr_rreg_18B[0])	dio2_top	0b	—
di_ioe2_x_clk100m_reg[15:0]	I	—	Digital input signal (E2 after filtering) (usr_rreg_18C[15:0])	di2_top	0000H	—
dio_ioe2_dio485_i_clk100m_reg	I	—	Digital input signal (digital input/output E2 after filtering) (usr_rreg_18D[0])	dio2_top	0b	—
ai_ioe0_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E0)(usr_rreg_18F[15:0])	ai2_top	0000H	—
ai_ioe0_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E0)(usr_rreg_190[15:0])	ai2_top	0000H	—
ai_ioe0_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E0)(usr_rreg_191[15:0])	ai2_top	0000H	—
ai_ioe0_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E0)(usr_rreg_192[15:0])	ai2_top	0000H	—
ai_ioe0_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E0)(usr_rreg_193[15:0])	ai2_top	0000H	—
ai_ioe0_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E0)(usr_rreg_194[15:0])	ai2_top	0000H	—
ai_ioe0_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E0)(usr_rreg_195[15:0])	ai2_top	0000H	—
ai_ioe0_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E0)(usr_rreg_196[15:0])	ai2_top	0000H	—
ai_ioe0_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E0)(usr_rreg_197[15:0])	ai2_top	0000H	—
ai_ioe0_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E0)(usr_rreg_198[15:0])	ai2_top	0000H	—
ai_ioe0_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E0)(usr_rreg_199[15:0])	ai2_top	0000H	—
ai_ioe0_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E0)(usr_rreg_19A[15:0])	ai2_top	0000H	—
ai_ioe1_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E1)(usr_rreg_19B[15:0])	ai2_top	0000H	—
ai_ioe1_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E1)(usr_rreg_19C[15:0])	ai2_top	0000H	—
ai_ioe1_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E1)(usr_rreg_19D[15:0])	ai2_top	0000H	—
ai_ioe1_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E1)(usr_rreg_19E[15:0])	ai2_top	0000H	—
ai_ioe1_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E1)(usr_rreg_19F[15:0])	ai2_top	0000H	—
ai_ioe1_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E1)(usr_rreg_1A0[15:0])	ai2_top	0000H	—
ai_ioe1_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E1)(usr_rreg_1A1[15:0])	ai2_top	0000H	—
ai_ioe1_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E1)(usr_rreg_1A2[15:0])	ai2_top	0000H	—
ai_ioe1_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E1)(usr_rreg_1A3[15:0])	ai2_top	0000H	—
ai_ioe1_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E1)(usr_rreg_1A4[15:0])	ai2_top	0000H	—
ai_ioe1_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E1)(usr_rreg_1A5[15:0])	ai2_top	0000H	—
ai_ioe1_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E1)(usr_rreg_1A6[15:0])	ai2_top	0000H	—

Signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
ai_ioe2_aival_0_clk100m_reg[15:0]	I	—	A/D conversion value CH0 (E2)(usr_rreg_1A7[15:0])	ai2_top	0000H	—
ai_ioe2_aival_1_clk100m_reg[15:0]	I	—	A/D conversion value CH1 (E2)(usr_rreg_1A8[15:0])	ai2_top	0000H	—
ai_ioe2_aival_2_clk100m_reg[15:0]	I	—	A/D conversion value CH2 (E2)(usr_rreg_1A9[15:0])	ai2_top	0000H	—
ai_ioe2_aival_3_clk100m_reg[15:0]	I	—	A/D conversion value CH3 (E2)(usr_rreg_1AA[15:0])	ai2_top	0000H	—
ai_ioe2_aival_4_clk100m_reg[15:0]	I	—	A/D conversion value CH4 (E2)(usr_rreg_1AB[15:0])	ai2_top	0000H	—
ai_ioe2_aival_5_clk100m_reg[15:0]	I	—	A/D conversion value CH5 (E2)(usr_rreg_1AC[15:0])	ai2_top	0000H	—
ai_ioe2_aival_6_clk100m_reg[15:0]	I	—	A/D conversion value CH6 (E2)(usr_rreg_1AD[15:0])	ai2_top	0000H	—
ai_ioe2_aival_7_clk100m_reg[15:0]	I	—	A/D conversion value CH7 (E2)(usr_rreg_1AE[15:0])	ai2_top	0000H	—
ai_ioe2_aival_8_clk100m_reg[15:0]	I	—	A/D conversion value CH8 (E2)(usr_rreg_1AF[15:0])	ai2_top	0000H	—
ai_ioe2_aival_9_clk100m_reg[15:0]	I	—	A/D conversion value CH9 (E2)(usr_rreg_1B0[15:0])	ai2_top	0000H	—
ai_ioe2_aival_a_clk100m_reg[15:0]	I	—	A/D conversion value CHA (E2)(usr_rreg_1B1[15:0])	ai2_top	0000H	—
ai_ioe2_aival_b_clk100m_reg[15:0]	I	—	A/D conversion value CHB (E2)(usr_rreg_1B2[15:0])	ai2_top	0000H	—
cnt_iob0_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B0) (usr_rreg_1B3[15:0], usr_rreg_1B4[15:0])	Counter control part	0000_0000H	—
cnt_iob1_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B1) (usr_rreg_1B5[15:0], usr_rreg_1B6[15:0])	Counter control part	0000_0000H	—
cnt_iob2_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (B2) (usr_rreg_1B7[15:0], usr_rreg_1B8[15:0])	Counter control part	0000_0000H	—
cnt_ioe0_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E0) (usr_rreg_1B9[15:0], usr_rreg_1BA[15:0])	Counter control part	0000_0000H	—
cnt_ioe1_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E1) (usr_rreg_1BB[15:0], usr_rreg_1BC[15:0])	Counter control part	0000_0000H	—
cnt_ioe2_32ring_2pha4multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (2-phase multiple of 4) counter value (E2) (usr_rreg_1BD[15:0], usr_rreg_1BE[15:0])	Counter control part	0000_0000H	—
cnt_iob0_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (B0) (usr_rreg_1BF[15:0], usr_rreg_1C0[15:0])	Counter control part	0000_0000H	—
cnt_iob1_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (B1) (usr_rreg_1C1[15:0], usr_rreg_1C2[15:0])	Counter control part	0000_0000H	—
cnt_iob2_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (B2) (usr_rreg_1C3[15:0], usr_rreg_1C4[15:0])	Counter control part	0000_0000H	—
cnt_ioe0_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (E0) (usr_rreg_1C5[15:0], usr_rreg_1C6[15:0])	Counter control part	0000_0000H	—
cnt_ioe1_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (E1) (usr_rreg_1C7[15:0], usr_rreg_1C8[15:0])	Counter control part	0000_0000H	—
cnt_ioe2_32ring_1pha1multi_counter_clk100m_reg[31:0]	I	—	32-bit ring counter (1-phase multiple of 1) counter value (E2) (usr_rreg_1C9[15:0], usr_rreg_1CA[15:0])	Counter control part	0000_0000H	—
pls_iob0_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (B0) (usr_rreg_1CB[15:0], usr_rreg_1CC[15:0])	Pulse output part	0000_0000H	—

Signal name	I/O	Logic	Description	Connection destination	Initial value	Pulse signal
pls_iob1_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (B1) (usr_rreg_1CD[15:0], usr_rreg_1CE[15:0])	Pulse output part	0000_0000H	—
pls_iob2_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (B2) (usr_rreg_1CF[15:0], usr_rreg_1D0[15:0])	Pulse output part	0000_0000H	—
pls_ioe0_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (E0) (usr_rreg_1D1[15:0], usr_rreg_1D2[15:0])	Pulse output part	0000_0000H	—
pls_ioe1_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (E1) (usr_rreg_1D3[15:0], usr_rreg_1D4[15:0])	Pulse output part	0000_0000H	—
pls_ioe2_plscnt_clk100m_reg[31:0]	I	—	Number of pulse outputs (E2) (usr_rreg_1D5[15:0], usr_rreg_1D6[15:0])	Pulse output part	0000_0000H	—
re_rs_usr_wreg_000_clk100m_reg[15:0] to re_rs_usr_wreg_1ff_clk100m_reg[15:0]	I	—	Writing data	re2_top	0000H each	—
re_rs_usr_alwreg_00_clk100m_reg[15:0] to re_rs_usr_alwreg_0f_clk100m_reg[15:0]	I	—	Always write register	re2_top	0000H each	—
ai_ioe0_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E0)	ai2_top	0b	1shot@clk100m
ai_ioe1_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E1)	ai2_top	0b	1shot@clk100m
ai_ioe2_aival_vald_clk100m_reg	I	H	A/D conversion value enable (E2)	ai2_top	0b	1shot@clk100m
re_rs_usr_rreg_000_clk100m_reg[15:0] to re_rs_usr_rreg_1ff_clk100m_reg[15:0]	O	—	Read data	re2_top	0000H each	—
re_rs_usr_alrreg_00_clk100m_reg[15:0] to re_rs_usr_alrreg_0f_clk100m_reg[15:0]	O	—	Always read register	re2_top	0000H each	—
uc_err_clk100m_reg	O	—	User circuit error signal	re2_top	0b	—
uc_iob0_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output B0)	dio2_top	0b	—
uc_iob1_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output B1)	dio2_top	0b	—
uc_iob2_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output B2)	dio2_top	0b	—
uc_ioe0_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output E0)	dio2_top	0b	—
uc_ioe1_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output E1)	dio2_top	0b	—
uc_ioe2_dio485_y_clk100m_reg	O	—	Digital output signal (digital input/output E2)	dio2_top	0b	—
uc_iob0_dio485_en_clk100m_reg	O	—	Digital input/output control signal (B0)	dio2_top	0b	—
uc_iob1_dio485_en_clk100m_reg	O	—	Digital input/output control signal (B1)	dio2_top	0b	—
uc_iob2_dio485_en_clk100m_reg	O	—	Digital input/output control signal (B2)	dio2_top	0b	—
uc_ioe0_dio485_en_clk100m_reg	O	—	Digital input/output control signal (E0)	dio2_top	0b	—
uc_ioe1_dio485_en_clk100m_reg	O	—	Digital input/output control signal (E1)	dio2_top	0b	—
uc_ioe2_dio485_en_clk100m_reg	O	—	Digital input/output control signal (E2)	dio2_top	0b	—
cpu_intpl_out[2:0]	O	—	General-purpose output	top1	0b	—
uc_sampling_tmgpulse_clk100m_1shot_reg[5:0]	O	—	User circuit data sampling pulse	ai2_top	0b	1shot@clk100m
logctrl_uperr	I	H	Logging control violation flag rising edge	Logging control part	0b	—
logctrl_downerr	I	H	Logging control violation flag falling edge	Logging control part	0b	—
rst_n	I	L	Reset	rc2_top	1b	—
uc_iob0_y_clk100m_reg[15:0]	O	—	Digital output signal (B0)	do2_top	0000H	—
uc_iob1_y_clk100m_reg[15:0]	O	—	Digital output signal (B1)	do2_top	0000H	—
uc_iob2_y_clk100m_reg[15:0]	O	—	Digital output signal (B2)	do2_top	0000H	—
uc_ioe0_y_clk100m_reg[15:0]	O	—	Digital output signal (E0)	do2_top	0000H	—
uc_ioe1_y_clk100m_reg[15:0]	O	—	Digital output signal (E1)	do2_top	0000H	—
uc_ioe2_y_clk100m_reg[15:0]	O	—	Digital output signal (E2)	do2_top	0000H	—

■A/D conversion value maximum/minimum hold

Holds the maximum and minimum values of A/D conversion values input from the extension module (E0, E1, E2). The maximum initial value is set to 8000H and the minimum initial value is set to 7FFFH, and when "A/D conversion value enable" is set to Enable (1), they are compared with the A/D conversion value and held.

A/D conversion value maximum/minimum: By enabling the update of current values, the maximum and minimum values are updated to the current A/D conversion value. The comparison and held results are connected to the read data. The truth table for the maximum and minimum values of A/D conversion value maximum/minimum hold is shown below.

• Truth table for holding maximum A/D conversion value

Ex.

Described in CH0 of E0. CH1 to CHB of E0 and CH0 to CHB of E1 and E2 have the same function.

usr_rst_n	clk100m	re_rs_usr_wreg_1d9_clk100m_reg	ai_ioe0_aival_vald_clk100m_reg	ai_ioe0_aival_0_max_clk100m_reg
0b (enable)	X	—	X	8000H
1b (disable)	↑	0b (enable)	—	ai_ioe0_aival_0_clk100m_reg
1b	↑	1b (disable)	ai_ioe0_aival_0_clk100m_reg>ai_ioe0_aival_0_max_clk100m_reg	ai_ioe0_aival_0_clk100m_reg
1b	↑	0b	ai_ioe0_aival_0_clk100m_reg≤ai_ioe0_aival_0_max_clk100m_reg	ai_ioe0_aival_0_max_clk100m_reg

• Truth table for maintaining minimum A/D conversion value

Ex.

Described in CH0 of E0. CH1 to CHB of E0 and CH0 to CHB of E1 and E2 have the same function.

usr_rst_n	clk100m	re_rs_usr_wreg_1d9_clk100m_reg	ai_ioe0_aival_vald_clk100m_reg	ai_ioe0_aival_0_min_clk100m_reg
0b (enable)	X	—	X	7FFFH
1b (disable)	↑	1b (enable)	—	ai_ioe0_aival_0_clk100m_reg
1b	↑	0b (disable)	ai_ioe0_aival_0_clk100m_reg<ai_ioe0_aival_0_min_clk100m_reg	ai_ioe0_aival_0_clk100m_reg
1b	↑	0b	ai_ioe0_aival_0_clk100m_reg≥ai_ioe0_aival_0_min_clk100m_reg	ai_ioe0_aival_0_min_clk100m_reg

The maximum and minimum analog values are displayed in the register for each circuit board according to the "Analog control A/D conversion value maximum/minimum selection" setting. The circuit board to select is shown below.

re_rs_usr_wreg_1d8_clk100m_reg	ai_ioe_aival_0_max to ai_ioe_aival_b_max	ai_ioe_aival_0_min to ai_ioe_aival_b_min
00b	ai_ioe0_aival_0_max_clk100m_reg to ai_ioe0_aival_b_max_clk100m_reg	ai_ioe0_aival_0_min_clk100m_reg to ai_ioe0_aival_b_min_clk100m_reg
01b	ai_ioe1_aival_0_max_clk100m_reg to ai_ioe1_aival_b_max_clk100m_reg	ai_ioe1_aival_0_min_clk100m_reg to ai_ioe1_aival_b_min_clk100m_reg
10b	ai_ioe2_aival_0_max_clk100m_reg to ai_ioe2_aival_b_max_clk100m_reg	ai_ioe2_aival_0_min_clk100m_reg to ai_ioe2_aival_b_min_clk100m_reg
11b	ai_ioe0_aival_0_max_clk100m_reg to ai_ioe0_aival_b_max_clk100m_reg	ai_ioe0_aival_0_min_clk100m_reg to ai_ioe0_aival_b_min_clk100m_reg

■A/D conversion value enable status

Implements a flip-flop that sets the extension module (E0, E1, E2) when A/D conversion value is enabled, and resets it when "Internal operation start/stop" is set to Stop (1). The set/reset signal is connected to the read data. The A/D conversion value enable status truth table is shown below.

usr_rst_n	clk100m	ai_ioe0_aival_vald_clk100m_reg	ai_ioe1_aival_vald_clk100m_reg	ai_ioe2_aival_vald_clk100m_reg	usr_rreg_18e_clk100m_reg		
					[0]	[1]	[2]
0b (enable)	X	X	X	X	0b	0b	0b
1b (disable)	↑	1b (enable)	X	X	1b	Previous value held	Previous value held
1b	↑	X	1b (enable)	X	Previous value held	1b	Previous value held
1b	↑	X	X	1b (enable)	Previous value held	Previous value held	1b

■Digital output control

Selects and outputs the digital output signal after digital control and output signal of the pulse output part. Also, HOLD/CLEAR is executed when "Microcomputer system error notification" is set to Enable (1), depending on the setting value of "Digital output HOLD/CLEAR". The truth table for digital output control is shown below.

usr_rst_n	clk100m	Digital output HOLD/ CLEAR	MCU system error notification	Digital input/output control Digital output selection (B0)[0]	uc_iob0_y_clk100m_reg[0]*1
0b (enable)	X	X	X	X	0b
1b (disable)	↑	0b(CLEAR)	0b (disable)	0b	dig_iob0_y_clk100m_reg[0]
1b	↑	0b	0b	1b	pls_iob0_y_dio485_clk100m_reg
1b	↑	0b	1b (enable)	0b	0b
1b	↑	0b	1b	1b	0b
1b	↑	1b(HOLD)	0b	0b	dig_iob0_y_clk100m_reg[0]
1b	↑	1b	0b	1b	pls_iob0_y_dio485_clk100m_reg
1b	↑	1b	1b	0b	Previous value held
1b	↑	1b	1b	1b	Previous value held

*1 Described in CH0 of B0. CH1 to CHF of B0, CH0 to CHF of B1/B2, and CH0 to CHF of E0/E1/E2 have the same structure.

■User circuit data sampling pulse

Outputs the signal (uc_sampling_tmgpulse_clk100m_1shot_reg) that has detected the rising edge of "Analog control data sampling pulse generation", to the analog input control part.

■Read data output

Read data (re_rs_usr_rreg_000_clk100m_reg[15: 0] to re_rs_usr_rreg_1FF_clk100m_reg[15: 0]) changes the connection according to the setting (Test mode enabled (1), Test mode disabled (0)) of the Test mode setting register (re_rs_usr_wreg_17f_clk100m_reg[0]). Connections when test mode is enabled and disabled are shown below.

• When test mode is enabled

Connects Write data (transient area) (usr_wreg_000 to usr_wreg_17F) (FPGA register address: 1000_B000H to 1000_B2FFH) to Read data (transient area) (usr_rreg_000 to usr_rreg_17F) (FPGA register address: 1000_B800H to 1000_BAFFH).

Connects Write data (cyclic area) (usr_wreg_180 to usr_wreg_1FF) (FPGA register address: 1000_B300H to 1000_B3FFH) to Read data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) (FPGA register address: 1000_BB00H to 1000_BBFFH).

• When test mode is disabled

Connects Write data (transient area) (usr_wreg_000 to usr_wreg_17F) (FPGA register address: 1000_B000H to 1000_B2FFH) to Read data (transient area) (usr_rreg_000 to usr_rreg_17F) (FPGA register address: 1000_B800H to 1000_BAFFH).

Connects the status of the user circuit part to Read data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) (FPGA register address: 1000_BB00H to 1000_BBFFH). For details, refer to the following.

Connects the status of the user circuit block to Read data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) (FPGA register address: 1000_BB00H to 1000_BBFFH). For details, refer to the following.

☞ Page 563 Write data

☞ Page 563 Read Data

■Always read register

Connects "Always write register (1000_A010h to 1000_A02Fh)" to "Always read register (1000_A030h to 1000_A04Fh)". However, the following register areas are connected to logging control violation rising/falling edge (logctrl_uperr/ logctrl_downerr).

• Always read register 14[0]: logctrl_uperr

• Always read register 14[1]: logctrl_downerr

■User circuit error signal

Outputs the signal (uc_err_clk100m_reg) that has detected the rising edge of "User circuit part error signal generation" to the register part.

■General-purpose output

Outputs the general-purpose input (cpu_intpl_in) to the general-purpose output (cpu_intpl_out) in one flip-flop level (clk100m).

Notes and restrictions for the sample circuit

■Safety circuit

Provide a safety circuit that operates on the safe side according to the error cause of your system.

In the sample circuit, the MCU system error notification (usr_micon_syserr) (FPGA register address: 1000_A004H) has an error (1) and implements a HOLD/CLEAR circuit that holds (holding the previous value) or clears (0 fixed output) the output.

Modify the safety circuit according to your system.

For circuit details, refer to the following.

- ☞ Page 288 Output block part (uc3_msc_top)
- ☞ Page 266 Analog output block (uc3_ao_top)

■When using the time division mode of the logging control part

The following table shows the notes and restrictions on using the time division mode of the logging control part. If the notes and restrictions are not followed, it will not work properly.

Notes and restrictions	Remarks
Set the FPGA register areas as follows. ■Logging operation control register (lgdw_ctrl) (FPGA register: 1000_9000H)*1 • b8: Trigger operation mode (1) • b12: User circuit output (0) (logging start selection) • b13: User circuit output (1) (sampling pulse selection) ■Set number of sampling after trigger (lower) (lgdw_triggered_lsample) (FPGA register: 1001_9000H), Set number of sampling after trigger (upper) (lgdw_triggered_usample) (FPGA register: 1001_9002H)*1 • Multiples of 2 (multiples of the number of divisions) ■User circuit logging mode selection (usr_logmode_sel) (FPGA register address: 1000_A002H) • Time division enabled (1) ■Logging control part: Sampling pulse signal selection (usr_wreg_093) (FPGA register address: 1000_B126H) • A/D conversion value enable (E0)(15H) to A/D conversion value enable (E2)(17H)	Logging may not be performed normally. Example: Only logging data lower side [432:0] is logged.
Logging control part: For the signal selected at logging enable signal selection (usr_wreg_091)(FPGA register address: 1000_B122H), input it with a pulse width greater than the setting value of the data sampling timing (E□) (FPGA register address: 1000_2108H, 1000_210AH, 1000_210CH).*2	The logging enable signal may not be output to the logging part.
Logging control part: For the signal selected at end trigger signal selection (usr_wreg_092) (FPGA register address: 1000_B124H), input it with a pulse with of 3μs or more.	The logging end trigger may not be output to the logging part.
Enable (1) the logging end trigger after logging enable is enabled (1).	The logging end trigger may not be recognized by the logging part.
After logging enable is enabled (1), do not set the logging end trigger to Enable (1) within 3μs.	The logging end trigger may not be recognized by the logging part.

*1 Logging operation control register (lgdw_ctrl) (FPGA register: 1000_9000H) b8 can be used in modes other than the trigger operation mode (1). In cases other than Trigger operation mode (1), it is unnecessary to set Set number of sampling after trigger (lower wide) (lgdw_triggered_lsample) (FPGA register: 1001_9000H) and Set number of sampling after trigger (upper side) (lgdw_triggered_usample) (FPGA register: 1001_9002H).

*2 Logging control part: Sampling pulse signal selection (usr_wreg_093) (FPGA register address: 1000_B126H). Depending on its settings, the corresponding data sampling timing (E□) (FPGA register address: 1000_2108H, 1000_210AH, 1000_210CH) are different.
Logging control part: Sampling pulse signal selection (usr_wreg_093) (FPGA register address: 1000_B126H) setting value is handled as shown below.
· 15H: Setting the data sampling timing (E0)
· 16H: Setting the data sampling timing (E1)
· 17H: Setting the data sampling timing (E2)

PART 6 FUNCTIONS

This part consists of the following chapter.

12 FUNCTIONS

This chapter describes the details of the functions that can be used in the FPGA module and how to set them.

12.1 Function List

The following table lists the functions of the FPGA module.

Item	Description	Reference
FPGA download function	Writes the created configuration data to the configuration ROM inside the FPGA module.	Page 300 FPGA Download Function
FPGA configuration function	The FPGA module performs FPGA configuration when: • Upon power-on or remote reset • During FPGA download	Page 311 FPGA Configuration Function
FPGA control function	The FPGA standard circuit and user circuits can be started or stopped.	Page 315 FPGA Control Function
FPGA register access function	Reads from and writes to the FPGA register areas from the master station program.	Page 321 FPGA Register Access Function
Logging function	The logging part of the FPGA acquires the external input/output from the user circuit, count values, and other sources at the timing of when the sampling pulse is input, and writes them to DDR3L SDRAM.	Page 327 Logging Function
FTP client function	Transfers logging data collected in DDR3L SDRAM to the FTP server.	Page 340 FTP Client Function
SLMP communication function	SLMP can be used to communicate with the FPGA module.	Page 351 SLMP Communication Function
CC-Link IE TSN network synchronous communication function	Reads and writes to the FPGA at the synchronous cycle of a master station that supports the CC-Link IE TSN network synchronous communication function.	Page 353 CC-Link IE TSN Network Synchronous Communication Function
Module power supply voltage drop detection function	This function detects a voltage drop of the module power supply.	Page 360 Module Power Supply Voltage Drop Detection Function
Firmware update function	Updates the FPGA module firmware via CC-Link IE TSN.	Page 361 Firmware Update Function

12.2 Operation Mode Shift at Power-On

The FPGA module enters one of the following operation modes when the power is turned on.

- CC-Link IE TSN communication mode
- CC-Link IE TSN synchronous communication mode
- Standalone mode
- Standalone mode (IP address initialization)
- Unit test mode

CC-Link IE TSN communication mode

The module operates as a remote station for CC-Link IE TSN communication in this mode.

The module switches to CC-Link IE TSN communication mode if any of the following conditions are met.

- The function setting switch 1 is set to OFF, and "Network Synchronous Communication" is set to "Asynchronous".
- The function setting switch 1 is set to OFF, and the module is connected to the master station whose inter-module synchronous communication is not set with this module.

CC-Link IE TSN synchronous communication mode

The module operates as a remote station for CC-Link IE TSN communication in synchronization with the synchronization cycle of the master station in this mode.

If all of the following conditions are met, the CC-Link IE TSN synchronous communication mode is entered.

- Function setting switch 1 is OFF.
- Function setting switch 2 is OFF.
- "Network Synchronous Communication" is set to "Synchronous".
- The module is connected to the master station whose inter-module synchronous communication is set with this module.

Standalone mode

The module operates independently according to the parameters set by the FPGA module configuration tool and operates according to SLMP commands sent from SLMP compatible devices.

If all of the following conditions are met, it will switch to standalone mode.

- Function setting switch 1 is ON.
- Function setting switch 2 is OFF.

Standalone mode (IP address initialization)

This mode is for initializing the IP address and subnet mask saved in the non-volatile memory of the FPGA module.

If all of the following conditions are met, the module switches to standalone mode (IP address initialization).

- IP address/station number setting switch (x1): F
- IP address/station number setting switch (x16): F
- Function setting switch 1 is ON.
- Function setting switch 2 is ON.

Unit test mode

This mode checks if there is an abnormality in the hardware of the FPGA module.

If all the following conditions are met, the unit test mode is entered.

- IP address/station number setting switch: other than 255
- Function setting switch 1 is ON.
- Function setting switch 2 is ON.

12.3 FPGA Download Function

Writes the created configuration data to the FPGA module.

There are two writing methods, as follows.

- How to write via JTAG (☞ Page 302 How to write via JTAG)
- How to write via Ethernet (☞ Page 305 How to write via Ethernet)

Configuration data

Configuration data created in advance with FPGA design software is required to perform an FPGA download.

The file format of the configuration data differs depending on the download method. (☞ Page 302 How to write via JTAG, ☞ Page 305 How to write via Ethernet) For how to create configuration data, refer to the following.

☞ Page 140 FPGA Development Procedures

For the procedure for converting from SOF format to JIC format or RPD format, refer to the following.

☞ Page 309 Procedure for conversion from SOF format to JIC format and RPD format

Design security

FPGAs have a design security function as a means of enhancing security.

The design security function encrypts the data using any desired key when generating configuration data.

During configuration when the power is turned on, the configuration data encrypted by the decryption key (AES key) already written to the FPGA is decrypted and configured.

Point

For instructions on how to use the Convert Programming File that comes with the FPGA design software, please contact the Intel® company.

Operation

■LED status

The status of the FPGA download can be checked by viewing the LED of the FPGA module.

Status of FPGA module		FPGA CONF. LED	ERR.LED
Normal operation		On	Off
During FPGA download		Flashing*1	Off*2
FPGA download completed	FPGA configuration completed successfully	On	Off
	FPGA configuration completed with an error	Off*3	On

*1 After the FPGA CONF. LED starts flashing due to the download operation, even if the writing is interrupted, such as when the cable has been disconnected, the FPGA CONF. LED will continue flashing. Even while in the flashing state, the download operation can be repeated using the FPGA design software or FPGA Module Configuration Tool.

*2 If an error is detected in accessing the configuration ROM during an FPGA download via Ethernet, the ERR.LED lights up. At this time, a configuration ROM access error (error code: 3A20H) will occur.

*3 If the FPGA download method uses the configuration ROM as the write destination, the FPGA module performs FPGA configuration after the writing to the configuration ROM is completed. If an error occurs in the FPGA configuration, the FPGA CONF. LED turns off. At this time, an FPGA configuration error (error code: 3C01H) occurs and the ERR.LED lights up.

■Remote input signals

When the FPGA download starts and the FPGA CONF. LED starts flashing, remote READY (RXB) turns off.

Remote READY (RXB) turns ON when the FPGA configuration is complete.

Error information

If writing is interrupted due to cable disconnection during FPGA download, check for messages on the windows of the FPGA design software and FPGA module configuration tool, and the communication environment, such as the cable connection status, and then perform the writing operation again.

Precautions

- Be sure to turn off the power to the FPGA module before connecting the JTAG cable. If connected while the power is ON, it may cause malfunction or failure.
- Write via JTAG in an environment that is not affected by noise. Using it in an environment affected by noise may cause malfunction or failure.
- When downloading configuration data in JIC format or RPD format, the total number of downloads should be 100000 or fewer.
- Do not execute FPGA download via JTAG and FPGA download via Ethernet at the same time.
- In CC-Link IE TSN communication mode, an FPGA module that has never been data linked with the master station operates with the default IP address and subnet mask. Note that this is different from the IP address (1st to 3rd octets) and subnet mask of the master station, so be careful when setting the connection destination with the FPGA module configuration tool. (☞ Page 54 IP address/station number setting switch setting)
- For safety reasons, before starting an FPGA download, assure that the FPGA module is stopped under FPGA control, the power supply of the external I/O connection partner device is turned off, and the Ethernet connection partner device is stopped from accessing the FPGA module via SLMP communication.

How to write via JTAG

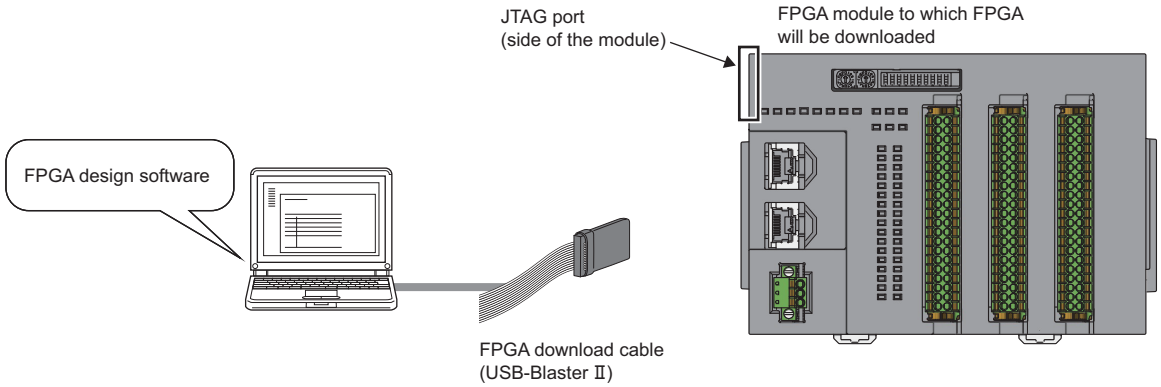
In this method, the personal computer and the FPGA module are connected one-to-one with the FPGA download cable, and the configuration data is written to the FPGA module via JTAG. Use JIC format or SOF format files as configuration data.

Application	Software used	File format	Data retention when power is turned off	Write destination	Recommended environment	Remarks
For development	FPGA development software	JIC	Yes	Configuration ROM	A noise-free environment (such as desktop)	Data can be retained even after power-off.
		SOF	No	FPGA		• Data is lost after power-off. • Debug function of FPGA design software can be used.

Point

- Some FPGA design software functions download and use SOF format configuration data. For details, refer to the FPGA design software manual.
- Writing via JTAG has restrictions on the usage environment. Use it in an environment free from noise, such as for desktop verification during user circuit development.

System configuration



Procedure for FPGA download

The following describes the procedure to write configuration data via JTAG.

Operating procedure

1. Prepare configuration data.

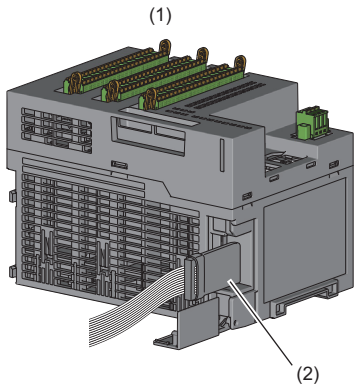
Prepare configuration data of .jic files or .sof files.

For how to convert .sof files to .jic files, refer to the following.

☞ Page 309 Procedure for conversion from SOF format to JIC format and RPD format

2. Connect an FPGA download cable.

Connect an FPGA download cable while the power supply of the FPGA module is off.



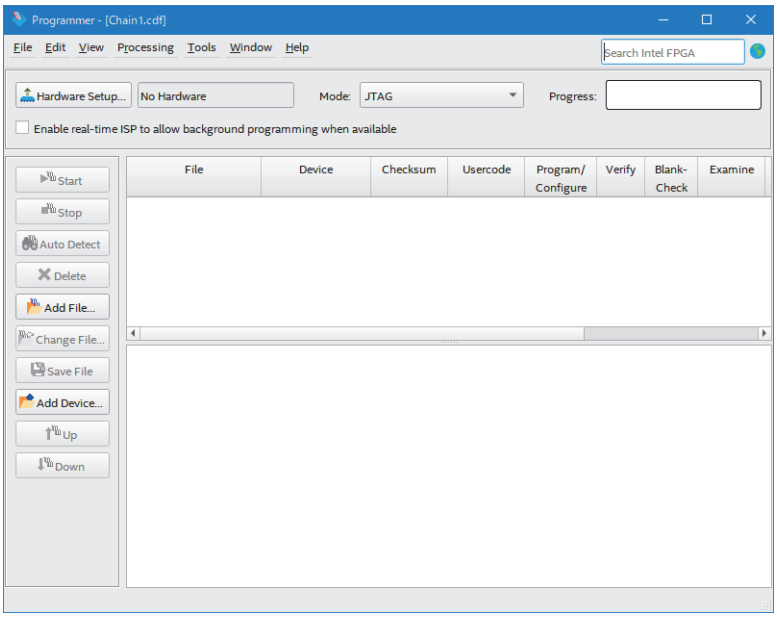
(1) FPGA module
(2) FPGA download cable

3. Turn on the function setting switch 5.

4. Power on the FPGA module.

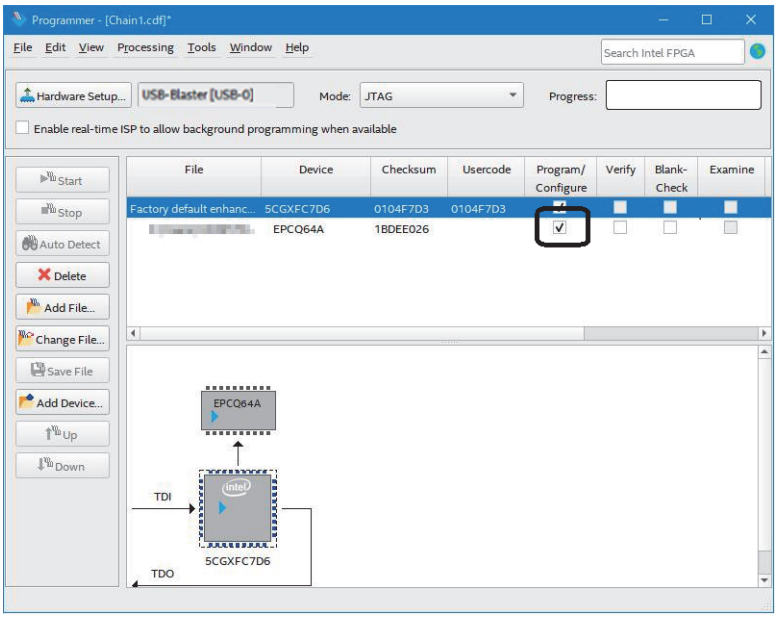
5. Display the "Programmer" window on FPGA development software and set items as follows.

[Tools] ⇨ [Programmer]



Item	Value or file to be set	Description
Hardware Setup	USB-BlasterⅡ	Download cable to be used
Mode	JTAG	Mode used for writing
Add File	Created JIC file (FPGA_test.jic)	JIC file to be written

6. Select the checkbox as shown below and click the [Start] button.



7. The download is complete.

When the download has been completed, the FPGA module performs the FPGA configuration. (☞ Page 312 Configuration)

8. Turn off the function setting switch 5 and restart the error detection for FPGA.

9. When FPGA control automatic start setting is set to Disable, turn on FPGA control start request (RY0) to start FPGA control.

Precautions

- Connect the FPGA download cable to the JTAG port while the power supply of the FPGA module is off. Connecting or removing the FPGA download cable while the FPGA module is powered on may cause malfunction or failure due to noise or static electricity.
- Perform the download from FPGA development software while the function setting switch 5 is on. Downloading the file while the function setting switch 5 is off causes an FPGA configuration error (error code: 3C01H).
- Be sure to turn off the function setting switch 5 after the completion of the download. When the FPGA module is used while the function setting switch 5 remains on, a hardware failure that occurs in the FPGA cannot be detected.

How to write via Ethernet

In this method configuration data from the FPGA module configuration tool is written to the configuration ROM via Ethernet. By connecting a personal computer to an available port on the same network as the FPGA module, downloading can be performed to any FPGA module connected to the same network.

Application	Software used	File format	Data retention when power is turned off	Write destination	Recommended environment	Remarks
Mass production	FPGA Module Configuration Tool	RPD	Available	Configuration ROM	A noise-free environment (such as on a desk) and inside a control panel	• Data can be retained even after power-off. • It is possible to write to multiple FPGA modules on the same network simply by changing the IP address setting without changing the connection cable of the personal computer.

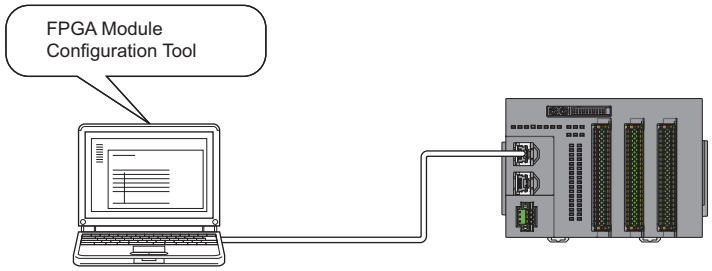
Point

Concerning the FPGA Module Configuration Tool, refer to the following.

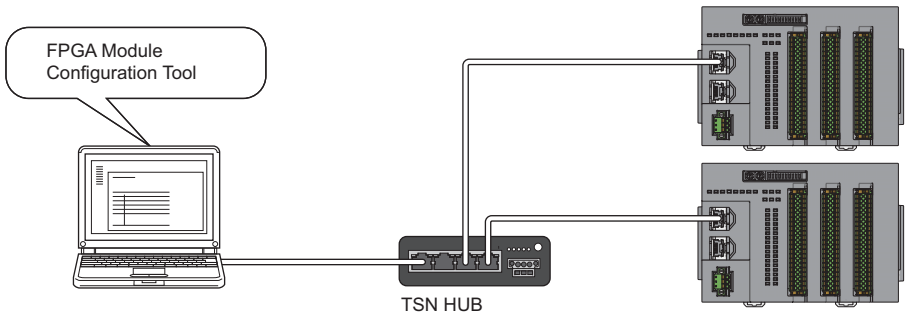
☞ Page 86 FPGA MODULE CONFIGURATION TOOL

System configuration

■For direct connection



■For star connection with TSN hub



Procedure for FPGA download

The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Prepare configuration data.

Create RPD format files from SOF format files.

For how to convert SOF format files to RPD format files, refer to the following.

☞ Page 309 Procedure for conversion from SOF format to JIC format and RPD format

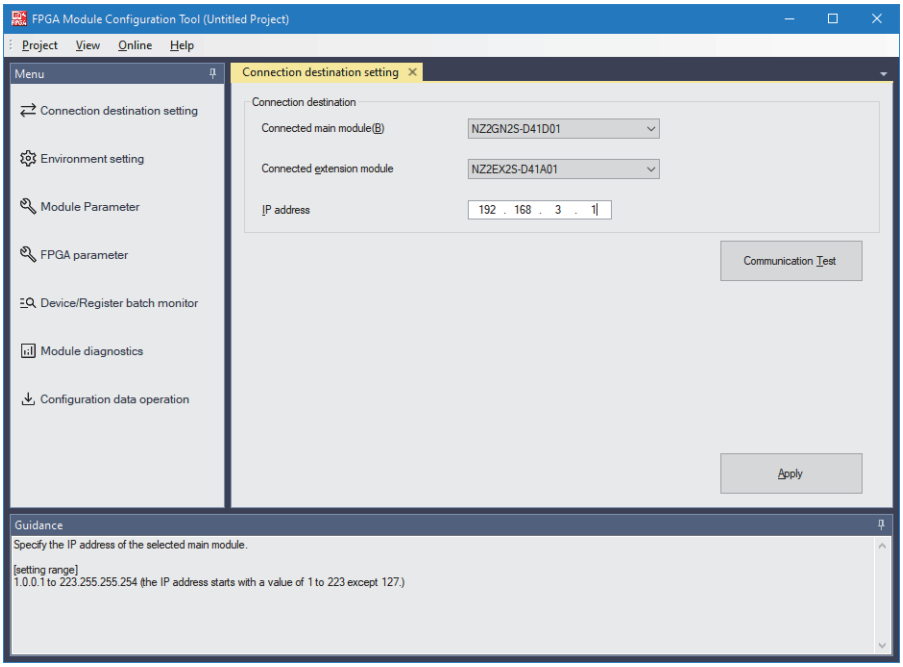
2. Connect to the network with an Ethernet cable.

Connect the computer on which the FPGA Module Configuration Tool is installed to the network with an Ethernet cable.

3. Download the configuration data from the FPGA Module Configuration Tool.

4. Set the IP address of the FPGA module in "Connection destination setting".

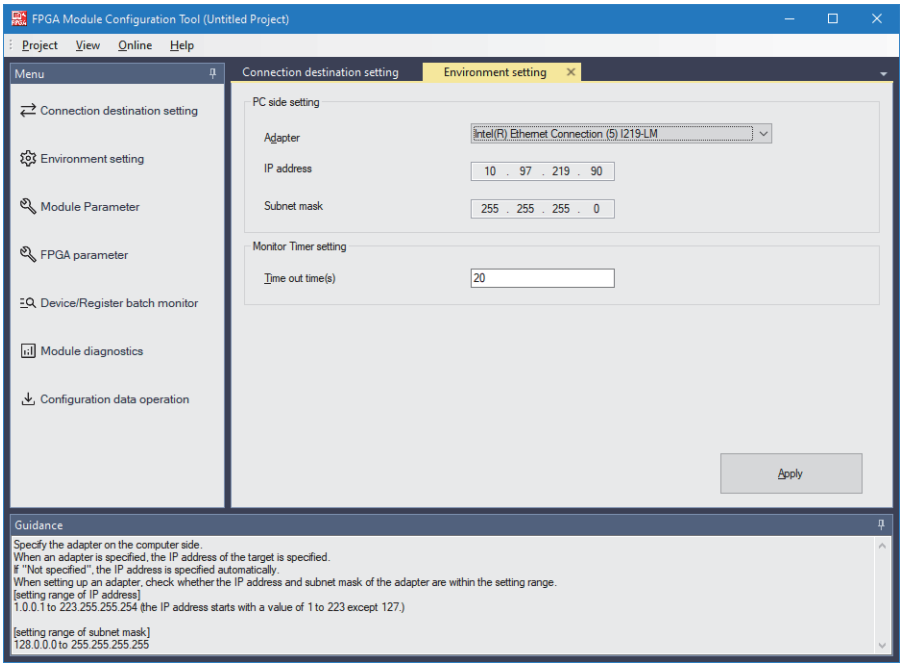
[Menu] ⇨ [Connection destination setting]



5. Click the [Apply] button.

6. In "Environment setting", set "PC side setting" and "Monitor Timer setting".

[Menu] ⇨ [Environment setting]

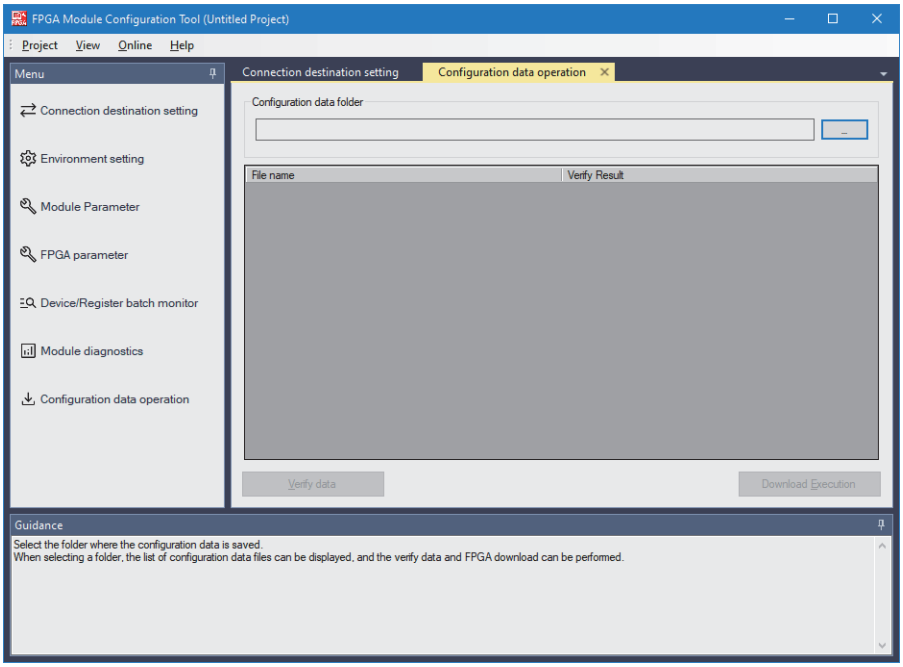


Item		Description
PC side setting	Adapter	Select the adapter on the personal computer side that is connected to the FPGA module.
	IP address	When an adapter is selected, the IP address of the target adapter is automatically input. If the adapter is "Not Specified", it will be blank.
	Subnet mask	When an adapter is selected, the subnet mask of the target adapter is automatically input. If the adapter is "Not Specified", it will be blank.
Monitor Timer setting	Time out time(s)	Set the time out time for SLMP communication and FTP communication.

7. Click the [Apply] button.

8. Select the configuration data and download it to the FPGA module.

[Menu] ⇨ [Configuration data operation]



9. Select the folder in which the configuration data is saved.

10. Click the [Download Execution] button.

When the download has been completed successfully, the FPGA module performs the FPGA configuration.

After FPGA configuration, it will enter one of the following states depending on the setting for "FPGA control automatic start setting".

- If "Enable": FPGA control is started.
- If "Disable": FPGA control remains stopped.

For details on FPGA configuration, refer to the following.

☞ Page 311 FPGA Configuration Function

11. To prohibit writing configuration data via Ethernet after starting FPGA control, set function setting switch 4 to on.

12. When the FPGA control automatic start setting is set to "Disable", turn off and on FPGA control start request (RY0) to start FPGA control.

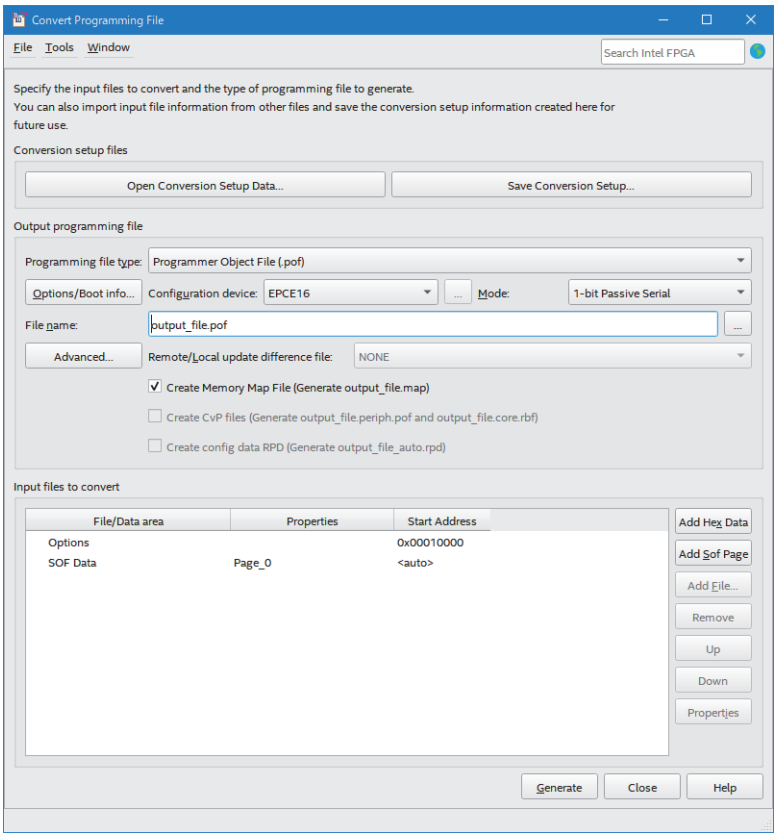
Procedure for conversion from SOF format to JIC format and RPD format

The following describes the procedure to convert the file format from SOF format to JIC format and RPD format.

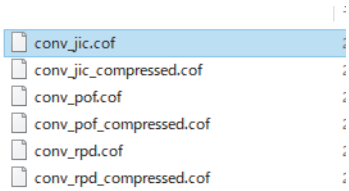
Operating procedure

1. Start FPGA development software.
2. Open the "Convert Programming File" window.

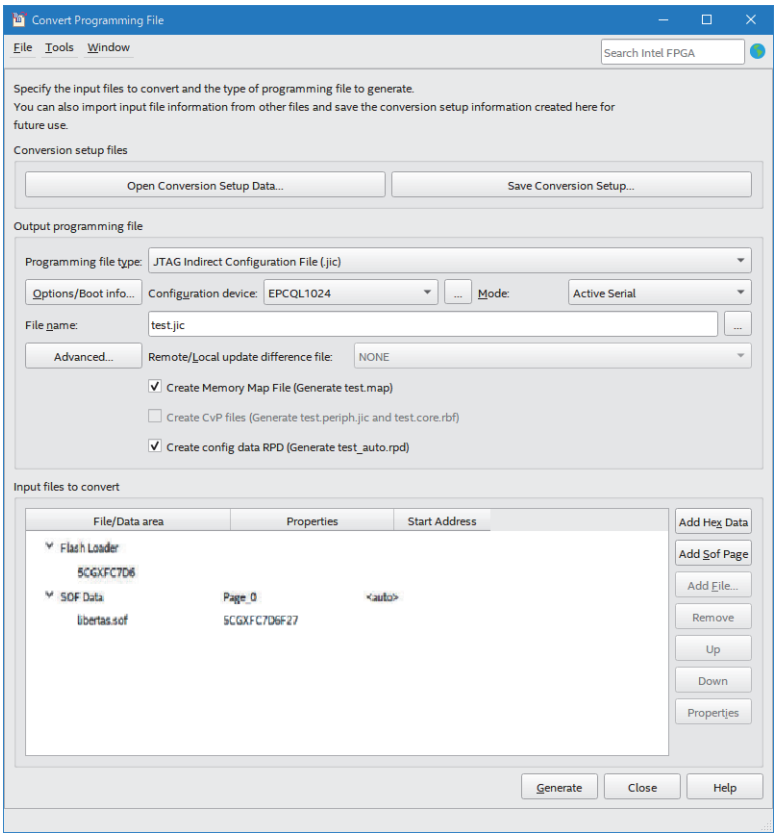
[File] ⇨ [Convert Programming Files]



3. Click the [Open Conversion Setup Data] button.
4. Select conv_jic.cof from the Conversion Setup Files (COF file) provided with the FPGA development environment for the CC-Link IE TSN FPGA module.



5. The device of the FPGA is input. Change the file name of JIC format file if necessary.



6. Click the [Generate] button.

7. A JIC format file and an RPD format file are generated in the 10_layout folder.

12.4 FPGA Configuration Function

The FPGA module performs FPGA configuration when:

❶ Upon power-on or remote reset

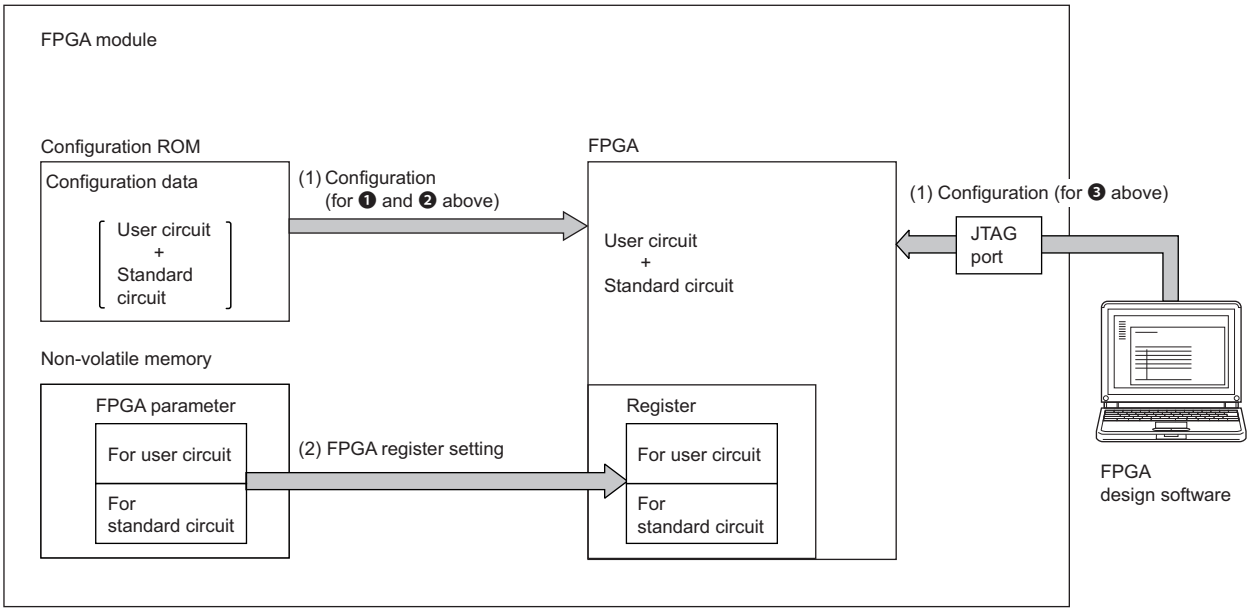
❷ At the time of FPGA download (configuration data file is JIC format, RPD format)

❸ At the time of FPGA download (configuration data file is SOF format)

For ❶❷, configuration is performed using the configuration data saved in the configuration ROM inside the FPGA module.

For ❸, configuration takes place using the data downloaded from the FPGA design software.

In addition, the FPGA module has FPGA parameters that change the operation of each block in the FPGA, and after configuration is completed, the FPGA parameters saved in the nonvolatile memory are set to the FPGA register areas.



Order of execution
(1) Order 1
(2) Order 2

Setting method

■Configuration data

Write from FPGA design software or FPGA Module Configuration Tool using the FPGA download function. (☞ Page 300 FPGA Download Function)

■FPGA parameter

FPGA parameters can be set from the FPGA Module Configuration Tool, the structure of which is described below.

- Parameters for register areas in the standard circuit part
- Parameters for user circuit part register areas

When writing to the FPGA module, if "Parameter write (Memory + Non-volatile memory)" is selected as the write destination, the data will be saved in the non-volatile memory of the FPGA module and retained even after the power is turned off. For details on the write operation, refer to the following.

☞ Page 116 Parameter writing

In addition, FPGA parameters can be set from a program and written to non-volatile memory. For details on FPGA parameters, refer to the following.

☞ Page 314 FPGA parameter

■User circuit part parameter size

The Writing data (transient area) of the FPGA register in the user circuit part can be saved in non-volatile memory as FPGA parameters from the start address to the size specified in the "User circuit part parameter size". After FPGA configuration is complete, parameters of a size equivalent to that saved in non-volatile memory are set to Writing data (transient area) (FPGA register address: 1000_B000H to 1000_B2FFH).

Item	Setting range
User circuit part parameter size	0 to 384 (Default: 0)

Point

With settings from 385 to 65535, it works as 384.

For User circuit part parameter size, the set values for the following operations are valid.

- When writing from the FPGA Module Configuration Tool
- When writing by FPGA parameter save request (RY2)

Configuration

The FPGA module transfers the configuration data saved in the configuration ROM or the configuration data downloaded by the FPGA design software to the FPGA.

If the configuration is completed successfully, the FPGA CONF. LED lights up, and the FPGA parameters saved in the nonvolatile memory are set to the FPGA register areas.

Once the settings to the FPGA register are completed, one of the following states will be entered depending on the "FPGA control automatic start setting".

- If enabled: FPGA control is started.
- If disabled: FPGA control remains stopped.

If disabled, FPGA control start request (RY0) can be turned on at any time to start FPGA control.

■Notification of configuration anomaly

If an error occurs in the FPGA configuration, the FPGA module will be in the following states.

- Latest error code (RWr0): FPGA configuration error (error code: 3C01H)
- Error status flag (RXA): ON
- ERR. LED: On
- FPGA CONF. LED: Off

Point

The FPGA module monitors the configuration status of the FPGA even after configuration completed successfully. If an error is detected by this monitoring, it will be in the same state. (☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT)

■Causes of configuration errors and corrective actions

Item	Cause	Corrective action
Configuration at power-on, remote RESET, and FPGA download (JIC format/RPD format file)	• The configuration data stored in the configuration ROM is invalid. • The configuration ROM has been erased. • An error was detected when accessing the configuration ROM.	After eliminating the cause of the error, turn on and off the power or perform a remote RESET. For details on the corrective action, refer to the following. ☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT
Configuration employing FPGA download (SOF format file)	• FPGA downloaded configuration data is invalid. • FPGA download was performed while function setting switch 5 was OFF.	After eliminating the cause of the error, turn off and on the power, or perform a remote reset. Then download from the FPGA design software again. For details on the corrective action, refer to the following. ☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT
In common	An error occurred when transferring the configuration data to the FPGA due to the effects of noise or other causes.	—

Point

The error is not cleared even after the error clear request flag (RYA) was turned off and on. Also, FPGA control will not start even if the FPGA control start request (RY0) is turned off and on.

■Precautions when saving parameters

- If the parameter save request (RY2) is turned on and off while the parameter is set to a value that is out of range or cannot be set, an error will occur and the parameter will not be saved to the non-volatile memory. Refer to the error code, set the parameters again, and turn on and off Parameter save request (RY2). (☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT)
- While "Parameter write (Memory + Non-volatile memory)" or the parameter read is being executed by the FPGA Module Configuration Tool, saving cannot be performed by turning off and on Parameter save request (RY2). If executed, non-volatile memory access conflict (parameter) (error code: 1063H) will occur. (☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT)
- If an abnormality is detected while writing to non-volatile memory, the non-volatile memory access error (parameter) (error code: 1062H) will occur. (☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT)

■Number of saves

The number of times that saving to the non-volatile memory is possible is 10000. If the number of saves to the non-volatile memory exceeds 10000, the parameters will not be saved. Also note that turning off and on Parameter save request (RY2) can also lead to the number of parameter saves exceeding 10000; in such cases an error will occur and the following status will be entered.

- Latest error code (RWr0): Parameter save limit error (error code: 1052H)
- Error status flag (RXA): ON
- ERR. LED: Flashing

Initializing FPGA parameters

When the parameter initialization command (remote buffer memory address: 1000H) is set to 1, the non-volatile memory, FPGA register, and remote buffer memory parameters are initialized. When initialization is completed, parameter initialization completed (remote buffer memory address: 1001H) is set to Completed (1). When a non-volatile memory data error (parameter) (error code: 2010H) occurs, the FPGA module can be restored.

Point

FPGA control will stop from the time when the parameter initialization command (remote buffer memory address: 1000H) has been issued command (1) until parameter initialization completed (remote buffer memory address: 1001H) is set to Completed (1). During this time, FPGA control cannot be started even if FPGA control start request (RY0) is turned on and off.

FPGA parameter

■FPGA register areas and remote buffer memory

FPGA parameters can be saved in non-volatile memory inside the FPGA module. The saved FPGA parameters are transferred to the FPGA register areas and remote buffer memory when FPGA configuration is completed successfully.

Classification	FPGA function block	FPGA parameter Item
Standard circuit	• Reset control part • Timing control part • Digital output control part • Digital input control part • Digital I/O control part • Analog input control part • Logging part	Register areas classified as parameters in FPGA register areas (☞ Page 503 List of FPGA register areas)
	• Analog output part • Logging part	• DAC setting parameters in remote buffer memory • Remote buffer memory logging settings
User circuit	User circuit part	Number of words (0 to 384) specified by the user circuit part parameter size from the start address of the Writing data (transient area) of the FPGA register FPGA register address: 1000_B000H to 1000_B000H + (User circuit part parameter size × 2 - 1)

FPGA parameters are reflected in the FPGA when FPGA control start (RY0) is turned from off to on. Changes are made to the FPGA register and remote buffer memory while FPGA control flag (RX0) is off. By turning FPGA control start (RY0) from off to on, the FPGA parameter can be reflected in the FPGA. The timing at which the FPGA register setting values are reflected in the FPGA operation differs depending on FPGA register. For details, refer to the following.

☞ Page 502 FPGA register

■Saving FPGA parameters to non-volatile memory

There are two methods for saving FPGA parameters to non-volatile memory.

Method	Procedure
Use the FPGA Module Configuration Tool to save parameters	For the procedure for writing parameters using the FPGA Module Configuration Tool, refer to the following. ☞ Page 98 FPGA parameters After parameter writing is completed by the FPGA Module Configuration Tool, the FPGA parameters are deployed to the FPGA register and remote buffer memory.
Use Parameter save request (RY2) to save parameters	By turning on and off Parameter save request (RY2), the FPGA register and remote buffer memory setting values of the FPGA parameters are saved in non-volatile memory. Also, the module parameter area of the remote buffer memory is saved together. For the FPGA register areas and remote buffer memory saved as FPGA parameters, refer to the following. ☞ Page 314 FPGA register areas and remote buffer memory

Checking FPGA parameters

■Setting range check

The FPGA module checks whether the FPGA parameters are within the settable range at the following timing.

- After FPGA configuration
- At FPGA control automatic start
- When the FPGA control start flag (RY0) turns off and on
- When Parameter save request (RY2) turns off and on

If the set value of the FPGA parameter is out of the settable range, an error corresponding to the parameter is output and the following status occurs.

- Latest error code (RWr0): Error code storage
- Error status flag (RXA): ON
- ERR. LED: On

If an FPGA parameter error occurs, even if FPGA control start request (RY0) is turned on and off, FPGA control does not start. After correcting the FPGA parameter to a value within the settable range, turn the error clear request flag (RYA) off and on, and turn off and on FPGA control start request (RY0).

■Data check in non-volatile memory

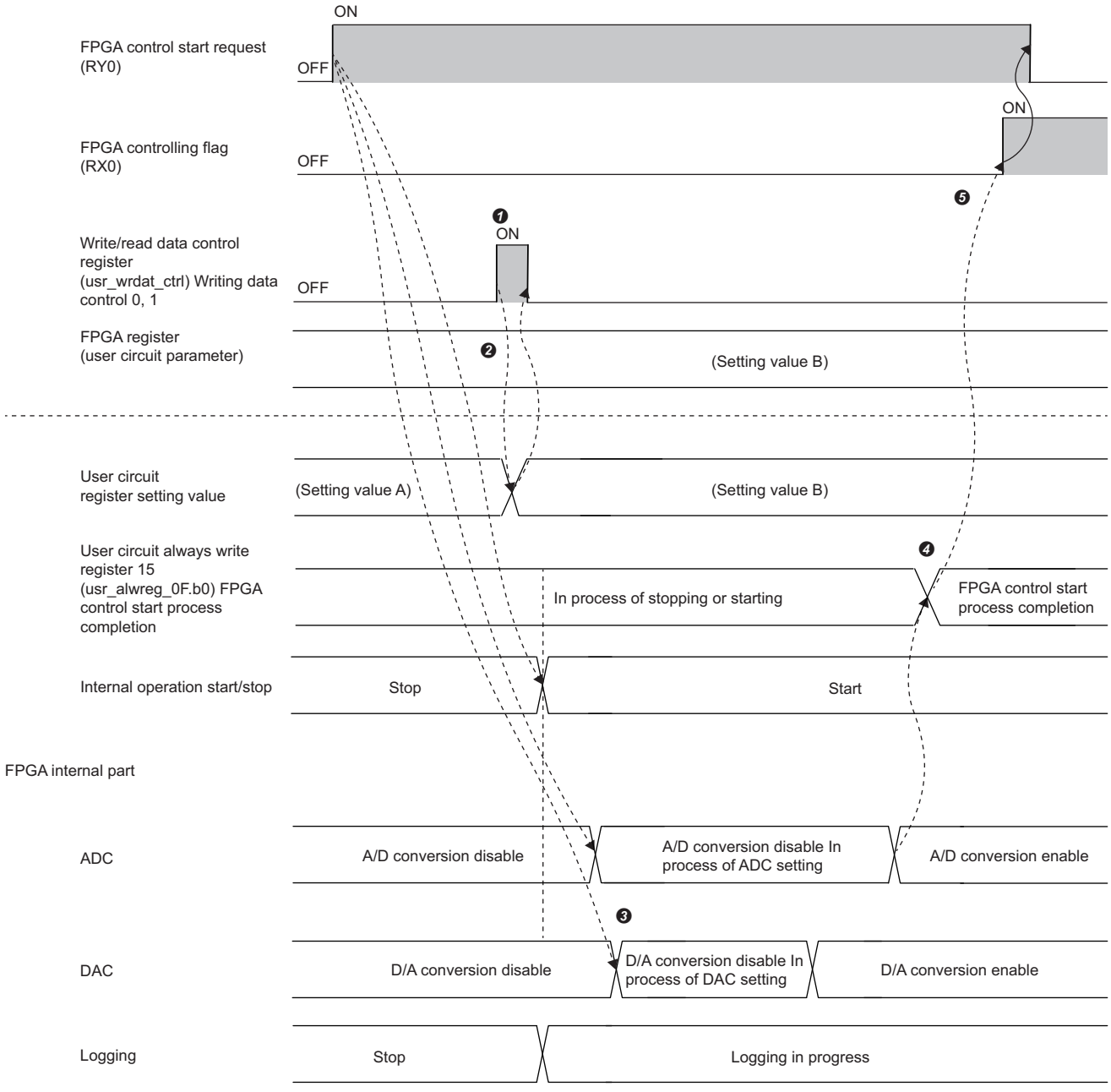
When an abnormality is detected in the data in non-volatile memory, a non-volatile memory data error (parameter) (error code: 2010H) will occur. Set the parameters again using the FPGA Module Configuration Tool. Or, issue the parameter initialization command (remote buffer memory address: 1000H) to initialize the parameters and set the parameters again.

12.5 FPGA Control Function

The FPGA standard circuit and user circuits can be started or stopped.

Starting FPGA control

FPGA control is started by turning off and on FPGA control start request (RY0). The starting order of the FPGA is shown below.



- - - - - - - - ▶ Implemented in FPGA module
——————▶ Executed by the program.

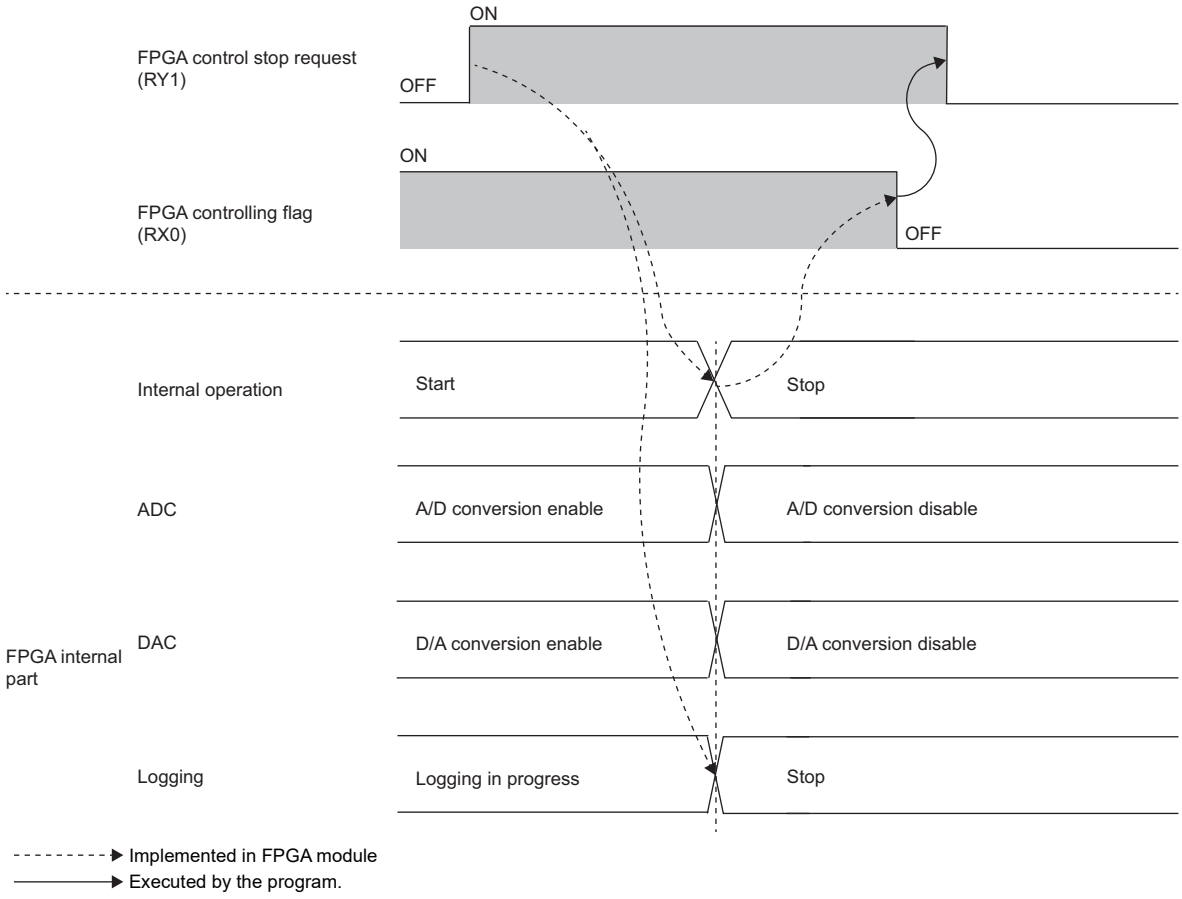
❶ b0, b1 of Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) are turned on, and the writing data (usr_wreg_000 to usr_wreg_1FF) are reflected in the user circuit.
❷ A clock is supplied to the standard circuit and user circuit, and FPGA control starts.
❸ ADC and DAC are set.
❹ b0 of Always write register 15 (usr_alwreg_0F) (FPGA register address: 1000_A02EH) of the user circuit part stores Start processing completed (1).
❺ FPGA control flag (RX0) turns on.

Point

ADC and DAC conversions do not start at the same time as the standard circuit and user circuit. Setting completion for ADC and DAC can be determined by checking b0 of Always write register 15 (usr_alwreg_0F) (FPGA register address: 1000_A02EH) of the user circuit part.

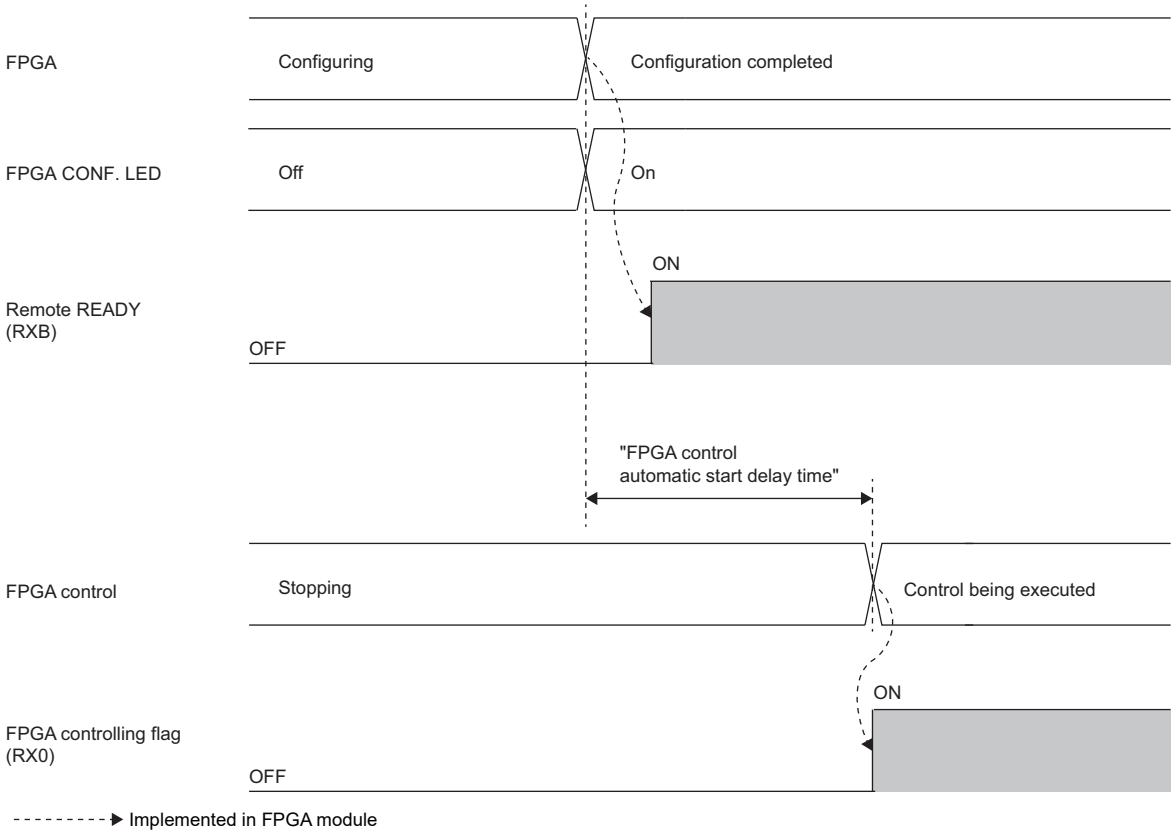
Stopping FPGA control

FPGA control is stopped by turning off and on FPGA control stop request (RY1).



FPGA control automatic start

When "FPGA control automatic start setting" is "Enable", FPGA control starts automatically after configuration is complete.
The "FPGA control automatic start delay setting" can be used to set a delay (seconds) before automatic start.
When a moderate error is cleared by turning on and off the error clear request flag (RYA), if "FPGA control automatic start setting" is "Enable", FPGA control starts automatically.



■Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 98 FPGA parameters)

Operating procedure

1. Set "FPGA control automatic start setting" to "Enable".
2. Set the time from after configuration is complete to when the FPGA automatically starts in "FPGA control automatic start delay setting".

Continue FPGA control

In CC-Link IE TSN communication mode, the "FPGA control continuation setting" allows selecting whether to continue or stop FPGA control according to the CPU module status and data link status. Depending on setting for the "FPGA control continuation setting", the FPGA operates as follows.

CPU module status and data link status		FPGA control continuation setting	
		0: "Stop"	1: "Continue"
Data link in operation	RUN state	Operating	Operating
	STOP state*1*2	Stop	Operating
	PAUSE state	Operating	Operating
	Stop error*1	Stop	Operating
During disconnection, cyclic stop*1		Stop	Operating

*1 RY and RWw retain the values received during CPU module RUN and PAUSE. RY and RWw are not cleared by the "Output Hold/Clear Setting during CPU STOP" of the master station.

*2 The retained RY and RWw can be changed by the remote device test of the master station. Therefore, when the CPU module is in the STOP state, it is possible to start or stop FPGA control and change things such as the on/off states of external output signals. For the remote device test, refer to the manual of the master station used.

Point

If a moderate error or severe error that prevents FPGA control from starting occurs in the FPGA module, the FPGA will stop regardless of "FPGA control continuation setting".

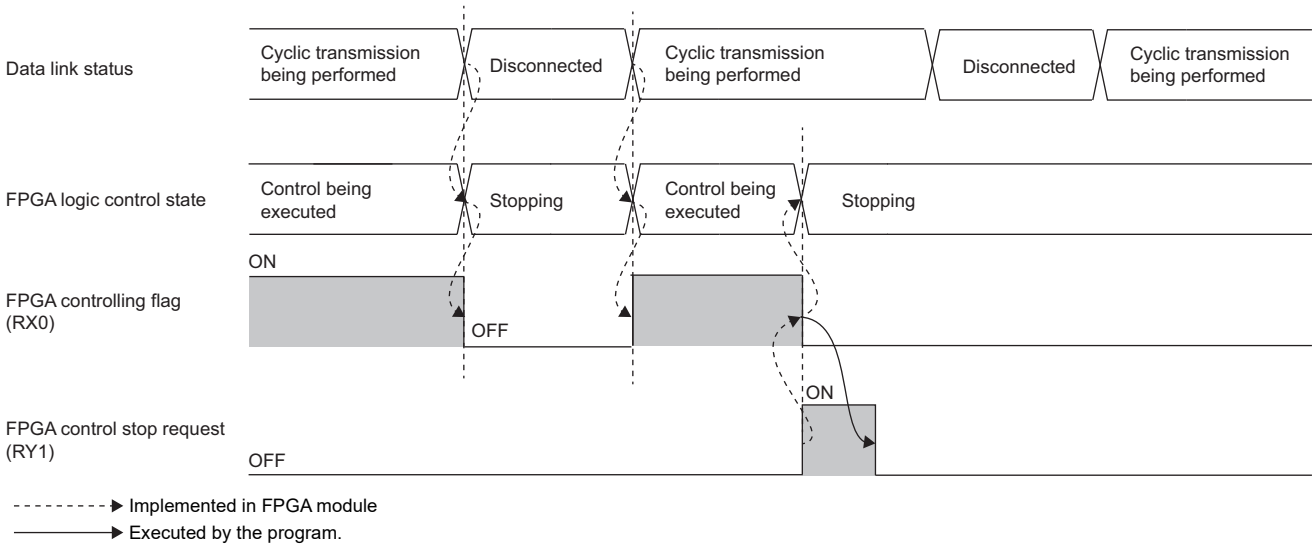
■Operation example of "FPGA control continuation setting"

The operation of the FPGA module during disconnection is shown below.

Ex.

When "Stop" is set for "FPGA control continuation setting"

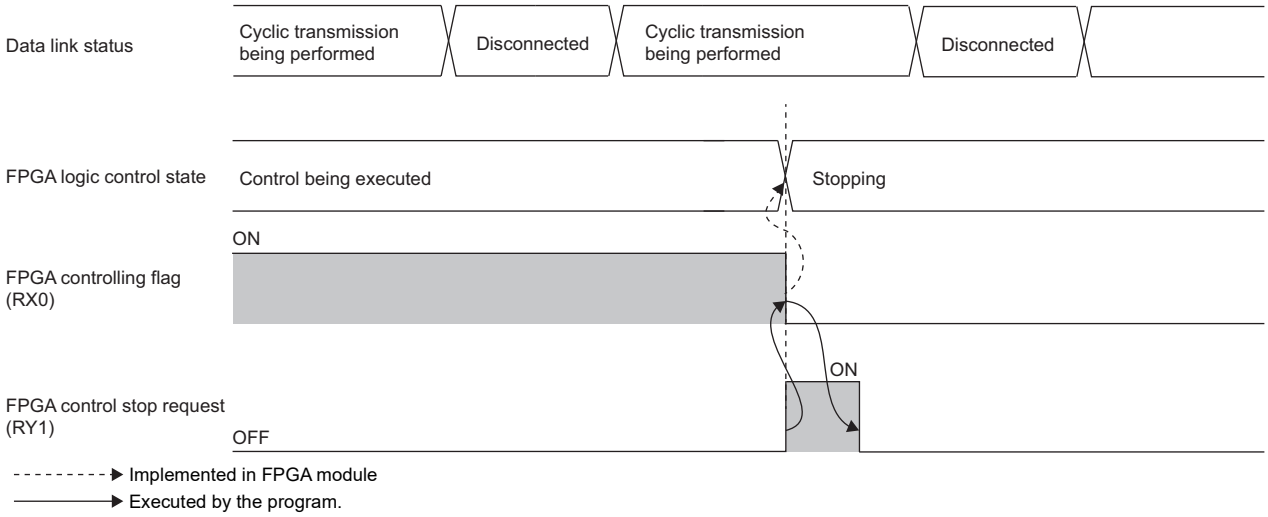
FPGA control stops at Disconnection. Upon Return, FPGA control returns to the state before disconnection.



Ex.

When "FPGA control continuation setting" is set to "Continue"

Continues FPGA control regardless of the data link status.

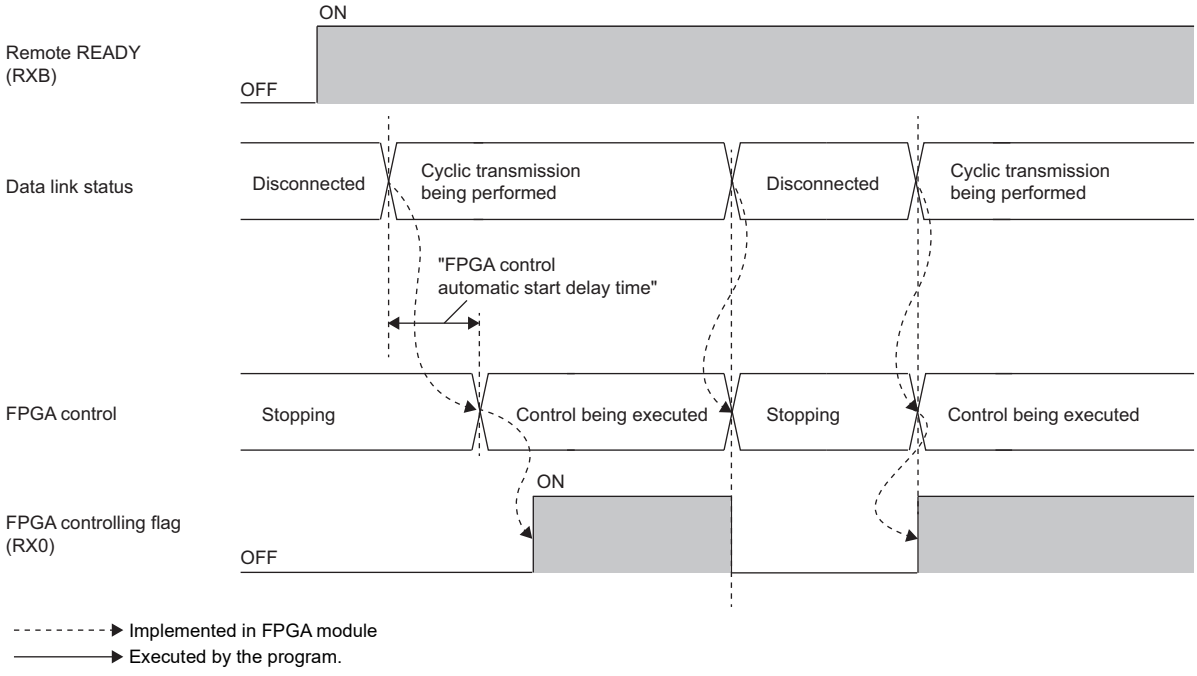


Ex.

When "FPGA control continuation setting" is set to "Stop" and " FPGA control automatic start setting" is set to "Enable"

FPGA control starts after the time set in "FPGA control automatic start delay time" has elapsed after data linking with the master station after configuration is completed.

The "FPGA control automatic start setting" and "FPGA control automatic start delay time" settings do not affect the restoration of FPGA control upon disconnection/return.



■Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 98 FPGA parameters)

Operating procedure

1. Set "FPGA control continuation setting" to "Stop" or "Continue".

Output HOLD/CLEAR setting

Sets whether to retain (HOLD) or clear (CLEAR) the value that was output immediately before FPGA control stops.

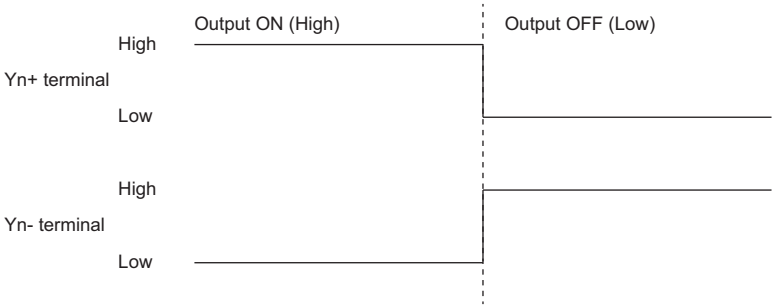
When FPGA control is stopped, the external output will be in the following states depending on the HOLD/CLEAR setting.

Output type	FPGA parameter		HOLD/CLEAR operation	Output just before stopping FPGA control	Output during FPGA control stop[*6]
	"External reset ON/OFF"	"Differential output HOLD/CLEAR Y☐ "[*1*2]			
DC output	OFF	—	HOLD	OFF	OFF
				ON	ON
	ON		CLEAR	OFF	OFF
				ON	
Differential output, differential input/output (when output is selected)	OFF	HOLD	HOLD	OFF (Low)	OFF (Low)[*3]
				ON (High)	ON (High)[*3]
		CLEAR (Fixed to H)	CLEAR (Fixed to H)	OFF (Low)	ON (High)[*3]
				ON (High)	ON (High)[*3]
		CLEAR (Fixed to L)	CLEAR (Fixed to L)	OFF (Low)	OFF (Low)[*3]
				ON (High)	OFF (Low)[*3]
	ON	—	CLEAR	OFF (Low)	Hi-Z (depending on connected equipment)[*7]
				ON (High)	
Analog output	OFF	—	HOLD	D/A conversion value	Retention[*4]
	ON		CLEAR	D/A conversion value	0V/0mA[*5]

*1 ☐: 0 to 7

*2 For differential input/output, it is "Differential output HOLD/CLEAR".

*3 The state of the Yn+/Yn- terminals is as follows.



*4 Of the analog output parameters, the output of CH whose range setting, offset, or HOLD/CLEAR has been changed becomes 0V/0mA when FPGA control starts.

*5 Immediately after FPGA control stops, it becomes Hi-Z.

*6 When a serious error occurs, the DC output is OFF, the differential output is Hi-Z, and the analog output becomes 0V/0mA due to Hi-Z.

*7 External output may change from on to off or from off to on when FPGA control is stopped.

■Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 98 FPGA parameters)

Operating procedure

1. Set "External reset ON/OFF" to "ON" or "OFF".
2. Set "Differential output HOLD/CLEAR Y☐ " or "Differential Output HOLD/CLEAR".

12.6 FPGA Register Access Function

Reads from and writes to the FPGA register areas from the master station program.

There are two methods for reading from and writing to FPGA register areas. The appropriate method should be selected.

- Remote register method
- Method using remote buffer memory

Remote register method

This is used to periodically read from and write to the FPGA register areas (user circuit areas) from a program.

In CC-Link IE TSN communication mode, data is cyclically updated between the remote register areas and FPGA register areas.

Access range of FPGA register access

○: Possible, △: Partially possible, ×: Impossible

FPGA register areas		Remote register areas	
		Read	Write
Reset control part		×	×
Timing generator			
Digital input control part			
Digital output control part			
Digital I/O control part			
Analog input control part			
Analog output control part			
Logging part			
User circuit	Cyclic area	○	○
	Transient area	×	×
	Others	×	×
Reserve		×	×
System area			

Details

Reading data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) (FPGA register address: 1000_BB00H to 1000_BBFEH) are read to the FPGA register read area (RWr10 to RWr8F). Also, the FPGA register write area (RWw10 to RWw8F) is Writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF) (FPGA register address: 1000_B300H to 1000_B3FEH).
When designing the user circuit, reading data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) (FPGA register address: 1000_BB00H to 1000_BBFEH) and writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF) (FPGA register address: 1000_B300H to 1000_B3FEH) can be accessed cyclically from the program.
The read/write register is 128 words.

■Write (remote register → FPGA register areas)

The values in the FPGA register write area (RWw10 to RWw8F) are written to the writing data (cyclic area) (FPGA register addresses: 1000_B300H to 1000_B3FEH).

■Read (remote register ← FPGA register)

After power-on, reading starts when FPGA configuration is completed.

■Writing in CC-Link IE TSN communication mode

The value of FPGA register write area (RWw10 to RWw8F) is reflected in the user circuit at all points simultaneously after being written to the FPGA register areas. Therefore, even if multiple FPGA register write areas are set in the same scan of the sequence program, they can be reflected in the user circuit at the same time.

■Reading in CC-Link IE TSN communication mode

FPGA register read areas (RWr10 to RWr8F) store the values read from the user circuit to FPGA register areas at all points simultaneously. Therefore, the sequence program can acquire FPGA register values at the same timing.

Allocation of read/write areas for FPGA register areas

The values in the FPGA register write area (RWw10 to RWw8F) are written to the writing data (cyclic area) (usr_wreg_180 to usr_wreg_1ff) (FPGA register addresses: 1000_B300H to 1000_B3FEH). Also, reading data (cyclic area) (usr_rreg_180 to usr_rreg_1ff) (FPGA register addresses: 1000_BB00H to 1000_BBFEH) is read out to the FPGA register read area (RWr10 to RWr8F).

■FPGA register write area and FPGA register areas

FPGA register write area		FPGA writing data (cyclic area)	
Device number	**Name**	**FPGA register address**	**Name**
RWw10	FPGA register write area 0	1000_B300H	Writing data 0 (usr_wreg_180)
RWw11	FPGA register write area 1	1000_B302H	Writing data 1 (usr_wreg_181)
RWw12	FPGA register write area 2	1000_B304H	Writing data 2 (usr_wreg_182)
⋮			
RWw8D	FPGA register write area 125	1000_B3FAH	Writing data 125 (usr_wreg_1fd)
RWw8E	FPGA register write area 126	1000_B3FCH	Writing data 126 (usr_wreg_1fe)
RWw8F	FPGA register write area 127	1000_B3FEH	Writing data 127 (usr_wreg_1ff)

■FPGA register read area and FPGA register areas

FPGA register read area		FPGA reading data (cyclic area)	
Device number	**Name**	**FPGA register address**	**Name**
RWr10	FPGA register read area 0	1000_BB00H	Reading data 0 (usr_rreg_180)
RWr11	FPGA register read area 1	1000_BB02H	Reading data 1 (usr_rreg_181)
RWr12	FPGA register read area 2	1000_BB04H	Reading data 2 (usr_rreg_182)
⋮			
RWr8D	FPGA register read area 125	1000_BBFAH	Reading data 125 (usr_rreg_1fd)
RWr8E	FPGA register read area 126	1000_BBFCH	Reading data 126 (usr_rreg_1fe)
RWr8F	FPGA register read area 127	1000_BBFEH	Reading data 127 (usr_rreg_1ff)

Precautions

- If the CC-Link TSN network synchronous communication function is not used in CC-Link IE TSN communication mode, data transfer between the remote register and FPGA register is performed in 1ms cycles. When using the CC-Link TSN network synchronous communication function, data transfer between the remote register areas and FPGA register areas is performed at the synchronous cycle of the master station. (☞ Page 353 CC-Link IE TSN Network Synchronous Communication Function)
- When used in CC-Link IE TSN communication mode, data is written and read between remote register areas and FPGA register areas by the number of remote register areas (RWr, RWw) of the FPGA module set in the network structure settings of the master station.
- Data transfer between the remote register areas and FPGA register areas is not performed when a moderate error or severe error occurs.

Method using remote buffer memory

Any FPGA register can be read from and written to. It is used to write and read at specific timings such as the initial setting of FPGA register areas from the program. Data is updated between the remote buffer memory and the FPGA register areas when writing to the remote buffer memory or writing a read request.

Access range of FPGA register access

When using the remote buffer memory, the read and write range of the FPGA register areas differs depending on whether writing or reading is taking place.

○: Possible, △: Partially possible, ×: Impossible

FPGA register		Remote buffer memory	
		Read	Write
Reset control part		○	△
Timing generator			
Digital input control part			
Digital output control part			
Digital I/O control part			
Analog input control part			
Analog output control part			
Logging part			
User circuit	Cyclic area	×	×
	Transient area	○	○
	Others	○	△
Reserve		○*1	○
System area			×

*1 Read value is not guaranteed. Do not use it for control.

■Access range when reading/writing FPGA register areas

The reading data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) is read to the FPGA register read area (RWr10H to RWr8FH). Also, the FPGA register write area (RWw10 to RWw8F) is written to the writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF).

When designing the user circuit, data allocated to the reading data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) and writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF) can be accessed periodically from the program.

■When reading

FPGA register areas other than writing data (cyclic area) (1000_B300H to 1000_B3FEH) and reading data (cyclic area) (1000_BB00H to 1000_BBFEH) can be read.

■When writing

The write range varies depending on the state of FPGA control flag (RX0).

○: Can be written, ×: Cannot be written

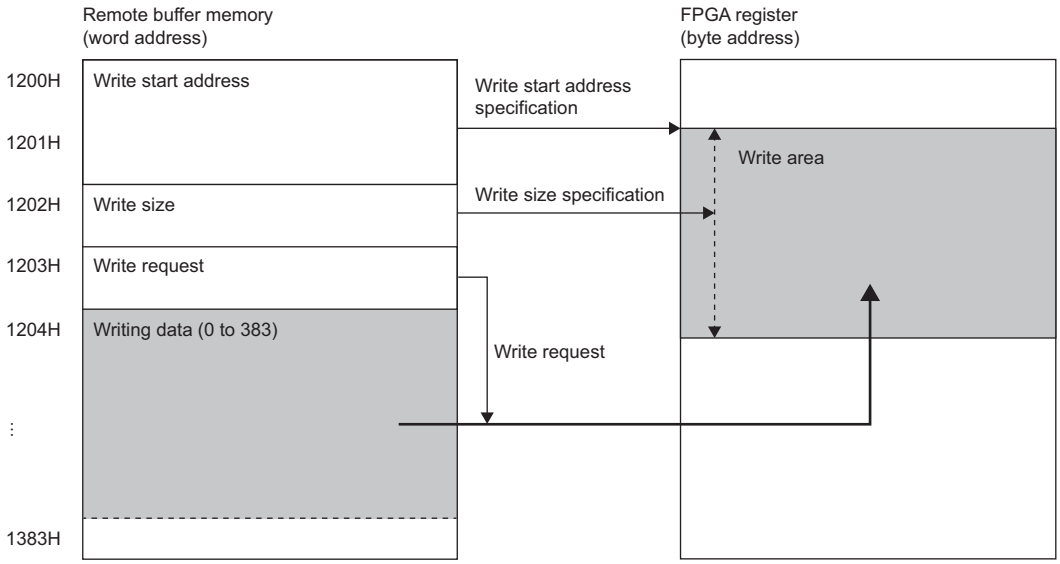
FPGA register		FPGA control flag (RX0)	
Region	Type	OFF (while FPGA control is stopped)	ON (during FPGA control)
Each control area	Control	○	○
	Parameter	○	×
	Monitor	×	×
	Reserve	○	×
	System area	×	×
User circuit area*1	Writing data (transient area)	○	○
	Writing data (cyclic area)	×	×
Reserve		○	×
System area		×	×

*1 Other than writing data (transient area) and writing data (cyclic area) in the user circuit area, it is the same as each control area.

Details

■Write

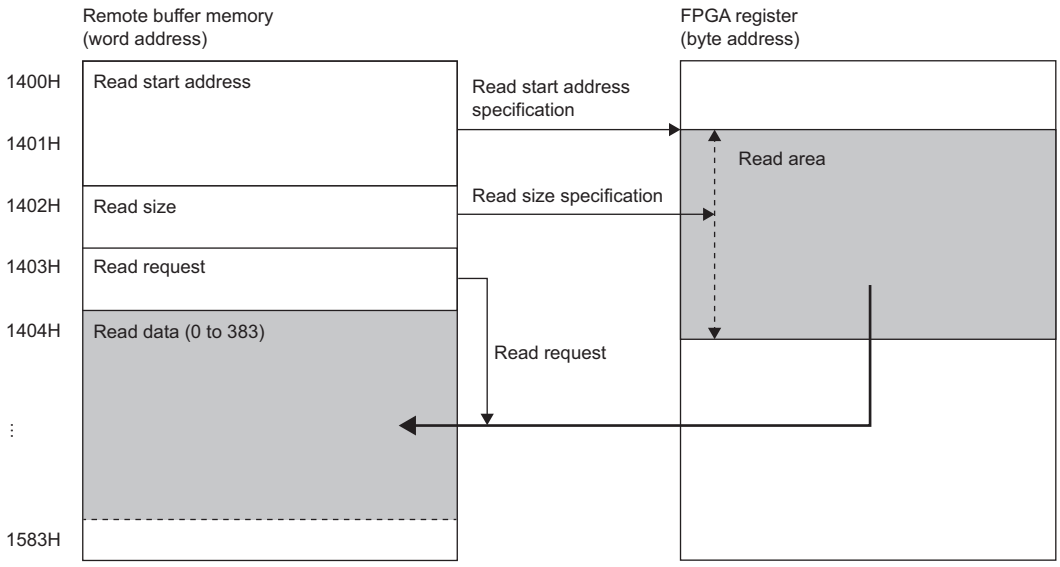
When a Write request (remote buffer memory address: 1203H) is requested (1), writing data 0 (remote buffer memory address: 1204H) to writing data 383 (remote buffer memory address: 1383H) are written, according to the number of words set for the write size (remote buffer memory address: 1202H), starting with the FPGA register that was set as the write start address (remote buffer memory address: 1200H, 1201H).



Remote buffer memory	Address	Description
Write start address	1200H, 1201H	Sets the start address (byte address) of the target FPGA register. Set an even address. If an invalid address is set as the write start address and the write request is set to 1 (requested), a "Write start address out-of-range error" occurs, Error status flag (RXA) turns on, and the ERR. LED flashes. In this case, writing data 0 to writing data 383 are not written to the FPGA register areas. The following are invalid addresses. • Odd-numbered address • Address of non-writable FPGA register
Write Size	1202H	Set the size (in word units) to be written to the FPGA register areas among writing data 0 to writing data 383 in the remote buffer memory. The number of words of data specified by the write size starting from writing data 0 in the remote buffer memory is written to the FPGA register specified by the write start address. The settable range is 1 to 384 words. If the write size is invalid, an "FPGA register write size out-of-range error" will occur, Error status flag (RXA) will turn on, and the ERR. LED flashes. In this case, writing data 0 to writing data 383 are not written to the FPGA register areas. The following are incorrect sizes. • A value other than 1 to 384 • When non-writable FPGA register areas are included in the write range
Write request	1203H	When the write request is set to 1 (requested), Writing data 0 to Writing data 383 of the remote buffer memory are written starting from the FPGA register specified by the write start address and the number of words specified by the write size. When writing to the FPGA register areas is completed, the execution result is stored in the write request. 0: When completed successfully -1: When completed with an error
Writing data 0 to writing data 383	1204H to 1383H	Sets the data to write to the FPGA register areas.

■Read

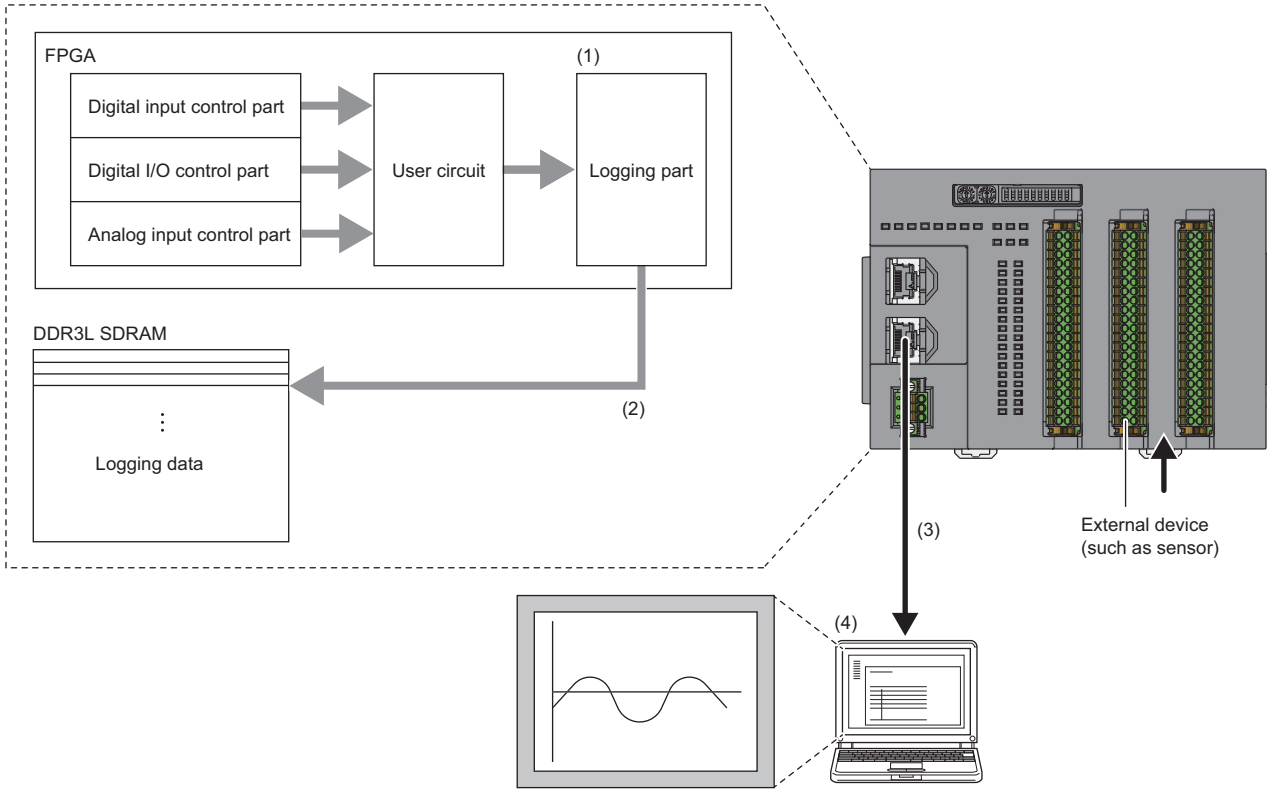
When a Read request (remote buffer memory address: 1403H) is requested (1), the number of words (read size) set in (remote buffer memory address: 1402H) is read to reading data 0 (remote buffer memory address: 1404H) to reading data 383 (remote buffer memory address: 1583H), from the FPGA register areas set for the read start address (remote buffer memory address: 1400H, 1401H).



Remote buffer memory	Address	Description
Read start address	1400H, 1401H	Set the start address (byte address) of the FPGA register to read from. Set an even address. If an invalid address is set as the read start address and the read request is set to 1 (requested), a "Read start address out-of-range error" occurs, Error status flag (RXA) turns on, and the ERR. LED flashes. In this case, the FPGA register values are not read from reading data 0 to reading data 383. The following are invalid addresses. • Odd-numbered address • Unreadable address
Read Size	1402H	Set the size (in words) to be read from the FPGA register to reading data 0 to reading data 383 of the remote buffer memory. Starting from the FPGA register specified by the read start address, the data for the number of words specified by the read size is read to reading data 0 to reading data 383 of the remote buffer memory. The settable range is 1 to 384 words. If the read size is invalid, an "FPGA register read size out-of-range error" will occur, Error status flag (RXA) will turn on, and the ERR LED will flash. In this case, the FPGA register values are not read from reading data 0 to reading data 383. The following are incorrect sizes. • A value other than 1 to 384 • When non-readable FPGA register areas are included in the read range
Read request	1403H	When the read request is set to 1 (requested), the data for the number of words specified by the read size is read from the FPGA register at the read start address to reading data 0 to reading data 383 of the remote buffer memory. When the read from the FPGA register is completed, the execution result is stored in the read request. 0: When completed successfully -1: When completed with an error
Reading data 0 to reading data 383	1404H to 1583H	The data read from the FPGA register is stored.

12.7 Logging Function

The logging part of the FPGA acquires the external input/output from the user circuit, count values, and other sources at the timing of when the sampling pulse is input, and writes them to DDR3L SDRAM. Since data before and after the occurrence of a problem can be stored, it can be used for phenomenon analysis. The logged data can be transferred to an FTP server using the FTP client function.



(1) Set logging parameters
- Logging operation setting
- Logging data size

(2) Logging data is stored in DDR3 SDRAM by sampling pulses.
(3) The logging data can be transferred to a personal computer via FTP.
(4) The logging data can be checked.

Logging control

The remote I/O signals that control the logging operation are shown below.

- Logging start flag (RX3)
- FTP transfer completion flag (RX4)
- FTP transfer error completion flag (RX5)
- FPGA control stop while data collection flag (RX6)
- Logging control stop flag (RX7)
- Logging start request (RY3)
- FTP resend allowed (RY4)
- Logging control stop request (RY7)

Start and stop logging

The method of starting and stopping logging differs depending on the "Select logging start control".

■When "Select logging start control" is "Register setting value (RY3)"

Logging is started or stopped by the logging start request (RY3). Logging cannot be started or stopped by logging enable (uc_logen_clk100m_reg) of the user circuit block terminal.

Logging state	Method
Start	When FPGA control flag (RX0) is on and the status of Logging operation state monitor (RWrB) is Collection start waiting (1H), Logging start request (RY3) is turned off and on to start the collection of logging data.
Stop	While the status of Logging operation state monitor (RWrB) is Collecting (2H) or Collecting after trigger (3H), switching on and off Logging start request (RY3) stops logging data collection. When collection is stopped, the collected logging data is transferred to the FTP server.

■When "Select logging start control" is "User circuit output"

Logging is started or stopped by logging enable (uc_logen_clk100m_reg) of the user circuit block terminal. Logging cannot be started or stopped by the logging start request (RY3).

Logging state	Update method
Start	When b3 of the Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Rising for logging start allowed (1), logging data collection starts by switching Logging enable (uc_logen_clk100m_reg) from Disable (0) to Enable (1).
Stop	When b3 of the Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Falling for logging start allowed (0), Logging enable (uc_logen_clk100m_reg) can be switched from Enable (1) to Disable (0) to stop the collection of logging data. When collection is stopped, logging data is transferred to the FTP server.

Logging operation status and availability of various requests

■Control by remote output signal

Control by the remote output signal may or may not be executed depending on the logging operation status. The following shows whether the logging operation state can be executed or not.

Remote output signals	Logging operation state monitor (RWrB)		Description
	Available upon request	After receiving the request	
Logging start request (RY3) turned off and on	Collection start waiting (1H)	Collecting (2H)	Starts collecting logging data.
	FTP transfer start waiting (5H)	FTP transfer in progress (4H)	Starts transferring logging data.
Logging start request (RY3) turned on and off	• Collecting (2H) • Collecting after trigger (3H)	FTP transfer in progress (4H)	Stops collecting logging data.
Logging control stop request (RY7) turned off and on	• Collecting (2H) • Collecting after trigger (3H)	Collection start waiting (1H)	Stops collecting logging data.
	FTP transfer in progress (4H)	Collection start waiting (1H), FTP transfer start waiting (5H)*1	Aborts the transfer of logging data.

*1 If FTP resend allowed (RY4) is on before executing the request by the remote output signal, the status becomes FTP transfer start waiting (5H). If FTP resend allowed (RY4) is off, it will be waiting for collection to start (1H). When the status of Logging operation state monitor (RWrB) is in FTP transfer start waiting (5H), if FTP resend allowed (RY4) is turned from on to off, the status becomes Collection start waiting (1H).

Point

Requests are not accepted in the non-executable state and are ignored.
Also, if the logging start request (RY3) is turned on when the logging operation status is one of the following, a logging start request error (error code: 1420H) occurs.

- Collecting (2H)
- Collecting after trigger (3H)
- FTP transfer in progress (4H)

Control by user circuit logging start/stop request

The statuses in which logging start requests or stop requests can be accepted by the user circuit are shown below. When issuing a logging start or stop request, set b3 of the logging operation control register (lgdw_ctrl) (remote register address: 1000_9000H) as an interlock.

Logging start/ stop request	Logging enable (uc_logen_clk100m_reg) status	State of b3 of logging operation control register (lgdw_ctrl) (remote register address: 1000_9000H)	Description
Logging start request	Switch from Disable (0) to Enable (1)	Logging start rising enable (1)	Starts collecting logging data.
Logging stop request	Switch from Enable (1) to Disable (0)	Enable logging start falling edge (0)	Stops collecting logging data.

Point

If a request to start or stop logging is made while requests cannot be accepted, an error will occur as follows.

- When b3 of Logging operation control register (lgdw_ctrl) (remote register address: 1000_9000H) is Falling for logging start allowed (0), and logging start is requested, logging control start violation error (error code: 1430H) occurs.
- When b3 of Logging operation control register (lgdw_ctrl) (remote register address: 1000_9000H) is Rising for logging start allowed (1), and logging stop is requested, the logging control stop violation error (error code: 1431H) occurs.

Retransmission and transfer of logging data

If the below described ❶ to ❸ occurs, the transfer of logging data to the FTP server will be incomplete. In this state, whether to resend or transfer logging data to the FTP server can be selected.

- ❶ If a communication error occurs during FTP transfer and the transfer is not completed successfully.
- ❷ If the logging control stop request (RY7) was turned off and on during FTP transfer
- ❸ When FPGA control stops while collecting logging data

■When resending or transferring logging data

- Set FTP resend allowed (RY4) to on before starting logging data collection. If ❶ to ❸ occurs, Logging operation state monitor (RWrB) will wait for FTP transfer start waiting (5H). In this state, turn off and on the logging start request (RY3), and the collected logging data can then be resent or transferred.
- When Logging operation state monitor (RWrB) is in FTP transfer start waiting (5H), if FTP resend allowed (RY4) is turned off, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H). In this state, turn off and on the logging start request (RY3), and the next logging will start.

■When not resending or transferring logging data

Turn off FTP resend allowed (RY4) before starting logging data collection. If ❶ to ❸ occurs, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H). In this state, turn off and on the logging start request (RY3) and the next logging will start.

Stopping logging control

When logging starts, logging data is collected and transferred to the FTP server. By turning off and on the logging control stop request (RY7) during this control, logging data collection and FTP transfer can be stopped.

■Aborting during logging data collection

Collecting logging data is stopped, and the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H).

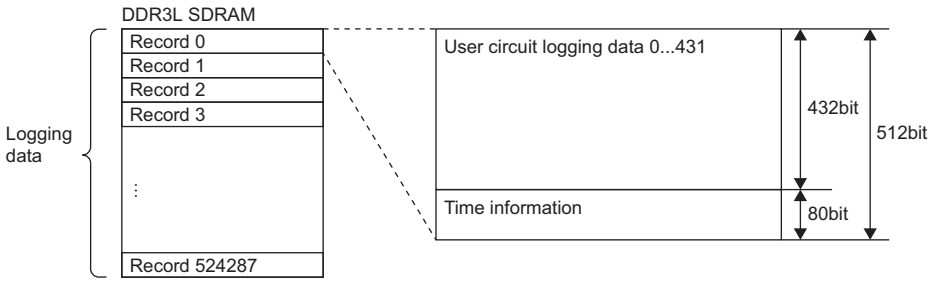
■Aborting during FTP transfer

Stops FTP transfer. For the status after cancellation, refer to the following.

☞ Page 330 Retransmission and transfer of logging data

Record details

A 512-bit record, which is a combination of 432-bit logging data and 80-bit time data, is called a record. Records cannot be resized.



Allocation of signals to be stored in logging data is configured by the user circuit. The allocation of logging data in the sample circuit is shown below.

	First bit	First word	Logging data															
			Description	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
User circuit logging data 0 to 431 (432 bits)	0	0	Digital input signal (after filtering) (B0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	16	1	Digital input signal (after filtering) (B1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	32	2	Digital input signal (after filtering) (B2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	48	3	Digital input signal (after filtering) (E0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	64	4	Digital input signal (after filtering) (E1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	80	5	Digital input signal (after filtering) (E2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	96	6	Counter control part 32-bit ring counter (2-phase multiple of 4) (B0)	Empty														Phase B	Phase A
	112	7		Counter value (32 bits)															
	128	8																	
	144	9	Counter control part 32-bit ring counter (2-phase multiple of 4) (B1)	Empty														Phase B	Phase A
	160	10		Counter value (32 bits)															
	176	11																	
	192	12	Counter control part 32-bit ring counter (2-phase multiple of 4) (B2)	Empty														Phase B	Phase A
	208	13		Counter value (32 bits)															
	224	14																	
	240	15	Counter control part 32-bit ring counter (2-phase multiple of 4) (E0)	Empty														Phase B	Phase A
	256	16		Counter value (32 bits)															
	272	17																	
	288	18	Counter control part 32-bit ring counter (2-phase multiple of 4) (E1)	Empty														Phase B	Phase A
	304	19		Counter value (32 bits)															
	320	20																	
	336	21	Counter control part 32-bit ring counter (2-phase multiple of 4) (E2)	Empty														Phase B	Phase A
	352	22		Counter value (32 bits)															
	368	23																	
	384	24	Empty	Empty															
	400	25																	
	416	26																	
Time information (80 bits)	432	27	µs	Empty						µs(10bit)									
	448	28	ms	Empty						ms(10bit)									
	464	29	Minute, second	Empty				Minute (6 bits)						Second (6 bits)					
	480	30	Month, day, hour	Empty		Month (4 bits)				Day (5 bits)					Hour (5 bits)				
	496	31	Year	Empty									Year (7 bits)						

By changing the RTL of the user circuit with reference to the sample circuit, the signal to be logged can be changed. For details, refer to the following.

☞ Page 217 User Circuit Block

Time setting

Set the time of the timestamp added to the logging data.

Point

The FPGA module does not correct time information for daylight saving time. Set the time corrected for summer time in the FPGA module.

CC-Link IE TSN communication mode

Set the first time information distributed from the master station during data link with the master station.

Point

If there is no data link with the master station at startup, it starts at 00:00:00 on January 1, 1970.

Standalone mode

Time information can be set by remote buffer memory.

- Time information set (remote buffer memory address: 1600H) (☞ Page 500 Time information set)

When Time information set (remote buffer memory address: 1600H) is used to set the time information (1), the following remote buffer memory values are set.

- Time information (year) (remote buffer memory address: 1601H) (☞ Page 500 Time information (year))
- Time information (month, day, hour) (remote buffer memory address: 1602H) (☞ Page 501 Time information (month, day, hour))
- Time information (minutes, seconds) (remote buffer memory address: 1603H) (☞ Page 501 Time information (minute, second))

The time information added to records is updated by the FPGA based on the set time. The FPGA time information can be checked with the following FPGA register areas.

- Time information (year) (lgdw_clock_rddata1) (FPGA register address: 1000_9030H)
- Time information (month, day, hour) (lgdw_clock_rddata2) (FPGA register address: 1000_9032H)
- Time information (minutes, seconds) (lgdw_clock_rddata3) (FPGA register address: 1000_9034H)
- Time information (ms) (lgdw_clock_rddata4) (FPGA register address: 1000_9036H)
- Time information (μs) (lgdw_clock_rddata5) (FPGA register address: 1000_9038H)

Point

- If a value outside the setting range is set, the time setting error (error code: 1210H) is stored in Latest error code (RWr0) and Error status flag (RXA) turns on.
- Time information (ms) (lgdw_clock_rddata4) (FPGA register address: 1000_9036H) and time information (μs) (lgdw_clock_rddata5) (FPGA register address: 1000_9038H) is reset to 0 when the time is set.
- If the time setting is not set, the time will start from January 1, 1970, 00:00:00.00.

When time information is changed during logging

The time information in the record is also changed partway through.

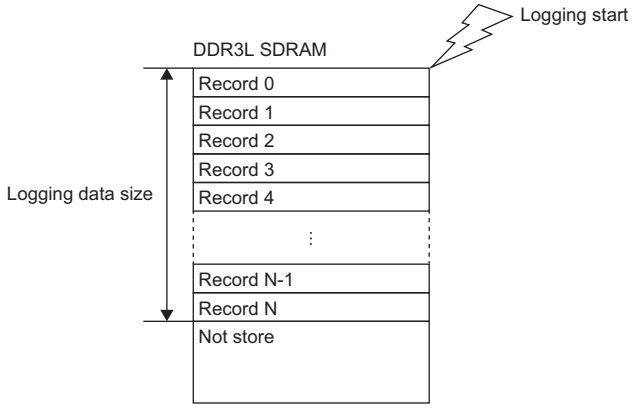
- In CC-Link IE TSN communication mode, when the time is set by the FPGA module by linking with the master station during logging.
- When the time is changed by the master station by 1 second or more in CC-Link IE TSN communication mode.
- When the time is set by the remote buffer memory during logging in standalone mode.

Operation example

Here is an example of logging operation.

Storage operation mode (linear buffer)

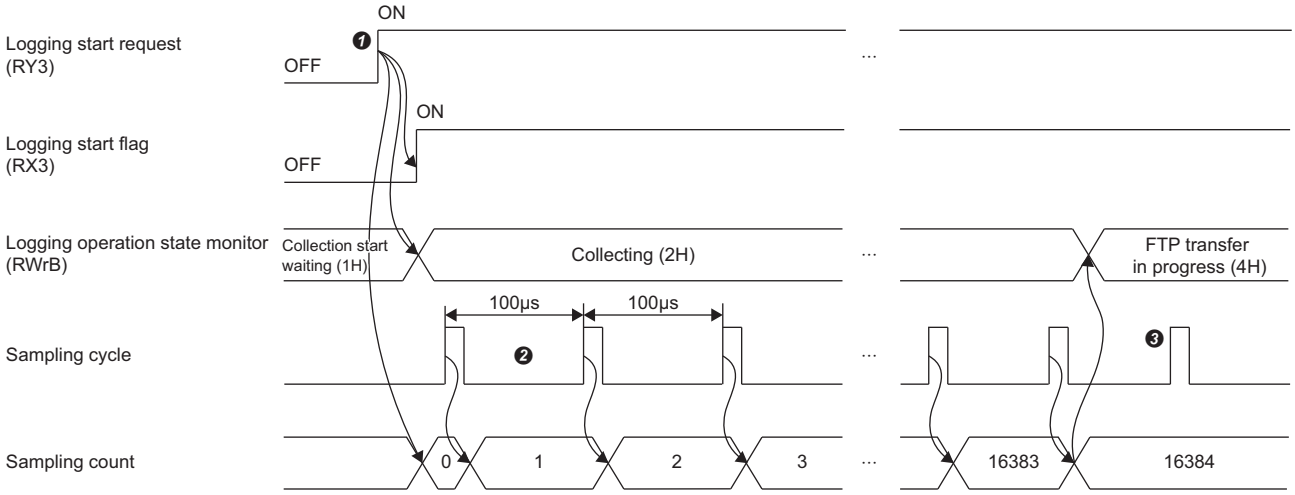
In this mode, sampling is performed only for the logging data size after logging has started. This is used when the logging period is clear before logging starts.



Ex.

Operation examples for when the following parameters are set are shown.

- "Logging function enable/disable": "Enable"
- "Logging operation mode setting": "Storage operation mode"
- "Buffer operation setting": "Linear buffer operation"
- "Select logging start control": "Register setting value (RY3)"
- "Select sampling pulses": "Logging cycle timing"
- "Logging cycle timing": "100µs"
- "Logging data size setting": "16384 records"



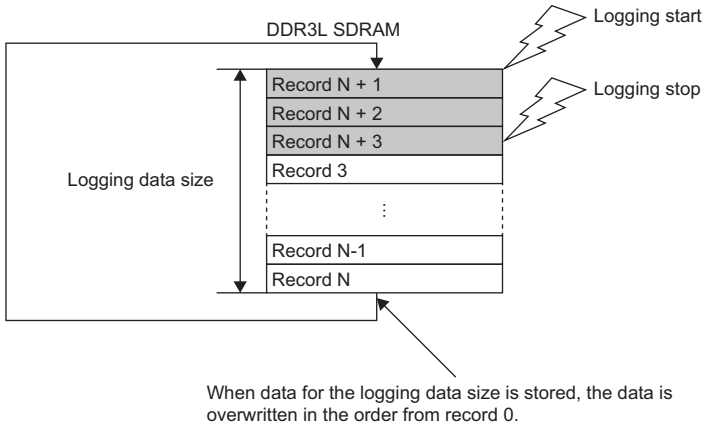
❶ Turn off and on Logging start request (RY3) at any time to start logging. When logging starts, the status of Logging operation state monitor (RWrB) becomes Collecting (2H) and Logging start flag (RX3) turns off and on.

❷ After logging starts, sampling takes place every "100µs", as was set for "Logging cycle timing".

❸ After a number of samples that meets the logging data size setting has been sampled, logging stops and Logging operation state monitor (RWrB) changes to FTP transfer in progress (4H).

Storage operation mode (ring buffer)

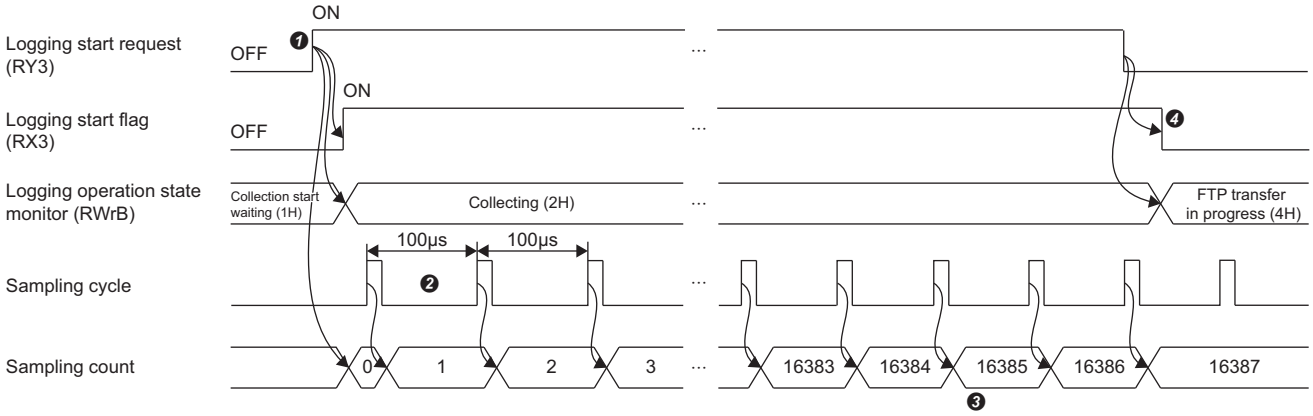
In this mode, sampling is performed until logging is stopped at an arbitrary timing after logging is started. This is used when the logging period is not clear before logging starts.



Ex.

Operation examples for when the following parameters are set are shown.

- "Logging function enable/disable": "Enable"
- "Logging operation mode setting": "Storage operation mode"
- "Buffer operation setting": "Ring buffer operation"
- "Select logging start control": "Register setting value (RY3)"
- "Select sampling pulses": "Logging cycle timing"
- "Logging cycle timing": "100μs"
- "Logging data size setting": "16384 records"



❶ Turn off and on Logging start request (RY3) at any time to start logging. When logging starts, the status of Logging operation state monitor (RWrB) becomes Collecting (2H) and Logging start flag (RX3) turns off and on.

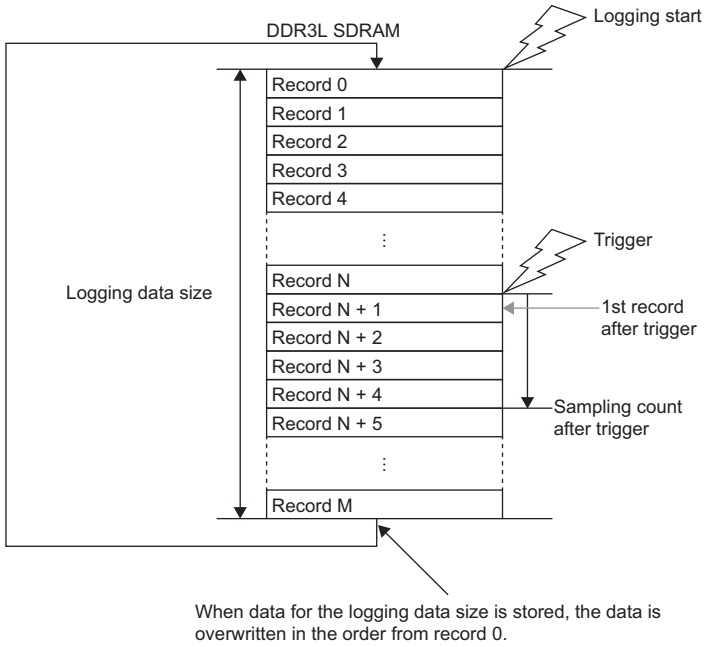
❷ After logging starts, sampling takes place every "100μs", as was set for "Logging cycle timing".

❸ After sampling an amount equivalent to the logging data size setting, overwriting starts from the beginning of the logging area.

❹ Turn on and off Logging start request (RY3) at any time to stop logging. When logging stops, the status of Logging operation state monitor (RWrB) changes to FTP transfer in progress (4H) and Logging start flag (RX3) turns on and off.

Trigger operation mode (ring buffer)

In this mode logging stops when a trigger occurs after logging has started. It is used to check the circuit status before and after the trigger occurs. After a trigger is generated, logging stops after sampling for the "Set number of sampling after trigger".



Point

The user circuit part outputs the trigger to the logging part. In the sample circuit, logging control part end trigger signal selection (usr_wreg_092) (FPGA register address: 1000_B124H) can specify the output trigger signal.

Restriction

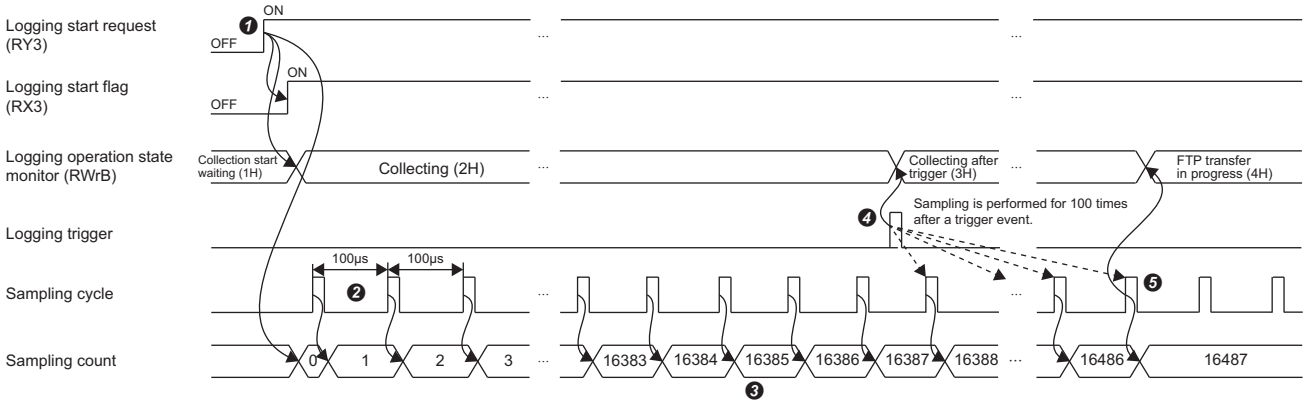
When inputting a trigger in the trigger operation mode (ring buffer), input one or more sampling pulses before inputting the trigger. If a trigger is input when the number of samples is 0 and logging is stopped while the status of Logging operation state monitor (RWrB) is Collecting after trigger (3H), the trigger generation record number is as follows.

- If the number of samples when logging stops is 0 or 1, the trigger occurrence record number will be -1 (invalid value).
- If the number of samples when logging stops is 2 or more, the trigger occurrence record number is 1.

Ex.

Operation examples for when the following parameters are set are shown.

- "Logging function enable/disable": "Enable"
- "Logging operation mode setting": "Trigger operation mode"
- "Select logging start control": "Register setting value (RY3)"
- "Select sampling pulses": "Logging cycle timing"
- "Logging cycle timing": "100μs"
- "Logging data size setting": "16384 records"
- "Set number of sampling after trigger": "100"



❶ Turn off and on Logging start request (RY3) at any time to start logging. When logging starts, the status of Logging operation state monitor (RWrB) becomes Collecting (2H) and Logging start flag (RX3) turns off and on.

❷ After logging starts, sampling takes place every "100μs", as was set for "Logging cycle timing".

❸ After sampling an amount equivalent to the logging data size setting, overwriting starts from the beginning of the logging area.

❹ If the rise of the trigger is input at any timing, Logging operation state monitor (RWrB) changes to Collecting after trigger (3H).

❺ Logging is performed for the number of sampling times after the trigger, and logging is stopped. When logging stops, Logging operation state monitor (RWrBH) changes to FTP transfer in progress (4H).

Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 98 FPGA parameters)

Operating procedure

1. Set whether to enable or disable the logging function in "Logging function enable/disable".

If set to "Disable", all parameters of the logging function will be disabled.

2. Set the logging operation mode in "Logging operation mode setting".

3. Set the buffer operation in the storage operation mode in "Buffer operation setting".

This setting is invalid when "Logging operation mode setting" is set to "Trigger operation mode". Buffer operation in "Trigger operation mode" is fixed to ring buffer operation.

4. Set the logging start method in "Select logging start control".

5. Set whether to use the logging cycle timing pulse or have the user circuit input the pulse as the timing pulse for sampling the logging data in "Select sampling pulses".

Restriction

When "Select sampling pulses" is set to "User circuit output", the sampling pulse interval from the user circuit needs to be 1μs or more.
If the sampling pulse interval is less than 1μs, logging data may not be sampled. In addition, the logging timing pulse error (error code: 1300H) is stored in Latest error code (RWr0), and Error status flag (RXA) turns on.
After the Logging timing pulse error (error code: 1300H) is output, until this error is cleared, another logging timing pulse error (error code: 1300H) will not be output even if a sampling pulse of less than 1μs is input.
After the error is cleared, if a sampling pulse of less than 1μs is input, a next error is output.

6. When "Logging cycle timing" is set for "Select sampling pulses" to "Logging cycle timing", set the cycle for sampling the data to be logged.

Logging cycle timing (tim_log_cyc) (FPGA register address: 1000_2200H) stores the value calculated by the following formula.

- Logging cycle timing (tim_log_cyc) (FPGA register address: 1000_2200H) = (set value - 1)×2 + 1

Ex.

When the setting value is 6μs

Logging cycle timing (tim_log_cyc) (FPGA register address: 1000_2200H) = (6-1) × 2 + 1 = 11

7. Set the size of the data to be logged to DDR3L SDRAM in "Logging data size setting".

8. Set the number of times logging data is to be sampled after a trigger in "Set number of sampling after trigger" when the trigger operation mode is used.

This setting is invalid if "Storage operation mode" is selected for the "Logging operation mode setting".

Set number of sampling after trigger is set in units of records.

The settable range of post-trigger sampling times is the range that satisfies the following conditions.

- Set number of sampling after trigger < number of records in logging data size setting

9. With the "Logging data time division setting", the logging data selection part mounted in the sample circuit can be set to time division mode or non-time division mode.

Point

- Since this is a setting for a module in the user circuit, it will not work if the logging control part of the sample circuit has been eliminated. Also, this parameter will not work if the logging control part of the sample circuit has been changed so that time division logging data generation is disabled.
- When the "Logging data time division setting" is set to "Time division mode", only binary format can be used as the file saving format of logging data.

Logging monitor

The remote register areas that can check the operating status of logging are shown below.

- Logging operation state monitor (RWrB) (☞ Page 486 Logging operation status monitor)
- Sampling count monitor (RWrC, RWrD) (☞ Page 487 Sampling count monitor)
- FTP transfer count monitor (RWrE) (☞ Page 487 FTP transfer count monitor)

Precautions

Time information is not saved in the FPGA module. The time information is initialized when the module power of the FPGA module is turned off and on. When using time information in standalone mode, set the time from the SLMP-compatible device after the FPGA module has started.

12.8 FTP Client Function

Transfers logging data collected in DDR3L SDRAM to the FTP server.

Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 98 FPGA parameters)

■Setting the transfer destination FTP server

Operating procedure

1. Set the IP address of the destination FTP server in "FTP server IP address".

Point

Set the FTP server IP address to the same IP address class as the FPGA module. Also, match the subnet mask setting with the subnet mask of the FPGA module.

2. Set the login name for the destination FTP server in "Login name".
3. Set the password for the destination FTP server in "Password".

Point

The connection method and connection port number are as follows.
Connection method: PORT
FTP server connection port number: 20, 21

4. Specify the path (ASCII) to the directory where the logging data file is to stored for "Directory path".

If the directory path is left blank, the logging data file will be transferred to the root directory of the FTP server.

Point

If the directory specified in the directory path does not exist when transferring logging data, FTP file generation abnormality (error code: 1403H) is stored in Latest error code (RWr0) and Error status flag (RXA) turns on. Specify the directory delimiter / or \ at the end of the directory path. If not specified, / is automatically added at the end.

Ex.

When saving to any folder on the FTP server

- Logging data file name: sample_20221031_171531_00000002.bin
- Directory path: /LOGGING/LOG1/
- Directory path and file name used for logging data transfer: /LOGGING/LOG1/sample_20221031_171531_00000002.bin

■Logging data file name setting

The basic file name of the logging data file name is a sequential 8-digit hexadecimal number. The number is the number of times the logging data was sent after the power of the FPGA module was turned on.

In addition to the basic file name, the date, time and character string can be appended. The file name can be specified arbitrarily within a range of up to 64 characters (including extensions and periods) by combining this information. An underscore (_) is added between each piece of information.

Item	Description
String	Any string of characters (ASCII) can be added. However, \ / : * ? < > | " cannot be used.
Date	Adds the date when the transfer started in YYYYMMDD format. • YYYY: Year (4 digits) • MM: Month (2 digits) • DD: Day (2 digits)
Time	Adds the time at the start of transfer in hhmmss format. • hh: Hour (2 digits) • mm: Minute (2 digits) • ss: Second (2 digits)

The extension is added according to the file saving format of the logging data.

- Binary format: bin
- CSV format: csv

Ex.

File name when saving in binary format with character string (sample), date and time added

sample_20221031_171530_00000001.bin

Operating procedure

1. Set whether to add the date, time, and character string to file name in "Logging data file name setting".
2. Set the character string to be added to the logging data file in "Logging data file character setting".

This setting is ignored if the current setting does not specify addition of a character string to the logging data file.

Point

A logging data file name (no extension).tmp is generated as a temporary file while the logging data file is being transferred. When transfer of the logging data is completed, the temporary file is deleted and a file with the name set in the logging data file name setting is generated.

Precautions

- During FTP transfer, if there is a file with the same file name as the file being transferred in the FTP server, the existing file is deleted and the logging data file transferred by FTP is created.
- If a cable disconnection or FTP server power failure occurs during file transfer, delete the logging data file name (extension None).tmp of the unnecessary temporary file left in the FTP server as necessary, and transfer the file again.

File saving format of logging data

When transferring logging data to an FTP server, the data can be converted to a CSV file before transfer.

Setting method

Use the FPGA Module Configuration Tool to set parameters. (☞ Page 95 Module parameters)

Operating procedure

1. Set "Logging data file storage type" to "Binary file" or "CSV Files".
2. Set the format of the output to CSV files in "CSV Format setting".

One CSV format setting is applied to 16 bits (32 bits when double word is selected) of logging data. The correspondence between the CSV Format setting and the logging data is shown below.

Setting name	Applicable range
CSV Format setting 0 (bit0~bit15)	User circuit logging data 1 bit to 16 bits
CSV Format setting 1 (bit16~bit31)	User circuit logging data 17 bits to 32 bits
CSV Format setting 2 (bit32~bit47)	User circuit logging data 33 bits to 48 bits
⋮	⋮
CSV Format setting 24 (bit384~bit399)	User circuit logging data 385 bits to 400 bits
CSV Format setting 25 (bit400~bit415)	User circuit logging data 401 bits to 416 bits
CSV Format setting 26 (bit416~bit431)	User circuit logging data 417 bits to 432 bits

Point

- When "Logging operation mode setting" is set to "Trigger operation mode", the trigger occurrence time can be checked.
- When"CSV Format setting☐" is set to "No setting", there will be no output to the CSV file. If all instances of "CSV Format setting☐" are set to "No setting", logging data will not be output to the CSV file, but the CSV file will be output. (☐: 0 to 26)
- When "CSV Format setting☐" is set to "Double Word [Signed], decimal format", "Double Word [Unsigned], decimal format", "Double Word [Unsigned], hexadecimal format", 32 bits is the applicable range. Therefore, "CSV format setting☐"+1 cannot be set. (☐: 0 to 25)

Binary format

Binary format is comprised of header information and record data.

For details on the record data when the file is saved in binary format, refer to the following.

☞ Page 331 Record details

Header information (256 bits)	Fixed to 0 (16 bits)
	Time division mode (16 bits)*1
	Sampling count (32 bits)
	Trigger occurrence record number (32 bits)
	Fixed to 0 (160 bits)
Record data	First record data (512 bits)
	⋮
	Last record data (512 bits)

*1 The time division enable/disable value in b0 of User circuit logging mode selection (usr_logmode_sel) (FPGA register address: 1000_A002H) is output.

■Header information in binary format

The header information in binary format is shown below.

Header information	Range
Time division mode	• 0: Non-Time division mode • 1: Time division mode
Number of samplings	1 to 4294967295
Trigger occurrence record number	• -1*1 • 0 to 524287

*1 If "Logging operation mode setting" is set to "Storage operation mode" or "Trigger operation mode" and logging is stopped before a trigger occurs, -1 is stored in the trigger position.

Point

In any of the following cases, -1 (invalid value) is stored in the trigger occurrence record number.

- When "Logging operation mode setting" is set to "Storage operation mode"
- If no trigger is input during logging
- When logging stops while no sampling pulse is input after a trigger is input during logging
- When a trigger is input when the number of samples is 0, logging is stopped while the status of Logging operation state monitor (RWrB) is Collecting after trigger (3H), and the number of samples when logging is stopped is 0 or 1

CSV format

The format of logging data saved in a CSV file is shown below.

(1)→	[LOGGING]	NZ2GN2S-D41_1	2	3	4						
(2)→	DATETIME[YYYY/MM/DD hh:mm:ss	us]	INDEX	BIT[1:0]	BIT[1:0]	BIT[1:0]	…	BIT[1:0]	…	USHORT[DEC.0]	TRIGGER[*]
(3)→	TIME	usec	INDEX	No.0 bit0	No.0 bit1	No.0 bit2	…	No.0 bit15	…	No.26 bit[0:15]	Trigger
	2021/9/21 14:15:00	443845	1	0	0	0	…	1	…	1	
	2021/9/21 14:15:00	443845	2	0	0	1	…	1	…	2	
(4)→	2021/9/21 14:15:00	443845	3	0	0	0	…	0	…	3	
	2021/9/21 14:15:00	443845	4	1	0	0	…	0	…	4	
	2021/9/21 14:15:00	443845	5	0	0	0	…	1	…	5	

No.	Row name	Column index	Column name	Description
(1)	File information	1st row	File type	Fixed characters are stored. [LOGGING]
		2nd row	Model information_file version	Fixed characters are stored. NZ2GN2S-D41_1
		3rd row	No. for data type information row	Contains a number pointing to the data type information row. Fixed value: 2
		4th row	No. for data name row	A number pointing to the data name row is stored. Fixed value: 3
		5th row	No. for data start row	Contains the starting number of the data row. Fixed value: 4
(2)	Data type information	1st row	Date column	Fixed characters are stored. DATETIME[YYYY/MM/DD hh:mm:ss
		2nd row	Microsecond string	Fixed characters are stored. us]
		3rd row	Index column	Fixed characters are stored. INDEX
		4th row or later	Data column	The data type of logging data is stored. Output format: Data type output character (☞ Page 345 Data type output character)
		Last row	Trigger occurrence information column	Fixed characters are stored. TRIGGER [(occurrence time string*2)]
(3)	Data name	1st row	Date column	Fixed characters are stored. TIME
		2nd row	Microsecond string	Fixed characters are stored. usec
		3rd row	Index column	Fixed characters are stored. INDEX
		4th row	Data column	The bit range according to the CSV format setting number and the CSV format setting is stored. Output format: CSV format setting number Bit range according to CSV Format setting
		Last row	Trigger occurrence information column	Fixed characters are stored. Trigger
(4)	Data	1st row	Date column*1	Stores date and time information. Output format: YYYY/MM/DD hh:mm:ss
		2nd row	Microsecond string*1	Times in milliseconds and microseconds are stored in terms of microseconds. Example: For 100ms200μs, 100200 is stored.
		3rd row	Index column	Stores the value of the index. Output format: Integer value
		4th row	Data column	Contains the value to be logged. Output format: Value according to the data type information row type
		Last row	Trigger occurrence information column	Information at the time of trigger occurrence is stored.

*1 If logging is performed under the following conditions, January 1, 1970 00:00:00 000000 microseconds will be stored when the FPGA module is powered on.
· Data link has never been established with the master station in CC-Link IE TSN communication mode.
· The time has not been set in standalone mode.

*2 [*] is output to the occurrence string.

Point

Trend graphs (signal waveforms) of the CSV files output by this function can be checked using GX LogViewer. The FPGA module can output 32 or more logging data strings to a CSV file, but GX LogViewer can simultaneously display 32 signals on the trend graph. If the signal to be observed is not displayed in the GX LogViewer trend graph, specify the display target using GX LogViewer, or set CSV Format setting to Do not output (0) to create a CSV file whose output volume of logging data is reduced.

■Data type output character

The correspondence between the data type specified in CSV Format setting and the data type output characters in the CSV file is shown below.

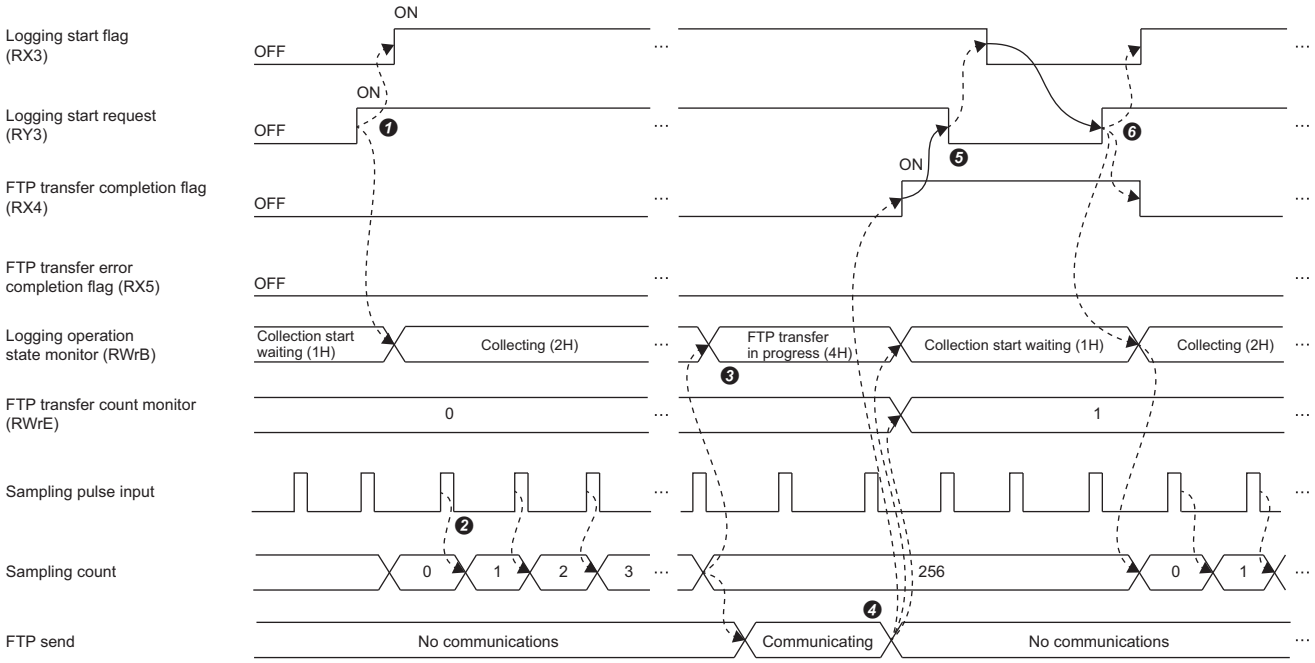
Data type	Output type	Output Content
Bit	Binary format	BIT[1;0]
Word [Signed]	Decimal format	SHORT[DEC.0]
Word [unsigned]	Decimal format	USHORT[DEC.0]
Word [unsigned]	Hexadecimal format	USHORT[HEX.0]
Double word [Signed]	Decimal format	LONG[DEC.0]
Double word (unsigned)	Decimal format	ULONG[DEC.0]
Double word (unsigned)	Hexadecimal format	ULONG[HEX.0]

Operation example

An operation example of the FTP client function is shown.

Logging data transfer

When "Select logging start control" is "Register setting value (RY3)", the control for transferring logging data after sampling is completed of 256 points is shown below.



Implemented in FPGA module

Executed by the program.

❶ Turn off and on Logging start request (RY3) at any time to start logging. When logging starts, the status of Logging operation state monitor (RWrB) becomes Collecting (2H), and Logging start flag (RX3) turns off and on.

❷ Sampling is performed after logging starts.

❸ Logging data collection is completed when sampling is performed for the logging data size setting. After that, logging data transfer to the FTP server starts, and the status of Logging operation state monitor (RWrB) becomes FTP transfer in progress (4H).

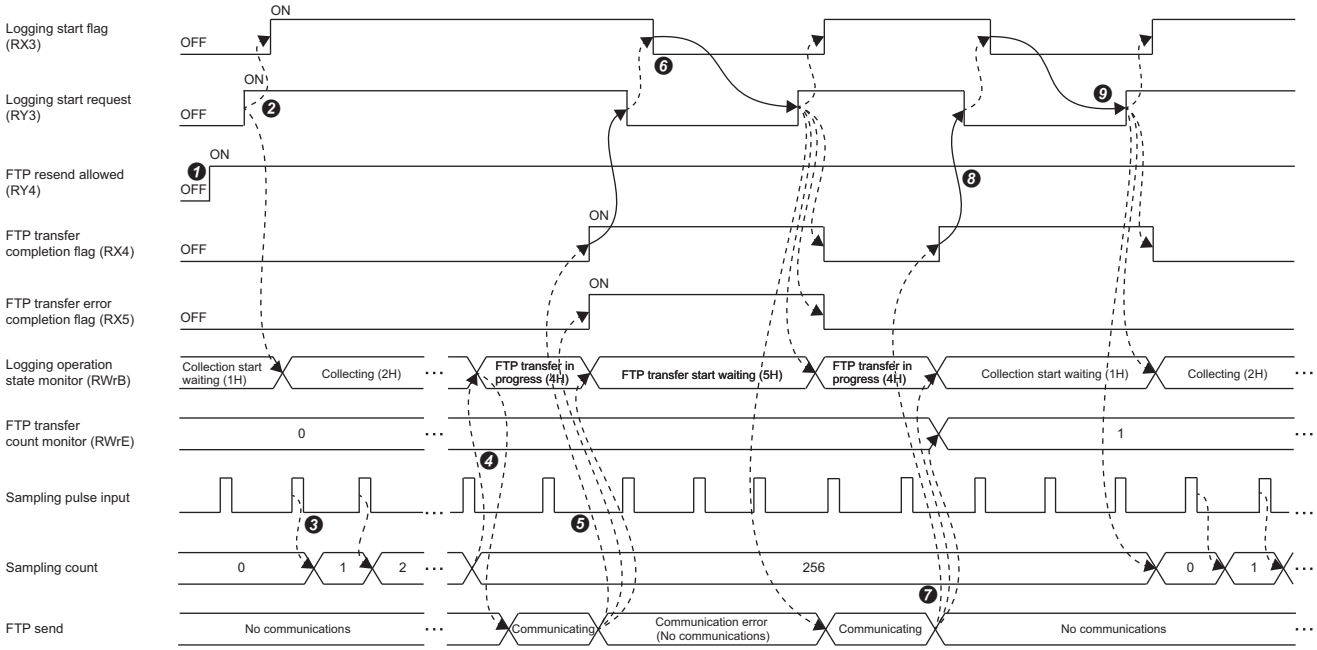
❹ When the logging data transfer to the FTP server is completed successfully, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H). While FTP transfer error completion flag (RX5) is off, FTP transfer completion flag (RX4) is turned from off to on. Also, the FTP transfer count monitor (RWrE) is incremented.

❺ When Logging start request (RY3) is turned on and off by the program, Logging start flag (RX3) turns on and off.

❻ Turn off and on the logging start request (RY3) to restart logging. If FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are on at this timing, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off.

Resend logging data

The following shows how to transfer logging data again when logging data transfer is stopped due to FTP communication error or other cause when "Select logging start control" is "Register setting value (RY3)".



- - - - - - - - - ▶ Implemented in FPGA module

——————▶ Executed by the program.

❶ If the logging data transfer fails and the logging data transfer is to be restarted from the beginning, turn on FTP resend allowed (RY4) before starting logging data collection.

❷ Turn off and on Logging start request (RY3) at any time to start collecting logging data. When collection starts, the status of Logging operation state monitor (RWrB) becomes Collecting (2H) and Logging start flag (RX3) turns off and on.

❸ Sampling is performed after logging starts.

❹ Logging data collection is completed when sampling is performed for the logging data size setting. After that, the transfer of logging data to the FTP server starts, and the status of Logging operation state monitor (RWrB) becomes FTP transferring (4H).

❺ If an error occurs in FTP communication while FTP resend allowed (RY4) is on during logging data transfer, the status of Logging operation state monitor (RWrB) becomes FTP transfer start waiting (5H), and FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned from off to on. *1

❻ If Logging start request (RY3) is turned from off to on at any time by the program, the transfer of logging data is restarted from the beginning. When the request is accepted, Logging start flag (RX3) turns off and on and the status of Logging operation state monitor (RWrB) becomes FTP transfer in progress (4H). Also, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off.

❼ When the logging data transfer to the FTP server is completed successfully, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H). While FTP transfer error completion flag (RX5) is off, FTP transfer completion flag (RX4) is turned from off to on. Also, the FTP transfer count monitor (RWrE) is incremented.

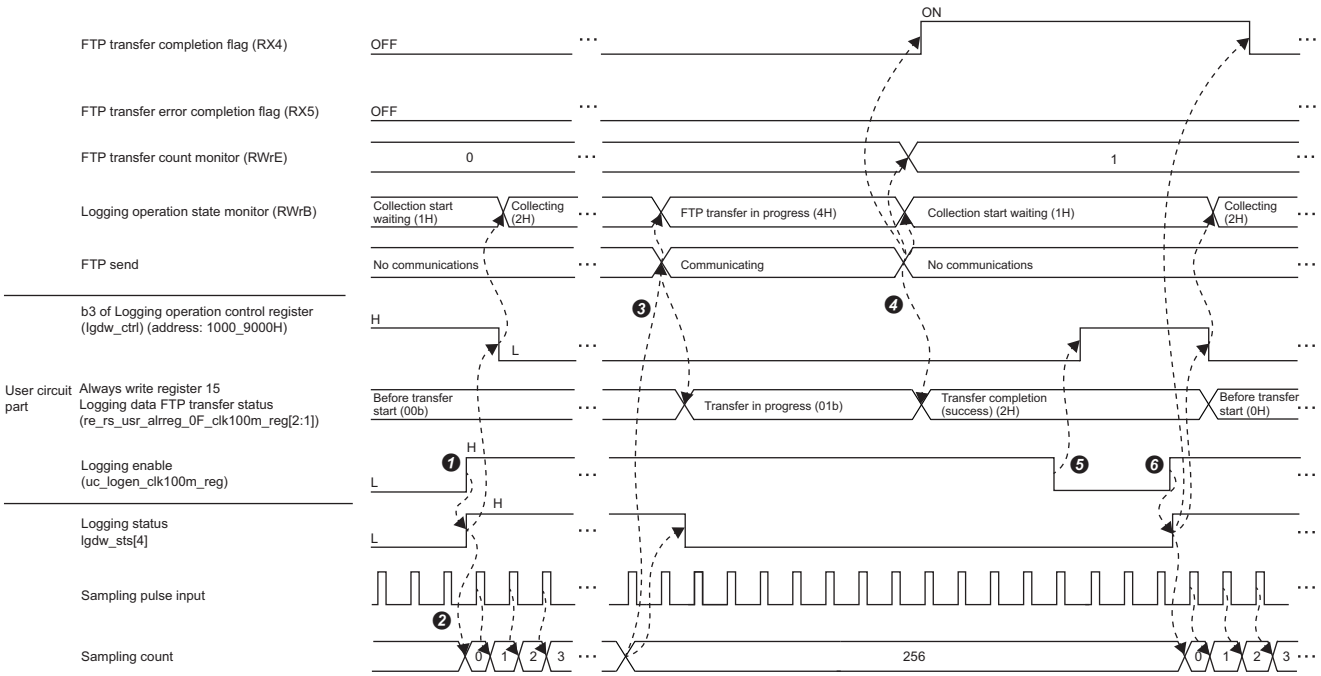
❽ When Logging start request (RY3) is turned on and off by the program, Logging start flag (RX3) turns on and off.

❾ Turn off and on the logging start request (RY3) to restart logging. If FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are on at this timing, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off.

*1 If an error occurs in FTP communication while FTP resend allowed (RY4) is off during logging data transfer, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H), and FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) turn off and on.

Logging data transfer using sample circuit

The following shows the control for transferring logging data after sampling completion of 256 points when "Select logging start control" is "User circuit output".



- - - - - - - - ▶ Implemented in FPGA module

——————▶ Executed by the program.

❶ When b3 of Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Rising for logging start allowed (1), enable (1) Logging enable (uc_logen_clk100m_reg) from the user circuit part at any timing.

❷ The logging unit writes logging data to DDR3L SDRAM for each sampling pulse.

❸ After the completion of logging for the logging data size setting, logging data transfer to the FTP server starts. At that time, the status of Logging operation state monitor (RWrB) becomes FTP transfer in progress (4H), and the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) becomes Transfer in progress (1H).

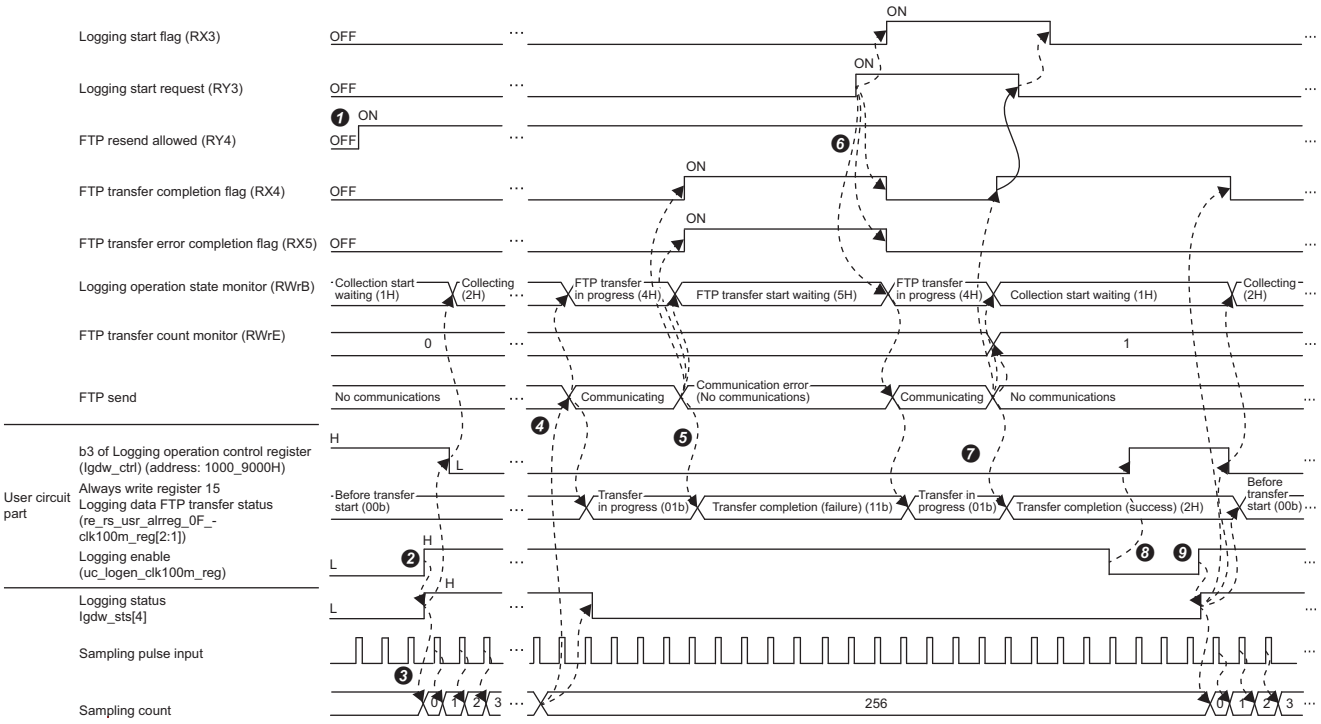
❹ When the logging data transfer to the FTP server completed successfully, the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) changes to Transfer completed (success) (2H). Also, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1), FTP transfer error completion flag (RX5) is off, FTP transfer completion flag (RX4) is turned from off to on, and FTP transfer count monitor (RWrE) is incremented.

❺ When b3 of Logging operation control register (lgdw_ctrl) is Falling for logging start allowed (0), disable Logging enable (uc_logen_clk100m_reg) from the user circuit part at any timing. Rising for logging start allowed (1) is set to b3 of Logging operation control register (lgdw_ctrl).

❻ When b3 of Logging operation control register (lgdw_ctrl) is Rising for logging start allowed (1), logging can be started again by enabling (1) Logging enable (uc_logen_clk100m_reg) from the user circuit part at any timing. At this timing, for the FPGA module, the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) changes to Before transfer start (0H), and if FTP transfer completion flag (RX4) is on, FTP transfer completion flag (RX4) is turned off.

Logging data retransmission using sample circuit

The figure below shows the control for transferring logging data again in the following situation: When "Select logging start control" is "User circuit output", the transfer of logging data is stopped due to a communication error after sampling 256 points.



Implemented in FPGA module

Executed by the program.

❶ If the logging data transfer fails and the logging data transfer is to be restarted from the beginning, turn on FTP resend allowed (RY4) before starting logging data collection.

❷ When b3 of Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Rising for logging start allowed (1), enable (1) Logging enable (uc_logen_clk100m_reg) from the user circuit part at any timing.

❸ The logging unit writes logging data to DDR3L SDRAM for each sampling pulse.

❹ After completion of logging for the logging data size setting, logging data transfer to the FTP server is started. At that time, the status of Logging operation state monitor (RWrB) becomes FTP transfer in progress (4H), and the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) becomes Transfer in progress (1H).

❺ If an error occurs in FTP communication while FTP resend allowed (RY4) is on during logging data transfer, the status of Logging operation state monitor (RWrB) becomes FTP transfer start waiting (5H) and the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) becomes Transfer completed (failure) (3H). Also, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off and on. *1

❻ If Logging start request (RY3) is turned from off to on at any time by the program, the transfer of logging data is restarted from the beginning. When the request is accepted, Logging start flag (RX3) turns from off to on, the status of Logging operation state monitor (RWrB) changes to FTP transfer in progress (4H), and the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) becomes Transfer in progress (1H). Also, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off.

❼ When the transfer of logging data to the FTP server completes successfully, the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) changes to Transfer completed (success) (2H). Also, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H), FTP transfer error completion flag (RX5) is off, FTP transfer completion flag (RX4) is turned from off to on, and FTP transfer count monitor (RWrE) is incremented.

❽ When b3 of Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Falling for logging start allowed (0), disable (0) Logging enable (uc_logen_clk100m_reg) from the user circuit at any timing. Logging operation control register (lgdw_ctrl) (address: 1000_9000H) b3 is logging start rising enable (1).

❾ When b3 of Logging operation control register (lgdw_ctrl) (address: 1000_9000H) is Rising for logging start allowed (1), logging can be started again by enabling (1) Logging enable (uc_logen_clk100m_reg) from the user circuit part at any timing. At this timing, for the FPGA module, the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) changes to Before transfer start (0H). If FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned on, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off.

*1 If an error occurs in FTP communication while FTP resend allowed (RY4) is off during logging data transfer, the status of Logging operation state monitor (RWrB) becomes Collection start waiting (1H) and the status of Always write register 15 logging data FTP transfer status (re_rs_usr_alwreg_0F_clk100m_reg[2:1]) becomes Transfer completed (failure) (3H). Also, FTP transfer completion flag (RX4) and FTP transfer error completion flag (RX5) are turned off and on.

Precautions

Set the interval from the start of logging data file transfer to the start of the next transfer to 3 seconds or more. An FTP communication error may occur if logging data files are transferred at intervals of less than 3 seconds.
If an FTP communication error occurs, FTP open abnormality (error code: 1401) is stored to Latest error code (RWr0) and Error status flag (RXA) turns on.

12.9 SLMP Communication Function

SLMP can be used to communicate with the FPGA module.

For details on SLMP, refer to the following.

SLMP Reference Manual

Applicable commands

SLMP commands*1				Description
Type	Operation	Command	Subcommand	
Remote Control	Remote Reset	1006H	0000H	Execute a remote RESET to the FPGA module.
Clear Error		1617H	0000H	Initializes the error code of the FPGA module and turns off the ERR. LED.
Device	Read	0401H	0000H	Reads the device of the FPGA module in word units. For the correspondence between the device code and the device of the FPGA module, refer to the following. ☞ Page 351 Correspondence between device code and FPGA unit device
			0001H	Reads the device of the FPGA module bit by bit. For the correspondence between the device code and the device of the FPGA module, refer to the following. ☞ Page 351 Correspondence between device code and FPGA unit device
	Write	1401H	0000H	Writes the device of the FPGA module word by word. For the correspondence between the device code and the device of the FPGA module, refer to the following. ☞ Page 351 Correspondence between device code and FPGA unit device
			0001H	Write the FPGA module device bit by bit. For the correspondence between the device code and the device of the FPGA module, refer to the following. ☞ Page 351 Correspondence between device code and FPGA unit device
Memory	Read	0613H	0000H	Read the remote buffer memory.
	Write	1613H	0000H	Write to the remote buffer memory.

*1 3E frame, 4E frame, and station number extension frame are supported.

Point

- Do not execute multiple SLMP commands simultaneously for one FPGA module. When using multiple SLMP commands, send the next command after receiving the response message from the FPGA module. If multiple SLMP commands are executed at the same time, the FPGA module may be unable to receive the SLMP commands, and the SLMP commands may time out.
- When connecting multiple communication devices (such as the GOT and FPGA Module Configuration Tool) to the FPGA module, actually communicate and adjust the execution interval so as to allow some leeway. If the FPGA module cannot receive SLMP commands, an error such as timeout may occur.

■Correspondence between device code and FPGA unit device

○: Available, ×: Not available

Device code	Device number	FPGA module		Supported devices for the Device Read command		Device Write command compatible devices	
		Device	Address	Word unit read	Bitwise read	Word unit write	Bitwise write
Input (X)	0 to 6F	Remote input (RX)	RX0 to RX6F	○*1	○	×	×
Output (Y)	0 to 6F	Remote output (RY)	RY0 to RY6F	○*1	○	○*1*2	○
Link register (W)	0 to 8F	Remote register (RWr)	RWr0 to RWr8F	○	×	×	×
	100 to 18F	Remote register (RWw)	RWw0 to RWw8F	○	×	○*2	×
Data register (D)	0 to FFFFH*3	Remote buffer memory	0 to FFFFH*3	○	×	○	×

*1 Specify the start device number of input (X) and output (Y) in units of words (16 points). If it is not specified in word units, an error response will be returned.

*2 Returns an abnormal response in CC-Link IE TSN communication mode.

*3 For the addresses that can be accessed in the remote buffer memory, refer to the following.
☞ Page 488 Remote Buffer Memory

Communications settings

When communicating with the FPGA module via SLMP, use the following.

- TCP/UDP: UDP
- Port: 45239
- Code: binary code

Usage method

Use the SLMPSND instruction to send SLMP commands to the FPGA module from the CPU module.

For details on the SLMPSND command, refer to the following.

MELSEC iQ-R Programming Manual (Module Dedicated Instructions)

SLMP communications end code

If the FPGA module detects an SLMP command error, it returns an error response, but the FPGA module does not enter error status. The error code is stored in the end code of the abnormal response data.

End code	Description and cause	Action
C059H	There is an error in the command or subcommand specification.	Review the command/subcommand and resend it.
C05CH	There is an error in the specification of the requested content.	Review the request and resend it.
C061H	The requested data length does not match the number of data.	Review the content and length of the request data, and resend it.
CF44H	The request destination does not support splitting.	The FPGA module does not support splitting. Send the request message without splitting it.

Precautions

Do not use prohibited areas of link devices and remote buffers. Doing so may cause an accident due to malfunction or incorrect output.

12.10 CC-Link IE TSN Network Synchronous Communication Function

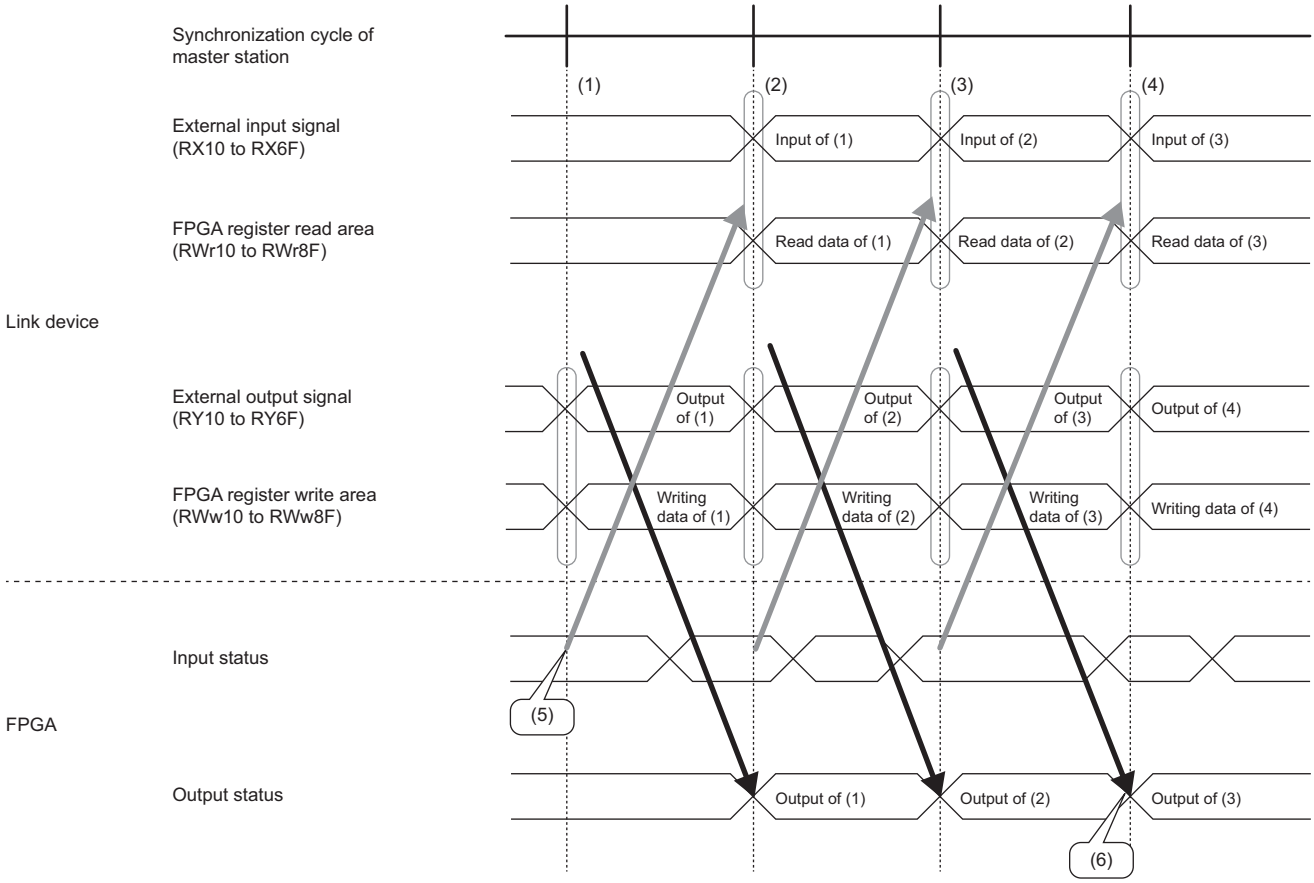
Reads and writes to the FPGA at the synchronous cycle of a master station that supports the CC-Link IE TSN network synchronous communication function.
This enables an A/D converter module to operate at the same timing as other remote stations on the same network.

Applicable version

When using the CC-Link IE TSN network synchronous communication function, check the version of the master station.
📖 User's manual for the master station used

Operation

Reads and writes to the register areas of the FPGA standard circuit and user circuit for each synchronization cycle of the master station. The value read from the FPGA is sent to the master station at the next synchronization cycle.
Also, the value to be written to the FPGA register received from the master station is written to the FPGA at the timing of the next synchronization cycle.



(5) Transmit the FPGA input value in the previous synchronization cycle.
(6) Write the output value received in the previous synchronization cycle to the FPGA.

Setting method

Calculate synchronization cycles from the formula below.

Synchronization cycle = Basic period (Communication period interval setting) × Magnification

Item	Description
Basic period (Communication period interval setting)	Setting values of the communication period interval setting of master station parameters
Magnification	Magnification that is determined by the following master station parameters • Setting values of the communication period setting for network configuration setting • Setting values of the multiple period setting for master station parameters

Set the synchronization cycle to satisfy the following condition.

1ms ≤ Synchronization cycle ≤ 1000.00ms

Set the basic period setting for master station parameters to satisfy the following conditions.

■Condition 1

Set the basic period (communication period interval setting) so that it matches the inter-module synchronous fixed scan interval setting.

■Condition 2

Configure the setting so that the transient transmission time satisfies the setting range shown below.

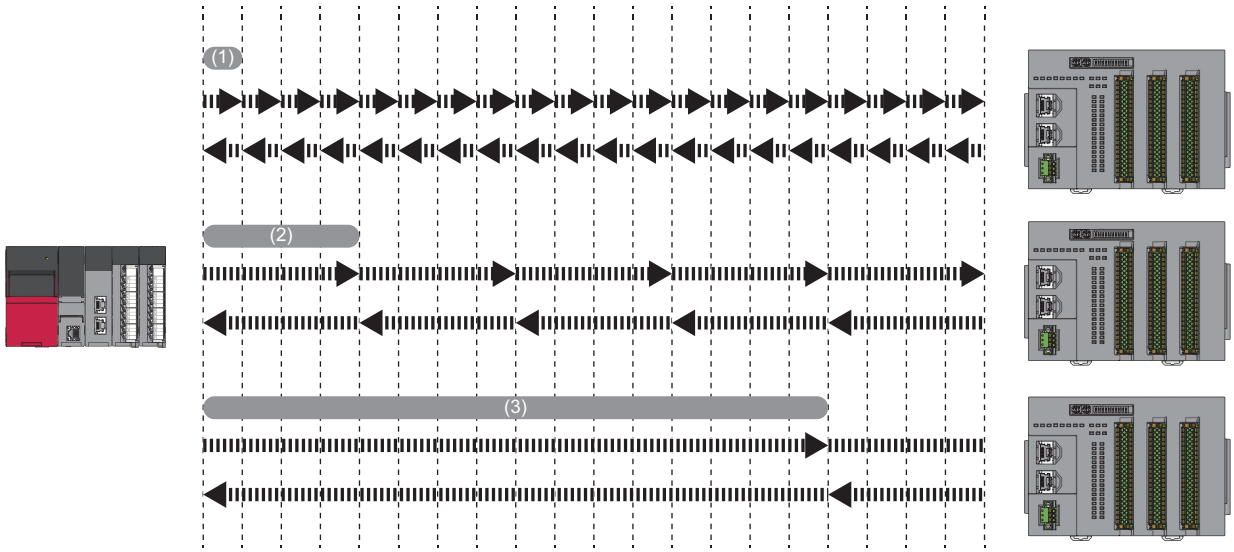
Communication speed		Value that can be set for the transient transmission time
Master station	FPGA module	
1Gbps	1Gbps	350μs or more
	100Mbps*1	22μs or more
100Mbps	100Mbps	350μs or more

*1 Use a TN HUB when communicating between Master station and FPGA module with different communication speeds.

For the setting procedure, refer to the manual for the master station being used.

Ex.

The following figure shows an example of a synchronization cycle.



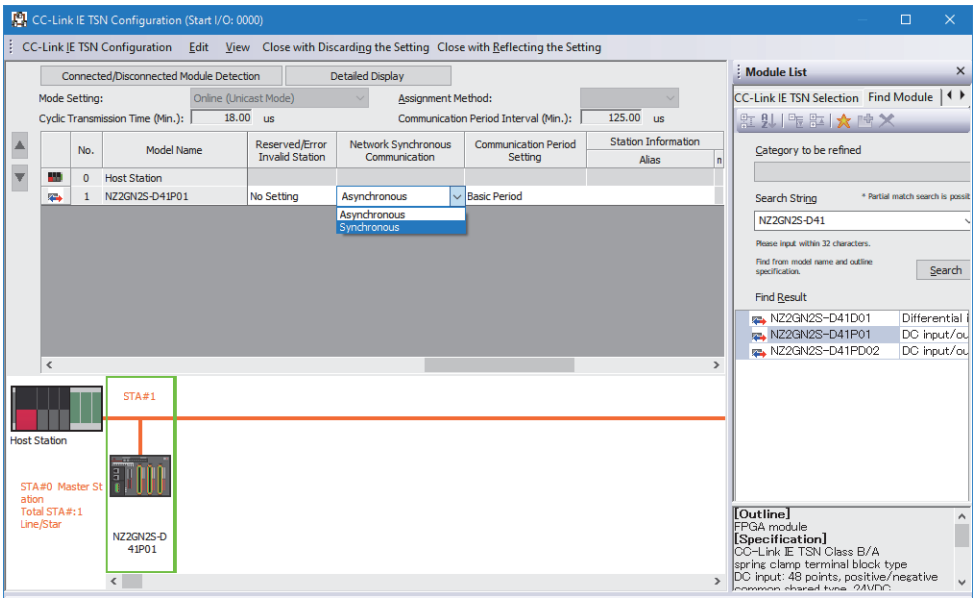
(1) Basic period
(2) Normal speed
(3) Low speed

Operating procedure

1. Display the "CC-Link IE TSN Configuration" window.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ Model ⇨ [Basic Setting] ⇨ [Network Configuration Settings]

2. Set "Network Synchronous Communication" to "Synchronous".



Point

- To use the CC-Link IE TSN network synchronous communication function for the FPGA module, enable the CC-Link IE TSN network synchronous communication function of the master station. For details, refer to the manual for the master station used.
- When the FPGA module is turned on, the setting of whether to use the CC-Link IE TSN network synchronous communication function (Synchronous/Asynchronous) cannot be changed.

Restrictions

This section describes restrictions to use the CC-Link IE TSN Network synchronous communication function.

■Restrictions on inter-module synchronous fixed scan interval setting

When "0.05ms Unit Setting" for "Fixed Scan Interval Setting of Inter-module Synchronization" of "System Parameter" is set to "Not Set", the CC-Link IE TSN network synchronous communication function cannot be used.

■CC-Link IE TSN Class restrictions

When "0.05ms Unit Setting" for "Fixed Scan Interval Setting of Inter-module Synchronization" of "System Parameter" is set to "Not Set", the CC-Link IE TSN network synchronous communication function cannot be used.

When the CC-Link IE TSN Class is CC-Link IE TSN Class A, event code 00C71H is recorded in the event history of the master station, and the FPGA module does not establish a data link.

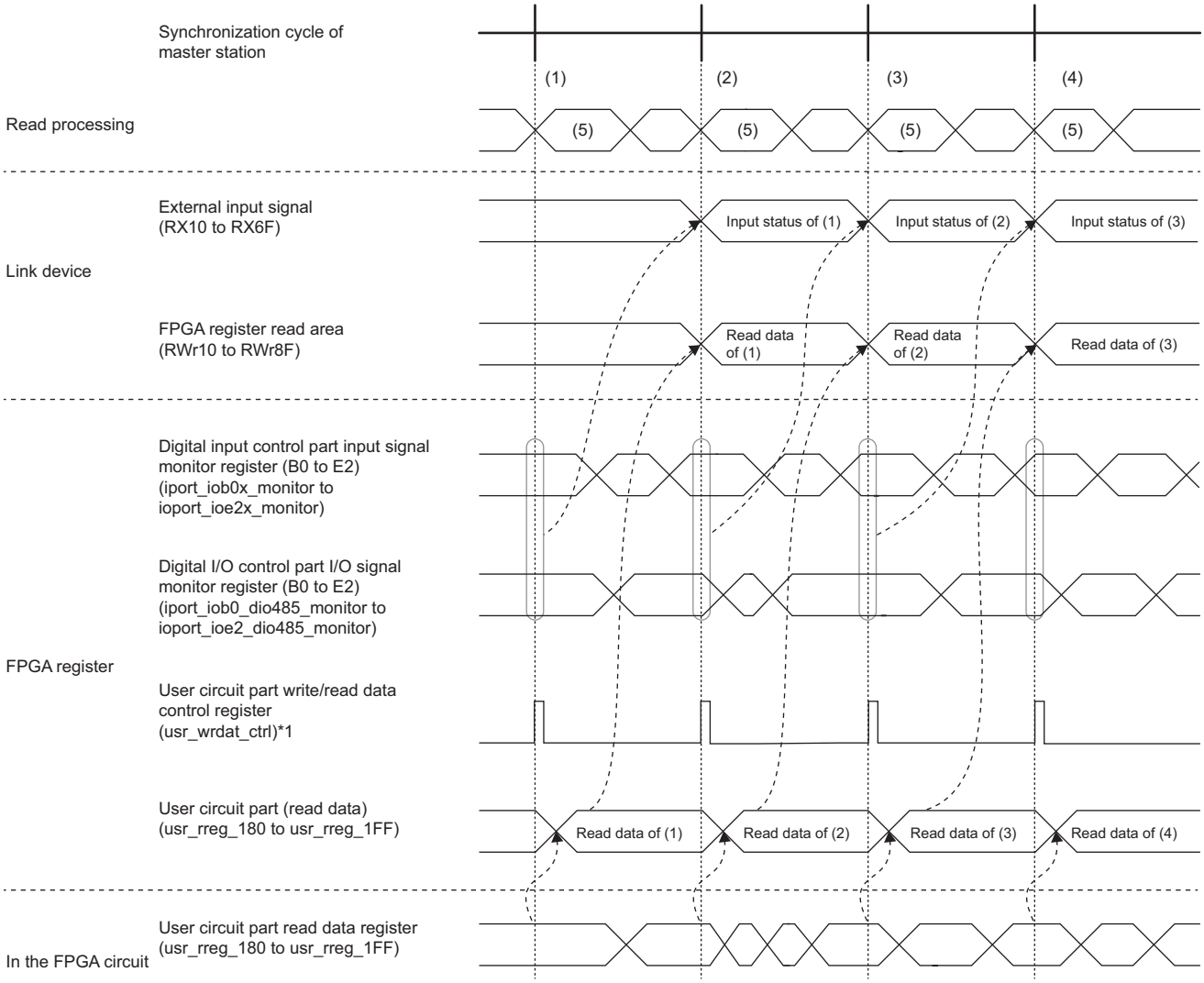
For details on the CC-Link IE TSN Class setting method, refer to the following.

☞ Page 58 Setting the function setting switches

Timing chart

■Read

The FPGA status is read at the timing of the synchronization cycle and sent to the master station at the next synchronization cycle.

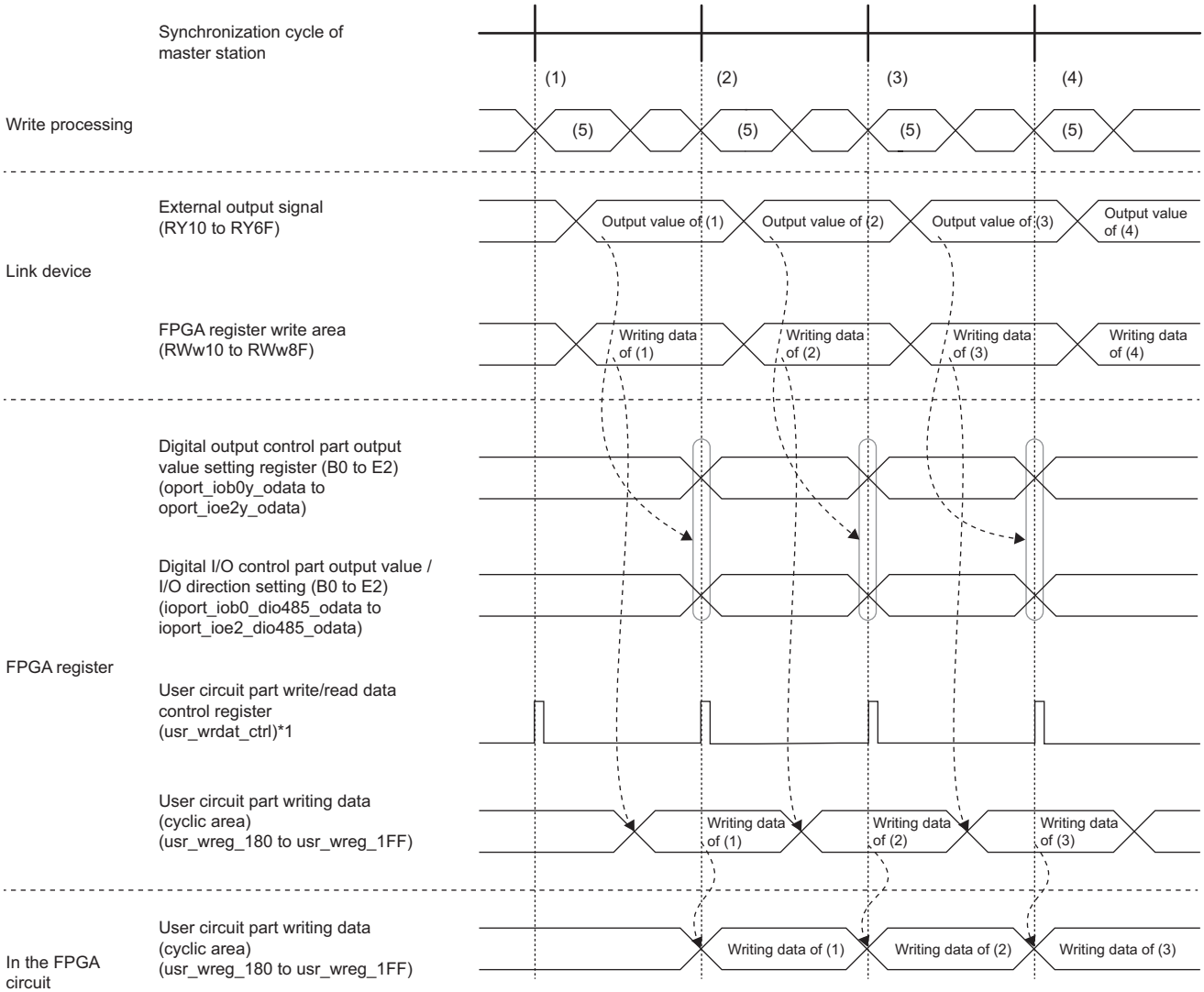


(5) Read processing

*1 Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) is controlled for each synchronization cycle, and the reading data of FPGA status (cyclic area) (usr_rreg_180 to usr_rreg_1FF) is read to (FPGA register addresses: 1000_BB00H to 1000_BBFFH).

■Write

The value to be written to the FPGA register is received at the timing of the synchronization cycle, and written to the FPGA at the timing of the next synchronization cycle.

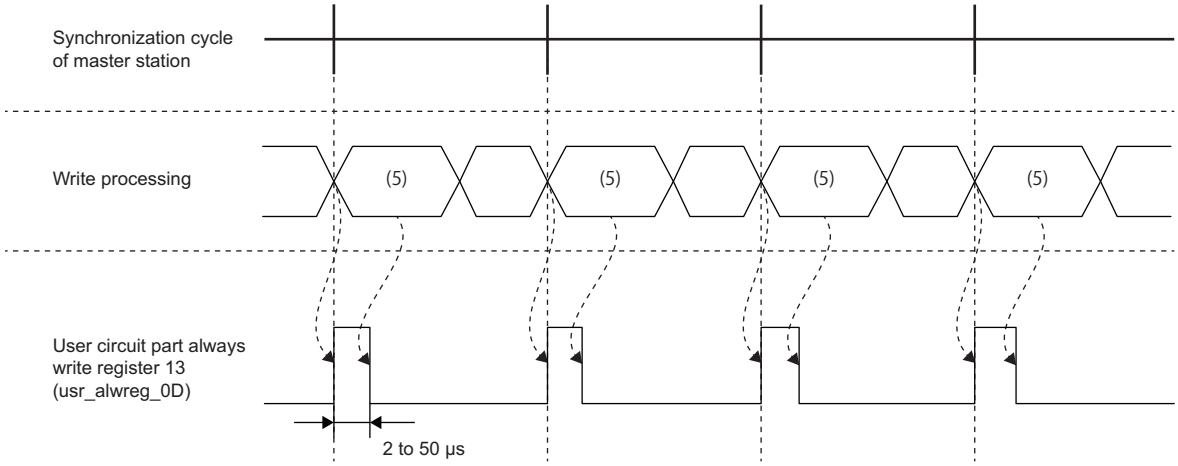


(5) Write processing

*1 Write/read data control register (usr_wrdat_ctrl) (FPGA register address: 1000_A000H) is controlled for each synchronization cycle, and the writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF) (FPGA register addresses: 1000_B300H to 1000_B3FEH) are reflected in the FPGA.

■Synchronization signal to FPGA

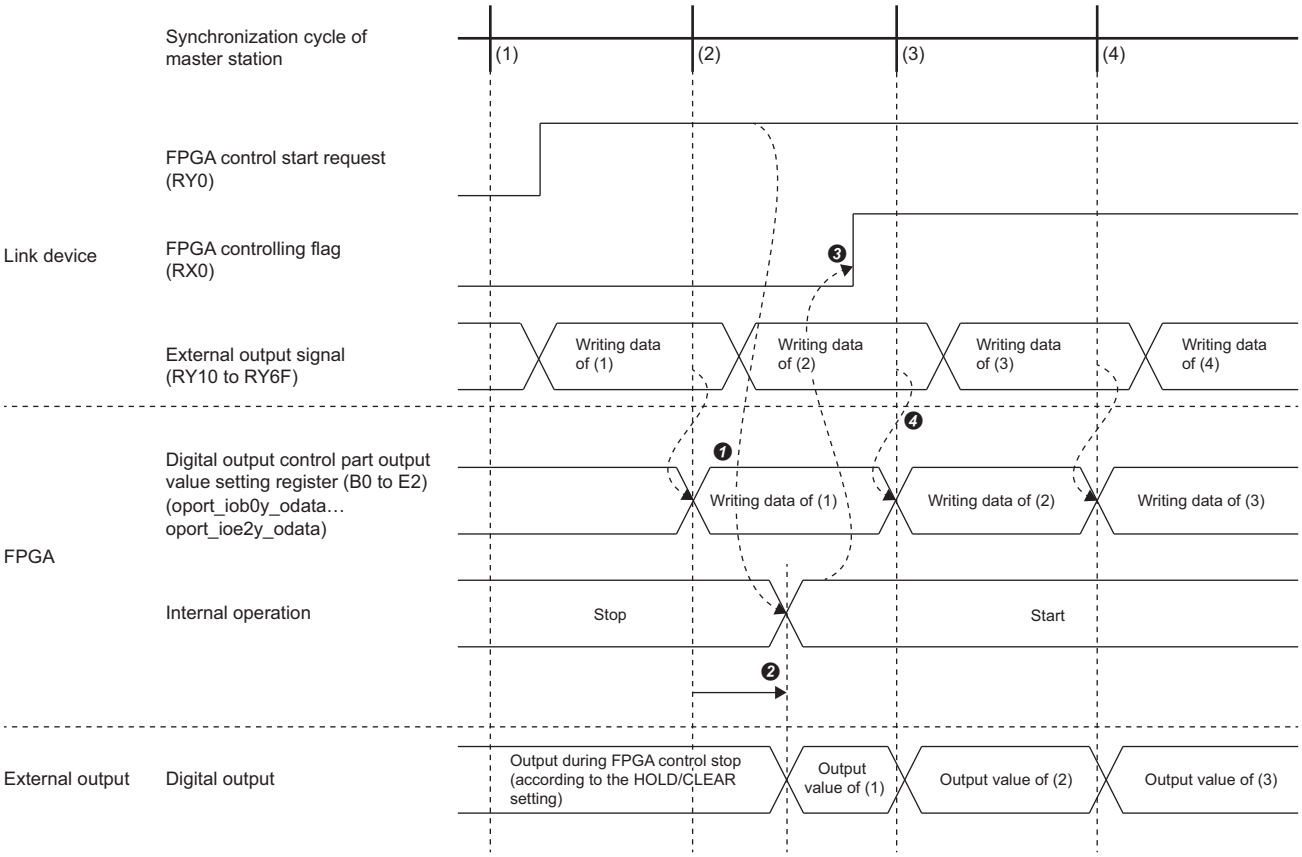
At the timing of the synchronization cycle, Always write register 13 (usr_alwreg_0D) (FPGA register address: 1000_A02AH) is stored with sync signal (1). Always write register 13 (usr_alwreg_0D) (FPGA register address: 1000_A02AH) allows for creation of a user circuit that operates at the synchronization cycle timing.



(5) Write processing

■Starting FPGA control

The start of FPGA control by turning on FPGA control start request (RY0) is accomplished after the external output signals (RY10 to RY6F) have been stored to Output value setting (B0) (oport_iob0y_odata) (FPGA register address: 1000_4010H) to Output value setting (E2) (oport_ioe2y_odata) (FPGA register address: 1000_401CH).



----------▶ Implemented in FPGA module

❶ The external output signals (RY10 to RY6F) of the synchronous cycle received in (1) are sent to the Output value setting (B0) (oport_iob0y_odata) (FPGA register address: 1000_4010H) to Output value setting (E2) (oport_ioe2y_odata) (FPGA register address: 1000_401CH).

❷ By turning off and on FPGA control start request (RY0) received in (1), the start processing of FPGA control is performed. FPGA internal operation start/stop from synchronous cycle (mode_ctrl2) (FPGA register address: 1000_0002H) to start (1) varies depending on the communication status, number of link devices, and FPGA parameter settings.

❸ When FPGA control start processing is completed, FPGA control flag (RX0) is turned off and on.

❹ The external output signals (RY10 to RY6F) are updated at each synchronous cycle by Output value setting (B0) (oport_iob0y_odata) (FPGA register address: 1000_4010H) to Output value setting (E2) (oport_ioe2y_odata) (FPGA register address: 1000_401CH). If Output signal selection (B0) (oport_iob0y_osel) (FPGA register address: 1000_4000H) to Output signal selection (E2) (oport_ioe2y_osel) (FPGA register address: 1000_400CH) have been set to the register setting value (oport_iob0y_odata: RY) (0), the external output is turned on/off according to the on/off of the external output signals (RY10 to RY6F).

12.11 Module Power Supply Voltage Drop Detection Function

This function detects a voltage drop of the module power supply.
This function makes troubleshooting easy when the voltage of power supplied to the FPGA module drops or when poor connection in the wiring occurs. Note that the voltage to be monitored for a module power supply voltage drop is 20.4V.

Operation

If a drop in the voltage of the module power supply is detected, the module enters the following state and an error is notified.

- The module power supply voltage drop error (error code: 1080H or 1081H) is stored in Latest error code (RWr0).
- Error flag (RXA) turns on.

Point

- When an error is detected, since the power supply environment is out of specification range, the operation is not guaranteed.
- A power supply voltage drop is not detected in the event of a sudden power failure or when power-off operation is performed.
- The voltage to be monitored varies depending on the environment.

12.12 Firmware Update Function

Updates the FPGA module firmware via CC-Link IE TSN.

Update firmware by using the CC-Link IE TSN Firmware Update Tool.

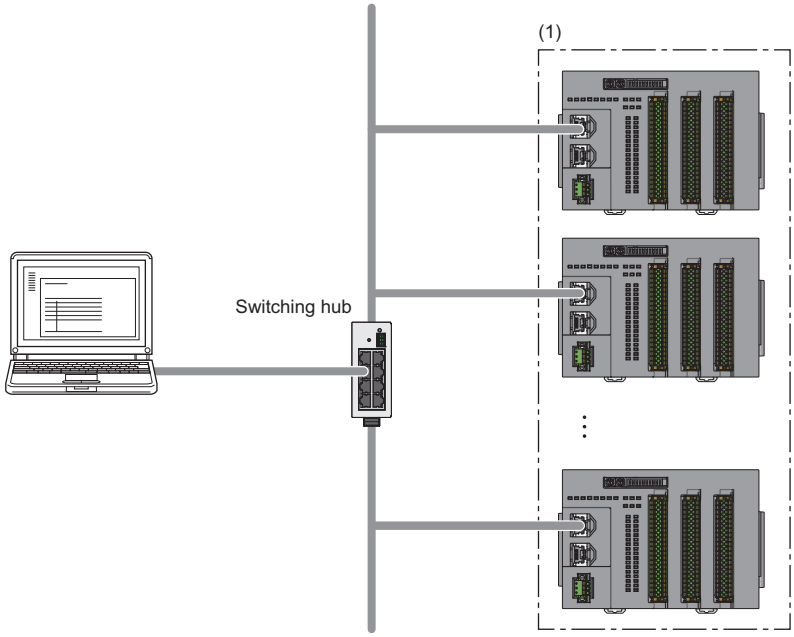
When the CC-Link IE TSN Firmware Update Tool is necessary, please consult your local Mitsubishi representative.

Restriction

The firmware update function cannot be used when using the CC-Link IE TSN network synchronous communication function.

System configuration

Connect a personal computer and the FPGA modules that are the firmware update targets with an Ethernet cable.



(1) FPGA module for firmware update

Firmware update file

When the firmware update file is necessary, please consult your local Mitsubishi representative.

The file name of firmware update file is listed below.

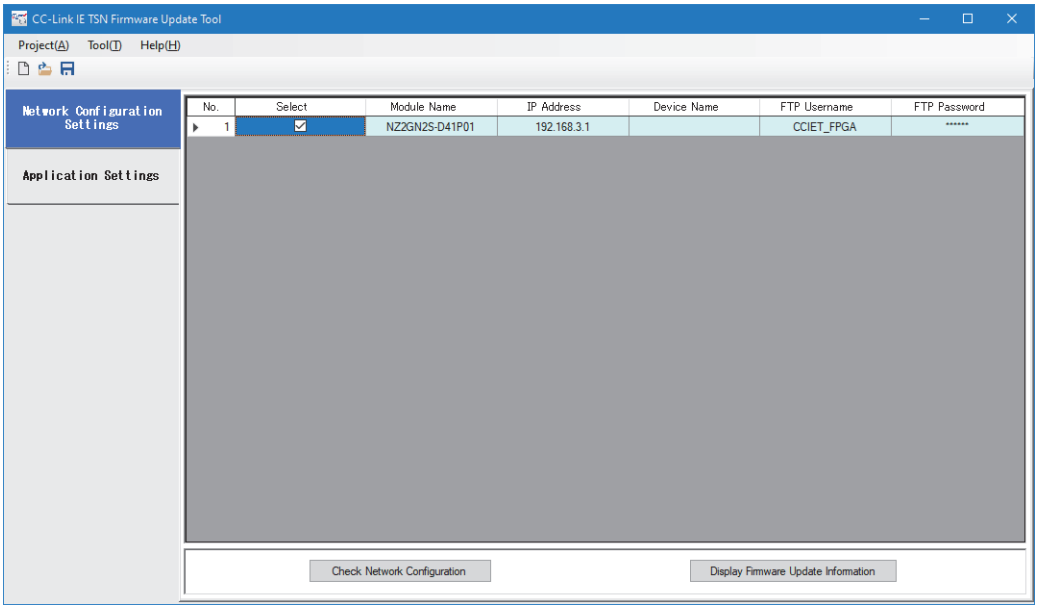
Model name	File name
NZ2GN2S-D41D01	CCIET_FPGA.SYF
NZ2GN2S-D41P01	
NZ2GN2S-D41PD02	

Setting method

Setting the CC-Link IE TSN Firmware Update Tool is required to update firmware for FPGA modules.
For details, refer to the "Help" of the CC-Link IE TSN Firmware Update Tool.

■"Network Configuration Settings" window

Window



Displayed items

Set the following items in the "Network Configuration Settings" window.

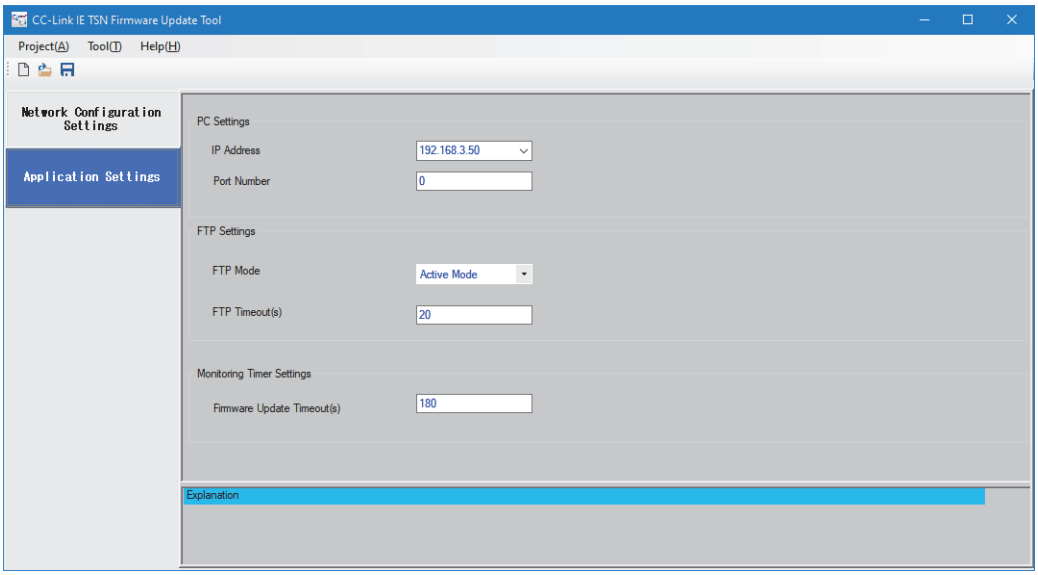
Item	Description
Module Name	Set the model name of the FPGA module whose firmware is to be updated.
IP address	Set the IP address of the FPGA module to update the firmware.
Device Name	Set the name of the equipment. Since the FPGA module does not use this value, the firmware can be updated even if the field is blank.
FTP User name	Set CCIET_FPGA.
FTP Password	Set CCIET_FPGA.

Point

Firmware can be simultaneously updated for FPGA modules with different model names, when the firmware update file that is used is the same, and the character strings set in "Module Name" of CC-Link IE TSN Firmware Update Tool are the same (it does not matter if the model names of the actual modules are different). For example, set NZ2GN2S-D41P01 as the model name of all FPGA modules for which the firmware is to be updated.

■"Application Settings" window

Window



Displayed items

Set the following items in the "Application Settings" window.

Classification	Item	Setting range	Description
PC Settings	IP Address	0.0.0.1 to 223.255.255.254	Set the IP address of the personal computer.
	Port Number	0, 49152 to 65535	Set 0.
FTP Settings	FTP Mode	"Active Mode" (fixed)	The FPGA module only supports "Active Mode".
	FTP Timeout(s)	1 to 600(s)	Set the FTP timeout time.
Monitoring Timer Settings	Firmware Update Timeout(s)	1 to 1200(s)	Set the firmware update timeout time.

Operation

■LED status

The status of the firmware update can be checked with the RUN LED of the FPGA module.

LED	Normal operation	Firmware update in progress	Firmware update completed (either completed successfully or completed with an error)
RUN LED	On	Flashing	Off

Error information list

The following table lists the error information of FPGA module-specific errors that can occur when a firmware update is performed.

Error information*1	Error name	Description and cause	Action
0001H	File error	A file that cannot be used for the FPGA module to be updated is specified.	Review the firmware update file specified with the CC-Link IE TSN Firmware Update Tool.
0002H	Communication error	A communication error has occurred during firmware update.	• Check whether Ethernet cables are connected properly. • Take measures to reduce noise on the transmission path.
0003H	Module error	An error has occurred on the module during firmware update.	Turn off and on the module power supply, and restart the CC-Link IE TSN Firmware Update Tool. If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
0004H	Firmware update disabled	Firmware update was attempted during data link.	Update firmware while data link is not being performed (disconnected).

*1 The error code of the CC-Link IE TSN Firmware Update Tool is displayed in 0x notation.

Point

If error information other than the above is displayed on the CC-Link IE TSN Firmware Update Tool, refer to the "Help" on the CC-Link IE TSN Firmware Update Tool.

Precautions

- It is not possible to update the firmware of a data-linked FPGA module. When updating the firmware of the FPGA module, do not connect the FPGA module with the master station. If firmware update is attempted for an FPGA module where data link is being performed, a firmware update disabled (error code: 0004H) is displayed on the error information of the firmware update information window. At this time, no error occurs in the FPGA module.
- When updating the firmware of the FPGA module, stop transient transmission with other stations. If the firmware update is executed without stopping transient transmission, an accident may occur due to malfunction.
- Do not update firmware for FPGA modules simultaneously by using multiple CC-Link IE TSN Firmware Update Tools.
- If an error has occurred during the firmware update, power off and on the FPGA module or perform a remote reset before attempting the firmware update again.
- After completing a firmware update, turn off and on the power supply of the FPGA module. Note that because restoration processing is performed when restarting after a firmware update, it may take a longer time compared to a normal start for the FPGA module to start (RUN LED on).

PART 7 SAMPLE CIRCUIT

This part consists of the following chapters.

13 SAMPLE CIRCUIT IN STANDALONE MODE

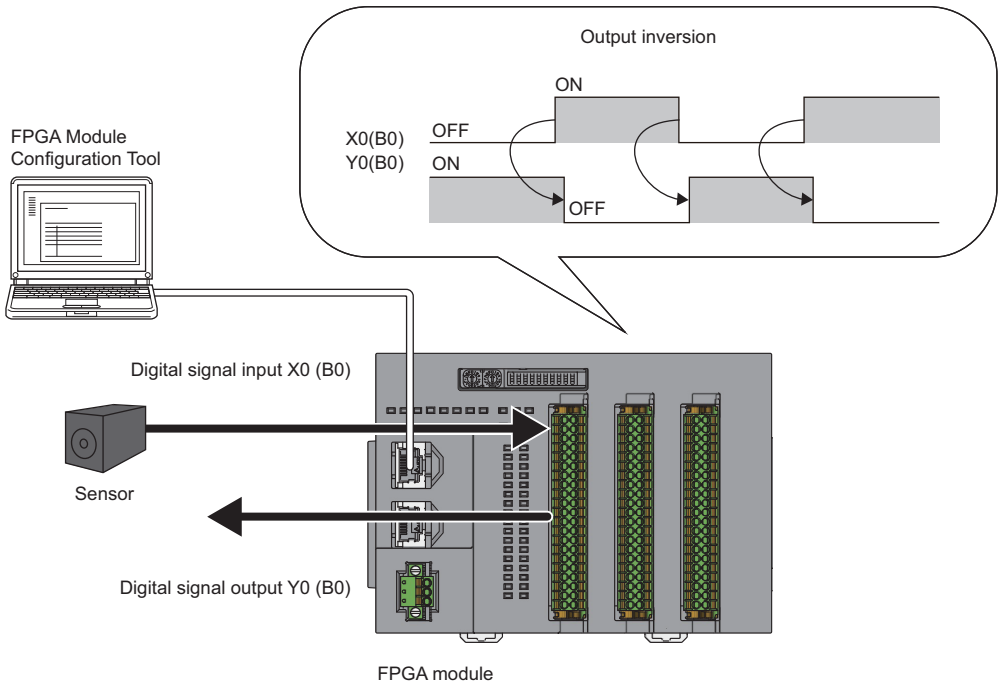
This chapter describes the sample circuit when using the following functions in standalone mode.

- Inversion output function of the digital control part (☞ Page 366 When Using the Inversion Output Function)
- Pulse count function of the counter control part (☞ Page 371 When Using the Pulse Count Function)
- D/A conversion function of the analog output part (☞ Page 376 When Using the D/A Conversion Function)
- Pulse output function of the pulse output part (☞ Page 380 When Using the Pulse Output Function)
- Logging function of the logging control part (☞ Page 384 When Using the Logging Function)

13.1 When Using the Inversion Output Function

This section describes the function to invert the digital signal input to X0 (B0) and output it to Y0 (B0).

System configuration



FPGA module: NZ2GN2S-D41P01

Module parameter

The setting value of the module parameter is shown below.

Setting item	Setting value
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (B0)	0.15μs
Data update timing (B0)	0.1μs
Output signal selection Y0 (B0)	User circuit output
Input filter upper limit value X0 (B0)	4000

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B000H (writing data 0)	Digital control part enable/disable control register (IOB0_X0 B0) (usr_wreg_000)	0003H
1000_B0F0H (writing data 120)	Digital output control digital output selection (B0) (usr_wreg_078)	0000H

Setting method

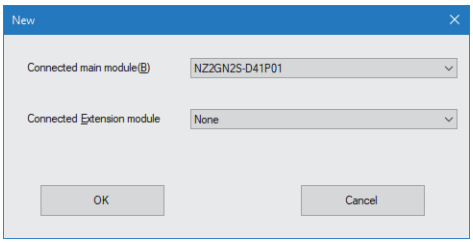
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

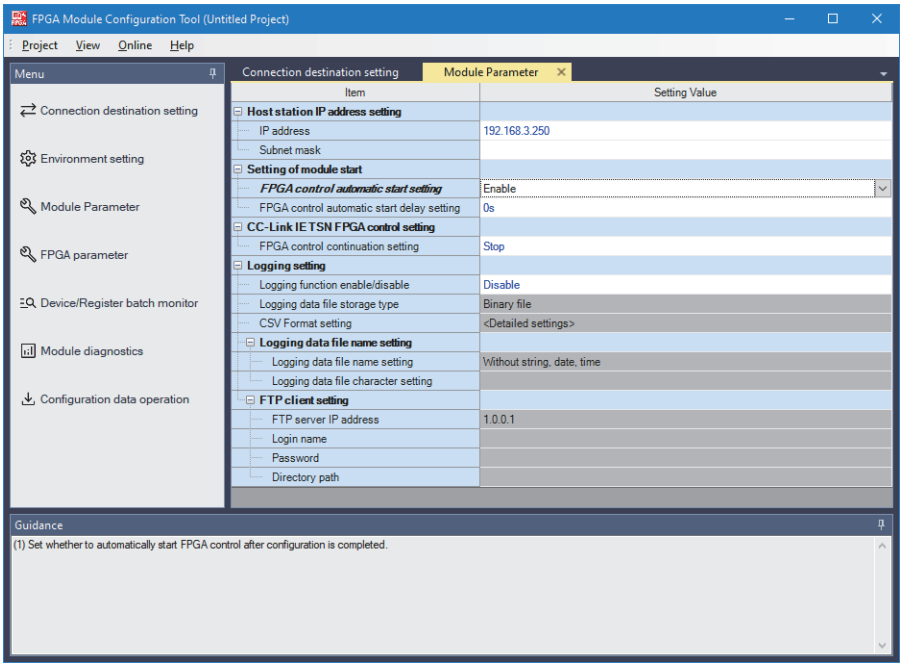
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



8. From the "FPGA parameter" window, set the values of the FPGA parameters.

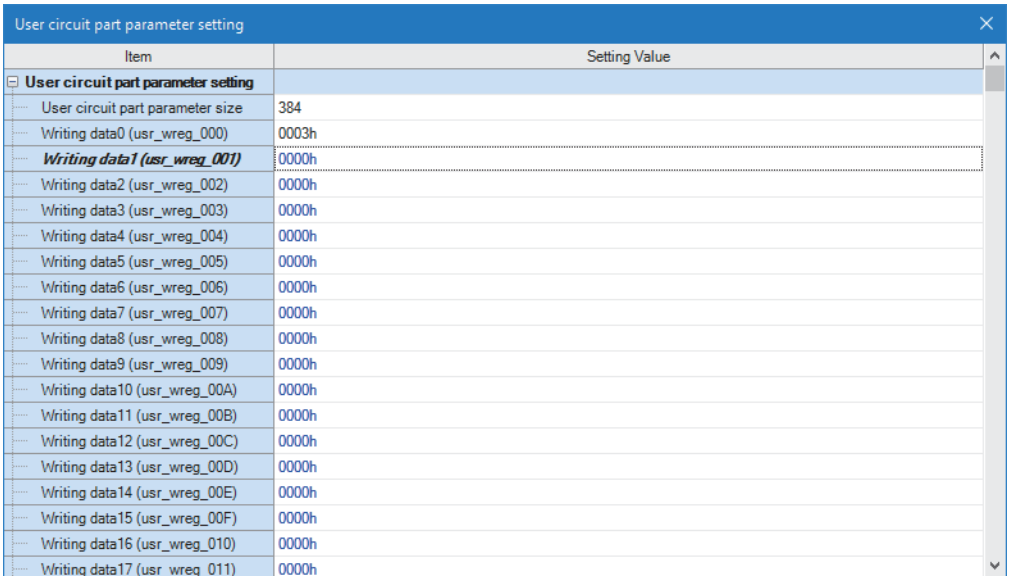
[Menu] ⇨ [FPGA parameter]

Connection destination setting | Environment setting | Module Parameter | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.15μs	0.15μs	0.15μs	0.15μs	0.15μs	0.15μs
Filter sampling pulse	Data sampling tin	Data sampling tin	Data sampling tin	Data sampling tin	Data sampling tin	Data sampling tin
Data update timing	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs
Logging cycle timing	1μs					
Digital input control part setting						
Input filter upper limit value						
Input filter upper limit value X0	4000	4000	4000	4000	4000	4000
Input filter upper limit value X1	4000	4000	4000	4000	4000	4000
Input filter upper limit value X2	4000	4000	4000	4000	4000	4000
Input filter upper limit value X3	4000	4000	4000	4000	4000	4000
Input filter upper limit value X4	4000	4000	4000	4000	4000	4000
Input filter upper limit value X5	4000	4000	4000	4000	4000	4000
Input filter upper limit value X6	4000	4000	4000	4000	4000	4000
Input filter upper limit value X7	4000	4000	4000	4000	4000	4000
Input filter upper limit value X8	4000	4000	4000	4000	4000	4000
Input filter upper limit value X9	4000	4000	4000	4000	4000	4000
Input filter upper limit value XA	4000	4000	4000	4000	4000	4000
Input filter upper limit value XB	4000	4000	4000	4000	4000	4000

9. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

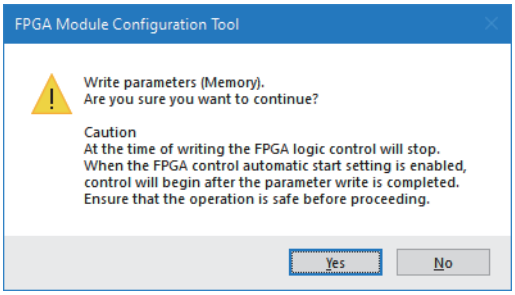
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



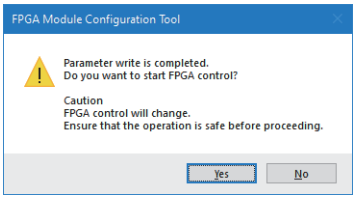
10. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

11. Click the [Yes] button.



12. Click the [Yes] button.



Implementation method and check method

Check that the digital signal input to X0 (B0) is inverted and the inverted signal is output.
Follow the steps below to monitor the FPGA register using the FPGA Module Configuration Tool.

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.
2. Input a digital signal from the sensor to X0 (B0).
3. In "Device/Register batch monitor", monitor the following FPGA register and check that the input digital signal to X0 (B0) is inverted and output from bit 0.

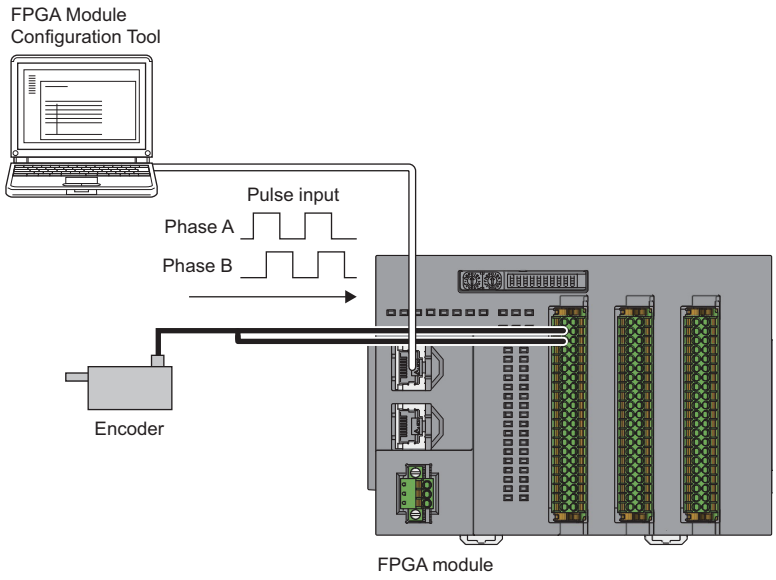
[Menu] ⇨ [Device/Register batch monitor]

Address	Name
1000_4020H	Output signal monitor (B0) (iport_iob0y_monitor)

13.2 When Using the Pulse Count Function

This section describes the function to use 32-bit ring counters to count pulses (2-phase multiple of 4) with the width of 100μs that are input to X1(B0) and X2(B0). Where the counter upper limit is 4294967295.

System configuration



FPGA module: NZ2GN2S-D41P01

Module parameter

The setting value of the module parameter is shown below.

Setting item	Setting value
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (B0)	0.10μs
Input filter upper limit value X1 (B0)	100
Input filter upper limit value X2 (B0)	100

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B146H (writing data 163)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0) (usr_wreg_0A3)	FFFFH
1000_B148H (writing data 164)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0) (usr_wreg_0A4)	FFFFH
1000_B14AH (writing data 165)	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	0302H

FPGA register setting while the FPGA module is running

When using the pulse count function, there are FPGA register areas in the user circuit that can be set while the module is running. The FPGA register areas in the user circuit that can be set while the FPGA module is running are shown below.

Address	Link register	Name
1000_B310H	RWw18	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B0) (usr_wreg_188)
1000_B312H	RWw19	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0) (usr_wreg_189)
1000_B314H	RWw1A	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0) (usr_wreg_18A)

Point

Set the value of Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (RWw19, RWw1A), and set Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (RWw18) to Enable (1). By doing so, the value of the 32-bit ring counter can be changed to the set preset value.

Setting method

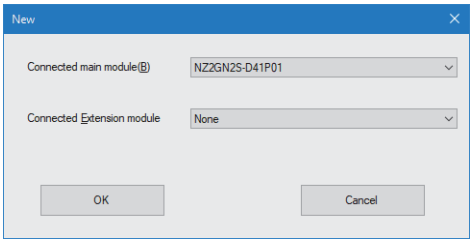
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

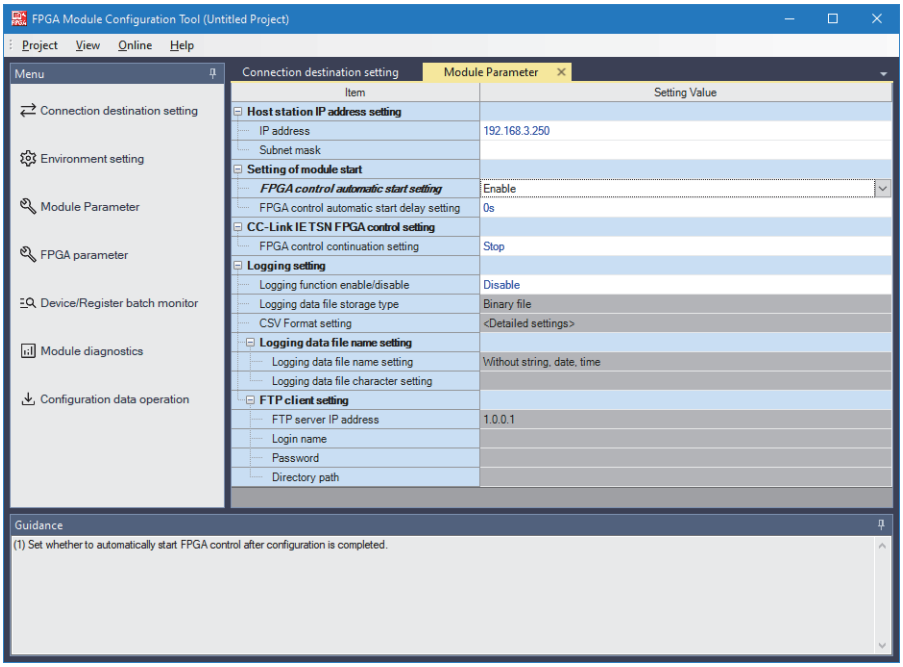
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



8. From the "FPGA parameter" window, set the values of the FPGA parameters.

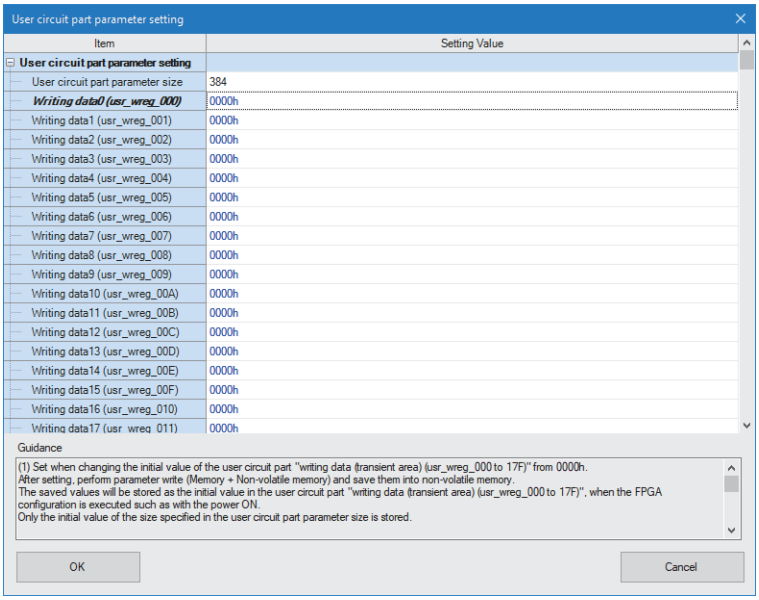
[Menu] ⇨ [FPGA parameter]

Connection destination setting | Environment setting | Module Parameter | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.10μs	0.15μs	0.15μs	0.15μs	0.15μs	0.15μs
Filter sampling pulse	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing
Data update timing	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs	0.10μs
Logging cycle timing	1μs					
Digital input control part setting						
Input filter upper limit value						
Input filter upper limit value X0	4000	4000	4000	4000	4000	4000
Input filter upper limit value X1	100	4000	4000	4000	4000	4000
Input filter upper limit value X2	100	4000	4000	4000	4000	4000
Input filter upper limit value X3	4000	4000	4000	4000	4000	4000
Input filter upper limit value X4	4000	4000	4000	4000	4000	4000
Input filter upper limit value X5	4000	4000	4000	4000	4000	4000
Input filter upper limit value X6	4000	4000	4000	4000	4000	4000
Input filter upper limit value X7	4000	4000	4000	4000	4000	4000
Input filter upper limit value X8	4000	4000	4000	4000	4000	4000
Input filter upper limit value X9	4000	4000	4000	4000	4000	4000
Input filter upper limit value XA	4000	4000	4000	4000	4000	4000
Input filter upper limit value XB	4000	4000	4000	4000	4000	4000

9. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

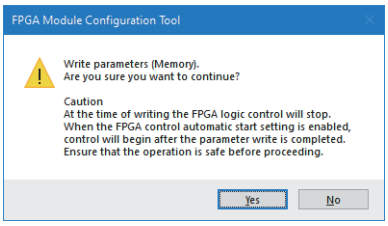
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



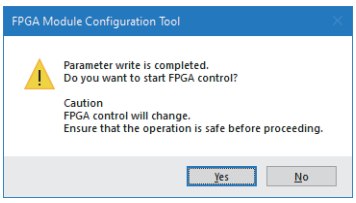
10. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

11. Click the [Yes] button.



12. Click the [Yes] button.



FPGA register change method

This section described the procedure to change the FPGA register setting while the FPGA module is running.

Operating procedure

1. Use "Device/Register batch monitor".

[Menu] ⇨ [Device/Register batch monitor]

2. In "FPGA register", enter the address of the register to be set and click the [Start Monitoring] button.

3. Click the current value to rewrite a desired value.

An FPGA register area assigned to a link device can be set by rewriting the value of the link device.

Implementation method and check method

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.
2. Input pulses from the encoder.
3. In "Device/Register batch monitor", monitor the following FPGA register areas and check that the counter value is increased.

[Menu] ⇨ [Device/Register batch monitor]

Address	Link register	Name
1000_BB66H	RWr43	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (usr_rreg_1B3)
1000_BB68H	RWr44	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (usr_rreg_1B4)

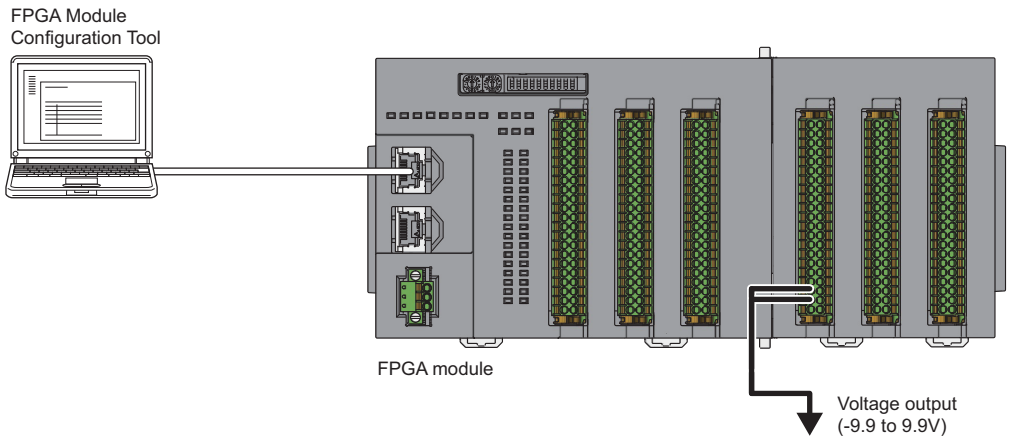
4. If necessary, set the following FPGA register areas and preset the counter values.

☞ Page 372 FPGA register setting while the FPGA module is running

13.3 When Using the D/A Conversion Function

This section describes the function to D/A-convert a digital value and output a voltage in CH0 (E0).

System configuration example



FPGA module: NZ2GN2S-D41P01+NZ2EX2S-D41A01

Module parameter

The setting value of the module parameter is shown below.

Setting item	Setting value
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be used are shown below.

Setting item	Setting value
D/A conversion enable/disable setting CH0 (E0)	Conversion-enable
Select D/A conversion value CH0 (E0)	User circuit output
Select D/A conversion timing (E0)	User circuit output
Select DAC LDAC signal (E0)	User circuit output
DAC offset value CH0 (E0)	0
DAC range setting CH0 (E0)	-9.9 to 9.9V

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B2C0H (writing data 352)	Analog output part LDAC output selection (usr_wreg_160)	0001H

FPGA register setting while the FPGA module is running

When using the D/A conversion function, there are FPGA register areas in the user circuit that can be set while the module is running. The FPGA register areas in the user circuit that can be set while the FPGA module is running are shown below.

Address	Link register	Name
1000_B380H	RWw50	Analog output part D/A conversion value CH0 (E0) (usr_wreg_1C0)
1000_B38CH	RWw56	Analog output part D/A conversion value enable (usr_wreg_1C6)

By setting b0 of Analog output part D/A conversion value enable (RWw56) to Pulse output (1), the D/A converted analog value is output from CH0 (E0).

Setting method

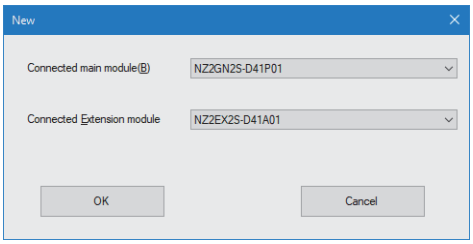
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

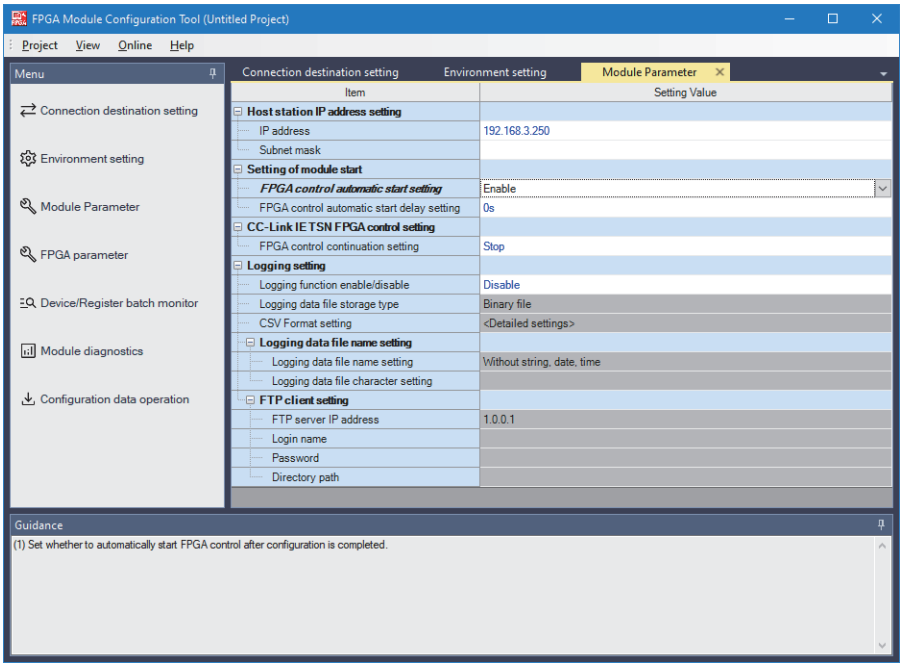
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

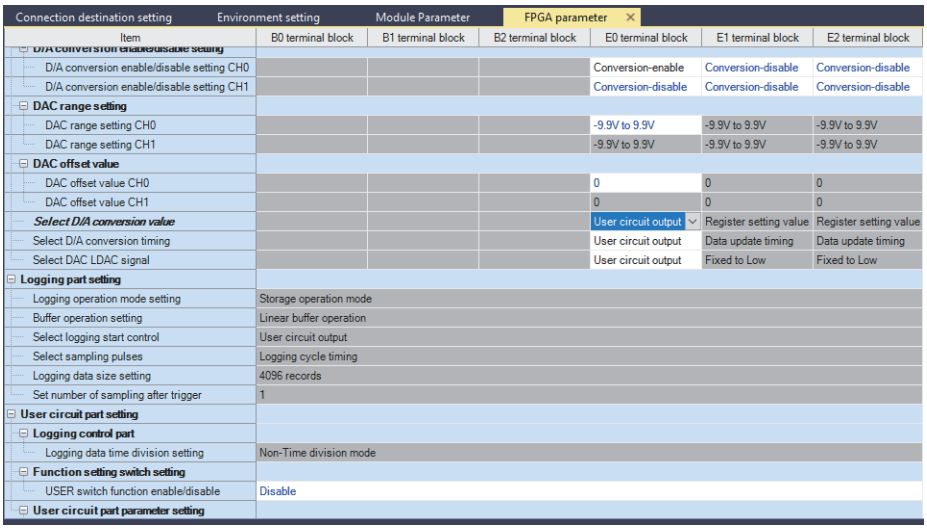
7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



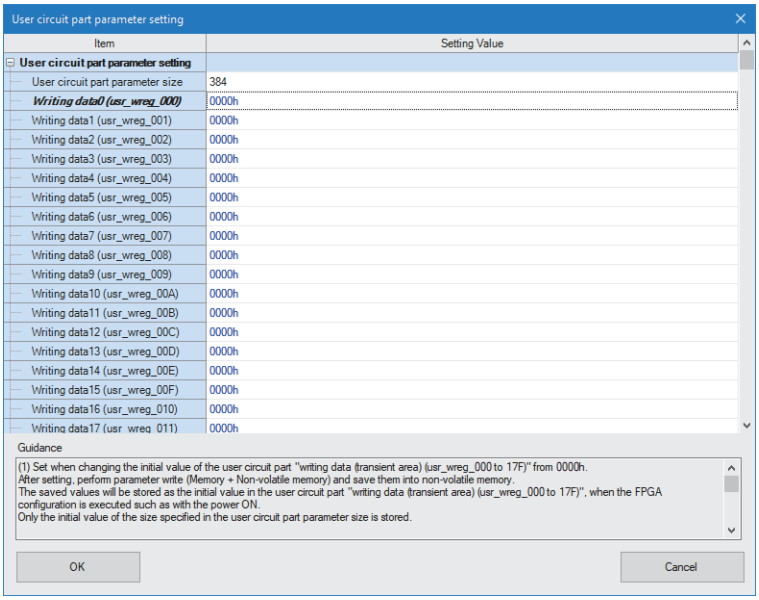
8. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]



9. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

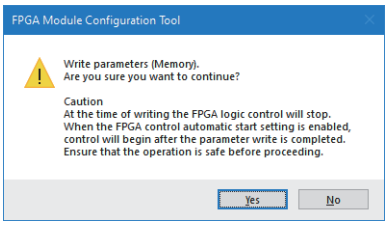
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



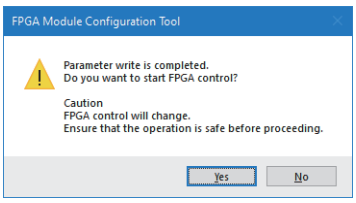
10. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

11. Click the [Yes] button.



12. Click the [Yes] button.



Implementation method and check method

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.

2. Set the following FPGA register areas in "Device/Register batch monitor".

[Menu] ⇨ [Device/Register batch monitor]

☞ Page 377 FPGA register setting while the FPGA module is running

3. Check that a voltage of 9.9V is being output on the connected device.

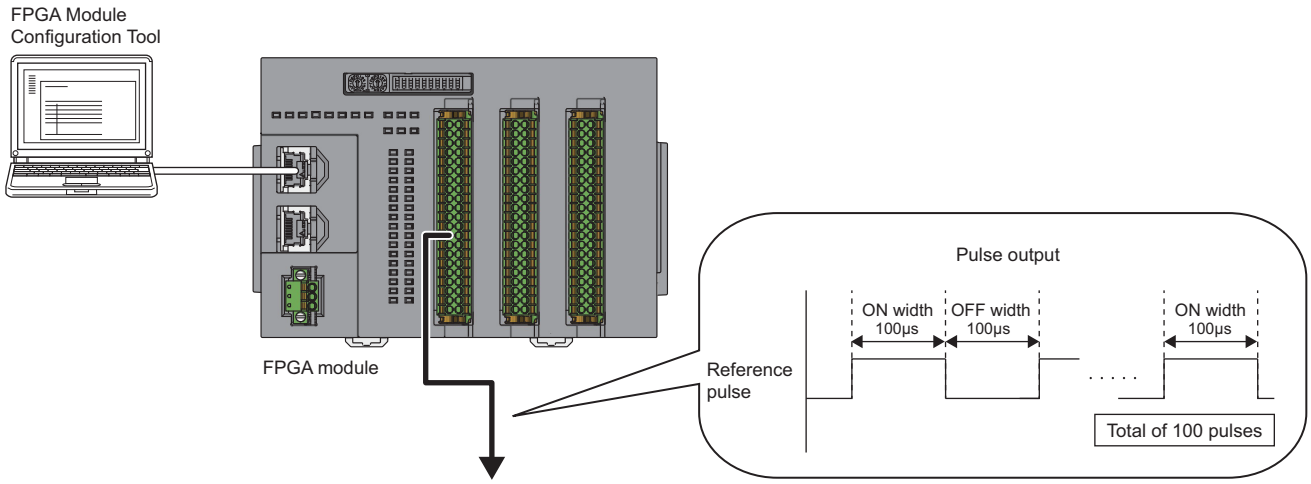
13.4 When Using the Pulse Output Function

This section describes how to generate a pulse under the following conditions.

- ON width: 100μs
- OFF width: 100μs
- Number of pulses: 100

System configuration

The figure below shows a connection example of using the pulse output function to output a pulse from Y1 (B0).



FPGA module: NZ2GN2S-D41P01

Module parameter

The setting value of the module parameter is shown below.

Setting item	Setting value
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data update timing (B0)	0.1μs
Output signal selection Y1 (B0)	User circuit output

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B0F0H (writing data 120)	Digital output control digital output selection (B0) (usr_wreg_078)	0002H
1000_B220H (writing data 272)	Pulse output part pulse width upper limit value (lower side) (B0) (usr_wreg_110)	270FH (100μs)
1000_B222H (writing data 273)	Pulse output part pulse width upper limit value (upper side) (B0) (usr_wreg_111)	0000H
1000_B224H (writing data 274)	Pulse output part output pulse count upper limit value (lower side) (B0) (usr_wreg_112)	0064H (100 pulses)
1000_B226H (writing data 275)	Pulse output part output pulse count upper limit value (upper side) (B0) (usr_wreg_113)	0000H
1000_B260H (writing data 304)	Pulse output part pulse output selection 0 (B0) (usr_wreg_130)	0000H
1000_B284H (writing data 322)	Pulse output part pulse output mask 0 (B0) (usr_wreg_142)	0002H

FPGA register setting while the FPGA module is running

When using the pulse output function, there are FPGA register areas in the user circuit that can be set while the module is running. The FPGA register area in the user circuit that can be set while the FPGA module is running is shown below.

Address	Link register	Name
1000_B370H	RWw48	Pulse output part pulse output enable (B0) (usr_wreg_1B8)

By setting b0 of Pulse output part pulse output enable (B0) (RWw48) to Enable (1), pulses are output from Y1 (B0).

Setting method

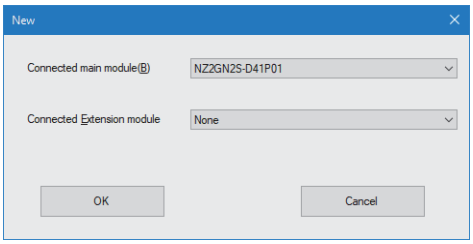
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

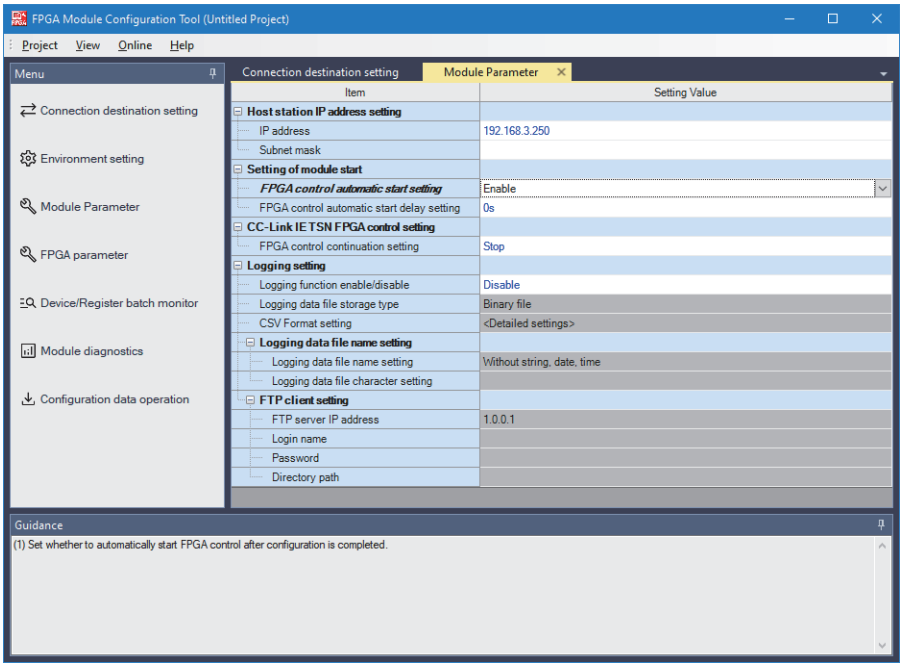
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

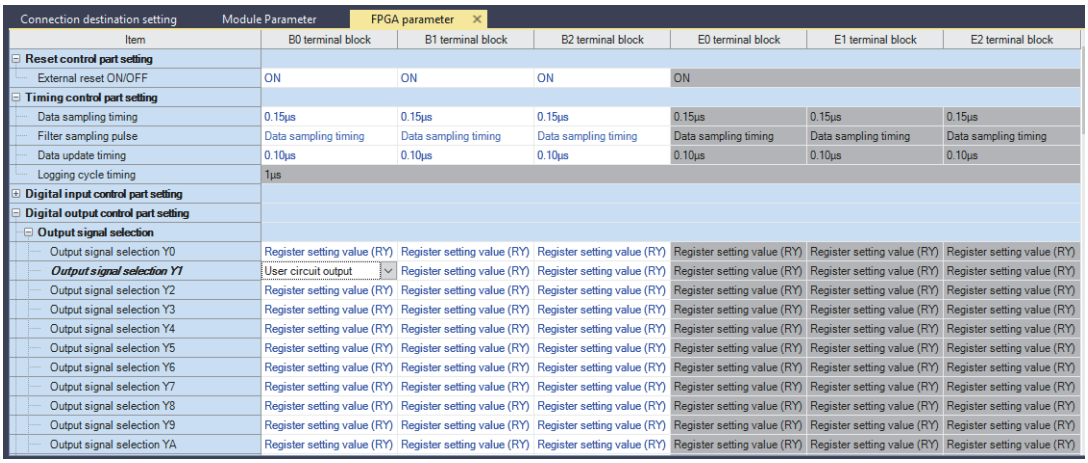
7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



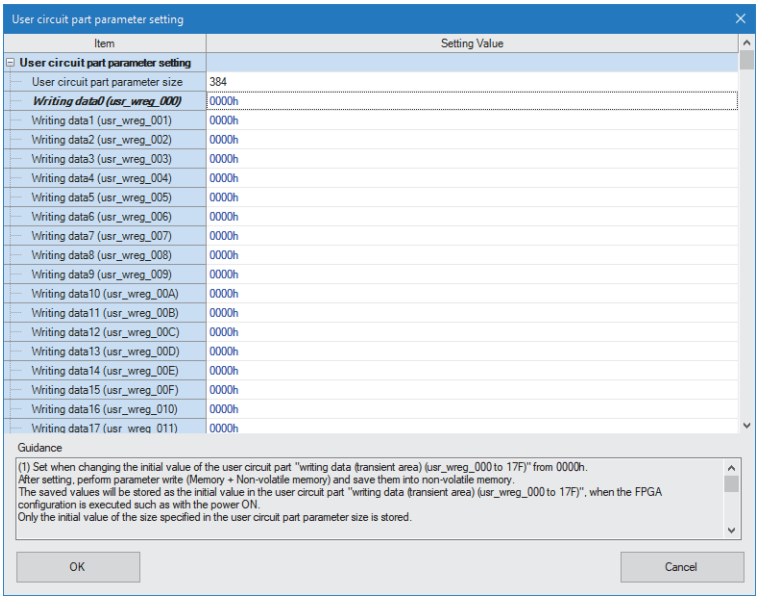
8. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]



9. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

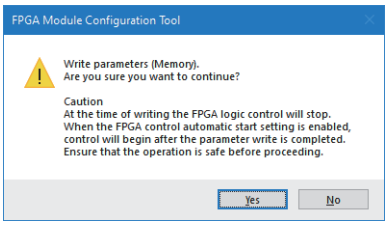
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



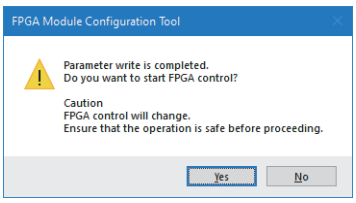
10. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

11. Click the [Yes] button.



12. Click the [Yes] button.



Implementation method and check method

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.

2. Set the following FPGA register areas in "Device/Register batch monitor".

[Menu] ⇨ [Device/Register batch monitor]

Set b0 of Pulse output part pulse output enable (B0) (RWw48) to Enable (1). (☞ Page 381 FPGA register setting while the FPGA module is running)

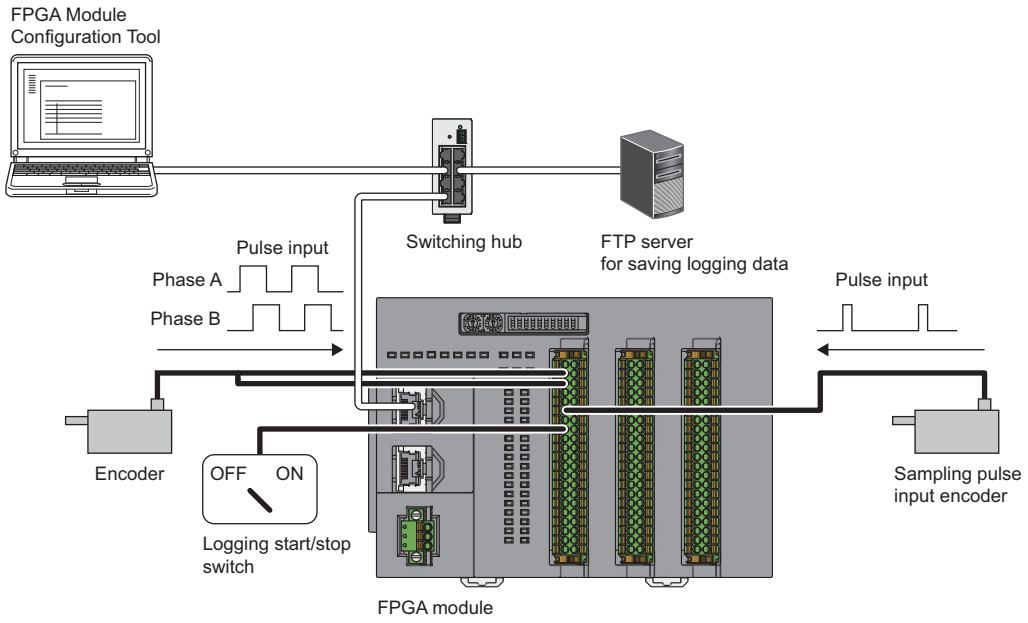
3. Check that 100 pulses with the ON width of 100μs and the OFF width of 100μs are output from Y1 (B0).

13.5 When Using the Logging Function

Logging external inputs and counters

This section describes how to log the status of external inputs and count values.

System configuration

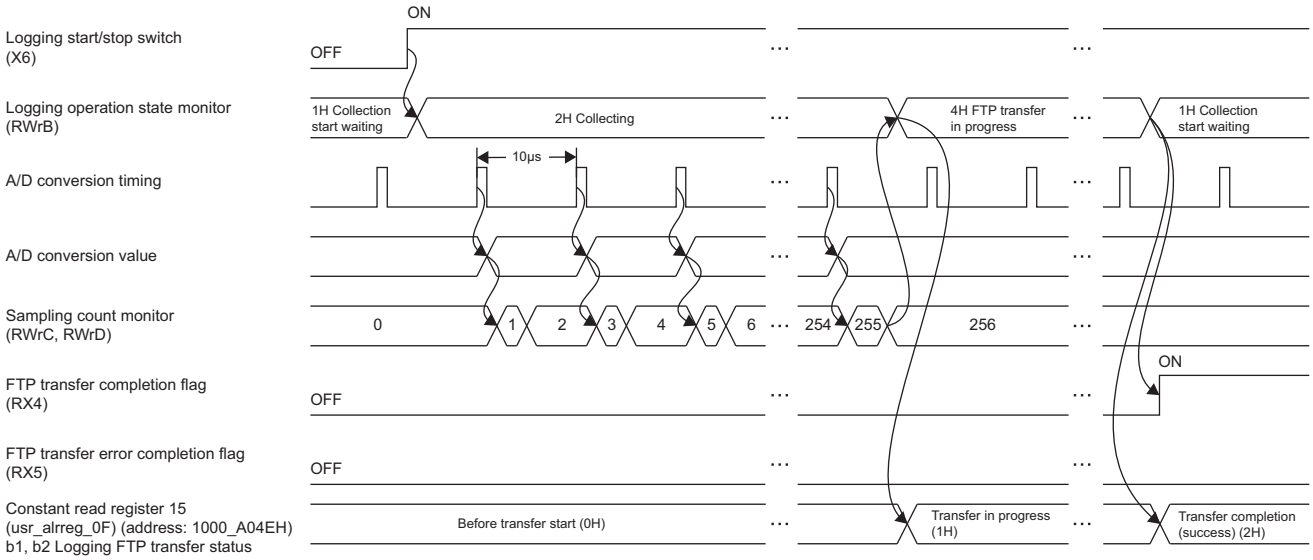


FPGA module: NZ2GN2S-D41P01

Operation

In this connection example, the input of X6 (B0) controls the start and stop of logging, and the pulse input of X4 (B0) controls the sampling timing. This enables the logging of the 32-bit ring counters that count pulses input to X1 (B0) and X2 (B0) with the pulse width of 100μs for 2-phase multiple of 4.

Also, when using the logging function, connect the FTP server for saving logging data to check the saved logging data, and transfer the logging data.



Module parameter

The setting values of the module parameters are shown below.

Setting item	Setting value
Logging function enable/disable	Enable
Logging data file storage type	CSV Files
CSV Format setting 0 (bit0~bit15)	Bit, binary format
CSV Format setting 6 (bit96~bit111)	Bit, binary format
CSV Format setting 7 (bit112~bit127)	Double Word [Unsigned], decimal format
FTP server IP address	IP address of the FTP server to be used
Login name	Login name of the FTP server to be used
Password	Password of the FTP server to be used
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (B0)	0.1μs
Input filter upper limit value X1 (B0)	100
Input filter upper limit value X2 (B0)	100
Logging operation mode setting	Storage operation mode
Buffer operation setting	Linear buffer operation
Select logging start control	User circuit output
Select sampling pulses	User circuit output
Logging data size setting	256 records

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B122H (writing data 145)	Logging control part logging enable signal selection (usr_wreg_091)	7H
1000_B126H (writing data 147)	Logging control part sampling pulse signal selection (usr_wreg_093)	5H
1000_B12AH (writing data 149)	Logging control part automatic transfer mode setting (usr_wreg_095)	1
1000_B146H (writing data 163)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0) (usr_wreg_0A3)	FFFFH
1000_B148H (writing data 164)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0) (usr_wreg_0A4)	FFFFH
1000_B14AH (writing data 165)	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	0302H

Logging data

The data to be logged is shown below.

	First bit	First word	Logging data															
			Description	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
User circuit logging data 0 to 431 (432 bits)	0	0	Digital input signal (after filtering) (B0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	16	1	Digital input signal (after filtering) (B1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	32	2	Digital input signal (after filtering) (B2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	48	3	Digital input signal (after filtering) (E0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	64	4	Digital input signal (after filtering) (E1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	80	5	Digital input signal (after filtering) (E2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	96	6	Counter control part 32-bit ring counter (2-phase multiple of 4) (B0)	Empty														Phase B	Phase A
	112	7		Counter value (32 bits)															
	128	8																	
	144	9	Counter control part 32-bit ring counter (2-phase multiple of 4) (B1)	Empty														Phase B	Phase A
	160	10		Counter value (32 bits)															
	176	11																	
	192	12	Counter control part 32-bit ring counter (2-phase multiple of 4) (B2)	Empty														Phase B	Phase A
	208	13		Counter value (32 bits)															
	224	14																	
	240	15	Counter control part 32-bit ring counter (2-phase multiple of 4) (E0)	Empty														Phase B	Phase A
	256	16		Counter value (32 bits)															
	272	17																	
	288	18	Counter control part 32-bit ring counter (2-phase multiple of 4) (E1)	Empty														Phase B	Phase A
	304	19		Counter value (32 bits)															
	320	20																	
	336	21	Counter control part 32-bit ring counter (2-phase multiple of 4) (E2)	Empty														Phase B	Phase A
	352	22		Counter value (32 bits)															
	368	23																	
	384	24	Empty	Empty															
	400	25																	
	416	26																	
Time information (80 bits)	432	27	µs	Empty						µs(10bit)									
	448	28	ms	Empty						ms(10bit)									
	464	29	Minute, second	Empty				Minute (6 bits)						Second (6 bits)					
	480	30	Month, day, hour	Empty		Month (4 bits)				Day (5 bits)					Hour (5 bits)				
	496	31	Year	Empty									Year (7 bits)						

Setting method

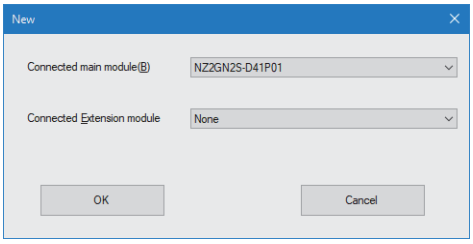
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

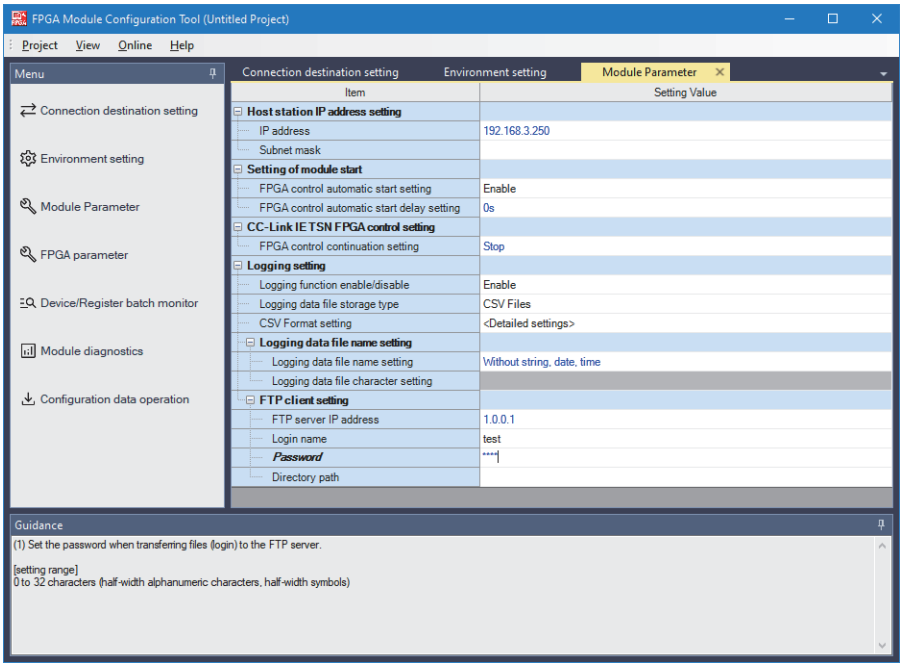
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

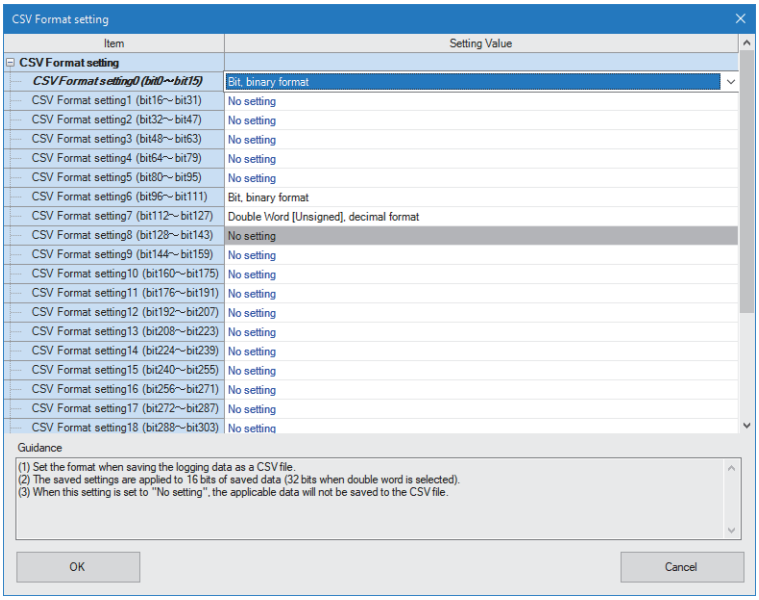
7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



8. Set the value of the CSV format setting in the "Logging data storage format setting" window.

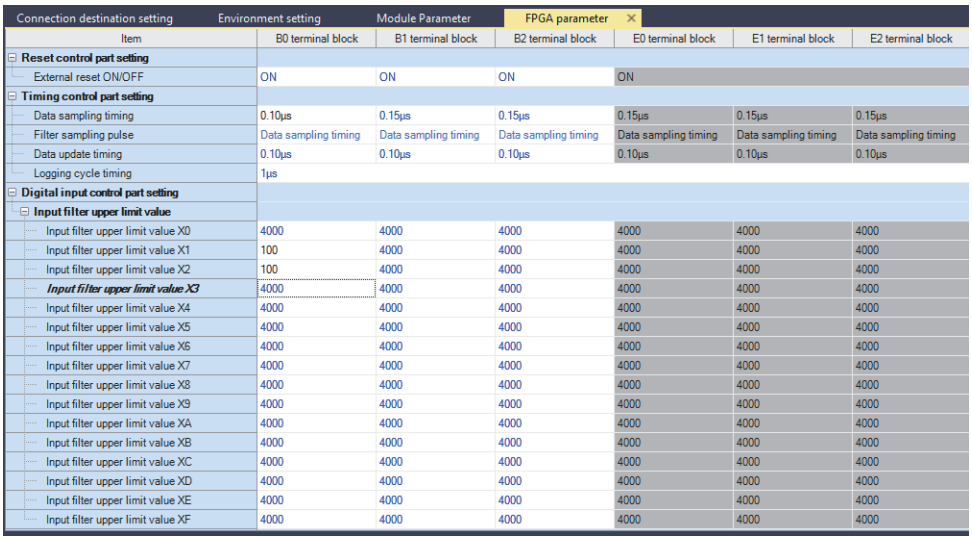
[Menu] ⇨ [Module Parameter] ⇨ [Logging setting] ⇨ [CSV Format setting] ⇨ <Detailed settings>



9. Click the [OK] button.

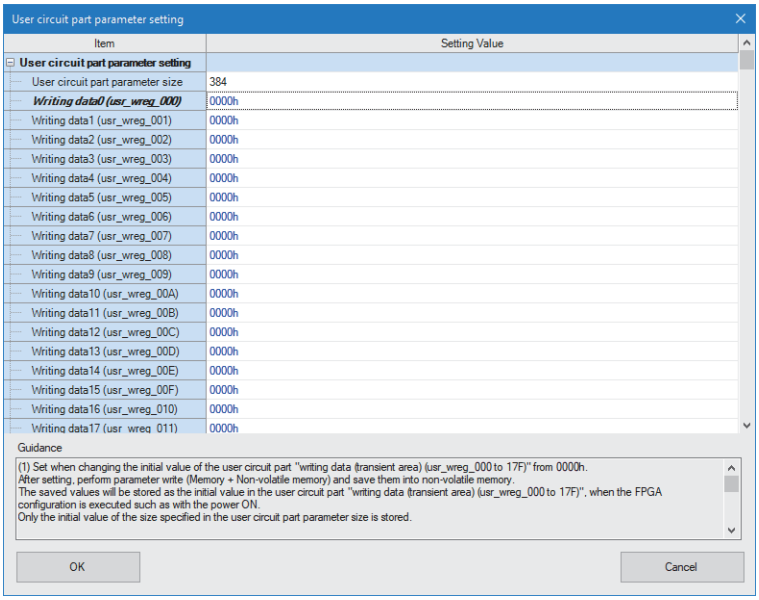
10. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]



11. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

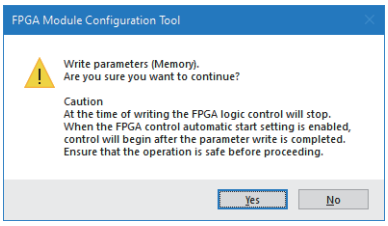
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



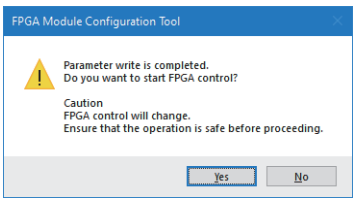
12. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

13. Click the [Yes] button.



14. Click the [Yes] button.



Implementation method and check method

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.

2. Start logging.

3. Input pulses from the encoder.

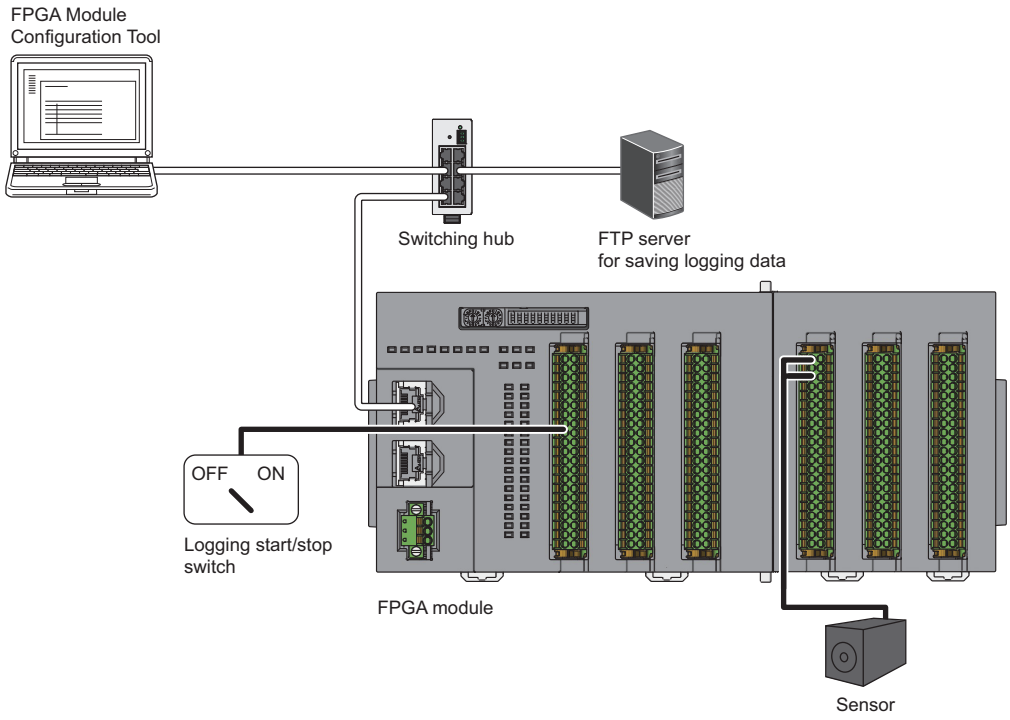
4. After 256 records of data have been collected, FTP transfer will start.

5. Check the file transferred over FTP.

Logging A/D conversion values

This section describes how to log A/D conversion values.

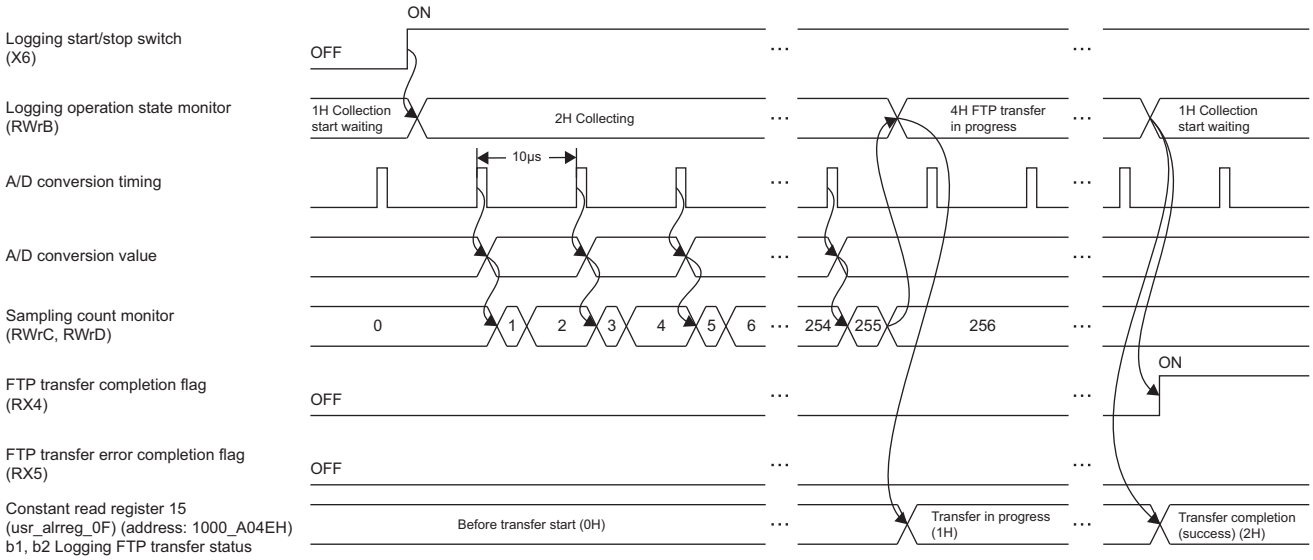
System configuration



FPGA module: NZ2GN2S-D41P01+NZ2EX2S-D41A01

Operation

The force of X6 (B0) controls the start and stop of logging, and logs the A/D conversion values of the sensor connected to CH0 (E0). Logging is performed for each A/D conversion timing of E0.



Module parameter

The setting values of the module parameters are shown below.

Setting item	Setting value
Logging function enable/disable	Enable
Logging data file storage type	Binary file
FTP server IP address	IP address of the FTP server to be used
Login name	Login name of the FTP server to be used
Password	Password of the FTP server to be used
FPGA control automatic start setting	Enable

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (E0)	10.00μs
A/D conversion enable/disable setting (E0)	Conversion-enable
Select A/D conversion timing CH0 (E0)	Data sampling timing
ADC range setting CH0 (E0)	Align with the analog signal output from the sensor.
Logging operation mode setting	Storage operation mode
Buffer operation setting	Linear buffer operation
Select logging start control	User circuit output*1
Select sampling pulses	User circuit output*1
Logging data size setting	256 records
Logging data time division setting	Time division mode

*1 When logging A/D conversion values in time division mode, set the user circuit output. If anything other than user circuit output is set, logging will not be performed properly.

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B122H (writing data 145)	Logging control part logging enable signal selection (usr_wreg_091)	7H
1000_B126H (writing data 147)	Logging control part sampling pulse signal selection (usr_wreg_093)	15H
1000_B12AH (writing data 149)	Logging control part automatic transfer mode setting (usr_wreg_095)	1H

Logging data

The data to be logged is shown below.

	First bit	First word	Logging data															
			Description	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
User circuit logging data 0 to 431 (432 bits)	0	0	Digital input signal (after filtering) (B0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	16	1	Digital input signal (after filtering) (B1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	32	2	Digital input signal (after filtering) (B2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	48	3	Digital input signal (after filtering) (E0)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	64	4	Digital input signal (after filtering) (E1)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	80	5	Digital input signal (after filtering) (E2)	XF	XE	XD	XC	XB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	96	6	Counter control part 32-bit ring counter (2-phase multiple of 4) (B0)	Empty														Phase B	Phase A
	112	7		Counter value (32 bits)															
	128	8																	
	144	9	Counter control part 32-bit ring counter (2-phase multiple of 4) (B1)	Empty														Phase B	Phase A
	160	10	Analog control A/D conversion value CH0 to CHB (E0)	Analog control A/D conversion value CH0 (E0)															
	176	11		Analog control A/D conversion value CH1 (E0)															
	192	12		Analog control A/D conversion value CH2 (E0)															
	208	13		Analog control A/D conversion value CH3 (E0)															
	224	14		Analog control A/D conversion value CH4 (E0)															
	240	15		Analog control A/D conversion value CH5 (E0)															
	256	16		Analog control A/D conversion value CH6 (E0)															
	272	17		Analog control A/D conversion value CH7 (E0)															
	288	18		Analog control A/D conversion value CH8 (E0)															
	304	19		Analog control A/D conversion value CH9 (E0)															
	320	20		Analog control A/D conversion value CHA (E0)															
	336	21		Analog control A/D conversion value CHB (E0)															
	352	22	Empty	Empty															
	368	23																	
	384	24																	
	400	25																	
	416	26																	
Time information (433 to 512 bits)	432	27	µs	Empty						µs(10bit)									
	448	28	ms	Empty						ms(10bit)									
	464	29	Minute, second	Empty				Minute (6 bits)						Second (6 bits)					
	480	30	Month, day, hour	Empty		Month (4 bits)				Day (5 bits)					Hour (5 bits)				
	496	31	Year	Empty									Year (7 bits)						
User circuit logging data 0 to 431 (513 to 944 bits)	512	32	Analog control A/D conversion value CH0 to CHB (E1)	Analog control A/D conversion value CH0 (E1)															
	528	33		Analog control A/D conversion value CH1 (E1)															
	544	34		Analog control A/D conversion value CH2 (E1)															
	560	35		Analog control A/D conversion value CH3 (E1)															
	576	36		Analog control A/D conversion value CH4 (E1)															
	592	37		Analog control A/D conversion value CH5 (E1)															
	608	38		Analog control A/D conversion value CH6 (E1)															
	624	39		Analog control A/D conversion value CH7 (E1)															
	640	40		Analog control A/D conversion value CH8 (E1)															
	656	41		Analog control A/D conversion value CH9 (E1)															
	672	42		Analog control A/D conversion value CHA (E1)															
	688	43		Analog control A/D conversion value CHB (E1)															
	704	44	Analog control A/D conversion value CH0 to CHB (E2)	Analog control A/D conversion value CH0 (E2)															
	720	45		Analog control A/D conversion value CH1 (E2)															
	736	46		Analog control A/D conversion value CH2 (E2)															
	752	47		Analog control A/D conversion value CH3 (E2)															
	768	48		Analog control A/D conversion value CH4 (E2)															
	784	49		Analog control A/D conversion value CH5 (E2)															
	800	50		Analog control A/D conversion value CH6 (E2)															
	816	51		Analog control A/D conversion value CH7 (E2)															
	832	52		Analog control A/D conversion value CH8 (E2)															
	848	53		Analog control A/D conversion value CH9 (E2)															
	864	54		Analog control A/D conversion value CHA (E2)															
	880	55		Analog control A/D conversion value CHB (E1)															
	896	56	Empty	Empty															
	912	57																	
	928	58																	
Time information (945 to 1024 bits)	944	59	µs	Empty						µs(10bit)									
	960	60	ms	Empty						ms(10bit)									
	976	61	Minute, second	Empty				Minute (6 bits)						Second (6 bits)					
	992	62	Month, day, hour	Empty		Month (4 bits)				Day (5 bits)					Hour (5 bits)				
	1008	63	Year	Empty									Year (7 bits)						

Setting method

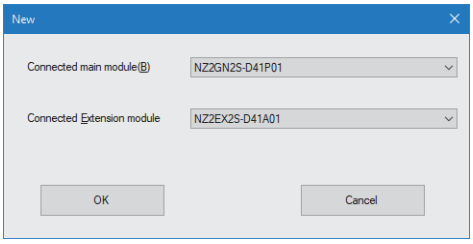
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

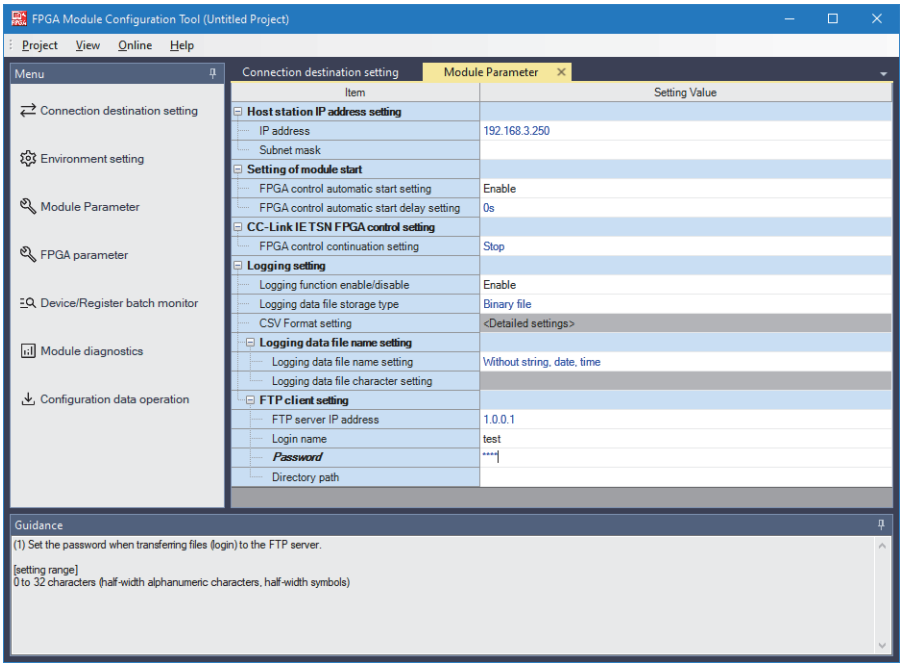
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



8. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]

Connection destination setting | Module Parameter | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.15μs	0.15μs	0.15μs	10.00μs	4.00μs	4.00μs
Filter sampling pulse	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing
Data update timing	0.10μs	0.10μs	0.10μs	6.00μs	6.00μs	6.00μs
Logging cycle timing	1μs					
Digital input control part setting						
Digital output control part setting						
Digital I/O control part setting						
Analog input control part setting						
A/D conversion enable/disable setting				Conversion-enable	Conversion-disable	Conversion-disable
ADC range setting						
ADC range setting CH0				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH1				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH2				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH3				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH4				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH5				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH6				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH7				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V

9. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>

User circuit part parameter setting

Item	Setting Value
User circuit part parameter setting	
User circuit part parameter size	384
Writing data0 (usr_wreg_000)	0000h
Writing data1 (usr_wreg_001)	0000h
Writing data2 (usr_wreg_002)	0000h
Writing data3 (usr_wreg_003)	0000h
Writing data4 (usr_wreg_004)	0000h
Writing data5 (usr_wreg_005)	0000h
Writing data6 (usr_wreg_006)	0000h
Writing data7 (usr_wreg_007)	0000h
Writing data8 (usr_wreg_008)	0000h
Writing data9 (usr_wreg_009)	0000h
Writing data10 (usr_wreg_00A)	0000h
Writing data11 (usr_wreg_00B)	0000h
Writing data12 (usr_wreg_00C)	0000h
Writing data13 (usr_wreg_00D)	0000h
Writing data14 (usr_wreg_00E)	0000h
Writing data15 (usr_wreg_00F)	0000h
Writing data16 (usr_wreg_010)	0000h
Writing data17 (usr_wreg_011)	0000h

Guidance

(1) Set when changing the initial value of the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)" from 0000h.
After setting, perform parameter write (Memory + Non-volatile memory) and save them into non-volatile memory.
The saved values will be stored as the initial value in the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)", when the FPGA configuration is executed such as with the power ON.
Only the initial value of the size specified in the user circuit part parameter size is stored.

OK | Cancel

10. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

11. Click the [Yes] button.

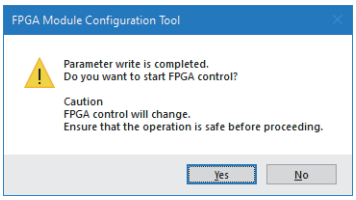
FPGA Module Configuration Tool

Write parameters (Memory).
Are you sure you want to continue?

Caution
At the time of writing the FPGA logic control will stop.
When the FPGA control automatic start setting is enabled, control will begin after the parameter write is completed.
Ensure that the operation is safe before proceeding.

Yes | No

12. Click the [Yes] button.



Implementation method and check method

Operating procedure

1. After writing the parameters, turn the power off and on to restart the module.

2. Start logging.

3. After 256 records of data have been collected, FTP transfer will start.

4. Check the file transferred over FTP.

Restriction

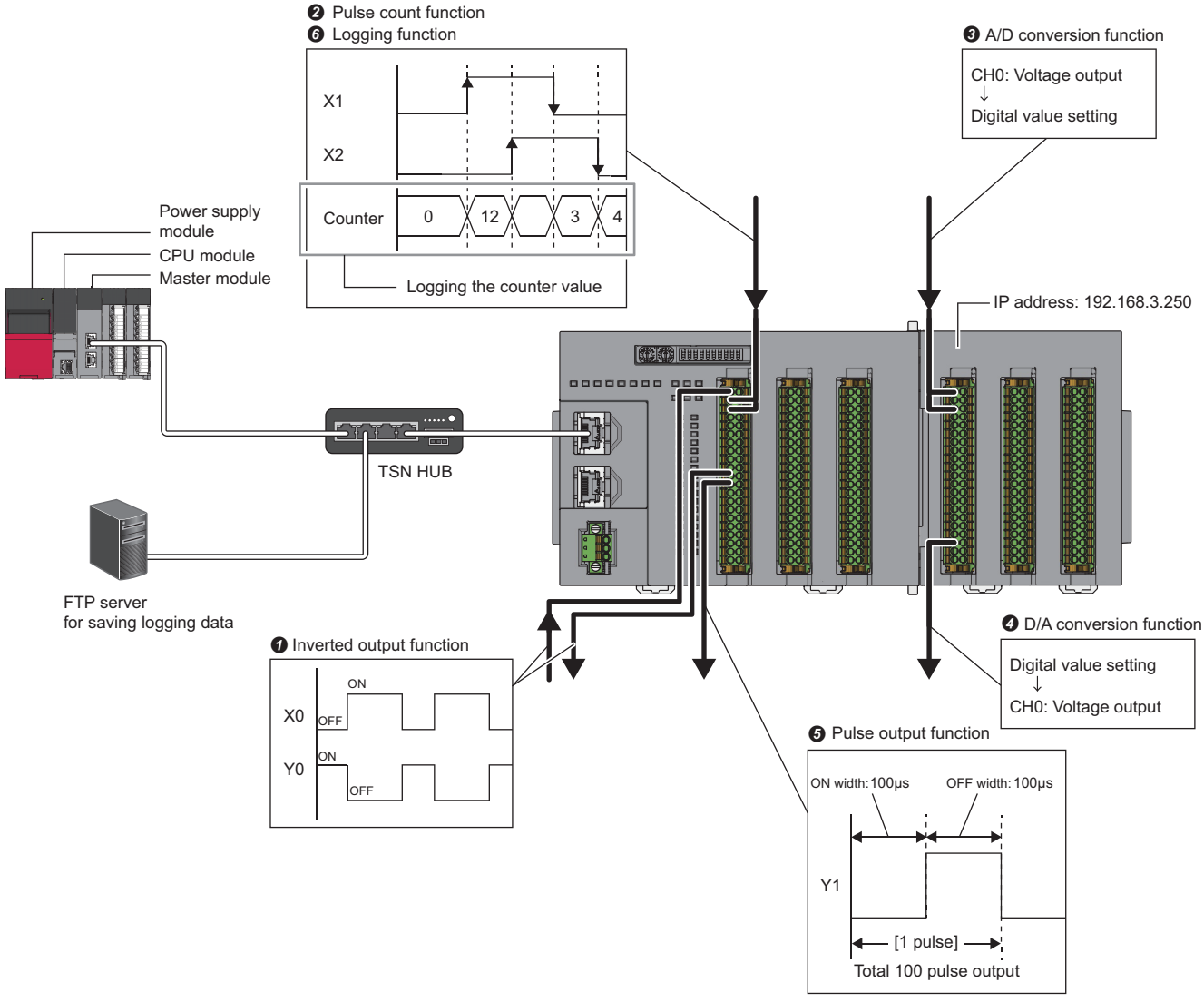
If FPGA control stops during logging of A/D conversion values in time division mode, logging will not be performed normally. If FTP resend allowed (RY4) is ON, turn off FTP resend allowed (RY4) and discard the logging data.

14 SAMPLE CIRCUIT IN CC-LINK IE TSN COMMUNICATION MODE

This chapter describes how to use the following functions of the sample circuit when setting the CC-Link IE TSN communication mode. Refer to the section for a desired function to be set.

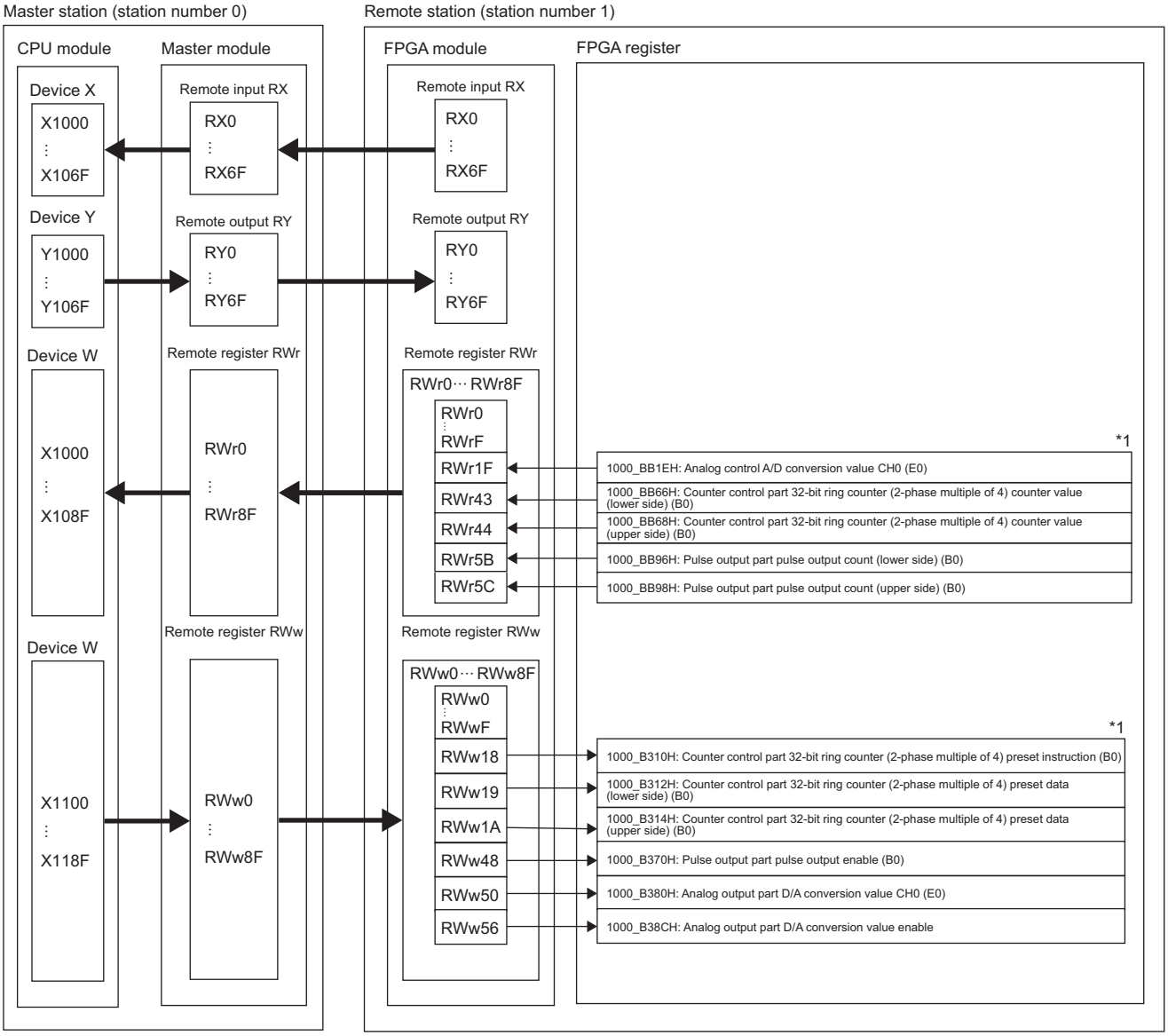
- Inversion output function of the digital control part (☞ Page 402 When Using the Inversion Output Function)
- Pulse count function of the counter control part (☞ Page 405 When Using the Pulse Count Function)
- Output block part A/D conversion function (☞ Page 408 When Using the A/D Conversion Function)
- D/A conversion function of the analog output part (☞ Page 411 When Using the D/A Conversion Function)
- Pulse output function of the pulse output part (☞ Page 414 When Using the Pulse Output Function)
- Logging function of the logging control part (☞ Page 417 When Using the Logging Function)

System configuration



- CPU module: R120CPU
- Master module: RJ71GN11-T2 (X0 to X1F/Y0 to Y1F)
- Input module: RX10 (X20 to X2F)
- Main module: NZ2GN2S-D41P01
- Extension module: NZ2EX2S-D41A01

Assignment of link devices



*1 The assignment of only FPGA register areas to be used is described.

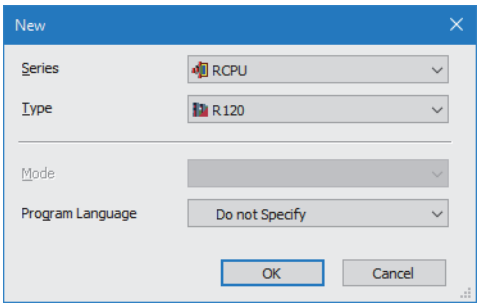
Setting of the master station

Connect the engineering tool to the CPU module of the master station and set parameters.

Operating procedure

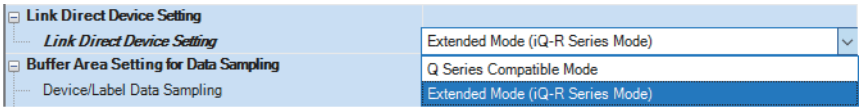
1. Set the CPU module as follows.

[Project] ⇨ [New]



2. In "CPU Parameter", set "Extended Mode (iQ-R Series Mode)" for "Link Direct Device Setting".

[CPU Parameter] ⇨ [Memory/Device Setting] ⇨ [Link Direct Device Setting] ⇨ [Link Direct Device Setting]

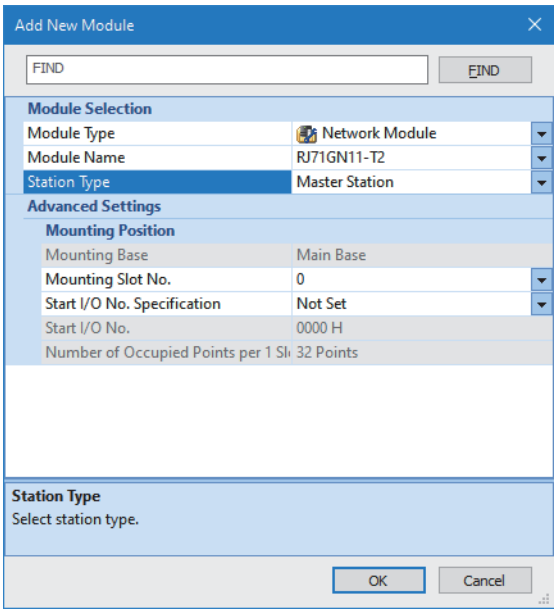


Restriction

When writing the module parameters of the RJ71GN11-T2 to the CPU module with the engineering tool, set "Extended Mode (iQ-R Series Mode)" for "Link Direct Device Setting".
When "Q Series Compatible Mode" is set for "Link Direct Device Setting", "Write to PLC" cannot be executed.

3. Set the RJ71GN11-T2 as follows.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ Right-click ⇨ [Add New Module]



4. Click the [OK] button.

5. Set the "Required Settings" as follows.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ [RJ71GN11-T2] ⇨ [Required Settings]

Setting Item

Item	Setting
Station Type	
Station Type	Master Station
Network No.	
Network No.	1
Parameter Setting Method	
Setting Method of Basic/Application Settings	Parameter Editor
Station No./IP Address Setting	
Station No./IP Address Setting Method	Parameter Editor
Station No.	
Station No.	0
IP Address	
IP Address	192 . 168 . 3 . 253
Subnet Mask	. . .
Default Gateway	. . .

6. Set the items in "Basic Settings" as follows.

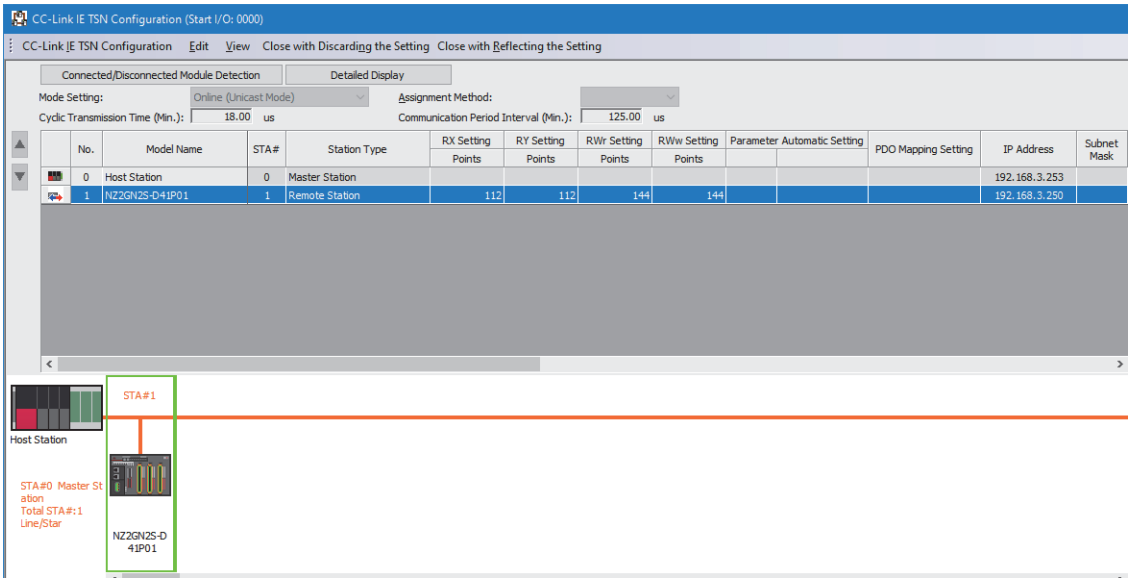
[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ [RJ71GN11-T2] ⇨ [Basic Settings]

Setting Item

Item	Setting
Network Configuration Settings	
Network Configuration Settings	<Detailed Setting>
Refresh Settings	
Refresh Settings	<Detailed Setting>
Network Topology	
Network Topology	Line/Star
Communication Period Setting	
Basic Period Setting	
Setting in Units of 1us	Not Set
Communication Period Interval Setting (Do not Set it in Units of 1us)	1000.00 us
Communication Period Interval Setting (Set it in Units of 1us)	1000.00 us
System Reservation Time	20.00 us
Cyclic Transmission Time	500.00 us
Transient Transmission Time	480.00 us
Multiple Period Setting	
Normal-Speed	x4
Low-Speed	x16
Connection Device Information	
Authentication Class Setting	Authentication Class B Only
TSN HUB Setting	Not to Use TSN HUB
Device Station Setting	
Disconnection Detection Setting	4 times

7. Set the network configuration as follows.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ [RJ71GN11-T2] ⇨ [Basic Settings] ⇨ [Network Configuration Settings] ⇨ <Detailed Setting>



8. Click the [Close with Reflecting the Setting] button to close the "CC-Link IE TSN Configuration" window.

9. Set the refresh settings as follows.

[Navigation Window] ⇨ [Parameter] ⇨ [Module Information] ⇨ [RJ71GN11-T2] ⇨ [Basic Settings] ⇨ [Refresh Setting] ⇨ <Detailed Setting>

No.	Link Side					CPU Side				
	Device Name	Points	Start	End		Target	Device Name	Points	Start	End
-	SB	512	00000	001FF		Specify Device	SB	512	00000	001FF
-	SW	512	00000	001FF		Specify Device	SW	512	00000	001FF
1	RX	112	00000	0006F		Specify Device	X	112	01000	0106F
2	RY	112	00000	0006F		Specify Device	Y	112	01000	0106F
3	RWr	144	00000	0008F		Specify Device	W	144	01000	0108F
4	RWw	144	00000	0008F		Specify Device	W	144	01100	0118F
5										

10. Click the [Apply] button.

11. Write the set parameter to the CPU module of the master station and reset the CPU module, or turn off and on the power supply.

[Online] ⇨ [Write to PLC]

14.1 Precautions for Programming

This section describes the precautions when creating programs for setting the CC-Link IE TSN communication mode.

Program for cyclic transmission

For a program for cyclic transmission, provide interlock between the following link special relay (SB) and the link special register (SW).

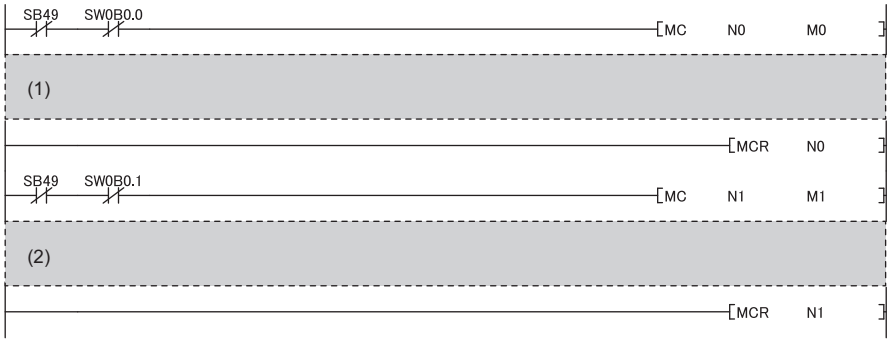
- Own station data link error status (master station) (SB0049)
- Data link status (each station) (SW00B0 to SW00B7)

For details, refer to the following.

User's manual for the master station used

Ex.

Interlock example



(1) Program for communications with station number 1
(2) Program for communications with station number 2

CC-Link IE TSN Network synchronous communication program

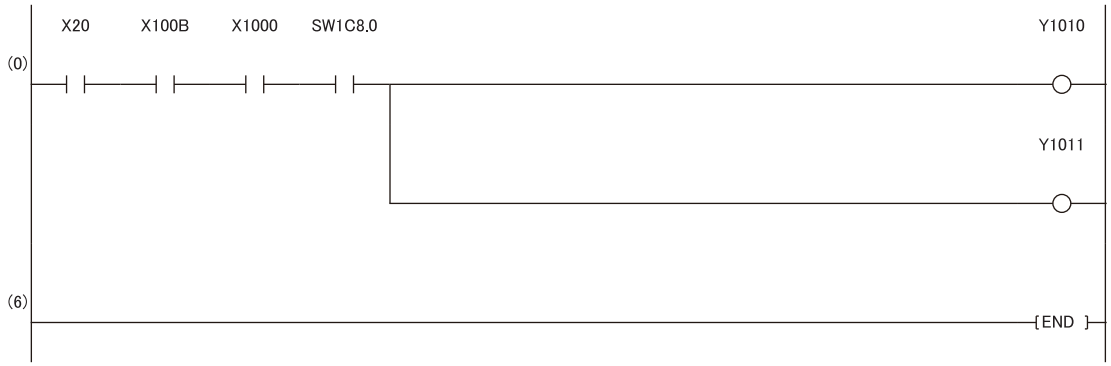
To check the operating status of the FPGA module (synchronous or asynchronous), use the following link special register (SW) on the master station.

- Synchronous/asynchronous operation status information (each station) (SW01C8 to SW01CF) of the master station

For details, refer to the following.

User's manual for the master station used

An example of a program that turns on and off External output signal Y0 (B0) and External output signal Y1 (B0) of the FPGA module with station number 1 is shown below.



- X20: Output command
- X100B: Remote READY
- X1000: FPGA controlling flag
- SW1C8.0: Synchronous/asynchronous operation status information (each station) of the station No.1
- Y1010: External output signal Y0 (B0)
- Y1011: External output signal Y1 (B0)

14.2 When Using the Inversion Output Function

This section describes the function to invert the digital signal input to External input signal X0 (B0), and output it from External output signal Y0 (B0).

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (B0)	0.15μs
Data update timing (B0)	0.1μs
Output signal selection Y0 (B0)	User circuit output
Input filter upper limit value X0 (B0)	4000

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B000H (writing data 0)	Digital control part enable/disable control register (IOB0_X0 B0) (usr_wreg_000)	0003H
1000_B0F0H (writing data 120)	Digital output control digital output selection (B0) (usr_wreg_078)	0000H

Setting method

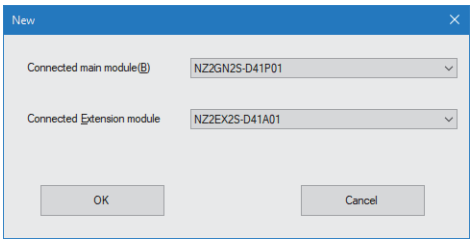
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]

Connection destination setting | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.15µs	0.15µs	0.15µs	4.00µs	4.00µs	4.00µs
Filter sampling pulse	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing
Data update timing	0.10µs	0.10µs	0.10µs	6.00µs	6.00µs	6.00µs
Logging cycle timing	1µs					
Digital input control part setting						
Input filter upper limit value						
Input filter upper limit value X0	4000	4000	4000	4000	4000	4000
Input filter upper limit value X1	4000	4000	4000	4000	4000	4000
Input filter upper limit value X2	4000	4000	4000	4000	4000	4000
Input filter upper limit value X3	4000	4000	4000	4000	4000	4000
Input filter upper limit value X4	4000	4000	4000	4000	4000	4000
Input filter upper limit value X5	4000	4000	4000	4000	4000	4000
Input filter upper limit value X6	4000	4000	4000	4000	4000	4000
Input filter upper limit value X7	4000	4000	4000	4000	4000	4000
Input filter upper limit value X8	4000	4000	4000	4000	4000	4000
Input filter upper limit value X9	4000	4000	4000	4000	4000	4000
Input filter upper limit value XA	4000	4000	4000	4000	4000	4000
Input filter upper limit value XB	4000	4000	4000	4000	4000	4000

8. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>

User circuit part parameter setting

Item	Setting Value
User circuit part parameter setting	
User circuit part parameter size	384
Writing data0 (usr_wreg_000)	0003h
Writing data1 (usr_wreg_001)	0000h
Writing data2 (usr_wreg_002)	0000h
Writing data3 (usr_wreg_003)	0000h
Writing data4 (usr_wreg_004)	0000h
Writing data5 (usr_wreg_005)	0000h
Writing data6 (usr_wreg_006)	0000h
Writing data7 (usr_wreg_007)	0000h
Writing data8 (usr_wreg_008)	0000h
Writing data9 (usr_wreg_009)	0000h
Writing data10 (usr_wreg_00A)	0000h
Writing data11 (usr_wreg_00B)	0000h
Writing data12 (usr_wreg_00C)	0000h
Writing data13 (usr_wreg_00D)	0000h
Writing data14 (usr_wreg_00E)	0000h
Writing data15 (usr_wreg_00F)	0000h
Writing data16 (usr_wreg_010)	0000h
Writing data17 (usr_wreg_011)	0000h

Guidance

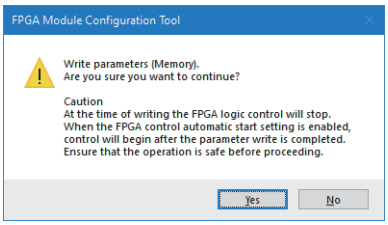
(1) Set when changing the initial value of the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)" from 0000h.
After setting, perform parameter write (Memory + Non-volatile memory) and save them into non-volatile memory.
The saved values will be stored as the initial value in the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)", when the FPGA configuration is executed such as with the power ON.
Only the initial value of the size specified in the user circuit part parameter size is stored.

OK | Cancel

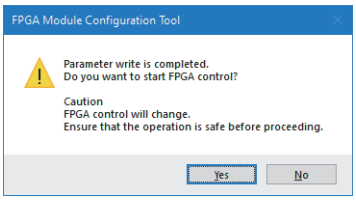
9. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

10. Click the [Yes] button.



11. Click the [Yes] button.



14.3 When Using the Pulse Count Function

This section describes the function to count pulses with the width of 100μs input to External input signals X1 (B0) and X2 (B0) with 2-phase multiple of 4 with the upper limit value of 4294967295, and to monitor them with the CPU device.

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (B0)	0.10μs
Input filter upper limit value X1 (B0)	100
Input filter upper limit value X2 (B0)	100

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B146H (writing data 163)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0) (usr_wreg_0A3)	FFFFH
1000_B148H (writing data 164)	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0) (usr_wreg_0A4)	FFFFH
1000_B14AH (writing data 165)	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	0302H

Setting method

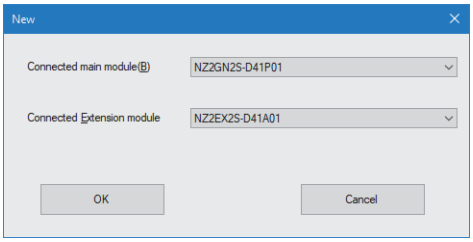
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]

Connection destination setting | Module Parameter | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.10µs	0.15µs	0.15µs	4.00µs	4.00µs	4.00µs
Filter sampling pulse	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing
Data update timing	0.10µs	0.10µs	0.10µs	6.00µs	6.00µs	6.00µs
Logging cycle timing	1µs					
Digital input control part setting						
Input filter upper limit value						
Input filter upper limit value X0	4000	4000	4000	4000	4000	4000
Input filter upper limit value X1	100	4000	4000	4000	4000	4000
Input filter upper limit value X2	100	4000	4000	4000	4000	4000
Input filter upper limit value X3	4000	4000	4000	4000	4000	4000
Input filter upper limit value X4	4000	4000	4000	4000	4000	4000
Input filter upper limit value X5	4000	4000	4000	4000	4000	4000
Input filter upper limit value X6	4000	4000	4000	4000	4000	4000
Input filter upper limit value X7	4000	4000	4000	4000	4000	4000
Input filter upper limit value X8	4000	4000	4000	4000	4000	4000
Input filter upper limit value X9	4000	4000	4000	4000	4000	4000
Input filter upper limit value XA	4000	4000	4000	4000	4000	4000
Input filter upper limit value XB	4000	4000	4000	4000	4000	4000

8. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>

User circuit part parameter setting

Item	Setting Value
User circuit part parameter setting	
User circuit part parameter size	384
Writing data0 (usr_wreg_000)	0000h
Writing data1 (usr_wreg_001)	0000h
Writing data2 (usr_wreg_002)	0000h
Writing data3 (usr_wreg_003)	0000h
Writing data4 (usr_wreg_004)	0000h
Writing data5 (usr_wreg_005)	0000h
Writing data6 (usr_wreg_006)	0000h
Writing data7 (usr_wreg_007)	0000h
Writing data8 (usr_wreg_008)	0000h
Writing data9 (usr_wreg_009)	0000h
Writing data10 (usr_wreg_00A)	0000h
Writing data11 (usr_wreg_00B)	0000h
Writing data12 (usr_wreg_00C)	0000h
Writing data13 (usr_wreg_00D)	0000h
Writing data14 (usr_wreg_00E)	0000h
Writing data15 (usr_wreg_00F)	0000h
Writing data16 (usr_wreg_010)	0000h
Writing data17 (usr_wreg_011)	0000h

Guidance

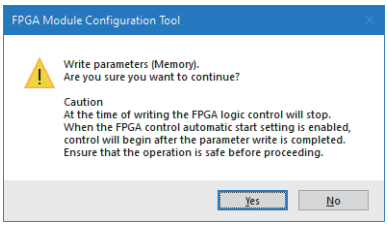
(1) Set when changing the initial value of the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)" from 0000h.
After setting, perform parameter write (Memory + Non-volatile memory) and save them into non-volatile memory.
The saved values will be stored as the initial value in the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)", when the FPGA configuration is executed such as with the power ON.
Only the initial value of the size specified in the user circuit part parameter size is stored.

OK | Cancel

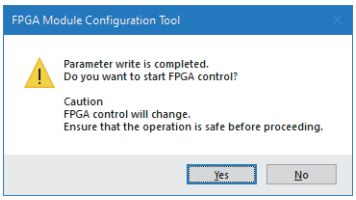
9. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

10. Click the [Yes] button.



11. Click the [Yes] button.



14.4 When Using the A/D Conversion Function

This section describes the function to A/D convert the analog value input to External input signal CH0 (E0) and monitor the value with the CPU device.

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data sampling timing (E0)	4μs
A/D conversion enable/disable setting (E0)	Conversion-enable
Select A/D conversion timing (E0)	Data sampling timing
ADC range setting CH0 (E0)	-9.9 to 9.9V
ADC oversampling ratio setting (E0)	No setting
ADC offset value CH0 (E0)	0

User circuit part parameter

The setting value of the user circuit part parameter to be set is shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384

Setting method

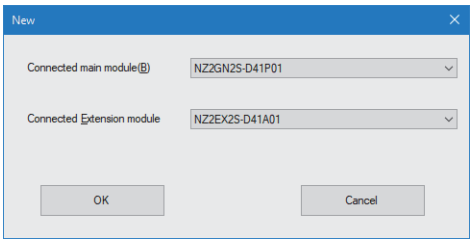
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "FPGA parameter" window, set the values of the FPGA parameters.

[Menu] ⇨ [FPGA parameter]

Connection destination setting | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
A/D conversion enable/disable setting				Conversion-enable	Conversion-disable	Conversion-disable
ADC range setting						
ADC range setting CH0				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH1				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH2				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH3				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH4				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH5				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH6				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH7				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH8				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CH9				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CHA				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC range setting CHB				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
ADC offset value						
ADC offset value CH0				0	0	0
ADC offset value CH1				0	0	0
ADC offset value CH2				0	0	0
ADC offset value CH3				0	0	0
ADC offset value CH4				0	0	0
ADC offset value CH5				0	0	0
ADC offset value CH6				0	0	0
ADC offset value CH7				0	0	0
ADC offset value CH8				0	0	0
ADC offset value CH9				0	0	0
ADC offset value CHA				0	0	0
ADC offset value CHB				0	0	0
Select A/D conversion timing				Data sampling timing	Data sampling timing	Data sampling timing
ADC oversampling ratio setting				No setting	No setting	No setting
Analog output control part setting						
D/A conversion enable/disable setting						
D/A conversion enable/disable setting CH0				Conversion-disable	Conversion-disable	Conversion-disable
D/A conversion enable/disable setting CH1				Conversion-disable	Conversion-disable	Conversion-disable

8. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>

User circuit part parameter setting

Item	Setting Value
User circuit part parameter setting	
User circuit part parameter size	384
Writing data0 (usr_wreg_000)	0000h
Writing data1 (usr_wreg_001)	0000h
Writing data2 (usr_wreg_002)	0000h
Writing data3 (usr_wreg_003)	0000h
Writing data4 (usr_wreg_004)	0000h
Writing data5 (usr_wreg_005)	0000h
Writing data6 (usr_wreg_006)	0000h
Writing data7 (usr_wreg_007)	0000h
Writing data8 (usr_wreg_008)	0000h
Writing data9 (usr_wreg_009)	0000h
Writing data10 (usr_wreg_00A)	0000h
Writing data11 (usr_wreg_00B)	0000h
Writing data12 (usr_wreg_00C)	0000h
Writing data13 (usr_wreg_00D)	0000h
Writing data14 (usr_wreg_00E)	0000h
Writing data15 (usr_wreg_00F)	0000h
Writing data16 (usr_wreg_010)	0000h
Writing data17 (usr_wreg_011)	0000h

Guidance

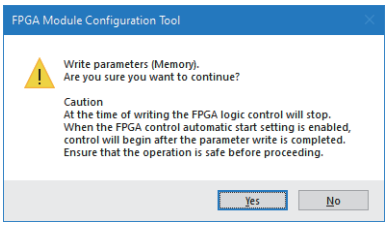
(1) Set when changing the initial value of the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)" from 0000h.
After setting, perform parameter write (Memory + Non-volatile memory) and save them into non-volatile memory.
The saved values will be stored as the initial value in the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)", when the FPGA configuration is executed such as with the power ON.
Only the initial value of the size specified in the user circuit part parameter size is stored.

OK | Cancel

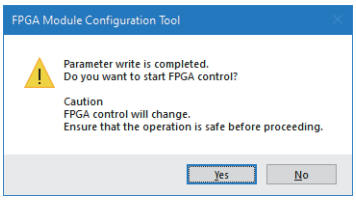
9. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

10. Click the [Yes] button.



11. Click the [Yes] button.



14.5 When Using the D/A Conversion Function

This section describes the function to D/A convert the digital value set by the FPGA register and output the converted analog value to External output signal CH0 (E0).

FPGA parameter

The setting values of the FPGA parameters to be used are shown below.

Setting item	Setting value
D/A conversion enable/disable setting CH0 (E0)	Conversion-enable
Select D/A conversion value (E0)	User circuit output
Select D/A conversion timing (E0)	User circuit output
Select DAC LDAC signal (E0)	User circuit output
DAC offset value CH0 (E0)	0
DAC range setting CH0 (E0)	-9.9 to 9.9V

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B2C0H (writing data 352)	Analog output part LDAC output selection (usr_wreg_160)	0001H

Setting method

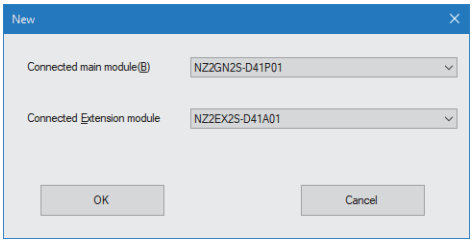
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

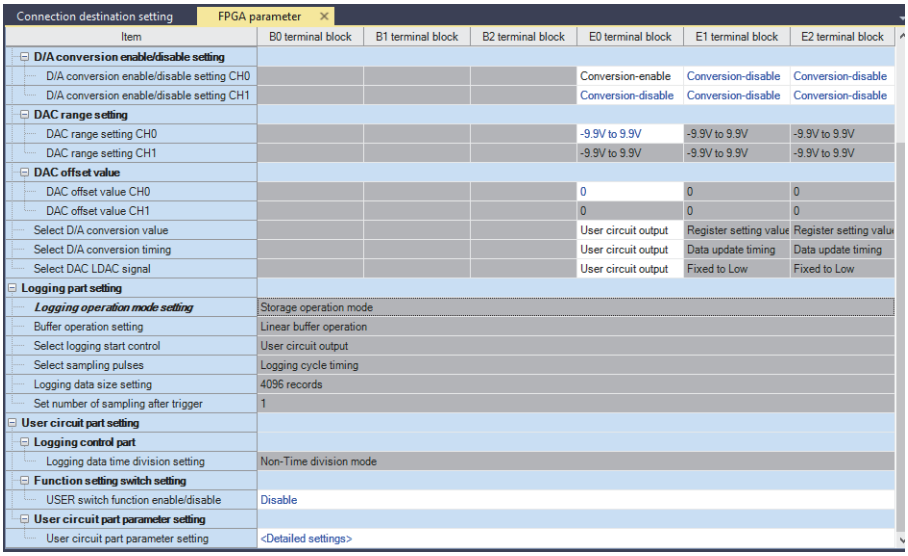
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "FPGA parameter" window, set the values of the FPGA parameters.

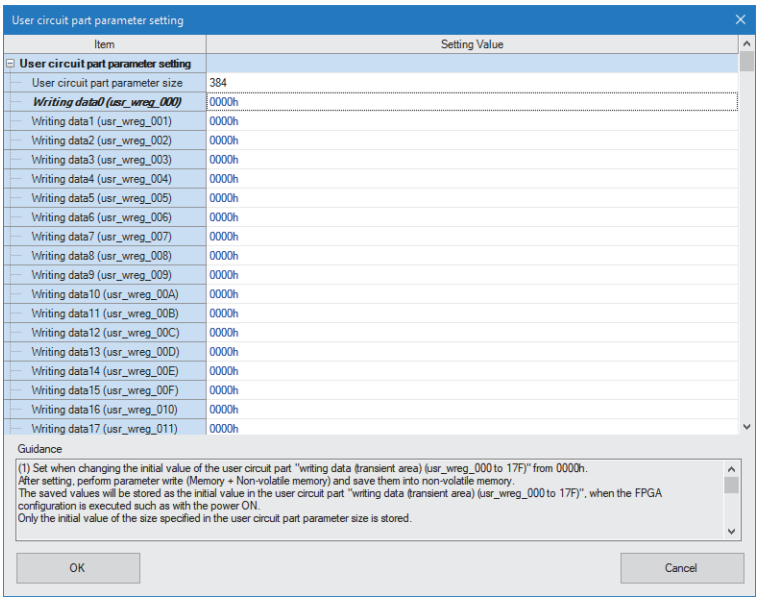
[Menu] ⇨ [FPGA parameter]



Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
D/A conversion enable/disable setting						
D/A conversion enable/disable setting CH0				Conversion-enable	Conversion-disable	Conversion-disable
D/A conversion enable/disable setting CH1				Conversion-disable	Conversion-disable	Conversion-disable
DAC range setting						
DAC range setting CH0				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
DAC range setting CH1				-9.9V to 9.9V	-9.9V to 9.9V	-9.9V to 9.9V
DAC offset value						
DAC offset value CH0				0	0	0
DAC offset value CH1				0	0	0
Select D/A conversion value				User circuit output	Register setting value	Register setting value
Select D/A conversion timing				User circuit output	Data update timing	Data update timing
Select DAC LDAC signal				User circuit output	Fixed to Low	Fixed to Low
Logging part setting						
Logging operation mode setting	Storage operation mode					
Buffer operation setting	Linear buffer operation					
Select logging start control	User circuit output					
Select sampling pulses	Logging cycle timing					
Logging data size setting	4096 records					
Set number of sampling after trigger	1					
User circuit part setting						
Logging control part						
Logging data time division setting	Non-Time division mode					
Function setting switch setting						
USER switch function enable/disable	Disable					
User circuit part parameter setting						
User circuit part parameter setting	<Detailed settings>					

8. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



Item	Setting Value
User circuit part parameter setting	
User circuit part parameter size	384
Writing data0 (usr_wreg_000)	0000h
Writing data1 (usr_wreg_001)	0000h
Writing data2 (usr_wreg_002)	0000h
Writing data3 (usr_wreg_003)	0000h
Writing data4 (usr_wreg_004)	0000h
Writing data5 (usr_wreg_005)	0000h
Writing data6 (usr_wreg_006)	0000h
Writing data7 (usr_wreg_007)	0000h
Writing data8 (usr_wreg_008)	0000h
Writing data9 (usr_wreg_009)	0000h
Writing data10 (usr_wreg_00A)	0000h
Writing data11 (usr_wreg_00B)	0000h
Writing data12 (usr_wreg_00C)	0000h
Writing data13 (usr_wreg_00D)	0000h
Writing data14 (usr_wreg_00E)	0000h
Writing data15 (usr_wreg_00F)	0000h
Writing data16 (usr_wreg_010)	0000h
Writing data17 (usr_wreg_011)	0000h

Guidance

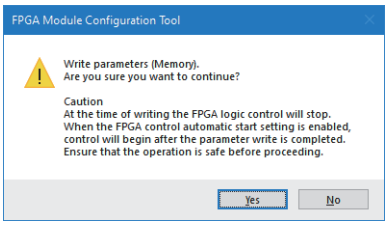
(1) Set when changing the initial value of the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)" from 0000h.
After setting, perform parameter write (Memory + Non-volatile memory) and save them into non-volatile memory.
The saved values will be stored as the initial value in the user circuit part "writing data (transient area) (usr_wreg_000 to 17F)", when the FPGA configuration is executed such as with the power ON.
Only the initial value of the size specified in the user circuit part parameter size is stored.

OK Cancel

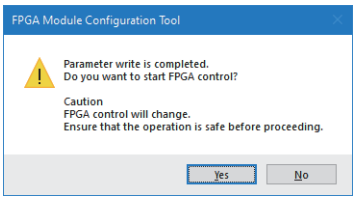
9. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

10. Click the [Yes] button.



11. Click the [Yes] button.



14.6 When Using the Pulse Output Function

This section describes the function to generate 100 pulses with the pulse width of 100μs and output them to External output signal Y1 (B0). Note that the digital signal is shown for 1-phase multiple of 1.

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Data update timing (B0)	0.1μs
Output signal selection Y1 (B0)	User circuit output

User circuit part parameter

The setting values of the user circuit part parameters to be set are shown below.

Address	Setting item	Setting value
—	User circuit part parameter size	384
1000_B0F0H (writing data 120)	Digital output control digital output selection (B0) (usr_wreg_078)	0002H
1000_B220H (writing data 272)	Pulse output part pulse width upper limit value (lower side) (B0) (usr_wreg_110)	270FH (100μs)
1000_B222H (writing data 273)	Pulse output part pulse width upper limit value (upper side) (B0) (usr_wreg_111)	0000H
1000_B224H (writing data 274)	Pulse output part output pulse count upper limit value (lower side) (B0) (usr_wreg_112)	0064H (100 pulses)
1000_B226H (writing data 275)	Pulse output part output pulse count upper limit value (upper side) (B0) (usr_wreg_113)	0000H
1000_B260H (writing data 304)	Pulse output part pulse output selection 0 (B0) (usr_wreg_130)	0000H
1000_B284H (writing data 322)	Pulse output part pulse output mask 0 (B0) (usr_wreg_142)	0002H

Setting method

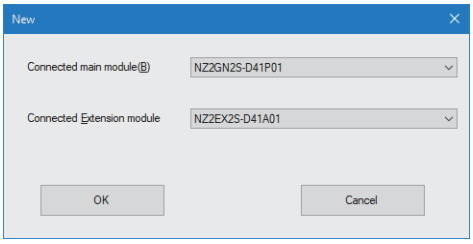
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

7. From the "FPGA parameter" window, set the values of the FPGA parameters.

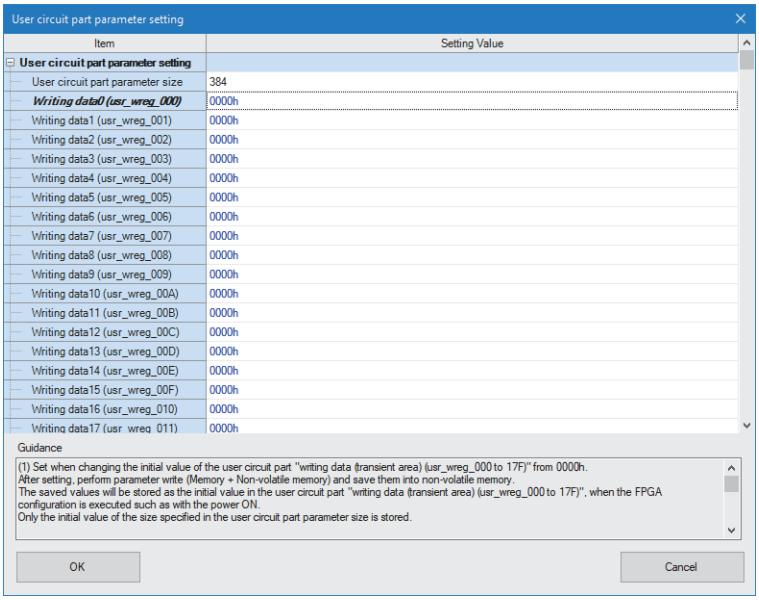
[Menu] ⇨ [FPGA parameter]

Connection destination setting | FPGA parameter

Item	B0 terminal block	B1 terminal block	B2 terminal block	E0 terminal block	E1 terminal block	E2 terminal block
Reset control part setting						
External reset ON/OFF	ON	ON	ON	ON		
Timing control part setting						
Data sampling timing	0.15μs	0.15μs	0.15μs	4.00μs	4.00μs	4.00μs
Filter sampling pulse	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing	Data sampling timing
Data update timing	0.10μs	0.10μs	0.10μs	6.00μs	6.00μs	6.00μs
Logging cycle timing	1μs					
Digital input control part setting						
Digital output control part setting						
Output signal selection						
Output signal selection Y0	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y1	User circuit output	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y2	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y3	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y4	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y5	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y6	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y7	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y8	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection Y9	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)
Output signal selection YA	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)	Register setting value (RY)

8. Set the values of the user circuit part parameters in the "User circuit part parameter setting" window.

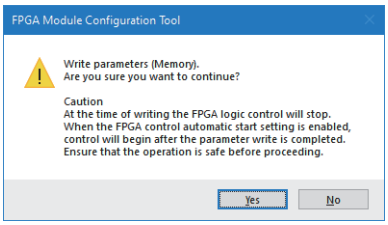
[Menu] ⇨ [FPGA parameter] ⇨ [User circuit part parameter setting] ⇨ <Detailed settings>



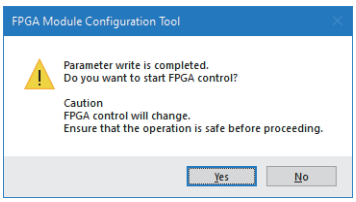
9. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

10. Click the [Yes] button.



11. Click the [Yes] button.



14.7 When Using the Logging Function

This section describes how to log the value of 32-bit ring counters used in the usage example of the counter control part.
In addition to the parameters set as described in the section below, set the parameters as described on this page.
☞ Page 405 When Using the Pulse Count Function

Module parameter

The setting values of the module parameters are shown below.

Setting item	Setting value
Logging function enable/disable	Enable
Logging data file storage type	CSV Files
CSV Format setting 0 (bit0~bit15)	Bit, binary format
CSV Format setting 6 (bit96~bit111)	Bit, binary format
CSV Format setting 7 (bit112~bit127)	Double Word [Unsigned], decimal format
FTP server IP address	IP address of the FTP server to be used
Login name	Login name of the FTP server to be used
Password	Password of the FTP server to be used

FPGA parameter

The setting values of the FPGA parameters to be set are shown below.

Setting item	Setting value
Logging cycle timing	1μs
Logging operation mode setting	Storage operation mode
Buffer operation setting	Linear buffer operation
Select logging start control	Register setting value (RY3)
Select sampling pulses	Logging cycle timing
Logging data size setting	256 records

Setting method

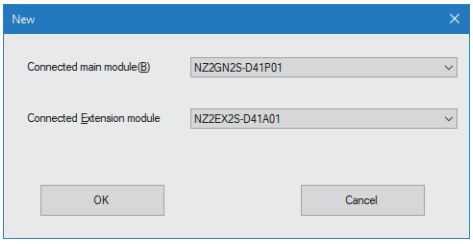
The procedure using the FPGA Module Configuration Tool is shown below.

Operating procedure

1. Create the project with the following settings.

Set NZ2GN2S-D41P01 as the connected main module and NZ2EX2S-D41A01 as the connection extension module.

[Project] ⇨ [New]



2. Click the [OK] button.

3. Enter the IP address of the FPGA module to be connected in the "Connection destination setting" window.

[Menu] ⇨ [Connection destination setting]

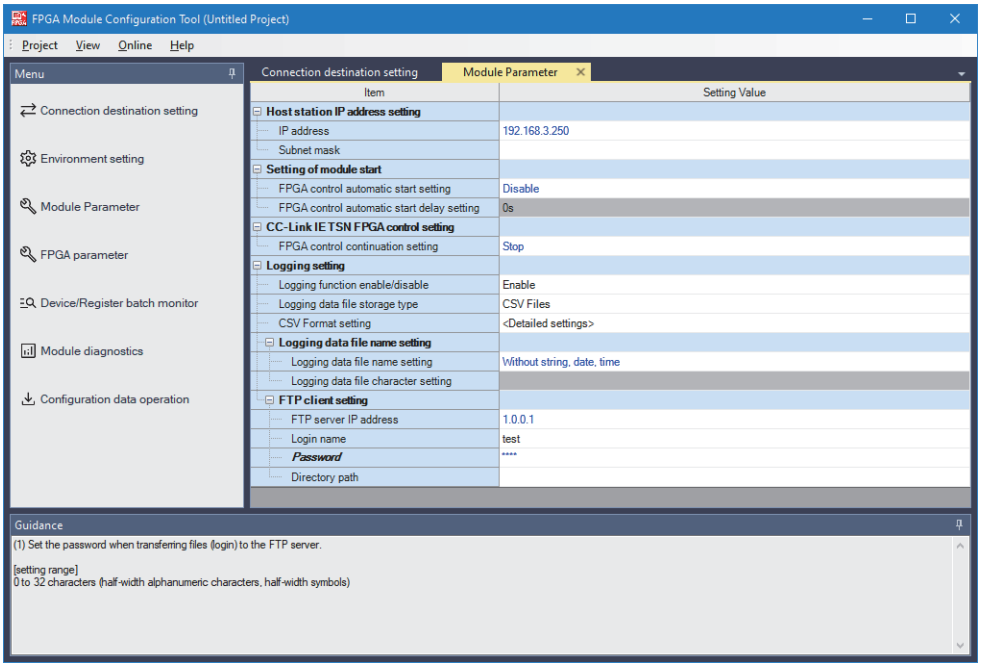
4. Click the [Communication Test] button.

5. Click the [OK] button.

6. Click the [Apply] button.

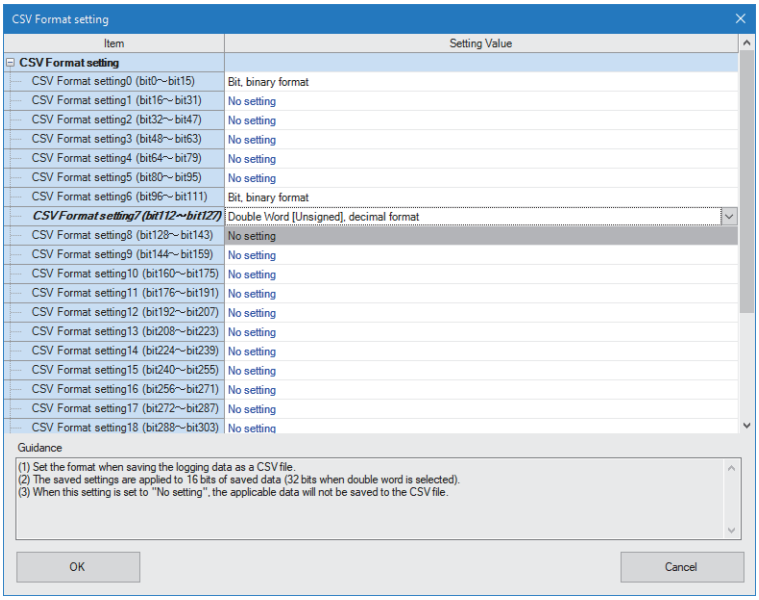
7. From the "Module Parameter" window, set the values of the module parameters.

[Menu] ⇨ [Module Parameter]



8. Set the value of the CSV format setting in the "CSV Format setting" window.

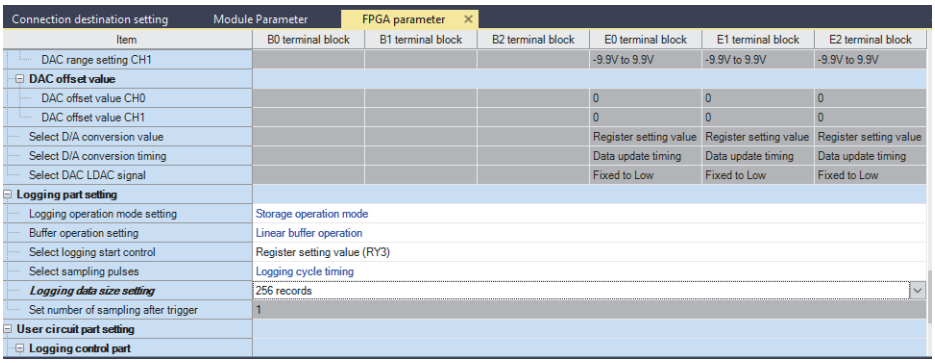
[Menu] ⇨ [Module Parameter] ⇨ [Logging setting] ⇨ [CSV Format setting] ⇨ <Detailed settings>



9. Click the [OK] button.

10. From the "FPGA parameter" window, set the values of the FPGA parameters.

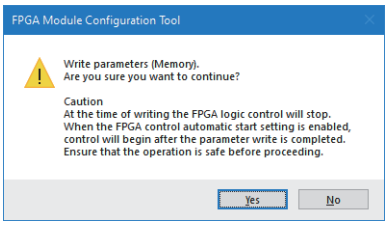
[Menu] ⇨ [FPGA parameter]



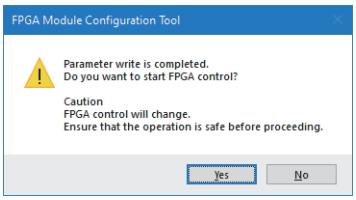
11. Write the set parameters.

[Online] ⇨ [Parameter write (Memory + Non-volatile memory)]

12. Click the [Yes] button.



13. Click the [Yes] button.



14.8 Program Examples

This section describes program examples for using the functions of the sample circuit.

Devices to be used

■Common device

Device	Description
SB0049	Data link status of the own station (master station)
SW00B0.0	Data link status of each station (station number 1)
N0	Nesting (station number 1)
M0	Communication ready flag (station number 1)
X100A	Error flag
W1000	Latest error code
D10	Storage variable for the latest error code
X20	FPGA control start/stop command
X21	Error clear command
Y100A	Error clear request flag
X1000	FPGA controlling flag
X100B	Remote READY
Y1000	FPGA control start request

■Devices to be used for the inversion output function

None

■Devices to be used in the pulse count function

Device	Description
X22	Preset data setting command
X23	Preset data write command
D20	Counter value storage register (lower)
D21	Counter value storage register (upper)
D22	Preset data setting value storage register (lower)
D23	Preset data setting value storage register (upper)
W1043	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B0)
W1044	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B0)
W1118	32-bit ring counter (2-phase multiple of 4) preset instruction (B0)
W1119	32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0)
W111A	32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0)

■Devices to be used for the A/D conversion function

Device	Description
D30	A/D conversion value CH0 (E0) storage register
W101F	Analog control A/D conversion value CH0 (E0)

■Devices to be used for the D/A conversion function

Device	Description
X24	Analog output enable command
D40	D/A conversion value CH0(E0) storage register
W1150	Analog output part D/A conversion value CH0 (E0)
W1156	Analog output part D/A conversion value enable (usr_wreg_1C6)

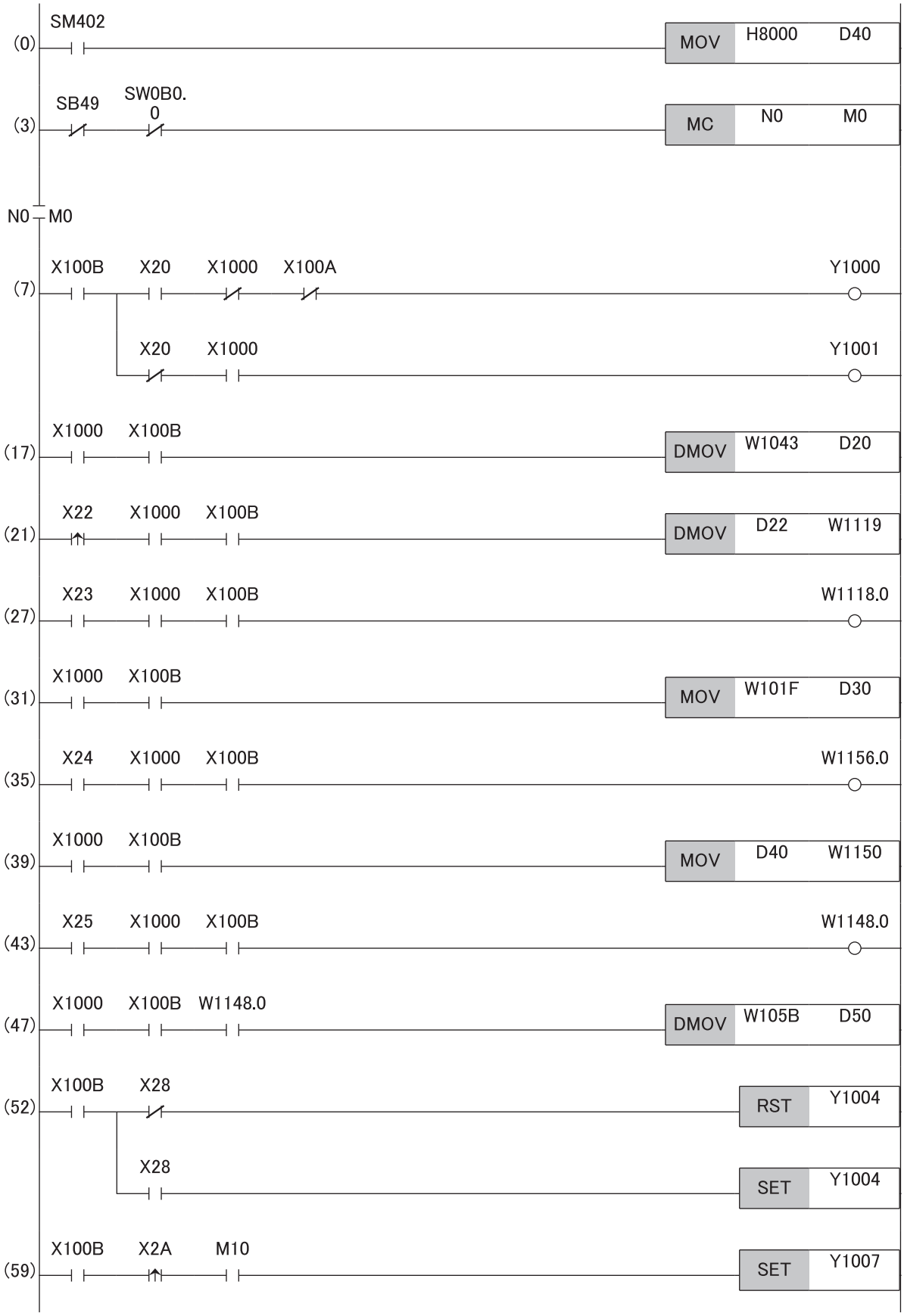
■Devices to be used for the pulse output function

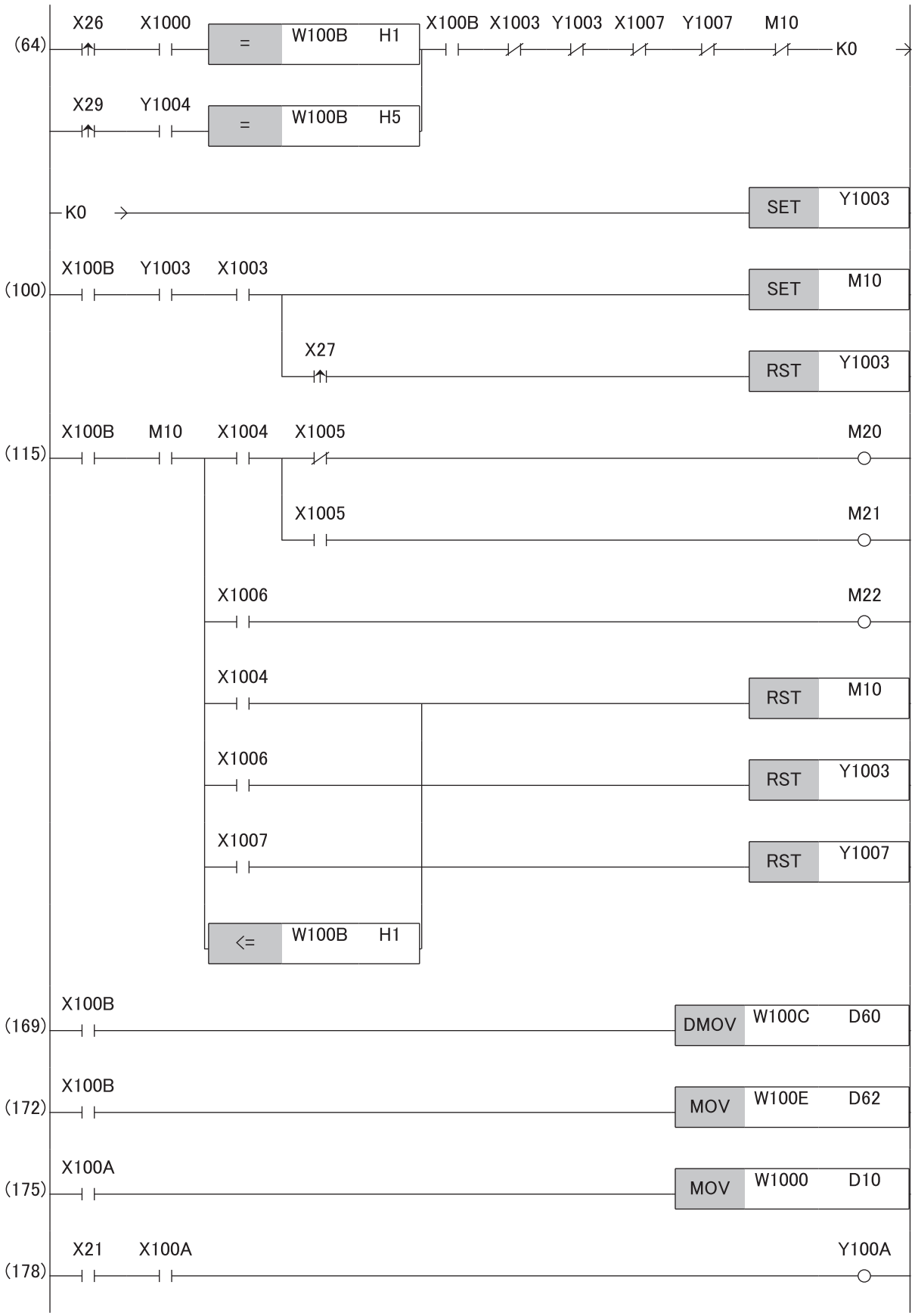
Device	Description
X25	Pulse output enable command
D50	Output pulse count (B0) (lower side)
D51	Output pulse count (B0) (upper side)
W105B	Pulse output part output pulse count (lower side) (B0)
W105C	Pulse output part output pulse count (upper side) (B0)
W1148	Pulse output part pulse output enable (B0)

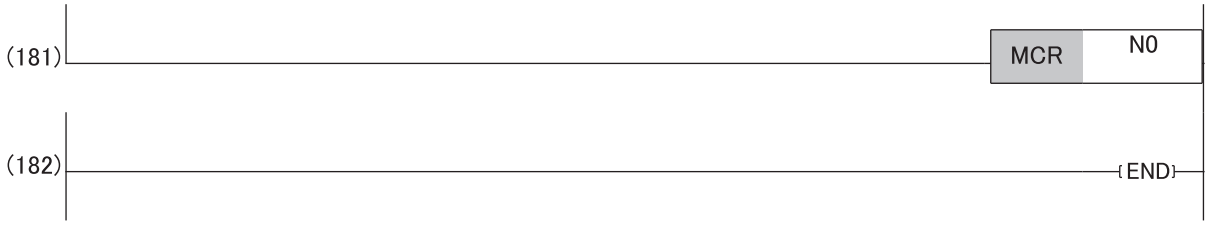
■Devices to be used by the logging function

Device	Description
X26	Logging start command
X27	Logging stop command
X28	Logging data resend allowed command
X29	Logging data resend command
X2A	Logging control suspend command
M20	Logging data transfer completion flag
M21	Logging data transfer error completion flag
M22	FPGA control stop while data collection flag
X1003	Logging start request flag
Y1003	Logging start request
Y1004	FTP resend allowed
X1004	FTP transfer completion flag
X1005	FTP transfer error completion flag
X1006	FPGA control stop while data collection flag
X1007	Logging control suspension flag
Y1007	Logging control suspend request
D60	Sampling number monitor (lower side)
D61	Sampling number monitor (upper side)
D62	FTP transfer count monitor
W100B	Logging operation state monitor
W100C	Sampling count monitor (lower side)
W100D	Sampling count monitor (upper side)
W100E	FTP transfer count monitor
M10	Logging start acceptance flag

Program example




(64)
X26
X1000
=
W100B
H1
X100B
X1003
Y1003
X1007
Y1007
M10
K0
X29
Y1004
=
W100B
H5
K0
SET
Y1003
(100)
X100B
Y1003
X1003
SET
M10
X27
RST
Y1003
(115)
X100B
M10
X1004
X1005
M20
X1005
M21
X1006
M22
X1004
RST
M10
X1006
RST
Y1003
X1007
RST
Y1007
<=
W100B
H1
(169)
X100B
DMOV
W100C
D60
(172)
X100B
MOV
W100E
D62
(175)
X100A
MOV
W1000
D10
(178)
X21
X100A
Y100A



(7) Start FPGA control.
Start FPGA control when FPGA control start/stop command (X20) is ON.
Stop FPGA control when FPGA control start/stop command (X20) is OFF.
(17)Monitor the count value when the pulse count function is used.
(21)Set the preset data when the pulse count function is used.
(27)Preset the counter value when the pulse count function is used.
(31)When using the A/D conversion function, store the A/D conversion value in D30.
(35)When using the D/A conversion function, set Analog output part D/A conversion value enable (usr_wreg_1C6) to Enable.
(39)When using the D/A conversion function, set the digital value of the voltage output from CH0 (E0).
(43)When using the pulse output function, set the pulse output enable to Enable and start pulse output.
(47)When using the pulse output function, monitor the number of pulses being output.
(52)When using the logging function, set the FTP resend allowed.
(59)When using the logging function, stop collecting or transferring logging data.
(64)When using the logging function, collect or transfer logging data.
(115)When using the logging function, check the transfer status of logging data.
(169)When using the logging function, store the number of samples in D60.
(172)When using the logging function, store the number of FTP transfers in D62.
(175)Store the latest error code in D10.
(178)Clear an error.

MEMO

PART 8 TROUBLESHOOTING

This part consists of the following chapters.

15 MAINTENANCE AND INSPECTION

There is no special item to be inspected for the FPGA module. However, to maintain the best condition of the system, perform the inspection in accordance with the items described in the following manual.

MELSEC iQ-R Module Configuration Manual

MEMO

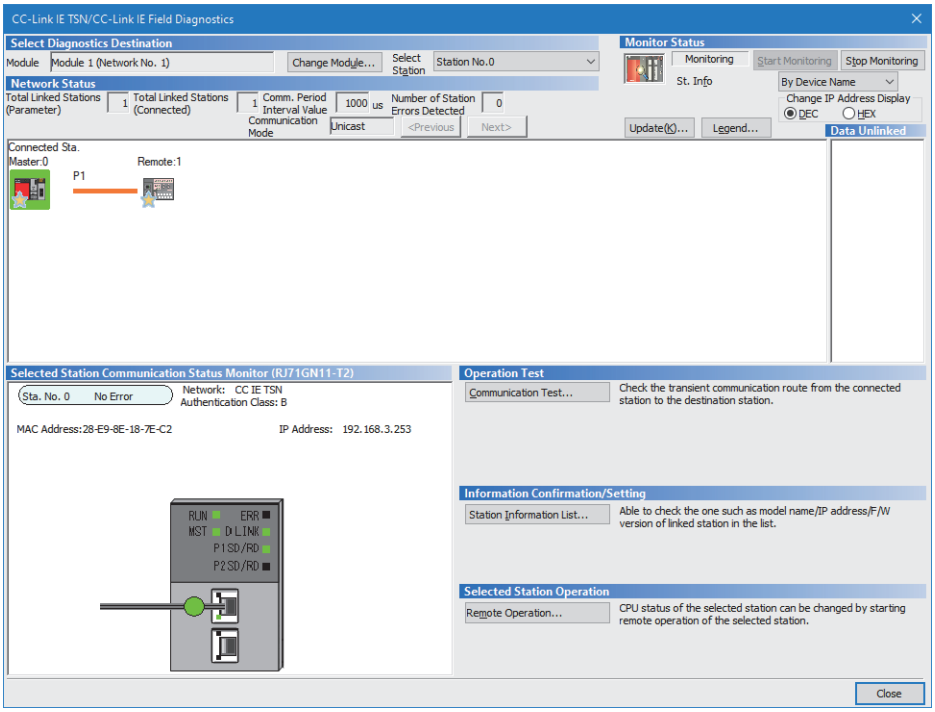
16 CC-Link IE TSN/CC-Link IE Field DIAGNOSTICS

For CC-Link IE TSN, monitor the status and conduct an operation test.
For details on CC-Link IE TSN/CC-Link IE Field diagnostics, refer to the following.
📖 User's manual for the master station used

Remote reset

Perform the following operation to remotely reset a selected FPGA module.

1. Select a device station to be reset and click the [Remote Operation] button.



2. Follow the on-screen instructions and click the [Yes] button.

3. Follow the on-screen instructions and click the [OK] button.

Precautions

■Remote reset

Remote reset of the FPGA module may cause the following because it affects communications on another station.

- Another station is disconnected.

■Setting of function setting switches

When remote reset is performed, if the setting of function setting switch 1, 2, or 3 is different from the setting at power-on, a Remote reset disable error (error code: 1090H) occurs, and the FPGA module is not reset.

Checking station information

The information of the FPGA module in data linking is displayed on the "Station Information List" window.
Information on the FPGA module, such as the production information, firmware version, and module-specific information, can be checked by clicking the [Station Information List] button in the "CC-Link IE TSN/CC-Link IE Field Diagnostics" window.
The FPGA module displays the current status of function setting switches or the status of the switches when the power is turned on, as module-specific information.
The setting status of function setting switches is treated as a bit string and displayed as a hexadecimal value.

- Function setting switches 1 to 3: Status of the function setting switches when the power is turned on
- Function setting switches 4 to 10: Current status of the function setting switches

Ex.
When function setting switches 5 and 7 are ON: Module-specific information is "0028".

Point

For items displayed in the "Station Information List" window, refer to the following.
User's manual for the master station used

17 MODULE DIAGNOSTICS WITH THE FPGA MODULE CONFIGURATION TOOL

The FPGA Module Configuration Tool displays the basic information of the FPGA module and monitors the status.
For details on module diagnostics using the FPGA Module Configuration Tool, refer to the following.
☞ Page 121 Module diagnostics

MEMO

18 CHECKING THE LEDS

This section describes how to troubleshoot the system by the LEDs.

When the PW LED does not turn on

When the PW LED does not turn on, check the following items.

Check item	Action
Is any LED other than the PW LED turned on?	When any LED other than the PW LED turns on, the possible cause is a hardware error. Please consult your local Mitsubishi representative.
Is the module power supply (24VDC) wired?	Wire the module power supply (24VDC).
Is the module power supply (24VDC) turned on?	Turn on the module power supply (24VDC).
Is the voltage of the module power supply (24VDC) within the specified range?	Set the voltage value within the range of performance specifications.

When the RUN LED does not turn on

When the RUN LED does not turn on, check the following items.

Check item	Action
Has any hardware error occurred?	Turn off and on the module power supply. If the RUN LED does not turn on even after the module power supply is turned off and on, the possible cause is a module failure. Please consult your local Mitsubishi representative.

When the RUN LED flashes

When the RUN LED flashes, check the following items.

Check item	Action
Is the FPGA module in execution of the unit test?	• When the FPGA module is in execution of the unit test, the RUN LED turns on after the unit test is completed. Take corrective action according to the result of the unit test. • When a unit test is not conducted, set the IP address/station number setting switches to an appropriate value.

When the FPGA RUN LED does not turn on

When the FPGA RUN LED does not turn on, check the following item.

Check item	Action
Is FPGA control flag (RX0) ON?	• Turn on FPGA control start request (RY0) to start FPGA control. • The conditions under which FPGA control can be started differ depending on the "FPGA control automatic start setting" and "FPGA control continuation setting" settings and the operating status of the master station and CPU module. For details, refer to the following. ☞ Page 315 FPGA Control Function

When the P1 LINK LED or P2 LINK LED turns off

When the P1 LINK LED or P2 LINK LED turns off, check the following items.

Check item	Action
Are Ethernet cables used compliant with the relevant standard?	Replace the cable with an Ethernet cable compliant with the relevant standard. 📖 User's manual for the master station used
Is the segment length 100m or less?	Change the segment length to 100m or less.
Does the cabling condition (bending radius) meet the specifications?	Refer to the manual for the Ethernet cable used, and correct the bending radius.
Is any Ethernet cable disconnected?	Replace the Ethernet cable.
Do the switching hub and other stations used in the system operate normally?	• Check that the switching hub and other stations are powered on. • Check that the switching hub used is compatible with the specifications of the master station used. (📖 User's manual for the master station used) • Disconnect Ethernet cables, and then reconnect them. • Power off and on the switching hub.
Is the communication speed of the FPGA module same as that of a device connected to the module?	When the function setting switch 3 is set to OFF, connect to a device that can communicate at 1Gbps, and when it is set to ON, connect to a device that can communicate at 100Mbps.
When the communication speed of the FPGA module is set to 100Mbps, is auto-negotiation of the connected device enabled?	Enable auto-negotiation of the connected device. Or connect the FPGA module to a device where the auto-negotiation is enabled.

Point

If link-up processing is repeated due to a condition of a device on the line, it may take a longer time for the P1 LINK LED/P2 LINK LED to turn on. This phenomenon may be eliminated by changing the connector of the relevant module to which the Ethernet cable is connected (example: P1 → P2).

For details on Ethernet cable wiring, refer to the following.

☞ Page 68 Ethernet cables

When the DATA LINK LED turns off

When the DATA LINK LED turns off in CC-Link IE TSN communication mode, check the following items.

Check item	Action
Are Ethernet cables used compliant with the relevant standard?	Replace the cable with an Ethernet cable compliant with the relevant standard. 📖 User's manual for the master station used
Is the segment length 100m or less?	Change the segment length to 100m or less.
Does the cabling condition (bending radius) meet the specifications?	Refer to the manual for the Ethernet cable used, and correct the bending radius.
Is any Ethernet cable disconnected?	Replace the Ethernet cable.
Do the switching hub and other stations operate normally?	• Check that the switching hub and other stations are powered on. • Check that the switching hub used is compatible with the specifications of the master station used. (www.cc-link.org) • Disconnect Ethernet cables, and then reconnect them. • Power off and on the switching hub.
Does the master station connected to the network operate normally?	• If an error occurs in the master station, clear the error in the master station. • Check that the master station in use is a supported master station. (☞ Page 26 Supported master station)
Is another module that is powered off or in the middle of remote reset connected between the master station and the FPGA module?	• Power on the FPGA module(s) that is off because an FPGA module becomes disconnected when it is off. • The FPGA module becomes disconnected during remote reset. Avoid unnecessary remote reset.
Does the module between the master station and the FPGA module link up at the desired communication speed?	Change the communication speed of the module or the switching hub to satisfy the communication speed.
Is the IP address of the FPGA module duplicated by any of other devices within the access range of CC-Link IE TSN?	Change the IP address so that no IP address duplication occurs in the access range of CC-Link IE TSN.
Is a device that is operating as a network other than CC-Link IE TSN connected between the master station and the FPGA module?	Disconnect a device that is not operating as CC-Link IE TSN from the system. For a device that can be set to operate on CC-Link IE TSN, check that it is operating as CC-Link IE TSN.
Is the module running in standalone mode?	Turn off function setting switch 1 if it is turned on, and turn off and on the module power supply.

When the DATA LINK LED flashes

When the DATA LINK LED flashes in CC-Link IE TSN communication mode, check the following items.

Check item	Action
Do the IP addresses match?	Match the IP address of the FPGA module with the IP address that is set in the network configuration settings of the master station.
Does the station type match?	Match the station type of the FPGA module with the station type that is set in the network configuration settings of the master station.
Is the FPGA module a reserved station?	Change the setting of reserved/error invalid station to other than the reserved station in the network configuration settings of the master station.
Is the IP address of the FPGA module duplicated with that of other station?	At least two IP addresses are overlapped. Change the setting so that all IP addresses differ.
In the network configuration settings of the master station, is the third or fourth octet of the IP address duplicated by that of another station?	Set the IP addresses so that there is no duplication in the third and fourth octets of the IP addresses for all the stations.
In the network configuration settings of the master station, does each network address (the subnet mask part of IP address) match that of the master station?	Set each IP address and subnet mask so that the network addresses of all the stations are the same.
Is another station in which a communication error has occurred connected between the master station and the FPGA module?	The FPGA module cannot establish data link if there is no path available with which the FPGA module can communicate with the master station without relaying data via a station with a communication error. If a communication error has occurred in two or more stations, clear the error one by one, starting from the station closest to the master station on the communication path.
Has another station been remotely reset or powered off?	Disconnection temporarily occurs due to remote reset or power-off of another station. Wait until communication restarts.
Does a station on the network link up at the desired communication speed?	Change the communication speed of the module or the switching hub to satisfy the communication speed.
Does the time synchronization source module operate normally?	• If an error occurs in the time synchronization source module, clear the error. • When the time synchronization source module is reset or powered off, disconnection temporarily occurs due to switching of time synchronization sources. Wait until communication restarts.
Is a time synchronization source module with a higher priority newly connected to the network?	Disconnection temporarily occurs due to switching of time synchronization sources. Wait until communication restarts.
Does the master station connected to the network operate normally?	If an error occurs in the master station, clear the error in the master station.
Does the model name of the device station set in the network configuration settings match the model name of the actual device?	Change the network configuration settings so that the model name of the device station set in the network configuration settings matches the model name of the actual device. Or, in the network configuration settings, set the FPGA module as a "general-purpose remote station".
Is the event code of 00C81H registered for the FPGA module with event history of the master station?	Change the CC-Link IE TSN Class in the network configuration settings so that the CC-Link IE TSN Class set in the network configuration settings matches the CC-Link IE TSN Class of the FPGA module. Alternatively, change the CC-Link IE TSN Class of the FPGA module.
Is the event code of 00C71H registered for the FPGA module with event history of the master station?	The CC-Link IE TSN Network synchronous communication function may be set to "Synchronous" for FPGA modules that have the CC-Link IE TSN Class setting set to CC-Link IE TSN Class A. In this case, set the CC-Link IE TSN Network synchronous communication function to "Asynchronous" or set the CC-Link IE TSN Class of the FPGA module to "CC-Link IE TSN Class B". If the event code of 00C71H is still registered even after the above actions are taken, check the manual for the master station in use and eliminate the cause.
Are the IP address and subnet mask that can be used for the FPGA module set in the network configuration settings?	Set the IP address and subnet mask that can be used for the FPGA module. (☞ Page 54 IP address/ station number setting switch setting)
In the network configuration settings, are the number of points set for RX and RY within the range that can be used for the FPGA module?	Set 112 or less for the number of points each for RX and RY.
In the network configuration settings, are the number of points set for RWr and RWw within the range that can be used for the FPGA module?	Set 144 or less for the number of points for each of RWr and RWw.
When the CC-Link IE TSN Network synchronous communication function is used, is the set synchronization cycle supported by the FPGA module?	When using the CC-Link IE TSN Network synchronous communication function, set values in the range that the FPGA module supports for the synchronous cycle. (☞ Page 353 CC-Link IE TSN Network Synchronous Communication Function)

Check item	Action
Has any error occurred in the FPGA module?	If an error has occurred in the FPGA module, a network parameter may be set to a value that the FPGA module cannot handle. If following errors have occurred, eliminate them in order from the top one. (☞ Page 443 TROUBLESHOOTING DURING FPGA DEVELOPMENT) • Communication cycle setting error (1Gbps) (error code: D023H) • Communication cycle setting error (100Mbps) (error code: D024H) • Communication cycle setting error (CC-Link IE TSN Class A) (error code: D028H) • Number of RX/RY points error (error code: D021H) • RWr/RWw number of points error (error code: D022H) • Synchronization cycle setting error (error code: D026H) • RWw/RWr setting error (error code: D025H) • Network synchronous communication setting error (error code: D020H) • Network synchronous communication setting change disable error (error code: D027H) • Communication setting error 2 (error code: D001H) • Communication setting error 1 (error code: D000H)
Has ring topology been configured?	When the CC-Link IE TSN Class of the FPGA module is CC-Link IE TSN Class A, set it to CC-Link IE TSN Class B or connect with line topology, star topology, or a mixture of star topology and line topology.
Is the CC-Link IE TSN Class of the FPGA module set to CC-Link IE TSN Class A?	If the CC-Link IE TSN Class setting of the FPGA module is set to CC-Link IE TSN Class A, take the following action. • Check the version of the master station, and if the version does not support CC-Link IE TSN Protocol version 2.0, please update the master station to the corresponding version. If the "Communication Period Setting" of the FPGA module is "Low-Speed", check CC-Link IE TSN Class A (Low-Speed) multiple (buffer memory address: 1294304) of the master module buffer memory. If the value of CC-Link IE TSN Class A (Low-Speed) multiple (buffer memory address: 1294304) is 6 or higher, set the value of basic period × multiple × CC-Link IE TSN Class A (Low-Speed) multiple (buffer memory address: 1294304) to 2.5ms or higher and 6.4 seconds or lower in the communication period interval settings. For details, refer to the manual for the master station used.
Is the network overloaded?	Reduce the load on the network. • If a broadcast storm has occurred, eliminate the cause. • If an Ethernet device is connected, reduce the frequency of packets sent by the Ethernet device.

When the ERR. LED turns on or flashes

When the ERR. LED turns on or flashes, check the following items.

Check item	Action
Has any error occurred?	Identify the cause of the error from the "CC-Link IE TSN/CC-Link IE Field Diagnostics" window, Latest error code (RWr0), or the value of the FPGA Module Configuration Tool, and take corrective action.

When the FPGA CONF. LED does not turn on

When the FPGA CONF. LED does not turn on, check the following item.

Check item	Action
Did the download of configuration data fail?	After downloading the configuration data, turn on the module power off and on. (☞ Page 300 FPGA Download Function)
Is invalid configuration data downloaded?	Use the FPGA development software to regenerate the configuration data, download the configuration data, and then turn off and on the power to the module.

When the input/output status display LED does not turn on

When the input/output status display LED does not turn on, check the following items.

Check item	Action
Is the external wiring correct?	Check if the wiring is correct. (☞ Page 54 INSTALLATION AND WIRING)
Is the FPGA RUN LED on?	Refer to the check items in "When the FPGA RUN LED does not turn on" to enable FPGA control. (☞ Page 434 When the FPGA RUN LED does not turn on)
Are there any problems with the standard circuit settings?	Check if the settings match the input/output specifications. (☞ Page 188 Standard Circuit)
For a terminal block to be checked for the input/output status, is the terminal number display LED of the terminal block on?	Operate function setting switch 6 so that the terminal number display LED of the terminal block turns on.
For a terminal to be checked for the input/output state, is the terminal performing pulse input/output?	Depending on the input/output pulse frequency, the LED may not turn on or the LED brightness may decrease, but this does not affect the input/output operation. To check whether pulse input/output is performed normally, use a pulse input/output device or other similar device to check that pulses can be counted normally.

19 UNIT TEST

Run a unit test to check if there is any abnormality in the hardware of the FPGA module.

Operating procedure

1. Download the configuration data in which the sample circuit is configured to the FPGA module.
2. Power off the FPGA module.
3. Connect P1 and P2 of the FPGA module with an Ethernet cable.
4. Set the IP address/station number setting switches and the function setting switches as follows.

- IP address/station number setting switch: other than 255
- Function setting switch 1: ON
- Function setting switch 2: ON

5. Power on the FPGA module.
6. Unit test begins. The RUN LED flashes during the unit test.
7. The RUN LED turns on when the unit test is completed.

- If the test is completed normally, the ERR. LED does not turn on, but remains off.
- If the test is completed with an error, the ERR. LED also turns on. If the test is completed with an error, replace the Ethernet cable and run the test again. If the test is completed with an error again, it may be due to a hardware error in the FPGA module. Please consult your local Mitsubishi representative.

MEMO

20 TROUBLESHOOTING BY SYMPTOM

Troubleshooting by symptom is suitable for the case where the FPGA module fails to operate normally even though no error has occurred in the FPGA module. If an error occurs in the FPGA module, identify the cause of the error using the engineering tool.

When the input from an external device becomes abnormal

When the input from an external device becomes abnormal, check the following items.

Check item	Action
Is the external wiring correct?	Check if the wiring is correct. (☞ Page 54 INSTALLATION AND WIRING) If a differential terminal is not wired, the input/output status display LED is on.
Is a shielded twisted pair cable used for wiring of pulse input?	Use a shielded twisted pair cable for wiring of pulse input.
Are noise countermeasures taken for adjacent devices in the control panel?	Take measures against noise, such as attaching a CR surge suppressor to a magnet switch.
Is the distance between the high voltage equipment and the pulse input line sufficient?	The pulse input line should be a separate pipe, and the wiring inside the panel should be separated from the power line by 150mm or more as a guideline.
Is noise entering from the grounded part?	Disconnect the ground cable of the FPGA module.
Are the power line and input cables not bundled?	Avoid bundling the cables with the power line.
Is there any wiring to unused terminals?	Do not wire to unused terminals.
Are the digital filter settings for the digital input control part and digital input/output control part appropriate?	Adjust the filter time of the digital filter. (☞ Page 202 Digital input/output control part (dio2_top))
Are the oversampling settings of the analog input control part appropriate?	Adjust the oversampling settings. (☞ Page 205 Analog input control part (ai2_top))
Are there any problems with the standard circuit settings?	Check if the settings match the input specifications. (☞ Page 188 Standard Circuit)
Is there a circuit that changes the input state in the user circuit?	Check the design of the user circuit.

Point

If the problem does not improve after checking all of the above and performing input using the sample circuit, the possible cause is a module failure. Please consult your local Mitsubishi representative.

When the output to an external device becomes abnormal

When the output to an external device becomes abnormal, check the following items.

Check item	Action
Is a shielded twisted pair cable used for wiring of pulse output?	Use a shield twisted pair cable for wiring of pulse output.
Are noise countermeasures taken for adjacent devices in the control panel?	Take measures against noise, such as attaching a CR surge suppressor to a magnet switch.
Is the distance between the high voltage equipment and the pulse output line sufficient?	The pulse output line should be a separate pipe, and the wiring inside the panel should be separated from the power line by 150mm or more as a guideline.
Is noise entering from the grounded part?	Disconnect the ground cable of the FPGA module.
Are the power line and output cables not bundled?	Avoid bundling the cables with the power line.
Are there any problems with the standard circuit settings?	Check if the settings match the output specifications. (☞ Page 188 Standard Circuit)
Is the differential output pulse obtained when FPGA control is stopped?	A pulse may be output when FPGA control is stopped, so please ignore it.
Is there a circuit that changes the output state in the user circuit?	Check the design of the user circuit.

Point

If the problem does not improve after checking all of the above and performing output using the sample circuit, the possible cause is a module failure. Please consult your local Mitsubishi representative.

When CC-Link IE TSN/CC-Link IE Field diagnostics cannot be performed

When CC-Link IE TSN/CC-Link IE Field diagnostics cannot be performed with the engineering tool in CC-Link IE TSN communication mode, check the following items.

Check item	Action
Is the DATA LINK LED of the FPGA module on?	Check the DATA LINK LED of the FPGA module, and if it is not on, perform the following troubleshooting. • ☞ Page 435 When the DATA LINK LED turns off • ☞ Page 436 When the DATA LINK LED flashes Also check other LEDs. (☞ Page 430 CC-Link IE TSN/CC-Link IE Field DIAGNOSTICS)
Is the version of the engineering tool supported?	Check the version of the engineering tool, and if it is prior to the supported versions, update it.
Are network parameter settings same as the settings of the CPU module?	Perform "Verify with PLC" and check that network parameter settings match the settings of the CPU module. If they differ, match the settings by performing "Read from PLC" and "Write to PLC", and write the parameters to modules on remote stations.

Point

After checking all of the above, checking the LEDs of the module, checking CC-Link IE TSN/ CC-Link IE Field diagnosis using the engineering tool, or checking error codes, if the online function cannot still be executed with the engineering tool, the possible cause is a module failure. Please consult your local Mitsubishi representative.

When the FPGA download cannot be performed via JTAG

When the FPGA download cannot perform via JTAG, check the following items.

Check item	Action
Is the FPGA module powered off?	Confirm that the FPGA module is powered on.
Is the FPGA download cable connected to a personal computer?	Check if the FPGA download cable is properly connected.
Is the driver of the FPGA download cable installed in a personal computer?	Please check if the driver of the FPGA download cable is properly installed in the personal computer.
Is the download performed in a noisy environment?	Perform the download in a noise-free environment.
Is there an error in the FPGA module?	Identify the cause of the FPGA module error and take corrective action.
Can the configuration data of the sample circuit be downloaded?	If the configuration data of the sample circuit can be downloaded normally, the synthesis environment for the configuration data that failed to download may be incorrect. Please review the settings of the synthesis environment.
Is the communication speed of the FPGA download cable fast?	By setting the communication speed of Programmer in the FPGA development software to 16MHz, the configuration data may be download normally. • Click [Hardware Setup]. • Set the "Hardware frequency" to 16000000.
If the problem does not improve after checking all of the above	By changing the setting of Programmer in the FPGA development software, the configuration data may be download normally. • Select [Tools] → [Options] • Check the "Halt on-chip configuration controller" option from "Programmer" in "Category". If the above procedure fails, the possible cause is a module failure. Please consult your local Mitsubishi representative.

When unable to communicate with the FPGA Module Configuration Tool

When unable to communicate with the FPGA Module Configuration Tool, check the following items.

Check item	Action
Is the FPGA module powered off?	Confirm that the FPGA module is powered on.
Is a Ethernet cable connected to a personal computer?	Check if the Ethernet cable is properly connected.
Is the Ethernet adapter on a personal computer enabled?	Enable the Ethernet adapter on the personal computer.
Is the Ethernet adapter working properly?	• Change the Ethernet adapter used to another one. • If the Ethernet adapter does not work properly, check with the manufacturer of the Ethernet adapter for solutions to problems.
Does the switching hub normally operate?	• Check if the switching hub is powered on. • Check if the switching HUB used supports communication with the FPGA module. (☞ Page 26 Switching hub) • Disconnect Ethernet cables, and then reconnect them. • Power off and on the switching hub.
Is Ethernet communication blocked by the firewall settings of the personal computer?	• Change the antivirus software and Windows firewall settings to allow Ethernet communication. • Allow SLMP and FTP communication ports. (☞ Page 692 Port Number)
Is the network configuration of the FPGA Module Configuration Tool and FPGA module set to line or ring topology?	Use star topology for network configuration.
Is the FPGA module connected to the network?	Check the P1 LINK LED and P2 LINK LED status of the FPGA module and take corrective action.
Does the IP address entered in the "Connection destination setting" window match the IP address of the module?	• Check if the IP address in the "Connection destination setting" window matches the IP address of the FPGA module. • In CC-Link IE TSN communication mode, the IP address of the FPGA module changes before and after the data link with the master station. (☞ Page 54 IP address/station number setting switch setting) • If the IP address set in the FPGA module is lost, initialize the IP address. (☞ Page 57 Initializing IP address in stand-alone mode)
Is the network communication load high?	Reduce the network communication load.
Is the communication load of the FPGA module high?	Check if any external device is not frequently performing Ethernet communication with the FPGA module.
Is there an error in the FPGA module?	Identify the cause of the FPGA module error and take corrective action.

When the FPGA Module Configuration Tool does not start normally

When the FPGA Module Configuration Tool does not start normally, check the following items.

Check item	Action
Does the personal computer runs out of memory?	Exit other applications before starting the FPGA Module Configuration Tool. Also, check whether the required memory has been secured. (📖 FPGA Module Configuration Tool Installation Instructions)

21 TROUBLESHOOTING DURING FPGA DEVELOPMENT

This section shows troubleshooting during FPGA development. Troubleshooting during FPGA development is performed when the FPGA does not operate normally even though normal signals are being input to the FPGA.

When unintended behavior occurs during actual device verification

When unintended behavior occurs during actual device verification, check the following items.

Check item	Action
Has the standard circuit been changed?	Using a difference check tool, check if there are any differences between the RTL downloaded from the Mitsubishi Electric FA site and the RTL for which FPGA logic synthesis is performed.
Is there any problem with FPGA design and verification?	Please review the FPGA design/verification performed by the customer. Confirm that the following precautions are observed. ☞ 4.5.2.2. User circuit, (4) User circuit (I/F specifications) notes/restrictions
Has the FPGA logic synthesis environment been changed?	Check if the configuration file for the logic synthesis environment in Table 3.7-21 has not been changed.
Has the FPGA pin assignment been changed?	Check that the report file (top.pin) after FPGA logic synthesis matches the result of logic synthesis with RTL downloaded from the Mitsubishi Electric FA site.
Does Timing Violation occur in the standard circuit during FPGA logic synthesis?	Please review the points shown below in the RTL (uc2_top.v) modified by the customer. • Circuit scale • Interface of uc2_top.v • Number of flip-flop fan-outs
Does Timing Violation occur in the user circuit during FPGA logic synthesis?	Please review the points shown below in the RTL (uc2_top.v) created by the customer. • Circuit scale • Amount of delay between flip-flops • Timing restriction file
Did a Warning/Error occur during FPGA logic synthesis?	Check the FPGA logic synthesis result.
Are there any problems with the parameter settings for actual device verification?	Check if the same parameters as used in FPGA design/verification are set. If there are no problems with the parameter settings, check the operation of the actual device using the Signal Tap logic analyzer that is included in the FPGA development software. For instructions on how to use the tools that are included in the FPGA development software, please contact the Intel® Corporation.

MEMO

22 TROUBLE EXAMPLES of DC INPUT/OUTPUT

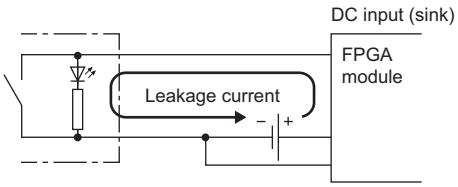
22.1 Troubles and Countermeasures for DC Input Circuits

Examples of troubles in the DC input circuit and countermeasures are shown below.

An input signal does not turn off No.1

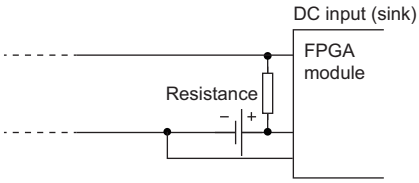
■Cause

Drive by a switch with LED indicator



■Action

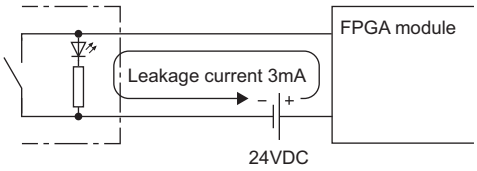
Connect an appropriate resistor as shown below so that a current through the DC input circuit may become lower than the OFF current.



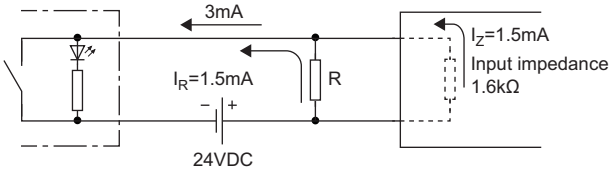
For the calculation example of a resistor to be connected, refer to the following.

■Calculation example

If the switch with LED indicator with maximum leakage current of 3mA when 24VDC external power supply is provided is connected



1. The OFF current through the DC input circuit is not 1.5mA or less. Therefore, connect a resistor as shown below.



2. To satisfy the condition that the OFF current of the DC input circuit is 1.5mA or lower, the current through the connected resistor should be 1.5mA or higher. From the formula below, the connected resistor (R) is lower than 1.6kΩ.

$I_R : I_Z$ = Z (input impedance): R

$$R \leq \frac{I_Z}{I_R} \times Z \text{ (input impedance)} = \frac{1.5}{1.5} \times 1.6 = 1.6 \text{ [k}\Omega\text{]}$$

3. When the resistor (R) is 1.3kΩ, for example, the power capacity (W) of the resistor (R) becomes 0.638W.

$W = (\text{input voltage})^2 \div 28.8^2 \div 1300 = 0.638W$

4. Because the resistor requires a power capacity that is 3 to 5 times larger than the actual current consumption, the resistor connected to the terminal should be 1.3kΩ and 2 to 3W.

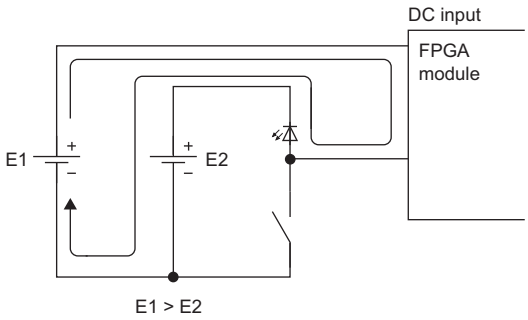
5. The OFF voltage when the resistor (R) is connected becomes 2.15V. This satisfies that the OFF voltage of the DC input circuit is 5V or lower.

$$\frac{1}{\frac{1}{1.3[k\Omega]} + \frac{1}{1.6[k\Omega]}} \times 3[mA] = 2.15[V]$$

An input signal does not turn off No.2

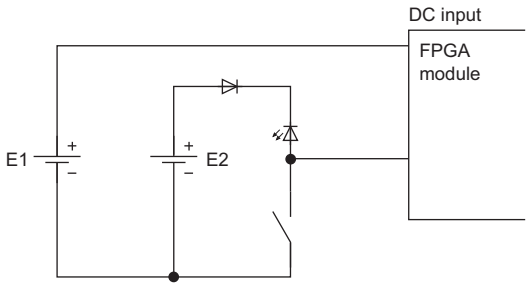
■Cause

By using two power supplies, a sneak path is configured.



■Action

- Use one power supply.
- To prevent the sneak path, connect a diode as shown below.



A signal incorrectly inputs data

■Cause

- Noise is taken as input data.
- The filter settings are incorrect.

■Action

- To prevent excessive noise, avoid installing power cables together with I/O cables. (150mm or more, as a guide)
- Check settings such as filter settings.
- Connect surge absorbers to noise-generating devices such as relays and conductors using the same power supply or take other noise reduction measures.
- To prevent radiation noise, take measures to reduce noise by using a shielded cable.

A count function cannot operate correctly

■Cause

- Noise is taken as input data.
- The filter settings are incorrect.

■Action

- To prevent excessive noise, avoid installing power cables together with I/O cables. (150mm or more, as a guide)
- Check settings such as filter settings.
- Connect surge absorbers to noise-generating devices such as relays and conductors using the same power supply or take other noise reduction measures.

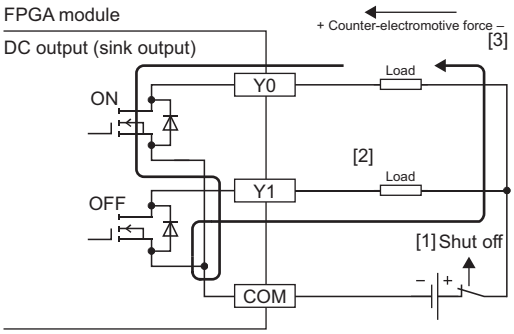
22.2 Troubles and Countermeasures for DC Output Circuits

Examples of troubles in DC output (transistor (sink) output) circuits and countermeasures are shown below.

A load momentarily turns on from off when the system is powered off

■Cause

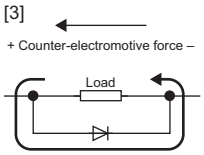
When an inductive load is connected, [2] Load may turn on from off due to a diversion of back electromotive force at [1] Shutoff.



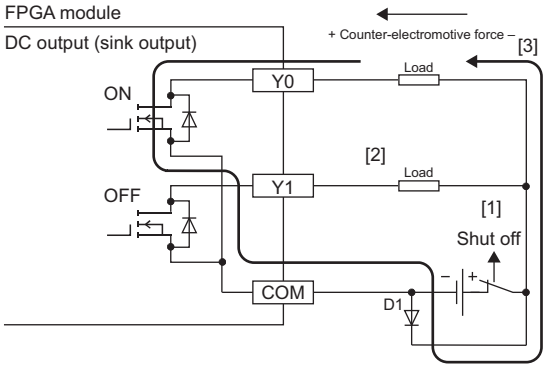
■Action

Take one of the two actions shown below.

Action 1. To suppress the back electromotive force, connect a diode parallel to the load where back electromotive force is generated.



Action 2. Configure a sneak current path by connecting a diode across positive and negative of the external power supply.



D1:
Reverse voltage VR (VRM)
Forward current IF (IFM)

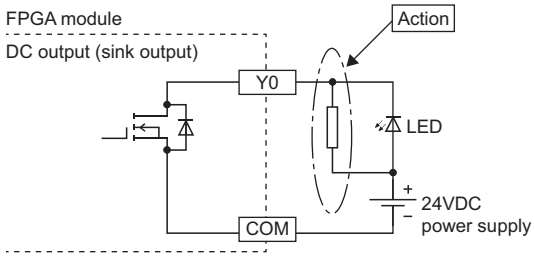
*1 Approximately 10 times the rated voltage in the specifications
Example: 24VDC → Approx. 200VDC

*2 Twice the maximum load current (common) in the performance specifications or more
Example: 0.4A/1 common (0.1A × 4 points) → 0.8A or more

When an output terminal is off, the LED connected as a load dimly turns on

■Cause

The load operates by the leakage current when the output module is off.



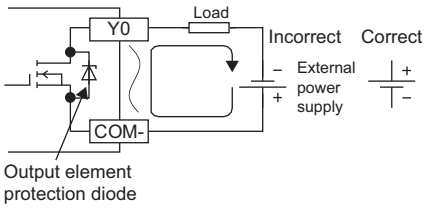
■Action

Connect a resistor of 5 to 50kΩ in parallel with the LED load.

A load operates only by turning on the external power supply

■Cause

- The external power supply is connected with its polarity reversed.



- The reversed polarity may allow current to flow via the output element protection diode into the load.

■Action

Connect the external power supply with the correct polarity.

23 CHECK/CLEAR ERROR CODES

23.1 Checking Error Codes

Error codes can be checked by any of the following methods:

- Checking with the FPGA Module Configuration Tool (☞ Page 121 Module diagnostics)
- Checking by using CC-Link IE TSN/CC-Link IE Field diagnostics (in CC-Link IE TSN communication mode) (☞ Page 450 Checking by using CC-Link IE TSN/CC-Link IE Field diagnostics)
- Checking by Latest error code (RWr0) (☞ Page 117 Batch monitor display)

Checking by using CC-Link IE TSN/CC-Link IE Field diagnostics

In CC-Link IE TSN communication mode, the error history stored inside the FPGA module can be read. Errors that occurred before powering-off can be checked as well.

Point

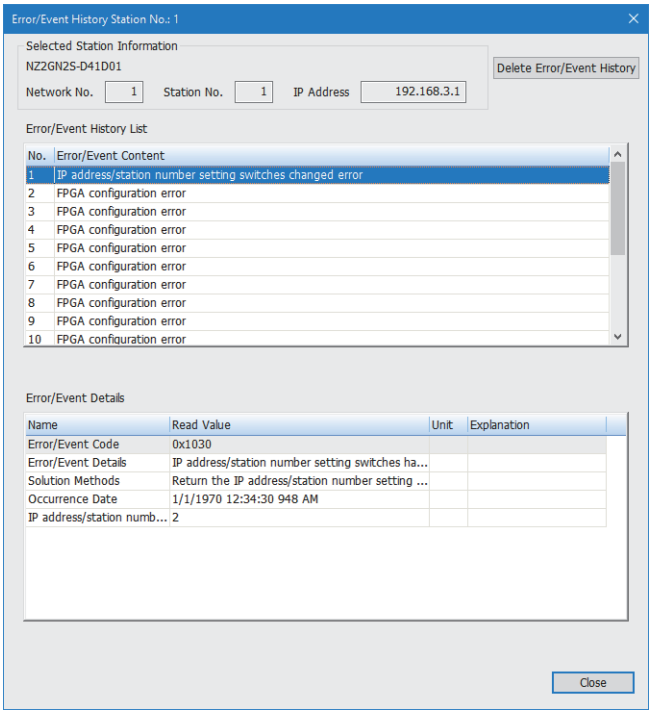
- The error history records a maximum of 16 errors in reverse chronological order of occurrence. If more than 16 errors occur, errors are deleted from the oldest.
- If the same error occurs continuously, only the error that occurred first is stored to the error history.
- The error history is stored in the non-volatile memory in the FPGA module. It is not lost when the power is cut off. However, when the upper limit for the number of writes to the non-volatile memory is reached, the error history cannot be stored in the non-volatile memory.
- "Occurrence Date" information in the error history is recorded after clock information is distributed from the master station. When an error occurs before clock information is distributed from the master station, "Occurrence Date" information is not recorded. If the date and time of occurrence are not recorded, the engineering tool displays "----/--/-- -:--:-- ---".

Operating procedure

1. Connect the engineering tool to the CPU module.
2. Start CC-Link IE TSN/CC-Link IE Field diagnostics from the menu.

[Diagnostics] ⇨ [CC-Link IE TSN/CC-Link IE Field Diagnostic]

3. Right-click the device station whose error history is to be checked, and select "Error/Event History".
4. Follow the on-screen instructions and click the [Yes] button.
5. The error history appears.



Point

To initialize the error history, click the [Delete Error/Event History] button.

23.2 Clearing Error Codes

The clearing method differs depending on the classification of each error.

Classification		How to clear an error
Major		An error cannot be cleared.
Moderate		Whether an error can be cleared depends on what the error is. (☞ Page 450 CHECK/CLEAR ERROR CODES) For an error code that can be cleared, clear the error after correcting the cause of the error.
Minor	Module related	Clear an error after correcting the cause of the error.
	Communication system	

Errors can be cleared by one of the following methods.

- Clearing by input/output signals
- Clearing by Command Execution of Device Station
- Clearing with the FPGA Module Configuration Tool (☞ Page 123 Executing error clear)

Clearing by input/output signals

Turn on Error clear request flag (RYA).

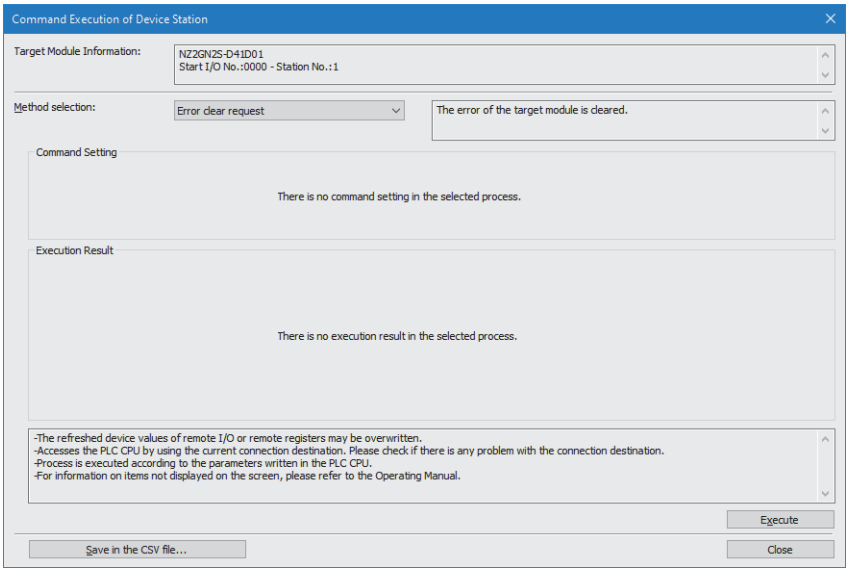
Clearing by Command Execution of Device Station

This section describes how to clear errors by executing a command of the device station.

Operating procedure

1. Select an FPGA module from the station list on the CC-Link IE TSN Configuration window.
2. Open the "Command Execution of Device Station" window.

[CC-Link IE TSN Configuration] ⇨ Right click on the target FPGA module ⇨ [Online] ⇨ [Command Execution of Device Station]



3. Set "Method selection" to "Error clear request", and click the [Execute] button.
4. When a window appears, click the [Yes] button.
5. When a window appears, click the [OK] button.
6. The FPGA module error is cleared.

24 ERROR CODE LIST

The error codes are classified into the following three types.

Classification		Description
Major error		An error that cannot be recovered. The RUN LED turns off.
Moderate error		An error where the module can continue to operate but FPGA control cannot continue. The ERR. LED turns on.
Minor error	Module-specific	An error where the module and FPGA control can continue to operate. The ERR. LED flashes.
	Communication system	An error that is related to the communication part. The DATA LINK LED flashes or turns off.

☐: Indicates the CH number where the error occurred.

△: Indicates the circuit board number where the error occurred.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
1020H*1	Minor	Remote buffer memory access error	A buffer memory area other than the remote buffer memory areas has been accessed using the REMFR/REMTO instruction.	Correct the setting data of the REMFR/REMTO instruction to access the remote buffer memory.
1030H*1	Minor	IP address/station number setting switch changed error	An IP address/station number setting switch has been changed with the module power supply on.	Return the IP address/station number setting switch to the setting it had when the module was powered on.
1041H*1	Minor	Function setting switch 1 changed error	The function setting switch 1 has been changed with the module power supply on.	Return the function setting switch 1 to the setting when the module power supply was on.
1042H*1	Minor	Function setting switch 2 changed error	The function setting switch 2 has been changed with the module power supply on.	Return the function setting switch 2 to the setting when the module power supply was on.
1043H*1	Minor	Function setting switch 3 changed error	The function setting switch 3 has been changed with the module power supply on.	Return the function setting switch 3 to the setting when the module power supply was on.
1050H*1	Minor	Error history save limit error	The upper limit for the number of times an error is saved in the error history is reached.	No more errors can be saved in the error history. Check the error by the latest error code.
1051H*1	Minor	IP address save limit error	The upper limit for the number of times the IP address is saved is reached.	IP address changes made after this error occurs will not be saved in the non-volatile memory.
1052H*1	Minor	Parameter save limit error	The upper limit for the number of times a parameter is saved is reached.	Parameter changes made after this error occurs will not be saved in the non-volatile memory.
1060H*1	Minor	Non-volatile memory access error (error history)	The error cannot be saved because an error in access to the non-volatile memory was detected.	• An error that occurred at the time of or before this error may not be saved into the non-volatile memory. • Take measures against noise with a shielded cable for connection. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
1061H*1	Minor	Non-volatile memory access error (IP address)	The IP address cannot be saved because an error in access to the non-volatile memory was detected.	• The IP address is not saved into the non-volatile memory. • Take measures against noise with a shielded cable for connection. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
1062H*1	Minor	Non-volatile memory access error (parameter)	The parameters cannot be saved because an error in access to the non-volatile memory was detected.	• The parameters are not saved in the non-volatile memory. • Take measures against noise with a shielded cable for connection. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
1063H[*1]	Minor	Competing access to non-volatile memory (parameter)	Parameter saving has been executed by turning on Parameter save request (RY2) while the parameter write (memory + non-volatile memory) or the parameter read (non-volatile memory) was being executed by the FPGA Module Configuration Tool.	• If this error has occurred, the parameter value that was attempted to be saved by Parameter save request (RY2) is not saved in the non-volatile memory. • After the parameter has been written or read by the FPGA Module Configuration Tool, execute the parameter saving again.
1080H[*1]	Minor	Module power supply voltage drop error	The module power supply voltage is dropped.	• Check the state of the module power supply. • Check if the power supply voltage satisfies the specifications for the FPGA module.
1081H[*1]	Minor	Module power supply voltage drop error	The module power supply voltage is dropped.	• Check the state of the module power supply. • Check if the power supply voltage satisfies the specifications for the FPGA module.
1090H[*1]	Minor	Remote reset disable error	Remote reset was not able to be performed because a setting of function setting switch 1, 2, or 3 is different from the setting it had when the module power supply was turned on.	Return the corresponding function setting switch to the setting it had when the power was turned on, and then perform remote reset again.
1100H[*1]	Minor	Write start address out-of-range error	The write request to the FPGA register was issued while an invalid value was set in Write start address (remote buffer memory address: 1200H, 1201H). • An odd-numbered address is set. • An address where the data write is prohibited is set.	• Set an even-numbered address. • Set an FPGA register address where the data write is allowed.
1101H[*1]	Minor	FPGA register write size out-of-range error	The write request to the FPGA register was issued while an invalid value was set in Write size (remote buffer memory address: 1202H). • A value other than 1 to 384 is set for Write size. • The write range includes the FPGA register areas where data write is prohibited.	• Set a value within 1 to 384 for Write size (remote buffer memory address: 1202H). • Correct Write size so that the write range does not include the FPGA register areas where data write is prohibited.
1102H[*1]	Minor	Read start address out-of-range error	The read request from the FPGA register was issued while an invalid value was set in Read start address (remote buffer memory address: 1400H, 1401H). • An odd-numbered address is set. • An address where the data read is prohibited is set.	• Set an even-numbered address. • Set an FPGA register address where the data read is allowed.
1103H[*1]	Minor	FPGA register read size out-of-range error	The read request from the FPGA register was issued while an invalid value was set for Read size (remote buffer memory address: 1402H). • A value other than 1 to 384 is set for Read size. • The read range includes the FPGA register areas where data read is prohibited.	• Set a value within 1 to 384 for Read size (remote buffer memory address: 1402H). • Correct Read size so that the read range does not include the FPGA register areas where data read is prohibited.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
1210H[*1]	Minor	Time setting error	The time setting request was issued while a value set for Time information is in any of the following states. • Time information (month) (remote buffer memory address: 1602H bits 10 to 13) is a value other than 1 to 12 • Time information (day) (remote buffer memory address: 1602H bits 5 to 9) is a value other than 1 to 31 • Time information (hour) (remote buffer memory address: 1602H bits 0 to 4) is a value other than 0 to 23 • Time information (minute) (remote buffer memory address: 1603H bits 8 to 13) is a value other than 0 to 59 • Time information (second) (remote buffer memory address: 1603H bits 0 to 5) is a value other than 0 to 59 • Time information (month, day) is a date that do not exist in the calendar, such as April 31st.	Set values that satisfy all of the following and execute the time setting again. • Time information (month) (remote buffer memory address: 1602H bits 10 to 13): 1 to 12 • Time information (day) (remote buffer memory address: 1602H bits 5 to 9): 1 to 31 • Time information (hour) (remote buffer memory address: 1602H bits 0 to 4): 0 to 23 • Time information (minute) (remote buffer memory address: 1603H bits 8 to 13): 0 to 59 • Time information (second) (remote buffer memory address: 1603H bits 0 to 5): 0 to 59 • Time information (month, day): a date that exists in the calendar
1300H[*1]	Minor	Logging timing pulse error	In the FPGA internal circuit, a sampling pulse for logging data was input from the user circuit to the logging part of standard circuits in a cycle of less than 1μs.	• Logging data may not be sampled. • Check the sampling pulse output specifications of the user circuit of the FPGA internal circuit. Input the sampling pulse to the logging part of standard circuits in a cycle of 1μs or longer.
1400H[*1]	Minor	FTP communication error	The connection became disconnected during communications with the FTP server.	• Check whether the PORT mode can be used as the FTP server connection method. • The Ethernet line may be congested. Wait for a while and perform the operation again. • Check the connection with the FTP server (such as looseness or disconnection of the Ethernet cable).
1401H[*1]	Minor	FTP open error	Connection to the FTP server failed.	• Check the IP address and subnet mask of the FPGA module. • Check the setting of the FTP server IP address in the FPGA module. • Check the settings of the FTP server (such as IP address and subnet mask). • Check whether the data port number of the FTP server is set to 20 and the control port number of the FTP server is set to 21. • Check the firewall settings of the FTP server. • Check the connection with the FTP server (such as looseness or disconnection of the Ethernet cable). • Check whether the data communications with the FTP server or the FPGA module are possible by using the Ping command. • Data communications may not be ready. Wait for a while and perform the operation again.
1402H[*1]	Minor	FTP login error	Login to the FTP server failed.	• Check the FTP client settings of the FPGA module (login name, password). • Check the login settings of the FTP server (login name, password). • Check the connection with the FTP server (such as looseness or disconnection of the Ethernet cable).

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
1403H[*1]	Minor	FTP file generation error	File generation in the FTP server failed.	• The specified file may be used in another process in the FTP server. Wait for a while and perform the operation again. • Check the folder path of the FTP server. • Check that the user has a right to access (read/write) the FTP server or the specified file. • Check that the specified folder path exists in the FTP server. • Delete unnecessary files on the FTP server to increase free space. • The Ethernet line may be congested. Wait for a while and perform the operation again. • Check the connection with the FTP server (such as looseness or disconnection of the Ethernet cable).
1410H[*1]	Minor	CSV file generation error	CSV file generation failed.	• Check whether the standard circuit was changed during FPGA internal circuit development. • Check whether a warning occurred in process of logic synthesis. If this error occurs again after the measures above are taken, the possible cause is a module failure. Please consult your local Mitsubishi representative.
1420H[*1]	Minor	Logging start request error	Logging start request (RY3) was turned on in the situation where logging data collection or logging data transfer cannot be performed.	■To start logging data collection Turn on Logging start request (RY3) when Logging operation state monitor (RWrB) is 1H: Collection start waiting. ■To start logging data transfer Turn on Logging start request (RY3) when Logging operation state monitor (RWrB) is 5H: FTP transfer start waiting.
1430H[*1]	Minor	Logging control start violation error	A logging start request from the user circuit was detected in the situation where logging cannot be started.	Correct FPGA internal circuit (user circuit), and start logging (change Logging enable (uc_logen_clk100m_reg) from Low to High) when Logging control trigger (lgdw_ctrl[3]) is "1b: Rising for logging start allowed".
1431H[*1]	Minor	Logging control stop violation error	A logging stop request from the user circuit was detected in the situation where logging cannot be stopped.	Correct FPGA internal circuit (user circuit), and stop logging (change Logging enable (uc_logen_clk100m_reg) from High to Low) when Logging control trigger (lgdw_ctrl[3]) is "0b: Falling for logging start allowed".
2010H[*2]	Moderate	Non-volatile memory data error (parameter)	The parameter data stored in the non-volatile memory are abnormal.	• To set the parameters of the non-volatile memory back to their default, change Parameter area initialization command (address: 1000H) to the following: Not commanded (0), Commanded (1), Not commanded (0), and turn off and on the module power supply. After that, set the parameters again. • Take measures against noise with a shielded cable for connection. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
2011H[*1]	Moderate	Non-volatile memory data error (IP address)	The IP address and subnet mask stored in the non-volatile memory are abnormal.	• The module will be automatically recovered immediately after the error occurs. However, the stored IP address and subnet mask are lost, and operation is performed assuming that the following are stored. IP Address: 192.168.3.250 Subnet mask: 255.255.255.0 • Take measures against noise with a shielded cable for connection. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
2210H[*2]	Moderate	Synchronous communication error 1	When CC-Link IE TSN Network synchronous communication function is used, time synchronization is abnormal.	• Check that the system configuration meets the specifications by referring to the manual for the master station. • Check that no communication error has occurred on the other stations. • Check that no remote reset has been performed to the other stations. • Take measures against noise on the transmission path. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
2220H[*2]	Moderate	Synchronous communication error 2	When CC-Link IE TSN Network synchronous communication function is used, synchronous communication with the master station has failed for a certain period of time.	• Set a longer time for the synchronization cycle of the master station. • Reduce the number of remote stations that operate with the CC-Link IE TSN Network synchronous communication function. • Take measures against noise on the transmission path. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
2400H[*2]	Moderate	IP address/station number setting switches out of range error (IP address)	The IP address/station number setting switches are set to 255.	Turn on the power supply with the IP address/station number setting switches set to a value in the range 0 to 254.
301△H[*1]	Moderate	Filter sampling pulse (B△) setting error	Set Filter sampling pulse (B△) (FPGA register address: 1000_2000H to 1000_2004H) is invalid. ■For DC input A value other than Data sampling timing (FH) is set for Filter sampling pulse (B△). ■For differential input • Data sampling timing (FH) is set for Filter sampling pulse (B△). • A value set for Filter sampling pulse (B△) is different from a value set for Data sampling timing (B△).	■For DC input Set Filter sampling pulse (B△) (FPGA register address: 1000_2000H to 1000_2004H) to Data sampling timing (FH). ■For differential input • Set Filter sampling pulse (B△) (FPGA register address: 1000_2000H to 1000_2004H) to a value within 0.01μs (0H) to 100.00μs (EH). • Set the same value for both Filter sampling pulse (B△) and Data sampling timing (B△).

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
302△H[*1]	Moderate	Filter sampling pulse (E△) setting error	The value of Filter sampling pulse (E△)(FPGA register address: 1000_2008H to 1000_200CH) is invalid. ■For DC input A value other than Data sampling timing (FH) is set for Filter sampling pulse (E△). ■For differential input • Data sampling timing (FH) is set for Filter sampling pulse (E△). • A value set for Filter sampling pulse (E△) is different from a value set for Data sampling timing (E△).	■For DC input • Set Filter sampling pulse (E△) (FPGA register address: 1000_2008H to 1000_200CH) to Data sampling timing (FH). • Set Filter sampling pulse (E△) (FPGA register address: 1000_2008H to 1000_200CH) to Data sampling timing (FH). ■For differential input • Set Filter sampling pulse (E△) (FPGA register address: 1000_2008H to 1000_200CH) to a value within 0.01μs (0H) to 100.00μs (EH). • Set the same value for both Filter sampling pulse (E△) and Data sampling timing (E△).
303△H[*1]	Moderate	Data sampling timing (B△) setting error	For the DC input terminal, a value other than 0.1μs (9H) to 655.36μs (FFFFH) is set for Data sampling timing (B△) (FPGA register address: 1000_2100H to 1000_2104H).	Set Data sampling timing (B△) (FPGA register address: 1000_2100H to 1000_2104H) to a value within 0.1μs (9H) to 655.36μs (FFFFH).
304△H[*1]	Moderate	Data sampling timing (E△) setting error	Data sampling timing (E△) (FPGA register address: 1000_2108H to 1000_210CH) is invalid. ■For DC input A value other than 0.1μs (9H) to 655.36μs (FFFFH) is set for Data sampling timing (E△). ■For analog input • A value other than 4μs (18FH) to 655.36μs (FFFFH) is set for Data sampling timing (E△). • The time required for A/D conversion value averaging by oversampling exceeds the cycle of Data sampling timing (E△).	■For DC input Set Data sampling timing (E△) (FPGA register address: 1000_2108H to 1000_210CH) to a value within 0.1μs (9H) to 655.36μs (FFFFH). ■For analog input • Set Data sampling timing (E△) (FPGA register address: 1000_2108H to 1000_210CH) to a value within 4μs (18FH) to 655.36μs (FFFFH). • Set ADC oversampling ratio setting and Data sampling timing to values within the setting ranges. ADC oversampling ratio setting: Data sampling timing • 2 times: 6μs (257H) or longer • 4 times: 8μs (31FH) or longer • 8 times: 13μs (513H) or longer • 16 times: 24μs (95FH) or longer • 32 times: 44μs (112FH) or longer • 64 times: 84μs (20CFH) or longer • 128 times: 165μs (4073H) or longer • 256 times: 328μs (801FH) or longer
305△H[*1]	Moderate	Data update timing (B△) setting error	For the DC output terminal, a value other than 0.1μs (9H) to 655.36μs (FFFFH) is set for Data update timing (B△) (FPGA register address: 1000_2110H to 1000_2114H).	Set Data update timing (B△) (FPGA register address: 1000_2110H to 1000_2114H) to a value within 0.1μs (9H) to 655.36μs (FFFFH).
306△H[*1]	Moderate	Data update timing (E△) setting error	A value set in Data update timing (E△) (FPGA register address: 1000_2118H to 1000_211CH) is out of range. ■For DC output A value other than 0.1μs (9H) to 655.36μs (FFFFH) is set for Data update timing (E△). ■For analog output A value other than 6μs (257H) to 655.36μs (FFFFH) is set for Data update timing (E△).	■For DC output Set Data update timing (E△) (FPGA register address: 1000_2118H to 1000_211CH) to a value within 0.1μs (9H) to 655.36μs (FFFFH). ■For analog output Set Data update timing (E△) (FPGA register address: 1000_2118H to 1000_211CH) to a value within 6μs (257H) to 655.36μs (FFFFH).
310△H[*1]	Moderate	Output signal/Input output direction signal selection (B△) setting error	A value other than Register setting value (0H) and User circuit output (3H) is set for Output signal/Input output direction signal selection (B△) (address: 1000_5020H to 1000_5024H).	Set Output signal/Input output direction signal selection (B△) (address: 1000_5020H to 1000_5024H) to Register setting value (0H) or User circuit output (3H).

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
311△H[*1]	Moderate	Output signal/Input output direction signal selection (E△) setting error	A value other than Register setting value (0H) and User circuit output (3H) is set for Output signal/Input output direction signal selection (E△) (address: 1000_5028H to 1000_502CH).	Set Output signal/Input/output direction signal selection (E△) (address: 1000_5028H to 1000_502CH) to Register setting value (0H) or User circuit output (3H).
32△□H[*1]	Moderate	ADC range setting CH□ (E△) setting error	A value other than -19.8 to 19.8mA (0H) and -9.9 to 9.9V (2H) is set for CH□ of ADC range setting CH0-B (E△)(FPGA register address: 1000_6100H to 1000_6110H).	Set CH□ of ADC range setting CH0-B (E△)(FPGA register address: 1000_6100H to 1000_6110H) to a value within -19.8 to 19.8mA (0H) or -9.9 to 9.9V (2H).
33△□H[*1]	Moderate	DAC range setting CH□ (E△) setting error	A value other than -9.9 to 9.9V (3H) and 0.2 to 19.8mA (4H) is set for DAC range setting CH□ (E△) (remote buffer memory address: 0602H, 0606H, 060AH, 060EH, 0612H, 0616H).	Set DAC range setting CH□ (E△) (remote buffer memory address: 0602H, 0606H, 060AH, 060EH, 0612H, 0616H) to a value within -9.9 to 9.9V (3H) or 0.2 to 19.8mA (4H).
34△0H[*1]	Moderate	D/A conversion signal selection (E△) setting error	Only for some of the following FPGA register areas, the user circuit is selected as a signal used for D/A conversion. • D/A conversion value selection (FPGA register address: 1000_7002H) • D/A conversion timing selection (FPGA register address: 1000_7004H) • DAC LDAC signal selection (FPGA register address: 1000_7006H)	When performing D/A conversion with the output of the user circuit, set the E△ setting of the following FPGA register areas and set User circuit output to Select (1). Alternatively, reset 0b if D/A conversion is not performed on the output of the user circuit. • D/A conversion value selection (FPGA register address: 1000_7002H) • D/A conversion timing selection (FPGA register address: 1000_7004H) • DAC LDAC signal selection (FPGA register address: 1000_7006H)
3500H[*1]	Moderate	Logging data size setting error	A value other than 256 records (0H) to 524288 records (BH) is set for Logging data size setting (FPGA register address: 1000_9008H).	Set Logging data size setting (FPGA register address: 1000_9008H) to a value within 256 records (0H) to 524288 records (BH).
3501H[*1]	Moderate	Number of sampling times after trigger setting error	The setting value of Number of sampling times after trigger setting (FPGA register address: 1001_9000H, 1001_9002H) is invalid. • 0 is set. • A value equal to or greater than the number of records set in Logging data size setting (FPGA register address: 1000_9008H) is set.	Set Number of sampling times after trigger setting (FPGA register address: 1001_9000H, 1001_9002H) to a value within 1 to (number of records - 1).
3A00H[*2]	Moderate	Module configuration error	The type of an extension module mounted (including the case where no extension module is mounted) is different from the extension module type when the parameter was saved.	• After setting the parameter again, execute "Parameter write (Memory + Non-volatile memory)" from the FPGA Module Configuration Tool. Alternatively, turn on and off Parameter save request (RY2), and then save the parameter to non-volatile memory. Then, turn off and on the module power supply. • When the type of extension module mounted is the same as the type when the parameter was saved, the possible cause is noise effects. Take measures to reduce noise. • If this error occurs again after the measures above are taken, the possible cause is a module failure. Please consult your local Mitsubishi representative.
3A10H[*2]	Moderate	Incompatible FPGA version error	The firmware version is not compatible with FPGA configuration data.	Update the firmware to the version compatible with FPGA version.
3A20H[*2]	Moderate	Configuration ROM access error	An error was detected during access to the configuration ROM, and the operation was completed with an error.	• Turn off and on the module power supply, and perform an FPGA download again. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
3C00H	Major	Hardware error	Module hardware error	• Power off and on the module power supply. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
3C01H*2	Major	FPGA configuration error	■During FPGA configuration FPGA configuration was not completed properly because of the following reasons. • Invalid configuration data is written to the configuration ROM. • Data in the configuration ROM is deleted. • During configuration data transfer, an error occurred due to noise. • Configuration data was written via JTAG while the function setting switch 5 was off. ■After FPGA configuration is complete An error was detected by FPGA configuration state monitor.	• Power off and on the module power supply. • Write configuration data to the configuration ROM again, and then turn off and on the module power supply. • Take measures to reduce noise, such as the use of shielded cables for external input/output signal connections. • Be sure that the function setting switch 5 is on while configuration data is being written via JTAG. • If this error occurs again after the measures above are taken, the possible cause is a module failure. Please consult your local Mitsubishi representative.
3C02H*2	Major	Extension module mounting state error	An extension module is not properly mounted.	• Turn off the module power supply, and check the mounting state of the extension module. Then, turn on the module power supply. • When the extension module is properly mounted, the possible cause is noise effects. Take measures to reduce noise. • If this error occurs again after the measures above are taken, the possible cause is a module failure. Please consult your local Mitsubishi representative.
3C03H	Major	Hardware error	Module hardware error	• Check whether the standard circuit was changed during FPGA internal circuit development. • Power off and on the module power supply. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.

*1 The error can be cleared by turning on and off Error clear request flag (RYA).

*2 The error cannot be cleared by turning on and off Error clear request flag (RYA). After eliminating the cause of the error, turn off and on the power supply or perform a remote reset.

Communication system error codes

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
D000H[*1*2]	Minor	Communication setting error 1	Invalid network settings are received.	• Power off and on the module power supply. • If this error occurs again, the possible cause is a module failure. Please consult your local Mitsubishi representative.
D001H[*1*2]	Minor	Communication setting error 2	Network settings that cannot be handled by the FPGA module are received.	• Check that the model name of the remote station set in the network configuration settings matches the model name of the actual device. • If this error occurs even when the model names match, perform a firmware update so that the firmware of the FPGA module becomes the latest. • If this error occurs even with the latest firmware, the possible cause is a module failure. Please consult your local Mitsubishi representative.
D010H[*1]	Minor	IP address duplication detection	An IP address duplication is detected.	Change the IP address so that no IP address duplication occurs in the access range of CC-Link IE TSN. After change, power off and on the module power supply.
D011H[*1*2]	Minor	IP address setting error	Values the FPGA module cannot use were set for the IP address and subnet mask settings.	• Without using the set IP address and subnet mask, the module is operated based on the previous IP address and subnet mask. • The set IP address and subnet mask will not be saved in non-volatile memory. • Check the IP address and subnet mask again, and change the settings to values the FPGA module can use. After change, power off and on the module power supply.
D020H[*1*2]	Minor	Network synchronous communication setting error	"Network Synchronous Communication" of the FPGA module is set to "Synchronous".	In the network configuration settings, set "Network Synchronous Communication" of the FPGA module to "Asynchronous".
D021H[*1*2]	Minor	Number of RX/RY points error	RX/RY with a number of points that cannot be handled by the FPGA module are set.	Set 112 or less for the number of points for RX and RY in the network configuration setting.
D022H[*1*2]	Minor	RWr/RWw number of points error	RWr/RWw with a number of points that cannot be handled by the FPGA module are set.	Set 144 or less for the number of points for RWr and RWw in the network configuration setting.
D023H[*1*2]	Minor	Communication cycle setting error (CC-Link IE TSN Class B/1Gbps)	When the FPGA module was operating at a communication speed of 1Gbps, a communication cycle the FPGA module could not support was set.	Correct the communication cycle setting so that the FPGA module can operate with the set communication cycle.
D024H[*1*2]	Minor	Communication cycle setting error (CC-Link IE TSN Class B/100Mbps)	When the FPGA module was operating at a communication speed of 100Mbps, a communication cycle the FPGA module could not support was set.	Correct the communication cycle setting so that the FPGA module can operate with the set communication cycle.
D025H[*1*2]	Minor	RWw/RWr setting error	In synchronous communication mode, the system area (RWwF/RWrF) is not assigned for the RWw/RWr settings in the network configuration setting.	In the RWw/RWr settings of the network configuration setting, assign the system area (RWwF/RWrF).
D026H[*1*2]	Minor	Synchronization cycle setting error	The synchronization cycle set in the master station is not supported by the module.	Adjust the synchronization cycle of the master station and then turn off and on the module power supply, or perform remote reset.
D027H[*1*2]	Minor	Network synchronous communication setting change disable error	After the module power supply is turned on, the network synchronous communication setting in the network configuration settings has been changed.	In the network configuration setting, return the network synchronous communication setting to the setting of when the module power supply was on.

Error code (hexadecimal)	Classification	Error name	Description and cause	Action
D028H[*1*2]	Minor	Communication cycle setting error (CC-Link IE TSN Class A)	The communication cycle that cannot be handled by the FPGA module is set while the FPGA module is operating with CC-Link IE TSN Class A.	Correct the communication cycle setting so that the FPGA module can operate with the set communication cycle.

*1 This error occurs only once when an abnormality is detected. Before clearing the error, eliminate the cause of the error and check that a data link is established.

*2 When this error occurs, errors other than this error may not occur. If this error occurs, eliminate the cause of one error after another until a data link is established.

APPENDICES

Appendix 1 Remote I/O Signal

Remote input (RX) is a signal that indicates the state of the FPGA module (such as control state and external input state). In the CC-Link IE TSN communication mode, it is an input signal from the FPGA module to the master module. In addition, regardless of the operation mode setting, it can be referenced by an external device via SLMP communication.
Remote output (RY) is a signal that gives various commands (such as control start/stop and external output) to the FPGA module. In CC-Link IE TSN communication mode, output from the master module to the FPGA module. In standalone mode, ON/OFF operation can be performed from an external device via SLMP communication.

Remote input signal (RX)	Remote output signal (RY)	Description
RX0 to RXF	RY0 to RYF	Common remote I/O signals for FPGA module models
RX10 to RX3F	RY10 to RY3F	Remote I/O signal specific to FPGA module model (external input/external output)
RX40 to RX6F*1	RY40 to RY6F*1	

*1 This area is an I/O signal allocated when an extension module is installed.

List of remote I/O signals

The table below lists the assignments for the remote I/O signals of the FPGA module.

Point

Do not use any "Use prohibited" remote I/O signals. Doing so may result in an accident due to an incorrect output or malfunction.

Common

Remote input signals	Name	Remote output signals	Name
Device number		Device number	
RX0	FPGA controlling flag	RY0	FPGA control start request
RX1	Use prohibited	RY1	FPGA control stop request
RX2	Parameter saving completion flag	RY2	Parameter save request
RX3	Logging start flag	RY3	Logging start request
RX4	FTP transfer completion flag	RY4	FTP resend allowed
RX5	FTP transfer error completion flag	RY5	Use prohibited
RX6	FPGA control stop while data collection flag	RY6	
RX7	Logging control suspension flag	RY7	Logging control suspend request
RX8	Use prohibited	RY8	Use prohibited
RX9		RY9	
RXA	Error flag	RYA	Error clear request flag
RXB	Remote READY	RYB	Use prohibited
RXC	Use prohibited	RYC	
RXD		RYD	
RXE		RYE	
RXF		RYF	

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Remote input signals Device number	Name	Remote output signals Device number	Name
RX10	External input signal X0(B0)	RY10	External output signal Y0(B0)
RX11	External input signal X1(B0)	RY11	External output signal Y1(B0)
RX12	External input signal X2(B0)	RY12	External output signal Y2(B0)
RX13	External input signal X3(B0)	RY13	External output signal Y3(B0)
RX14	External input signal X4(B0)	RY14	External output signal Y4(B0)
RX15	External input signal X5(B0)	RY15	External output signal Y5(B0)
RX16	External input signal X6(B0)	RY16	External output signal Y6(B0)
RX17	External input signal X7(B0)	RY17	External output signal Y7(B0)
RX18	External input signal X8(B0)	RY18	External output signal Y8(B0)
RX19	External input signal X9(B0)	RY19	External output signal Y9(B0)
RX1A	External input signal XA(B0)	RY1A	External output signal YA(B0)
RX1B	External input signal XB(B0)	RY1B	External output signal YB(B0)
RX1C	External input signal XC(B0)	RY1C	External output signal YC(B0)
RX1D	External input signal XD(B0)	RY1D	External output signal YD(B0)
RX1E	External input signal XE(B0)	RY1E	External output signal YE(B0)
RX1F	External input signal XF(B0)	RY1F	External output signal YF(B0)
RX20	External input signal X0(B1)	RY20	External output signal Y0(B1)
RX21	External input signal X1(B1)	RY21	External output signal Y1(B1)
RX22	External input signal X2(B1)	RY22	External output signal Y2(B1)
RX23	External input signal X3(B1)	RY23	External output signal Y3(B1)
RX24	External input signal X4(B1)	RY24	External output signal Y4(B1)
RX25	External input signal X5(B1)	RY25	External output signal Y5(B1)
RX26	External input signal X6(B1)	RY26	External output signal Y6(B1)
RX27	External input signal X7(B1)	RY27	External output signal Y7(B1)
RX28	External input signal X8(B1)	RY28	External output signal Y8(B1)
RX29	External input signal X9(B1)	RY29	External output signal Y9(B1)
RX2A	External input signal XA(B1)	RY2A	External output signal YA(B1)
RX2B	External input signal XB(B1)	RY2B	External output signal YB(B1)
RX2C	External input signal XC(B1)	RY2C	External output signal YC(B1)
RX2D	External input signal XD(B1)	RY2D	External output signal YD(B1)
RX2E	External input signal XE(B1)	RY2E	External output signal YE(B1)
RX2F	External input signal XF(B1)	RY2F	External output signal YF(B1)
RX30	External input signal X0(B2)	RY30	External output signal Y0(B2)
RX31	External input signal X1(B2)	RY31	External output signal Y1(B2)
RX32	External input signal X2(B2)	RY32	External output signal Y2(B2)
RX33	External input signal X3(B2)	RY33	External output signal Y3(B2)
RX34	External input signal X4(B2)	RY34	External output signal Y4(B2)
RX35	External input signal X5(B2)	RY35	External output signal Y5(B2)
RX36	External input signal X6(B2)	RY36	External output signal Y6(B2)
RX37	External input signal X7(B2)	RY37	External output signal Y7(B2)
RX38	External input signal X8(B2)	RY38	External output signal Y8(B2)
RX39	External input signal X9(B2)	RY39	External output signal Y9(B2)
RX3A	External input signal XA(B2)	RY3A	External output signal YA(B2)
RX3B	External input signal XB(B2)	RY3B	External output signal YB(B2)
RX3C	External input signal XC(B2)	RY3C	External output signal YC(B2)
RX3D	External input signal XD(B2)	RY3D	External output signal YD(B2)
RX3E	External input signal XE(B2)	RY3E	External output signal YE(B2)
RX3F	External input signal XF(B2)	RY3F	External output signal YF(B2)

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Remote input signals Device number	Name	Remote output signals Device number	Name
RX10	External input signal X0(B0)	RY10	External output signal Y0(B0)
RX11	External input signal X1(B0)	RY11	External output signal Y1(B0)
RX12	External input signal X2(B0)	RY12	External output signal Y2(B0)
RX13	External input signal X3(B0)	RY13	External output signal Y3(B0)
RX14	External input signal X4(B0)	RY14	External output signal Y4(B0)
RX15	External input signal X5(B0)	RY15	External output signal Y5(B0)
RX16	External input signal X6(B0)	RY16	External output signal Y6(B0)
RX17	External input signal X7(B0)	RY17	External output signal Y7(B0)
RX18	External input signal XY(B0) (when input is selected)	RY18	External output signal XY(B0) (when output is selected)
RX19 to RX1F	Use prohibited	RY19 to RY1F	Use prohibited
RX20	External input signal X0(B1)	RY20	External output signal Y0(B1)
RX21	External input signal X1(B1)	RY21	External output signal Y1(B1)
RX22	External input signal X2(B1)	RY22	External output signal Y2(B1)
RX23	External input signal X3(B1)	RY23	External output signal Y3(B1)
RX24	External input signal X4(B1)	RY24	External output signal Y4(B1)
RX25	External input signal X5(B1)	RY25	External output signal Y5(B1)
RX26	External input signal X6(B1)	RY26	External output signal Y6(B1)
RX27	External input signal X7(B1)	RY27	External output signal Y7(B1)
RX28	External input signal XY(B1) (when input is selected)	RY28	External output signal XY(B1) (when output is selected)
RX29 to RX2F	Use prohibited	RY29 to RY2F	Use prohibited
RX30	External input signal X0(B2)	RY30	External output signal Y0(B2)
RX31	External input signal X1(B2)	RY31	External output signal Y1(B2)
RX32	External input signal X2(B2)	RY32	External output signal Y2(B2)
RX33	External input signal X3(B2)	RY33	External output signal Y3(B2)
RX34	External input signal X4(B2)	RY34	External output signal Y4(B2)
RX35	External input signal X5(B2)	RY35	External output signal Y5(B2)
RX36	External input signal X6(B2)	RY36	External output signal Y6(B2)
RX37	External input signal X7(B2)	RY37	External output signal Y7(B2)
RX38	External input signal XY(B2) (when input is selected)	RY38	External output signal XY(B2) (when output is selected)
RX39 to RX3F	Use prohibited	RY39 to RY3F	Use prohibited

NZ2GN2S-D41PD02

Remote input signals	Name	Remote output signals	Name
Device number		Device number	
RX10	External input signal X0(B0)	RY10	External output signal Y0(B0)
RX11	External input signal X1(B0)	RY11	External output signal Y1(B0)
RX12	External input signal X2(B0)	RY12	External output signal Y2(B0)
RX13	External input signal X3(B0)	RY13	External output signal Y3(B0)
RX14	External input signal X4(B0)	RY14	External output signal Y4(B0)
RX15	External input signal X5(B0)	RY15	External output signal Y5(B0)
RX16	External input signal X6(B0)	RY16	External output signal Y6(B0)
RX17	External input signal X7(B0)	RY17	External output signal Y7(B0)
RX18	External input signal X8(B0)	RY18	External output signal Y8(B0)
RX19	External input signal X9(B0)	RY19	External output signal Y9(B0)
RX1A	External input signal XA(B0)	RY1A	External output signal YA(B0)
RX1B	External input signal XB(B0)	RY1B	External output signal YB(B0)
RX1C	External input signal XC(B0)	RY1C	External output signal YC(B0)
RX1D	External input signal XD(B0)	RY1D	External output signal YD(B0)
RX1E	External input signal XE(B0)	RY1E	External output signal YE(B0)
RX1F	External input signal XF(B0)	RY1F	External output signal YF(B0)
RX20	External input signal X0(B1)	RY20	External output signal Y0(B1)
RX21	External input signal X1(B1)	RY21	External output signal Y1(B1)
RX22	External input signal X2(B1)	RY22	External output signal Y2(B1)
RX23	External input signal X3(B1)	RY23	External output signal Y3(B1)
RX24	External input signal X4(B1)	RY24	External output signal Y4(B1)
RX25	External input signal X5(B1)	RY25	External output signal Y5(B1)
RX26	External input signal X6(B1)	RY26	External output signal Y6(B1)
RX27	External input signal X7(B1)	RY27	External output signal Y7(B1)
RX28	External input signal X8(B1)	RY28	External output signal Y8(B1)
RX29	External input signal X9(B1)	RY29	External output signal Y9(B1)
RX2A	External input signal XA(B1)	RY2A	External output signal YA(B1)
RX2B	External input signal XB(B1)	RY2B	External output signal YB(B1)
RX2C	External input signal XC(B1)	RY2C	External output signal YC(B1)
RX2D	External input signal XD(B1)	RY2D	External output signal YD(B1)
RX2E	External input signal XE(B1)	RY2E	External output signal YE(B1)
RX2F	External input signal XF(B1)	RY2F	External output signal YF(B1)
RX30	External input signal X0(B2)	RY30	External output signal Y0(B2)
RX31	External input signal X1(B2)	RY31	External output signal Y1(B2)
RX32	External input signal X2(B2)	RY32	External output signal Y2(B2)
RX33	External input signal X3(B2)	RY33	External output signal Y3(B2)
RX34	External input signal X4(B2)	RY34	External output signal Y4(B2)
RX35	External input signal X5(B2)	RY35	External output signal Y5(B2)
RX36	External input signal X6(B2)	RY36	External output signal Y6(B2)
RX37	External input signal X7(B2)	RY37	External output signal Y7(B2)
RX38	External input signal XY(B2) (when input is selected)	RY38	External output signal XY(B2) (when output is selected)
RX39 to RX3F	Use prohibited	RY39 to RY3F	Use prohibited

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Remote input signals	Name	Remote output signals	Name
Device number		Device number	
RX40 to RX6F	Use prohibited	RY40 to RY6F	Use prohibited

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Remote input signals Device number	Name	Remote output signals Device number	Name
RX40	External input signal X0 (E0)	RY40	External output signal Y0(E0)
RX41	External input signal X1 (E0)	RY41	External output signal Y1(E0)
RX42	External input signal X2 (E0)	RY42	External output signal Y2(E0)
RX43	External input signal X3 (E0)	RY43	External output signal Y3(E0)
RX44	External input signal X4 (E0)	RY44	External output signal Y4(E0)
RX45	External input signal X5 (E0)	RY45	External output signal Y5(E0)
RX46	External input signal X6 (E0)	RY46	External output signal Y6(E0)
RX47	External input signal X7 (E0)	RY47	External output signal Y7(E0)
RX48	External input signal X8 (E0)	RY48	External output signal Y8(E0)
RX49	External input signal X9 (E0)	RY49	External output signal Y9(E0)
RX4A	External input signal XA (E0)	RY4A	External output signal YA(E0)
RX4B	External input signal XB (E0)	RY4B	External output signal YB(E0)
RX4C	External input signal XC (E0)	RY4C	External output signal YC(E0)
RX4D	External input signal XD (E0)	RY4D	External output signal YD(E0)
RX4E	External input signal XE (E0)	RY4E	External output signal YE(E0)
RX4F	External input signal XF (E0)	RY4F	External output signal YF(E0)
RX50	External input signal X0 (E1)	RY50	External output signal Y0(E1)
RX51	External input signal X1 (E1)	RY51	External output signal Y1(E1)
RX52	External input signal X2 (E1)	RY52	External output signal Y2(E1)
RX53	External input signal X3 (E1)	RY53	External output signal Y3(E1)
RX54	External input signal X4 (E1)	RY54	External output signal Y4(E1)
RX55	External input signal X5 (E1)	RY55	External output signal Y5(E1)
RX56	External input signal X6 (E1)	RY56	External output signal Y6(E1)
RX57	External input signal X7 (E1)	RY57	External output signal Y7(E1)
RX58	External input signal X8 (E1)	RY58	External output signal Y8(E1)
RX59	External input signal X9 (E1)	RY59	External output signal Y9(E1)
RX5A	External input signal XA (E1)	RY5A	External output signal YA(E1)
RX5B	External input signal XB (E1)	RY5B	External output signal YB(E1)
RX5C	External input signal XC (E1)	RY5C	External output signal YC(E1)
RX5D	External input signal XD (E1)	RY5D	External output signal YD(E1)
RX5E	External input signal XE (E1)	RY5E	External output signal YE(E1)
RX5F	External input signal XF (E1)	RY5F	External output signal YF(E1)
RX60	External input signal X0 (E2)	RY60	External output signal Y0(E2)
RX61	External input signal X1 (E2)	RY61	External output signal Y1(E2)
RX62	External input signal X2 (E2)	RY62	External output signal Y2(E2)
RX63	External input signal X3 (E2)	RY63	External output signal Y3(E2)
RX64	External input signal X4 (E2)	RY64	External output signal Y4(E2)
RX65	External input signal X5 (E2)	RY65	External output signal Y5(E2)
RX66	External input signal X6 (E2)	RY66	External output signal Y6(E2)
RX67	External input signal X7 (E2)	RY67	External output signal Y7(E2)
RX68	External input signal X8 (E2)	RY68	External output signal Y8(E2)
RX69	External input signal X9 (E2)	RY69	External output signal Y9(E2)
RX6A	External input signal XA (E2)	RY6A	External output signal YA(E2)
RX6B	External input signal XB (E2)	RY6B	External output signal YB(E2)
RX6C	External input signal XC (E2)	RY6C	External output signal YC(E2)
RX6D	External input signal XD (E2)	RY6D	External output signal YD(E2)
RX6E	External input signal XE (E2)	RY6E	External output signal YE(E2)
RX6F	External input signal XF (E2)	RY6F	External output signal YF(E2)

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Remote input signals	Name	Remote output signals	Name
Device number		Device number	
RX40	External input signal X0 (E0)	RY40	External output signal Y0(E0)
RX41	External input signal X1 (E0)	RY41	External output signal Y1(E0)
RX42	External input signal X2 (E0)	RY42	External output signal Y2(E0)
RX43	External input signal X3 (E0)	RY43	External output signal Y3(E0)
RX44	External input signal X4 (E0)	RY44	External output signal Y4(E0)
RX45	External input signal X5 (E0)	RY45	External output signal Y5(E0)
RX46	External input signal X6 (E0)	RY46	External output signal Y6(E0)
RX47	External input signal X7 (E0)	RY47	External output signal Y7(E0)
RX48	External input signal XY (E0) (when input is selected)	RY48	External output signal XY(E0) (when output is selected)
RX49 to RX4F	Use prohibited	RY49 to RY4F	Use prohibited
RX50	External input signal X0 (E1)	RY50	External output signal Y0(E1)
RX51	External input signal X1 (E1)	RY51	External output signal Y1(E1)
RX52	External input signal X2 (E1)	RY52	External output signal Y2(E1)
RX53	External input signal X3 (E1)	RY53	External output signal Y3(E1)
RX54	External input signal X4 (E1)	RY54	External output signal Y4(E1)
RX55	External input signal X5 (E1)	RY55	External output signal Y5(E1)
RX56	External input signal X6 (E1)	RY56	External output signal Y6(E1)
RX57	External input signal X7 (E1)	RY57	External output signal Y7(E1)
RX58	External input signal XY (E1) (when input is selected)	RY58	External output signal XY(E1) (when output is selected)
RX59 to RX5F	Use prohibited	RY59 to RY5F	Use prohibited
RX60	External input signal X0 (E2)	RY60	External output signal Y0(E2)
RX61	External input signal X1 (E2)	RY61	External output signal Y1(E2)
RX62	External input signal X2 (E2)	RY62	External output signal Y2(E2)
RX63	External input signal X3 (E2)	RY63	External output signal Y3(E2)
RX64	External input signal X4 (E2)	RY64	External output signal Y4(E2)
RX65	External input signal X5 (E2)	RY65	External output signal Y5(E2)
RX66	External input signal X6 (E2)	RY66	External output signal Y6(E2)
RX67	External input signal X7 (E2)	RY67	External output signal Y7(E2)
RX68	External input signal XY (E2) (when input is selected)	RY68	External output signal XY(E2) (when output is selected)
RX69 to RX6F	Use prohibited	RY69 to RY6F	Use prohibited

Details of remote input signals

FPGA controlling flag

■Device number

Name	Device number
FPGA controlling flag	RX0

■Description

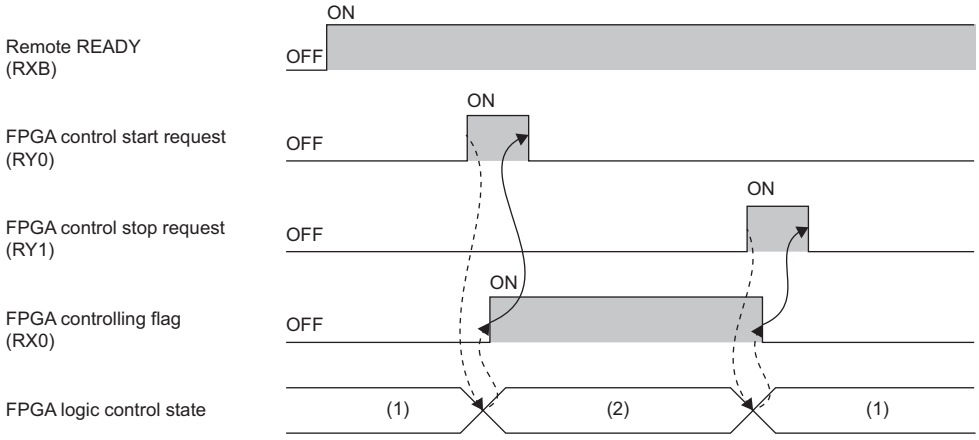
The FPGA controlling flag (RX0) turns on while the FPGA is operating.

This signal turns on under the following conditions.

- When FPGA control start request (RY0) turns on
- When FPGA configuration is completed when "FPGA control automatic start setting" is "enable"
- When "FPGA control continuation setting" is set to "Stop" in CC-Link IE TSN communication mode and FPGA control is started depending on the status of the CPU module or data link (example: CPU module STOP → RUN, during disconnection → during cyclic transmission)

This signal turns off under the following conditions.

- When FPGA control stop request (RY1) turns on
- When a moderate or severe error occurs in the FPGA module
- When "FPGA control continuation setting" is set to "Stop" in CC-Link IE TSN communication mode and the CPU module status and data link status become such that FPGA control is stopped (example: CPU module RUN → STOP, during cyclic transmission → during disconnection)
- When starting FPGA download
- While executing the parameter write using FPGA Module Configuration Tool



A

Parameter saving completion flag

■Device number

Name	Device number
Parameter saving completion flag	RX2

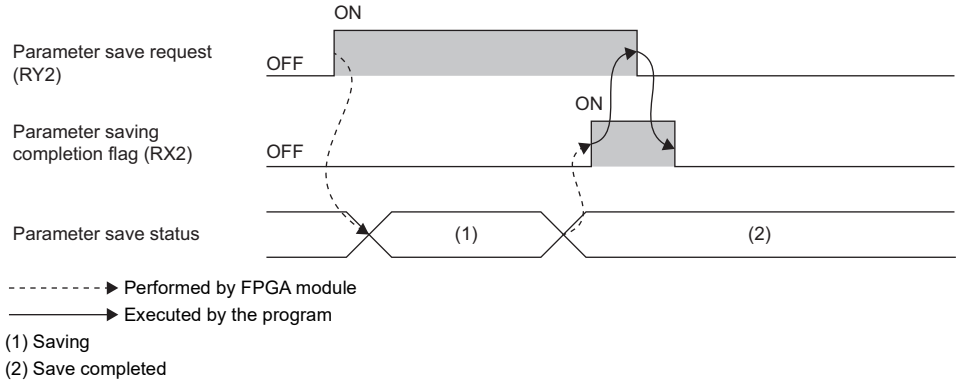
■Description

Turns on when a parameter is saved in non-volatile memory by turning on Parameter save request (RY2).

Use as an interlock to turn on and off Parameter save request (RY2).

For details on parameters, refer to the following.

☞ Page 502 FPGA register



(1) Saving

(2) Save completed

Logging start flag

■Device number

Name	Device number
Logging start flag	RX3

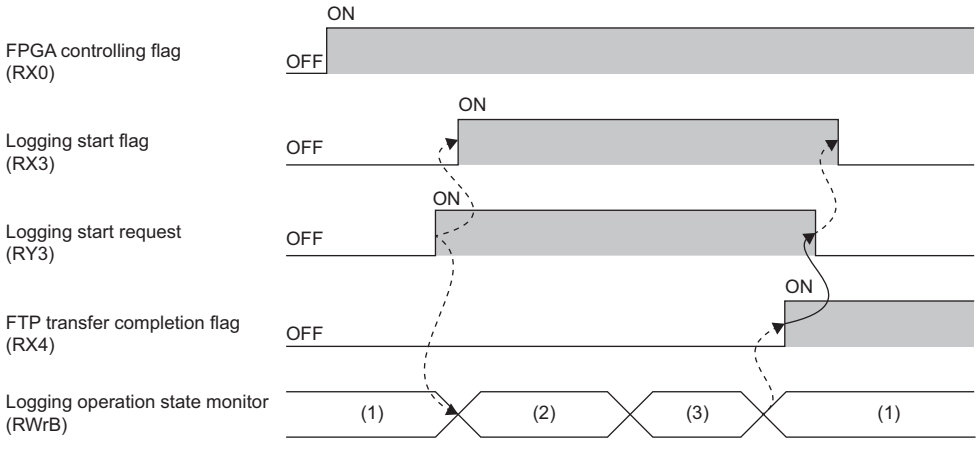
■Description

Turns on when starting the logging or transferring logging data to the FTP server by turning on Logging start request (RY3).
Use as an interlock to turn on and off Logging start request (RY3).
This signal turns on in the following conditions.

- Logging start request (RY3) is turned on when FPGA controlling flag (RX0) is ON and Logging operation status monitor (RWrB) is "Collection start waiting (1H)".
- When Logging operation status monitor (RWrB) is FTP transfer start waiting (5H), Logging start request (RY3) is turned on.

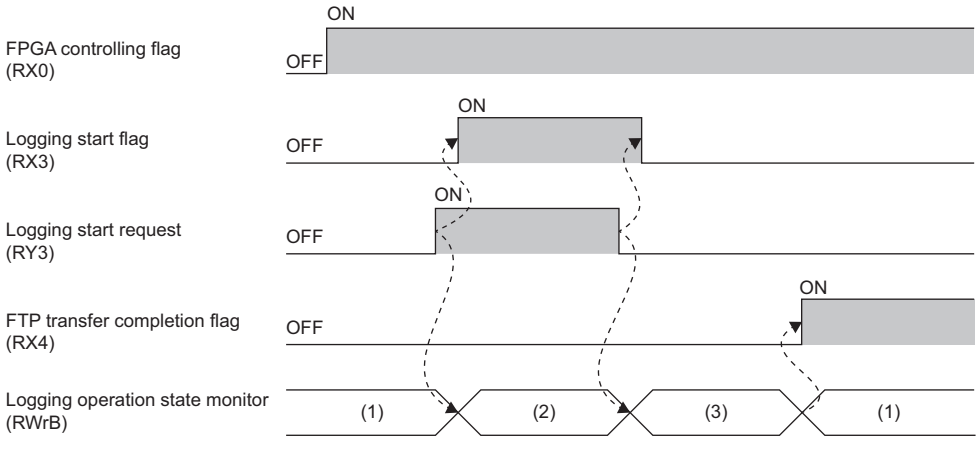
This signal turns off when Logging start request (RY3) is turned off.

■Logging start request



(1) Collection start waiting (1H)
(2) Collecting (2H)
(3) FTP transferring (4H)

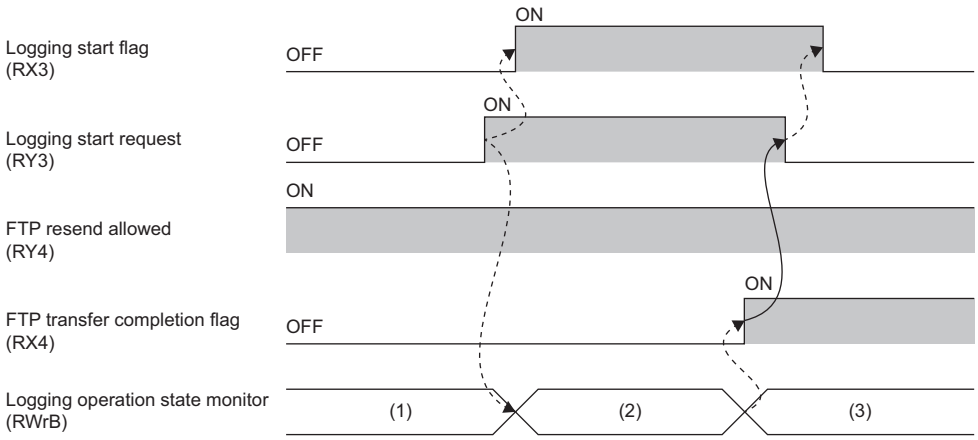
■Stop request at arbitrary timing after logging starts



(1) Collection start waiting (1H)
(2) Collecting (2H)
(3) FTP transferring (4H)

A

■Logging data re-transfer



Performed by FPGA module

Executed by the program

(1) FTP transfer start waiting (5H)

(2) FTP transferring (4H)

(3) Collection start waiting (1H)

FTP transfer completion flag

■Device number

Name	Device number
FTP transfer completion flag	RX4

■Description

Turns on when the logging data transfer to the FTP server is completed successfully or with an error.

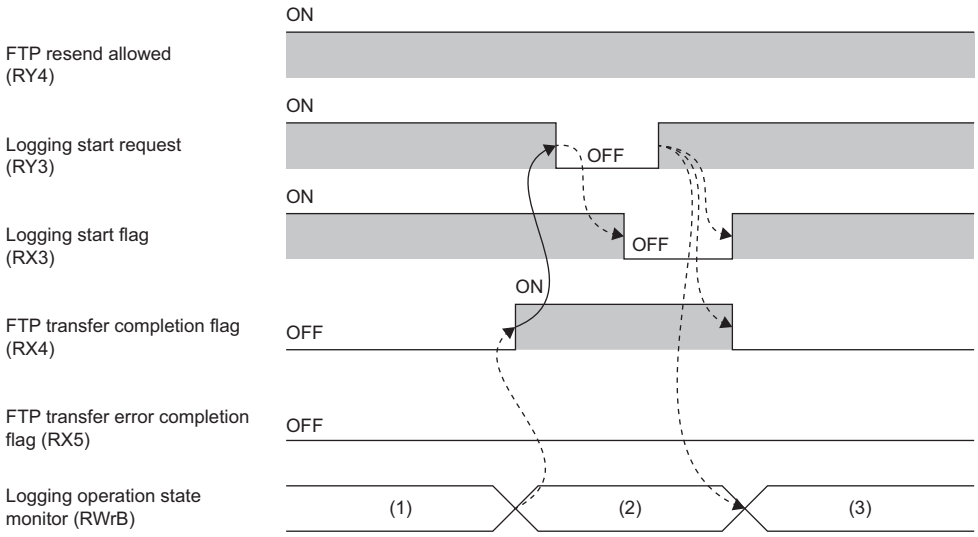
Successful completion and error completion can be verified with FTP transfer error completion flag (RX5).

- When completed successfully: FTP transfer error completion flag (RX5) is OFF
- When completed with an error: FTP transfer error completion flag (RX5) is ON

This signal and FTP transfer error completion flag (RX5) turn off in the following conditions.

- Logging start request (RY3) was turned on and the logging started.
- Logging start request (RY3) was turned on and the logging data was transferred again from the beginning.
- Logging started from the user circuit.

■When completed successfully



Performed by FPGA module

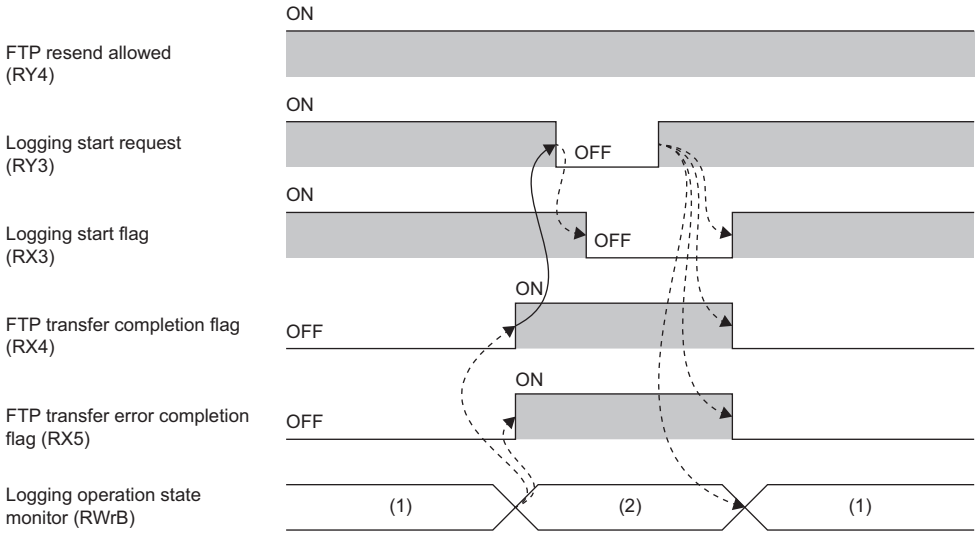
Executed by the program

(1) FTP transferring (4H)

(2) Collection start waiting (1H)

(3) Collecting (2H)

■When completed with an error



Performed by FPGA module

Executed by the program

(1) FTP transferring (4H)

(2) FTP transfer start waiting (5H)

FTP transfer error completion flag

■Device number

Name	Device number
FTP transfer error completion flag	RX5

■Description

Turns on when the transfer of logging data to the FTP server is completed with an error. For details, refer to the following.

☞ Page 473 FTP transfer completion flag

FPGA control stop while data collection flag

■Device number

Name	Device number
FPGA control stop while data collection flag	RX6

■Description

Turns on when FPGA control stops while collecting the logging data.

The logging data is not transferred to the FTP server when FPGA control operation stops. Refer to this signal and perform transfer as necessary.

This signal turns off in the following conditions.

- Logging start request (RY3) was turned on and the logging started.
- Logging start request (RY3) was turned on and the logging data was transferred again from the beginning.
- Logging started from the user circuit.

Logging control suspension flag

■Device number

Name	Device number
Logging control suspension flag	RX7

■Description

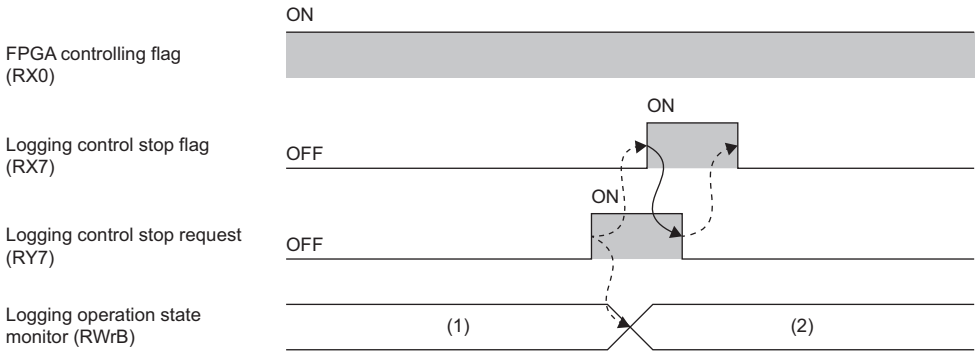
Use as an interlock to turn on and off the logging control suspend request (RY7) used to stop the logging data collection or FTP transfer.

This signal turns on under the following conditions.

- When Logging operation status monitor (RWrB) is Collecting (2H) or Collecting after trigger (3H), if Logging control suspend request (RY7) is turned on, this signal turns on and Logging operation status monitor (RWrB) becomes Collection start waiting (1H).
- This signal turns on when the logging control suspend request (RY7) is turned on while the Logging operation status monitor (RWrB) is FTP transferring (4H). Depending on the ON/OFF state of FTP resend allowed (RY4), the Logging operation status monitor (RWrB) becomes FTP transfer start waiting (5H) when FTP resend allowed (RY4) is ON, and becomes Collection start waiting (1H) when FTP resend allowed (RY4) is OFF.

This signal turns off when Logging control suspend request (RY7) is turned off.

■2H: Collecting or 3H: Collecting after trigger



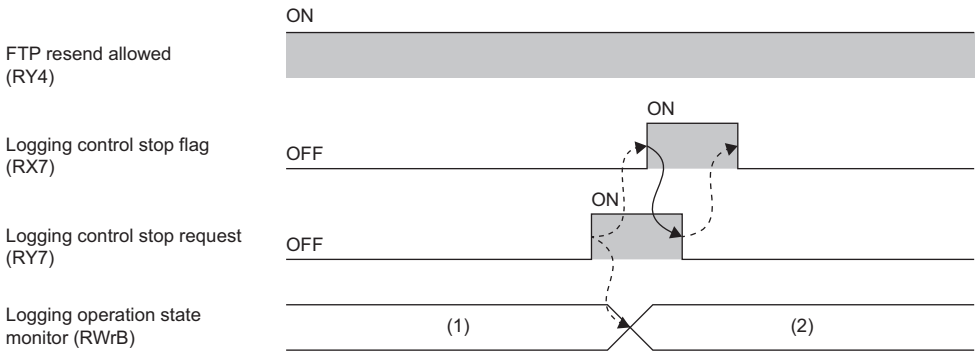
Performed by FPGA module

Executed by the program

(1) Collecting (2H) / Collecting after trigger (3H)

(2) Collection start waiting (1H)

■4H: FTP transfer



Performed by FPGA module

Executed by the program

(1) FTP transferring (4H)

(2) FTP transfer start waiting (5H)

A

Error flag

■Device number

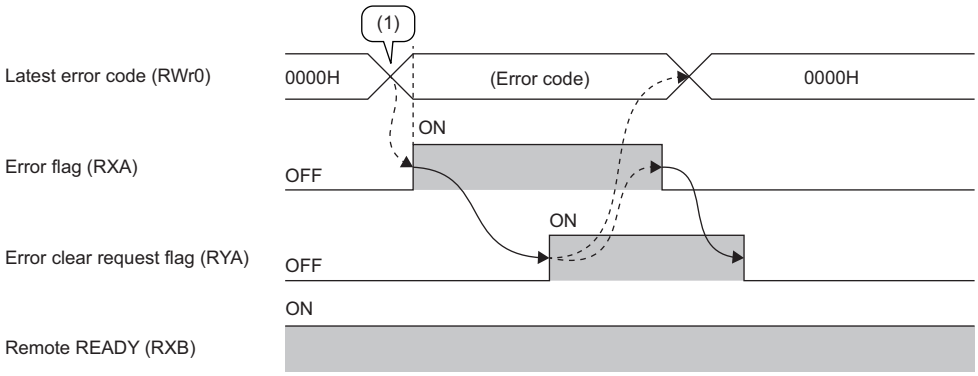
Name	Device number
Error flag	RXA

■Description

Error flag (RXA) turns on when an error occurs.

To clear the Error flag (RXA) and the latest error code (RWr0), turn the error clear request (RYA) on and off.

■When a minor error occurs

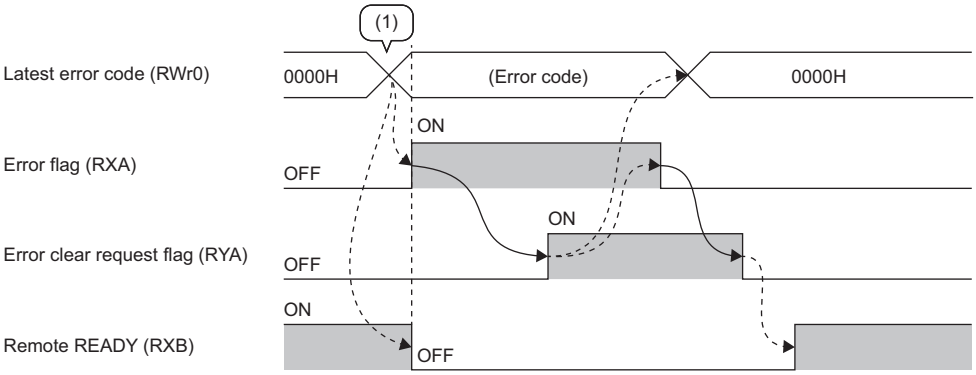


Performed by FPGA module

Executed by the program

(1) An error occurs.

■With a moderate error

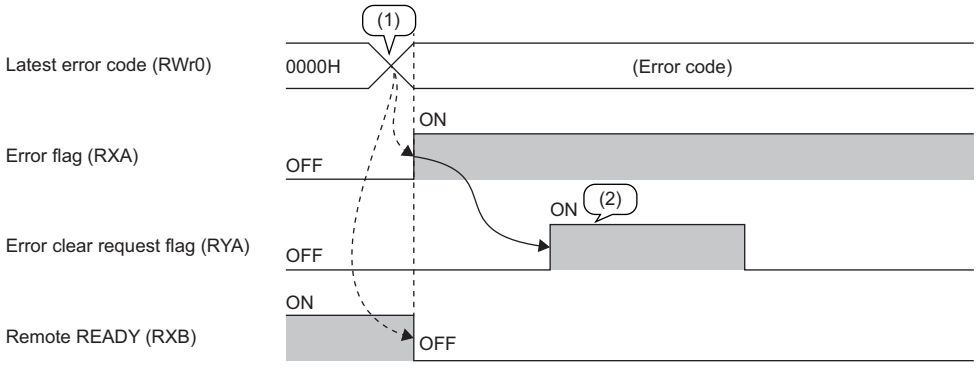


Performed by FPGA module

Executed by the program

(1) An error occurs.

■When a major error occurs



Performed by FPGA module

Executed by the program

(1) An error occurs.

(2) When a major error occurs, it is not cleared even by executing an error clear request.

Remote READY

■Device number

Name	Device number
Remote READY	RXB

■Description

Remote READY (RXB) turns on after the module power supply is turned on.

Use as an interlock to read and write remote I/O signals, remote register areas, and remote buffer memory from the master module or SLMP-compatible device.

Remote READY (RXB) turns off in the following conditions.

- When a moderate or severe error occurs
- During FPGA download

External input signal X0 to XF (B0 to B2, E0 to E2)

■Device number

Name	Device number
External input signal X0 to XF (B0 to B2, E0 to E2)	RX10 to RX6F

Point

- The allocation differs depending on the mounted module. (☞ Page 463 List of remote I/O signals)
- This signal reflects the value of the 0th bit of the input signal monitor (iport_iob0x_monitor to iport_ioe2x_monitor) and I/O signal monitor (ioport_iob0_dio485_monitor to ioport_ioe2_dio485_monitor) in the FPGA register. (☞ Page 519 FPGA register details (reset control part))

■Description

Indicates the ON/OFF status of external inputs B0 to B2 and E0 to E2.

Point

While FPGA control is stopped, the external input signal is turned off.

External input signal XY (B0 to B2, E0 to E2)

■Device number

Name	Device number
External input signal XY (B0 to B2, E0 to E2)	RX18, RX28, RX38, RX48, RX58, RX68

Point

- The allocation differs depending on the mounted module. (☞ Page 463 List of remote I/O signals)
- This signal reflects the value of the 0th bit of the input signal monitor (iport_iob0x_monitor to iport_ioe2x_monitor) and I/O signal monitor (ioport_iob0_dio485_monitor to ioport_ioe2_dio485_monitor) in the FPGA register. (☞ Page 519 FPGA register details (reset control part))

■Description

Indicates the ON/OFF status of the external input when using the XY terminal as an input terminal in a main module or extension module that has an XY terminal.

When used as an output terminal, it is always OFF.

For how to use the XY terminal (input/output selection), refer to the following register. (☞ Page 519 FPGA register details (reset control part))

- Output signal/Input output direction signal selection (B0) (ioport_iob0_dio485_osel)
- Output value/Input output direction setting (B0) (ioport_iob0_dio485_odata)

Point

While FPGA control is stopped, the external input signal is turned off.

Details of remote output signals

FPGA control start request

■Device number

Name	Device number
FPGA control start request	RY0

■Description

Use to start FPGA control.

If FPGA controlling flag (RX0) is OFF, FPGA control is stopped.

Turning on FPGA control start request (RY0) starts FPGA control.

When FPGA control automatic start setting is set to "Enable", FPGA control starts automatically when the module power supply is turned on. It is not necessary to turn on FPGA control start request (RY0).

For the timing of turning on and off FPGA control start request (RY0), refer to the following.

☞ Page 469 FPGA controlling flag

FPGA control stop request

■Device number

Name	Device number
FPGA control stop request	RY1

■Description

Use to stop FPGA control.

When FPGA control is stopped by turning and on FPGA control stop request (RY1), operations such as digital input/output, A/D conversion, and D/A conversion are stopped. The values of FPGA register areas that monitor the digital input and analog input are also cleared. (☞ Page 502 FPGA register)

For the timing of turning on and off FPGA control stop request (RY1), refer to the following.

☞ Page 469 FPGA controlling flag

Parameter save request

■Device number

Name	Device number
Parameter save request	RY2

■Description

Turning on the FPGA parameter save request (RY2) saves the current FPGA module parameters in non-volatile memory.

For the timing of turning on and off FPGA parameter save request (RY2), refer to the following.

☞ Page 470 Parameter saving completion flag

For the parameter area, refer to the following.

☞ Page 502 FPGA register

Logging start request

■Device number

Name	Device number
Logging start request	RY3

■Description

Use to start/stop collecting logging data. It is also used to re-transfer logging data from the beginning.

For the timing of turning on and off Logging start request (RY3), refer to the following.

☞ Page 471 Logging start flag

FTP resend allowed

■Device number

Name	Device number
FTP resend allowed	RY4

■Description

Specify whether to re-transfer logging data to the FTP server when the following occurs.

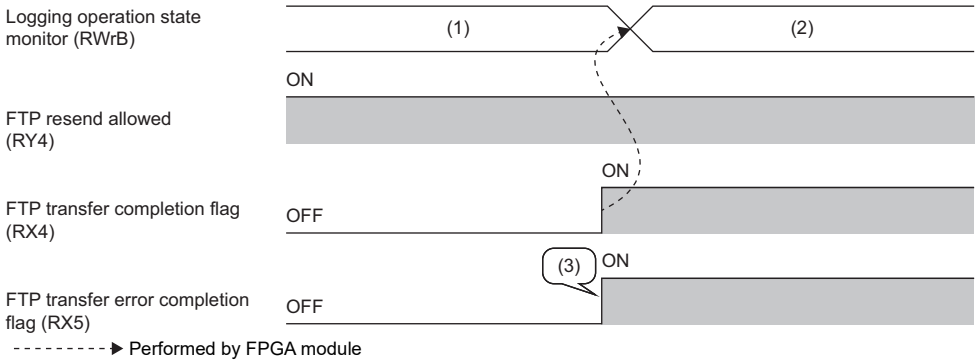
❶An FTP communication error occurred while transferring logging data to the FTP server.

❷Turn on Logging control suspend request (RY7) during logging data transfer.

❸FPGA control was stopped while collecting logging data.

■When re-transferring

- Start logging with FTP resend allowed (RY4) ON. When ❶ to ❸ occurs, the Logging operation status monitor (RWrB) becomes FTP transfer start waiting (5H), and logging data can be re-transferred. When Logging start request (RY3) is turned on in this state, the transfer is executed again.

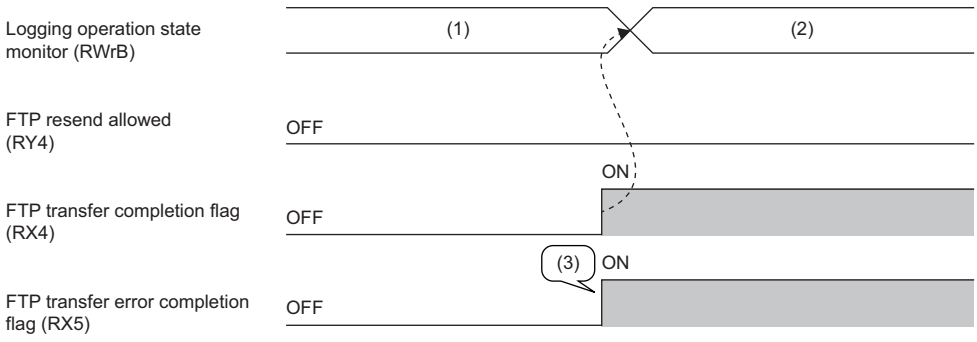


(1) FTP transferring (4H)
(2) FTP transfer start waiting (5H)
(3) FTP communication error occurred

- If FTP resend allowed (RY4) is turned off while Logging operation status monitor (RWrB) is FTP transfer start waiting (5H), Logging operation status monitor (RWrB) becomes Collection start waiting (1H). (The re-transferable state is canceled and logging can be started.)

■When not to re-transfer

Start logging with FTP resend allowed (RY4) OFF. When ❶ to ❸ occurs, the Logging operation status monitor (RWrB) becomes Collection start waiting (1H).



(1) FTP transferring (4H)
(2) Collection start waiting (1H)
(3) FTP communication error occurred

A

Logging control suspend request

■Device number

Name	Device number
Logging control suspend request	RY7

■Description

Use to stop collecting logging data or transferring logging data to the FTP server.

For the timing of turning on and off Logging control suspension flag (RX7), refer to the following.

☞ Page 475 Logging control suspension flag

Error clear request flag

■Device number

Name	Device number
Error clear request flag	RYA

■Description

Use to clear Error flag (RXA) and Latest error code (RWr0).

The error history is not cleared even when this flag is turned on.

For the timing of turning on and off Error clear request flag (RYA), refer to the following.

☞ Page 476 Error flag

■When a minor or moderate error occurs

- Eliminating the cause of the error and turning on Error clear request flag (RYA) allows the error status to be cleared, resulting in Error flag (RXA) turning off.
- Before Error flag (RXA) turns off, turning off Error clear request flag (RYA) does not allow Error flag (RXA) to turn off.

■When a major error occurs

Error status (RXA) does not turn off even by turning on Error clear request flag (RYA).

External output signal Y0 to YF(B0 to B2, E0 to E2)

■Device number

Name	Device number
External output signal Y0 to YF(B0 to B2, E0 to E2)	RY10 to RY6F

Point

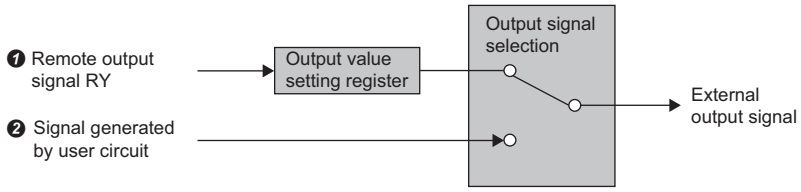
The external output signal corresponding to the remote output signal (RY) differs depending on the FPGA module model. (☞ Page 463 List of remote I/O signals)

■Description

External output signals for digital output (24VDC output, differential output) can be selected to output any of the following by setting the FPGA register.

❶Remote output signal (RY)

❷Signal generated by user circuit



When ❶ is selected, this signal can be used to turn on/off the external output signal.
When ❷ is selected, turning this signal on/off is not reflected in the external output signal.

In either ❶ or ❷, the state of this signal is reflected in the output value setting (B0) (oport_iob0y_odata) to output value setting (E2) (oport_ioe2y_odata) of the FPGA register. Select the output signal using Output signal selection (B0) (oport_iob0y_osel) to Output signal selection (E2) (oport_ioe2y_osel). (☞ Page 502 FPGA register)

External output signals for analog output cannot be turned on/off with this signal.

Point

- Always set Remote output (RY), which is prohibited to use, to OFF. (☞ Page 463 List of remote I/O signals)
- External output signals while FPGA control is stopped follow the HOLD/CLEAR setting. (☞ Page 315 FPGA Control Function)

A

External output signal XY(B0 to B2, E0 to E2)

■Device number

Name	Device number
External output signal XY(B0 to B2, E0 to E2)	RY18, RY28, RY38, RY48, RY58, RY68

Point

The external output signal corresponding to the remote output signal (RY) differs depending on the FPGA module model. (☞ Page 463 List of remote I/O signals)

■Description

When an XY terminal is set to ❶ and ❷ below in Main module or Extension module with XY terminal, the external output signal can be turned on or off with this signal.

❶Use XY terminals as output terminals

❷Use Remote output signal RY as the output value (selection of output signal is the same as for external output signals Y0 to YF)

If ❶ or ❷ is not satisfied, RY18, RY28, RY38, RY48, RY58, and RY68 must always be OFF.

I/O selection and output signal selection are performed in Output value/Input output direction setting (B0) (ioport_iob0_dio485_odata) to Output value/Input output direction setting (E2) (ioport_ioe2_dio485_osel) register areas. (☞ Page 502 FPGA register)

Point

External output signals while FPGA control is stopped follow the HOLD/CLEAR setting. (☞ Page 315 FPGA Control Function)

Appendix 2 Remote Register

Remote register (RWr) is the state of FPGA module (error, logging, user circuit).
In CC-Link IE TSN communication mode, the master module receives Remote register (RWr) from FPGA module. Also, Remote register (RWr) can be received from an external device via SLMP communication regardless of the operation mode setting.
Remote register (RWw) is information (such as logging and user circuit) that controls FPGA module.
In CC-Link IE TSN communication mode, the master module sends Remote register (RWw) to FPGA module. In standalone mode, Remote register (RWw) can be sent from an external device via SLMP communication.

List of remote registers

A list of remote register assignments is shown below.

Point

Do not write to prohibited remote register areas. Writing data may result in an accident due to an incorrect output or malfunction.

Remote register areas (RWr) Device number	Name	Remote register areas (RWw) Device number	Name
RWr0	Latest error code	RWw0	Use prohibited
RWr1	Use prohibited	RWw1	
RWr2		RWw2	
RWr3		RWw3	
RWr4		RWw4	
RWr5		RWw5	
RWr6		RWw6	
RWr7		RWw7	
RWr8		RWw8	
RWr9		RWw9	
RWrA	Echo back number	RWwA	Confirmation number
RWrB	Logging operation status monitor	RWwB	Use prohibited
RWrC	Sampling count monitor	RWwC	
RWrD		RWwD	
RWrE	FTP transfer count monitor	RWwE	
RWrF	Use prohibited	RWwF	
RWr10 to RWr8F	FPGA register read area	RWw10 to RWw8F	FPGA register write area

Details of remote registers

Latest error code

■Device number

Name	Device number
Latest error code	RWr0

■Description

The error code is stored when an error occurs. This register is cleared when Error clear request flag (RYA) is turned on after removing the cause of the error that occurred.

When the generated error is a major error, this register will not be cleared even if Error clear request (RYA) is turned on.

For errors that occurred in the past, refer to the following.

☞ Page 450 Checking by using CC-Link IE TSN/CC-Link IE Field diagnostics

Echo back number, confirmation number

■Device number

Name	Device number
Echo back number	RWrA
Confirmation number	RWwA

■Description

Whether the value of the remote register (RWw) has been transferred to the FPGA module can be checked. The confirmation number is reflected in the echo back number by the FPGA module.

In the CC-Link IE TSN system configure, the scan time of the CPU module and the communication cycle interval of the master station are asynchronous. Therefore, if the communication cycle interval is longer than the scan time, Remote register (RWw) is not transmitted to the FPGA module for each scan of the CPU module.

The confirmation number and echo back number can be used as conditions for changing the remote register (RWw) of FPGA module in the program of the CPU module.

Logging operation status monitor

■Device number

Name	Device number
Logging operation status monitor	RWrB

■Description

Monitors the operating status of the logging function. Stored values and operating states are shown below. (☞ Page 327 Logging Function)

Stored value	Logging operation status	Description
0H	Disable	The logging function is disabled and data cannot be collected.
1H	Collection start waiting	Waiting for the logging to start.
2H	Collecting	Logging data is being collected.
3H	Collecting after trigger	Data is being collected after trigger detection when the trigger operation is set.
4H	FTP transferring	The collected logging data is being transferred to the FTP server.
5H	FTP transfer start waiting	Waiting for FTP re-transfer request.

Precautions

When FPGA download is executed, logging data collection and logging data transfer are stopped, and Logging operation status monitor (RWrB) becomes Disable (0H).

Sampling count monitor

■Device number

Name	Device number
Sampling count monitor	RWrC, RWrD

■Description

Stores the number of times logging data was sampled after logging started.
The value is cleared to 0 when logging starts and is incremented by 1 at each sampling.
It does not count up beyond 4294967295 (FFFFFFFFH).

FTP transfer count monitor

■Device number

Name	Device number
FTP transfer count monitor	RWrE

■Description

The monitor is incremented by 1 when the FTP transfer is completed successfully.
When it exceeds 65535 (FFFFH), it becomes 0, but continues incrementing upon completion of the FTP transfer.

FPGA register read area

■Device number

Name	Device number
FPGA register read area	RWr10 to RWr8F

■Description

The value of read data (cyclic area) (usr_rreg_180 to usr_rreg_1FF) is read to this register. (☞ Page 321 FPGA Register Access Function)

FPGA register write area

■Device number

Name	Device number
FPGA register write area	RWw10 to RWw8F

■Description

This register is written to the write data (cyclic area) (usr_wreg_180 to usr_wreg_1FF). (☞ Page 321 FPGA Register Access Function)

Appendix 3 Remote Buffer Memory

Describes the remote buffer memory.

The SLMP command and dedicated instructions (REMTO, REMTOD, REMTOIP, REMTODIP, REMFR, REMFRD, REMFRIP, and REMFRDIP instructions) can be used to read from and write to the remote buffer memory.

For the dedicated instructions, refer to the following.

📖 MELSEC iQ-R Programming Manual (Module Dedicated Instructions)

For SLMP commands, refer to the following.

☞ Page 351 SLMP Communication Function

Point

- Do not read or write data from/to any "Use prohibited" remote buffer memory areas. Doing so may result in an accident due to an incorrect output or malfunction.
- For a single FPGA module, do not execute multiple dedicated instructions at the same time. If multiple dedicated instructions are executed at the same time, the FPGA module may be unable to receive the dedicated instructions, and the dedicated instructions may time out.

List of remote buffer memory areas

Module parameter area

■Function setting switch setting

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
04D0H	1232	User switch enable/disable	0H	○	○

■Setting of module start

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
04D1H	1233	FPGA control automatic start setting	0H	○	○
04D2H	1234	FPGA control automatic start delay setting	0	○	○

■Parameter setting

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
04D3H	1235	User circuit part parameter size	0	○	○

■Operation setting during disconnection

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
04D4H	1236	FPGA control continuation setting	0	○	○

■DAC CH0 (E0) setting parameter to DAC CH1 (E2) setting parameter

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
0600H	1536	Use prohibited	—	×	×
0601H	1537	DAC offset CH0(E0)	8000H	○	○
0602H	1538	DAC range setting CH0(E0)	0003H	○	○
0603H, 0604H	1539, 1540	Use prohibited	—	×	×
0605H	1541	DAC offset CH1(E0)	8000H	○	○
0606H	1542	DAC range setting CH1(E0)	0003H	○	○
0607H, 0608H	1543, 1544	Use prohibited	—	×	×
0609H	1545	DAC offset CH0(E1)	8000H	○	○
060AH	1546	DAC range setting CH0(E1)	0003H	○	○
060BH, 060CH	1547, 1548	Use prohibited	—	×	×
060DH	1549	DAC offset CH1(E1)	8000H	○	○
060EH	1550	DAC range setting CH1(E1)	0003H	○	○
060FH, 0610H	1551, 1552	Use prohibited	—	×	×
0611H	1553	DAC offset CH0(E2)	8000H	○	○
0612H	1554	DAC range setting CH0(E2)	0003H	○	○
0613H, 0614H	1555, 1556	Use prohibited	—	×	×
0615H	1557	DAC offset CH1(E2)	8000H	○	○
0616H	1558	DAC range setting CH1(E2)	0003H	○	○
0617H to 8FFH	1559 to 2303	Use prohibited	—	×	×

Monitor area

■User circuit check

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
0900H, 0901H	2304, 2305	Configuration data CRC	0	○	×

■Function setting switch monitor

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
0902H	2306	Function setting switch state monitor	—	○	×

■Module information monitor

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
0903H	2307	Firmware version	—	○	×
0904H	2308	FPGA version	—	○	×

Module control data area

■Parameter initialization

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1000H	4096	Parameter initialization command	0	○	○
1001H	4097	Parameter initialization completion	0	○	×

FPGA register access area

■FPGA register write

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1200H, 1201H	4608, 4609	Write start address	0000H	○	○
1202H	4610	Write size	0000H	○	○
1203H	4611	Write request	0000H	○	○

■Write area

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1204H	4612	Write data 0	0000H	○	○
1205H	4613	Write data 1	0000H	○	○
1206H	4614	Write data 2	0000H	○	○
⋮		⋮			
1381H	4993	Write data 381	0000H	○	○
1382H	4994	Write data 382	0000H	○	○
1383H	4995	Write data 383	0000H	○	○

■FPGA register read

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1400H, 1401H	5120, 5121	Read start address	0000H	○	○
1402H	5122	Read size	0000H	○	○
1403H	5123	Read request	0000H	○	○

■Read area

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1404H	5124	Read data 0	—	○	○
1405H	5125	Read data 1	—	○	○
1406H	5126	Read data 2	—	○	○
⋮		⋮			
1581H	5505	Read data 381	—	○	○
1582H	5506	Read data 382	—	○	○
1583H	5507	Read data 383	—	○	○

Time information setting area

■Time information setting

○: Applicable, ×: Not applicable

Address		Name	Default value	Read	Write
Hexadecimal	Decimal				
1600H	5632	Time information set	0000H	○	○
1601H	5633	Time information (year)	0000H	○	○
1602H	5634	Time information (month, day, hour)	0000H	○	○
1603H	5635	Time information (minute, second)	0000H	○	○

Details of remote buffer memory

This section describes the details of remote buffer memory addresses of FPGA module.

User switch enable/disable

■Address

Name	Remote buffer memory address
User switch enable/disable	04D0H

■Description

Enables or disables USER switch (function setting switch 7) to USER switch (function setting switch 10).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) USER switch
0: Disable (Default)
1: Enable

When enabled (1), the corresponding bit of Always write register 0 (usr_alwreg_00) in the user circuit part can be operated from the USER switch. The correspondence between USER switches and Always write register 0 (usr_alwreg_00) is shown below.

- USER switch (function setting switch 7): Always write register 0 (usr_alwreg_00) (FPGA register address: 1000_A010H) b3
- USER switch (function setting switch 8): Always write register 0 (usr_alwreg_00) (FPGA register address: 1000_A010H) b2
- USER switch (function setting switch 9): Always write register 0 (usr_alwreg_00) (FPGA register address: 1000_A010H) b1
- USER switch (function setting switch 10): Always write register 0 (usr_alwreg_00) (FPGA register address: 1000_A010H) b0

For details on the USER switch (function setting switch 7) to USER switch (function setting switch 10), refer to the following.

☞ Page 58 Setting the function setting switches

■Enabling the setting

It is reflected when starting FPGA control.

FPGA control automatic start setting

■Address

Name	Remote buffer memory address
FPGA control automatic start setting	04D1H

■Description

Sets whether to automatically start FPGA control after FPGA configuration is complete.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) FPGA control automatic start setting
0: Disable (Default)
1: Enable

■Enabling the setting

When Parameter save request (RY2) is turned on and off, the setting is enabled.

FPGA control automatic start delay setting

■Address

Name	Remote buffer memory address
FPGA control automatic start delay setting	04D2H

■Description

Sets the time from FPGA configuration completion until the automatic start of FPGA control.

■Setting range

0 to 255[s] (Default: 0)

Point

When the value outside of the setting range is specified, the FPGA module works as 255.

■Enabling the setting

When Parameter save request (RY2) is turned on and off, the setting is enabled.

User circuit part parameter size

■Address

Name	Remote buffer memory address
User circuit part parameter size	04D3H

■Description

From the start address of the write data (transient area) in the FPGA register of the user circuit part, sets the size to be saved in non-volatile memory as the FPGA parameter in units of words.

After FPGA configuration is complete, parameters of a size equivalent to that saved in non-volatile memory are set to Write data (transient area) in FPGA register.

■Setting range

0 to 384 (Default: 0)

Point

If a value other than the above is set, it works as 384.

■Save to non-volatile memory

When saving FPGA register areas to non-volatile memory, turn on and off FPGA parameter save request (RY2).

FPGA control continuation setting

■Address

Name	Remote buffer memory address
FPGA control continuation setting	04D4H

■Description

Sets whether to stop or continue FPGA control when the data link with the CPU module and master station is broken during FPGA module operation in CC-Link IE TSN communication mode.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) FPGA control
0: Stop (default)
1: Continue

Point

This setting is ignored in standalone mode.

■Enabling the setting

When Parameter save request (RY2) is turned on and off, the setting is enabled.

DAC offset

■Address

Name	Remote buffer memory address
DAC offset CH0(E0)	0601H
DAC offset CH1(E0)	0605H
DAC offset CH0(E1)	0609H
DAC offset CH1(E1)	060DH
DAC offset CH0(E2)	0611H
DAC offset CH1(E2)	0615H

■Description

Sets the DAC offset. For details on the offset function, refer to the following.

☞ Page 211 Analog output control part (ao2_top)

■Setting range

0H to FFFFH (default: 8000H)

■Enabling the setting

Enabled at the start of FPGA control.

DAC range setting

■Address

Name	Remote buffer memory address
DAC range setting CH0(E0)	0602H
DAC range setting CH1(E0)	0606H
DAC range setting CH0(E1)	060AH
DAC range setting CH1(E1)	060EH
DAC range setting CH0(E2)	0612H
DAC range setting CH1(E2)	0616H

■Description

Sets the DAC output range.

■Setting range

- 3H: -9.9 to 9.9V (default)
- 4H: 0.2 to 19.8mA

Point

If a value outside the setting range is set, a DAC range setting CH□ (E△) setting error (error code: 33△□) is stored in the latest error code (RWr0), the error status flag (RXA) turns ON and the ERR. LED turns on.

■Enabling the setting

Enabled at the start of FPGA control.

Configuration data CRC

■Address

Name	Remote buffer memory address
Configuration data CRC	0900H, 0901H

■Description

The CRC value of the configuration data can be checked. CRC value is the CRC value of the entire configuration ROM. It is different from the checksum displayed in FPGA design software. This remote buffer memory is used when the FPGA Module Configuration Tool performs data verification of configuration data.

Point

- 0 is stored until the CRC value calculation of the configuration data reaches End.
- When writing configuration data via JTAG, the entire configuration ROM may not be written. Therefore, even if the same jic-format configuration data is written, the values in this remote buffer memory may differ.

Function setting switch state monitor

■Address

Name	Remote buffer memory address
Function setting switch state monitor	0902H

■Description

The ON/OFF status of function setting switches 1 to 10 can be checked.

At what point ON, OFF status is displayed differs depending on the function setting switch.

- Function setting switch 1 and function setting switch 3: ON/OFF status when the module power supply is ON
- Function setting switch 4 to function setting switch 10: Current ON/OFF state

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)						(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)

(1) Function setting switch 1
(2) Function setting switch 2
(3) Function setting switch 3
(4) Function setting switch 4
(5) Function setting switch 5
(6) Function setting switch 6
(7) Function setting switch 7
(8) Function setting switch 8
(9) Function setting switch 9
(10) Function setting switch 10
- 0: OFF
- 1: ON

Firmware version

■Address

Name	Remote buffer memory address
Firmware version	0903H

■Description

The firmware version of the FPGA module can be checked.

FPGA version

■Address

Name	Remote buffer memory address
FPGA version	0904H

■Description

The version of the FPGA module can be checked.

Parameter initialization command

■Address

Name	Remote buffer memory address
Parameter initialization command	1000H

■Description

This command resets parameters stored in the remote buffer memory, FPGA register, and non-volatile memory to the default values. When non-volatile memory data error (parameter) (error code: 2010H) occurs, the FPGA module can be restored. When the parameter initialization command (remote buffer memory address 1000H) is set to Commanded (1), parameters are initialized.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Parameter initialization command
- 0: Not commanded (default)
- 1: Commanded

Parameter initialization completion

■Address

Name	Remote buffer memory address
Parameter initialization completion	1001H

■Description

If the parameter initialization is completed, it will be Completed (1). For details, refer to the following.

☞ Page 496 Parameter initialization command

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Parameter initialization completed
- 0: Not implemented (default)
- 1: Finish

Write start address

■Address

Name	Remote buffer memory address
Write start address	1200H, 1201H

■Description

When writing the value stored in the write data ☐ (remote buffer memory address: 1204H to 1383H) to an FPGA register, set the start address of the FPGA register to be written.

For the writable range, refer to the following.

☞ Page 324 Method using remote buffer memory

Point

- When an odd-numbered FPGA register address or an FPGA register address outside the setting range is set and a write request (remote buffer memory address: 1203H) is set to Requested (1), Write start address out-of-range error (error code: 1100H) is stored in the latest error code (RWr0) and Error flag (RXA) turns on. At this time, writing to the FPGA register is not performed.
- The remote buffer memory is word-addressed, and FPGA register is byte-addressed. Therefore, the FPGA register stores one piece of information in a 2-byte area.

Write size

■Address

Name	Remote buffer memory address
Write size	1202H

■Description

Sets the range of FPGA register address to be written from Write start address (remote buffer memory address: 1200H, 1201H) in units of words.

For the writable range, refer to the following.

☞ Page 324 Method using remote buffer memory

■Setting range

The setting range is from 1 to 384.

Point

Set a value outside the settable range and send a write request (remote buffer memory address: 1203H) is set to requested (1), the latest error code (RWr0) is the FPGA register write size out-of-range error (error code: 1101H) is stored and Error flag (RXA) turns on. At this time, writing to the FPGA register is not performed.

Write request

■Address

Name	Remote buffer memory address
Write request	1203H

■Description

After setting Write start address (remote buffer memory address: 1200H, 1201H) and the write size (remote buffer memory address: 1202H), set this remote buffer memory to Requested (1H). The value of the write data ☐ (remote buffer memory address: 1204H to 1383H) will be stored in the set FPGA register. If the write processing is completed successfully, No request/Completed successfully (0H) is indicated. When the write processing is completed with an error, Completed with an error (-1) is indicated.

■Setting range

- 1: Requested
- 0: No request/Completed successfully (default)
- -1: Completed with an error

Point

The set value outside the setting range will be ignored.

Write data

■Address

Name	Remote buffer memory address
Write data 0 to Write data 383	1204H to 1383H

■Description

Sets the value to write to the FPGA register.

Read start address

■Address

Name	Remote buffer memory address
Read start address	1400H, 1401H

■Description

Sets the start address of the FPGA register to be read. The read value is stored in Read data ☐ (remote buffer memory address: 1404H to 1583H).

For the readable range, refer to the following.

☞ Page 324 Method using remote buffer memory

Point

- When an odd-numbered FPGA register address or an FPGA register address outside the setting range is set and Read request (remote buffer memory address: 1403H) is set to Requested (1), Read start address out-of-range error (error code: 1102H) is stored in the latest error code (RWr0), and Error flag (RXA) turns on. At this time, the FPGA register is not read.
- The remote buffer memory is word-addressed, and FPGA register is byte-addressed. Therefore, the FPGA register stores one piece of information in a 2-byte area.

Read size

■Address

Name	Remote buffer memory address
Read size	1402H

■Description

Sets the address range of the FPGA register to be read in units of words.

For the readable range, refer to the following.

☞ Page 324 Method using remote buffer memory

■Setting range

The setting range is from 1 to 384.

Point

When a value outside the setting range is set and Read request (remote buffer memory address: 1403H) is set to Requested (1), an FPGA register read size out-of-range error (error code: 1103H) is stored in the latest error code (RWr0), and Error flag (RXA) turns on. At this time, the FPGA register is not read.

Read request

■Address

Name	Remote buffer memory address
Read request	1403H

■Description

After setting Read start address (remote buffer memory address: 1400H, 1401H) and read size (remote buffer memory address: 1402H), set this remote buffer memory to Requested (1H) to store FPGA register value in Read data ☐ (remote buffer memory address: 1404H to 1583H). If the read processing is completed successfully, No request/Completed successfully (0H) is indicated. If the read processing is completed with an error, Completed with an error (-1) is indicated.

■Setting range

- 1: Requested
- 0: No request/Completed successfully (default)
- -1: Completed with an error

Point

The set value outside the setting range will be ignored.

Read Data

■Address

Name	Remote buffer memory address
Read data 0 to Read data 383	1404H to 1583H

■Description

The value read from FPGA register is stored.

Time information set

■Address

Name	Remote buffer memory address
Time information set	1600H

■Description

Time information set is used to reflect the values set below to logging data during logging and time information of error history while operating in standalone mode.

- Time information (year) (address: 1601H)
- Time information (month, day, hour) (address: 1602H)
- Time information (minute, second) (address: 1603H)

Time information is reflected by setting this buffer memory to the time information set (1). When Time information set is completed, No action (0) is indicated.

For details, refer to the following.

☞ Page 327 Logging Function

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Time information set
- 0: No action (default)
- 1: Time information set

Point

- In CC-Link IE TSN communication mode, the time sent from the master station is recorded, so the time information by this setting is not reflected.
- If no time information is set in standalone mode, FPGA module starts operating at 00:00:00.00 on January 1, 1970.
- If the time information is outside the setting range, or if the time information is within the setting range but is not valid as a date (e.g., February 30) and the time information is set (1), a time setting error (error code: 1210H) is stored in the latest error code (RWr0), and Error flag (RXA) turns on. At this time, time information is not set.

Time information (year)

■Address

Name	Remote buffer memory address
Time information (year)	1601H

■Description

Sets the time information (year) to be reflected in the logging data and error history. Set the number of years since 1970. It can be set from 1970 to 2097.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)									Time information (year)						

Time information (month, day, hour)

■Address

Name	Remote buffer memory address
Time information (month, day, hour)	1602H

■Description

Sets the time information (month, day, hour) to be reflected in the logging data and error history.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)		Month				Day					Hour				

■Setting range

- Month: 1 to 12
- Day: 1 to 31
- Hour: 0 to 23

Point

- Be careful when setting because three pieces of information are stored in one word.
- If a value outside the setting range is set, 00:00 on January 1st will be set.

Time information (minute, second)

■Address

Name	Remote buffer memory address
Time information (minute, second)	1603H

■Description

Sets the time information (month, day, hour) to be reflected in the logging data and error history.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)		Minute						0 (fixed)		Second					

■Setting range

- Minute: 0 to 59
- Second: 0 to 59

Point

- Be careful when setting because two pieces of information are stored in one word.
- If a value outside the setting range is set, 00:00 will be set.

Appendix 4 FPGA register

Describes FPGA register areas.

Precautions
Read-only bits: Invalid when writing.
Write-only bits: Fixed to 0 when read.
For the types of each register, refer to the following. ☞ Page 503 List of FPGA register areas There are restrictions on setting values for parameter register areas. Check the notes and restrictions in the FPGA register details. Setting value restrictions are checked by firmware at the start of FPGA control and when the parameter save request (RY2) is turned on, and a moderate error may occur in the module depending on the conflicting restrictions. For details, refer to the following. ☞ Page 445 TROUBLE EXAMPLES of DC INPUT/OUTPUT
The only reset cause for FPGA register areas is a reset. If there is a cause other than the above, describe it in the reset cause of FPGA register details.
FPGA initial value: Default value set by RTL for the standard and sample circuits. Firmware setting initial value: Default value set by firmware by parameter initialization command (remote buffer memory address: 1000H). If there is a cause other than the above, describe in the notes and restrictions section in FPGA register details.

List of FPGA register areas

A list of FPGA register assignments is shown below.

Reset control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_0002H	mode_ctrl2	Internal operation start/stop	—	○	○
1000_0004H	unit_set_base	Module type (main)	Monitor	○	×
1000_0006H	unit_set_ext	Module type (extension)		○	×
1000_0020H	ioport_set	External reset ON/OFF setting	—	○	○
1000_0100H	fpga_version	FPGA version register	Monitor	○	×

Timing control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_2000H	tim_iob0x_samp	Filter sampling pulse (B0)	Parameter	○	○
1000_2002H	tim_iob1x_samp	Filter sampling pulse (B1)	Parameter	○	○
1000_2004H	tim_iob2x_samp	Filter sampling pulse (B2)	Parameter	○	○
1000_2006H	Reserve				
1000_2008H	tim_ioe0x_samp	Filter sampling pulse (E0)	Parameter	○	○
1000_200AH	tim_ioe1x_samp	Filter sampling pulse (E1)	Parameter	○	○
1000_200CH	tim_ioe2x_samp	Filter sampling pulse (E2)	Parameter	○	○
1000_200EH to 1000_20FEH	Reserve				
1000_2100H	tim_iob0x_en	Data sampling timing (B0)	Parameter	○	○
1000_2102H	tim_iob1x_en	Data sampling timing (B1)	Parameter	○	○
1000_2104H	tim_iob2x_en	Data sampling timing (B2)	Parameter	○	○
1000_2106H	Reserve				
1000_2108H	tim_ioe0x_en	Data sampling timing (E0)	Parameter	○	○
1000_210AH	tim_ioe1x_en	Data sampling timing (E1)	Parameter	○	○
1000_210CH	tim_ioe2x_en	Data sampling timing (E2)	Parameter	○	○
1000_210EH	Reserve				
1000_2110H	tim_iob0x_conv	Data update timing (B0)	Parameter	○	○
1000_2112H	tim_iob1x_conv	Data update timing (B1)	Parameter	○	○
1000_2114H	tim_iob2x_conv	Data update timing (B2)	Parameter	○	○
1000_2116H	Reserve				
1000_2118H	tim_ioe0x_conv	Data update timing (E0)	Parameter	○	○
1000_211AH	tim_ioe1x_conv	Data update timing (E1)	Parameter	○	○
1000_211CH	tim_ioe2x_conv	Data update timing (E2)	Parameter	○	○
1000_2200H	tim_log_cyc	Logging cycle timing	—	○	○

Digital input control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_3000H	iport_iob0_0_filcnt_upper	Input filter counter upper limit (IOB0_X0)(B0)	Parameter	○	○
1000_3002H	iport_iob0_1_filcnt_upper	Input filter counter upper limit (IOB0_X1)(B0)	Parameter	○	○
1000_3004H	iport_iob0_2_filcnt_upper	Input filter counter upper limit (IOB0_X2)(B0)	Parameter	○	○
1000_3006H	iport_iob0_3_filcnt_upper	Input filter counter upper limit (IOB0_X3)(B0)	Parameter	○	○
1000_3008H	iport_iob0_4_filcnt_upper	Input filter counter upper limit (IOB0_X4)(B0)	Parameter	○	○
1000_300AH	iport_iob0_5_filcnt_upper	Input filter counter upper limit (IOB0_X5)(B0)	Parameter	○	○
1000_300CH	iport_iob0_6_filcnt_upper	Input filter counter upper limit (IOB0_X6)(B0)	Parameter	○	○
1000_300EH	iport_iob0_7_filcnt_upper	Input filter counter upper limit (IOB0_X7)(B0)	Parameter	○	○
1000_3010H	iport_iob0_8_filcnt_upper	Input filter counter upper limit (IOB0_X8)(B0)	Parameter	○	○
1000_3012H	iport_iob0_9_filcnt_upper	Input filter counter upper limit (IOB0_X9)(B0)	Parameter	○	○
1000_3014H	iport_iob0_a_filcnt_upper	Input filter counter upper limit (IOB0_XA)(B0)	Parameter	○	○
1000_3016H	iport_iob0_b_filcnt_upper	Input filter counter upper limit (IOB0_XB)(B0)	Parameter	○	○
1000_3018H	iport_iob0_c_filcnt_upper	Input filter counter upper limit (IOB0_XC)(B0)	Parameter	○	○
1000_301AH	iport_iob0_d_filcnt_upper	Input filter counter upper limit (IOB0_XD)(B0)	Parameter	○	○
1000_301CH	iport_iob0_e_filcnt_upper	Input filter counter upper limit (IOB0_XE)(B0)	Parameter	○	○
1000_301EH	iport_iob0_f_filcnt_upper	Input filter counter upper limit (IOB0_XF)(B0)	Parameter	○	○
1000_3020H	iport_iob1_0_filcnt_upper	Input filter counter upper limit (IOB1_X0)(B1)	Parameter	○	○
1000_3022H	iport_iob1_1_filcnt_upper	Input filter counter upper limit (IOB1_X1)(B1)	Parameter	○	○
1000_3024H	iport_iob1_2_filcnt_upper	Input filter counter upper limit (IOB1_X2)(B1)	Parameter	○	○
1000_3026H	iport_iob1_3_filcnt_upper	Input filter counter upper limit (IOB1_X3)(B1)	Parameter	○	○
1000_3028H	iport_iob1_4_filcnt_upper	Input filter counter upper limit (IOB1_X4)(B1)	Parameter	○	○
1000_302AH	iport_iob1_5_filcnt_upper	Input filter counter upper limit (IOB1_X5)(B1)	Parameter	○	○
1000_302CH	iport_iob1_6_filcnt_upper	Input filter counter upper limit (IOB1_X6)(B1)	Parameter	○	○
1000_302EH	iport_iob1_7_filcnt_upper	Input filter counter upper limit (IOB1_X7)(B1)	Parameter	○	○
1000_3030H	iport_iob1_8_filcnt_upper	Input filter counter upper limit (IOB1_X8)(B1)	Parameter	○	○
1000_3032H	iport_iob1_9_filcnt_upper	Input filter counter upper limit (IOB1_X9)(B1)	Parameter	○	○
1000_3034H	iport_iob1_a_filcnt_upper	Input filter counter upper limit (IOB1_XA)(B1)	Parameter	○	○
1000_3036H	iport_iob1_b_filcnt_upper	Input filter counter upper limit (IOB1_XB)(B1)	Parameter	○	○
1000_3038H	iport_iob1_c_filcnt_upper	Input filter counter upper limit (IOB1_XC)(B1)	Parameter	○	○
1000_303AH	iport_iob1_d_filcnt_upper	Input filter counter upper limit (IOB1_XD)(B1)	Parameter	○	○
1000_303CH	iport_iob1_e_filcnt_upper	Input filter counter upper limit (IOB1_XE)(B1)	Parameter	○	○
1000_303EH	iport_iob1_f_filcnt_upper	Input filter counter upper limit (IOB1_XF)(B1)	Parameter	○	○
1000_3040H	iport_iob2_0_filcnt_upper	Input filter counter upper limit (IOB2_X0)(B2)	Parameter	○	○
1000_3042H	iport_iob2_1_filcnt_upper	Input filter counter upper limit (IOB2_X1)(B2)	Parameter	○	○
1000_3044H	iport_iob2_2_filcnt_upper	Input filter counter upper limit (IOB2_X2)(B2)	Parameter	○	○
1000_3046H	iport_iob2_3_filcnt_upper	Input filter counter upper limit (IOB2_X3)(B2)	Parameter	○	○
1000_3048H	iport_iob2_4_filcnt_upper	Input filter counter upper limit (IOB2_X4)(B2)	Parameter	○	○
1000_304AH	iport_iob2_5_filcnt_upper	Input filter counter upper limit (IOB2_X5)(B2)	Parameter	○	○
1000_304CH	iport_iob2_6_filcnt_upper	Input filter counter upper limit (IOB2_X6)(B2)	Parameter	○	○
1000_304EH	iport_iob2_7_filcnt_upper	Input filter counter upper limit (IOB2_X7)(B2)	Parameter	○	○
1000_3050H	iport_iob2_8_filcnt_upper	Input filter counter upper limit (IOB2_X8)(B2)	Parameter	○	○
1000_3052H	iport_iob2_9_filcnt_upper	Input filter counter upper limit (IOB2_X9)(B2)	Parameter	○	○
1000_3054H	iport_iob2_a_filcnt_upper	Input filter counter upper limit (IOB2_XA)(B2)	Parameter	○	○
1000_3056H	iport_iob2_b_filcnt_upper	Input filter counter upper limit (IOB2_XB)(B2)	Parameter	○	○
1000_3058H	iport_iob2_c_filcnt_upper	Input filter counter upper limit (IOB2_XC)(B2)	Parameter	○	○
1000_305AH	iport_iob2_d_filcnt_upper	Input filter counter upper limit (IOB2_XD)(B2)	Parameter	○	○
1000_305CH	iport_iob2_e_filcnt_upper	Input filter counter upper limit (IOB2_XE)(B2)	Parameter	○	○
1000_305EH	iport_iob2_f_filcnt_upper	Input filter counter upper limit (IOB2_XF)(B2)	Parameter	○	○
1000_3060H	iport_ioe0_0_filcnt_upper	Input filter counter upper limit (IOE0_X0)(E0)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_3062H	iport_ioe0_1_filcnt_upper	Input filter counter upper limit (IOE0_X1)(E0)	Parameter	○	○
1000_3064H	iport_ioe0_2_filcnt_upper	Input filter counter upper limit (IOE0_X2)(E0)	Parameter	○	○
1000_3066H	iport_ioe0_3_filcnt_upper	Input filter counter upper limit (IOE0_X3)(E0)	Parameter	○	○
1000_3068H	iport_ioe0_4_filcnt_upper	Input filter counter upper limit (IOE0_X4)(E0)	Parameter	○	○
1000_306AH	iport_ioe0_5_filcnt_upper	Input filter counter upper limit (IOE0_X5)(E0)	Parameter	○	○
1000_306CH	iport_ioe0_6_filcnt_upper	Input filter counter upper limit (IOE0_X6)(E0)	Parameter	○	○
1000_306EH	iport_ioe0_7_filcnt_upper	Input filter counter upper limit (IOE0_X7)(E0)	Parameter	○	○
1000_3070H	iport_ioe0_8_filcnt_upper	Input filter counter upper limit (IOE0_X8)(E0)	Parameter	○	○
1000_3072H	iport_ioe0_9_filcnt_upper	Input filter counter upper limit (IOE0_X9)(E0)	Parameter	○	○
1000_3074H	iport_ioe0_a_filcnt_upper	Input filter counter upper limit (IOE0_XA)(E0)	Parameter	○	○
1000_3076H	iport_ioe0_b_filcnt_upper	Input filter counter upper limit (IOE0_XB)(E0)	Parameter	○	○
1000_3078H	iport_ioe0_c_filcnt_upper	Input filter counter upper limit (IOE0_XC)(E0)	Parameter	○	○
1000_307AH	iport_ioe0_d_filcnt_upper	Input filter counter upper limit (IOE0_XD)(E0)	Parameter	○	○
1000_307CH	iport_ioe0_e_filcnt_upper	Input filter counter upper limit (IOE0_XE)(E0)	Parameter	○	○
1000_307EH	iport_ioe0_f_filcnt_upper	Input filter counter upper limit (IOE0_XF)(E0)	Parameter	○	○
1000_3080H	iport_ioe1_0_filcnt_upper	Input filter counter upper limit (IOE1_X0)(E1)	Parameter	○	○
1000_3082H	iport_ioe1_1_filcnt_upper	Input filter counter upper limit (IOE1_X1)(E1)	Parameter	○	○
1000_3084H	iport_ioe1_2_filcnt_upper	Input filter counter upper limit (IOE1_X2)(E1)	Parameter	○	○
1000_3086H	iport_ioe1_3_filcnt_upper	Input filter counter upper limit (IOE1_X3)(E1)	Parameter	○	○
1000_3088H	iport_ioe1_4_filcnt_upper	Input filter counter upper limit (IOE1_X4)(E1)	Parameter	○	○
1000_308AH	iport_ioe1_5_filcnt_upper	Input filter counter upper limit (IOE1_X5)(E1)	Parameter	○	○
1000_308CH	iport_ioe1_6_filcnt_upper	Input filter counter upper limit (IOE1_X6)(E1)	Parameter	○	○
1000_308EH	iport_ioe1_7_filcnt_upper	Input filter counter upper limit (IOE1_X7)(E1)	Parameter	○	○
1000_3090H	iport_ioe1_8_filcnt_upper	Input filter counter upper limit (IOE1_X8)(E1)	Parameter	○	○
1000_3092H	iport_ioe1_9_filcnt_upper	Input filter counter upper limit (IOE1_X9)(E1)	Parameter	○	○
1000_3094H	iport_ioe1_a_filcnt_upper	Input filter counter upper limit (IOE1_XA)(E1)	Parameter	○	○
1000_3096H	iport_ioe1_b_filcnt_upper	Input filter counter upper limit (IOE1_XB)(E1)	Parameter	○	○
1000_3098H	iport_ioe1_c_filcnt_upper	Input filter counter upper limit (IOE1_XC)(E1)	Parameter	○	○
1000_309AH	iport_ioe1_d_filcnt_upper	Input filter counter upper limit (IOE1_XD)(E1)	Parameter	○	○
1000_309CH	iport_ioe1_e_filcnt_upper	Input filter counter upper limit (IOE1_XE)(E1)	Parameter	○	○
1000_309EH	iport_ioe1_f_filcnt_upper	Input filter counter upper limit (IOE1_XF)(E1)	Parameter	○	○
1000_30A0H	iport_ioe2_0_filcnt_upper	Input filter counter upper limit (IOE2_X0)(E2)	Parameter	○	○
1000_30A2H	iport_ioe2_1_filcnt_upper	Input filter counter upper limit (IOE2_X1)(E2)	Parameter	○	○
1000_30A4H	iport_ioe2_2_filcnt_upper	Input filter counter upper limit (IOE2_X2)(E2)	Parameter	○	○
1000_30A6H	iport_ioe2_3_filcnt_upper	Input filter counter upper limit (IOE2_X3)(E2)	Parameter	○	○
1000_30A8H	iport_ioe2_4_filcnt_upper	Input filter counter upper limit (IOE2_X4)(E2)	Parameter	○	○
1000_30AAH	iport_ioe2_5_filcnt_upper	Input filter counter upper limit (IOE2_X5)(E2)	Parameter	○	○
1000_30ACH	iport_ioe2_6_filcnt_upper	Input filter counter upper limit (IOE2_X6)(E2)	Parameter	○	○
1000_30AEH	iport_ioe2_7_filcnt_upper	Input filter counter upper limit (IOE2_X7)(E2)	Parameter	○	○
1000_30B0H	iport_ioe2_8_filcnt_upper	Input filter counter upper limit (IOE2_X8)(E2)	Parameter	○	○
1000_30B2H	iport_ioe2_9_filcnt_upper	Input filter counter upper limit (IOE2_X9)(E2)	Parameter	○	○
1000_30B4H	iport_ioe2_a_filcnt_upper	Input filter counter upper limit (IOE2_XA)(E2)	Parameter	○	○
1000_30B6H	iport_ioe2_b_filcnt_upper	Input filter counter upper limit (IOE2_XB)(E2)	Parameter	○	○
1000_30B8H	iport_ioe2_c_filcnt_upper	Input filter counter upper limit (IOE2_XC)(E2)	Parameter	○	○
1000_30BAH	iport_ioe2_d_filcnt_upper	Input filter counter upper limit (IOE2_XD)(E2)	Parameter	○	○
1000_30BCH	iport_ioe2_e_filcnt_upper	Input filter counter upper limit (IOE2_XE)(E2)	Parameter	○	○
1000_30BEH	iport_ioe2_f_filcnt_upper	Input filter counter upper limit (IOE2_XF)(E2)	Parameter	○	○
1000_3100H	iport_iob0x_monitor	Input signal monitor (B0)	Monitor	○	×
1000_3102H	iport_iob1x_monitor	Input signal monitor (B1)	Monitor	○	×
1000_3104H	iport_iob2x_monitor	Input signal monitor (B2)	Monitor	○	×
1000_3110H	iport_ioe0x_monitor	Input signal monitor (E0)	Monitor	○	×
1000_3112H	iport_ioe1x_monitor	Input signal monitor (E1)	Monitor	○	×

FPGA register address	Register name	Description	Type	Read	Write
1000_3114H	iport_ioe2x_monitor	Input signal monitor (E2)	Monitor	○	×

Digital output control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_4000H	oport_iob0y_osel	Output signal selection (B0)	Parameter	○	○
1000_4002H	oport_iob1y_osel	Output signal selection (B1)	Parameter	○	○
1000_4004H	oport_iob2y_osel	Output signal selection (B2)	Parameter	○	○
1000_4006H	Reserve				
1000_4008H	oport_ioe0y_osel	Output signal selection (E0)	Parameter	○	○
1000_400AH	oport_ioe1y_osel	Output signal selection (E1)	Parameter	○	○
1000_400CH	oport_ioe2y_osel	Output signal selection (E2)	Parameter	○	○
1000_4010H	oport_iob0y_odata	Output value setting (B0)	—	○	○
1000_4012H	oport_iob1y_odata	Output value setting (B1)	—	○	○
1000_4014H	oport_iob2y_odata	Output value setting (B2)	—	○	○
1000_4018H	oport_ioe0y_odata	Output value setting (E0)	—	○	○
1000_401AH	oport_ioe1y_odata	Output value setting (E1)	—	○	○
1000_401CH	oport_ioe2y_odata	Output value setting (E2)	—	○	○
1000_4020H	iport_iob0y_monitor	Output signal monitor (B0)	Monitor	○	×
1000_4022H	iport_iob1y_monitor	Output signal monitor (B1)	Monitor	○	×
1000_4024H	iport_iob2y_monitor	Output signal monitor (B2)	Monitor	○	×
1000_4030H	iport_ioe0y_monitor	Output signal monitor (E0)	Monitor	○	×
1000_4032H	iport_ioe1y_monitor	Output signal monitor (E1)	Monitor	○	×
1000_4034H	iport_ioe2y_monitor	Output signal monitor (E2)	Monitor	○	×
1000_4040H	oport_iob0y_holdclr	Differential output HOLD/CLEAR (B0)	Parameter	○	○
1000_4042H	oport_iob1y_holdclr	Differential output HOLD/CLEAR (B1)	Parameter	○	○
1000_4044H	oport_iob2y_holdclr	Differential output HOLD/CLEAR (B2)	Parameter	○	○
1000_4046H	oport_ioe0y_holdclr	Differential output HOLD/CLEAR (E0)	Parameter	○	○
1000_4048H	oport_ioe1y_holdclr	Differential output HOLD/CLEAR (E1)	Parameter	○	○
1000_404AH	oport_ioe2y_holdclr	Differential output HOLD/CLEAR (E2)	Parameter	○	○

Digital I/O control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_5000H	iport_iob0_dio485_filcnt_upper	Input filter counter upper limit (IOB0_DIO485_I)(B0)	Parameter	○	○
1000_5002H	iport_iob1_dio485_filcnt_upper	Input filter counter upper limit (IOB1_DIO485_I)(B1)	Parameter	○	○
1000_5004H	iport_iob2_dio485_filcnt_upper	Input filter counter upper limit (IOB2_DIO485_I)(B2)	Parameter	○	○
1000_5006H	Reserve				
1000_5008H	iport_ioe0_dio485_filcnt_upper	Input filter counter upper limit (IOE0_DIO485_I)(E0)	Parameter	○	○
1000_500AH	iport_ioe1_dio485_filcnt_upper	Input filter counter upper limit (IOE1_DIO485_I)(E1)	Parameter	○	○
1000_500CH	iport_ioe2_dio485_filcnt_upper	Input filter counter upper limit (IOE2_DIO485_I)(E2)	Parameter	○	○
1000_5010H	ioport_iob0_dio485_monitor	I/O signal monitor (IOB0_DIO485)(B0)	Monitor	○	×
1000_5012H	ioport_iob1_dio485_monitor	I/O signal monitor (IOB1_DIO485)(B1)	Monitor	○	×
1000_5014H	ioport_iob2_dio485_monitor	I/O signal monitor (IOB2_DIO485)(B2)	Monitor	○	×
1000_5018H	ioport_ioe0_dio485_monitor	I/O signal monitor (IOE0_DIO485)(E0)	Monitor	○	×
1000_501AH	ioport_ioe1_dio485_monitor	I/O signal monitor (IOE1_DIO485)(E1)	Monitor	○	×
1000_501CH	ioport_ioe2_dio485_monitor	I/O signal monitor (IOE2_DIO485)(E2)	Monitor	○	×
1000_5020H	ioport_iob0_dio485_osel	Output signal/Input output direction signal selection (B0)	Parameter	○	○
1000_5022H	ioport_iob1_dio485_osel	Output signal/Input output direction signal selection (B1)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_5024H	ioport_iob2_dio485_osel	Output signal/Input output direction signal selection (B2)	Parameter	○	○
1000_5026H	Reserve				
1000_5028H	ioport_ioe0_dio485_osel	Output signal/Input output direction signal selection (E0)	Parameter	○	○
1000_502AH	ioport_ioe1_dio485_osel	Output signal/Input output direction signal selection (E1)	Parameter	○	○
1000_502CH	ioport_ioe2_dio485_osel	Output signal/Input output direction signal selection (E2)	Parameter	○	○
1000_5030H	ioport_iob0_dio485_odata	Output value/Input output direction setting (B0)	—	○	○
1000_5032H	ioport_iob1_dio485_odata	Output value/Input output direction setting (B1)	—	○	○
1000_5034H	ioport_iob2_dio485_odata	Output value/Input output direction setting (B2)	—	○	○
1000_5038H	ioport_ioe0_dio485_odata	Output value/Input output direction setting (E0)	—	○	○
1000_503AH	ioport_ioe1_dio485_odata	Output value/Input output direction setting (E1)	—	○	○
1000_503CH	ioport_ioe2_dio485_odata	Output value/Input output direction setting (E2)	—	○	○
1000_5040H	ioport_iob0y_holdclr	Differential output HOLD/CLEAR (IOB0_DIO485_O) (B0)	Parameter	○	○
1000_5042H	ioport_iob1y_holdclr	Differential output HOLD/CLEAR (IOB1_DIO485_O) (B1)	Parameter	○	○
1000_5044H	ioport_iob2y_holdclr	Differential output HOLD/CLEAR (IOB2_DIO485_O) (B2)	Parameter	○	○
1000_5046H	ioport_ioe0y_holdclr	Differential output HOLD/CLEAR (IOE0_DIO485_O) (E0)	Parameter	○	○
1000_5048H	ioport_ioe1y_holdclr	Differential output HOLD/CLEAR (IOE1_DIO485_O) (E1)	Parameter	○	○
1000_504AH	ioport_ioe2y_holdclr	Differential output HOLD/CLEAR (IOE2_DIO485_O) (E2)	Parameter	○	○

Analog input control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_6000H	aiport_ad_start	A/D conversion enable/disable setting	Parameter	○	○
1000_6002H	aiport_ad_cyc_sel	A/D conversion timing selection	Parameter	○	○
1000_6008H	aiport_ade0_vi_set	ADC voltage/current input setting (E0)	—	○	○
1000_600AH	aiport_ade1_vi_set	ADC voltage/current input setting (E1)	—	○	○
1000_600CH	aiport_ade2_vi_set	ADC voltage/current input setting (E2)	—	○	○
1000_6010H	aiport_ade0_0_result	A/D conversion value CH0 (E0)	Monitor	○	×
1000_6012H	aiport_ade0_1_result	A/D conversion value CH1 (E0)	Monitor	○	×
1000_6014H	aiport_ade0_2_result	A/D conversion value CH2 (E0)	Monitor	○	×
1000_6016H	aiport_ade0_3_result	A/D conversion value CH3 (E0)	Monitor	○	×
1000_6018H	aiport_ade0_4_result	A/D conversion value CH4 (E0)	Monitor	○	×
1000_601AH	aiport_ade0_5_result	A/D conversion value CH5 (E0)	Monitor	○	×
1000_601CH	aiport_ade0_6_result	A/D conversion value CH6 (E0)	Monitor	○	×
1000_601EH	aiport_ade0_7_result	A/D conversion value CH7 (E0)	Monitor	○	×
1000_6020H	aiport_ade0_8_result	A/D conversion value CH8 (E0)	Monitor	○	×
1000_6022H	aiport_ade0_9_result	A/D conversion value CH9 (E0)	Monitor	○	×
1000_6024H	aiport_ade0_a_result	A/D conversion value CHA (E0)	Monitor	○	×
1000_6026H	aiport_ade0_b_result	A/D conversion value CHB (E0)	Monitor	○	×
1000_6030H	aiport_ade1_0_result	A/D conversion value CH0 (E1)	Monitor	○	×
1000_6032H	aiport_ade1_1_result	A/D conversion value CH1 (E1)	Monitor	○	×
1000_6034H	aiport_ade1_2_result	A/D conversion value CH2 (E1)	Monitor	○	×
1000_6036H	aiport_ade1_3_result	A/D conversion value CH3 (E1)	Monitor	○	×
1000_6038H	aiport_ade1_4_result	A/D conversion value CH4 (E1)	Monitor	○	×
1000_603AH	aiport_ade1_5_result	A/D conversion value CH5 (E1)	Monitor	○	×
1000_603CH	aiport_ade1_6_result	A/D conversion value CH6 (E1)	Monitor	○	×
1000_603EH	aiport_ade1_7_result	A/D conversion value CH7 (E1)	Monitor	○	×
1000_6040H	aiport_ade1_8_result	A/D conversion value CH8 (E1)	Monitor	○	×
1000_6042H	aiport_ade1_9_result	A/D conversion value CH9 (E1)	Monitor	○	×
1000_6044H	aiport_ade1_a_result	A/D conversion value CHA (E1)	Monitor	○	×
1000_6046H	aiport_ade1_b_result	A/D conversion value CHB (E1)	Monitor	○	×
1000_6050H	aiport_ade2_0_result	A/D conversion value CH0 (E2)	Monitor	○	×

FPGA register address	Register name	Description	Type	Read	Write
1000_6052H	aiport_ade2_1_result	A/D conversion value CH1 (E2)	Monitor	○	×
1000_6054H	aiport_ade2_2_result	A/D conversion value CH2 (E2)	Monitor	○	×
1000_6056H	aiport_ade2_3_result	A/D conversion value CH3 (E2)	Monitor	○	×
1000_6058H	aiport_ade2_4_result	A/D conversion value CH4 (E2)	Monitor	○	×
1000_605AH	aiport_ade2_5_result	A/D conversion value CH5 (E2)	Monitor	○	×
1000_605CH	aiport_ade2_6_result	A/D conversion value CH6 (E2)	Monitor	○	×
1000_605EH	aiport_ade2_7_result	A/D conversion value CH7 (E2)	Monitor	○	×
1000_6060H	aiport_ade2_8_result	A/D conversion value CH8 (E2)	Monitor	○	×
1000_6062H	aiport_ade2_9_result	A/D conversion value CH9 (E2)	Monitor	○	×
1000_6064H	aiport_ade2_a_result	A/D conversion value CHA (E2)	Monitor	○	×
1000_6066H	aiport_ade2_b_result	A/D conversion value CHB (E2)	Monitor	○	×
1000_6100H	aiport_ade0_0-3_range	ADC range setting CH0-3(E0)	Parameter	○	○
1000_6102H	aiport_ade0_4-7_range	ADC range setting CH4-7(E0)	Parameter	○	○
1000_6104H	aiport_ade0_8-b_range	ADC range setting CH8-B(E0)	Parameter	○	○
1000_6106H	aiport_ade1_0-3_range	ADC range setting CH0-3(E1)	Parameter	○	○
1000_6108H	aiport_ade1_4-7_range	ADC range setting CH4-7(E1)	Parameter	○	○
1000_610AH	aiport_ade1_8-b_range	ADC range setting CH8-B(E1)	Parameter	○	○
1000_610CH	aiport_ade2_0-3_range	ADC range setting CH0-3(E2)	Parameter	○	○
1000_610EH	aiport_ade2_4-7_range	ADC range setting CH4-7(E2)	Parameter	○	○
1000_6110H	aiport_ade2_8-b_range	ADC range setting CH8-B(E2)	Parameter	○	○
1000_6112H to 1000_611EH	Reserve				
1000_6120H	aiport_ade0_oversamp	ADC oversampling ratio setting (E0)	Parameter	○	○
1000_6122H	aiport_ade1_oversamp	ADC oversampling ratio setting (E1)	Parameter	○	○
1000_6124H	aiport_ade2_oversamp	ADC oversampling ratio setting (E2)	Parameter	○	○
1000_6160H	aiport_ade0_0-1_offset	ADC offset value CH0-1 (E0)	Parameter	○	○
1000_6162H	aiport_ade0_2-3_offset	ADC offset value CH2-3 (E0)	Parameter	○	○
1000_6164H	aiport_ade0_4-5_offset	ADC offset value CH4-5 (E0)	Parameter	○	○
1000_6166H	aiport_ade0_6-7_offset	ADC offset value CH6-7 (E0)	Parameter	○	○
1000_6168H	aiport_ade0_8-9_offset	ADC offset value CH8-9 (E0)	Parameter	○	○
1000_616AH	aiport_ade0_a-b_offset	ADC offset value CHA-B (E0)	Parameter	○	○
1000_616CH	aiport_ade1_0-1_offset	ADC offset value CH0-1 (E1)	Parameter	○	○
1000_616EH	aiport_ade1_2-3_offset	ADC offset value CH2-3 (E1)	Parameter	○	○
1000_6170H	aiport_ade1_4-5_offset	ADC offset value CH4-5 (E1)	Parameter	○	○
1000_6172H	aiport_ade1_6-7_offset	ADC offset value CH6-7 (E1)	Parameter	○	○
1000_6174H	aiport_ade1_8-9_offset	ADC offset value CH8-9 (E1)	Parameter	○	○
1000_6176H	aiport_ade1_a-b_offset	ADC offset value CHA-B (E1)	Parameter	○	○
1000_6178H	aiport_ade2_0-1_offset	ADC offset value CH0-1 (E2)	Parameter	○	○
1000_617AH	aiport_ade2_2-3_offset	ADC offset value CH2-3 (E2)	Parameter	○	○
1000_617CH	aiport_ade2_4-5_offset	ADC offset value CH4-5 (E2)	Parameter	○	○
1000_617EH	aiport_ade2_6-7_offset	ADC offset value CH6-7 (E2)	Parameter	○	○
1000_6180H	aiport_ade2_8-9_offset	ADC offset value CH8-9 (E2)	Parameter	○	○
1000_6182H	aiport_ade2_a-b_offset	ADC offset value CHA-B (E2)	Parameter	○	○

Analog output control part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_7000H	aoport_da_start	D/A conversion enable/disable setting	Parameter	○	○
1000_7002H	aoport_da_data_sel	D/A conversion value selection	Parameter	○	○
1000_7004H	aoport_da_cyc_sel	D/A conversion timing selection	Parameter	○	○
1000_7006H	aoport_da_ldac_sel	DAC LDAC signal selection	Parameter	○	○
1000_7100H	aoport_dae0_0_data	D/A conversion value CH0 (E0)	Control	○	○
1000_7102H	aoport_dae0_1_data	D/A conversion value CH1 (E0)	Control	○	○
1000_7104H	aoport_dae1_0_data	D/A conversion value CH0 (E1)	Control	○	○
1000_7106H	aoport_dae1_1_data	D/A conversion value CH1 (E1)	Control	○	○
1000_7108H	aoport_dae2_0_data	D/A conversion value CH0 (E2)	Control	○	○
1000_710AH	aoport_dae2_1_data	D/A conversion value CH1 (E2)	Control	○	○

Logging part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_9000H	lgdw_ctrl	Logging operation control register	—	○	○
1000_9002H	lgdw_sts	Logging state register	Monitor	○	×
1000_9004H	lgdw_sys_sts	Logging system flag	Monitor	○	×
1000_9006H	lgdw_flag_clr	Flag clear register	—	○	○
1000_9008H	lgdw_area	Logging data size setting	Parameter	○	○
1000_9030H	lgdw_clock_rddata1	Time information (year)	Monitor	○	×
1000_9032H	lgdw_clock_rddata2	Time information (month, day, hour)	Monitor	○	×
1000_9034H	lgdw_clock_rddata3	Time information (minute, second)	Monitor	○	×
1000_9036H	lgdw_clock_rddata4	Time information (ms)	Monitor	○	×
1000_9038H	lgdw_clock_rddata5	Time information (μs)	Monitor	○	×
1001_9000H	lgdw_triggered_lsample	Set number of sampling after trigger (lower side)	Parameter	○	○
1001_9002H	lgdw_triggered_usample	Set number of sampling after trigger (upper side)	Parameter	○	○
1001_9004H	lgdw_sample_lcount	Number of samplings (lower)	Monitor	○	×
1001_9006H	lgdw_sample_ucount	Number of samplings (upper)	Monitor	○	×

User circuit part

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_A000H	usr_wrdat_ctrl	Write/read data control register	—	○	○
1000_A002H	usr_logmode_sel	User circuit logging mode selection	Parameter	○	○
1000_A004H	usr_micon_syserr	MCU system error notification	—	○	○
1000_A010H to 1000_A02EH	usr_alwreg_00 to usr_alwreg_0f	Always write register	Control	○	○
1000_A030H to 1000_A04EH	usr_alrreg_00 to usr_alrreg_0f	Always read register	Monitor	○	×
1000_B000H to 1000_B2FEH	usr_wreg_000 to usr_wreg_17f	Write data (transient area)	Control/ parameter		
1000_B300H to 1000_B3FEH	usr_wreg_180 to usr_wreg_1ff	Write data (cyclic area)	Control	○	○
1000_B800H to 1000_BAFEH	usr_rreg_000 to usr_rreg_17f	Read data (transient area)	Monitor	○	×
1000_BB00H to 1000_BBFEH	usr_rreg_180 to usr_rreg_1ff	Read data (cyclic area)	Monitor	○	×

User circuit part register (Write data)

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_B000H	usr_wreg_000	Digital control part enable/disable control register (IOB0_X0 B0)	Parameter	○	○
1000_B002H	usr_wreg_001	Digital control part enable/disable control register (IOB0_X1 B0)	Parameter	○	○
1000_B004H	usr_wreg_002	Digital control part enable/disable control register (IOB0_X2 B0)	Parameter	○	○
1000_B006H	usr_wreg_003	Digital control part enable/disable control register (IOB0_X3 B0)	Parameter	○	○
1000_B008H	usr_wreg_004	Digital control part enable/disable control register (IOB0_X4 B0)	Parameter	○	○
1000_B00AH	usr_wreg_005	Digital control part enable/disable control register (IOB0_X5 B0)	Parameter	○	○
1000_B00CH	usr_wreg_006	Digital control part enable/disable control register (IOB0_X6 B0)	Parameter	○	○
1000_B00EH	usr_wreg_007	Digital control part enable/disable control register (IOB0_X7 B0)	Parameter	○	○
1000_B010H	usr_wreg_008	Digital control part enable/disable control register (IOB0_X8 B0)	Parameter	○	○
1000_B012H	usr_wreg_009	Digital control part enable/disable control register (IOB0_X9 B0)	Parameter	○	○
1000_B014H	usr_wreg_00A	Digital control part enable/disable control register (IOB0_XA B0)	Parameter	○	○
1000_B016H	usr_wreg_00B	Digital control part enable/disable control register (IOB0_XB B0)	Parameter	○	○
1000_B018H	usr_wreg_00C	Digital control part enable/disable control register (IOB0_XC B0)	Parameter	○	○
1000_B01AH	usr_wreg_00D	Digital control part enable/disable control register (IOB0_XD B0)	Parameter	○	○
1000_B01CH	usr_wreg_00E	Digital control part enable/disable control register (IOB0_XE B0)	Parameter	○	○
1000_B01EH	usr_wreg_00F	Digital control part enable/disable control register (IOB0_XF B0)	Parameter	○	○
1000_B028H	usr_wreg_014	Digital control part enable/disable control register (IOB1_X0 B1)	Parameter	○	○
1000_B02AH	usr_wreg_015	Digital control part enable/disable control register (IOB1_X1 B1)	Parameter	○	○
1000_B02CH	usr_wreg_016	Digital control part enable/disable control register (IOB1_X2 B1)	Parameter	○	○
1000_B02EH	usr_wreg_017	Digital control part enable/disable control register (IOB1_X3 B1)	Parameter	○	○
1000_B030H	usr_wreg_018	Digital control part enable/disable control register (IOB1_X4 B1)	Parameter	○	○
1000_B032H	usr_wreg_019	Digital control part enable/disable control register (IOB1_X5 B1)	Parameter	○	○
1000_B034H	usr_wreg_01A	Digital control part enable/disable control register (IOB1_X6 B1)	Parameter	○	○
1000_B036H	usr_wreg_01B	Digital control part enable/disable control register (IOB1_X7 B1)	Parameter	○	○
1000_B038H	usr_wreg_01C	Digital control part enable/disable control register (IOB1_X8 B1)	Parameter	○	○
1000_B03AH	usr_wreg_01D	Digital control part enable/disable control register (IOB1_X9 B1)	Parameter	○	○
1000_B03CH	usr_wreg_01E	Digital control part enable/disable control register (IOB1_XA B1)	Parameter	○	○
1000_B03EH	usr_wreg_01F	Digital control part enable/disable control register (IOB1_XB B1)	Parameter	○	○
1000_B040H	usr_wreg_020	Digital control part enable/disable control register (IOB1_XC B1)	Parameter	○	○
1000_B042H	usr_wreg_021	Digital control part enable/disable control register (IOB1_XD B1)	Parameter	○	○
1000_B044H	usr_wreg_022	Digital control part enable/disable control register (IOB1_XE B1)	Parameter	○	○
1000_B046H	usr_wreg_023	Digital control part enable/disable control register (IOB1_XF B1)	Parameter	○	○
1000_B050H	usr_wreg_028	Digital control part enable/disable control register (IOB2_X0 B2)	Parameter	○	○
1000_B052H	usr_wreg_029	Digital control part enable/disable control register (IOB2_X1 B2)	Parameter	○	○
1000_B054H	usr_wreg_02A	Digital control part enable/disable control register (IOB2_X2 B2)	Parameter	○	○
1000_B056H	usr_wreg_02B	Digital control part enable/disable control register (IOB2_X3 B2)	Parameter	○	○
1000_B058H	usr_wreg_02C	Digital control part enable/disable control register (IOB2_X4 B2)	Parameter	○	○
1000_B05AH	usr_wreg_02D	Digital control part enable/disable control register (IOB2_X5 B2)	Parameter	○	○
1000_B05CH	usr_wreg_02E	Digital control part enable/disable control register (IOB2_X6 B2)	Parameter	○	○
1000_B05EH	usr_wreg_02F	Digital control part enable/disable control register (IOB2_X7 B2)	Parameter	○	○
1000_B060H	usr_wreg_030	Digital control part enable/disable control register (IOB2_X8 B2)	Parameter	○	○
1000_B062H	usr_wreg_031	Digital control part enable/disable control register (IOB2_X9 B2)	Parameter	○	○
1000_B064H	usr_wreg_032	Digital control part enable/disable control register (IOB2_XA B2)	Parameter	○	○
1000_B066H	usr_wreg_033	Digital control part enable/disable control register (IOB2_XB B2)	Parameter	○	○
1000_B068H	usr_wreg_034	Digital control part enable/disable control register (IOB2_XC B2)	Parameter	○	○
1000_B06AH	usr_wreg_035	Digital control part enable/disable control register (IOB2_XD B2)	Parameter	○	○
1000_B06CH	usr_wreg_036	Digital control part enable/disable control register (IOB2_XE B2)	Parameter	○	○
1000_B06EH	usr_wreg_037	Digital control part enable/disable control register (IOB2_XF B2)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B078H	usr_wreg_03C	Digital control part enable/disable control register (IOE0_X0 E0)	Parameter	○	○
1000_B07AH	usr_wreg_03D	Digital control part enable/disable control register (IOE0_X1 E0)	Parameter	○	○
1000_B07CH	usr_wreg_03E	Digital control part enable/disable control register (IOE0_X2 E0)	Parameter	○	○
1000_B07EH	usr_wreg_03F	Digital control part enable/disable control register (IOE0_X3 E0)	Parameter	○	○
1000_B080H	usr_wreg_040	Digital control part enable/disable control register (IOE0_X4 E0)	Parameter	○	○
1000_B082H	usr_wreg_041	Digital control part enable/disable control register (IOE0_X5 E0)	Parameter	○	○
1000_B084H	usr_wreg_042	Digital control part enable/disable control register (IOE0_X6 E0)	Parameter	○	○
1000_B086H	usr_wreg_043	Digital control part enable/disable control register (IOE0_X7 E0)	Parameter	○	○
1000_B088H	usr_wreg_044	Digital control part enable/disable control register (IOE0_X8 E0)	Parameter	○	○
1000_B08AH	usr_wreg_045	Digital control part enable/disable control register (IOE0_X9 E0)	Parameter	○	○
1000_B08CH	usr_wreg_046	Digital control part enable/disable control register (IOE0_XA E0)	Parameter	○	○
1000_B08EH	usr_wreg_047	Digital control part enable/disable control register (IOE0_XB E0)	Parameter	○	○
1000_B090H	usr_wreg_048	Digital control part enable/disable control register (IOE0_XC E0)	Parameter	○	○
1000_B092H	usr_wreg_049	Digital control part enable/disable control register (IOE0_XD E0)	Parameter	○	○
1000_B094H	usr_wreg_04A	Digital control part enable/disable control register (IOE0_XE E0)	Parameter	○	○
1000_B096H	usr_wreg_04B	Digital control part enable/disable control register (IOE0_XF E0)	Parameter	○	○
1000_B0A0H	usr_wreg_050	Digital control part enable/disable control register (IOE1_X0 E1)	Parameter	○	○
1000_B0A2H	usr_wreg_051	Digital control part enable/disable control register (IOE1_X1 E1)	Parameter	○	○
1000_B0A4H	usr_wreg_052	Digital control part enable/disable control register (IOE1_X2 E1)	Parameter	○	○
1000_B0A6H	usr_wreg_053	Digital control part enable/disable control register (IOE1_X3 E1)	Parameter	○	○
1000_B0A8H	usr_wreg_054	Digital control part enable/disable control register (IOE1_X4 E1)	Parameter	○	○
1000_B0AAH	usr_wreg_055	Digital control part enable/disable control register (IOE1_X5 E1)	Parameter	○	○
1000_B0ACH	usr_wreg_056	Digital control part enable/disable control register (IOE1_X6 E1)	Parameter	○	○
1000_B0AEH	usr_wreg_057	Digital control part enable/disable control register (IOE1_X7 E1)	Parameter	○	○
1000_B0B0H	usr_wreg_058	Digital control part enable/disable control register (IOE1_X8 E1)	Parameter	○	○
1000_B0B2H	usr_wreg_059	Digital control part enable/disable control register (IOE1_X9 E1)	Parameter	○	○
1000_B0B4H	usr_wreg_05A	Digital control part enable/disable control register (IOE1_XA E1)	Parameter	○	○
1000_B0B6H	usr_wreg_05B	Digital control part enable/disable control register (IOE1_XB E1)	Parameter	○	○
1000_B0B8H	usr_wreg_05C	Digital control part enable/disable control register (IOE1_XC E1)	Parameter	○	○
1000_B0BAH	usr_wreg_05D	Digital control part enable/disable control register (IOE1_XD E1)	Parameter	○	○
1000_B0BCH	usr_wreg_05E	Digital control part enable/disable control register (IOE1_XE E1)	Parameter	○	○
1000_B0BEH	usr_wreg_05F	Digital control part enable/disable control register (IOE1_XF E1)	Parameter	○	○
1000_B0C8H	usr_wreg_064	Digital control part enable/disable control register (IOE2_X0 E2)	Parameter	○	○
1000_B0CAH	usr_wreg_065	Digital control part enable/disable control register (IOE2_X1 E2)	Parameter	○	○
1000_B0CCH	usr_wreg_066	Digital control part enable/disable control register (IOE2_X2 E2)	Parameter	○	○
1000_B0CEH	usr_wreg_067	Digital control part enable/disable control register (IOE2_X3 E2)	Parameter	○	○
1000_B0D0H	usr_wreg_068	Digital control part enable/disable control register (IOE2_X4 E2)	Parameter	○	○
1000_B0D2H	usr_wreg_069	Digital control part enable/disable control register (IOE2_X5 E2)	Parameter	○	○
1000_B0D4H	usr_wreg_06A	Digital control part enable/disable control register (IOE2_X6 E2)	Parameter	○	○
1000_B0D6H	usr_wreg_06B	Digital control part enable/disable control register (IOE2_X7 E2)	Parameter	○	○
1000_B0D8H	usr_wreg_06C	Digital control part enable/disable control register (IOE2_X8 E2)	Parameter	○	○
1000_B0DAH	usr_wreg_06D	Digital control part enable/disable control register (IOE2_X9 E2)	Parameter	○	○
1000_B0DCH	usr_wreg_06E	Digital control part enable/disable control register (IOE2_XA E2)	Parameter	○	○
1000_B0DEH	usr_wreg_06F	Digital control part enable/disable control register (IOE2_XB E2)	Parameter	○	○
1000_B0E0H	usr_wreg_070	Digital control part enable/disable control register (IOE2_XC E2)	Parameter	○	○
1000_B0E2H	usr_wreg_071	Digital control part enable/disable control register (IOE2_XD E2)	Parameter	○	○
1000_B0E4H	usr_wreg_072	Digital control part enable/disable control register (IOE2_XE E2)	Parameter	○	○
1000_B0E6H	usr_wreg_073	Digital control part enable/disable control register (IOE2_XF E2)	Parameter	○	○
1000_B0F0H	usr_wreg_078	Digital output control digital output selection (B0)	Parameter	○	○
1000_B0F2H	usr_wreg_079	Digital output control digital output selection (B1)	Parameter	○	○
1000_B0F4H	usr_wreg_07A	Digital output control digital output selection (B2)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B0F6H	usr_wreg_07B	Digital output control digital output selection (E0)	Parameter	○	○
1000_B0F8H	usr_wreg_07C	Digital output control digital output selection (E1)	Parameter	○	○
1000_B0FAH	usr_wreg_07D	Digital output control digital output selection (E2)	Parameter	○	○
1000_B100H	usr_wreg_080	Digital I/O control I/O control register (B0)	Parameter	○	○
1000_B102H	usr_wreg_081	Digital I/O control I/O control register (B1)	Parameter	○	○
1000_B104H	usr_wreg_082	Digital I/O control I/O control register (B2)	Parameter	○	○
1000_B106H	usr_wreg_083	Digital I/O control I/O control register (E0)	Parameter	○	○
1000_B108H	usr_wreg_084	Digital I/O control I/O control register (E1)	Parameter	○	○
1000_B10AH	usr_wreg_085	Digital I/O control I/O control register (E2)	Parameter	○	○
1000_B10CH	usr_wreg_086	Digital I/O control digital output selection	Parameter	○	○
1000_B110H	usr_wreg_088	Digital output HOLD/CLEAR	Parameter	○	○
1000_B122H	usr_wreg_091	Logging control part logging enable signal selection	Parameter	○	○
1000_B124H	usr_wreg_092	Logging control part end trigger signal selection	Parameter	○	○
1000_B126H	usr_wreg_093	Logging control part sampling pulse signal selection	Parameter	○	○
1000_B128H	usr_wreg_094	Logging control part logging enable mode setting	Parameter	○	○
1000_B12AH	usr_wreg_095	Logging control part automatic transfer mode setting	Parameter	○	○
1000_B146H	usr_wreg_0A3	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (lower side) (B0)	Parameter	○	○
1000_B148H	usr_wreg_0A4	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value (upper side) (B0)	Parameter	○	○
1000_B14AH	usr_wreg_0A5	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0)	Parameter/ Control	○	○
1000_B156H	usr_wreg_0AB	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (B1)	Parameter	○	○
1000_B158H	usr_wreg_0AC	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (B1)	Parameter	○	○
1000_B15AH	usr_wreg_0AD	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1)	Parameter/ Control	○	○
1000_B166H	usr_wreg_0B3	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (B2)	Parameter	○	○
1000_B168H	usr_wreg_0B4	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (B2)	Parameter	○	○
1000_B16AH	usr_wreg_0B5	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2)	Parameter/ Control	○	○
1000_B176H	usr_wreg_0BB	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E0)	Parameter	○	○
1000_B178H	usr_wreg_0BC	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E0)	Parameter	○	○
1000_B17AH	usr_wreg_0BD	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0)	Parameter/ Control	○	○
1000_B186H	usr_wreg_0C3	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E1)	Parameter	○	○
1000_B188H	usr_wreg_0C4	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E1)	Parameter	○	○
1000_B18AH	usr_wreg_0C5	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1)	Parameter/ Control	○	○
1000_B196H	usr_wreg_0CB	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E2)	Parameter	○	○
1000_B198H	usr_wreg_0CC	Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E2)	Parameter	○	○
1000_B19AH	usr_wreg_0CD	Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2)	Parameter/ Control	○	○
1000_B1A6H	usr_wreg_0D3	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B0)	Parameter	○	○
1000_B1A8H	usr_wreg_0D4	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B0)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B1AAH	usr_wreg_0D5	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0)	Parameter/ Control	○	○
1000_B1B6H	usr_wreg_0DB	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B1)	Parameter	○	○
1000_B1B8H	usr_wreg_0DC	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B1)	Parameter	○	○
1000_B1BAH	usr_wreg_0DD	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1)	Parameter/ Control	○	○
1000_B1C6H	usr_wreg_0E3	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B2)	Parameter	○	○
1000_B1C8H	usr_wreg_0E4	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B2)	Parameter	○	○
1000_B1CAH	usr_wreg_0E5	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2)	Parameter/ Control	○	○
1000_B1D6H	usr_wreg_0EB	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E0)	Parameter	○	○
1000_B1D8H	usr_wreg_0EC	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E0)	Parameter	○	○
1000_B1DAH	usr_wreg_0ED	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0)	Parameter/ Control	○	○
1000_B1E6H	usr_wreg_0F3	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E1)	Parameter	○	○
1000_B1E8H	usr_wreg_0F4	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E1)	Parameter	○	○
1000_B1EAH	usr_wreg_0F5	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1)	Parameter/ Control	○	○
1000_B1F6H	usr_wreg_0FB	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E2)	Parameter	○	○
1000_B1F8H	usr_wreg_0FC	Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E2)	Parameter	○	○
1000_B1FAH	usr_wreg_0FD	Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2)	Parameter/ Control	○	○
1000_B220H	usr_wreg_110	Pulse output part pulse width upper limit value (lower side) (B0)	Parameter	○	○
1000_B222H	usr_wreg_111	Pulse output part pulse width upper limit value (upper side) (B0)	Parameter	○	○
1000_B224H	usr_wreg_112	Pulse output part output pulse count upper limit value (lower side) (B0)	Parameter	○	○
1000_B226H	usr_wreg_113	Pulse output part output pulse count upper limit value (upper side) (B0)	Parameter	○	○
1000_B22AH	usr_wreg_115	Pulse output part pulse width upper limit value (lower side) (B1)	Parameter	○	○
1000_B22CH	usr_wreg_116	Pulse output part pulse width upper limit value (upper side) (B1)	Parameter	○	○
1000_B22EH	usr_wreg_117	Pulse output part output pulse count upper limit value (lower side) (B1)	Parameter	○	○
1000_B230H	usr_wreg_118	Pulse output part output pulse count upper limit value (upper side) (B1)	Parameter	○	○
1000_B234H	usr_wreg_11A	Pulse output part pulse width upper limit value (lower side) (B2)	Parameter	○	○
1000_B236H	usr_wreg_11B	Pulse output part pulse width upper limit value (upper side) (B2)	Parameter	○	○
1000_B238H	usr_wreg_11C	Pulse output part output pulse count upper limit value (lower side) (B2)	Parameter	○	○
1000_B23AH	usr_wreg_11D	Pulse output part output pulse count upper limit value (upper side) (B2)	Parameter	○	○
1000_B23EH	usr_wreg_11F	Pulse output part pulse width upper limit value (lower side) (E0)	Parameter	○	○
1000_B240H	usr_wreg_120	Pulse output part pulse width upper limit value (upper side) (E0)	Parameter	○	○
1000_B242H	usr_wreg_121	Pulse output part output pulse count upper limit value (lower side) (E0)	Parameter	○	○
1000_B244H	usr_wreg_122	Pulse output part output pulse count upper limit value (upper side) (E0)	Parameter	○	○
1000_B248H	usr_wreg_124	Pulse output part pulse width upper limit value (lower side) (E1)	Parameter	○	○
1000_B24AH	usr_wreg_125	Pulse output part pulse width upper limit value (upper side) (E1)	Parameter	○	○
1000_B24CH	usr_wreg_126	Pulse output part output pulse count upper limit value (lower side) (E1)	Parameter	○	○
1000_B24EH	usr_wreg_127	Pulse output part output pulse count upper limit value (upper side) (E1)	Parameter	○	○
1000_B252H	usr_wreg_129	Pulse output part pulse width upper limit value (lower side) (E2)	Parameter	○	○
1000_B254H	usr_wreg_12A	Pulse output part pulse width upper limit value (upper side) (E2)	Parameter	○	○
1000_B256H	usr_wreg_12B	Pulse output part output pulse count upper limit value (lower side) (E2)	Parameter	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B258H	usr_wreg_12C	Pulse output part output pulse count upper limit value (upper side) (E2)	Parameter	○	○
1000_B260H	usr_wreg_130	Pulse output part pulse output selection 0 (B0)	Parameter	○	○
1000_B262H	usr_wreg_131	Pulse output part pulse output selection 1 (B0)	Parameter	○	○
1000_B264H	usr_wreg_132	Pulse output part pulse output selection 2 (B0)	Parameter	○	○
1000_B266H	usr_wreg_133	Pulse output part pulse output selection 0 (B1)	Parameter	○	○
1000_B268H	usr_wreg_134	Pulse output part pulse output selection 1 (B1)	Parameter	○	○
1000_B26AH	usr_wreg_135	Pulse output part pulse output selection 2 (B1)	Parameter	○	○
1000_B26CH	usr_wreg_136	Pulse output part pulse output selection 0 (B2)	Parameter	○	○
1000_B26EH	usr_wreg_137	Pulse output part pulse output selection 1 (B2)	Parameter	○	○
1000_B270H	usr_wreg_138	Pulse output part pulse output selection 2 (B2)	Parameter	○	○
1000_B272H	usr_wreg_139	Pulse output part pulse output selection 0 (E0)	Parameter	○	○
1000_B274H	usr_wreg_13A	Pulse output part pulse output selection 1 (E0)	Parameter	○	○
1000_B276H	usr_wreg_13B	Pulse output part pulse output selection 2 (E0)	Parameter	○	○
1000_B278H	usr_wreg_13C	Pulse output part pulse output selection 0 (E1)	Parameter	○	○
1000_B27AH	usr_wreg_13D	Pulse output part pulse output selection 1 (E1)	Parameter	○	○
1000_B27CH	usr_wreg_13E	Pulse output part pulse output selection 2 (E1)	Parameter	○	○
1000_B27EH	usr_wreg_13F	Pulse output part pulse output selection 0 (E2)	Parameter	○	○
1000_B280H	usr_wreg_140	Pulse output part pulse output selection 1 (E2)	Parameter	○	○
1000_B282H	usr_wreg_141	Pulse output part pulse output selection 2 (E2)	Parameter	○	○
1000_B284H	usr_wreg_142	Pulse output part pulse output mask 0 (B0)	Parameter	○	○
1000_B286H	usr_wreg_143	Pulse output part pulse output mask 1 (B0)	Parameter	○	○
1000_B288H	usr_wreg_144	Pulse output part pulse output mask 0 (B1)	Parameter	○	○
1000_B28AH	usr_wreg_145	Pulse output part pulse output mask 1 (B1)	Parameter	○	○
1000_B28CH	usr_wreg_146	Pulse output part pulse output mask 0 (B2)	Parameter	○	○
1000_B28EH	usr_wreg_147	Pulse output part pulse output mask 1 (B2)	Parameter	○	○
1000_B290H	usr_wreg_148	Pulse output part pulse output mask 0 (E0)	Parameter	○	○
1000_B292H	usr_wreg_149	Pulse output part pulse output mask 1 (E0)	Parameter	○	○
1000_B294H	usr_wreg_14A	Pulse output part pulse output mask 0 (E1)	Parameter	○	○
1000_B296H	usr_wreg_14B	Pulse output part pulse output mask 1 (E1)	Parameter	○	○
1000_B298H	usr_wreg_14C	Pulse output part pulse output mask 0 (E2)	Parameter	○	○
1000_B29AH	usr_wreg_14D	Pulse output part pulse output mask 1 (E2)	Parameter	○	○
1000_B2C0H	usr_wreg_160	Analog output part LDAC output selection	Parameter	○	○
1000_B2D0H	usr_wreg_168	Analog output part HOLD/CLEAR	Parameter	○	○
1000_B2FEH	usr_wreg_17F	Test mode setting	Parameter	○	○
1000_B300H	usr_wreg_180	Logging control part user logging control	Control	○	○
1000_B302H	usr_wreg_181	Logging control part 1 enable clear	Control	○	○
1000_B310H	usr_wreg_188	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B0)	Control	○	○
1000_B312H	usr_wreg_189	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0)	Control	○	○
1000_B314H	usr_wreg_18A	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0)	Control	○	○
1000_B316H	usr_wreg_18B	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B1)	Control	○	○
1000_B318H	usr_wreg_18C	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B1)	Control	○	○
1000_B31AH	usr_wreg_18D	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B1)	Control	○	○
1000_B31CH	usr_wreg_18E	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B2)	Control	○	○
1000_B31EH	usr_wreg_18F	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B2)	Control	○	○
1000_B320H	usr_wreg_190	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B2)	Control	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B322H	usr_wreg_191	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E0)	Control	○	○
1000_B324H	usr_wreg_192	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E0)	Control	○	○
1000_B326H	usr_wreg_193	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E0)	Control	○	○
1000_B328H	usr_wreg_194	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E1)	Control	○	○
1000_B32AH	usr_wreg_195	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E1)	Control	○	○
1000_B32CH	usr_wreg_196	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E1)	Control	○	○
1000_B32EH	usr_wreg_197	Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E2)	Control	○	○
1000_B330H	usr_wreg_198	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E2)	Control	○	○
1000_B332H	usr_wreg_199	Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E2)	Control	○	○
1000_B340H	usr_wreg_1A0	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B0)	Control	○	○
1000_B342H	usr_wreg_1A1	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B0)	Control	○	○
1000_B344H	usr_wreg_1A2	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B0)	Control	○	○
1000_B346H	usr_wreg_1A3	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B1)	Control	○	○
1000_B348H	usr_wreg_1A4	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B1)	Control	○	○
1000_B34AH	usr_wreg_1A5	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B1)	Control	○	○
1000_B34CH	usr_wreg_1A6	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B2)	Control	○	○
1000_B34EH	usr_wreg_1A7	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B2)	Control	○	○
1000_B350H	usr_wreg_1A8	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B2)	Control	○	○
1000_B352H	usr_wreg_1A9	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E0)	Control	○	○
1000_B354H	usr_wreg_1AA	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E0)	Control	○	○
1000_B356H	usr_wreg_1AB	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E0)	Control	○	○
1000_B358H	usr_wreg_1AC	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E1)	Control	○	○
1000_B35AH	usr_wreg_1AD	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E1)	Control	○	○
1000_B35CH	usr_wreg_1AE	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E1)	Control	○	○
1000_B35EH	usr_wreg_1AF	Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E2)	Control	○	○
1000_B360H	usr_wreg_1B0	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E2)	Control	○	○
1000_B362H	usr_wreg_1B1	Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E2)	Control	○	○
1000_B370H	usr_wreg_1B8	Pulse output part pulse output enable (B0)	Control	○	○
1000_B372H	usr_wreg_1B9	Pulse output part pulse output enable (B1)	Control	○	○
1000_B374H	usr_wreg_1BA	Pulse output part pulse output enable (B2)	Control	○	○
1000_B376H	usr_wreg_1BB	Pulse output part pulse output enable (E0)	Control	○	○

FPGA register address	Register name	Description	Type	Read	Write
1000_B378H	usr_wreg_1BC	Pulse output part pulse output enable (E1)	Control	○	○
1000_B37AH	usr_wreg_1BD	Pulse output part pulse output enable (E2)	Control	○	○
1000_B380H	usr_wreg_1C0	Analog output part D/A conversion value CH0 (E0)	Control	○	○
1000_B382H	usr_wreg_1C1	Analog output part D/A conversion value CH1 (E0)	Control	○	○
1000_B384H	usr_wreg_1C2	Analog output part D/A conversion value CH0 (E1)	Control	○	○
1000_B386H	usr_wreg_1C3	Analog output part D/A conversion value CH1 (E1)	Control	○	○
1000_B388H	usr_wreg_1C4	Analog output part D/A conversion value CH0 (E2)	Control	○	○
1000_B38AH	usr_wreg_1C5	Analog output part D/A conversion value CH1 (E2)	Control	○	○
1000_B38CH	usr_wreg_1C6	Analog output part D/A conversion value enable	Control	○	○
1000_B390H	usr_wreg_1C8	Analog control data sampling pulse generation	Control	○	○
1000_B3A0H	usr_wreg_1D0	User circuit part error signal generation	Control	○	○
1000_B3B0H	usr_wreg_1D8	A/D conversion value maximum/minimum value selection	Control	○	○
1000_B3B2H	usr_wreg_1D9	A/D conversion value maximum/minimum current value update	Control	○	○

User circuit part register (Read data)

○: Applicable, ×: Not applicable

FPGA register address	Register name	Description	Type	Read	Write
1000_BB00H	usr_rreg_180	Module type signal (main)	Monitor	○	×
1000_BB02H	usr_rreg_181	Module type signal (extension)	Monitor	○	×
1000_BB04H	usr_rreg_182	Digital input (after filtering) CH0 to CHF (B0)	Monitor	○	×
1000_BB06H	usr_rreg_183	Digital input (after filtering) IOB0_DIO485_I (B0)	Monitor	○	×
1000_BB08H	usr_rreg_184	Digital input (after filtering) CH0 to CHF (B1)	Monitor	○	×
1000_BB0AH	usr_rreg_185	Digital input (after filtering) IOB1_DIO485_I (B1)	Monitor	○	×
1000_BB0CH	usr_rreg_186	Digital input (after filtering) CH0 to CHF (B2)	Monitor	○	×
1000_BB0EH	usr_rreg_187	Digital input (after filtering) IOB2_DIO485_I (B2)	Monitor	○	×
1000_BB10H	usr_rreg_188	Digital input (after filtering) CH0 to CHF (E0)	Monitor	○	×
1000_BB12H	usr_rreg_189	Digital input (after filtering) IOE0_DIO485_I (E0)	Monitor	○	×
1000_BB14H	usr_rreg_18A	Digital input (after filtering) CH0 to CHF (E1)	Monitor	○	×
1000_BB16H	usr_rreg_18B	Digital input (after filtering) IOE1_DIO485_I (E1)	Monitor	○	×
1000_BB18H	usr_rreg_18C	Digital input (after filtering) CH0 to CHF (E2)	Monitor	○	×
1000_BB1AH	usr_rreg_18D	Digital input (after filtering) IOE2_DIO485_I (E2)	Monitor	○	×
1000_BB1CH	usr_rreg_18E	A/D conversion value enable status	Monitor	○	×
1000_BB1EH	usr_rreg_18F	Analog control A/D conversion value CH0 (E0)	Monitor	○	×
1000_BB20H	usr_rreg_190	Analog control A/D conversion value CH1 (E0)	Monitor	○	×
1000_BB22H	usr_rreg_191	Analog control A/D conversion value CH2 (E0)	Monitor	○	×
1000_BB24H	usr_rreg_192	Analog control A/D conversion value CH3 (E0)	Monitor	○	×
1000_BB26H	usr_rreg_193	Analog control A/D conversion value CH4 (E0)	Monitor	○	×
1000_BB28H	usr_rreg_194	Analog control A/D conversion value CH5 (E0)	Monitor	○	×
1000_BB2AH	usr_rreg_195	Analog control A/D conversion value CH6 (E0)	Monitor	○	×
1000_BB2CH	usr_rreg_196	Analog control A/D conversion value CH7 (E0)	Monitor	○	×
1000_BB2EH	usr_rreg_197	Analog control A/D conversion value CH8 (E0)	Monitor	○	×
1000_BB30H	usr_rreg_198	Analog control A/D conversion value CH9 (E0)	Monitor	○	×
1000_BB32H	usr_rreg_199	Analog control A/D conversion value CHA (E0)	Monitor	○	×
1000_BB34H	usr_rreg_19A	Analog control A/D conversion value CHB (E0)	Monitor	○	×
1000_BB36H	usr_rreg_19B	Analog control A/D conversion value CH0 (E1)	Monitor	○	×
1000_BB38H	usr_rreg_19C	Analog control A/D conversion value CH1 (E1)	Monitor	○	×
1000_BB3AH	usr_rreg_19D	Analog control A/D conversion value CH2 (E1)	Monitor	○	×
1000_BB3CH	usr_rreg_19E	Analog control A/D conversion value CH3 (E1)	Monitor	○	×
1000_BB3EH	usr_rreg_19F	Analog control A/D conversion value CH4 (E1)	Monitor	○	×

FPGA register address	Register name	Description	Type	Read	Write
1000_BB40H	usr_rreg_1A0	Analog control A/D conversion value CH5 (E1)	Monitor	○	×
1000_BB42H	usr_rreg_1A1	Analog control A/D conversion value CH6 (E1)	Monitor	○	×
1000_BB44H	usr_rreg_1A2	Analog control A/D conversion value CH7 (E1)	Monitor	○	×
1000_BB46H	usr_rreg_1A3	Analog control A/D conversion value CH8 (E1)	Monitor	○	×
1000_BB48H	usr_rreg_1A4	Analog control A/D conversion value CH9 (E1)	Monitor	○	×
1000_BB4AH	usr_rreg_1A5	Analog control A/D conversion value CHA (E1)	Monitor	○	×
1000_BB4CH	usr_rreg_1A6	Analog control A/D conversion value CHB (E1)	Monitor	○	×
1000_BB4EH	usr_rreg_1A7	Analog control A/D conversion value CH0 (E2)	Monitor	○	×
1000_BB50H	usr_rreg_1A8	Analog control A/D conversion value CH1 (E2)	Monitor	○	×
1000_BB52H	usr_rreg_1A9	Analog control A/D conversion value CH2 (E2)	Monitor	○	×
1000_BB54H	usr_rreg_1AA	Analog control A/D conversion value CH3 (E2)	Monitor	○	×
1000_BB56H	usr_rreg_1AB	Analog control A/D conversion value CH4 (E2)	Monitor	○	×
1000_BB58H	usr_rreg_1AC	Analog control A/D conversion value CH5 (E2)	Monitor	○	×
1000_BB5AH	usr_rreg_1AD	Analog control A/D conversion value CH6 (E2)	Monitor	○	×
1000_BB5CH	usr_rreg_1AE	Analog control A/D conversion value CH7 (E2)	Monitor	○	×
1000_BB5EH	usr_rreg_1AF	Analog control A/D conversion value CH8 (E2)	Monitor	○	×
1000_BB60H	usr_rreg_1B0	Analog control A/D conversion value CH9 (E2)	Monitor	○	×
1000_BB62H	usr_rreg_1B1	Analog control A/D conversion value CHA (E2)	Monitor	○	×
1000_BB64H	usr_rreg_1B2	Analog control A/D conversion value CHB (E2)	Monitor	○	×
1000_BB66H	usr_rreg_1B3	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B0)	Monitor	○	×
1000_BB68H	usr_rreg_1B4	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B0)	Monitor	○	×
1000_BB6AH	usr_rreg_1B5	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B1)	Monitor	○	×
1000_BB6CH	usr_rreg_1B6	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B1)	Monitor	○	×
1000_BB6EH	usr_rreg_1B7	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B2)	Monitor	○	×
1000_BB70H	usr_rreg_1B8	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B2)	Monitor	○	×
1000_BB72H	usr_rreg_1B9	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E0)	Monitor	○	×
1000_BB74H	usr_rreg_1BA	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E0)	Monitor	○	×
1000_BB76H	usr_rreg_1BB	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E1)	Monitor	○	×
1000_BB78H	usr_rreg_1BC	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E1)	Monitor	○	×
1000_BB7AH	usr_rreg_1BD	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E2)	Monitor	○	×
1000_BB7CH	usr_rreg_1BE	Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E2)	Monitor	○	×
1000_BB7EH	usr_rreg_1BF	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B0)	Monitor	○	×
1000_BB80H	usr_rreg_1C0	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B0)	Monitor	○	×
1000_BB82H	usr_rreg_1C1	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B1)	Monitor	○	×
1000_BB84H	usr_rreg_1C2	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B1)	Monitor	○	×
1000_BB86H	usr_rreg_1C3	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B2)	Monitor	○	×
1000_BB88H	usr_rreg_1C4	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B2)	Monitor	○	×

FPGA register address	Register name	Description	Type	Read	Write
1000_BB8AH	usr_rreg_1C5	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E0)	Monitor	○	×
1000_BB8CH	usr_rreg_1C6	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E0)	Monitor	○	×
1000_BB8EH	usr_rreg_1C7	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E1)	Monitor	○	×
1000_BB90H	usr_rreg_1C8	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E1)	Monitor	○	×
1000_BB92H	usr_rreg_1C9	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E2)	Monitor	○	×
1000_BB94H	usr_rreg_1CA	Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E2)	Monitor	○	×
1000_BB96H	usr_rreg_1CB	Pulse output part output pulse count (lower side) (B0)	Monitor	○	×
1000_BB98H	usr_rreg_1CC	Pulse output part output pulse count (upper side) (B0)	Monitor	○	×
1000_BB9AH	usr_rreg_1CD	Pulse output part output pulse count (lower side) (B1)	Monitor	○	×
1000_BB9CH	usr_rreg_1CE	Pulse output part output pulse count (upper side) (B1)	Monitor	○	×
1000_BB9EH	usr_rreg_1CF	Pulse output part output pulse count (lower side) (B2)	Monitor	○	×
1000_BBA0H	usr_rreg_1D0	Pulse output part output pulse count (upper side) (B2)	Monitor	○	×
1000_BBA2H	usr_rreg_1D1	Pulse output part output pulse count (lower side) (E0)	Monitor	○	×
1000_BBA4H	usr_rreg_1D2	Pulse output part output pulse count (upper side) (E0)	Monitor	○	×
1000_BBA6H	usr_rreg_1D3	Pulse output part output pulse count (lower side) (E1)	Monitor	○	×
1000_BBA8H	usr_rreg_1D4	Pulse output part output pulse count (upper side) (E1)	Monitor	○	×
1000_BBAAH	usr_rreg_1D5	Pulse output part output pulse count (lower side) (E2)	Monitor	○	×
1000_BBACH	usr_rreg_1D6	Pulse output part output pulse count (upper side) (E2)	Monitor	○	×
1000_BBAEH	usr_rreg_1D7	Maximum A/D conversion value CH0	Monitor	○	×
1000_BBB0H	usr_rreg_1D8	Maximum A/D conversion value CH1	Monitor	○	×
1000_BBB2H	usr_rreg_1D9	Maximum A/D conversion value CH2	Monitor	○	×
1000_BBB4H	usr_rreg_1DA	Maximum A/D conversion value CH3	Monitor	○	×
1000_BBB6H	usr_rreg_1DB	Maximum A/D conversion value CH4	Monitor	○	×
1000_BBB8H	usr_rreg_1DC	Maximum A/D conversion value CH5	Monitor	○	×
1000_BBBAH	usr_rreg_1DD	Maximum A/D conversion value CH6	Monitor	○	×
1000_BBBCH	usr_rreg_1DE	Maximum A/D conversion value CH7	Monitor	○	×
1000_BBBEH	usr_rreg_1DF	Maximum A/D conversion value CH8	Monitor	○	×
1000_BBC0H	usr_rreg_1E0	Maximum A/D conversion value CH9	Monitor	○	×
1000_BBC2H	usr_rreg_1E1	Maximum A/D conversion value CHA	Monitor	○	×
1000_BBC4H	usr_rreg_1E2	Maximum A/D conversion value CHB	Monitor	○	×
1000_BBC6H	usr_rreg_1E3	Minimum A/D conversion value CH0	Monitor	○	×
1000_BBC8H	usr_rreg_1E4	Minimum A/D conversion value CH1	Monitor	○	×
1000_BBCAH	usr_rreg_1E5	Minimum A/D conversion value CH2	Monitor	○	×
1000_BBCCH	usr_rreg_1E6	Minimum A/D conversion value CH3	Monitor	○	×
1000_BBCEH	usr_rreg_1E7	Minimum A/D conversion value CH4	Monitor	○	×
1000_BBD0H	usr_rreg_1E8	Minimum A/D conversion value CH5	Monitor	○	×
1000_BBD2H	usr_rreg_1E9	Minimum A/D conversion value CH6	Monitor	○	×
1000_BBD4H	usr_rreg_1EA	Minimum A/D conversion value CH7	Monitor	○	×
1000_BBD6H	usr_rreg_1EB	Minimum A/D conversion value CH8	Monitor	○	×
1000_BBD8H	usr_rreg_1EC	Minimum A/D conversion value CH9	Monitor	○	×
1000_BBDAH	usr_rreg_1ED	Minimum A/D conversion value CHA	Monitor	○	×
1000_BBDCH	usr_rreg_1EE	Minimum A/D conversion value CHB	Monitor	○	×

FPGA register details (reset control part)

The details of the FPGA register of the reset control part are shown below.

Internal operation start/stop

■Address

Name	FPGA register address
Internal operation start/stop (mode_ctrl2)	1000_0002H

■Description

Use for FPGA internal operation start/stop.

Firmware controls the FPGA control start processing and FPGA control stop processing.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Internal operation start/stop
- 0: Stop
- 1: Start

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Module type (main)

■Address

Name	FPGA register address
Module type (basic) (unit_set_base)	1000_0004H

■Description

The module type of the circuit board connected to the connector (B0 to B2) of the main module is stored.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)				(3)				(2)				(1)			

(1) Module type (B0) (IOB0_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

(2) Module type (B1) (IOB1_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

(3) Module type (B2) (IOB2_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Module type (extension)

■Address

Name	FPGA register address
Module type (extension) (unit_set_ext)	1000_0006H

■Description

Stores the module type of the circuit board connected to the connector (E0 to E2) of the extension module.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)											(1)				

(1) Module type (E0 to E2) (IOE_UNIT[4:0])
- 0_0001: DC I/O circuit board (E0 to E2)
- 0_0010: Differential I/O circuit board (E0 to E2)
- 0_0011: Analog I/O circuit board (E0 to E2)
- 0_1111: No connection circuit board (E0 to E2)

■FPGA initial value

0_0000H

■Firmware initial value

—

■Reset cause

Reset

External reset ON/OFF setting

■Address

Name	FPGA register address
If the external reset ON/OFF setting (ioport_set)	1000_0020H

■Description

Sets ON (issued) or OFF (not issued) for the reset issued to the circuit board when FPGA control is stopped (when the internal operation start/stop is stop).

The external output when ON differs depending on the circuit board type.

- DC I/O circuit board: OFF
- Differential I/O circuit board: Hi-Z
- Analog I/O circuit board: 0V/0mA

The external output when OFF differs depending on the circuit board type.

- DC I/O circuit board: Previous value held
- Differential I/O circuit board: "CLEAR (L fixed output)", "CLEAR (H fixed output)", and " HOLD (previous value hold)" can be set by "Differential output HOLD/CLEAR" setting.
- Analog I/O circuit board: Previous value held external reset ON/OFF setting (E0 to E2)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												(4)	(3)	(2)	(1)

(1) External reset ON/OFF setting (B0)
- 1: Reset OFF
- 0: Reset ON

(2) External reset ON/OFF setting (B1)
- 1: Reset OFF
- 0: Reset ON

(3) External reset ON/OFF setting (B2)
- 1: Reset OFF
- 0: Reset ON

(4) External reset ON/OFF setting (E0 to E2)
- 1: Reset OFF
- 0: Reset ON

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

- Changes to this register when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0) are immediately reflected.
- Settings cannot be made by the FPGA register access function. Set from the FPGA Module Configuration Tool.

FPGA version register

■Address

Name	FPGA register address
FPGA version register (fpga_version)	1000_0100H

■Description

The version of the standard circuit and sample circuit can be checked.

- 0001H: Version 1.00

■FPGA initial value

FPGA version

■Firmware initial value

—

■Reset cause

Reset

FPGA register details (timing generator)

The details of the FPGA register of the timing generator are shown below.

Filter sampling pulse

■Address

Name	FPGA register address
Filter sampling pulse (B0) (tim_iob0x_samp)	1000_2000H
Filter sampling pulse (B1) (tim_iob1x_samp)	1000_2002H
Filter sampling pulse (B2) (tim_iob2x_samp)	1000_2004H
Filter sampling pulse (E0) (tim_ioe0x_samp)	1000_2008H
Filter sampling pulse (E1) (tim_ioe1x_samp)	1000_200AH
Filter sampling pulse (E2) (tim_ioe2x_samp)	1000_200CH

■Description

Sets the operation cycle of the digital filter. This setting is common to all input terminals of B☐ and E☐.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												Filter sampling pulse setting			

- FH: Data sampling timing
- EH: 100.00μs
- DH: 10.00μs
- CH: 2.00μs
- BH: 1.00μs
- AH: 0.50μs
- 9H: 0.40μs
- 8H: 0.32μs
- 7H: 0.20μs
- 6H: 0.16μs
- 5H: 0.14μs
- 4H: 0.10μs
- 3H: 0.08μs
- 2H: 0.04μs
- 1H: 0.02μs
- 0H: 0.01μs

The filter time is given by the following formula. Set each register appropriately.

- Filter time = Filter sampling pulse × Input filter counter upper limit

Set the filter time to a value with a margin from the minimum value of the ON/OFF width to be taken in as an input, taking into consideration the delay time outside the FPGA.

The following is a rough indication for the filter time for this module.

Application		Rough indication
For general-purpose input		60% of the minimum ON/OFF width taken as input
For pulse counting	For DC input	• 1-phase input: 10% of pulse cycle • 2-phase input: 5% of pulse cycle
	For differential (RS-422/RS-485) input	• 1-phase input: 15% of pulse cycle • 2-phase input: 12.5% of pulse cycle

■FPGA initial value

0H

■Firmware initial value

- DC I/O circuit board: FH
- Differential I/O circuit board: 0H

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to B☐ or E☐, only data sampling timing (FH) can be used.
- When differential I/O circuit board is connected to B☐ and E☐, data sampling timing (FH) cannot be set.
- When an analog I/O circuit board is connected to E☐, the setting is disabled.

A

Data sampling timing (B□)

■Address

Name	FPGA register address
Data sampling timing (B0) (tim_iob0x_en)	1000_2100H
Data sampling timing (B1) (tim_iob1x_en)	1000_2102H
Data sampling timing (B2) (tim_iob2x_en)	1000_2104H

■Description

Sets the timing (cycle) for sampling DC/differential (RS-422/RS-485). (Setting unit: 0.01μs)

- FFFFH: 655.36μs
- FFFEH: 655.35μs to 0004H: 0.05μs
- 0003H: 0.04μs
- 0002H: 0.03μs
- 0001H: 0.02μs
- 0000H: 0.01μs

■FPGA initial value

0000H

■Firmware initial value

- DC I/O circuit board: 000EH(0.15μs)
- Differential I/O circuit board: 0000H(0.01μs)

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to B□, the value cannot be set to less than 0009H (0.10μs).
- When a differential I/O circuit board is connected to B□, set the same setting value as for the filter sampling pulse (B□).

Data sampling timing (E☐)

■Address

Name	FPGA register address
Data sampling timing (E0) (tim_ioe0x_en)	1000_2108H
Data sampling timing (E1) (tim_ioe1x_en)	1000_210AH
Data sampling timing (E2) (tim_ioe2x_en)	1000_210CH

■Description

Sets the timing (cycle) for sampling DC/differential (RS-422/RS-485)/analog input. (Setting unit: 0.01μs)

- FFFFH: 655.36μs
- FFFEH: 655.35μs to 0004H: 0.05μs
- 0003H: 0.04μs
- 0002H: 0.03μs
- 0001H: 0.02μs
- 0000H: 0.01μs

■FPGA initial value

0000H

■Firmware initial value

- DC I/O circuit board, No circuit board: 000EH (0.15μs)
- Differential I/O circuit board: 0000H (0.01μs)
- Analog I/O circuit board: 018FH (4.00μs)

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to E☐, the value cannot be set to less than 0009H (0.10μs).
- When the differential I/O circuit board is connected to E☐, the filter sampling pulse (E☐) should be set to the same setting value.
- When an analog I/O circuit board is connected to E☐, the setting is invalid if any of the following conditions are met.

Conditions
• "A/D conversion enable/disable setting" is set to "Conversion-disable" • "A/D conversion timing selection" is set to "user circuit output"

- When an analog I/O circuit board is connected to E☐, the lower limit value of the setting range differs depending on ADC oversampling ratio setting. Set as follows.

ADC oversampling ratio setting	Setting range of data sampling timing
No Setting	4μs or more
2x	6μs or more
4x	8μs or more
8x	13μs or more
16x	24μs or more
32x	44μs or more
64x	84μs or more
128x	165μs or more
256x	328μs or more

Data update timing

■Address

Name	FPGA register address
Data update timing (B0) (tim_iob0x_conv)	1000_2110H
Data update timing (B1) (tim_iob1x_conv)	1000_2112H
Data update timing (B2) (tim_iob2x_conv)	1000_2114H
Data update timing (E0) (tim_ioe0x_conv)	1000_2118H
Data update timing (E1) (tim_ioe1x_conv)	1000_211AH
Data update timing (E2) (tim_ioe2x_conv)	1000_211CH

■Description

Sets the output timing (cycle) for DC/differential (RS-422/RS-485)/analog output. (Setting unit: 0.01μs)

- FFFFH: 655.36μs
- FFFEH: 655.35μs to 0004H: 0.05μs
- 0003H: 0.04μs
- 0002H: 0.03μs
- 0001H: 0.02μs
- 0000H: 0.01μs

■FPGA initial value

0000H

■Firmware initial value

- DC I/O circuit board: 0009H (0.10μs)
- Differential I/O circuit board: 0000H (0.01μs)
- Analog I/O circuit board: 0257H (6.00μs) (E0 to E2 only)
- No circuit board: 0009H (0.10μs) (E0 to E2 only)

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to B☐ or E☐, the value cannot be set to less than 0009H (0.10μs).
- When an Analog I/O circuit board is connected to E☐, the value cannot be set to less than 0256H (6.00μs). D/A conversion timing selection (E☐) (aoport_da_cyc_sel) is the user circuit output (1), the setting is disabled.

Logging cycle timing

■Address

Name	FPGA register address
Logging cycle timing (tim_log_cyc)	1000_2200H

■Description

Sets the logging cycle timing.

- FFFFH: 32.768ms
- FFFEH: 32.7675ms to 0003H: 2μs
- 0002H: 1.5μs
- 0000H to 0001H: 1μs

■FPGA initial value

0000H

■Firmware initial value

0001H

■Reset cause

Reset

■Precautions and restrictions

- Settings cannot be made by the FPGA register access function. Set from the FPGA Module Configuration Tool.
- The contents of this register are in increments of 0.5μs, but the FPGA Module Configuration Tool sets them in increments of 1μs.
- If b13 of the logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) is set to user circuit output (1), the setting is disabled.

FPGA register details (digital input control part)

The details of the FPGA register of the digital input control part are shown below.

Input filter counter upper limit

■Address

Name	FPGA register address
Input filter counter upper limit (IOB0_X0)(B0) (iport_iob0_0_filcnt_upper) to Input filter counter upper limit (IOB0_XF)(B0) (iport_iob0_f_filcnt_upper)	1000_3000H to 1000_301EH
Input filter counter upper limit (IOB1_X0)(B1) (iport_iob1_0_filcnt_upper) to Input filter counter upper limit (IOB1_XF)(B1) (iport_iob1_f_filcnt_upper)	1000_3020H to 1000_303EH
Input filter counter upper limit (IOB2_X0)(B2) (iport_iob2_0_filcnt_upper) to Input filter counter upper limit (IOB2_XF)(B2) (iport_iob2_f_filcnt_upper)	1000_3040H to 1000_305EH
Input filter counter upper limit (IOE0_X0)(E0) (iport_ioe0_0_filcnt_upper) to Input filter counter upper limit (IOE0_XF)(E0) (iport_ioe0_f_filcnt_upper)	1000_3060H to 1000_307EH
Input filter counter upper limit (IOE1_X0)(E1) (iport_ioe1_0_filcnt_upper) to Input filter counter upper limit (IOE1_XF)(E1) (iport_ioe1_f_filcnt_upper)	1000_3080H to 1000_309EH
Input filter counter upper limit (IOE2_X0)(E2) (iport_ioe2_0_filcnt_upper) to Input filter counter upper limit (IOE2_XF)(E2) (iport_ioe2_f_filcnt_upper)	1000_30A0H to 1000_30BEH

■Description

Sets the filter counter upper limit value of the DC/differential (RS-422) input digital filter.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)				(1)											

(1) Digital input filter (up/down counter) upper limit value
- 001H to FFFH
- 000H: No filter (through output)

The filter time is given by the following formula. Set each register appropriately.

- Filter time = Filter sampling pulse × Input filter counter upper limit

Set the filter time to a value with a margin from the minimum value of the ON/OFF width to be taken in as an input, taking into consideration the delay time outside the FPGA.

The following is a rough indication for the filter time for this module.

Application		Rough indication
For general-purpose input		60% of the minimum ON/OFF width taken as input
For pulse counting	For DC input	• 1-phase input: 10% of pulse cycle • 2-phase input: 5% of pulse cycle
	For differential (RS-422) input	• 1-phase input: 15% of pulse cycle • 2-phase input: 12.5% of pulse cycle

■FPGA initial value

0FFFH

■Firmware initial value

- DC I/O circuit board: FA0H (4000)
- Differential I/O circuit board: 5DCH (1500)
- Analog I/O circuit board: FA0H (4000)
- No circuit board: FA0H (4000)

■Reset cause

Reset

■Precautions and restrictions

- When a differential I/O circuit board is connected to B□, the input filter counter upper limit (IOB□_X8)(B□) (iport_iob□_8_filcnt_upper) to input filter counter upper limit (IOB□_XF)(B□) (iport_iob□_f_filcnt_upper) settings are disabled.
- When a differential I/O circuit board is connected to E□, the input filter counter upper limit (IOE□_X8)(E□) (iport_ioe□_8_filcnt_upper) to input filter counter upper limit (IOE□_XF)(E□) (iport_ioe□_f_filcnt_upper) settings are disabled.
- When an analog I/O circuit board is connected to E□, the setting is disabled.

Input signal monitor

■Address

Name	FPGA register address
Input signal monitor (B0) (iport_iob0x_monitor)	1000_3100H
Input signal monitor (B1) (iport_iob1x_monitor)	1000_3102H
Input signal monitor (B2) (iport_iob2x_monitor)	1000_3104H
Input signal monitor (E0) (iport_ioe0x_monitor)	1000_3110H
Input signal monitor (E1) (iport_ioe1x_monitor)	1000_3112H
Input signal monitor (E2) (iport_ioe2x_monitor)	1000_3114H

■Description

The input signal after filtering can be checked.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOB□_XF	IOB□_XE	IOB□_XD	IOB□_XC	IOB□_XB	IOB□_XA	IOB□_X9	IOB□_X8	IOB□_X7	IOB□_X6	IOB□_X5	IOB□_X4	IOB□_X3	IOB□_X2	IOB□_X1	IOB□_X0
IOE□_XF	IOE□_XE	IOE□_XD	IOE□_XC	IOE□_XB	IOE□_XA	IOE□_X9	IOE□_X8	IOE□_X7	IOE□_X6	IOE□_X5	IOE□_X4	IOE□_X3	IOE□_X2	IOE□_X1	IOE□_X0

■FPGA initial value

Input signal (IOB□_X0 to IOB□_XF), or (IOE□_X0 to IOE□_XF)

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

- When a differential I/O circuit board is connected to B□ or E□, b15 to b8 are fixed to 0.
- When an analog I/O circuit board is connected to E□, all are fixed to 0.

A

FPGA register details (digital output control part)

Output signal selection

■Address

Name	FPGA register address
Output signal selection (B0) (oport_iob0y_osel)	1000_4000H
Output signal selection (B1) (oport_iob1y_osel)	1000_4002H
Output signal selection (B2) (oport_iob2y_osel)	1000_4004H
Output signal selection (E0) (oport_ioe0y_osel)	1000_4008H
Output signal selection (E1) (oport_ioe1y_osel)	1000_400AH
Output signal selection (E2) (oport_ioe2y_osel)	1000_400CH

■Description

Sets the signal to output to the DC/differential (RS-422) output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOB□_YF	IOB□_YE	IOB□_YD	IOB□_YC	IOB□_YB	IOB□_YA	IOB□_Y9	IOB□_Y8	IOB□_Y7	IOB□_Y6	IOB□_Y5	IOB□_Y4	IOB□_Y3	IOB□_Y2	IOB□_Y1	IOB□_Y0
IOE□_YF	IOE□_YE	IOE□_YD	IOE□_YC	IOE□_YB	IOE□_YA	IOE□_Y9	IOE□_Y8	IOE□_Y7	IOE□_Y6	IOE□_Y5	IOE□_Y4	IOE□_Y3	IOE□_Y2	IOE□_Y1	IOE□_Y0

Setting value	Description
1: Select the user circuit output.	Digital output signals (B□) (uc_iob□_y_clk100m_reg) and digital output signals (E□) (uc_ioe□_y_clk100m_reg) from the user circuit part are output to DC/differential (RS-422) output.
0: Select the register setting value (oport_iob□y_odata: RY) and the register setting value (oport_ioe□y_odata: RY).	The values set for the output value setting (B□) and output value setting (E□) are output to the DC/differential (RS-422) output. The output value setting (B□) and output value setting (E□) store the remote output signal (RY) value by firmware.

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

■Precautions and restrictions

- When a differential I/O circuit board is connected to B□ or E□, the b15 to b8 settings are disabled.
- When an analog I/O circuit board is connected to E□, the settings are disabled.

Output value setting register

■Address

Name	FPGA register address
Output value setting (B0) (oport_iob0y_odata)	1000_4010H
Output value setting (B1) (oport_iob1y_odata)	1000_4012H
Output value setting (B2) (oport_iob2y_odata)	1000_4014H
Output value setting (E0) (oport_ioe0y_odata)	1000_4018H
Output value setting (E1) (oport_ioe1y_odata)	1000_401AH
Output value setting (E2) (oport_ioe2y_odata)	1000_401CH

■Description

Sets the signal value to be output to the output signal (IOB□_Yx) and the output signal (IOE□_Yx).

Remote output signal (RY) is set by firmware.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOB□_YF	IOB□_YE	IOB□_YD	IOB□_YC	IOB□_YB	IOB□_YA	IOB□_Y9	IOB□_Y8	IOB□_Y7	IOB□_Y6	IOB□_Y5	IOB□_Y4	IOB□_Y3	IOB□_Y2	IOB□_Y1	IOB□_Y0
IOE□_YF	IOE□_YE	IOE□_YD	IOE□_YC	IOE□_YB	IOE□_YA	IOE□_Y9	IOE□_Y8	IOE□_Y7	IOE□_Y6	IOE□_Y5	IOE□_Y4	IOE□_Y3	IOE□_Y2	IOE□_Y1	IOE□_Y0

- 1: (1) Output
- 0: (0) Output

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

■Precautions and restrictions

- When the user circuit output (1) is set to output signal selection (B0) (oport_iob0y_osel) (FPGA register address: 1000_4000H) to output signal selection (E2) (oport_ioe2y_osel) (FPGA register address: 1000_400CH), the setting is disabled.
- When a differential I/O circuit board is connected to B□ or E□, the b15 to b8 settings are disabled.
- When an analog I/O circuit board is connected to E□, the settings are disabled.

Output signal monitor register

■Address

Name	FPGA register address
Output signal monitor (B0) (iport_iob0y_monitor)	1000_4020H
Output signal monitor (B1) (iport_iob1y_monitor)	1000_4022H
Output signal monitor (B2) (iport_iob2y_monitor)	1000_4024H
Output signal monitor (E0) (iport_ioe0y_monitor)	1000_4030H
Output signal monitor (E1) (iport_ioe1y_monitor)	1000_4032H
Output signal monitor (E2) (iport_ioe2y_monitor)	1000_4034H

■Description

The output signals (IOB0_Y0 to IOB0_YF) after output signal selection (after selecting with the oport_iob0y_osel register) to the output signals (IOE2_Y0 to IOE2_YF) after output signal selection (after selecting with the oport_ioe2y_osel register) can be checked.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOB□_YF	IOB□_YE	IOB□_YD	IOB□_YC	IOB□_YB	IOB□_YA	IOB□_Y9	IOB□_Y8	IOB□_Y7	IOB□_Y6	IOB□_Y5	IOB□_Y4	IOB□_Y3	IOB□_Y2	IOB□_Y1	IOB□_Y0
IOE□_YF	IOE□_YE	IOE□_YD	IOE□_YC	IOE□_YB	IOE□_YA	IOE□_Y9	IOE□_Y8	IOE□_Y7	IOE□_Y6	IOE□_Y5	IOE□_Y4	IOE□_Y3	IOE□_Y2	IOE□_Y1	IOE□_Y0

■FPGA initial value

Output signal (IOB□_Y0 to IOB□_YF), or (IOE□_X0 to IOE□_XF)

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

- When a differential I/O circuit board is connected to B□ or E□, b15 to b8 are fixed to 0.
- When an analog I/O circuit board is connected to E□, all are fixed to 0.

Differential output HOLD/CLEAR

■Address

Name	FPGA register address
Differential output HOLD/CLEAR (B0) (oport_iob0y_holdclr)	1000_4040H
Differential output HOLD/CLEAR (B1) (oport_iob1y_holdclr)	1000_4042H
Differential output HOLD/CLEAR (B2) (oport_iob2y_holdclr)	1000_4044H
Differential output HOLD/CLEAR (E0) (oport_ioe0y_holdclr)	1000_4046H
Differential output HOLD/CLEAR (E1) (oport_ioe1y_holdclr)	1000_4048H
Differential output HOLD/CLEAR (E2) (oport_ioe2y_holdclr)	1000_404AH

■Description

Fix the logic of output signals (IOB0_Y0 to IOB0_Y7) to output signals (IOE2_Y0 to IOE2_Y7) when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IOB□_Y7		IOB□_Y6		IOB□_Y5		IOB□_Y4		IOB□_Y3		IOB□_Y2		IOB□_Y1		IOB□_Y0	
IOE□_Y7		IOE□_Y6		IOE□_Y5		IOE□_Y4		IOE□_Y3		IOE□_Y2		IOE□_Y1		IOE□_Y0	

- 2H, 3H: HOLD (previous value held)
- 1H: CLEAR (fixed to H)
- 0H: CLEAR (fixed to L)

■FPGA initial value

1H

■Firmware initial value

1H

■Reset cause

Reset

■Precautions and restrictions

- Changes to this register when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0) are immediately reflected.
- External reset ON/OFF setting (ioport_set) (FPGA register address: 1000_0020H) is reset ON (0), the differential output circuit outside the FPGA is reset. Therefore, the logic of the output signals (IOB0_Y0 to IOB0_Y7) set by the differential output HOLD/CLEAR to the output signals (IOE2_Y0 to IOE2_Y7) after output signal selection (after selection by the oport_ioe2y_osel register) is not output outside the module.
- When a DC I/O circuit board is connected to B□, the settings are disabled.
- When a DC I/O circuit board or an analog I/O circuit board is connected to E□, the settings are disabled.

FPGA register details (digital I/O control part)

Input filter counter upper limit

■Address

Name	FPGA register address
Input filter counter upper limit (IOB0_DIO485_I)(B0) (iport_iob0_dio485_filcnt_upper)	1000_5000H
Input filter counter upper limit (IOB1_DIO485_I)(B1) (iport_iob1_dio485_filcnt_upper)	1000_5002H
Input filter counter upper limit (IOB2_DIO485_I)(B2) (iport_iob2_dio485_filcnt_upper)	1000_5004H
Input filter counter upper limit (IOE0_DIO485_I)(E0) (iport_ioe0_dio485_filcnt_upper)	1000_5008H
Input filter counter upper limit (IOE1_DIO485_I)(E1) (iport_ioe1_dio485_filcnt_upper)	1000_500AH
Input filter counter upper limit (IOE2_DIO485_I)(E2) (iport_ioe2_dio485_filcnt_upper)	1000_500CH

■Description

Sets the filter counter upper limit value of the differential (RS-485) input digital filter.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)				(1)											

(1) Digital input filter (up/down counter) upper limit value
- 001H to FFFH
- 000H: No filter (through output)

The filter time is given by the following formula. Set each register appropriately.

- Filter time = Filter sampling pulse × Input filter counter upper limit

Set the filter time to a value with a margin from the minimum value of the ON/OFF width to be taken in as an input, taking into consideration the delay time outside the FPGA.

The following is a rough indication for the filter time for this module.

Application	Rough indication
For general-purpose input	60% of the minimum ON/OFF width taken as input
For pulse counting	1-phase input: 15% of pulse cycle

■FPGA initial value

FFFH

■Firmware initial value

- DC I/O circuit board: FA0H (4000)
- Differential I/O circuit board: 5DCH (1500)
- Analog I/O circuit board: FA0H (4000)
- No circuit board: FA0H (4000)

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to B☐ or E☐, the settings are disabled.
- When an analog I/O circuit board is connected to E☐, the settings are disabled.

I/O signal monitor

■Address

Name	FPGA register address
I/O signal monitor (IOB0_DIO485)(B0) (ioport_iob0_dio485_monitor)	1000_5010H
I/O signal monitor (IOB1_DIO485)(B1) (ioport_iob1_dio485_monitor)	1000_5012H
I/O signal monitor (IOB2_DIO485)(B2) (ioport_iob2_dio485_monitor)	1000_5014H
I/O signal monitor (IOE0_DIO485)(E0) (ioport_ioe0_dio485_monitor)	1000_5018H
I/O signal monitor (IOE1_DIO485)(E1) (ioport_ioe1_dio485_monitor)	1000_501AH
I/O signal monitor (IOE2_DIO485)(E2) (ioport_ioe2_dio485_monitor)	1000_501CH

■Description

Monitors input signals (IOB□_DIO485_I, IOE□_DIO485_I) after filtering, and output signals (IOB□_DIO485_O, IOE□_DIO485_O) after the output selection (ioport_iob□_dio485_osel selection, ioport_ioe□_dio485_osel selection).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) Displays the input signal after filtering. (IOB□_DIO485_I) or (IOE□_DIO485_I)
(2) Displays the output signal after output selection. (IOB□_DIO485_O) or (IOE□_DIO485_O)
(3) Displays I/O direction signals after output selection. (IOB□_DIO485_EN) or (IOE□_DIO485_EN)
- 1: Output direction
- 0: Input direction

■FPGA initial value

- b0: (IOB□_DIO485_I) or (IOE□_DIO485_I)
- b1: (IOB□_DIO485_O) or (IOE□_DIO485_O)
- b2: (IOB□_DIO485_EN) or (IOE□_DIO485_EN)

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board is connected to B□ or E□, it is fixed to 0.
- When an analog I/O circuit board is connected to E□, it is fixed to 0.

Select output signal or I/O direction signal

■Address

Name	FPGA register address
Output signal/Input output direction signal selection (B0) (ioport_iob0_dio485_osel)	1000_5020H
Output signal/Input output direction signal selection (B1) (ioport_iob1_dio485_osel)	1000_5022H
Output signal/Input output direction signal selection (B2) (ioport_iob2_dio485_osel)	1000_5024H
Output signal/Input output direction signal selection (E0) (ioport_ioe0_dio485_osel)	1000_5028H
Output signal/Input output direction signal selection (E1) (ioport_ioe1_dio485_osel)	1000_502AH
Output signal/Input output direction signal selection (E2) (ioport_ioe2_dio485_osel)	1000_502CH

■Description

Selects the signal to output to the differential (RS-485) output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) The output value of IOB□_DIO485_O or IOE□_DIO485_O output signal
- 1: Select the user circuit output*1.
- 0: Output value/Input output direction setting*2

(2) IOB□_DIO485_EN or IOE□_DIO485_EN I/O direction
- 1: Select the user circuit output*1.
- 0: Output value/Input output direction setting*2

*1 Digital I/O signals (B□) (uc_iob□_dio485_o_clk100m_reg) from the user circuit part or digital I/O signals (E□) (uc_ioe□_dio485_o_clk100m_reg) is selected.

*2 A value set by the output value/Input output direction setting (B□) (ioport_iob□_dio485_odata), or output value/Input output direction setting (E□) (ioport_ioe□_dio485_odata) is selected. It can be operated from the remote output signal (RY).

■FPGA initial value

00

■Firmware initial value

00

■Reset cause

Reset

■Precautions and restrictions

- Changes to this register when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0) are immediately reflected.
- When a DC I/O circuit board is connected to B□ or E□, the settings are disabled.
- When an analog I/O circuit board is connected to E□, the settings are disabled.

Output value/Input output direction setting

■Address

Name	FPGA register address
Output value/Input output direction setting (B0) (ioport_iob0_dio485_odata)	1000_5030H
Output value/Input output direction setting (B1) (ioport_iob1_dio485_odata)	1000_5032H
Output value/Input output direction setting (B2) (ioport_iob2_dio485_odata)	1000_5034H
Output value/Input output direction setting (E0) (ioport_ioe0_dio485_odata)	1000_5038H
Output value/Input output direction setting (E1) (ioport_ioe1_dio485_odata)	1000_503AH
Output value/Input output direction setting (E2) (ioport_ioe2_dio485_odata)	1000_503CH

■Description

Sets the differential (RS-485) I/O direction when Output signal/Input output direction signal selection (B☐) is set to the register setting value (ioport_iob☐_dio485_odata: RY) (00) or Output signal/Input output direction signal selection (E☐) is set to the register setting value (ioport_ioe☐_dio485_odata: RY) (00). Also, set the output value of the differential (RS-485) output.
The direction of differential (RS-485) I/O can be set from FPGA Module Configuration Tool.
For the output value of the differential (RS-485) output, the external output signal XY(B0 to B2, E0 to E2) (RY18, RY28, RY38, RY48, RY58, RY68) of the remote output signal (RY) is set by firmware.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) IOB☐_DIO485_O, or IOE☐_DIO485_O
- 1: 1 output (H output in output direction)
- 0: 0 output (L output in output direction)

(2) IOB☐_DIO485_EN, or IOE☐_DIO485_EN
- 1: 1 output (output direction)
- 0: 0 output (input direction)

■FPGA initial value

00

■Firmware initial value

00

■Reset cause

Reset

■Precautions and restrictions

- When Output signal/Input output direction signal selection (B☐) (ioport_iob☐_dio485_osel) or Output signal/Input output direction signal selection (E☐) (ioport_ioe☐_dio485_osel) is the user output circuit (11), the settings are disabled.
- When a DC I/O circuit board is connected to B☐ or E☐, the settings are disabled.

Differential output HOLD/CLEAR

■Address

Name	FPGA register address
Differential output HOLD/CLEAR (IOB0_DIO485_O) (B0) (ioport_iob0y_holdclr)	1000_5040H
Differential output HOLD/CLEAR (IOB1_DIO485_O) (B1) (ioport_iob1y_holdclr)	1000_5042H
Differential output HOLD/CLEAR (IOB2_DIO485_O) (B2) (ioport_iob2y_holdclr)	1000_5044H
Differential output HOLD/CLEAR (IOE0_DIO485_O) (E0) (ioport_ioe0y_holdclr)	1000_5046H
Differential output HOLD/CLEAR (IOE1_DIO485_O) (E1) (ioport_ioe1y_holdclr)	1000_5048H
Differential output HOLD/CLEAR (IOE2_DIO485_O) (E2) (ioport_ioe2y_holdclr)	1000_504AH

■Description

When the internal operation start/stop (mode_ctrl2) is stopped (0), the logic of the output signal (IOB□_DIO485_O) or the output signal (IOE□_DIO485_O) is fixed.

- 2H, 3H: HOLD (previous value held)
- 1H: CLEAR (fixed to H)
- 0H: CLEAR (fixed to L)

■FPGA initial value

1H

■Firmware initial value

1H

■Reset cause

Reset

■Precautions and restrictions

- Changes to this register when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0) are immediately reflected.
- If the external reset ON/OFF setting (ioport_set) is reset ON (0), the differential output circuit outside the FPGA is reset. Therefore, the logic of the output signals (IOB□_Y0 to IOB□_Y7) set by the differential output HOLD/CLEAR to the output signals (IOB□_Y0 to IOB□_Y7) after output signal selection (after selection by the oport_iob0y_osel register), or output signals (IOE□_Y0 to IOE□_Y7) to the output signals (IOE□_Y0 to IOE□_Y7) after output signal selection (after selection by the oport_ioe0y_osel register) is not output outside the module.
- When a DC I/O circuit board is connected to B□ or E□, the settings are disabled.
- When an analog I/O circuit board is connected to E□, the settings are disabled.

FPGA register details (analog input control part)

A/D conversion enable/disable setting

■Address

Name	FPGA register address
A/D conversion enable/disable setting (aiport_ad_start)	1000_6000H

■Description

Enable or disable A/D conversion.

The firmware sets the A/D conversion enable/disable setting value to A/D conversion start as FPGA control start processing, and A/D conversion starts. Therefore, A/D conversion start setting is not required.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)									(6)	(5)	(4)	0 (fixed)	(3)	(2)	(1)

(1) A/D conversion enable/disable setting (E0)
- 1: Conversion-enable
- 0: Conversion-disable

(2) A/D conversion enable/disable setting (E1)
- 1: Conversion-enable
- 0: Conversion-disable

(3) A/D conversion enable/disable setting (E2)
- 1: Conversion-enable
- 0: Conversion-disable

(4) A/D conversion start/stop setting
- 1: Start
- 0: Stop

(5) A/D conversion start/stop setting
- 1: Start
- 0: Stop

(6) A/D conversion start/stop setting
- 1: Start
- 0: Stop

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.

A/D conversion timing selection

■Address

Name	FPGA register address
A/D conversion timing selection (aiport_ad_cyc_sel)	1000_6002H

■Description

Select the A/D conversion timing of ADC.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) A/D conversion timing selection (E0)
- 1: User circuit output*1
- 0: Data sampling timing*2

(2) A/D conversion timing selection (E1)
- 1: User circuit output*1
- 0: Data sampling timing*2

(3) A/D conversion timing selection (E2)
- 1: User circuit output*1
- 0: Data sampling timing*2

*1 User circuit part sampling pulse (uc_sampling_tmgpulse_clk100m_reg) is used to perform A/D conversion.

*2 A/D conversion is performed at the cycle set by the data sampling timing (tim_iob0x_en).

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.

ADC voltage/current input setting

■Address

Name	FPGA register address
ADC voltage/current input setting (E0) (aiport_ade0_vi_set)	1000_6008H
ADC voltage/current input setting (E1) (aiport_ade1_vi_set)	1000_600AH
ADC voltage/current input setting (E2) (aiport_ade2_vi_set)	1000_600CH

■Description

Set the ADC voltage/current range for each CH.

The firmware automatically performs the settings according to the ADC range setting CH0 to 3 (E0) (aiport_ade0_0-3_range) (FPGA register address: 1000_6100H) to ADC range setting CH8 to B (E2) (aiport_ade2_8-B_range) (FPGA register address: 1000_6110H).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)				CHB	CHA	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- 1: Current input
- 0: Voltage input

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E☐, the settings are disabled.

A/D conversion value

■Address

Name	FPGA register address
A/D conversion value CH0 (E0) (aiport_ade0_0_result) to A/D conversion value CHB (E0) (aiport_ade0_b_result)	1000_6010H to 1000_6026H
A/D conversion value CH0 (E1) (aiport_ade1_0_result) to A/D conversion value CHB(E1) (aiport_ade1_b_result)	1000_6030H to 1000_6046H
A/D conversion value CH0 (E2) (aiport_ade2_0_result) to A/D conversion value CHB (E2) (aiport_ade2_b_result)	1000_6050H to 1000_6066H

■Description

The A/D conversion value for E☐ can be checked.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E☐, the settings are disabled.

ADC range setting

■Address

Name	FPGA register address
ADC range setting CH0 to 3 (E0) (aiport_ade0_0-3_range)	1000_6100H
ADC range setting CH4 to 7 (E0) (aiport_ade0_4-7_range)	1000_6102H
ADC range setting CH8 to B (E0) (aiport_ade0_8-B_range)	1000_6104H
ADC range setting CH0 to 3 (E1) (aiport_ade1_0-3_range)	1000_6106H
ADC range setting CH4 to 7 (E1) (aiport_ade1_4-7_range)	1000_6108H
ADC range setting CH8 to B (E1) (aiport_ade1_8-B_range)	1000_610AH
ADC range setting CH0 to 3 (E2) (aiport_ade2_0-3_range)	1000_610CH
ADC range setting CH4 to 7 (E2) (aiport_ade2_4-7_range)	1000_610EH
ADC range setting CH8 to B (E2) (aiport_ade2_8-B_range)	1000_6110H

■Description

Sets the ADC range.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CH3 ADC range setting (E□)				CH2 ADC range setting (E□)				CH1 ADC range setting (E□)				CH0 ADC range setting (E□)			
CH7 ADC range setting (E□)				CH6 ADC range setting (E□)				CH5 ADC range setting (E□)				CH4 ADC range setting (E□)			
CHB ADC range setting (E□)				CHA ADC range setting (E□)				CH9 ADC range setting (E□)				CH8 ADC range setting (E□)			

- 0H: -19.8 to 19.8mA
- 2H: -9.9 to 9.9V

■FPGA initial value

3H

■Firmware initial value

2H

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.

The FPGA initial value 3H is the system initial value. Set 0H or 2H when setting the range.

ADC oversampling ratio setting

■Address

Name	FPGA register address
ADC oversampling ratio setting (E0) (aiport_ade0_oversamp)	1000_6120H
ADC oversampling ratio setting (E1) (aiport_ade1_oversamp)	1000_6122H
ADC oversampling ratio setting (E2) (aiport_ade2_oversamp)	1000_6124H

■Description

Sets the ADC oversampling ratio.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												(1)			

(1) ADC oversampling ratio setting (E□)

- 9H to FH: No Setting
- 8H: 256x oversampling
- 7H: 128x oversampling
- 6H: 64x oversampling
- 5H: 32x oversampling
- 4H: 16x oversampling
- 3H: 8x oversampling
- 2H: 4x oversampling
- 1H: 2x oversampling
- 0H: No Setting

■FPGA initial value

0H

■Firmware initial value

0H

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.
- The values that can be set differ depending on the set value of the data sampling timing. Set to satisfy the following.

ADC oversampling ratio setting	Setting range of data sampling timing
No Setting	4μs or more
2x	6μs or more
4x	8μs or more
8x	13μs or more
16x	24μs or more
32x	44μs or more
64x	84μs or more
128x	165μs or more
256x	328μs or more

ADC offset setting value

■Address

Name	FPGA register address
ADC offset setting value CH0 to 1 (E0) (aiport_ade0_0-1_offset) to ADC offset setting value CHA to B (E0) (aiport_ade0_a-b_offset)	1000_6160H to 1000_616AH
ADC offset setting value CH0 to 1 (E1) (aiport_ade1_0-1_offset) to ADC offset setting value CHA to B (E1) (aiport_ade1_a-b_offset)	1000_616CH to 1000_6176H
ADC offset setting value CH0 to 1 (E2) (aiport_ade2_0-1_offset) to ADC offset setting value CHA to B (E2) (aiport_ade2_a-b_offset)	1000_6178H to 1000_6182H

■Description

Adds/subtracts the ADC offset value to/from the A/D conversion value of each CH.

The value obtained by adding -128 to 127 to the A/D conversion value inside the ADC is stored in the A/D conversion value CH0 (E0) (aiport_ade0_0_result) (FPGA register address: 1000_6010H) to A/D conversion value CHB (E2) (aiport_ade2_b_result) (FPGA register address: 1000_6066H).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CH1 ADC offset value (E□)								CH0 ADC offset value (E□)							
CH3 ADC offset value (E□)								CH2 ADC offset value (E□)							
CH5 ADC offset value (E□)								CH4 ADC offset value (E□)							
CH7 ADC offset value (E□)								CH6 ADC offset value (E□)							
CH9 ADC offset value (E□)								CH8 ADC offset value (E□)							
CHB ADC offset value (E□)								CHA ADC offset value (E□)							

The value obtained by adding -128 to 127 to the A/D conversion value inside the ADC is stored in the A/D conversion value CH0 (E0) (aiport_ade0_0_result) (FPGA register address: 1000_6010H) to A/D conversion value CHB (E2) (aiport_ade2_b_result) (FPGA register address: 1000_6066H). (Setting value: The value added to the A/D conversion value)

- FFH: 127
- 80H: No offset
- 00H: -128

■FPGA initial value

80H

■Firmware initial value

80H

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.

FPGA register details (analog output control part)

D/A conversion enable/disable setting

■Address

Name	FPGA register address
D/A conversion enable/disable setting (aoport_da_start)	1000_7000H

■Description

Enables or disables D/A conversion.

The firmware reads this setting during FPGA control start processing and sets the DAC.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(6)	(5)	(4)	(3)	(2)	(1)

(1) CH0 D/A conversion enable/disable setting (E0)
- 1: Conversion-enable
- 0: Conversion-disable

(2) CH1 D/A conversion enable/disable setting (E0)
- 1: Conversion-enable
- 0: Conversion-disable

(3) CH0 D/A conversion enable/disable setting (E1)
- 1: Conversion-enable
- 0: Conversion-disable

(4) CH1 D/A conversion enable/disable setting (E1)
- 1: Conversion-enable
- 0: Conversion-disable

(5) CH0 D/A conversion enable/disable setting (E2)
- 1: Conversion-enable
- 0: Conversion-disable

(6) CH1 D/A conversion enable/disable setting (E2)
- 1: Conversion-enable
- 0: Conversion-disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.

D/A conversion value selection

■Address

Name	FPGA register address
D/A conversion value selection (aoport_da_data_sel)	1000_7002H

■Description

Selects the D/A conversion value to output to DAC.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(6)	(5)	(4)	(3)	(2)	(1)

(1) CH0 D/A conversion value setting selection (E0)
- 1: User circuit output*1
- 0: Register setting value*2

(2) CH1 D/A conversion value setting selection (E0)
- 1: User circuit output*1
- 0: Register setting value*2

(3) CH0 D/A conversion value setting selection (E1)
- 1: User circuit output*1
- 0: Register setting value*2

(4) CH1 D/A conversion value setting selection (E1)
- 1: User circuit output*1
- 0: Register setting value*2

(5) CH0 D/A conversion value setting selection (E2)
- 1: User circuit output*1
- 0: Register setting value*2

(6) CH1 D/A conversion value setting selection (E2)
- 1: User circuit output*1
- 0: Register setting value*2

*1 Select the D/A conversion value CH△ (E□) (uc_ioe□_andat_clk100m_reg) from the user circuit part.

*2 Select D/A conversion value CH△ (E□) (aoport_dae□_△_data) (FPGA register address: 1000_7100H to 1000_710AH).

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

- Changes to this register when b0 of internal operation start/stop (mode_ctrl2) (FPGA register address: 1000_0002H) is stopped (0) are immediately reflected.
- When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.
- Set CH0 and CH1 to the same setting value.
- If register setting value (0) is set, set the following for each circuit board.

Item	Description
D/A conversion timing selection (aoport_da_cyc_sel)	Data update timing
DAC LDAC signal selection (aoport_da_ldac_sel)	Fixed to Low

- When setting the user circuit output (1), set the following for each circuit board.

Item	Description
D/A conversion timing selection (aoport_da_cyc_sel)	User circuit output
DAC LDAC signal selection (aoport_da_ldac_sel)	User circuit output

D/A conversion timing selection

■Address

Name	FPGA register address
D/A conversion timing selection (aoport_da_cyc_sel)	1000_7004H

■Description

Selects the D/A conversion timing of DAC.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) D/A conversion timing selection (E0)
- 1: User circuit output*1
- 0: Data update timing*2

(2) D/A conversion timing selection (E1)
- 1: User circuit output*1
- 0: Data update timing*2

(3) D/A conversion timing selection (E2)
- 1: User circuit output*1
- 0: Data update timing*2

*1 Perform the D/A conversion with D/A conversion value enable (E□) (uc_ioe□andat_en_clk100m_reg) from the user circuit part.

*2 D/A conversion is performed at the cycle set by the data update timing.

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.
- If data update timing (0) is set, set the following for each circuit board.

Item	Description
D/A conversion value selection (aoport_da_data_sel)	Register setting value
DAC LDAC signal selection (aoport_da_ldac_sel)	Fixed to Low

- When setting the user circuit output (1), set the following for each circuit board.

Item	Description
D/A conversion value selection (aoport_da_data_sel)	User circuit output
DAC LDAC signal selection (aoport_da_ldac_sel)	User circuit output

DAC LDAC signal selection

■Address

Name	FPGA register address
DAC LDAC signal selection (aoport_da_ldac_sel)	1000_7006H

■Description

Selects the LDAC signal to output to DAC.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(6)	(5)	(4)	(3)	(2)	(1)

(1) CH0 DAC LDAC signal selection (E0)
- 1: User circuit output*1
- 0: Fixed to Low*2

(2) CH1 DAC LDAC signal selection (E0)
- 1: User circuit output*1
- 0: Fixed to Low*2

(3) CH0 DAC LDAC signal selection (E1)
- 1: User circuit output*1
- 0: Fixed to Low*2

(4) CH1 DAC LDAC signal selection (E1)
- 1: User circuit output*1
- 0: Fixed to Low*2

(5) CH0 DAC LDAC signal selection (E2)
- 1: User circuit output*1
- 0: Fixed to Low*2

(6) CH1 DAC LDAC signal selection (E2)
- 1: User circuit output*1
- 0: Fixed to Low*2

*1 LDAC output (E☐) (uc_ioe☐_ldac_clk100m_reg) from the user circuit part is output.

*2 D/A conversion is performed for each channel at the cycle set by the data update timing.

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

- When a DC I/O circuit board or Differential I/O circuit board is connected to E☐, the settings are disabled.
- Set CH0 and CH1 to the same setting value.
- When setting to Fixed to Low (0), set the following for each circuit board.

Item	Description
D/A conversion value selection (aoport_da_data_sel)	Register setting value
D/A conversion timing selection (aoport_da_cyc_sel)	Data update timing

- When setting the user circuit output (1), set the following for each circuit board.

Item	Description
D/A conversion value selection (aoport_da_data_sel)	User circuit output
D/A conversion timing selection (aoport_da_cyc_sel)	User circuit output

D/A conversion value

■Address

Name	FPGA register address
D/A conversion value CH0 (E0) (aoport_dae0_0_data)	1000_7100H
D/A conversion value CH1 (E0) (aoport_dae0_1_data)	1000_7102H
D/A conversion value CH0 (E1) (aoport_dae1_0_data)	1000_7104H
D/A conversion value CH1 (E1) (aoport_dae1_1_data)	1000_7106H
D/A conversion value CH0 (E2) (aoport_dae2_0_data)	1000_7108H
D/A conversion value CH1 (E2) (aoport_dae2_1_data)	1000_710AH

■Description

The value transferred to DAC and converted to D/A.

■FPGA initial value

0000H

■Firmware initial value

8000H

■Reset cause

Reset

■Precautions and restrictions

- When D/A conversion value selection (aoport_da_data_sel) (FPGA register address: 1000_7002H) is set to user circuit output (1), the setting is disabled.
- When a DC I/O circuit board or Differential I/O circuit board is connected to E□, the settings are disabled.
- Upon completion of the configuration, the following values are stored according to the DAC range setting CH□(E□) stored in the non-volatile memory.

Range	Value
-9.9 to 9.9V	8000H
0.2 to 19.8mA	0000H

FPGA register details (logging part)

Logging operation control register

■Address

Name	FPGA register address
Logging operation control register (lgdw_ctrl)	1000_9000H

■Description

Configure and control the logging operation. The firmware controls.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)		(9)	(8)	0 (fixed)	(7)	(6)	(5)	0 (fixed)				(4)	(3)	(2)	(1)

(1) Start logging
- 1: Start logging (write enabled)
- 0: Stop logging (write disabled)

(2) Suspend logging
- 1: Suspend (write disabled)
- 0: Operating (write enabled)

(3) Disable logging stop
- 1: Ignore stop by logging start operation
- 0: Can be stopped by logging start operation

(4) Logging control trigger
- 1: Rising for logging start allowed
- 0: Logging start falling edge enable

(5) Logging operation mode
- 1: Trigger operation mode
- 0: Storage operation mode

(6) Buffer operation in storage operation mode*2
- 1: Ring buffer operation
- 0: Linear buffer operation

(7) Automatic transfer mode (logging part)
- 1: Automatic transfer mode enabled
- 0: Automatic transfer mode disabled

(8) Select logging start control
- 1: Register setting value (RY3)

The b0 of the logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) is operated from the remote output signal (RY3).
- 0: User circuit output

Select the logging enable (uc_logen_clk100m_reg) from the user circuit part.

(9) Select sampling pulses
- 1: User circuit output

Logging is performed with the user sampling pulse (uc_loguserpulse_clk100m_reg) from the user circuit part.
- 0: Logging cycle timing

Logging is performed at the cycle set by the logging cycle timing (tim_log_cyc) (FPGA register address: 1000_2200H).

*1 The trigger operation mode is always the ring buffer operation.

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

■Precautions and restrictions

When b0 of the user circuit logging mode selection (usr_logmode_sel) (FPGA register address: 1000_A002H) is set to time division mode (1), only the user circuit output (1) can be used for the sampling pulse selection and logging start control selection.

Logging state register

■Address

Name	FPGA register address
Logging state register (lgdw_sts)	1000_9002H

■Description

The status of the logging part can be checked.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)					(5)	0 (fixed)	(4)	0 (fixed)		(3)	(2)	0 (fixed)			(1)

(1) Start logging (user circuit)
- 1: Start logging (write enabled)
- 0: Stop logging (write disabled)

(2) Logging status
- 1: Logging enabled
- 0: Logging disabled

(3) Logging status (suspended)
- 1: Suspended
- 0: Operating

(4) Logging operation end flag*1
- 1: Stops when the logging end condition is met during logging operation
- 0: Logging end condition is not met

(5) Logging trigger status flag*2
- 1: When trigger mode is set, a trigger occurs during logging operation
- 0: No trigger occurred during logging operation

*1 Cleared when logging starts. It is also cleared by setting b8 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.

*2 Cleared when logging starts.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

A

Logging system flag

■Address

Name	FPGA register address
Logging system flag (lgdw_sys_sts)	1000_9004H

■Description

The status of the logging system flag can be checked.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(9)	(8)	(7)	(6)	0 (fixed)						(5)	(4)	0 (fixed)	(3)	(2)	(1)

(1) Current status of buffer (FIFO) full
- 1: Full
- 0: Not full

(2) Current status of buffer (FIFO) almost full (75% full)
- 1: Almost full
- 0: Not almost full

(3) Current status of buffer (FIFO) empty
- 1: Empty
- 0: Not empty

(4) Buffer (FIFO) full detection flag*1
- 1: Full detected in the past
- 0: Full has not occurred

(5) Buffer (FIFO) almost full (75% full) detection flag*2
- 1: Almost full detected in the past
- 0: Almost full has not occurred

(6) User sampling pulse cycle error (less than cycle 1μs)*3
- 1: Cycle error was detected in the past
- 0: Cycle error has not occurred

(7) Logging control violation flag rising edge*4
- 1: Violation
- 0: No violation

(8) Logging control violation flag falling edge*5
- 1: Violation
- 0: No violation

(9) Logging stop flag*6
- 1: Logging start stopped during logging operation
- 0: Logging start is not stopped during logging operation

*1 The flag is cleared by setting b4 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.
*2 The flag is cleared by setting b5 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.
*3 The flag is cleared by setting b12 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.
*4 The flag is cleared by setting b13 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.
*5 The flag is cleared by setting b14 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.
*6 The flag is cleared by setting b15 in the flag clear register (lgdw_flag_clr) (FPGA register address: 1000_9006H) to 1.

■FPGA initial value

0004H

■Firmware initial value

—

■Reset cause

Reset

Flag clear register

■Address

Name	FPGA register address
Flag clear register (lgdw_flag_clr)	1000_9006H

■Description

Clears the logging state register and logging system flags.

All bits of the flag clear register are cleared by writing 1 to the corresponding bit. 0 is always read when reading.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(7)	(6)	(5)	(4)	0 (fixed)			(3)	0 (fixed)		(2)	(1)	0 (fixed)			

(1) Clears the buffer (FIFO) full detection flag (b4) of the logging system flag (lgdw_sys_sts).
(2) Clears the buffer (FIFO) almost full (75% full) detection flag (b5) of the logging system flag (lgdw_sys_sts).
(3) Clears the logging operation end flag (b8) of logging state register (lgdw_sts).
(4) Clears the user sampling pulse cycle error (less than 1μs) (b12) of the logging system flag (lgdw_sys_sts).
(5) Clears the logging control violation flag rising edge (b13) of the logging system flag (lgdw_sys_sts).
(6) Clears the logging control violation flag falling edge (b14) of the logging system flag (lgdw_sys_sts).
(7) Clears the logging stop flag (b15) of the logging system flag (lgdw_sys_sts).

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Logging data size setting

■Address

Name	FPGA register address
Logging data size setting (lgdw_area)	1000_9008H

■Description

Sets a size for storing the logging data.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												Logging data size			

- 0H: 256 records (16kB) (last address: 0000_3FFFH)
- 1H: 512 records (32kB) (last address: 0000_7FFFH)
- 2H: 1024 records (64kB) (last address: 0000_FFFFH)
- 3H: 2048 records (128kB) (last address: 0001_FFFFH)
- 4H: 4096 records (256kB) (last address: 0003_FFFFH)
- 5H: 8192 records (512kB) (last address: 0007_FFFFH)
- 6H: 16384 records (1024kB) (last address: 000F_FFFFH)
- 7H: 32768 records (2MB) (last address: 001F_FFFFH)
- 8H: 65536 records (4MB) (last address: 003F_FFFFH)
- 9H: 131072 records (8MB) (last address: 007F_FFFFH)
- AH: 262144 records (16MB) (last address: 00FF_FFFFH)
- BH: 524288 records (32MB) (last address: 01FF_FFFFH)

■FPGA initial value

FH

■Firmware initial value

4H

■Reset cause

Reset

Time information

■Address

Name	FPGA register address
Time information (year) (lgdw_clock_rddata1)	1000_9030H
Time information (month, day, hour) (lgdw_clock_rddata2)	1000_9032H
Time information (minutes, seconds) (lgdw_clock_rddata3)	1000_9034H
Time information (ms) (lgdw_clock_rddata4)	1000_9036H
Time information (μs) (lgdw_clock_rddata5)	1000_9038H

■Description

Time information. Read data (data added in the logging part)

FPGA register address	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
1000_9030H*1	0 (fixed)									Time information (year: 0 to 127)						
1000_9032H*2	0 (fixed)		Time information (month: 1 to 12)				Time information (Day: 1 to 31)					Time information (hour: 0 to 23)				
1000_9034H*2	0 (fixed)		Time information (minutes: 0 to 59)						0 (fixed)		Time information (seconds: 0 to 59)					
1000_9036H*2	0 (fixed)						Time information (ms: 0 to 999)									
1000_9038H*2	0 (fixed)						Time information (μs: 0 to 999)									

*1 Shows the offset from 1970.

*2 To prevent data inconsistency, it is fixed when the time information (year) (lgdw_clock_rddata1) is read.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Set number of sampling after trigger

■Address

Name	FPGA register address
Set number of sampling after trigger (lower side) (lgdw_triggered_lsample)	1001_9000H
Set number of sampling after trigger (upper side) (lgdw_triggered_usample)	1001_9002H

■Description

Sets the number of times logging occurs after trigger input.

FPGA register address	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
1001_9000H	Set number of sampling after trigger (lower side)															
1001_9002H	0 (fixed)															
	Set number of sampling after trigger (upper side)															

■FPGA initial value

0000H

■Firmware initial value

0001H

■Reset cause

Reset

■Precautions and restrictions

- If b8 of the logging operation control register (lgdw_ctrl) (FPGA register address: 1000_9000H) is in storage operation mode (0), the setting is disabled.
- 1 to (the number of records set in the logging data size setting (lgdw_area) (FPGA register address: 1000_9008H) - 1) can be set.

A

Number of samplings

■Address

Name	FPGA register address
Number of samplings (lower) (lgdw_sample_lcount)	1001_9004H
Number of samplings (upper) (lgdw_sample_ucount)	1001_9006H

■Description

The number of samplings of logging data can be checked.

Point

- It does not count beyond FFFF_FFFFH.
- Cleared when logging starts.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

FPGA register details (user circuit)

Write/read data control register

■Address

Name	FPGA register address
Write/read data control register (usr_wrdat_ctrl)	1000_A000H

■Description

The firmware controls this register and transfers data to the user circuit.

- When 1 is written to write data control (transient area/cyclic area) and read data control (transient area/cyclic area), it is automatically cleared by hardware.
- When 1 is written to the write data control (transient area), the write data area (FPGA register address: 1000_B000H to 1000_B2FFH) is reflected in the user circuit.
- When 1 is written to the write data control (cyclic area), the write data area (FPGA register address: 1000_B300H to 1000_B3FFH) is reflected in the user circuit.
- When 1 is written to the read data control (transient area), the data from the user circuit is reflected in the read data area (FPGA register address: 1000_B800H to 1000_BAFFH).
- When 1 is written to the read data control (cyclic area), the data from the user circuit is reflected in the read data area (FPGA register address: 1000_BB00H to 1000_BBFFH).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)						(4)	(3)	0 (fixed)						(2)	(1)

(1) Write data control (transient area)
- 1: Enable
- 0: Disable

(2) Write data control (cyclic area)
- 1: Enable
- 0: Disable

(3) Read data control (transient area)
- 1: Enable
- 0: Disable

(4) Read data control (cyclic area)
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

Write data (transient area) (FPGA register address: 1000_B000H to 1000_B2FFH) and write data (cyclic area) (FPGA register address: 1000_B300H to 1000_B3FFH) can also be read from and written to unused areas.

User circuit logging mode selection

■Address

Name	FPGA register address
User circuit logging mode selection (usr_logmode_sel)	1000_A002H

■Description

Sets the non-time division/time division mode (time division enabled/disabled).

- Non-time division mode (time division disabled): Logs 512-bit (1 record) data together with time information for each sampling.
- Time division mode (time division enabled): Logs 1024-bit (2 records) data together with time information for each sampling.

When logging the A/D conversion value using the time division mode (time division enabled) in the sample circuit, set one of the following to the logging control part sampling pulse signal selection (usr_wreg_093) (FPGA register address: 1000_B126H) from the user circuit part parameter setting. Logging is performed at the set circuit board A/D conversion timing.

- 15H: A/D conversion value enable(E0)
- 16H: A/D conversion value enable(E1)
- 17H: A/D conversion value enable(E2)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) Time division enable/disable
- 1: Enable
- 0: Disable

(2) Reserve

Point

The b1 is the firmware control area. FPGA operation does not change.

■FPGA initial value

00

■Firmware initial value

00

■Reset cause

Reset

■Precautions and restrictions

- When time division is enabled (1), set as follows.

Item	Description
Select logging start control	User circuit output
Select sampling pulses	User circuit output
Logging data file storage type	Binary file

MCU system error notification

■Address

Name	FPGA register address
MCU system error notification (usr_micon_syserr)	1000_A004H

■Description

This register notifies the system error from the microcomputer to FPGA. Since this is a register for future extension, the setting cannot be changed from No error (0).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) MCU system error notification
- 1: Error exists
- 0: No error

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

A

Always write register 0

■Address

Name	FPGA register address
Always write register 0 (usr_alwreg_00)	1000_A010H

■Description

Stores the value to be output to the user circuit when "USER switch enable/disable" is "disable".

Stores the states of function setting switches 7 to 10 when "User switch enable/disable" is "enable".

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												(4)	(3)	(2)	(1)

(1) Function setting switch 10
- 1: ON
- 0: OFF

(2) Function setting switch 9
- 1: ON
- 0: OFF

(3) Function setting switch 8
- 1: ON
- 0: OFF

(4) Function setting switch 7
- 1: ON
- 0: OFF

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

■Precautions and restrictions

When "User switch enable/disable" is "enable", writing by the FPGA register access function is not possible.

Always write register areas 1 to 12

■Address

Name	FPGA register address
Always write register 1 (usr_alwreg_01) to Constant write register 12 (usr_alwreg_0C)	1000_A012H to 1000_A029H

■Description

Stores the value to be output to the user circuit.

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 13

■Address

Name	FPGA register address
Always write register 13 (usr_alwreg_0D)	1000_A02AH

■Description

Stores the value to be output to the user circuit, and the status for each synchronization cycle of the master station when using the CC-Link IE TSN network synchronous communication function.

- 1: With synchronization signal
- 0: Without synchronization signal

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(16)	(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)

(13) CC-Link IE TSN network synchronization signal 12
(14) CC-Link IE TSN network synchronization signal 13
(15) CC-Link IE TSN network synchronization signal 14
(16) CC-Link IE TSN network synchronization signal 15
(9) CC-Link IE TSN network synchronization signal 8
(10) CC-Link IE TSN network synchronization signal 9
(11) CC-Link IE TSN network synchronization signal 10
(12) CC-Link IE TSN network synchronization signal 11
(5) CC-Link IE TSN network synchronization signal 4
(6) CC-Link IE TSN network synchronization signal 5
(7) CC-Link IE TSN network synchronization signal 6
(8) CC-Link IE TSN network synchronization signal 7
(1) CC-Link IE TSN network synchronization signal 0
(2) CC-Link IE TSN network synchronization signal 1
(3) CC-Link IE TSN network synchronization signal 2
(4) CC-Link IE TSN network synchronization signal 3

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 14

■Address

Name	FPGA register address
Always write register 14 (usr_alwreg_0E)	1000_A02CH

■Description

Stores the value to be output to the user circuit, and clears the rising/falling edge of the logging control violation flag.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(3)														(2)	(1)

(1) Logging control violation flag rising edge clear
- 1: Clear

(2) Logging control violation flag falling edge clear
- 1: Clear

(3) Read/write register for user circuit

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 15

■Address

Name	FPGA register address
Always write register 15 (usr_alwreg_0F)	1000_A02EH

■Description

The statuses of the logging data FTP transfer and FPGA control processing can be checked.

By checking the status of FPGA control processing, it can be used as the timing to start LDAC output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(2)		(1)

(1) Status of FPGA control start processing[*1]
- 1: Start processing completed
- 0: In process of stopping or starting

(2) Logging data FTP transfer status[*2]
- 11: Transfer completed (failed)
- 10: Transfer completed (success)
- 01: Transferring
- 00: Before starting transfer

*1 When FPGA control is stopped, it will be "In process of stopping or starting" (0).

*2 After the transfer is completed, "Before starting transfer" (00) is stored when the next logging starts.

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

Writing cannot be made by the FPGA register access function.

Always read register

■Address

Name	FPGA register address
Always read register (usr_alrreg_00 to usr_alrreg_0F)	1000_A030H to 1000_A04FH

■Description

Stores the signal from the user circuit.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Write data

■Address

Name	FPGA register address
Writing data (transient area) (usr_wreg_000 to usr_wreg_17F)	1000_B000H to 1000_B2FFH
Writing data (cyclic area) (usr_wreg_180 to usr_wreg_1FF)	1000_B300H to 1000_B3FFH

■Description

Stores the value to be output to the user circuit.

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Read Data

■Address

Name	FPGA register address
Read data (transient area) (usr_rreg_000 to usr_rreg_17F)	1000_B800H to 1000_BAFFH
Read data (cyclic area) (usr_rreg_180 to usr_rreg_1FF)	1000_BB00H to 1000_BBFFH

■Description

Stores the signal from the user circuit.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

FPGA register details (sample circuit register)

The following functions are implemented to control the circuit to be implemented in the sample circuit.

- Always write register
- Always read register
- Write data
- Read Data

Write/read data control register

■Address

Name	FPGA register address
Write/read data control register (usr_wrdat_ctrl)	1000_A000H

■Description

The firmware controls this register and transfers data to the user circuit.

- When 1 is written to write data control (transient area/cyclic area) and read data control (transient area/cyclic area), it is automatically cleared by hardware.
- When 1 is written to the write data control (transient area), the write data area (remote register address: 1000_B000H to 1000_B2FFH) is reflected in the user circuit.
- When 1 is written to the write data control (cyclic area), the write data area (remote register address: 1000_B300H to 0_B3FFH) is reflected in the user circuit.
- When 1 is written to the read data control (transient area), the data from the user circuit is reflected in the read data area (remote register address: 1000_B800H to 1000_BAFFH).
- When 1 is written to the read data control (cyclic area), the data from the user circuit is reflected in the read data area (remote register address: 1000_BB00H to 1000_BBFFH).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)						(4)	(3)	0 (fixed)						(2)	(1)

(1) Write data control (transient area)
- 1: Enable
- 0: Disable

(2) Write data control (cyclic area)
- 1: Enable
- 0: Disable

(3) Read data control (transient area)
- 1: Enable
- 0: Disable

(4) Read data control (cyclic area)
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

Write data (transient area) (FPGA register address: 1000_B000H to 1000_B2FFH) and write data (cyclic area) (FPGA register address: 1000_B300H to 1000_B3FFH) can also be read from and written to unused areas.

User circuit logging mode selection

■Address

Name	FPGA register address
User circuit logging mode selection (usr_logmode_sel)	1000_A002H

■Description

Sets the non-time division/time division mode (time division enabled/disabled).

- Non-time division mode (time division disabled): Logs 512-bit (1 record) data together with time information for each sampling.
- Time division mode (time division enabled): Logs 1024-bit (2 records) data together with time information for each sampling.

When logging the A/D conversion value using the time division mode (time division enabled) in the sample circuit, set one of the following to the logging control part sampling pulse signal selection (usr_wreg_093) (FPGA register address: 1000_B126H) from the user circuit part parameter setting. Logging is performed at the set circuit board A/D conversion timing.

- 15H: A/D conversion value enable(E0)
- 16H: A/D conversion value enable(E1)
- 17H: A/D conversion value enable(E2)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) Time division enable/disable
- 1: Enable
- 0: Disable

(2) Reserve

Point

The b1 is the firmware control area. FPGA operation does not change.

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

- When time division is enabled (1), set as follows.

Item	Description
Select logging start control	User circuit output
Select sampling pulses	User circuit output
Logging data file storage type	Binary file

A

MCU system error notification

■Address

Name	FPGA register address
MCU system error notification (usr_micon_syserr)	1000_A004H

■Description

This register notifies the system error from the microcomputer to FPGA. Since this is a register for future extension, the setting cannot be changed from No error (0).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) MCU system error notification
- 1: Error exists
- 0: No error

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Always write register 0

■Address

Name	FPGA register address
Always write register 0 (usr_alwreg_00)	1000_A010H

■Description

Stores the value to be output to the user circuit when "USER switch enable/disable" is "disable".
Stores the states of function setting switches 7 to 10 when "User switch enable/disable" is "enable".

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												(4)	(3)	(2)	(1)

(1) Function setting switch 10
- 1: ON
- 0: OFF

(2) Function setting switch 9
- 1: ON
- 0: OFF

(3) Function setting switch 8
- 1: ON
- 0: OFF

(4) Function setting switch 7
- 1: ON
- 0: OFF

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

■Precautions and restrictions

When "User switch enable/disable" is "enable", writing by the FPGA register access function is not possible.

Always write register areas 1 to 12

■Address

Name	FPGA register address
Always write register 1 (usr_alwreg_01) to Constant write register 12 (usr_alwreg_0C)	1000_A012H to 1000_A029H

■Description

Stores the value to be output to the user circuit.

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 13

■Address

Name	FPGA register address
Always write register 13 (usr_alwreg_0D)	1000_A02AH

■Description

Stores the value to be output to the user circuit, and the status for each synchronization cycle of the master station when using the CC-Link IE TSN network synchronous communication function.

- 1: With synchronization signal
- 0: Without synchronization signal

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(16)	(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)

(13) CC-Link IE TSN network synchronization signal 12
(14) CC-Link IE TSN network synchronization signal 13
(15) CC-Link IE TSN network synchronization signal 14
(16) CC-Link IE TSN network synchronization signal 15
(9) CC-Link IE TSN network synchronization signal 8
(10) CC-Link IE TSN network synchronization signal 9
(11) CC-Link IE TSN network synchronization signal 10
(12) CC-Link IE TSN network synchronization signal 11
(5) CC-Link IE TSN network synchronization signal 4
(6) CC-Link IE TSN network synchronization signal 5
(7) CC-Link IE TSN network synchronization signal 6
(8) CC-Link IE TSN network synchronization signal 7
(1) CC-Link IE TSN network synchronization signal 0
(2) CC-Link IE TSN network synchronization signal 1
(3) CC-Link IE TSN network synchronization signal 2
(4) CC-Link IE TSN network synchronization signal 3

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 14

■Address

Name	FPGA register address
Always write register 14 (usr_alwreg_0E)	1000_A02CH

■Description

Stores the value to be output to the user circuit, and clears the rising/falling edge of the logging control violation flag.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(3)														(2)	(1)

(1) Logging control violation flag rising edge clear
- 1: Clear

(2) Logging control violation flag falling edge clear
- 1: Clear

(3) Read/write register for user circuit

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Always write register 15

■Address

Name	FPGA register address
Always write register 15 (usr_alwreg_0F)	1000_A02EH

■Description

The statuses of the logging data FTP transfer and FPGA control processing can be checked.

By checking the status of FPGA control processing, it can be used as the timing to start LDAC output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(2)		(1)

(1) Status of FPGA control start processing*1
- 1: Start processing completed
- 0: In process of stopping or starting

(2) Logging data FTP transfer status*2
- 11: Transfer completed (failed)
- 10: Transfer completed (success)
- 01: Transferring
- 00: Before starting transfer

*1 When FPGA control is stopped, it will be "In process of stopping or starting" (0).

*2 After the transfer is completed, "Before starting transfer" (00) is stored when the next logging starts.

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

■Precautions and restrictions

Writing cannot be made by the FPGA register access function.

Always read register 0

■Address

Name	FPGA register address
Always read register 0 (usr_alrreg_00)	1000_A030H

■Description

The signal from the user circuit is stored when "USER switch enable/disable" is "disable".

Stores the states of function setting switches 7 to 10 when "User switch enable/disable" is "enable".

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)												(4)	(3)	(2)	(1)

(1) Function setting switch 10
- 1: ON
- 0: OFF

(2) Function setting switch 9
- 1: ON
- 0: OFF

(3) Function setting switch 8
- 1: ON
- 0: OFF

(4) Function setting switch 7
- 1: ON
- 0: OFF

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

When "User switch enable/disable" is "enable", writing by the FPGA register access function is not possible.

Always read register areas 1 to 12

■Address

Name	FPGA register address
Always read register areas 1 to 12 (usr_alrreg_01 to usr_alrreg_0C)	1000_A032H to 1000_A048H

■Description

Stores the signal from the user circuit.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Always read register 13

■Address

Name	FPGA register address
Always read register 13 (usr_alwreg_0D)	1000_A04AH

■Description

Stores the signal from the user circuit, and the status for each synchronization cycle of the master station when using the CC-Link IE TSN network synchronous communication function.

- 1: With synchronization signal
- 0: Without synchronization signal

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(16)	(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)

(13) CC-Link IE TSN network synchronization signal 12
(14) CC-Link IE TSN network synchronization signal 13
(15) CC-Link IE TSN network synchronization signal 14
(16) CC-Link IE TSN network synchronization signal 15
(9) CC-Link IE TSN network synchronization signal 8
(10) CC-Link IE TSN network synchronization signal 9
(11) CC-Link IE TSN network synchronization signal 10
(12) CC-Link IE TSN network synchronization signal 11
(5) CC-Link IE TSN network synchronization signal 4
(6) CC-Link IE TSN network synchronization signal 5
(7) CC-Link IE TSN network synchronization signal 6
(8) CC-Link IE TSN network synchronization signal 7
(1) CC-Link IE TSN network synchronization signal 0
(2) CC-Link IE TSN network synchronization signal 1
(3) CC-Link IE TSN network synchronization signal 2
(4) CC-Link IE TSN network synchronization signal 3

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Always read register 14

■Address

Name	FPGA register address
Always read register 14 (usr_alwreg_0E)	1000_A04CH

■Description

Stores the signal from the user circuit and the status of Logging control violation flag: Rising edge/Falling edge.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
(3)														(2)	(1)

(1) Logging control violation flag rising edge
- 1: Violation
- 0: No violation

(2) Logging control violation flag falling edge
- 1: Violation
- 0: No violation

(3) Read/write register for user circuit

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Always read register 15

■Address

Name	FPGA register address
Always read register 15 (usr_alwreg_0F)	1000_A04EH

■Description

The statuses of the logging data FTP transfer and FPGA control processing can be checked.

By checking the status of FPGA control processing, it can be used as the timing to start LDAC output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(2)		(1)

(1) Status of FPGA control start processing[*1]
- 1: Start processing completed
- 0: In process of stopping or starting

(2) Logging data FTP transfer status[*2]
- 11: Transfer completed (failed)
- 10: Transfer completed (success)
- 01: Transferring
- 00: Before starting transfer

*1 When FPGA control is stopped, it will be "In process of stopping or starting" (0).

*2 After the transfer is completed, "Before starting transfer" (00) is stored when the next logging starts.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

Writing cannot be made by the FPGA register access function.

Digital control part enable/disable control register

■Address

Name	FPGA register address
Digital control part enable/disable control register (IOB0_X0 B0) (usr_wreg_000)	1000_B000H
Digital control part enable/disable control register (IOB0_X1 B0) (usr_wreg_001)	1000_B002H
Digital control part enable/disable control register (IOB0_X2 B0) (usr_wreg_002)	1000_B004H
Digital control part enable/disable control register (IOB0_X3 B0) (usr_wreg_003)	1000_B006H
Digital control part enable/disable control register (IOB0_X4 B0) (usr_wreg_004)	1000_B008H
Digital control part enable/disable control register (IOB0_X5 B0) (usr_wreg_005)	1000_B00AH
Digital control part enable/disable control register (IOB0_X6 B0) (usr_wreg_006)	1000_B00CH
Digital control part enable/disable control register (IOB0_X7 B0) (usr_wreg_007)	1000_B00EH
Digital control part enable/disable control register (IOB0_X8 B0) (usr_wreg_008)	1000_B010H
Digital control part enable/disable control register (IOB0_X9 B0) (usr_wreg_009)	1000_B012H
Digital control part enable/disable control register (IOB0_XA B0) (usr_wreg_00A)	1000_B014H
Digital control part enable/disable control register (IOB0_XB B0) (usr_wreg_00B)	1000_B016H
Digital control part enable/disable control register (IOB0_XC B0) (usr_wreg_00C)	1000_B018H
Digital control part enable/disable control register (IOB0_XD B0) (usr_wreg_00D)	1000_B01AH
Digital control part enable/disable control register (IOB0_XE B0) (usr_wreg_00E)	1000_B01CH
Digital control part enable/disable control register (IOB0_XF B0) (usr_wreg_00F)	1000_B01EH
Digital control part enable/disable control register (IOB1_X0 B1) (usr_wreg_014)	1000_B028H
Digital control part enable/disable control register (IOB1_X1 B1) (usr_wreg_015)	1000_B02AH
Digital control part enable/disable control register (IOB1_X2 B1) (usr_wreg_016)	1000_B02CH
Digital control part enable/disable control register (IOB1_X3 B1) (usr_wreg_017)	1000_B02EH
Digital control part enable/disable control register (IOB1_X4 B1) (usr_wreg_018)	1000_B030H
Digital control part enable/disable control register (IOB1_X5 B1) (usr_wreg_019)	1000_B032H
Digital control part enable/disable control register (IOB1_X6 B1) (usr_wreg_01A)	1000_B034H
Digital control part enable/disable control register (IOB1_X7 B1) (usr_wreg_01B)	1000_B036H
Digital control part enable/disable control register (IOB1_X8 B1) (usr_wreg_01C)	1000_B038H
Digital control part enable/disable control register (IOB1_X9 B1) (usr_wreg_01D)	1000_B03AH
Digital control part enable/disable control register (IOB1_XA B1) (usr_wreg_01E)	1000_B03CH
Digital control part enable/disable control register (IOB1_XB B1) (usr_wreg_01F)	1000_B03EH
Digital control part enable/disable control register (IOB1_XC B1) (usr_wreg_020)	1000_B040H
Digital control part enable/disable control register (IOB1_XD B1) (usr_wreg_021)	1000_B042H
Digital control part enable/disable control register (IOB1_XE B1) (usr_wreg_022)	1000_B044H
Digital control part enable/disable control register (IOB1_XF B1) (usr_wreg_023)	1000_B046H
Digital control part enable/disable control register (IOB2_X0 B2) (usr_wreg_028)	1000_B050H
Digital control part enable/disable control register (IOB2_X1 B2) (usr_wreg_029)	1000_B052H
Digital control part enable/disable control register (IOB2_X2 B2) (usr_wreg_02A)	1000_B054H
Digital control part enable/disable control register (IOB2_X3 B2) (usr_wreg_02B)	1000_B056H
Digital control part enable/disable control register (IOB2_X4 B2) (usr_wreg_02C)	1000_B058H
Digital control part enable/disable control register (IOB2_X5 B2) (usr_wreg_02D)	1000_B05AH
Digital control part enable/disable control register (IOB2_X6 B2) (usr_wreg_02E)	1000_B05CH
Digital control part enable/disable control register (IOB2_X7 B2) (usr_wreg_02F)	1000_B05EH
Digital control part enable/disable control register (IOB2_X8 B2) (usr_wreg_030)	1000_B060H
Digital control part enable/disable control register (IOB2_X9 B2) (usr_wreg_031)	1000_B062H
Digital control part enable/disable control register (IOB2_XA B2) (usr_wreg_032)	1000_B064H
Digital control part enable/disable control register (IOB2_XB B2) (usr_wreg_033)	1000_B066H
Digital control part enable/disable control register (IOB2_XC B2) (usr_wreg_034)	1000_B068H
Digital control part enable/disable control register (IOB2_XD B2) (usr_wreg_035)	1000_B06AH
Digital control part enable/disable control register (IOB2_XE B2) (usr_wreg_036)	1000_B06CH
Digital control part enable/disable control register (IOB2_XF B2) (usr_wreg_037)	1000_B06EH
Digital control part enable/disable control register (IOE0_X0 E0) (usr_wreg_03C)	1000_B078H

Name	FPGA register address
Digital control part enable/disable control register (IOE0_X1 E0) (usr_wreg_03D)	1000_B07AH
Digital control part enable/disable control register (IOE0_X2 E0) (usr_wreg_03E)	1000_B07CH
Digital control part enable/disable control register (IOE0_X3 E0) (usr_wreg_03F)	1000_B07EH
Digital control part enable/disable control register (IOE0_X4 E0) (usr_wreg_040)	1000_B080H
Digital control part enable/disable control register (IOE0_X5 E0) (usr_wreg_041)	1000_B082H
Digital control part enable/disable control register (IOE0_X6 E0) (usr_wreg_042)	1000_B084H
Digital control part enable/disable control register (IOE0_X7 E0) (usr_wreg_043)	1000_B086H
Digital control part enable/disable control register (IOE0_X8 E0) (usr_wreg_044)	1000_B088H
Digital control part enable/disable control register (IOE0_X9 E0) (usr_wreg_045)	1000_B08AH
Digital control part enable/disable control register (IOE0_XA E0) (usr_wreg_046)	1000_B08CH
Digital control part enable/disable control register (IOE0_XB E0) (usr_wreg_047)	1000_B08EH
Digital control part enable/disable control register (IOE0_XC E0) (usr_wreg_048)	1000_B090H
Digital control part enable/disable control register (IOE0_XD E0) (usr_wreg_049)	1000_B092H
Digital control part enable/disable control register (IOE0_XE E0) (usr_wreg_04A)	1000_B094H
Digital control part enable/disable control register (IOE0_XF E0) (usr_wreg_04B)	1000_B096H
Digital control part enable/disable control register (IOE1_X0 E1) (usr_wreg_050)	1000_B0A0H
Digital control part enable/disable control register (IOE1_X1 E1) (usr_wreg_051)	1000_B0A2H
Digital control part enable/disable control register (IOE1_X2 E1) (usr_wreg_052)	1000_B0A4H
Digital control part enable/disable control register (IOE1_X3 E1) (usr_wreg_053)	1000_B0A6H
Digital control part enable/disable control register (IOE1_X4 E1) (usr_wreg_054)	1000_B0A8H
Digital control part enable/disable control register (IOE1_X5 E1) (usr_wreg_055)	1000_B0AAH
Digital control part enable/disable control register (IOE1_X6 E1) (usr_wreg_056)	1000_B0ACH
Digital control part enable/disable control register (IOE1_X7 E1) (usr_wreg_057)	1000_B0AEH
Digital control part enable/disable control register (IOE1_X8 E1) (usr_wreg_058)	1000_B0B0H
Digital control part enable/disable control register (IOE1_X9 E1) (usr_wreg_059)	1000_B0B2H
Digital control part enable/disable control register (IOE1_XA E1) (usr_wreg_05A)	1000_B0B4H
Digital control part enable/disable control register (IOE1_XB E1) (usr_wreg_05B)	1000_B0B6H
Digital control part enable/disable control register (IOE1_XC E1) (usr_wreg_05C)	1000_B0B8H
Digital control part enable/disable control register (IOE1_XD E1) (usr_wreg_05D)	1000_B0BAH
Digital control part enable/disable control register (IOE1_XE E1) (usr_wreg_05E)	1000_B0BCH
Digital control part enable/disable control register (IOE1_XF E1) (usr_wreg_05F)	1000_B0BEH
Digital control part enable/disable control register (IOE2_X0 E2) (usr_wreg_064)	1000_B0C8H
Digital control part enable/disable control register (IOE2_X1 E2) (usr_wreg_065)	1000_B0CAH
Digital control part enable/disable control register (IOE2_X2 E2) (usr_wreg_066)	1000_B0CCH
Digital control part enable/disable control register (IOE2_X3 E2) (usr_wreg_067)	1000_B0CEH
Digital control part enable/disable control register (IOE2_X4 E2) (usr_wreg_068)	1000_B0D0H
Digital control part enable/disable control register (IOE2_X5 E2) (usr_wreg_069)	1000_B0D2H
Digital control part enable/disable control register (IOE2_X6 E2) (usr_wreg_06A)	1000_B0D4H
Digital control part enable/disable control register (IOE2_X7 E2) (usr_wreg_06B)	1000_B0D6H
Digital control part enable/disable control register (IOE2_X8 E2) (usr_wreg_06C)	1000_B0D8H
Digital control part enable/disable control register (IOE2_X9 E2) (usr_wreg_06D)	1000_B0DAH
Digital control part enable/disable control register (IOE2_XA E2) (usr_wreg_06E)	1000_B0DCH
Digital control part enable/disable control register (IOE2_XB E2) (usr_wreg_06F)	1000_B0DEH
Digital control part enable/disable control register (IOE2_XC E2) (usr_wreg_070)	1000_B0E0H
Digital control part enable/disable control register (IOE2_XD E2) (usr_wreg_071)	1000_B0E2H
Digital control part enable/disable control register (IOE2_XE E2) (usr_wreg_072)	1000_B0E4H
Digital control part enable/disable control register (IOE2_XF E2) (usr_wreg_073)	1000_B0E6H

■Description

Sets the digital output signal (after digital control) of the digital control part.

When the digital output is enabled, the digital control part outputs the digital input signal (after filtering) from the digital input control part in inversion output or through output. When the digital output is disabled, the digital output signal (after digital control) is fixed to 0.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) Digital output enable/disable CH△ (B□)*1, digital output enable/disable CH△ (E□)*1

- 1: Enable
- 0: Disable

(2) Digital output inversion control CH△ (B□)*1, digital output inversion control CH△ (E□)*1

- 1: Enabled (inversion control)
- 0: Disable

*1 △: 0 to F, □: B0 to B2, E0 to E2

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

A

Digital output control digital output selection

■Address

Name	FPGA register address
Digital output control digital output selection (B0) (usr_wreg_078)	1000_B0F0H
Digital output control digital output selection (B1) (usr_wreg_079)	1000_B0F2H
Digital output control digital output selection (B2) (usr_wreg_07A)	1000_B0F4H
Digital output control digital output selection (E0) (usr_wreg_07B)	1000_B0F6H
Digital output control digital output selection (E1) (usr_wreg_07C)	1000_B0F8H
Digital output control digital output selection (E2) (usr_wreg_07D)	1000_B0FAH

■Description

Select the signal to be output from the user circuit to the digital output control part of the standard circuit. Either the digital control part or the pulse output part can be selected as the output source.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CHF	CHE	CHD	CHC	CHB	CHA	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- 1: Pulse output signal
- 0: Digital control output signal

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Digital I/O control I/O control register

■Address

Name	FPGA register address
Digital I/O control I/O control register (B0) (usr_wreg_080)	1000_B100H
Digital I/O control I/O control register (B1) (usr_wreg_081)	1000_B102H
Digital I/O control I/O control register (B2) (usr_wreg_082)	1000_B104H
Digital I/O control I/O control register (E0) (usr_wreg_083)	1000_B106H
Digital I/O control I/O control register (E1) (usr_wreg_084)	1000_B108H
Digital I/O control I/O control register (E2) (usr_wreg_085)	1000_B10AH

■Description

Sets the digital output signal (digital I/O after digital control) of the digital control part. Also, sets the signal to select the I/O direction to the digital I/O control part.

When the digital output is enabled, the digital control part outputs the digital input signal (digital I/O after filtering) from the digital I/O control part in inversion output or through output. When the digital output is disabled, the digital control part is 0 fixed output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) Digital output enable/disable
- 1: Enable
- 0: Disable

(2) Digital output inversion control
- 1: Enabled (inversion control)
- 0: Disable

(3) Digital I/O I/O control
- 1: Output
- 0: Input

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

A

Digital I/O control digital output selection

■Address

Name	FPGA register address
Digital I/O control digital output selection (usr_wreg_086)	1000_B10CH

■Description

Selects the signal to be output from the user circuit to the digital I/O control part of the standard circuit. Either the digital control part or the pulse output part can be selected as the output source.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(6)	(5)	(4)	(3)	(2)	(1)

(1) Digital I/O (B0)
- 1: Pulse output signal
- 0: Digital control output signal

(2) Digital I/O (B1)
- 1: Pulse output signal
- 0: Digital control output signal

(3) Digital I/O (B2)
- 1: Pulse output signal
- 0: Digital control output signal

(4) Digital I/O (E0)
- 1: Pulse output signal
- 0: Digital control output signal

(5) Digital I/O (E1)
- 1: Pulse output signal
- 0: Digital control output signal

(6) Digital I/O (E2)
- 1: Pulse output signal
- 0: Digital control output signal

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Digital output HOLD/CLEAR

■Address

Name	FPGA register address
Digital output HOLD/CLEAR (usr_wreg_088)	1000_B110H

■Description

Controls HOLD/CLEAR of digital output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) HOLD/CLEAR setting
- 1: HOLD
- 0: CLEAR

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Logging control part logging enable signal selection

■Address

Name	FPGA register address
Logging control part logging enable signal selection (usr_wreg_091)	1000_B122H

■Description

Selects the logging enable signal (logging start) of the logging control part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)											Logging enable selection				

- 15H: b0 of the logging control part user logging control (usr_wreg_180)
- 14H: Digital control part output signal (IOB0_X9 B0)
- 13H: Digital control part output signal (IOB0_X8 B0)
- 12H: Digital control part output signal (IOB0_X7 B0)
- 11H: Digital control part output signal (IOB0_X6 B0)
- 10H: Digital control part output signal (IOB0_X5 B0)
- FH: Digital control part output signal (IOB0_X4 B0)
- EH: Digital control part output signal (IOB0_X3 B0)
- DH: Digital control part output signal (IOB0_X2 B0)
- CH: Digital control part output signal (IOB0_X1 B0)
- BH: Digital control part output signal (IOB0_X0 B0)
- AH: Digital input control part output signal (IOB0_X9 B0)
- 9H: Digital input control part output signal (IOB0_X8 B0)
- 8H: Digital input control part output signal (IOB0_X7 B0)
- 7H: Digital input control part output signal (IOB0_X6 B0)
- 6H: Digital input control part output signal (IOB0_X5 B0)
- 5H: Digital input control part output signal (IOB0_X4 B0)
- 4H: Digital input control part output signal (IOB0_X3 B0)
- 3H: Digital input control part output signal (IOB0_X2 B0)
- 2H: Digital input control part output signal (IOB0_X1 B0)
- 1H: Digital input control part output signal (IOB0_X0 B0)
- 0H: Not selected

Digital input control part output signal: Digital input signal from the digital input control part (B0 after filtering)
Digital control part output signal: Digital output signal from the digital control part (B0 after digital control)

■FPGA initial value

00H

■Firmware initial value

00H

■Reset cause

Reset

Logging control part end trigger signal selection

■Address

Name	FPGA register address
Logging control part end trigger signal selection (usr_wreg_092)	1000_B124H

■Description

Selects the logging end trigger signal of the logging control part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)											End trigger signal selection				

- 15H: b1 of the logging control part user logging control (usr_wreg_180)
- 14H: Digital control part output signal (IOB0_X9 B0)
- 13H: Digital control part output signal (IOB0_X8 B0)
- 12H: Digital control part output signal (IOB0_X7 B0)
- 11H: Digital control part output signal (IOB0_X6 B0)
- 10H: Digital control part output signal (IOB0_X5 B0)
- FH: Digital control part output signal (IOB0_X4 B0)
- EH: Digital control part output signal (IOB0_X3 B0)
- DH: Digital control part output signal (IOB0_X2 B0)
- CH: Digital control part output signal (IOB0_X1 B0)
- BH: Digital control part output signal (IOB0_X0 B0)
- AH: Digital input control part output signal (IOB0_X9 B0)
- 9H: Digital input control part output signal (IOB0_X8 B0)
- 8H: Digital input control part output signal (IOB0_X7 B0)
- 7H: Digital input control part output signal (IOB0_X6 B0)
- 6H: Digital input control part output signal (IOB0_X5 B0)
- 5H: Digital input control part output signal (IOB0_X4 B0)
- 4H: Digital input control part output signal (IOB0_X3 B0)
- 3H: Digital input control part output signal (IOB0_X2 B0)
- 2H: Digital input control part output signal (IOB0_X1 B0)
- 1H: Digital input control part output signal (IOB0_X0 B0)
- 0H: Not selected

Digital input control part output signal: Digital input signal from the digital input control part (B0 after filtering)

Digital control part output signal: Digital output signal from the digital control part (B0 after digital control)

■FPGA initial value

00H

■Firmware initial value

00H

■Reset cause

Reset

Logging control part sampling pulse signal selection

■Address

Name	FPGA register address
Logging control part sampling pulse signal selection (usr_wreg_093)	1000_B126H

■Description

Selects the user sampling pulse signal of the logging control part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)									Sampling pulse signal selection						

- 17H: A/D conversion value enable (E2)
- 16H: A/D conversion value enable (E1)
- 15H: A/D conversion value enable (E0)
- 14H: Digital control part output signal (IOB0_X9 B0)
- 13H: Digital control part output signal (IOB0_X8 B0)
- 12H: Digital control part output signal (IOB0_X7 B0)
- 11H: Digital control part output signal (IOB0_X6 B0)
- 10H: Digital control part output signal (IOB0_X5 B0)
- FH: Digital control part output signal (IOB0_X4 B0)
- EH: Digital control part output signal (IOB0_X3 B0)
- DH: Digital control part output signal (IOB0_X2 B0)
- CH: Digital control part output signal (IOB0_X1 B0)
- BH: Digital control part output signal (IOB0_X0 B0)
- AH: Digital input control part output signal (IOB0_X9 B0)
- 9H: Digital input control part output signal (IOB0_X8 B0)
- 8H: Digital input control part output signal (IOB0_X7 B0)
- 7H: Digital input control part output signal (IOB0_X6 B0)
- 6H: Digital input control part output signal (IOB0_X5 B0)
- 5H: Digital input control part output signal (IOB0_X4 B0)
- 4H: Digital input control part output signal (IOB0_X3 B0)
- 3H: Digital input control part output signal (IOB0_X2 B0)
- 2H: Digital input control part output signal (IOB0_X1 B0)
- 1H: Digital input control part output signal (IOB0_X0 B0)
- 0H: Not selected

Digital input control part output signal: Digital input signal from the digital input control part (B0 after filtering)
Digital control part output signal: Digital output signal from the digital control part (B0 after digital control)

■FPGA initial value

00H

■Firmware initial value

00H

■Reset cause

Reset

■Precautions and restrictions

To select the analog I/O circuit board and log the A/D conversion value, enable (1) b0 of user circuit logging mode selection (usr_logmode_sel) and set this register to 15H to 17H. If the A/D conversion value does not require logging, disable (0) b0 of user circuit logging mode selection (usr_logmode_sel) and set this register to 1H to 14H. Otherwise, the data will not be stored properly in DDR3L SDRAM.

Logging control part logging enable mode setting

■Address

Name	FPGA register address
Logging control part logging enable mode setting (usr_wreg_094)	1000_B128H

■Description

Selects the mode of the logging enable signal.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Logging enable mode setting
- 1: 1 enable mode
- 0: Multiple enable mode

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Logging control part automatic transfer mode setting

■Address

Name	FPGA register address
Logging control part automatic transfer mode setting (usr_wreg_095)	1000_B12AH

■Description

Enables or disables the automatic transfer mode of the user circuit part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Automatic transfer mode (user circuit part)
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit value

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (B0) (usr_wreg_0A3)	1000_B146H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (B0) (usr_wreg_0A4)	1000_B148H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (B1) (usr_wreg_0AB)	1000_B156H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (B1) (usr_wreg_0AC)	1000_B158H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (B2) (usr_wreg_0B3)	1000_B166H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (B2) (usr_wreg_0B4)	1000_B168H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E0) (usr_wreg_0BB)	1000_B176H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E0) (usr_wreg_0BC)	1000_B178H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E1) (usr_wreg_0C3)	1000_B186H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E1) (usr_wreg_0C4)	1000_B188H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (lower side) (E2) (usr_wreg_0CB)	1000_B196H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter upper limit (upper side) (E2) (usr_wreg_0CC)	1000_B198H

■Description

Sets the counter upper limit value of the 32-bit ring counter (2-phase multiple of 4).

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B0) (usr_wreg_0A5)	1000_B14AH
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B1) (usr_wreg_0AD)	1000_B15AH
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (B2) (usr_wreg_0B5)	1000_B16AH
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E0) (usr_wreg_0BD)	1000_B17AH
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E1) (usr_wreg_0C5)	1000_B18AH
Counter control part 32-bit ring counter (2-phase multiple of 4) input signal selection (E2) (usr_wreg_0CD)	1000_B19AH

■Description

Sets the input signal of the 32-bit ring counter (2-phase multiple of 4).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)		(4)	(3)					0 (fixed)		(2)	(1)				

(3) Phase B input selection
- 12H to 1FH: Same as 0H
- 11H: IO□_DIO485_I[*1]
- 10H: IO□_X[7]chF[*1]
- FH: IO□_X[6]chE[*1]
- EH: IO□_X[5]chD[*1]
- DH: IO□_X[4]chC[*1]
- CH: IO□_X[3]chB[*1]
- BH: IO□_X[2]chA[*1]
- AH: IO□_X[1]ch9[*1]
- 9H: IO□_X[0]ch8[*1]
- 8H: IO□_X[7]ch7 or IO□_DI422[7][*1]
- 7H: IO□_X[6]ch6 or IO□_DI422[6][*1]
- 6H: IO□_X[5]ch5 or IO□_DI422[5][*1]
- 5H: IO□_X[4]ch4 or IO□_DI422[4][*1]
- 4H: IO□_X[3]ch3 or IO□_DI422[3][*1]
- 3H: IO□_X[2]ch2 or IO□_DI422[2][*1]
- 2H: IO□_X[1]ch1 or IO□_DI422[1][*1]
- 1H: IO□_X[0]ch0 or IO□_DI422[0][*1]
- 0H: Phase B register input (b13)

(4) Phase B register input
- 1: 1 input
- 0: 0 input

(1) Phase A input selection
- 12H to 1FH: Same as 0H
- 11H: IO□_DIO485_I[*1]
- 10H: IO□_X[7]chF[*1]
- FH: IO□_X[6]chE[*1]
- EH: IO□_X[5]chD[*1]
- DH: IO□_X[4]chC[*1]
- CH: IO□_X[3]chB[*1]
- BH: IO□_X[2]chA[*1]
- AH: IO□_X[1]ch9[*1]
- 9H: IO□_X[0]ch8[*1]
- 8H: IO□_X[7]ch7 or IO□_DI422[7][*1]
- 7H: IO□_X[6]ch6 or IO□_DI422[6][*1]
- 6H: IO□_X[5]ch5 or IO□_DI422[5][*1]
- 5H: IO□_X[4]ch4 or IO□_DI422[4][*1]
- 4H: IO□_X[3]ch3 or IO□_DI422[3][*1]
- 3H: IO□_X[2]ch2 or IO□_DI422[2][*1]
- 2H: IO□_X[1]ch1 or IO□_DI422[1][*1]
- 1H: IO□_X[0]ch0 or IO□_DI422[0][*1]
- 0H: Phase A register input (b5)

(2) phase A register input
- 1: 1 input
- 0: 0 input

*1 □: B0 to B2, E0 to E2

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B0) (usr_wreg_0D3)	1000_B1A6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B0) (usr_wreg_0D4)	1000_B1A8H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B1) (usr_wreg_0DB)	1000_B1B6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B1) (usr_wreg_0DC)	1000_B1B8H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (B2) (usr_wreg_0E3)	1000_B1C6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (B2) (usr_wreg_0E4)	1000_B1C8H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E0) (usr_wreg_0EB)	1000_B1D6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E0) (usr_wreg_0EC)	1000_B1D8H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E1) (usr_wreg_0F3)	1000_B1E6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E1) (usr_wreg_0F4)	1000_B1E8H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (lower side) (E2) (usr_wreg_0FB)	1000_B1F6H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter upper limit value (upper side) (E2) (usr_wreg_0FC)	1000_B1F8H

■Description

Sets the counter upper limit value of the 32-bit ring counter (1-phase multiple of 1).

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B0) (usr_wreg_0D5)	1000_B1AAH
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B1) (usr_wreg_0DD)	1000_B1BAH
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (B2) (usr_wreg_0E5)	1000_B1CAH
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E0) (usr_wreg_0ED)	1000_B1DAH
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E1) (usr_wreg_0F5)	1000_B1EAH
Counter control part 32-bit ring counter (1-phase multiple of 1) input signal selection (E2) (usr_wreg_0FD)	1000_B1FAH

■Description

Sets the input signal of the 32-bit ring counter (1-phase multiple of 1).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)		(4)	(3)					0 (fixed)		(2)	(1)				

(3) Phase Z input selection
- 12H to 1FH: Same as 0H
- 11H: IO□_DIO485_I[*1]
- 10H: IO□_X[7]chF[*1]
- FH: IO□_X[6]chE[*1]
- EH: IO□_X[5]chD[*1]
- DH: IO□_X[4]chC[*1]
- CH: IO□_X[3]chB[*1]
- BH: IO□_X[2]chA[*1]
- AH: IO□_X[1]ch9[*1]
- 9H: IO□_X[0]ch8[*1]
- 8H: IO□_X[7]ch7 or IO□_DI422[7][*1]
- 7H: IO□_X[6]ch6 or IO□_DI422[6][*1]
- 6H: IO□_X[5]ch5 or IO□_DI422[5][*1]
- 5H: IO□_X[4]ch4 or IO□_DI422[4][*1]
- 4H: IO□_X[3]ch3 or IO□_DI422[3][*1]
- 3H: IO□_X[2]ch2 or IO□_DI422[2][*1]
- 2H: IO□_X[1]ch1 or IO□_DI422[1][*1]
- 1H: IO□_X[0]ch0 or IO□_DI422[0][*1]
- 0H: Phase Z register input (b13)

(4) Phase Z register input
- 1: 1 input
- 0: 0 input

(1) Phase A input selection
- 12H to 1FH: Same as 0H
- 11H: IO□_DIO485_I[*1]
- 10H: IO□_X[7]chF[*1]
- FH: IO□_X[6]chE[*1]
- EH: IO□_X[5]chD[*1]
- DH: IO□_X[4]chC[*1]
- CH: IO□_X[3]chB[*1]
- BH: IO□_X[2]chA[*1]
- AH: IO□_X[1]ch9[*1]
- 9H: IO□_X[0]ch8[*1]
- 8H: IO□_X[7]ch7 or IO□_DI422[7][*1]
- 7H: IO□_X[6]ch6 or IO□_DI422[6][*1]
- 6H: IO□_X[5]ch5 or IO□_DI422[5][*1]
- 5H: IO□_X[4]ch4 or IO□_DI422[4][*1]
- 4H: IO□_X[3]ch3 or IO□_DI422[3][*1]
- 3H: IO□_X[2]ch2 or IO□_DI422[2][*1]
- 2H: IO□_X[1]ch1 or IO□_DI422[1][*1]
- 1H: IO□_X[0]ch0 or IO□_DI422[0][*1]
- 0H: Phase A register input (b5)

(2) phase A register input
- 1: 1 input
- 0: 0 input

*1 □: B0 to B2, E0 to E2

■FPGA initial value

00H

■Firmware initial value

00H

■Reset cause

Reset

Pulse output part pulse width upper limit value

■Address

Name	FPGA register address
Pulse output part pulse width upper limit value (lower side) (B0) (usr_wreg_110)	1000_B220H
Pulse output part pulse width upper limit value (upper side) (B0) (usr_wreg_111)	1000_B222H
Pulse output part pulse width upper limit value (lower side) (B1) (usr_wreg_115)	1000_B22AH
Pulse output part pulse width upper limit value (upper side) (B1) (usr_wreg_116)	1000_B22CH
Pulse output part pulse width upper limit value (lower side) (B2) (usr_wreg_11A)	1000_B234H
Pulse output part pulse width upper limit value (upper side) (B2) (usr_wreg_11B)	1000_B236H
Pulse output part pulse width upper limit value (lower side) (E0) (usr_wreg_11F)	1000_B23EH
Pulse output part pulse width upper limit value (upper side) (E0) (usr_wreg_120)	1000_B240H
Pulse output part pulse width upper limit value (lower side) (E1) (usr_wreg_124)	1000_B248H
Pulse output part pulse width upper limit value (upper side) (E1) (usr_wreg_125)	1000_B24AH
Pulse output part pulse width upper limit value (lower side) (E2) (usr_wreg_129)	1000_B252H
Pulse output part pulse width upper limit value (upper side) (E2) (usr_wreg_12A)	1000_B254H

■Description

Sets the pulse width to be output to the digital output control part.

- FFFF_FFFFH: 42.94968 seconds to 0004H: 0.05μs
- 0000H to 0003H: 0.04μs

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Pulse output part output pulse count upper limit value

■Address

Name	FPGA register address
Pulse output part output pulse count upper limit value (lower side) (B0) (usr_wreg_112)	1000_B224H
Pulse output part output pulse count upper limit value (upper side) (B0) (usr_wreg_113)	1000_B226H
Pulse output part output pulse count upper limit value (lower side) (B1) (usr_wreg_117)	1000_B22EH
Pulse output part output pulse count upper limit value (upper side) (B1) (usr_wreg_118)	1000_B230H
Pulse output part output pulse count upper limit value (lower side) (B2) (usr_wreg_11C)	1000_B238H
Pulse output part output pulse count upper limit value (upper side) (B2) (usr_wreg_11D)	1000_B23AH
Pulse output part output pulse count upper limit value (lower side) (E0) (usr_wreg_121)	1000_B242H
Pulse output part output pulse count upper limit value (upper side) (E0) (usr_wreg_122)	1000_B244H
Pulse output part output pulse count upper limit value (lower side) (E1) (usr_wreg_126)	1000_B24CH
Pulse output part output pulse count upper limit value (upper side) (E1) (usr_wreg_127)	1000_B24EH
Pulse output part output pulse count upper limit value (lower side) (E2) (usr_wreg_12B)	1000_B256H
Pulse output part output pulse count upper limit value (upper side) (E2) (usr_wreg_12C)	1000_B258H

■Description

Sets the pulse count to be output to the digital output control part.

- FFFF_FFFFH: 4294967295 pulse to 0002H: 2 pulses
- 0001H: 1 pulse
- 0000H: No pulse output

■FPGA initial value

0000H

■Firmware initial value

0000H

■Reset cause

Reset

Pulse output part pulse output selection

■Address

Name	FPGA register address
Pulse output part pulse output selection 0 (B0) (usr_wreg_130)	1000_B260H
Pulse output part pulse output selection 1 (B0) (usr_wreg_131)	1000_B262H
Pulse output part pulse output selection 2 (B0) (usr_wreg_132)	1000_B264H
Pulse output part pulse output selection 0 (B1) (usr_wreg_133)	1000_B266H
Pulse output part pulse output selection 1 (B1) (usr_wreg_134)	1000_B268H
Pulse output part pulse output selection 2 (B1) (usr_wreg_135)	1000_B26AH
Pulse output part pulse output selection 0 (B2) (usr_wreg_136)	1000_B26CH
Pulse output part pulse output selection 1 (B2) (usr_wreg_137)	1000_B26EH
Pulse output part pulse output selection 2 (B2) (usr_wreg_138)	1000_B270H
Pulse output part pulse output selection 0 (E0) (usr_wreg_139)	1000_B272H
Pulse output part pulse output selection 1 (E0) (usr_wreg_13A)	1000_B274H
Pulse output part pulse output selection 2 (E0) (usr_wreg_13B)	1000_B276H
Pulse output part pulse output selection 0 (E1) (usr_wreg_13C)	1000_B278H
Pulse output part pulse output selection 1 (E1) (usr_wreg_13D)	1000_B27AH
Pulse output part pulse output selection 2 (E1) (usr_wreg_13E)	1000_B27CH
Pulse output part pulse output selection 0 (E2) (usr_wreg_13F)	1000_B27EH
Pulse output part pulse output selection 1 (E2) (usr_wreg_140)	1000_B280H
Pulse output part pulse output selection 2 (E2) (usr_wreg_141)	1000_B282H

■Description

Selects the output pulses from 0, 90, 180, and 270 degrees.

Name	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Pulse output part pulse output selection 0	CH7		CH6		CH5		CH4		CH3		CH2		CH1		CH0	
Pulse output part pulse output selection 1	CHF		CHE		CHD		CHC		CHB		CHA		CH9		CH8	
Pulse output part pulse output selection 2	0 (fixed)														IOB0_DIO485_O (for I/O control)	

- 11: Basic pulse (270 degrees)
- 10: Basic pulse (180 degrees)
- 01: Basic pulse (90 degrees)
- 00: Basic pulse (0 degrees)

■FPGA initial value

00

■Firmware initial value

00

■Reset cause

Reset

Pulse output part pulse output mask

■Address

Name	FPGA register address
Pulse output part pulse output mask 0 (B0) (usr_wreg_142)	1000_B284H
Pulse output part pulse output mask 1 (B0) (usr_wreg_143)	1000_B286H
Pulse output part pulse output mask 0 (B1) (usr_wreg_144)	1000_B288H
Pulse output part pulse output mask 1 (B1) (usr_wreg_145)	1000_B28AH
Pulse output part pulse output mask 0 (B2) (usr_wreg_146)	1000_B28CH
Pulse output part pulse output mask 1 (B2) (usr_wreg_147)	1000_B28EH
Pulse output part pulse output mask 0 (E0) (usr_wreg_148)	1000_B290H
Pulse output part pulse output mask 1 (E0) (usr_wreg_149)	1000_B292H
Pulse output part pulse output mask 0 (E1) (usr_wreg_14A)	1000_B294H
Pulse output part pulse output mask 1 (E1) (usr_wreg_14B)	1000_B296H
Pulse output part pulse output mask 0 (E2) (usr_wreg_14C)	1000_B298H
Pulse output part pulse output mask 1 (E2) (usr_wreg_14D)	1000_B29AH

■Description

Enables or disables the pulse output.

Name	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Pulse output part pulse output mask 0	CHF	CHE	CHD	CHC	CHB	CHA	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Pulse output part pulse output mask 1	0 (fixed)															(1)

CH0 to CHF
- 1: Enable
- 0: Disable

(1) IOB0_DIO485_O (for I/O control)
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Analog output part LDAC output selection

■Address

Name	FPGA register address
Analog output part LDAC output selection (usr_wreg_160)	1000_B2C0H

■Description

Select LDAC1 or LDAC0 output.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(3)		(2)		(1)	

(1) E0 LDAC1, LDAC0 output
- 11: 11b output
- 10: LDAC output for inter-channel synchronization
- 01: 00b output
- 00: 11b output

(2) E1 LDAC1, LDAC0 output
- 11: 11b output
- 10: LDAC output for inter-channel synchronization
- 01: 00b output
- 00: 11b output

(3) E2 LDAC1, LDAC0 output
- 11: 11b output
- 10: LDAC output for inter-channel synchronization
- 01: 00b output
- 00: 11b output

■FPGA initial value

00

■Firmware initial value

00

■Reset cause

Reset

■Precautions and restrictions

When the analog output cycle is set faster than 5μs, do not set the LDAC output for inter-channel synchronization.

Analog output part HOLD/CLEAR

■Address

Name	FPGA register address
Analog output part HOLD/CLEAR (usr_wreg_168)	1000_B2D0H

■Description

Controls HOLD/CLEAR of analog control.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) HOLD/CLEAR setting
- 1: HOLD
- 0: CLEAR

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Test mode setting

■Address

Name	FPGA register address
Test mode setting (usr_wreg_17F)	1000_B2FEH

■Description

When the test mode is enabled, the value of write data (cyclic area) is transferred to read data (cyclic area). When the test mode is disabled, the status of the user circuit is transferred to the read data (cyclic area).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Test mode function enable/disable
- 1: Test mode enable
- 0: Test mode disable

■FPGA initial value

0

■Firmware initial value

0

■Reset cause

Reset

Logging control part user logging control

■Address

Name	FPGA register address
Logging control part: User logging control (usr_wreg_180)	1000_B300H

■Description

Sets logging enable and logging stop.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(2)	(1)

(1) Logging enable
- 1: Logging enable assert
- 0: Logging enable negate

(2) End trigger
- 1: End trigger assert
- 0: End trigger negate

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

To output the end trigger again, set b1 to End trigger assert (1) → End trigger negate (0) → End trigger assert (1).

Logging control part 1 enable clear

■Address

Name	FPGA register address
Logging control part 1 enable clear (usr_wreg_181)	1000_B302H

■Description

1 Clears the logging enable signal in enable mode.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) 1 logging enable clear setting
- 1: 1 enable mode clear

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B0) (usr_wreg_188)	1000_B310H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B1) (usr_wreg_18B)	1000_B316H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (B2) (usr_wreg_18E)	1000_B31CH
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E0) (usr_wreg_191)	1000_B322H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E1) (usr_wreg_194)	1000_B328H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset instruction (E2) (usr_wreg_197)	1000_B32EH

■Description

Enables or disables the preset of the 32-bit ring counter (2-phase multiple of 4).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Presets the 32-bit ring counter (2-phase multiple of 4).
- 1: Preset enable
- 0: Preset disable

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Counter control part 32-bit ring counter (2-phase multiple of 4) preset data

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B0) (usr_wreg_189)	1000_B312H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B0) (usr_wreg_18A)	1000_B314H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B1) (usr_wreg_18C)	1000_B318H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B1) (usr_wreg_18D)	1000_B31AH
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (B2) (usr_wreg_18F)	1000_B31EH
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (B2) (usr_wreg_190)	1000_B320H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E0) (usr_wreg_192)	1000_B324H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E0) (usr_wreg_193)	1000_B326H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E1) (usr_wreg_195)	1000_B32AH
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E1) (usr_wreg_196)	1000_B32CH
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (lower side) (E2) (usr_wreg_198)	1000_B330H
Counter control part 32-bit ring counter (2-phase multiple of 4) preset data (upper side) (E2) (usr_wreg_199)	1000_B332H

■Description

Sets the preset data of the 32-bit ring counter (2-phase multiple of 4).

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B0) (usr_wreg_1A0)	1000_B340H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B1) (usr_wreg_1A3)	1000_B346H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (B2) (usr_wreg_1A6)	1000_B34CH
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E0) (usr_wreg_1A9)	1000_B352H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E1) (usr_wreg_1AC)	1000_B358H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset instruction (E2) (usr_wreg_1AF)	1000_B35EH

■Description

Enables or disables the preset of the 32-bit ring counter (1-phase multiple of 1).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Presets the 32-bit ring counter (1-phase multiple of 1).
- 1: Preset enable
- 0: Preset disable

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

A

Counter control part 32-bit ring counter (1-phase multiple of 1) preset data

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B0) (usr_wreg_1A1)	1000_B342H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B0) (usr_wreg_1A2)	1000_B344H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B1) (usr_wreg_1A4)	1000_B348H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B1) (usr_wreg_1A5)	1000_B34AH
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (B2) (usr_wreg_1A7)	1000_B34EH
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (B2) (usr_wreg_1A8)	1000_B350H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E0) (usr_wreg_1AA)	1000_B354H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E0) (usr_wreg_1AB)	1000_B356H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E1) (usr_wreg_1AD)	1000_B35AH
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E1) (usr_wreg_1AE)	1000_B35CH
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (lower side) (E2) (usr_wreg_1B0)	1000_B360H
Counter control part 32-bit ring counter (1-phase multiple of 1) preset data (upper side) (E2) (usr_wreg_1B1)	1000_B362H

■Description

Sets the preset data of the 32-bit ring counter (1-phase multiple of 1).

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Pulse output part pulse output enable

■Address

Name	FPGA register address
Pulse output part pulse output enable (B0) (usr_wreg_1B8)	1000_B370H
Pulse output part pulse output enable (B1) (usr_wreg_1B9)	1000_B372H
Pulse output part pulse output enable (B2) (usr_wreg_1BA)	1000_B374H
Pulse output part pulse output enable (E0) (usr_wreg_1BB)	1000_B376H
Pulse output part pulse output enable (E1) (usr_wreg_1BC)	1000_B378H
Pulse output part pulse output enable (E2) (usr_wreg_1BD)	1000_B37AH

■Description

Outputs pulses for a set number of times to Pulse output part output pulse count upper limit value (lower side) (B0) (usr_wreg_112) (FPGA register address: 1000_B224H) to Pulse output part output pulse count upper limit value (upper side) (E2) (usr_wreg_12C) (FPGA register address: 1000_B258H).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) Pulse output enable/disable
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Analog output part D/A conversion value

■Address

Name	FPGA register address
Analog output part D/A conversion value CH0 (E0) (usr_wreg_1C0)	1000_B380H
Analog output part D/A conversion value CH1 (E0) (usr_wreg_1C1)	1000_B382H
Analog output part D/A conversion value CH0 (E1) (usr_wreg_1C2)	1000_B384H
Analog output part D/A conversion value CH1 (E1) (usr_wreg_1C3)	1000_B386H
Analog output part D/A conversion value CH0 (E2) (usr_wreg_1C4)	1000_B388H
Analog output part D/A conversion value CH1 (E2) (usr_wreg_1C5)	1000_B38AH

■Description

Sets the D/A conversion value.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Analog output part D/A conversion value enable

■Address

Name	FPGA register address
Analog output part D/A conversion value enable (usr_wreg_1C6)	1000_B38CH

■Description

Outputs 1 pulse of the data update timing to the analog output control part, and performs the D/A conversion for the analog output part D/A conversion value.

Also, outputs the analog output start pulse at the same timing.

The LDAC signal is output at the second pulse of the analog output start pulse.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) E0 D/A conversion value enable
- 1: Pulse output
- 0: No pulse output

(2) E1 D/A conversion value enable
- 1: Pulse output
- 0: No pulse output

(3) E2 D/A conversion value enable
- 1: Pulse output
- 0: No pulse output

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

1 pulse is output by setting pulse output (1) to each bit. To output a pulse again, set to No pulse output (0) → Pulse output (1).

Analog control data sampling pulse generation

■Address

Name	FPGA register address
Analog control data sampling pulse generation (usr_wreg_1C8)	1000_B390H

■Description

Outputs the data sampling of the analog input control part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)										(6)	(5)	(4)	(3)	(2)	(1)

(1) Analog control data sampling pulse generation (B0)
- 1: Pulse output
- 0: No pulse output

(2) Analog control data sampling pulse generation (B1)
- 1: Pulse output
- 0: No pulse output

(3) Analog control data sampling pulse generation (B2)
- 1: Pulse output
- 0: No pulse output

(4) Analog control data sampling pulse generation (E0)
- 1: Pulse output
- 0: No pulse output

(5) Analog control data sampling pulse generation (E1)
- 1: Pulse output
- 0: No pulse output

(6) Analog control data sampling pulse generation (E2)
- 1: Pulse output
- 0: No pulse output

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

■Precautions and restrictions

1 pulse is output by setting pulse output (1) to each bit. To output a pulse again, set to No pulse output (0) → Pulse output (1).

User circuit part error signal generation

■Address

Name	FPGA register address
User circuit part error signal generations (usr_wreg_1D0)	1000_B3A0H

■Description

Generates an error signal to output from the user circuit.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)															(1)

(1) User circuit: Error signal generation
- 1: (1) Output
- 0: (0) Output

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

A/D conversion value maximum/minimum value selection

■Address

Name	FPGA register address
A/D conversion value maximum/minimum selection (usr_wreg_1D8)	1000_B3B0H

■Description

Selects one circuit board from E0 to E2 to transfer the maximum and minimum A/D conversion values to maximum A/D conversion value CH0 (usr_rreg_1D7) (FPGA register address: 1000_BBAEH) to maximum A/D conversion value CHB (usr_rreg_1E2) (FPGA register address: 1000_BBC4H), and to minimum A/D conversion value CH0 (usr_rreg_1E3) (FPGA register address: 1000_BBC6H) to minimum A/D conversion value CHB (usr_rreg_1EE) (FPGA register address: 1000_BBDCH).

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)														(1)	

(1) Analog control: A/D conversion value maximum/minimum value selection
- 11: E0
- 10: E2
- 01: E1
- 00: E0

■FPGA initial value

00

■Firmware initial value

—

■Reset cause

Reset

A/D conversion value maximum/minimum current value update

■Address

Name	FPGA register address
A/D conversion value maximum/minimum current value update (usr_wreg_1D9)	1000_B3B2H

■Description

Updates the maximum and minimum values of A/D conversion values of E0 to E2 to the current values.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) A/D conversion value maximum/minimum value: Current value update(E0)
- 1: Update to the current value

(2) A/D conversion value maximum/minimum value: Current value update(E1)
- 1: Update to the current value

(3) A/D conversion value maximum/minimum value: Current value update(E2)
- 1: Update to the current value

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Read data (transient area)

■Address

Name	FPGA register address
Read data (transient area) (usr_rreg_000 to usr_rreg_17F)	1000_B800H to 1000_BAFFH

■Description

The value of write data (transient area) is stored.

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Module type signal (main)

■Address

Name	FPGA register address
Module type signal (main) (usr_rreg_180)	1000_BB00H

■Description

The module type of the circuit board connected to the connector (B0 to B2) of the main module is stored.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)				(3)				(2)				(1)			

(1) Module type (B0) (IOB0_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

(2) Module type (B1) (IOB1_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

(3) Module type (B2) (IOB2_UNIT[3:0])
- 0001: DC I/O circuit board
- 0010: Differential I/O circuit board

■FPGA initial value

0000

■Firmware initial value

—

■Reset cause

Reset

Module type signal (extension)

■Address

Name	FPGA register address
Module type signal (extension) (usr_rreg_181)	1000_BB02H

■Description

Stores the module type of the circuit board connected to the connector (E0 to E2) of the extension module.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)											(1)				

(1) Module type (E0 to E2) (IOE_UNIT[4:0])
- 0001: DC I/O circuit board (E0 to E2)
- 0010: Differential I/O circuit board (E0 to E2)
- 0011: Analog I/O circuit board (E0 to E2)
- 1111: No connection circuit board (E0 to E2)

■FPGA initial value

0000

■Firmware initial value

—

■Reset cause

Reset

Digital input (after filtering) CH0 to CHF

■Address

Name	FPGA register address
Digital input (after filtering) CH0 to CHF (B0) (usr_rreg_182)	1000_BB04H
Digital input (after filtering) CH0 to CHF (B1) (usr_rreg_184)	1000_BB08H
Digital input (after filtering) CH0 to CHF (B2) (usr_rreg_186)	1000_BB0CH
Digital input (after filtering) CH0 to CHF (E0) (usr_rreg_188)	1000_BB10H
Digital input (after filtering) CH0 to CHF (E1) (usr_rreg_18A)	1000_BB14H
Digital input (after filtering) CH0 to CHF (E2) (usr_rreg_18C)	1000_BB18H

■Description

Stores the digital input (after filtering) of CH0 to CHF.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CHF	CHE	CHD	CHC	CHB	CHA	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

■FPGA initial value

0000

■Firmware initial value

—

■Reset cause

Reset

Digital input (after filtering) IOB0_DIO485_I

■Address

Name	FPGA register address
Digital input (after filtering) IOB0_DIO485_I (B0) (usr_rreg_183)	1000_BB06H
Digital input (after filtering) IOB0_DIO485_I (B1) (usr_rreg_185)	1000_BB0AH
Digital input (after filtering) IOB0_DIO485_I (B2) (usr_rreg_187)	1000_BB0EH
Digital input (after filtering) IOB0_DIO485_I (E0) (usr_rreg_189)	1000_BB12H
Digital input (after filtering) IOB0_DIO485_I (E1) (usr_rreg_18B)	1000_BB16H
Digital input (after filtering) IOB0_DIO485_I (E2) (usr_rreg_18D)	1000_BB1AH

■Description

Stores the digital input (after filtering) IOB0_DIO485_I.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

A/D conversion value enable status

■Address

Name	FPGA register address
A/D conversion value enable status (usr_rreg_18E)	1000_BB1CH

■Description

Stores the enable/disable of the A/D conversion value of E□.

It is enabled at the timing when the A/D conversion value is input from the ADC to the analog input control part.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0 (fixed)													(3)	(2)	(1)

(1) A/D conversion value enable status(E0)
- 1: Enable
- 0: Disable

(2) A/D conversion value enable status(E1)
- 1: Enable
- 0: Disable

(3) A/D conversion value enable status(E2)
- 1: Enable
- 0: Disable

■FPGA initial value

0

■Firmware initial value

—

■Reset cause

Reset

Analog control A/D conversion value

■Address

Name	FPGA register address
Analog control A/D conversion value CH0 (E0) (usr_rreg_18F)	1000_BB1EH
Analog control A/D conversion value CH1 (E0) (usr_rreg_190)	1000_BB20H
Analog control A/D conversion value CH2 (E0) (usr_rreg_191)	1000_BB22H
Analog control A/D conversion value CH3 (E0) (usr_rreg_192)	1000_BB24H
Analog control A/D conversion value CH4 (E0) (usr_rreg_193)	1000_BB26H
Analog control A/D conversion value CH5 (E0) (usr_rreg_194)	1000_BB28H
Analog control A/D conversion value CH6 (E0) (usr_rreg_195)	1000_BB2AH
Analog control A/D conversion value CH7 (E0) (usr_rreg_196)	1000_BB2CH
Analog control A/D conversion value CH8 (E0) (usr_rreg_197)	1000_BB2EH
Analog control A/D conversion value CH9 (E0) (usr_rreg_198)	1000_BB30H
Analog control A/D conversion value CHA (E0) (usr_rreg_199)	1000_BB32H
Analog control A/D conversion value CHB (E0) (usr_rreg_19A)	1000_BB34H
Analog control A/D conversion value CH0 (E1) (usr_rreg_19B)	1000_BB36H
Analog control A/D conversion value CH1 (E1) (usr_rreg_19C)	1000_BB38H
Analog control A/D conversion value CH2 (E1) (usr_rreg_19D)	1000_BB3AH
Analog control A/D conversion value CH3 (E1) (usr_rreg_19E)	1000_BB3CH
Analog control A/D conversion value CH4 (E1) (usr_rreg_19F)	1000_BB3EH
Analog control A/D conversion value CH5 (E1) (usr_rreg_1A0)	1000_BB40H
Analog control A/D conversion value CH6 (E1) (usr_rreg_1A1)	1000_BB42H
Analog control A/D conversion value CH7 (E1) (usr_rreg_1A2)	1000_BB44H
Analog control A/D conversion value CH8 (E1) (usr_rreg_1A3)	1000_BB46H
Analog control A/D conversion value CH9 (E1) (usr_rreg_1A4)	1000_BB48H
Analog control A/D conversion value CHA (E1) (usr_rreg_1A5)	1000_BB4AH
Analog control A/D conversion value CHB (E1) (usr_rreg_1A6)	1000_BB4CH
Analog control A/D conversion value CH0 (E2) (usr_rreg_1A7)	1000_BB4EH
Analog control A/D conversion value CH1 (E2) (usr_rreg_1A8)	1000_BB50H
Analog control A/D conversion value CH2 (E2) (usr_rreg_1A9)	1000_BB52H
Analog control A/D conversion value CH3 (E2) (usr_rreg_1AA)	1000_BB54H
Analog control A/D conversion value CH4 (E2) (usr_rreg_1AB)	1000_BB56H
Analog control A/D conversion value CH5 (E2) (usr_rreg_1AC)	1000_BB58H
Analog control A/D conversion value CH6 (E2) (usr_rreg_1AD)	1000_BB5AH
Analog control A/D conversion value CH7 (E2) (usr_rreg_1AE)	1000_BB5CH
Analog control A/D conversion value CH8 (E2) (usr_rreg_1AF)	1000_BB5EH
Analog control A/D conversion value CH9 (E2) (usr_rreg_1B0)	1000_BB60H
Analog control A/D conversion value CHA (E2) (usr_rreg_1B1)	1000_BB62H
Analog control A/D conversion value CHB (E2) (usr_rreg_1B2)	1000_BB64H

■Description

Stores the A/D conversion value.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Counter control part 32-bit ring counter (2-phase multiple of 4) counter value

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B0) (usr_rreg_1B3)	1000_BB66H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B0) (usr_rreg_1B4)	1000_BB68H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B1) (usr_rreg_1B5)	1000_BB6AH
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B1) (usr_rreg_1B6)	1000_BB6CH
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (B2) (usr_rreg_1B7)	1000_BB6EH
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (B2) (usr_rreg_1B8)	1000_BB70H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E0) (usr_rreg_1B9)	1000_BB72H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E0) (usr_rreg_1BA)	1000_BB74H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E1) (usr_rreg_1BB)	1000_BB76H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E1) (usr_rreg_1BC)	1000_BB78H
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (lower side) (E2) (usr_rreg_1BD)	1000_BB7AH
Counter control part 32-bit ring counter (2-phase multiple of 4) counter value (upper side) (E2) (usr_rreg_1BE)	1000_BB7CH

■Description

Stores the counter (2-phase multiple of 4).

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Counter control part 32-bit ring counter (1-phase multiple of 1) counter value

■Address

Name	FPGA register address
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B0) (usr_rreg_1BF)	1000_BB7EH
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B0) (usr_rreg_1C0)	1000_BB80H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B1) (usr_rreg_1C1)	1000_BB82H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B1) (usr_rreg_1C2)	1000_BB84H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (B2) (usr_rreg_1C3)	1000_BB86H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (B2) (usr_rreg_1C4)	1000_BB88H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E0) (usr_rreg_1C5)	1000_BB8AH
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E0) (usr_rreg_1C6)	1000_BB8CH
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E1) (usr_rreg_1C7)	1000_BB8EH
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E1) (usr_rreg_1C8)	1000_BB90H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (lower side) (E2) (usr_rreg_1C9)	1000_BB92H
Counter control part 32-bit ring counter (1-phase multiple of 1) counter value (upper side) (E2) (usr_rreg_1CA)	1000_BB94H

■Description

Stores the counter (1-phase multiple of 1).

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Pulse output part output pulse count

■Address

Name	FPGA register address
Pulse output part output pulse count (lower side) (B0) (usr_rreg_1CB)	1000_BB96H
Pulse output part output pulse count (upper side) (B0) (usr_rreg_1CC)	1000_BB98H
Pulse output part output pulse count (lower side) (B1) (usr_rreg_1CD)	1000_BB9AH
Pulse output part output pulse count (upper side) (B1) (usr_rreg_1CE)	1000_BB9CH
Pulse output part output pulse count (lower side) (B2) (usr_rreg_1CF)	1000_BB9EH
Pulse output part output pulse count (upper side) (B2) (usr_rreg_1D0)	1000_BBA0H
Pulse output part output pulse count (lower side) (E0) (usr_rreg_1D1)	1000_BBA2H
Pulse output part output pulse count (upper side) (E0) (usr_rreg_1D2)	1000_BBA4H
Pulse output part output pulse count (lower side) (E1) (usr_rreg_1D3)	1000_BBA6H
Pulse output part output pulse count (upper side) (E1) (usr_rreg_1D4)	1000_BBA8H
Pulse output part output pulse count (lower side) (E2) (usr_rreg_1D5)	1000_BBAAH
Pulse output part output pulse count (upper side) (E2) (usr_rreg_1D6)	1000_BBACH

■Description

Counts the number of pulse outputs.

■FPGA initial value

0000H

■Firmware initial value

—

■Reset cause

Reset

Maximum A/D conversion value

■Address

Name	FPGA register address
Maximum A/D conversion value CH0 (usr_rreg_1D7)	1000_BBAEH
Maximum A/D conversion value CH1 (usr_rreg_1D8)	1000_BBB0H
Maximum A/D conversion value CH2 (usr_rreg_1D9)	1000_BBB2H
Maximum A/D conversion value CH3 (usr_rreg_1DA)	1000_BBB4H
Maximum A/D conversion value CH4 (usr_rreg_1DB)	1000_BBB6H
Maximum A/D conversion value CH5 (usr_rreg_1DC)	1000_BBB8H
Maximum A/D conversion value CH6 (usr_rreg_1DD)	1000_BBBAH
Maximum A/D conversion value CH7 (usr_rreg_1DE)	1000_BBBCH
Maximum A/D conversion value CH8 (usr_rreg_1DF)	1000_BBBEH
Maximum A/D conversion value CH9 (usr_rreg_1E0)	1000_BBC0H
Maximum A/D conversion value CHA (usr_rreg_1E1)	1000_BBC2H
Maximum A/D conversion value CHB (usr_rreg_1E2)	1000_BBC4H

■Description

Stores the maximum A/D conversion value of the circuit board selected by the maximum/minimum A/D conversion value selection register.

■FPGA initial value

8000H

■Firmware initial value

—

■Reset cause

Reset

Minimum A/D conversion value

■Address

Name	FPGA register address
Minimum A/D conversion value CH0 (usr_rreg_1E3)	1000_BBC6H
Minimum A/D conversion value CH1 (usr_rreg_1E4)	1000_BBC8H
Minimum A/D conversion value CH2 (usr_rreg_1E5)	1000_BBCAH
Minimum A/D conversion value CH3 (usr_rreg_1E6)	1000_BBCCH
Minimum A/D conversion value CH4 (usr_rreg_1E7)	1000_BBCEH
Minimum A/D conversion value CH5 (usr_rreg_1E8)	1000_BBD0H
Minimum A/D conversion value CH6 (usr_rreg_1E9)	1000_BBD2H
Minimum A/D conversion value CH7 (usr_rreg_1EA)	1000_BBD4H
Minimum A/D conversion value CH8 (usr_rreg_1EB)	1000_BBD6H
Minimum A/D conversion value CH9 (usr_rreg_1EC)	1000_BBD8H
Minimum A/D conversion value CHA (usr_rreg_1ED)	1000_BBDAH
Minimum A/D conversion value CHB (usr_rreg_1EE)	1000_BBDCH

■Description

Stores the minimum A/D conversion value of the circuit board selected by the maximum/minimum A/D conversion value selection register.

■FPGA initial value

7FFFH

■Firmware initial value

—

■Reset cause

Reset

Appendix 5 List of User Circuit Block Terminals

The list of external terminals of the user circuit block is shown below.

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Clock control part	u_cc2_top	clk100m	System clock	1	Input	—	0H	—	—	—
Reset control part	u_rc2_top	rst_n	System reset (OR of reset and S/W reset)	1	Input	L	0H	—	—	—
Digital input control part	u_di2_top_b0	di_iob0_x_clk100m_reg	Digital input signal (B0 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital input control part	u_di2_top_b1	di_iob1_x_clk100m_reg	Digital input signal (B1 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital input control part	u_di2_top_b2	di_iob2_x_clk100m_reg	Digital input signal (B2 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital input control part	u_di2_top_e0	di_ioe0_x_clk100m_reg	Digital input signal (E0 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital input control part	u_di2_top_e1	di_ioe1_x_clk100m_reg	Digital input signal (E1 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital input control part	u_di2_top_e2	di_ioe2_x_clk100m_reg	Digital input signal (E2 after filtering)	16	Input	—	0000H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b0	dio_iob0_dio485_i_clk100m_reg	Digital input signal (digital I/O B0 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b1	dio_iob1_dio485_i_clk100m_reg	Digital input signal (digital I/O B1 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b2	dio_iob2_dio485_i_clk100m_reg	Digital input signal (digital I/O B2 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e0	dio_ioe0_dio485_i_clk100m_reg	Digital input signal (digital I/O E0 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e1	dio_ioe1_dio485_i_clk100m_reg	Digital input signal (digital I/O E1 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e2	dio_ioe2_dio485_i_clk100m_reg	Digital input signal (digital I/O E2 after filtering)	1	Input	—	0H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_vald_clk100m_reg	A/D conversion value enable (E0)	1	Input	—	0H	○	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_0_clk100m_reg	A/D conversion value CH0(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_1_clk100m_reg	A/D conversion value CH1(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_2_clk100m_reg	A/D conversion value CH2(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_3_clk100m_reg	A/D conversion value CH3(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_4_clk100m_reg	A/D conversion value CH4(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_5_clk100m_reg	A/D conversion value CH5(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_6_clk100m_reg	A/D conversion value CH6(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_7_clk100m_reg	A/D conversion value CH7(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_8_clk100m_reg	A/D conversion value CH8(E0)	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_9_clk100m_reg	A/D conversion value CH9(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_a_clk100m_reg	A/D conversion value CHA(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0	ai_ioe0_aival_b_clk100m_reg	A/D conversion value CHB(E0)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_vald_clk100m_reg	A/D conversion value enable (E1)	1	Input	—	0H	○	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_0_clk100m_reg	A/D conversion value CH0(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_1_clk100m_reg	A/D conversion value CH1(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_2_clk100m_reg	A/D conversion value CH2(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_3_clk100m_reg	A/D conversion value CH3(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_4_clk100m_reg	A/D conversion value CH4(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_5_clk100m_reg	A/D conversion value CH5(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_6_clk100m_reg	A/D conversion value CH6(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_7_clk100m_reg	A/D conversion value CH7(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_8_clk100m_reg	A/D conversion value CH8(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_9_clk100m_reg	A/D conversion value CH9(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_a_clk100m_reg	A/D conversion value CHA(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e1	ai_ioe1_aival_b_clk100m_reg	A/D conversion value CHB(E1)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_vald_clk100m_reg	A/D conversion value enable (E2)	1	Input	—	0H	○	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_0_clk100m_reg	A/D conversion value CH0(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_1_clk100m_reg	A/D conversion value CH1(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_2_clk100m_reg	A/D conversion value CH2(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_3_clk100m_reg	A/D conversion value CH3(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_4_clk100m_reg	A/D conversion value CH4(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_5_clk100m_reg	A/D conversion value CH5(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_6_clk100m_reg	A/D conversion value CH6(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_7_clk100m_reg	A/D conversion value CH7(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_8_clk100m_reg	A/D conversion value CH8(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_9_clk100m_reg	A/D conversion value CH9(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_a_clk100m_reg	A/D conversion value CHA(E2)	16	Input	—	0000H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e2	ai_ioe2_aival_b_clk100m_reg	A/D conversion value CHB(E2)	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Timing generator	u_tg2_top	tg_05us_tmgpulse_clk100m_1shot_reg	0.5us sampling pulse for user circuit	1	Input	H	0H	○	100MHz	clk100m
FPGA external	top1	IOB0_UNIT	Module type (B0)	4	Input	—	0H	—	100MHz	clk100m
FPGA external	top1	IOB1_UNIT	Module type (B1)	4	Input	—	0H	—	100MHz	clk100m
FPGA external	top1	IOB2_UNIT	Module type (B2)	4	Input	—	0H	—	100MHz	clk100m
FPGA external	top1	IOE_UNIT	Module type (E0, E1, E2)	5	Input	—	00H	—	100MHz	clk100m
FPGA external	top1	cpu_intpl_in	General-purpose input (for future extension)	3	Input	—	7H	—	100MHz	clk100m
Register part	u_re2_top	re_rd_mode_ctrl2_0_clk100m_reg	Internal operation start/stop	1	Input	H	0H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_00_clk100m_reg	Always write register 0	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_01_clk100m_reg	Always write register 1	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_02_clk100m_reg	Always write register 2	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_03_clk100m_reg	Always write register 3	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_04_clk100m_reg	Always write register 4	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_05_clk100m_reg	Always write register 5	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_06_clk100m_reg	Always write register 6	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_07_clk100m_reg	Always write register 7	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_08_clk100m_reg	Always write register 8	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_09_clk100m_reg	Always write register 9	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0a_clk100m_reg	Always write register 10	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0b_clk100m_reg	Always write register 11	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0c_clk100m_reg	Always write register 12	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0d_clk100m_reg	Always write register 13	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0e_clk100m_reg	Always write register 14	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_alwreg_0f_clk100m_reg	Always write register 15	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_000_clk100m_reg	Write data 0	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_001_clk100m_reg	Write data 1	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_002_clk100m_reg	Write data 2	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_003_clk100m_reg	Write data 3	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_004_clk100m_reg	Write data 4	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_005_clk100m_reg	Write data 5	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_006_clk100m_reg	Write data 6	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_007_clk100m_reg	Write data 7	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_008_clk100m_reg	Write data 8	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_009_clk100m_reg	Write data 9	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00a_clk100m_reg	Write data 10	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00b_clk100m_reg	Write data 11	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00c_clk100m_reg	Write data 12	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00d_clk100m_reg	Write data 13	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00e_clk100m_reg	Write data 14	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_00f_clk100m_reg	Write data 15	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_010_clk100m_reg	Write data 16	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_011_clk100m_reg	Write data 17	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_012_clk100m_reg	Write data 18	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_013_clk100m_reg	Write data 19	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_014_clk100m_reg	Write data 20	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_015_clk100m_reg	Write data 21	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_016_clk100m_reg	Write data 22	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_017_clk100m_reg	Write data 23	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_018_clk100m_reg	Write data 24	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_019_clk100m_reg	Write data 25	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01a_clk100m_reg	Write data 26	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01b_clk100m_reg	Write data 27	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01c_clk100m_reg	Write data 28	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01d_clk100m_reg	Write data 29	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01e_clk100m_reg	Write data 30	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_01f_clk100m_reg	Write data 31	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_020_clk100m_reg	Write data 32	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_021_clk100m_reg	Write data 33	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_022_clk100m_reg	Write data 34	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_023_clk100m_reg	Write data 35	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_024_clk100m_reg	Write data 36	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_025_clk100m_reg	Write data 37	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_026_clk100m_reg	Write data 38	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_027_clk100m_reg	Write data 39	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_028_clk100m_reg	Write data 40	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_029_clk100m_reg	Write data 41	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02a_clk100m_reg	Write data 42	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02b_clk100m_reg	Write data 43	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02c_clk100m_reg	Write data 44	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02d_clk100m_reg	Write data 45	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02e_clk100m_reg	Write data 46	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_02f_clk100m_reg	Write data 47	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_030_clk100m_reg	Write data 48	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_031_clk100m_reg	Write data 49	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_032_clk100m_reg	Write data 50	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_033_clk100m_reg	Write data 51	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_034_clk100m_reg	Write data 52	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_035_clk100m_reg	Write data 53	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_036_clk100m_reg	Write data 54	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_037_clk100m_reg	Write data 55	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_038_clk100m_reg	Write data 56	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_039_clk100m_reg	Write data 57	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03a_clk100m_reg	Write data 58	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03b_clk100m_reg	Write data 59	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03c_clk100m_reg	Write data 60	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03d_clk100m_reg	Write data 61	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03e_clk100m_reg	Write data 62	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_03f_clk100m_reg	Write data 63	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_040_clk100m_reg	Write data 64	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_041_clk100m_reg	Write data 65	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_042_clk100m_reg	Write data 66	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_043_clk100m_reg	Write data 67	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_044_clk100m_reg	Write data 68	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_045_clk100m_reg	Write data 69	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_046_clk100m_reg	Write data 70	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_047_clk100m_reg	Write data 71	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_048_clk100m_reg	Write data 72	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_049_clk100m_reg	Write data 73	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04a_clk100m_reg	Write data 74	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04b_clk100m_reg	Write data 75	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04c_clk100m_reg	Write data 76	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04d_clk100m_reg	Write data 77	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04e_clk100m_reg	Write data 78	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_04f_clk100m_reg	Write data 79	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_050_clk100m_reg	Write data 80	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_051_clk100m_reg	Write data 81	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_052_clk100m_reg	Write data 82	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_053_clk100m_reg	Write data 83	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_054_clk100m_reg	Write data 84	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_055_clk100m_reg	Write data 85	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_056_clk100m_reg	Write data 86	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_057_clk100m_reg	Write data 87	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_058_clk100m_reg	Write data 88	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_059_clk100m_reg	Write data 89	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_05a_clk100m_reg	Write data 90	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_05b_clk100m_reg	Write data 91	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_05c_clk100m_reg	Write data 92	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_05d_clk100m_reg	Write data 93	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_05e_clk100m_reg	Write data 94	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_05f_clk100m_reg	Write data 95	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_060_clk100m_reg	Write data 96	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_061_clk100m_reg	Write data 97	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_062_clk100m_reg	Write data 98	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_063_clk100m_reg	Write data 99	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_064_clk100m_reg	Write data 100	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_065_clk100m_reg	Write data 101	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_066_clk100m_reg	Write data 102	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_067_clk100m_reg	Write data 103	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_068_clk100m_reg	Write data 104	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_069_clk100m_reg	Write data 105	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06a_clk100m_reg	Write data 106	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06b_clk100m_reg	Write data 107	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06c_clk100m_reg	Write data 108	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06d_clk100m_reg	Write data 109	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06e_clk100m_reg	Write data 110	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_06f_clk100m_reg	Write data 111	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_070_clk100m_reg	Write data 112	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_071_clk100m_reg	Write data 113	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_072_clk100m_reg	Write data 114	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_073_clk100m_reg	Write data 115	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_074_clk100m_reg	Write data 116	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_075_clk100m_reg	Write data 117	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_076_clk100m_reg	Write data 118	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_077_clk100m_reg	Write data 119	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_078_clk100m_reg	Write data 120	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_079_clk100m_reg	Write data 121	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_07a_clk100m_reg	Write data 122	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_07b_clk100m_reg	Write data 123	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_07c_clk100m_reg	Write data 124	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_07d_clk100m_reg	Write data 125	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_07e_clk100m_reg	Write data 126	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_07f_clk100m_reg	Write data 127	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_080_clk100m_reg	Write data 128	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_081_clk100m_reg	Write data 129	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_082_clk100m_reg	Write data 130	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_083_clk100m_reg	Write data 131	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_084_clk100m_reg	Write data 132	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_085_clk100m_reg	Write data 133	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_086_clk100m_reg	Write data 134	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_087_clk100m_reg	Write data 135	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_088_clk100m_reg	Write data 136	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_089_clk100m_reg	Write data 137	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08a_clk100m_reg	Write data 138	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08b_clk100m_reg	Write data 139	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08c_clk100m_reg	Write data 140	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08d_clk100m_reg	Write data 141	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08e_clk100m_reg	Write data 142	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_08f_clk100m_reg	Write data 143	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_090_clk100m_reg	Write data 144	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_091_clk100m_reg	Write data 145	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_092_clk100m_reg	Write data 146	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_093_clk100m_reg	Write data 147	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_094_clk100m_reg	Write data 148	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_095_clk100m_reg	Write data 149	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_096_clk100m_reg	Write data 150	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_097_clk100m_reg	Write data 151	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_098_clk100m_reg	Write data 152	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_099_clk100m_reg	Write data 153	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09a_clk100m_reg	Write data 154	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09b_clk100m_reg	Write data 155	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09c_clk100m_reg	Write data 156	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09d_clk100m_reg	Write data 157	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09e_clk100m_reg	Write data 158	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_09f_clk100m_reg	Write data 159	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a0_clk100m_reg	Write data 160	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a1_clk100m_reg	Write data 161	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a2_clk100m_reg	Write data 162	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a3_clk100m_reg	Write data 163	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a4_clk100m_reg	Write data 164	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a5_clk100m_reg	Write data 165	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a6_clk100m_reg	Write data 166	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a7_clk100m_reg	Write data 167	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a8_clk100m_reg	Write data 168	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0a9_clk100m_reg	Write data 169	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0aa_clk100m_reg	Write data 170	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ab_clk100m_reg	Write data 171	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ac_clk100m_reg	Write data 172	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ad_clk100m_reg	Write data 173	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ae_clk100m_reg	Write data 174	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0af_clk100m_reg	Write data 175	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b0_clk100m_reg	Write data 176	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b1_clk100m_reg	Write data 177	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b2_clk100m_reg	Write data 178	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b3_clk100m_reg	Write data 179	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_0b4_clk100m_reg	Write data 180	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b5_clk100m_reg	Write data 181	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b6_clk100m_reg	Write data 182	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b7_clk100m_reg	Write data 183	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b8_clk100m_reg	Write data 184	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0b9_clk100m_reg	Write data 185	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ba_clk100m_reg	Write data 186	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0bb_clk100m_reg	Write data 187	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0bc_clk100m_reg	Write data 188	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0bd_clk100m_reg	Write data 189	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0be_clk100m_reg	Write data 190	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0bf_clk100m_reg	Write data 191	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c0_clk100m_reg	Write data 192	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c1_clk100m_reg	Write data 193	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c2_clk100m_reg	Write data 194	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c3_clk100m_reg	Write data 195	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c4_clk100m_reg	Write data 196	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c5_clk100m_reg	Write data 197	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c6_clk100m_reg	Write data 198	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c7_clk100m_reg	Write data 199	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c8_clk100m_reg	Write data 200	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0c9_clk100m_reg	Write data 201	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ca_clk100m_reg	Write data 202	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0cb_clk100m_reg	Write data 203	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0cc_clk100m_reg	Write data 204	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0cd_clk100m_reg	Write data 205	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ce_clk100m_reg	Write data 206	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0cf_clk100m_reg	Write data 207	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d0_clk100m_reg	Write data 208	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_0d1_clk100m_reg	Write data 209	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d2_clk100m_reg	Write data 210	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d3_clk100m_reg	Write data 211	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d4_clk100m_reg	Write data 212	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d5_clk100m_reg	Write data 213	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d6_clk100m_reg	Write data 214	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d7_clk100m_reg	Write data 215	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d8_clk100m_reg	Write data 216	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0d9_clk100m_reg	Write data 217	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0da_clk100m_reg	Write data 218	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0db_clk100m_reg	Write data 219	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0dc_clk100m_reg	Write data 220	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0dd_clk100m_reg	Write data 221	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0de_clk100m_reg	Write data 222	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0df_clk100m_reg	Write data 223	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e0_clk100m_reg	Write data 224	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e1_clk100m_reg	Write data 225	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e2_clk100m_reg	Write data 226	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e3_clk100m_reg	Write data 227	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e4_clk100m_reg	Write data 228	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e5_clk100m_reg	Write data 229	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e6_clk100m_reg	Write data 230	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e7_clk100m_reg	Write data 231	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e8_clk100m_reg	Write data 232	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0e9_clk100m_reg	Write data 233	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ea_clk100m_reg	Write data 234	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0eb_clk100m_reg	Write data 235	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ec_clk100m_reg	Write data 236	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ed_clk100m_reg	Write data 237	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_0ee_clk100m_reg	Write data 238	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ef_clk100m_reg	Write data 239	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f0_clk100m_reg	Write data 240	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f1_clk100m_reg	Write data 241	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f2_clk100m_reg	Write data 242	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f3_clk100m_reg	Write data 243	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f4_clk100m_reg	Write data 244	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f5_clk100m_reg	Write data 245	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f6_clk100m_reg	Write data 246	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f7_clk100m_reg	Write data 247	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f8_clk100m_reg	Write data 248	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0f9_clk100m_reg	Write data 249	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0fa_clk100m_reg	Write data 250	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0fb_clk100m_reg	Write data 251	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0fc_clk100m_reg	Write data 252	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0fd_clk100m_reg	Write data 253	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0fe_clk100m_reg	Write data 254	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_0ff_clk100m_reg	Write data 255	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_100_clk100m_reg	Write data 256	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_101_clk100m_reg	Write data 257	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_102_clk100m_reg	Write data 258	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_103_clk100m_reg	Write data 259	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_104_clk100m_reg	Write data 260	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_105_clk100m_reg	Write data 261	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_106_clk100m_reg	Write data 262	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_107_clk100m_reg	Write data 263	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_108_clk100m_reg	Write data 264	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_109_clk100m_reg	Write data 265	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_10a_clk100m_reg	Write data 266	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_10b_clk100m_reg	Write data 267	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_10c_clk100m_reg	Write data 268	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_10d_clk100m_reg	Write data 269	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_10e_clk100m_reg	Write data 270	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_10f_clk100m_reg	Write data 271	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_110_clk100m_reg	Write data 272	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_111_clk100m_reg	Write data 273	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_112_clk100m_reg	Write data 274	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_113_clk100m_reg	Write data 275	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_114_clk100m_reg	Write data 276	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_115_clk100m_reg	Write data 277	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_116_clk100m_reg	Write data 278	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_117_clk100m_reg	Write data 279	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_118_clk100m_reg	Write data 280	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_119_clk100m_reg	Write data 281	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11a_clk100m_reg	Write data 282	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11b_clk100m_reg	Write data 283	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11c_clk100m_reg	Write data 284	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11d_clk100m_reg	Write data 285	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11e_clk100m_reg	Write data 286	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_11f_clk100m_reg	Write data 287	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_120_clk100m_reg	Write data 288	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_121_clk100m_reg	Write data 289	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_122_clk100m_reg	Write data 290	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_123_clk100m_reg	Write data 291	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_124_clk100m_reg	Write data 292	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_125_clk100m_reg	Write data 293	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_126_clk100m_reg	Write data 294	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_127_clk100m_reg	Write data 295	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_128_clk100m_reg	Write data 296	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_129_clk100m_reg	Write data 297	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12a_clk100m_reg	Write data 298	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12b_clk100m_reg	Write data 299	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12c_clk100m_reg	Write data 300	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12d_clk100m_reg	Write data 301	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12e_clk100m_reg	Write data 302	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_12f_clk100m_reg	Write data 303	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_130_clk100m_reg	Write data 304	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_131_clk100m_reg	Write data 305	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_132_clk100m_reg	Write data 306	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_133_clk100m_reg	Write data 307	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_134_clk100m_reg	Write data 308	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_135_clk100m_reg	Write data 309	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_136_clk100m_reg	Write data 310	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_137_clk100m_reg	Write data 311	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_138_clk100m_reg	Write data 312	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_139_clk100m_reg	Write data 313	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13a_clk100m_reg	Write data 314	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13b_clk100m_reg	Write data 315	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13c_clk100m_reg	Write data 316	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13d_clk100m_reg	Write data 317	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13e_clk100m_reg	Write data 318	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_13f_clk100m_reg	Write data 319	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_140_clk100m_reg	Write data 320	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_141_clk100m_reg	Write data 321	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_142_clk100m_reg	Write data 322	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_143_clk100m_reg	Write data 323	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_144_clk100m_reg	Write data 324	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_145_clk100m_reg	Write data 325	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_146_clk100m_reg	Write data 326	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_147_clk100m_reg	Write data 327	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_148_clk100m_reg	Write data 328	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_149_clk100m_reg	Write data 329	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14a_clk100m_reg	Write data 330	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14b_clk100m_reg	Write data 331	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14c_clk100m_reg	Write data 332	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14d_clk100m_reg	Write data 333	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14e_clk100m_reg	Write data 334	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_14f_clk100m_reg	Write data 335	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_150_clk100m_reg	Write data 336	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_151_clk100m_reg	Write data 337	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_152_clk100m_reg	Write data 338	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_153_clk100m_reg	Write data 339	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_154_clk100m_reg	Write data 340	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_155_clk100m_reg	Write data 341	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_156_clk100m_reg	Write data 342	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_157_clk100m_reg	Write data 343	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_158_clk100m_reg	Write data 344	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_159_clk100m_reg	Write data 345	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15a_clk100m_reg	Write data 346	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15b_clk100m_reg	Write data 347	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15c_clk100m_reg	Write data 348	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15d_clk100m_reg	Write data 349	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15e_clk100m_reg	Write data 350	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_15f_clk100m_reg	Write data 351	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_160_clk100m_reg	Write data 352	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_161_clk100m_reg	Write data 353	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_162_clk100m_reg	Write data 354	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_163_clk100m_reg	Write data 355	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_164_clk100m_reg	Write data 356	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_165_clk100m_reg	Write data 357	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_166_clk100m_reg	Write data 358	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_167_clk100m_reg	Write data 359	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_168_clk100m_reg	Write data 360	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_169_clk100m_reg	Write data 361	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16a_clk100m_reg	Write data 362	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16b_clk100m_reg	Write data 363	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16c_clk100m_reg	Write data 364	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16d_clk100m_reg	Write data 365	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16e_clk100m_reg	Write data 366	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_16f_clk100m_reg	Write data 367	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_170_clk100m_reg	Write data 368	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_171_clk100m_reg	Write data 369	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_172_clk100m_reg	Write data 370	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_173_clk100m_reg	Write data 371	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_174_clk100m_reg	Write data 372	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_175_clk100m_reg	Write data 373	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_176_clk100m_reg	Write data 374	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_177_clk100m_reg	Write data 375	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_178_clk100m_reg	Write data 376	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_179_clk100m_reg	Write data 377	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_17a_clk100m_reg	Write data 378	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_17b_clk100m_reg	Write data 379	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_17c_clk100m_reg	Write data 380	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_17d_clk100m_reg	Write data 381	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_17e_clk100m_reg	Write data 382	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_17f_clk100m_reg	Write data 383	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_180_clk100m_reg	Write data 384	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_181_clk100m_reg	Write data 385	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_182_clk100m_reg	Write data 386	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_183_clk100m_reg	Write data 387	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_184_clk100m_reg	Write data 388	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_185_clk100m_reg	Write data 389	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_186_clk100m_reg	Write data 390	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_187_clk100m_reg	Write data 391	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_188_clk100m_reg	Write data 392	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_189_clk100m_reg	Write data 393	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18a_clk100m_reg	Write data 394	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18b_clk100m_reg	Write data 395	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18c_clk100m_reg	Write data 396	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18d_clk100m_reg	Write data 397	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18e_clk100m_reg	Write data 398	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_18f_clk100m_reg	Write data 399	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_190_clk100m_reg	Write data 400	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_191_clk100m_reg	Write data 401	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_192_clk100m_reg	Write data 402	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_193_clk100m_reg	Write data 403	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_194_clk100m_reg	Write data 404	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_195_clk100m_reg	Write data 405	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_196_clk100m_reg	Write data 406	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_197_clk100m_reg	Write data 407	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_198_clk100m_reg	Write data 408	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_199_clk100m_reg	Write data 409	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_19a_clk100m_reg	Write data 410	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_19b_clk100m_reg	Write data 411	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_19c_clk100m_reg	Write data 412	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_19d_clk100m_reg	Write data 413	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_19e_clk100m_reg	Write data 414	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_19f_clk100m_reg	Write data 415	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a0_clk100m_reg	Write data 416	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a1_clk100m_reg	Write data 417	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a2_clk100m_reg	Write data 418	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a3_clk100m_reg	Write data 419	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a4_clk100m_reg	Write data 420	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a5_clk100m_reg	Write data 421	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a6_clk100m_reg	Write data 422	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a7_clk100m_reg	Write data 423	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a8_clk100m_reg	Write data 424	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1a9_clk100m_reg	Write data 425	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1aa_clk100m_reg	Write data 426	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ab_clk100m_reg	Write data 427	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ac_clk100m_reg	Write data 428	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ad_clk100m_reg	Write data 429	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ae_clk100m_reg	Write data 430	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1af_clk100m_reg	Write data 431	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b0_clk100m_reg	Write data 432	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b1_clk100m_reg	Write data 433	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b2_clk100m_reg	Write data 434	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b3_clk100m_reg	Write data 435	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b4_clk100m_reg	Write data 436	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b5_clk100m_reg	Write data 437	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b6_clk100m_reg	Write data 438	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b7_clk100m_reg	Write data 439	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1b8_clk100m_reg	Write data 440	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_1b9_clk100m_reg	Write data 441	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ba_clk100m_reg	Write data 442	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1bb_clk100m_reg	Write data 443	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1bc_clk100m_reg	Write data 444	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1bd_clk100m_reg	Write data 445	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1be_clk100m_reg	Write data 446	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1bf_clk100m_reg	Write data 447	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c0_clk100m_reg	Write data 448	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c1_clk100m_reg	Write data 449	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c2_clk100m_reg	Write data 450	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c3_clk100m_reg	Write data 451	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c4_clk100m_reg	Write data 452	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c5_clk100m_reg	Write data 453	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c6_clk100m_reg	Write data 454	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c7_clk100m_reg	Write data 455	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c8_clk100m_reg	Write data 456	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1c9_clk100m_reg	Write data 457	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ca_clk100m_reg	Write data 458	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1cb_clk100m_reg	Write data 459	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1cc_clk100m_reg	Write data 460	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1cd_clk100m_reg	Write data 461	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ce_clk100m_reg	Write data 462	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1cf_clk100m_reg	Write data 463	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d0_clk100m_reg	Write data 464	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d1_clk100m_reg	Write data 465	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d2_clk100m_reg	Write data 466	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d3_clk100m_reg	Write data 467	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d4_clk100m_reg	Write data 468	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d5_clk100m_reg	Write data 469	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_1d6_clk100m_reg	Write data 470	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d7_clk100m_reg	Write data 471	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d8_clk100m_reg	Write data 472	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1d9_clk100m_reg	Write data 473	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1da_clk100m_reg	Write data 474	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1db_clk100m_reg	Write data 475	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1dc_clk100m_reg	Write data 476	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1dd_clk100m_reg	Write data 477	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1de_clk100m_reg	Write data 478	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1df_clk100m_reg	Write data 479	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e0_clk100m_reg	Write data 480	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e1_clk100m_reg	Write data 481	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e2_clk100m_reg	Write data 482	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e3_clk100m_reg	Write data 483	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e4_clk100m_reg	Write data 484	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e5_clk100m_reg	Write data 485	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e6_clk100m_reg	Write data 486	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e7_clk100m_reg	Write data 487	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e8_clk100m_reg	Write data 488	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1e9_clk100m_reg	Write data 489	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ea_clk100m_reg	Write data 490	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1eb_clk100m_reg	Write data 491	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ec_clk100m_reg	Write data 492	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ed_clk100m_reg	Write data 493	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ee_clk100m_reg	Write data 494	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ef_clk100m_reg	Write data 495	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f0_clk100m_reg	Write data 496	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f1_clk100m_reg	Write data 497	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f2_clk100m_reg	Write data 498	16	Input	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_wreg_1f3_clk100m_reg	Write data 499	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f4_clk100m_reg	Write data 500	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f5_clk100m_reg	Write data 501	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f6_clk100m_reg	Write data 502	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f7_clk100m_reg	Write data 503	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f8_clk100m_reg	Write data 504	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1f9_clk100m_reg	Write data 505	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1fa_clk100m_reg	Write data 506	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1fb_clk100m_reg	Write data 507	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1fc_clk100m_reg	Write data 508	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1fd_clk100m_reg	Write data 509	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1fe_clk100m_reg	Write data 510	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_wreg_1ff_clk100m_reg	Write data 511	16	Input	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_logmode_sel_1_0_clk100m_reg	User circuit logging mode selection	1	Input	—	0H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_micon_syserr_clk100m_reg	MCU system error notification	1	Input	—	0H	—	100MHz	clk100m
Digital output control part	u_do2_top_b0	uc_iob0_y_clk100m_reg	Digital output signal (B0)	16	Output	—	0000H	—	100MHz	clk100m
Digital output control part	u_do2_top_b1	uc_iob1_y_clk100m_reg	Digital output signal (B1)	16	Output	—	0000H	—	100MHz	clk100m
Digital output control part	u_do2_top_b2	uc_iob2_y_clk100m_reg	Digital output signal (B2)	16	Output	—	0000H	—	100MHz	clk100m
Digital output control part	u_do2_top_e0	uc_ioe0_y_clk100m_reg	Digital output signal (E0)	16	Output	—	0000H	—	100MHz	clk100m
Digital output control part	u_do2_top_e1	uc_ioe1_y_clk100m_reg	Digital output signal (E1)	16	Output	—	0000H	—	100MHz	clk100m
Digital output control part	u_do2_top_e2	uc_ioe2_y_clk100m_reg	Digital output signal (E2)	16	Output	—	0000H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b0	uc_iob0_dio485_o_clk100m_reg	Digital output signal (digital I/O B0)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b0	uc_iob0_dio485_en_clk100m_reg	Digital I/O control (B0)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b1	uc_iob1_dio485_o_clk100m_reg	Digital output signal (digital I/O B1)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b1	uc_iob1_dio485_en_clk100m_reg	Digital I/O control (B1)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b2	uc_iob2_dio485_o_clk100m_reg	Digital output signal (digital I/O B2)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_b2	uc_iob2_dio485_en_clk100m_reg	Digital I/O control (B2)	1	Output	—	0H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Digital I/O control part	u_dio2_top_e0	uc_ioe0_dio485_o_clk100m_reg	Digital output signal (digital I/O E0)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e0	uc_ioe0_dio485_en_clk100m_reg	Digital I/O control (E0)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e1	uc_ioe1_dio485_o_clk100m_reg	Digital output signal (digital I/O E1)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e1	uc_ioe1_dio485_en_clk100m_reg	Digital I/O control (E1)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e2	uc_ioe2_dio485_o_clk100m_reg	Digital output signal (digital I/O E2)	1	Output	—	0H	—	100MHz	clk100m
Digital I/O control part	u_dio2_top_e2	uc_ioe2_dio485_en_clk100m_reg	Digital I/O control (E2)	1	Output	—	0H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e0	uc_ioe0_andat_clk100m_reg	D/A conversion value (E0)	32	Output	—	00000000H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e0	uc_ioe0_andat_en_clk100m_reg	D/A conversion value enable (E0)	1	Output	H	0H	○	100MHz	clk100m
Analog output control part	u_ao2_top_e0	uc_ioe0_ldac_clk100m_reg	LDAC output (E0)	2	Output	—	0H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e1	uc_ioe1_andat_clk100m_reg	D/A conversion value (E1)	32	Output	—	00000000H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e1	uc_ioe1_andat_en_clk100m_reg	D/A conversion value enable (E1)	1	Output	H	0H	○	100MHz	clk100m
Analog output control part	u_ao2_top_e1	uc_ioe1_ldac_clk100m_reg	LDAC output (E1)	2	Output	—	0H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e2	uc_ioe2_andat_clk100m_reg	D/A conversion value (E2)	32	Output	—	00000000H	—	100MHz	clk100m
Analog output control part	u_ao2_top_e2	uc_ioe2_andat_en_clk100m_reg	D/A conversion value enable (E2)	1	Output	H	0H	○	100MHz	clk100m
Analog output control part	u_ao2_top_e2	uc_ioe2_ldac_clk100m_reg	LDAC output (E2)	2	Output	—	0H	—	100MHz	clk100m
Logging part	u_lf2_top	uc_logdat_clk100m_reg	Logging data	432	Output	—	ALL0H	—	100MHz	clk100m
Logging part	u_lf2_top	uc_logen_clk100m_reg	Logging enable	1	Output	H	0H	—	100MHz	clk100m
Logging part	u_lf2_top	uc_logend_clk100m_reg	Logging end trigger	1	Output	H	0H	—	100MHz	clk100m
Logging part	u_lf2_top	uc_loguserpulse_clk100m_reg	User sampling pulse	1	Output	H	0H	—	100MHz	clk100m
Register part	u_re2_top	uc_err_clk100m_reg	User circuit: error signal	1	Output	H	0H	—	100MHz	clk100m
FPGA external	top1	cpu_intpl_out	General-purpose output	3	Output	—	7H	—	100MHz	clk100m
Analog input control part	u_ai2_top_e0, u_ai2_top_e1, u_ai2_top_e2	uc_sampling_tmgpulse_clk100m_1shot_reg	User circuit: Data sampling pulse	6	Output	H	0H	○	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_00_clk100m_reg	Always read register 0	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_01_clk100m_reg	Always read register 1	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_02_clk100m_reg	Always read register 2	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_03_clk100m_reg	Always read register 3	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_04_clk100m_reg	Always read register 4	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	uc_rs_usr_alrreg_05_clk100m_reg	Always read register 5	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_06_clk100m_reg	Always read register 6	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_07_clk100m_reg	Always read register 7	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_08_clk100m_reg	Always read register 8	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_09_clk100m_reg	Always read register 9	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0a_clk100m_reg	Always read register 10	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0b_clk100m_reg	Always read register 11	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0c_clk100m_reg	Always read register 12	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0d_clk100m_reg	Always read register 13	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0e_clk100m_reg	Always read register 14	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	uc_rs_usr_alrreg_0f_clk100m_reg	Always read register 15	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_000_clk100m_reg	Read data 0	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_001_clk100m_reg	Read data 1	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_002_clk100m_reg	Read data 2	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_003_clk100m_reg	Read data 3	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_004_clk100m_reg	Read data 4	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_005_clk100m_reg	Read data 5	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_006_clk100m_reg	Read data 6	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_007_clk100m_reg	Read data 7	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_008_clk100m_reg	Read data 8	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_009_clk100m_reg	Read data 9	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00a_clk100m_reg	Read data 10	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00b_clk100m_reg	Read data 11	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00c_clk100m_reg	Read data 12	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00d_clk100m_reg	Read data 13	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00e_clk100m_reg	Read data 14	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_00f_clk100m_reg	Read data 15	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_010_clk100m_reg	Read data 16	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_011_clk100m_reg	Read data 17	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_012_clk100m_reg	Read data 18	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_013_clk100m_reg	Read data 19	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_014_clk100m_reg	Read data 20	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_015_clk100m_reg	Read data 21	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_016_clk100m_reg	Read data 22	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_017_clk100m_reg	Read data 23	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_018_clk100m_reg	Read data 24	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_019_clk100m_reg	Read data 25	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01a_clk100m_reg	Read data 26	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01b_clk100m_reg	Read data 27	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01c_clk100m_reg	Read data 28	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01d_clk100m_reg	Read data 29	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01e_clk100m_reg	Read data 30	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_01f_clk100m_reg	Read data 31	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_020_clk100m_reg	Read data 32	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_021_clk100m_reg	Read data 33	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_022_clk100m_reg	Read data 34	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_023_clk100m_reg	Read data 35	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_024_clk100m_reg	Read data 36	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_025_clk100m_reg	Read data 37	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_026_clk100m_reg	Read data 38	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_027_clk100m_reg	Read data 39	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_028_clk100m_reg	Read data 40	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_029_clk100m_reg	Read data 41	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_02a_clk100m_reg	Read data 42	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_02b_clk100m_reg	Read data 43	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_02c_clk100m_reg	Read data 44	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_02d_clk100m_reg	Read data 45	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_02e_clk100m_reg	Read data 46	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_02f_clk100m_reg	Read data 47	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_030_clk100m_reg	Read data 48	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_031_clk100m_reg	Read data 49	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_032_clk100m_reg	Read data 50	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_033_clk100m_reg	Read data 51	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_034_clk100m_reg	Read data 52	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_035_clk100m_reg	Read data 53	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_036_clk100m_reg	Read data 54	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_037_clk100m_reg	Read data 55	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_038_clk100m_reg	Read data 56	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_039_clk100m_reg	Read data 57	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03a_clk100m_reg	Read data 58	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03b_clk100m_reg	Read data 59	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03c_clk100m_reg	Read data 60	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03d_clk100m_reg	Read data 61	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03e_clk100m_reg	Read data 62	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_03f_clk100m_reg	Read data 63	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_040_clk100m_reg	Read data 64	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_041_clk100m_reg	Read data 65	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_042_clk100m_reg	Read data 66	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_043_clk100m_reg	Read data 67	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_044_clk100m_reg	Read data 68	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_045_clk100m_reg	Read data 69	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_046_clk100m_reg	Read data 70	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_047_clk100m_reg	Read data 71	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_048_clk100m_reg	Read data 72	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_049_clk100m_reg	Read data 73	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_04a_clk100m_reg	Read data 74	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_04b_clk100m_reg	Read data 75	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_04c_clk100m_reg	Read data 76	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_04d_clk100m_reg	Read data 77	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_04e_clk100m_reg	Read data 78	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_04f_clk100m_reg	Read data 79	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_050_clk100m_reg	Read data 80	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_051_clk100m_reg	Read data 81	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_052_clk100m_reg	Read data 82	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_053_clk100m_reg	Read data 83	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_054_clk100m_reg	Read data 84	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_055_clk100m_reg	Read data 85	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_056_clk100m_reg	Read data 86	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_057_clk100m_reg	Read data 87	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_058_clk100m_reg	Read data 88	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_059_clk100m_reg	Read data 89	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05a_clk100m_reg	Read data 90	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05b_clk100m_reg	Read data 91	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05c_clk100m_reg	Read data 92	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05d_clk100m_reg	Read data 93	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05e_clk100m_reg	Read data 94	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_05f_clk100m_reg	Read data 95	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_060_clk100m_reg	Read data 96	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_061_clk100m_reg	Read data 97	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_062_clk100m_reg	Read data 98	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_063_clk100m_reg	Read data 99	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_064_clk100m_reg	Read data 100	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_065_clk100m_reg	Read data 101	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_066_clk100m_reg	Read data 102	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_067_clk100m_reg	Read data 103	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_068_clk100m_reg	Read data 104	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_069_clk100m_reg	Read data 105	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06a_clk100m_reg	Read data 106	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06b_clk100m_reg	Read data 107	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06c_clk100m_reg	Read data 108	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06d_clk100m_reg	Read data 109	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06e_clk100m_reg	Read data 110	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_06f_clk100m_reg	Read data 111	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_070_clk100m_reg	Read data 112	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_071_clk100m_reg	Read data 113	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_072_clk100m_reg	Read data 114	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_073_clk100m_reg	Read data 115	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_074_clk100m_reg	Read data 116	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_075_clk100m_reg	Read data 117	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_076_clk100m_reg	Read data 118	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_077_clk100m_reg	Read data 119	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_078_clk100m_reg	Read data 120	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_079_clk100m_reg	Read data 121	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07a_clk100m_reg	Read data 122	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07b_clk100m_reg	Read data 123	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07c_clk100m_reg	Read data 124	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07d_clk100m_reg	Read data 125	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07e_clk100m_reg	Read data 126	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_07f_clk100m_reg	Read data 127	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_080_clk100m_reg	Read data 128	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_081_clk100m_reg	Read data 129	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_082_clk100m_reg	Read data 130	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_083_clk100m_reg	Read data 131	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_084_clk100m_reg	Read data 132	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_085_clk100m_reg	Read data 133	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_086_clk100m_reg	Read data 134	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_087_clk100m_reg	Read data 135	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_088_clk100m_reg	Read data 136	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_089_clk100m_reg	Read data 137	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08a_clk100m_reg	Read data 138	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08b_clk100m_reg	Read data 139	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08c_clk100m_reg	Read data 140	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08d_clk100m_reg	Read data 141	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08e_clk100m_reg	Read data 142	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_08f_clk100m_reg	Read data 143	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_090_clk100m_reg	Read data 144	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_091_clk100m_reg	Read data 145	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_092_clk100m_reg	Read data 146	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_093_clk100m_reg	Read data 147	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_094_clk100m_reg	Read data 148	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_095_clk100m_reg	Read data 149	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_096_clk100m_reg	Read data 150	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_097_clk100m_reg	Read data 151	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_098_clk100m_reg	Read data 152	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_099_clk100m_reg	Read data 153	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09a_clk100m_reg	Read data 154	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09b_clk100m_reg	Read data 155	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09c_clk100m_reg	Read data 156	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09d_clk100m_reg	Read data 157	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09e_clk100m_reg	Read data 158	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_09f_clk100m_reg	Read data 159	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a0_clk100m_reg	Read data 160	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a1_clk100m_reg	Read data 161	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a2_clk100m_reg	Read data 162	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_0a3_clk100m_reg	Read data 163	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a4_clk100m_reg	Read data 164	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a5_clk100m_reg	Read data 165	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a6_clk100m_reg	Read data 166	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a7_clk100m_reg	Read data 167	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a8_clk100m_reg	Read data 168	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0a9_clk100m_reg	Read data 169	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0aa_clk100m_reg	Read data 170	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ab_clk100m_reg	Read data 171	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ac_clk100m_reg	Read data 172	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ad_clk100m_reg	Read data 173	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ae_clk100m_reg	Read data 174	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0af_clk100m_reg	Read data 175	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b0_clk100m_reg	Read data 176	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b1_clk100m_reg	Read data 177	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b2_clk100m_reg	Read data 178	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b3_clk100m_reg	Read data 179	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b4_clk100m_reg	Read data 180	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b5_clk100m_reg	Read data 181	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b6_clk100m_reg	Read data 182	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b7_clk100m_reg	Read data 183	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b8_clk100m_reg	Read data 184	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0b9_clk100m_reg	Read data 185	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ba_clk100m_reg	Read data 186	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0bb_clk100m_reg	Read data 187	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0bc_clk100m_reg	Read data 188	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0bd_clk100m_reg	Read data 189	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0be_clk100m_reg	Read data 190	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0bf_clk100m_reg	Read data 191	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_0c0_clk100m_reg	Read data 192	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c1_clk100m_reg	Read data 193	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c2_clk100m_reg	Read data 194	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c3_clk100m_reg	Read data 195	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c4_clk100m_reg	Read data 196	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c5_clk100m_reg	Read data 197	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c6_clk100m_reg	Read data 198	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c7_clk100m_reg	Read data 199	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c8_clk100m_reg	Read data 200	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0c9_clk100m_reg	Read data 201	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ca_clk100m_reg	Read data 202	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0cb_clk100m_reg	Read data 203	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0cc_clk100m_reg	Read data 204	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0cd_clk100m_reg	Read data 205	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ce_clk100m_reg	Read data 206	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0cf_clk100m_reg	Read data 207	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d0_clk100m_reg	Read data 208	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d1_clk100m_reg	Read data 209	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d2_clk100m_reg	Read data 210	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d3_clk100m_reg	Read data 211	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d4_clk100m_reg	Read data 212	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d5_clk100m_reg	Read data 213	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d6_clk100m_reg	Read data 214	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d7_clk100m_reg	Read data 215	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d8_clk100m_reg	Read data 216	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0d9_clk100m_reg	Read data 217	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0da_clk100m_reg	Read data 218	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0db_clk100m_reg	Read data 219	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0dc_clk100m_reg	Read data 220	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_0dd_clk100m_reg	Read data 221	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0de_clk100m_reg	Read data 222	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0df_clk100m_reg	Read data 223	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e0_clk100m_reg	Read data 224	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e1_clk100m_reg	Read data 225	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e2_clk100m_reg	Read data 226	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e3_clk100m_reg	Read data 227	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e4_clk100m_reg	Read data 228	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e5_clk100m_reg	Read data 229	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e6_clk100m_reg	Read data 230	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e7_clk100m_reg	Read data 231	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e8_clk100m_reg	Read data 232	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0e9_clk100m_reg	Read data 233	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ea_clk100m_reg	Read data 234	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0eb_clk100m_reg	Read data 235	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ec_clk100m_reg	Read data 236	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ed_clk100m_reg	Read data 237	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ee_clk100m_reg	Read data 238	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ef_clk100m_reg	Read data 239	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f0_clk100m_reg	Read data 240	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f1_clk100m_reg	Read data 241	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f2_clk100m_reg	Read data 242	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f3_clk100m_reg	Read data 243	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f4_clk100m_reg	Read data 244	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f5_clk100m_reg	Read data 245	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f6_clk100m_reg	Read data 246	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f7_clk100m_reg	Read data 247	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f8_clk100m_reg	Read data 248	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0f9_clk100m_reg	Read data 249	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_0fa_clk100m_reg	Read data 250	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0fb_clk100m_reg	Read data 251	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0fc_clk100m_reg	Read data 252	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0fd_clk100m_reg	Read data 253	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0fe_clk100m_reg	Read data 254	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_0ff_clk100m_reg	Read data 255	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_100_clk100m_reg	Read data 256	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_101_clk100m_reg	Read data 257	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_102_clk100m_reg	Read data 258	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_103_clk100m_reg	Read data 259	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_104_clk100m_reg	Read data 260	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_105_clk100m_reg	Read data 261	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_106_clk100m_reg	Read data 262	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_107_clk100m_reg	Read data 263	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_108_clk100m_reg	Read data 264	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_109_clk100m_reg	Read data 265	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10a_clk100m_reg	Read data 266	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10b_clk100m_reg	Read data 267	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10c_clk100m_reg	Read data 268	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10d_clk100m_reg	Read data 269	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10e_clk100m_reg	Read data 270	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_10f_clk100m_reg	Read data 271	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_110_clk100m_reg	Read data 272	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_111_clk100m_reg	Read data 273	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_112_clk100m_reg	Read data 274	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_113_clk100m_reg	Read data 275	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_114_clk100m_reg	Read data 276	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_115_clk100m_reg	Read data 277	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_116_clk100m_reg	Read data 278	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_117_clk100m_reg	Read data 279	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_118_clk100m_reg	Read data 280	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_119_clk100m_reg	Read data 281	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11a_clk100m_reg	Read data 282	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11b_clk100m_reg	Read data 283	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11c_clk100m_reg	Read data 284	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11d_clk100m_reg	Read data 285	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11e_clk100m_reg	Read data 286	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_11f_clk100m_reg	Read data 287	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_120_clk100m_reg	Read data 288	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_121_clk100m_reg	Read data 289	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_122_clk100m_reg	Read data 290	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_123_clk100m_reg	Read data 291	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_124_clk100m_reg	Read data 292	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_125_clk100m_reg	Read data 293	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_126_clk100m_reg	Read data 294	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_127_clk100m_reg	Read data 295	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_128_clk100m_reg	Read data 296	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_129_clk100m_reg	Read data 297	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12a_clk100m_reg	Read data 298	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12b_clk100m_reg	Read data 299	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12c_clk100m_reg	Read data 300	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12d_clk100m_reg	Read data 301	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12e_clk100m_reg	Read data 302	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_12f_clk100m_reg	Read data 303	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_130_clk100m_reg	Read data 304	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_131_clk100m_reg	Read data 305	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_132_clk100m_reg	Read data 306	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_133_clk100m_reg	Read data 307	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_134_clk100m_reg	Read data 308	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_135_clk100m_reg	Read data 309	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_136_clk100m_reg	Read data 310	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_137_clk100m_reg	Read data 311	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_138_clk100m_reg	Read data 312	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_139_clk100m_reg	Read data 313	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13a_clk100m_reg	Read data 314	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13b_clk100m_reg	Read data 315	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13c_clk100m_reg	Read data 316	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13d_clk100m_reg	Read data 317	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13e_clk100m_reg	Read data 318	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_13f_clk100m_reg	Read data 319	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_140_clk100m_reg	Read data 320	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_141_clk100m_reg	Read data 321	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_142_clk100m_reg	Read data 322	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_143_clk100m_reg	Read data 323	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_144_clk100m_reg	Read data 324	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_145_clk100m_reg	Read data 325	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_146_clk100m_reg	Read data 326	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_147_clk100m_reg	Read data 327	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_148_clk100m_reg	Read data 328	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_149_clk100m_reg	Read data 329	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14a_clk100m_reg	Read data 330	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14b_clk100m_reg	Read data 331	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14c_clk100m_reg	Read data 332	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14d_clk100m_reg	Read data 333	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14e_clk100m_reg	Read data 334	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_14f_clk100m_reg	Read data 335	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_150_clk100m_reg	Read data 336	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_151_clk100m_reg	Read data 337	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_152_clk100m_reg	Read data 338	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_153_clk100m_reg	Read data 339	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_154_clk100m_reg	Read data 340	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_155_clk100m_reg	Read data 341	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_156_clk100m_reg	Read data 342	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_157_clk100m_reg	Read data 343	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_158_clk100m_reg	Read data 344	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_159_clk100m_reg	Read data 345	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15a_clk100m_reg	Read data 346	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15b_clk100m_reg	Read data 347	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15c_clk100m_reg	Read data 348	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15d_clk100m_reg	Read data 349	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15e_clk100m_reg	Read data 350	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_15f_clk100m_reg	Read data 351	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_160_clk100m_reg	Read data 352	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_161_clk100m_reg	Read data 353	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_162_clk100m_reg	Read data 354	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_163_clk100m_reg	Read data 355	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_164_clk100m_reg	Read data 356	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_165_clk100m_reg	Read data 357	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_166_clk100m_reg	Read data 358	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_167_clk100m_reg	Read data 359	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_168_clk100m_reg	Read data 360	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_169_clk100m_reg	Read data 361	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_16a_clk100m_reg	Read data 362	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_16b_clk100m_reg	Read data 363	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_16c_clk100m_reg	Read data 364	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_16d_clk100m_reg	Read data 365	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_16e_clk100m_reg	Read data 366	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_16f_clk100m_reg	Read data 367	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_170_clk100m_reg	Read data 368	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_171_clk100m_reg	Read data 369	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_172_clk100m_reg	Read data 370	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_173_clk100m_reg	Read data 371	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_174_clk100m_reg	Read data 372	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_175_clk100m_reg	Read data 373	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_176_clk100m_reg	Read data 374	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_177_clk100m_reg	Read data 375	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_178_clk100m_reg	Read data 376	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_179_clk100m_reg	Read data 377	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17a_clk100m_reg	Read data 378	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17b_clk100m_reg	Read data 379	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17c_clk100m_reg	Read data 380	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17d_clk100m_reg	Read data 381	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17e_clk100m_reg	Read data 382	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_17f_clk100m_reg	Read data 383	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_180_clk100m_reg	Read data 384	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_181_clk100m_reg	Read data 385	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_182_clk100m_reg	Read data 386	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_183_clk100m_reg	Read data 387	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_184_clk100m_reg	Read data 388	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_185_clk100m_reg	Read data 389	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_186_clk100m_reg	Read data 390	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_187_clk100m_reg	Read data 391	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_188_clk100m_reg	Read data 392	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_189_clk100m_reg	Read data 393	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_18a_clk100m_reg	Read data 394	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_18b_clk100m_reg	Read data 395	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_18c_clk100m_reg	Read data 396	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_18d_clk100m_reg	Read data 397	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_18e_clk100m_reg	Read data 398	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_18f_clk100m_reg	Read data 399	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_190_clk100m_reg	Read data 400	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_191_clk100m_reg	Read data 401	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_192_clk100m_reg	Read data 402	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_193_clk100m_reg	Read data 403	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_194_clk100m_reg	Read data 404	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_195_clk100m_reg	Read data 405	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_196_clk100m_reg	Read data 406	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_197_clk100m_reg	Read data 407	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_198_clk100m_reg	Read data 408	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_199_clk100m_reg	Read data 409	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19a_clk100m_reg	Read data 410	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19b_clk100m_reg	Read data 411	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19c_clk100m_reg	Read data 412	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19d_clk100m_reg	Read data 413	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19e_clk100m_reg	Read data 414	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_19f_clk100m_reg	Read data 415	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a0_clk100m_reg	Read data 416	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a1_clk100m_reg	Read data 417	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a2_clk100m_reg	Read data 418	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a3_clk100m_reg	Read data 419	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a4_clk100m_reg	Read data 420	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a5_clk100m_reg	Read data 421	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a6_clk100m_reg	Read data 422	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a7_clk100m_reg	Read data 423	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_1a8_clk100m_reg	Read data 424	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1a9_clk100m_reg	Read data 425	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1aa_clk100m_reg	Read data 426	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ab_clk100m_reg	Read data 427	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ac_clk100m_reg	Read data 428	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ad_clk100m_reg	Read data 429	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ae_clk100m_reg	Read data 430	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1af_clk100m_reg	Read data 431	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b0_clk100m_reg	Read data 432	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b1_clk100m_reg	Read data 433	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b2_clk100m_reg	Read data 434	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b3_clk100m_reg	Read data 435	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b4_clk100m_reg	Read data 436	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b5_clk100m_reg	Read data 437	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b6_clk100m_reg	Read data 438	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b7_clk100m_reg	Read data 439	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b8_clk100m_reg	Read data 440	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1b9_clk100m_reg	Read data 441	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ba_clk100m_reg	Read data 442	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1bb_clk100m_reg	Read data 443	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1bc_clk100m_reg	Read data 444	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1bd_clk100m_reg	Read data 445	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1be_clk100m_reg	Read data 446	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1bf_clk100m_reg	Read data 447	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c0_clk100m_reg	Read data 448	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c1_clk100m_reg	Read data 449	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c2_clk100m_reg	Read data 450	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c3_clk100m_reg	Read data 451	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c4_clk100m_reg	Read data 452	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_1c5_clk100m_reg	Read data 453	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c6_clk100m_reg	Read data 454	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c7_clk100m_reg	Read data 455	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c8_clk100m_reg	Read data 456	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1c9_clk100m_reg	Read data 457	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ca_clk100m_reg	Read data 458	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1cb_clk100m_reg	Read data 459	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1cc_clk100m_reg	Read data 460	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1cd_clk100m_reg	Read data 461	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ce_clk100m_reg	Read data 462	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1cf_clk100m_reg	Read data 463	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d0_clk100m_reg	Read data 464	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d1_clk100m_reg	Read data 465	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d2_clk100m_reg	Read data 466	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d3_clk100m_reg	Read data 467	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d4_clk100m_reg	Read data 468	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d5_clk100m_reg	Read data 469	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d6_clk100m_reg	Read data 470	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d7_clk100m_reg	Read data 471	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d8_clk100m_reg	Read data 472	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1d9_clk100m_reg	Read data 473	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1da_clk100m_reg	Read data 474	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1db_clk100m_reg	Read data 475	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1dc_clk100m_reg	Read data 476	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1dd_clk100m_reg	Read data 477	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1de_clk100m_reg	Read data 478	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1df_clk100m_reg	Read data 479	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e0_clk100m_reg	Read data 480	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e1_clk100m_reg	Read data 481	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_1e2_clk100m_reg	Read data 482	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e3_clk100m_reg	Read data 483	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e4_clk100m_reg	Read data 484	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e5_clk100m_reg	Read data 485	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e6_clk100m_reg	Read data 486	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e7_clk100m_reg	Read data 487	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e8_clk100m_reg	Read data 488	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1e9_clk100m_reg	Read data 489	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ea_clk100m_reg	Read data 490	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1eb_clk100m_reg	Read data 491	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ec_clk100m_reg	Read data 492	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ed_clk100m_reg	Read data 493	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ee_clk100m_reg	Read data 494	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1ef_clk100m_reg	Read data 495	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f0_clk100m_reg	Read data 496	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f1_clk100m_reg	Read data 497	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f2_clk100m_reg	Read data 498	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f3_clk100m_reg	Read data 499	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f4_clk100m_reg	Read data 500	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f5_clk100m_reg	Read data 501	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f6_clk100m_reg	Read data 502	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f7_clk100m_reg	Read data 503	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f8_clk100m_reg	Read data 504	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1f9_clk100m_reg	Read data 505	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1fa_clk100m_reg	Read data 506	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1fb_clk100m_reg	Read data 507	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1fc_clk100m_reg	Read data 508	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1fd_clk100m_reg	Read data 509	16	Output	—	0000H	—	100MHz	clk100m
Register part	u_re2_top	re_rs_usr_rreg_1fe_clk100m_reg	Read data 510	16	Output	—	0000H	—	100MHz	clk100m

Connection destination		Terminal		Bit width	Input/ output	Polarity	Initial value	1shot	Sync clock	
Block name	Instance name	signal	Signal name						Feq	Clock
Register part	u_re2_top	re_rs_usr_rreg_1ff _clk100m_reg	Read data 511	16	Output	—	0000H	—	100MHz	clk100m

Appendix 6 A List of FPGA External Terminals

A list of FPGA external terminals is shown below.

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	System terminal												
—	K25	CLKIN_SYS	CLKIN_SYS	Clock (crystal oscillator) input	Input	—	3.3-V LVCMOS	3.3V	—	—	—	—	25MHz
—	T13	CLKIN_DDR	CLKIN_DDR	Clock (crystal oscillator) input (level shift buffer output)	Input	—	SSTL-135	1.35V	—	—	—	—	25MHz
—	G14	RSTL	RSTL	Reset input	Input	—	3.3-V LVCMOS	3.3V	Negative	PU	L	H	Asynchronous
—	Microcomputer interface terminal												
—	A13	PLL_LOCK	PLL_LOCK	PLL lock signal output	Output	—	3.3-V LVCMOS	3.3V	Positive	PU	L	L	Asynchronous
—	G11	CPU_BUSCLK	CPU_BUSCLK	Bus clock input	Input	—	3.3-V LVCMOS	3.3V	—	PU	L	L	50MHz
—	A11	CPU_CSL0	CPU_CSL[0]	Chip select signal input	Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	C12	CPU_CSL1	CPU_CSL[1]		Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	C13	CPU_CSL2	CPU_CSL[2]		Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz

A

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	A12	CPU_A01	CPU_A[1]	Address input	Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	D13	CPU_A02	CPU_A[2]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	N12	CPU_A03	CPU_A[3]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	M12	CPU_A04	CPU_A[4]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	L12	CPU_A05	CPU_A[5]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	J12	CPU_A06	CPU_A[6]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	H12	CPU_A07	CPU_A[7]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	G12	CPU_A08	CPU_A[8]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	F12	CPU_A09	CPU_A[9]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	D12	CPU_A10	CPU_A[10]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	M11	CPU_A11	CPU_A[11]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	L11	CPU_A12	CPU_A[12]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	K11	CPU_A13	CPU_A[13]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	M10	CPU_A14	CPU_A[14]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	K10	CPU_A15	CPU_A[15]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	J10	CPU_A16	CPU_A[16]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	H10	CPU_A17	CPU_A[17]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	G10	CPU_A18	CPU_A[18]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	E10	CPU_A19	CPU_A[19]	Address input	Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	D10	CPU_A20	CPU_A[20]		Input	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	J7	CPU_A21	CPU_A[21]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	H7	CPU_A22	CPU_A[22]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	G7	CPU_A23	CPU_A[23]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	F7	CPU_A24	CPU_A[24]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	D7	CPU_A25	CPU_A[25]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	C7	CPU_A26	CPU_A[26]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	B7	CPU_A27	CPU_A[27]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	L7	CPU_A28	CPU_A[28]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz
—	A8	CPU_A29	CPU_A[29]		Input	—	3.3-V LVCMOS	3.3V	—	PU	H	L	50MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	C10	CPU_D00	CPU_D[0]	Data bus	Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	B10	CPU_D01	CPU_D[1]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	N9	CPU_D02	CPU_D[2]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	M9	CPU_D03	CPU_D[3]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	L9	CPU_D04	CPU_D[4]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	K9	CPU_D05	CPU_D[5]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	H9	CPU_D06	CPU_D[6]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	E9	CPU_D07	CPU_D[7]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	C9	CPU_D08	CPU_D[8]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	B9	CPU_D09	CPU_D[9]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	A9	CPU_D10	CPU_D[10]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	L8	CPU_D11	CPU_D[11]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	K8	CPU_D12	CPU_D[12]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	J8	CPU_D13	CPU_D[13]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	H8	CPU_D14	CPU_D[14]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	D8	CPU_D15	CPU_D[15]		Input/output	—	3.3-V LVCMOS	3.3V	—	—	L	L	50MHz
—	D11	CPU_RDL	CPU_RDL	Read strobe input	Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	B11	CPU_WRSTBL	CPU_WRSTBL	Write strobe input	Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	E11	CPU_WRL0	CPU_WRL[0]	Valid Byte Lane Strobe Input (not used)	Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	J11	CPU_WRL1	CPU_WRL[1]		Input	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	B12	CPU_WAITL	CPU_WAITL	Wait output	Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	A5	CPU_INTPL0	CPU_INTPL[0]	External interrupt output/ general purpose I/O	Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	B6	CPU_INTPL1	CPU_INTPL[1]		Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	D6	CPU_INTPL2	CPU_INTPL[2]		Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	E6	CPU_INTPL3	CPU_INTPL[3]		Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	F6	CPU_INTPL4	CPU_INTPL[4]		Output	—	3.3-V LVCMOS	3.3V	Negative	PU	H	H	50MHz
—	G6	CPU_INTPL5	CPU_INTPL[5]		Input/ output	—	3.3-V LVCMOS	3.3V	—	PU	H	—	50MHz
—	K6	CPU_INTPL6	CPU_INTPL[6]		Input/ output	—	3.3-V LVCMOS	3.3V	—	PU	H	—	50MHz
—	A7	CPU_INTPL7	CPU_INTPL[7]		Input/ output	—	3.3-V LVCMOS	3.3V	—	PU	H	—	50MHz
—	DDR3L SDRAM terminal												
—	N10	DDR_CK_P	DDR_CK_P	DDR3L SDRAM differential clock output	Output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	L	L	400MHz
—	P10	DDR_CK_N	DDR_CK_N		Output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	H	L	400MHz

A

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	AF14	DDR_CKE	DDR_CKE	DDR3L SDRAM clock enable output	Output	—	SSTL-135	1.35V	Positive	—	L	L	200MHz
—	AE6	DDR_A00	DDR_A[0]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AF6	DDR_A01	DDR_A[1]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AF7	DDR_A02	DDR_A[2]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AF8	DDR_A03	DDR_A[3]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	U10	DDR_A04	DDR_A[4]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	U11	DDR_A05	DDR_A[5]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AE9	DDR_A06	DDR_A[6]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AF9	DDR_A07	DDR_A[7]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AB12	DDR_A08	DDR_A[8]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AB11	DDR_A09	DDR_A[9]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AC9	DDR_A10	DDR_A[10]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AC8	DDR_A11	DDR_A[11]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AB10	DDR_A12	DDR_A[12]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AC10	DDR_A13	DDR_A[13]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	W11	DDR_A14	DDR_A[14]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	V10	DDR_BA0	DDR_BA[0]	DDR3L SDRAM bank address output	Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AD8	DDR_BA1	DDR_BA[1]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AE8	DDR_BA2	DDR_BA[2]		Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	R11	DDR_CSL	DDR_CSL	DDR3L SDRAM chip select output	Output	—	SSTL-135	1.35V	Negative	—	L	L	200MHz
—	W10	DDR_CASL	DDR_CASL	DDR3L SDRAM CAS output	Output	—	SSTL-135	1.35V	Negative	—	L	L	200MHz
—	Y10	DDR_RASL	DDR_RASL	DDR3L SDRAM RAS output	Output	—	SSTL-135	1.35V	Negative	—	L	L	200MHz
—	T9	DDR_WEL	DDR_WEL	DDR3L SDRAM write enable output	Output	—	SSTL-135	1.35V	Negative	—	L	L	200MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	AF11	DDR_DM0	DDR_DM[0]	DDR3L SDRAM data mask output	Output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AE18	DDR_DM1	DDR_DM[1]		Output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AA14	DDR_DQ00	DDR_DQ[0]	DDR3L SDRAM data I/O	Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	Y14	DDR_DQ01	DDR_DQ[1]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AD11	DDR_DQ02	DDR_DQ[2]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AD12	DDR_DQ03	DDR_DQ[3]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	Y13	DDR_DQ04	DDR_DQ[4]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	W12	DDR_DQ05	DDR_DQ[5]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AD10	DDR_DQ06	DDR_DQ[6]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AF12	DDR_DQ07	DDR_DQ[7]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AC15	DDR_DQ08	DDR_DQ[8]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AB15	DDR_DQ09	DDR_DQ[9]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AC14	DDR_DQ10	DDR_DQ[10]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AF13	DDR_DQ11	DDR_DQ[11]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AB16	DDR_DQ12	DDR_DQ[12]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AA16	DDR_DQ13	DDR_DQ[13]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AE14	DDR_DQ14	DDR_DQ[14]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz
—	AF18	DDR_DQ15	DDR_DQ[15]		Input/output	—	SSTL-135	1.35V	—	—	L	L	400MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	V13	DDR_DQS_P[0]	DDR_DQS_P[0]	DDR3L SDRAM data strobe differential I/O	Input/output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	L	L	400MHz
—	W13	DDR_DQS_N[0]	DDR_DQS_N[0]		Input/output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	L	L	400MHz
—	U14	DDR_DQS_P[1]	DDR_DQS_P[1]		Input/output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	L	L	400MHz
—	V14	DDR_DQS_N[2]	DDR_DQS_N[1]		Input/output	—	DIFFERENTIAL 1.35-V SSTL	1.35V	—	—	L	L	400MHz
—	AD13	DDR_ODT	DDR_ODT	DDR3L SDRAM ODT output	Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AE19	DDR_RSTL	DDR_RSTL	DDR3L SDRAM reset output	Output	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	AE11	DDR_OCT_RZQ	DDR_OCT_RZQ	DDR3L SDRAM RZQ input	Input	—	SSTL-135	1.35V	—	—	L	L	200MHz
—	B0, B1, B2 common terminal												
—	H18	IOB_DCDL	IOB_DCDL	Power supply monitoring input	Input	Input	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	B0 connection terminal (compatible with DC I/O circuit board and Differential I/O circuit board)												
DC I/O circuit board	E13	IOB0_X0	IOB0_X[0]	DC input [0]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB0_DI422[0]	Differential (RS-422) input [0]		Input							4.17MHz
DC I/O circuit board	A14	IOB0_X1	IOB0_X[1]	DC input [1]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB0_DI422[1]	Differential (RS-422) input [1]		Input							4.17MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	B14	IOB0_X2	IOB0_X[2]	DC input [2]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB0_DI422[2]	Differential (RS-422) input [2]		Input							4.17MHz
DC I/O circuit board	C14	IOB0_X3	IOB0_X[3]	DC input [3]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB0_DI422[3]	Differential (RS-422) input [3]		Input							4.17MHz
DC I/O circuit board	C15	IOB0_X4	IOB0_X[4]	DC input [4]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB0_DI422[4]	Differential (RS-422) input [4]		Input							4.17MHz
DC I/O circuit board	D15	IOB0_X5	IOB0_X[5]	DC input [5]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB0_DI422[5]	Differential (RS-422) input [5]		Input							4.17MHz
DC I/O circuit board	E15	IOB0_X6	IOB0_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB0_DI422[6]	Differential (RS-422) input [6]		Input							4.17MHz
DC I/O circuit board	G15	IOB0_X7	IOB0_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB0_DI422[7]	Differential (RS-422) input [7]		Input							4.17MHz
DC I/O circuit board	B15	IOB0_XOEL0	IOB0_XOEL[0]	DC input output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOB0_DIO485_EN	Differential (RS-485) I/O direction		Output			Positive/ negative			L	Asynchronous
DC I/O circuit board	A16	IOB0_XOEL1	IOB0_XOEL[1]	DC input output enable [1]	Input/ output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOB0_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz
DC I/O circuit board	D16	IOB0_Y0	IOB0_Y[0]	DC output [0]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[0]	Differential (RS-422) output [0]		Output						H	4.17MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	E16	IOB0_Y1	IOB0_Y[1]	DC output [1]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[1]	Differential (RS-422) output [1]		Output						H	4.17MHz
DC I/O circuit board	F16	IOB0_Y2	IOB0_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[2]	Differential (RS-422) output [2]		Output						H	4.17MHz
DC I/O circuit board	G16	IOB0_Y3	IOB0_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[3]	Differential (RS-422) output [3]		Output						H	4.17MHz
DC I/O circuit board	B17	IOB0_Y4	IOB0_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[4]	Differential (RS-422) output [4]		Output						H	4.17MHz
DC I/O circuit board	C17	IOB0_Y5	IOB0_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[5]	Differential (RS-422) output [5]		Output						H	4.17MHz
DC I/O circuit board	D17	IOB0_Y6	IOB0_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[6]	Differential (RS-422) output [6]		Output						H	4.17MHz
DC I/O circuit board	G17	IOB0_Y7	IOB0_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB0_DO422[7]	Differential (RS-422) output [7]		Output						H	4.17MHz
DC I/O circuit board	A17	IOB0_YCK0	IOB0_YCK[0]	DC output output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		Output			—				—
DC I/O circuit board	A18	IOB0_YCK1	IOB0_YCK[1]	DC output output enable [1]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOB0_DIO485_O	Differential (RS-485) output		Output			—			H	10MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
—	H13	IOB0_UNIT0	IOB0_UNIT[0]	Module type	Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	H14	IOB0_UNIT1	IOB0_UNIT[1]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	H15	IOB0_UNIT2	IOB0_UNIT[2]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	J16	IOB0_UNIT3	IOB0_UNIT[3]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	H17	IOB0_RSTL	IOB0_RSTL	Output enable (B0)	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	B1 connection terminal (compatible with DC I/O circuit board and Differential I/O circuit board)												
DC I/O circuit board	C18	IOB1_X0	IOB1_X[0]	DC input [0]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB1_DI422[0]	Differential (RS-422) input [0]		Input							4.17MHz
DC I/O circuit board	D18	IOB1_X1	IOB1_X[1]	DC input [1]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB1_DI422[1]	Differential (RS-422) input [1]		Input							4.17MHz
DC I/O circuit board	E18	IOB1_X2	IOB1_X[2]	DC input [2]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB1_DI422[2]	Differential (RS-422) input [2]		Input							4.17MHz
DC I/O circuit board	F18	IOB1_X3	IOB1_X[3]	DC input [3]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB1_DI422[3]	Differential (RS-422) input [3]		Input							4.17MHz
DC I/O circuit board	A19	IOB1_X4	IOB1_X[4]	DC input [4]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB1_DI422[4]	Differential (RS-422) input [4]		Input							4.17MHz
DC I/O circuit board	B19	IOB1_X5	IOB1_X[5]	DC input [5]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB1_DI422[5]	Differential (RS-422) input [5]		Input							4.17MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	C19	IOB1_X6	IOB1_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB1_DI422[6]	Differential (RS-422) input [6]		Input							4.17MHz
DC I/O circuit board	E19	IOB1_X7	IOB1_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB1_DI422[7]	Differential (RS-422) input [7]		Input							4.17MHz
DC I/O circuit board	B20	IOB1_XOEL0	IOB1_XOEL[0]	DC input output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOB1_DIO485_EN	Differential (RS-485) I/O direction		Output			Positive/negative			L	Asynchronous
DC I/O circuit board	A21	IOB1_XOEL1	IOB1_XOEL[1]	DC input output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOB1_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz
DC I/O circuit board	C20	IOB1_Y0	IOB1_Y[0]	DC output [0]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[0]	Differential (RS-422) output [0]		Output						H	4.17MHz
DC I/O circuit board	D20	IOB1_Y1	IOB1_Y[1]	DC output [1]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[1]	Differential (RS-422) output [1]		Output						H	4.17MHz
DC I/O circuit board	E20	IOB1_Y2	IOB1_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[2]	Differential (RS-422) output [2]		Output						H	4.17MHz
DC I/O circuit board	B21	IOB1_Y3	IOB1_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[3]	Differential (RS-422) output [3]		Output						H	4.17MHz
DC I/O circuit board	D21	IOB1_Y4	IOB1_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[4]	Differential (RS-422) output [4]		Output						H	4.17MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	B22	IOB1_Y5	IOB1_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[5]	Differential (RS-422) output [5]		Output						H	4.17MHz
DC I/O circuit board	C22	IOB1_Y6	IOB1_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[6]	Differential (RS-422) output [6]		Output						H	4.17MHz
DC I/O circuit board	C23	IOB1_Y7	IOB1_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB1_DO422[7]	Differential (RS-422) output [7]		Output						H	4.17MHz
DC I/O circuit board	A22	IOB1_YCK0	IOB1_YCK[0]	DC output output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		Output			—				—
DC I/O circuit board	A23	IOB1_YCK1	IOB1_YCK[1]	DC output output enable [1]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOB1_DIO485_O	Differential (RS-485) output		Output			—			H	10MHz
—	H19	IOB1_UNIT0	IOB1_UNIT[0]	Module type	Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	G20	IOB1_UNIT1	IOB1_UNIT[1]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	H20	IOB1_UNIT2	IOB1_UNIT[2]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	J20	IOB1_UNIT3	IOB1_UNIT[3]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	A24	IOB1_RSTL	IOB1_RSTL	Output enable (B1)	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	B2 connection terminal (compatible with DC I/O circuit board and Differential I/O circuit board)												
DC I/O circuit board	B26	IOB2_X0	IOB2_X[0]	DC input [0]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB2_DI422[0]	Differential (RS-422) input [0]		Input							4.17MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	B25	IOB2_X1	IOB2_X[1]	DC input [1]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB2_DI422[1]	Differential (RS-422) input [1]		Input							4.17MHz
DC I/O circuit board	B24	IOB2_X2	IOB2_X[2]	DC input [2]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB2_DI422[2]	Differential (RS-422) input [2]		Input							4.17MHz
DC I/O circuit board	C25	IOB2_X3	IOB2_X[3]	DC input [3]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB2_DI422[3]	Differential (RS-422) input [3]		Input							4.17MHz
DC I/O circuit board	D25	IOB2_X4	IOB2_X[4]	DC input [4]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOB2_DI422[4]	Differential (RS-422) input [4]		Input							4.17MHz
DC I/O circuit board	D22	IOB2_X5	IOB2_X[5]	DC input [5]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB2_DI422[5]	Differential (RS-422) input [5]		Input							4.17MHz
DC I/O circuit board	E25	IOB2_X6	IOB2_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB2_DI422[6]	Differential (RS-422) input [6]		Input							4.17MHz
DC I/O circuit board	E24	IOB2_X7	IOB2_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOB2_DI422[7]	Differential (RS-422) input [7]		Input							4.17MHz
DC I/O circuit board	D26	IOB2_XOEL0	IOB2_XOEL[0]	DC input output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOB2_DIO485_EN	Differential (RS-485) I/O direction		Output			Positive/negative			L	Asynchronous
DC I/O circuit board	E26	IOB2_XOEL1	IOB2_XOEL[1]	DC input output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOB2_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	E23	IOB2_Y0	IOB2_Y[0]	DC output [0]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[0]	Differential (RS-422) output [0]		Output						H	4.17MHz
DC I/O circuit board	E21	IOB2_Y1	IOB2_Y[1]	DC output [1]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[1]	Differential (RS-422) output [1]		Output						H	4.17MHz
DC I/O circuit board	F24	IOB2_Y2	IOB2_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[2]	Differential (RS-422) output [2]		Output						H	4.17MHz
DC I/O circuit board	F23	IOB2_Y3	IOB2_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[3]	Differential (RS-422) output [3]		Output						H	4.17MHz
DC I/O circuit board	F22	IOB2_Y4	IOB2_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[4]	Differential (RS-422) output [4]		Output						H	4.17MHz
DC I/O circuit board	F21	IOB2_Y5	IOB2_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[5]	Differential (RS-422) output [5]		Output						H	4.17MHz
DC I/O circuit board	G25	IOB2_Y6	IOB2_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[6]	Differential (RS-422) output [6]		Output						H	4.17MHz
DC I/O circuit board	H25	IOB2_Y7	IOB2_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOB2_DO422[7]	Differential (RS-422) output [7]		Output						H	4.17MHz
DC I/O circuit board	F26	IOB2_YCK0	IOB2_YCK[0]	DC output output enable [0]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		Output			—				—

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	G26	IOB2_YCK1	IOB2_YCK[1]	DC output output enable [1]	Output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOB2_DIO485_O	Differential (RS-485) output		Output			—			H	10MHz
—	G22	IOB2_UNIT0	IOB2_UNIT[0]	Module type	Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	H22	IOB2_UNIT1	IOB2_UNIT[1]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	J21	IOB2_UNIT2	IOB2_UNIT[2]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	K21	IOB2_UNIT3	IOB2_UNIT[3]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	W20	IOB2_RSTL	IOB2_RSTL	Output enable (B2)	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	E0, E1, E2 common terminal												
—	U20	IOE_RSTL	IOE_RSTL	Output enable (E)	Output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	V20	IOE_DCDL	IOE_DCDL	Power supply monitoring input	Input	Input	3.3-V LVCMOS	3.3V	Negative	PU	L	L	Asynchronous
—	T19	IOE_UNIT0	IOE0_UNIT[0]	Module type	Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	U19	IOE_UNIT1	IOE0_UNIT[1]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	N20	IOE_UNIT2	IOE0_UNIT[2]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	P20	IOE_UNIT3	IOE0_UNIT[3]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	R20	IOE_UNIT4	IOE0_UNIT[4]		Input	Input	3.3-V LVCMOS	3.3V	—	PU	—	—	Asynchronous
—	E0 connection terminal (compatible with DC I/O circuit board, Differential I/O circuit board, and Analog I/O circuit board)												
DC I/O circuit board	G24	IOE0_X0	IOE0_X[0]	DC input [0]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE0_DI422[0]	Differential (RS-422) input [0]		Input			—				4.17MHz
Analog I/O circuit board			IOE0_CONVST	A/D conversion start output (common to 3 chips)		Output			Positive				12.5MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	H24	IOE0_X1	IOE0_X[1]	DC input [1]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE0_DI422[1]	Differential (RS-422) input [1]		Input			—				4.17MHz
Analog I/O circuit board			IOE0_AD_CSL[0]	ADC chip select [0]		Output			Negative			H	12.5MHz
DC I/O circuit board	H23	IOE0_X2	IOE0_X[2]	DC input [2]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE0_DI422[2]	Differential (RS-422) input [2]		Input							4.17MHz
Analog I/O circuit board			IOE0_AD_SCLK	ADC serial clock output (common to 3 chips)		Output						H	25MHz
DC I/O circuit board	J25	IOE0_X3	IOE0_X[3]	DC input [3]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE0_DI422[3]	Differential (RS-422) input [3]		Input							4.17MHz
Analog I/O circuit board			IOE0_AD_CSL[1]	ADC chip select [1]		Output						H	12.5MHz
DC I/O circuit board	J23	IOE0_X4	IOE0_X[4]	DC input [4]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE0_DI422[4]	Differential (RS-422) input [4]		Input							4.17MHz
Analog I/O circuit board			IOE0_AD_SDI	ADC serial data output (common to 3 chips)		Output						H	12.5MHz
DC I/O circuit board	K24	IOE0_X5	IOE0_X[5]	DC input [5]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE0_DI422[5]	Differential (RS-422) input [5]		Input							4.17MHz
Analog I/O circuit board			IOE0_AD_CSL[2]	ADC chip select [2]		Output			Negative			H	12.5MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	K23	IOE0_X6	IOE0_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	H	20MHz
Differential I/O circuit board			IOE0_DI422[6]	Differential (RS-422) input [6]									4.17MHz
Analog I/O circuit board			IOE0_AD_SCLK_B	Serial read back clock								L	25MHz
DC I/O circuit board	L24	IOE0_X7	IOE0_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE0_DI422[7]	Differential (RS-422) input [7]									4.17MHz
Analog I/O circuit board			IOE0_AD_BUSY	ADC busy input (common to 3 chips)					Positive		L		12.5MHz
DC I/O circuit board	J26	IOE0_XOEL0	IOE0_XOEL[0]	DC input output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOE0_DIO485_EN	Differential (RS-485) I/O direction					Positive/negative			L	Asynchronous
Analog I/O circuit board			IOE0_AD0_DOUTA	ADC0 serial data input A		Input			—				12.5MHz
DC I/O circuit board	K26	IOE0_XOEL1	IOE0_XOEL[1]	DC input output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOE0_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz
Analog I/O circuit board			IOE0_AD0_DOUTB	ADC0 serial data input B									12.5MHz
DC I/O circuit board	L23	IOE0_Y0	IOE0_Y[0]	DC output [0]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[0]	Differential (RS-422) output [0]								H	4.17MHz
Analog I/O circuit board			IOE0_AD2_DOUTA	ADC2 serial data input A		Input						L	12.5MHz
DC I/O circuit board	L22	IOE0_Y1	IOE0_Y[1]	DC output [1]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[1]	Differential (RS-422) output [1]								H	4.17MHz
Analog I/O circuit board			IOE0_AD2_DOUTB	ADC2 serial data input B		Input						L	12.5MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	M25	IOE0_Y2	IOE0_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[2]	Differential (RS-422) output [2]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_SCLK	DAC serial clock output (common to 2 chips)								L	25MHz
DC I/O circuit board	M24	IOE0_Y3	IOE0_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[3]	Differential (RS-422) output [3]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_SDI	DAC serial data output (common to 2 chips)								L	12.5MHz
DC I/O circuit board	M22	IOE0_Y4	IOE0_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[4]	Differential (RS-422) output [4]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_SYNCL	DAC sync output (common to 2 chips)					Negative				12.5MHz
DC I/O circuit board	M21	IOE0_Y5	IOE0_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[5]	Differential (RS-422) output [5]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_SDO	DAC serial data input (reserved)									—
DC I/O circuit board	N25	IOE0_Y6	IOE0_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[6]	Differential (RS-422) output [6]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_LDACL[0]	DACLDAC signal output					Positive			L	12.5MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	N24	IOE0_Y7	IOE0_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE0_DO422[7]	Differential (RS-422) output [7]								H	4.17MHz
Analog I/O circuit board			IOE0_DA_LDACL[1]	DACLDAC signal output					Positive			L	12.5MHz
DC I/O circuit board	M26	IOE0_YCK0	IOE0_YCK[0]	DC output output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		—			—			H	—
Analog I/O circuit board			IOE0_AD1_DOUTA	ADC1 serial data input A		Input						L	12.5MHz
DC I/O circuit board	P26	IOE0_YCK1	IOE0_YCK[1]	DC output output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOE0_DIO485_O	Differential (RS-485) output					—			H	10MHz
Analog I/O circuit board			IOE0_AD1_DOUTB	ADC1 serial data input B		Input						L	12.5MHz
—	E1 connection terminal (compatible with DC I/O circuit board, Differential I/O circuit board, and Analog I/O circuit board)												
DC I/O circuit board	N23	IOE1_X0	IOE1_X[0]	DC input [0]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE1_DI422[0]	Differential (RS-422) input [0]									4.17MHz
Analog I/O circuit board			IOE1_CONVST	A/D conversion start output (common to 3 chips)		Output			Positive				12.5MHz
DC I/O circuit board	P23	IOE1_X1	IOE1_X[1]	DC input [1]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE1_DI422[1]	Differential (RS-422) input [1]									4.17MHz
Analog I/O circuit board			IOE1_AD_CSL[0]	ADC chip select [0]		Output			Negative			H	12.5MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	P22	IOE1_X2	IOE1_X[2]	DC input [2]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE1_DI422[2]	Differential (RS-422) input [2]									4.17MHz
Analog I/O circuit board			IOE1_AD_SCLK	ADC serial clock output (common to 3 chips)		Output						H	25MHz
DC I/O circuit board	P21	IOE1_X3	IOE1_X[3]	DC input [3]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE1_DI422[3]	Differential (RS-422) input [3]									4.17MHz
Analog I/O circuit board			IOE1_AD_CSL[1]	ADC chip select [1]		Output						H	12.5MHz
DC I/O circuit board	R25	IOE1_X4	IOE1_X[4]	DC input [4]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE1_DI422[4]	Differential (RS-422) input [4]									4.17MHz
Analog I/O circuit board			IOE1_AD_SDI	ADC serial data output (common to 3 chips)		Output						H	12.5MHz
DC I/O circuit board	R24	IOE1_X5	IOE1_X[5]	DC input [5]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE1_DI422[5]	Differential (RS-422) input [5]									4.17MHz
Analog I/O circuit board			IOE1_AD_CSL[2]	ADC chip select [2]		Output			Negative			H	12.5MHz
DC I/O circuit board	R23	IOE1_X6	IOE1_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	H	20MHz
Differential I/O circuit board			IOE1_DI422[6]	Differential (RS-422) input [6]									4.17MHz
Analog I/O circuit board			IOE1_AD_SCLK_B	Serial read back clock								L	25MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	T24	IOE1_X7	IOE1_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE1_DI422[7]	Differential (RS-422) input [7]									4.17MHz
Analog I/O circuit board			IOE1_AD_BUSY	ADC busy input (common to 3 chips)					Positive		L	H	12.5MHz
DC I/O circuit board	R26	IOE1_XOEL0	IOE1_XOEL[0]	DC input output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOE1_DIO485_EN	Differential (RS-485) I/O direction					Positive/negative			L	Asynchronous
Analog I/O circuit board			IOE1_AD0_DOUTA	ADC0 serial data input A		Input			—				12.5MHz
DC I/O circuit board	T26	IOE1_XOEL1	IOE1_XOEL[1]	DC input output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOE1_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz
Analog I/O circuit board			IOE1_AD0_DOUTB	ADC0 serial data input B									12.5MHz
DC I/O circuit board	T23	IOE1_Y0	IOE1_Y[0]	DC output [0]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[0]	Differential (RS-422) output [0]								H	4.17MHz
Analog I/O circuit board			IOE1_AD2_DOUTA	ADC2 serial data input A		Input						L	12.5MHz
DC I/O circuit board	T22	IOE1_Y1	IOE1_Y[1]	DC output [1]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[1]	Differential (RS-422) output [1]								H	4.17MHz
Analog I/O circuit board			IOE1_AD2_DOUTB	ADC2 serial data input B		Input						L	12.5MHz
DC I/O circuit board	T21	IOE1_Y2	IOE1_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[2]	Differential (RS-422) output [2]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_SCLK	DAC serial clock output (common to 2 chips)								L	25MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	U25	IOE1_Y3	IOE1_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[3]	Differential (RS-422) output [3]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_SDI	DAC serial data output (common to 2 chips)								L	12.5MHz
DC I/O circuit board	U24	IOE1_Y4	IOE1_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[4]	Differential (RS-422) output [4]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_SYNCL	DAC sync output (common to 2 chips)					Negative				12.5MHz
DC I/O circuit board	U22	IOE1_Y5	IOE1_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[5]	Differential (RS-422) output [5]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_SDO	DAC serial data input (reserved)									—
DC I/O circuit board	V25	IOE1_Y6	IOE1_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[6]	Differential (RS-422) output [6]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_LDACL[0]	DACLDAC signal output					Positive			L	12.5MHz
DC I/O circuit board	V24	IOE1_Y7	IOE1_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE1_DO422[7]	Differential (RS-422) output [7]								H	4.17MHz
Analog I/O circuit board			IOE1_DA_LDACL[1]	DACLDAC signal output					Positive			L	12.5MHz
DC I/O circuit board	U26	IOE1_YCK0	IOE1_YCK[0]	DC output output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		—			—			H	
Analog I/O circuit board			IOE1_AD1_DOUTA	ADC1 serial data input A		Input						L	12.5MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	W26	IOE1_YCK1	IOE1_YCK[1]	DC output output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOE1_DIO485_O	Differential (RS-485) output					—			H	10MHz
Analog I/O circuit board			IOE1_AD1_DOUTB	ADC1 serial data input B		Input						L	12.5MHz
—	E2 connection terminal (compatible with DC I/O circuit board, Differential I/O circuit board, and Analog I/O circuit board)												
DC I/O circuit board	W25	IOE2_X0	IOE2_X[0]	DC input [0]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE2_DI422[0]	Differential (RS-422) input [0]									4.17MHz
Analog I/O circuit board			IOE2_CONVST	A/D conversion start output (common to 3 chips)		Output			Positive				12.5MHz
DC I/O circuit board	V23	IOE2_X1	IOE2_X[1]	DC input [1]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE2_DI422[1]	Differential (RS-422) input [1]									4.17MHz
Analog I/O circuit board			IOE2_AD_CSL[0]	ADC chip select [0]		Output			Negative			H	12.5MHz
DC I/O circuit board	V22	IOE2_X2	IOE2_X[2]	DC input [2]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE2_DI422[2]	Differential (RS-422) input [2]									4.17MHz
Analog I/O circuit board			IOE2_AD_SCLK	ADC serial clock output (common to 3 chips)		Output						H	25MHz
DC I/O circuit board	W21	IOE2_X3	IOE2_X[3]	DC input [3]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE2_DI422[3]	Differential (RS-422) input [3]									4.17MHz
Analog I/O circuit board			IOE2_AD_CSL[1]	ADC chip select [1]		Output						H	12.5MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	Y25	IOE2_X4	IOE2_X[4]	DC input [4]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	L	L	20MHz
Differential I/O circuit board			IOE2_DI422[4]	Differential (RS-422) input [4]									4.17MHz
Analog I/O circuit board			IOE2_AD_SDI	ADC serial data output (common to 3 chips)		Output						H	12.5MHz
DC I/O circuit board	Y24	IOE2_X5	IOE2_X[5]	DC input [5]	Input/output	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE2_DI422[5]	Differential (RS-422) input [5]									4.17MHz
Analog I/O circuit board			IOE2_AD_CSL[2]	ADC chip select [2]		Output			Negative			H	12.5MHz
DC I/O circuit board	Y23	IOE2_X6	IOE2_X[6]	DC input [6]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	H	20MHz
Differential I/O circuit board			IOE2_DI422[6]	Differential (RS-422) input [6]									4.17MHz
Analog I/O circuit board			IOE2_AD_SCLK_B	Serial read back clock								L	25MHz
DC I/O circuit board	AA24	IOE2_X7	IOE2_X[7]	DC input [7]	Input	Input	3.3-V LVCMOS	3.3V	—	PU	H	L	20MHz
Differential I/O circuit board			IOE2_DI422[7]	Differential (RS-422) input [7]									4.17MHz
Analog I/O circuit board			IOE2_AD_BUSY	ADC busy input (common to 3 chips)					Positive		L		12.5MHz
DC I/O circuit board	Y26	IOE2_XOEL0	IOE2_XOEL[0]	DC input output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	L	H	20MHz
Differential I/O circuit board			IOE2_DIO485_EN	Differential (RS-485) I/O direction					Positive/negative			L	Asynchronous
Analog I/O circuit board			IOE2_AD0_DOUTA	ADC0 serial data input A		Input			—				12.5MHz
DC I/O circuit board	AA26	IOE2_XOEL1	IOE2_XOEL[1]	DC input output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Negative	PU	H	H	20MHz
Differential I/O circuit board			IOE2_DIO485_I	Differential (RS-485) input		Input			—			L	10MHz
Analog I/O circuit board			IOE2_AD0_DOUTB	ADC0 serial data input B									12.5MHz

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Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	AA23	IOE2_Y0	IOE2_Y[0]	DC output [0]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[0]	Differential (RS-422) output [0]								H	4.17MHz
Analog I/O circuit board			IOE2_AD2_DOUTA	ADC2 serial data input A		Input						L	12.5MHz
DC I/O circuit board	AA22	IOE2_Y1	IOE2_Y[1]	DC output [1]	Input/output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[1]	Differential (RS-422) output [1]								H	4.17MHz
Analog I/O circuit board			IOE2_AD2_DOUTB	ADC2 serial data input B		Input						L	12.5MHz
DC I/O circuit board	AB25	IOE2_Y2	IOE2_Y[2]	DC output [2]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[2]	Differential (RS-422) output [2]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_SCLK	DAC serial clock output (common to 2 chips)								L	25MHz
DC I/O circuit board	AB24	IOE2_Y3	IOE2_Y[3]	DC output [3]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[3]	Differential (RS-422) output [3]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_SDI	DAC serial data output (common to 2 chips)								L	12.5MHz
DC I/O circuit board	AC25	IOE2_Y4	IOE2_Y[4]	DC output [4]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[4]	Differential (RS-422) output [4]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_SYNCL	DAC sync output (common to 2 chips)					Negative				12.5MHz

Connection circuit board	Terminal number	External terminal name	Each circuit board function terminal name	Functions	I/O direction	I/O direction for each circuit board	I/O type	I/O voltage	Logic	PU/PD in FPGA	Initial state		Operating frequency
											Resetting	After reset release	
DC I/O circuit board	AC24	IOE2_Y5	IOE2_Y[5]	DC output [5]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[5]	Differential (RS-422) output [5]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_SDO	DAC serial data input (reserved)									—
DC I/O circuit board	AC23	IOE2_Y6	IOE2_Y[6]	DC output [6]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[6]	Differential (RS-422) output [6]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_LDACL[0]	DACLDAC signal output					Positive			L	12.5MHz
DC I/O circuit board	AC22	IOE2_Y7	IOE2_Y[7]	DC output [7]	Output	Output	3.3-V LVCMOS	3.3V	—	PU	H	L	25MHz
Differential I/O circuit board			IOE2_DO422[7]	Differential (RS-422) output [7]								H	4.17MHz
Analog I/O circuit board			IOE2_DA_LDACL[1]	DACLDAC signal output					Positive			L	12.5MHz
DC I/O circuit board	AB26	IOE2_YCK0	IOE2_YCK[0]	DC output output enable [0]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			—	—		—			—			H	—
Analog I/O circuit board			IOE2_AD1_DOUTA	ADC1 serial data input A		Input						L	12.5MHz
DC I/O circuit board	AD25	IOE2_YCK1	IOE2_YCK[1]	DC output output enable [1]	Input/output	Output	3.3-V LVCMOS	3.3V	Positive	PU	L	L	—
Differential I/O circuit board			IOE2_DIO485_O	Differential (RS-485) output					—			H	10MHz
Analog I/O circuit board			IOE2_AD1_DOUTB	ADC1 serial data input B		Input						L	12.5MHz

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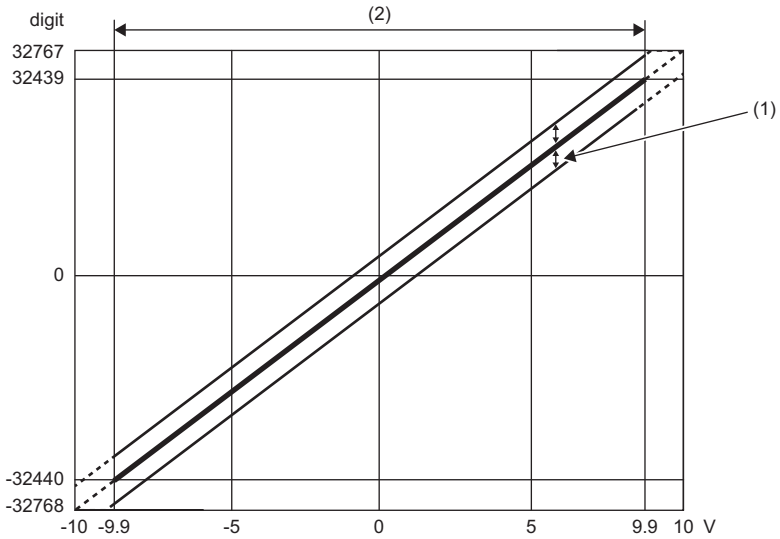
Appendix 7 I/O Conversion Characteristics and Accuracy

A/D conversion

Voltage input

The graph below shows the conversion characteristics during voltage input and the accuracy against the maximum A/D conversion value. Excluded when the wiring is influenced by noise.



digit: A/D conversion value V: Analog input voltage (V)
(1) Fluctuation range
(2) Practical analog input range

The maximum resolution and accuracy during the voltage input are shown below.

Input range setting	A/D conversion value*1	Maximum resolution	Accuracy	
			Ambient temperature 25±5℃	Ambient temperature 0 to 55℃
-9.9 to 9.9V	-32440 to 32439	305.2μV	Within ±0.2% (±65 digits)	

*1 The maximum and minimum A/D conversion values are as follows.

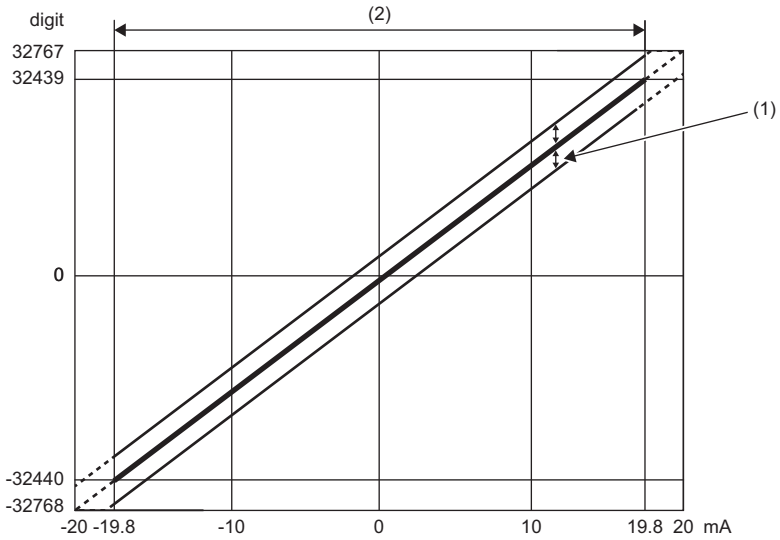
Input range setting	A/D conversion value	
	Minimum	Maximum
-9.9 to 9.9V	-32768	32767

Restriction

- Use within each practical analog input range and practical A/D conversion value range. If the range is exceeded, the resolution and accuracy may not fall within the range of the performance specifications. (Do not use the value in the dotted line region in the graph of voltage input characteristics.)
- Do not set the voltage over ±15V. Doing so can cause breakdown of the elements.

During current input

The graph below shows the conversion characteristics during the current input and the accuracy against the maximum A/D conversion value. Excluded when the wiring is influenced by noise.



digit: A/D conversion value mA: Analog input current (mA)
(1) Fluctuation range
(2) Practical analog input range

The maximum resolution and accuracy during the current input are shown below.

Input range setting	A/D conversion value*1	Maximum resolution	Accuracy	
			Ambient temperature 25±5℃	Ambient temperature 0 to 55℃
-19.8 to 19.8mA	-32440 to 32439	610.4nA	±0.3% (±98 digits)	

*1 The maximum and minimum A/D conversion values are as follows.

Input range setting	A/D conversion value	
	Minimum	Maximum
-19.8 to 19.8mA	-32768	32767

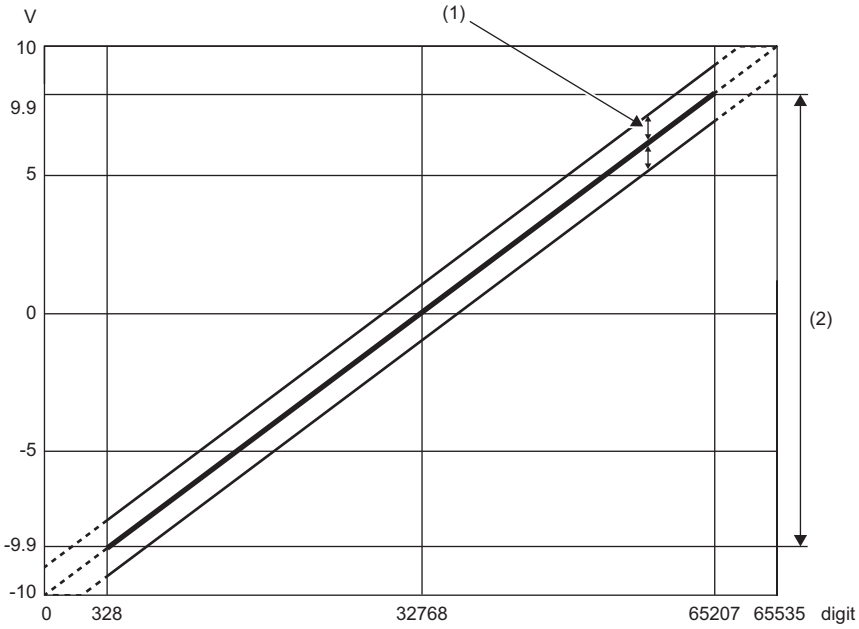
Restriction

- Use within each practical analog input range and practical A/D conversion value range. If the range is exceeded, the resolution and accuracy may not fall within the range of the performance specifications. (Do not use the value in the dotted line region in the graph of current input characteristics.)
- Do not set the current over ±30mA. Doing so can cause breakdown of the elements.

D/A conversion

During voltage output

The graph below shows the conversion characteristics during the voltage output and the accuracy against the maximum analog output value. Excluded when the wiring is influenced by noise.



digit: D/A conversion value V: Analog output voltage (V)
(1) Fluctuation range
(2) Practical analog output range

The maximum resolution and accuracy during the voltage output are shown below.

Output range setting	D/A conversion value*1	Maximum resolution	Accuracy	
			Ambient temperature 25±5℃	Ambient temperature 0 to 55℃
-9.9 to 9.9V	328 to 65207	305.2μV	Within ±0.2%	

*1 The maximum and minimum D/A conversion values are as follows.

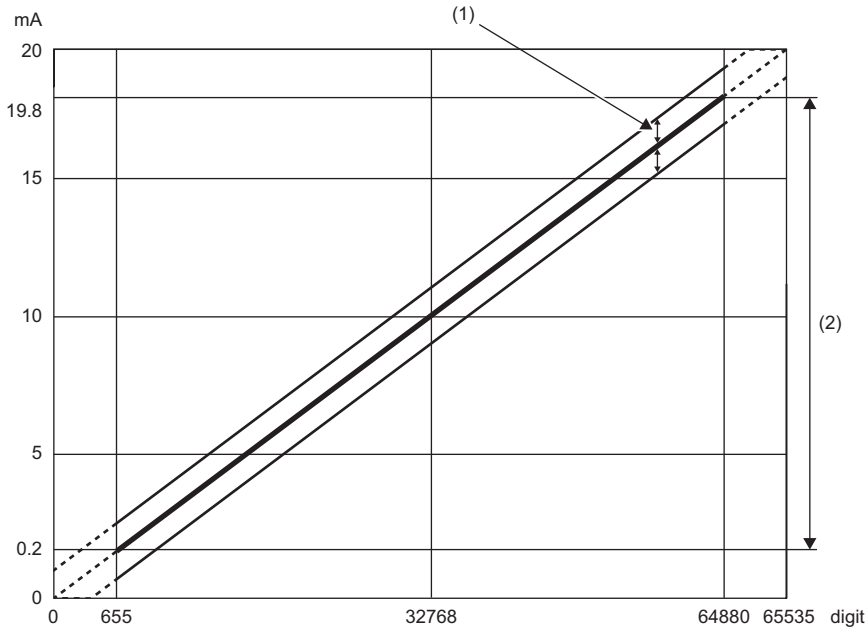
Output range setting	D/A conversion value	
	Minimum	Maximum
-9.9 to 9.9V	0	65535

Restriction

Use within each practical analog output range and practical D/A conversion value range. If the range is exceeded, the resolution and accuracy may not fall within the range of the performance specifications. (Do not use the value in the dotted line region in the graph of voltage output characteristics.)

During current output

The graph below shows the conversion characteristics during the current output and the accuracy against the maximum analog output value. Excluded when the wiring is influenced by noise.



digit: D/A conversion value
mA: Analog output current (mA)
(1) Fluctuation range
(2) Practical analog output range

The maximum resolution and accuracy during the current output are shown below.

Output range setting	D/A conversion value*1	Maximum resolution	Accuracy	
			Ambient temperature 25±5℃	Ambient temperature 0 to 55℃
0.2 to 19.8mA	655 to 64880	305.2μV	Within ±0.3%	

*1 The maximum and minimum D/A conversion values are as follows.

Output range setting	D/A conversion value	
	Minimum	Maximum
0.2 to 19.8mA	0	65535

Restriction

Use within each practical analog output range and practical D/A conversion value range. If the range is exceeded, the resolution and accuracy may not fall within the range of the performance specifications. (Do not use the values in the dotted line region in the graph of current output characteristics.)

Appendix 8 CC-Link IE TSN Processing Time

The processing time of CC-Link IE TSN is the time until the device operation of the master station CPU module is reflected in the FPGA register, or the time until the state of FPGA register is reflected in the device of the master station CPU module. The CC-Link IE TSN processing time is determined by the following processing time.

• CC-Link IE TSN processing time = cyclic transmission delay time + remote station processing time

Transmission delay time of cyclic transmission (📖 User's manual of the master station used)

Remote station processing time: 1ms

Appendix 9 Logging Data FTP Transfer Time

The time to transfer logging data to the FTP server depends on the logging parameters. Examples of parameters and transfer times are shown below.

Logging setting parameters			Transfer time
Logging data format	**Logging data size (number of records)**	**Number of targets for CSV conversion**	
Binary format (.bin)	256kB (4096 records)	—	0.7 seconds
CSV format (.csv)	256kB (4096 records)	4 words • Signed 16 bits×2 • Signed 32 bits×1	1 seconds

Point

- If the logging data size is large, the transfer time may become longer.
- It may take some time depending on the module status and Ethernet network load (line congestion).
- If an FTP server is connected to the line on the Ethernet port (P2) side of the FPGA module, the initial transfer time will increase by about 2 seconds after starting the FPGA module.

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Appendix 10 EMC and Low Voltage Directives

In each country, laws and regulations concerning electromagnetic compatibility (EMC) and electrical safety are enacted.
For the products sold in the European countries, compliance with the EU's EMC Directive has been a legal obligation as EMC regulation since 1996, as well as the EU's Low Voltage Directive as electrical safety regulation since 1997.
Manufacturers who recognize their products are compliant with the EMC and Low Voltage Directives are required to attach a "CE marking" on their products in European countries.
In some other countries and regions, manufacturers are required to make their products compliant with applicable laws or regulations and attach a certification mark on the products as well (such as UK Conformity Assessed (UKCA) marking in the UK, and Korea Certification (KC) marking in South Korea).
Each country works to make their regulatory requirements consistent across countries based on international standards. When the requirements are consistent, measures to comply with the EMC and electrical safety regulations become common across countries.
The UK and South Korea have enacted EMC regulations whose requirements are consistent with those of the EMC Directive. The UK has also enacted electrical safety regulations whose requirements are consistent with those of the Low Voltage Directive. In this section, the requirements of the EMC and Low Voltage Directives are described as examples of those of the EMC and electrical safety regulations.

Measures to comply with the EMC Directive

The EMC Directive sets requirements for emission (conducted and radiated electromagnetic interference emitted by a product) and immunity (the ability of a product not to be influenced by externally generated electromagnetic interference).
This section summarizes the precautions on compliance with the EMC Directive of the machinery constructed with the module.
These precautions are based on the requirements of the EMC Directive and the harmonized standards. However, they do not guarantee that the entire machinery constructed according to the descriptions complies with the EMC Directive.
The manufacturer of the machinery must determine the testing method for compliance and declare conformity to the EMC Directive.

EMC Directive related standards

■Emission requirements

Standard: EN61131-2:2007

Test item	Test details	Standard value
CISPR16-2-3 Radiated emission*2	Radio waves from the product are measured.	• 30 to 230MHz, QP: 40dBμV/m (measured at 10m distance)*1 • 230 to 1000MHz, QP: 47dBμV/m (measured at 10m distance)
CISPR16-2-1, CISPR16-1-2 Conducted emission*2	Noise from the product to the power line is measured.	• 0.15 to 0.5MHz, QP: 79dB, Mean: 66dB*1 • 0.5 to 30MHz, QP: 73dB, Mean: 60dB

*1 QP (Quasi-Peak): quasi-peak value, Mean: mean value
*2 The module is an open type device (a device designed to be housed in other equipment) and must be installed inside a conductive control panel. The tests were conducted with the module installed in a control panel.

■Immunity requirements

Standard: EN61131-2:2007

Test item	Test details	Standard value
EN61000-4-2 Electrostatic discharge immunity*1	Static electricity is applied to the cabinet of the equipment.	• 8kV: Air discharge • 4kV: Contact discharge
EN61000-4-3 Radiated, radio-frequency, electromagnetic field immunity*1	Electric fields are radiated to the product.	80% AM modulation @1kHz • 80 to 1000MHz: 10V/m • 1.4 to 2.0GHz: 3V/m • 2.0 to 2.7GHz: 1V/m
EN61000-4-4 Fast transient burst immunity*1	Burst noise is applied to the power line and signal line.	• AC/DC main power supply, I/O power supply, AC I/O (unshielded): 2kV • DC I/O, analog, communication cable: 1kV

Test item	Test details	Standard value
EN61000-4-5 Surge immunity*1	A lightning surge is applied to the power line and signal line.	• AC power line, AC I/O power supply, AC I/O (unshielded): 2kV CM, 1kV DM • DC power line, DC I/O power supply: 0.5kV CM, DM • DC I/O, AC I/O (shielded), analog*2, and communication lines: 1kV CM
EN61000-4-6 Conducted RF immunity*1	High frequency noise is applied to the power line and signal line.	0.15 to 80MHz, 80% AM modulation @1kHz, 10Vrms
EN61000-4-8 Power-frequency magnetic field immunity*1	The product is installed in an inductive magnetic field.	50Hz/60Hz, 30A/m
EN61000-4-11 Voltage dips and interruptions immunity*1	A momentary power failure is caused to the power supply voltage.	• Apply at 0%, 0.5 cycles and zero-cross point • 0%, 250/300 cycles (50/60Hz) • 40%, 10/12 cycles (50/60Hz) • 70%, 25/30 cycles (50/60Hz)

*1 The module is an open type device (a device designed to be housed in other equipment) and must be installed inside a conductive control panel. The tests were conducted with the module installed in a control panel.

*2 The accuracy of analog input and analog output may temporarily vary within ±10%.

Installation in a control panel

The module is an open type device and must be installed inside a control panel.

This ensures safety as well as effective shielding of module-generated electromagnetic noise.

■Control panel

- Use a conductive control panel.
- When securing the top or bottom plate using bolts, cover the grounding part on the control panel so that the part will not be painted.
- To ensure electrical contact between inner plates and the control panel, mask off the bolt installation areas of each inner plate so that conductivity can be ensured in the largest area.
- Ground the control panel with a thick ground cable so that low impedance can be ensured even at high frequencies.
- Keep the diameter of the holes on the control panel to 10cm or less. If the diameter is larger than 10cm, electromagnetic wave may leak. In addition, because radio waves leak through a clearance between the control panel and its door, reduce the clearance as much as possible. The leakage of radio waves can be suppressed by the direct application of an EMI gasket on the paint surface.

Our tests have been carried out on a control panel having the damping characteristics of 56dB (max.) and 48dB (mean) (measured by 3m method, 30 to 300MHz).

■Wiring of power cables and ground cables

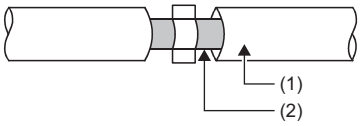
Near the power supply part, provide a ground point to the control panel. Ground the FG terminal with the thickest and shortest possible ground cable (30cm or shorter).

Cables

Use shielded cables for the cables which are connected to the module and run out from the control panel. If a shielded cable is not used or not grounded correctly, the noise immunity will not meet the standard value.

■Network cable

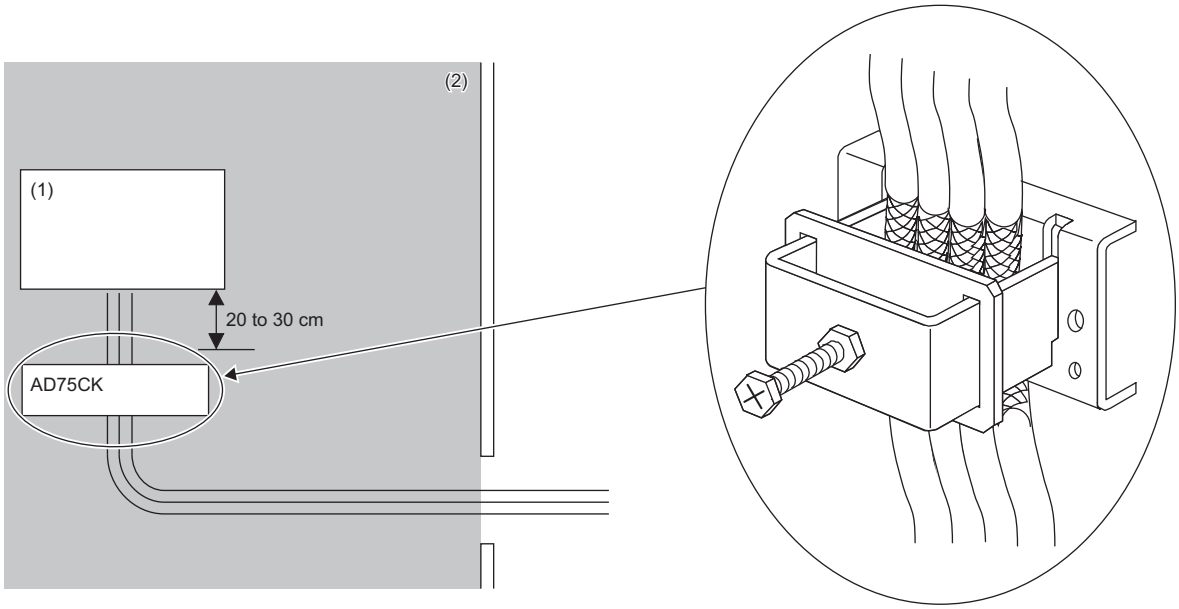
Network cables are shielded cables. Strip a part of the jacket as shown below and ground the exposed shield in the largest possible area.



(1) Network cable
(2) Shield

■Grounding the cable clamp

Use shielded cables for external wiring and ground the shields of the external wiring cables to the control panel with the AD75CK cable clamp (manufactured by Mitsubishi Electric Corporation). (Ground the shield section 20 to 30cm away from the module.)



(1) Module
(2) In the control panel

For details on AD75CK, refer to the following.

AD75CK-type Cable Clamping Instruction Manual

■I/O signal lines

For the lengths of signal lines to be connected to the I/O terminal block of the module, observe the following.

Signal	Length
Digital input	30m or shorter
Digital output	3m or shorter
Differential input	30m or shorter
Differential output	8m or shorter
Differential input/output	10m or shorter
Analog input	30m or shorter
Analog output	30m or shorter

■JTAG connector and FPGA download cable

Do not use the JTAG connector and the FPGA download cable in an environment that is affected by noise.

External power supply

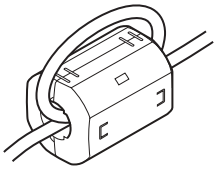
- Use a CE-marked product for an external power supply and always ground the FG terminal. (External power supply used for the tests conducted by Mitsubishi: ESSENTIAL-PS/1AC/24DC/240W/EE manufactured by PHOENIX CONTACT GmbH & Co. KG)
- Use a power cable of 10m or shorter when connecting it to the module power supply terminal and the digital output terminal.

Others

■Ferrite core

Ferrite cores are effective in reducing radiation noise of 30 to 200MHz.
It is recommended to attach ferrite cores to the I/O cables coming out of the control panel.
For I/O cables, attach the ferrite cores at the position closest to the cable hole inside the control panel.
When attaching the ferrite core, pass the cable through a hole of the ferrite core. (1 turn). (Ferrite core used for the tests conducted by Mitsubishi: E04SR401938 manufactured by SEIWA ELECTRIC MFG. CO., LTD.)
For network cables as well as terminals that are connected to the module power supply of the FPGA module and the external power supply, attach a ferrite core 4cm away from the module. (Ferrite core used for the tests conducted by Mitsubishi: ZCAT3035-1330 manufactured by TDK Corporation)
When using a ferrite core for the module power supply and the external power supply, wind the cable around the ferrite core by one (2 turn). When using it for network cables, pass the cable through a hole of the ferrite core (1 turn). If attached at an improper position, the ferrite core will not produce any effect.

Ex.
Example of attaching a ferrite core (2 turn)

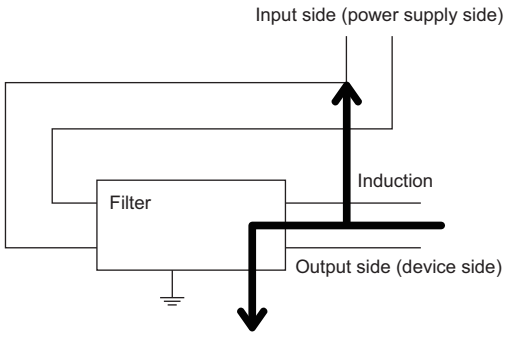


■Noise filter (power supply line filter)

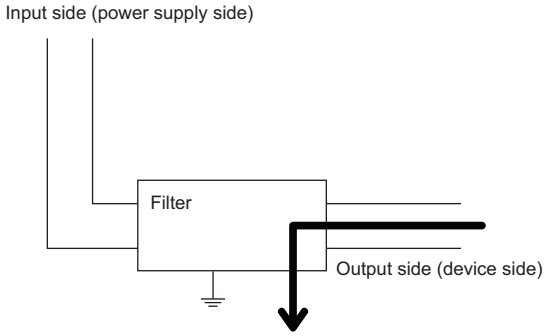
A noise filter is a component which has an effect on conducted noise. Attaching the filter can suppress more noise. (The noise filter has the effect of reducing conducted noise of 10MHz or less.)
Connect a noise filter to the external power supply. Use a noise filter with the damping characteristics equivalent to those of RSMN-2006 (manufactured by TDK-Lambda Corporation). Note that a noise filter is not required if the module is used in Zone A defined in EN61131-2.
The precautions for attaching a noise filter are described below.

- Do not bundle the cables on the input side and output side of the noise filter. If bundled, the output side noise will be induced into the input side cables from which the noise was removed.

• Example of failure
Bundling input and output wires all together induces noise.



• Example of countermeasure
Route the input and output wires separated from each other.



- Ground the noise filter grounding terminal to the control panel with the shortest cable possible (approx. 10cm).
- Install a noise filter within 3m from the module. (a distance between the external power supply and the module: 10m)

FPGA circuit

Do not change the source code of the standard circuit part provided by Mitsubishi. For each input filter, set a condition that is recommended by Mitsubishi or higher.

Requirements for compliance with the Low Voltage Directive

The module operates at the rated voltage of 24VDC.

The Low Voltage Directive is not applied to the modules that operate at the rated voltage of less than 50VAC and 75VDC.

Appendix 11 How to Check Production Information and Firmware Version

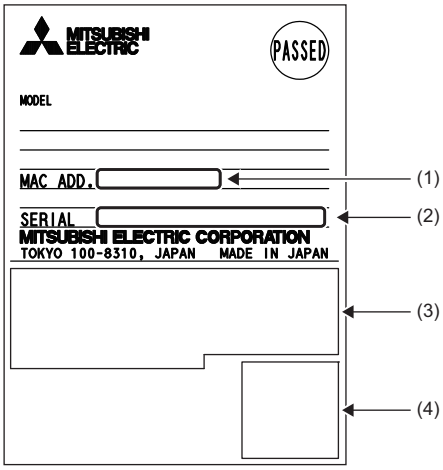
Checking the production information

The manufacturing information of the FPGA module can be checked below.

- Rating plate
- CC-Link IE TSN/CC-Link IE Field Diagnostics

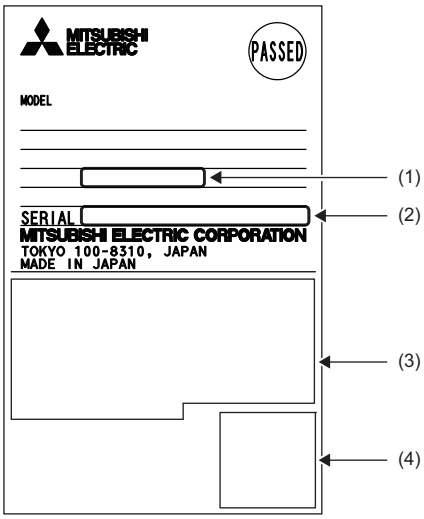
Checking on the rating plate

■Main module



(1) MAC address
(2) Production information
(3) Relevant standard symbol
(4) QR code

■Extension module



(1) MAC address
(2) Production information
(3) Relevant standard symbol
(4) QR code

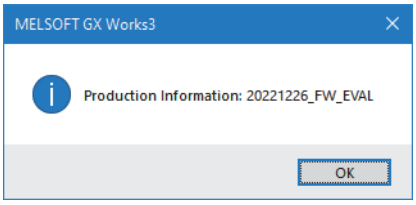
Checking by using CC-Link IE TSN/CC-Link IE Field diagnostics

Operating procedure

1. Connect the engineering tool to the CPU module.
2. Start CC-Link IE TSN/CC-Link IE Field diagnostics from the menu.

[Diagnostics] ⇨ [CC-Link IE TSN/CC-Link IE Field Diagnostics]

3. Right-click the device station and then select "Production Information" to display the production information.
4. The production information appears.



■Checking with the "Station Information List" window

For how to check the production information, refer to the following.

☞ Page 431 Checking station information

Checking the firmware version

Check the firmware version of FPGA module with the following.

- "Station Information List" window of CC-Link IE TSN/CC-Link IE Field Diagnostics
- CC-Link IE TSN Firmware Update Tool
- FPGA Module Configuration Tool

Point

For an I/O module on which a firmware update has not been performed yet, the firmware version can be checked with the production information. (The first two digits of production information show the firmware version.)

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Appendix 12 Port Number

The following table lists the port numbers of FPGA module.

System port numbers cannot be specified.

Use a port number that matches the content of communication with the communication destination and the communication method.

Port Number		Application
Decimal	Hexadecimal	
20	14H	For system
21	15H	
161	A1H	For system
5001	1389H	For system
45238	B0B6H	For system
45239	B0B7H	SLMP Transmission Port (UDP/IP)
62000 to 65534	F230H to FFFEH	FTP transmission port (TCP/IP) (used by the FTP client function)

Appendix 13 Warning List

Sample circuit warning list

No.	Target file	Corresponding part	Description
1	*.fit.rpt	Warning (169133): Can't reserve pin RESERVED_AC13 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AC19 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AD18 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AD20 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AD22 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AD26 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AE23 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AF22 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_AF24 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_T17 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_U15 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_U16 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_U17 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_U9 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_V19 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_V9 -- pin name is an illegal or unsupported format Warning (169133): Can't reserve pin RESERVED_W18 -- pin name is an illegal or unsupported format	Warning about the pin assignment for DDR3L SDRAM. There is no problem since the settings are intended in the sample circuit.
2	*.fit.rpt	Critical Warning (11887): The following pin RESERVED_U9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC13 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_T17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD20 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AE23 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U16 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U15 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF24 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD26 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_W18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC13 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded	Warning about the pin assignment for DDR3L SDRAM. There is no problem since the settings are intended in the sample circuit.

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No.	Target file	Corresponding part	Description
2	*.fit.rpt	Critical Warning (11887): The following pin RESERVED_T17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD20 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AE23 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U16 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U15 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF24 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD26 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_W18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V9 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC13 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_T17 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD20 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD22 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AE23 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U16 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_U15 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AF24 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AD26 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_AC19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_W18 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded Critical Warning (11887): The following pin RESERVED_V19 was placed in a reserved GND location. This may cause decreased performance for HMC. Intel recommends the pin location to be grounded	Warning about the pin assignment for DDR3L SDRAM. There is no problem since the settings are intended in the sample circuit.
3	*.fit.rpt	Warning (332043): Overwriting existing clock: altera_reserved_tck	Clock constraint for the JTAG terminal. There is no problem since the settings are intended in the sample circuit.

No.	Target file	Corresponding part	Description
4	*.fit.rpt	Warning (332174): Ignored filter at pt2_top_ni2_top_cpu.sdc(48): *pt2_top_ni2_top_cpu:*|pt2_top_ni2_top_cpu_nios2_oci:the_pt2_top_ni2_top_cpu_nios2_oci|pt2_top_ni2_top_cpu_nios2_oci_debug:the_pt2_top_ni2_top_cpu_nios2_oci_debug|monitor_ready could not be matched with a keeper File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 48 Warning (332049): Ignored set_false_path at pt2_top_ni2_top_cpu.sdc(48): Argument <from> is an empty collection File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 48 Warning (332174): Ignored filter at pt2_top_ni2_top_cpu.sdc(49): *pt2_top_ni2_top_cpu:*|pt2_top_ni2_top_cpu_nios2_oci:the_pt2_top_ni2_top_cpu_nios2_oci|pt2_top_ni2_top_cpu_nios2_oci_debug:the_pt2_top_ni2_top_cpu_nios2_oci_debug|monitor_error could not be matched with a keeper File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 49 Warning (332049): Ignored set_false_path at pt2_top_ni2_top_cpu.sdc(49): Argument <from> is an empty collection File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 49	Warning for IP of the sample circuit. There is no problem.
5	*.fit.rpt	Warning (171167): Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.	Warning for IP of the sample circuit. There is no problem.*1
6	*.map.rpt	Warning (12251): Pt2_top.dc3_top: 'Quick' simulation modes are NOT timing accurate. Some simulation memory models may issue warnings or errors Warning (12251): Pt2_top.dc3_top.pll_bridge: pll_bridge.pll_sharing cannot be both connected and exported Warning (12251): Pt2_top.dc3_top: dc3_top.pll_sharing must be exported, or connected to a matching conduit. Warning (10229): Verilog HDL Expression warning at pt2_top_ni2_top_cpu.v(2098): truncated literal to match 32 bits File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.v Line: 2098 Warning (10229): Verilog HDL Expression warning at pt2_top_ni2_top_cpu.v(2100): truncated literal to match 32 bits File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.v Line: 2100 Warning (10229): Verilog HDL Expression warning at pt2_top_ni2_top_cpu.v(3859): truncated literal to match 32 bits File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.v Line: 3859 Warning (10229): Verilog HDL Expression warning at pt2_top_ni2_top_cpu.v(4525): truncated literal to match 32 bits File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.v Line: 4525 Warning (10229): Verilog HDL Expression warning at pt2_top_ni2_top_cpu.v(4527): truncated literal to match 32 bits File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.v Line: 4527 Warning (10036): Verilog HDL or VHDL warning at pt2_top_dc3_top_p0_acv_hard_memphy.v(461): object "seq_calib_init_reg" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_p0_acv_hard_memphy.v Line: 461 Warning (10230): Verilog HDL assignment warning at pt2_top_dc3_top_p0_acv_hard_memphy.v(582): truncated value with size 4 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_p0_acv_hard_memphy.v Line: 582 Warning (10034): Output port "ddio_phy_dqdin[179..68]" at pt2_top_dc3_top_p0_acv_hard_io_pads.v(192) has no driver File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_p0_acv_hard_io_pads.v Line: 192 Warning (10034): Output port "ddio_phy_dqdin[35..32]" at pt2_top_dc3_top_p0_acv_hard_io_pads.v(192) has no driver File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_p0_acv_hard_io_pads.v Line: 192 Warning (10036): Verilog HDL or VHDL warning at pt2_top_dc3_top_dmaster_timing_adt.sv(82): object "in_ready" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_dmaster_timing_adt.sv Line: 82 Warning (10036): Verilog HDL or VHDL warning at pt2_top_dc3_top_dmaster_b2p_adapter.sv(78): object "out_channel" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_dmaster_b2p_adapter.sv Line: 78 Warning (10230): Verilog HDL assignment warning at pt2_top_dc3_top_dmaster_b2p_adapter.sv(90): truncated value with size 8 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_dmaster_b2p_adapter.sv Line: 90 Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1166): truncated value with size 320 to match size of target (64) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1166 Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1167): truncated value with size 320 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1167 Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1168): truncated value with size 320 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1168 Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1169): truncated value with size 320 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1169	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1170): truncated value with size 320 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/ altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1170 Warning (10230): Verilog HDL assignment warning at altera_mem_if_hard_memory_controller_top_cyclonev.sv(1171): truncated value with size 320 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/ altera_mem_if_hard_memory_controller_top_cyclonev.sv Line: 1171 Warning (10036): Verilog HDL or VHDL warning at altera_merlin_width_adapter.sv(283): object "in_write" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/ altera_merlin_width_adapter.sv Line: 283 Warning (10036): Verilog HDL or VHDL warning at altera_merlin_width_adapter.sv(742): object "aligned_addr" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/ altera_merlin_width_adapter.sv Line: 742 Warning (10036): Verilog HDL or VHDL warning at altera_merlin_width_adapter.sv(743): object "aligned_byte_cnt" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/ altera_merlin_width_adapter.sv Line: 743 Warning (113015): Width of data items in "nios_fw_mem.hex" is greater than the memory width. Wrapping data items to subsequent addresses. Found 960 warnings, reporting 10 File: C:/FPGA_release/RTL/TOP/PT/ mem_init/nios_fw_mem.hex Line: 1 Warning (113009): Data at line (2) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 2 Warning (113009): Data at line (3) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 3 Warning (113009): Data at line (4) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 4 Warning (113009): Data at line (5) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 5 Warning (113009): Data at line (6) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 6 Warning (113009): Data at line (7) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 7 Warning (113009): Data at line (8) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 8 Warning (113009): Data at line (9) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 9 Warning (113009): Data at line (10) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 10 Warning (113009): Data at line (11) of memory initialization file "nios_fw_mem.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_fw_mem.hex Line: 11 Warning (113015): Width of data items in "nios_ram_init.hex" is greater than the memory width. Wrapping data items to subsequent addresses. Found 640 warnings, reporting 10 File: C:/FPGA_release/RTL/TOP/PT/ mem_init/nios_ram_init.hex Line: 1 Warning (113009): Data at line (2) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_ram_init.hex Line: 2 Warning (113009): Data at line (3) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_ram_init.hex Line: 3 Warning (113009): Data at line (4) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_ram_init.hex Line: 4 Warning (113009): Data at line (5) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_ram_init.hex Line: 5 Warning (113009): Data at line (6) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/ nios_ram_init.hex Line: 6	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (113009): Data at line (7) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/nios_ram_init.hex Line: 7 Warning (113009): Data at line (8) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/nios_ram_init.hex Line: 8 Warning (113009): Data at line (9) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/nios_ram_init.hex Line: 9 Warning (113009): Data at line (10) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/nios_ram_init.hex Line: 10 Warning (113009): Data at line (11) of memory initialization file "nios_ram_init.hex" is too wide to fit in one memory word. Wrapping data to subsequent addresses. File: C:/FPGA_release/RTL/TOP/PT/mem_init/nios_ram_init.hex Line: 11 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(267): object "av_write_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 267 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(268): object "av_read_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 268 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(269): object "av_address_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 269 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(270): object "av_writedata_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 270 Warning (10036): Verilog HDL or VHDL warning at altera_merlin_width_adapter.sv(283): object "in_write" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_merlin_width_adapter.sv Line: 283 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(267): object "av_write_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 267 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(268): object "av_read_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 268 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(269): object "av_address_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 269 Warning (10036): Verilog HDL or VHDL warning at altera_error_response_slave.sv(270): object "av_writedata_in" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_error_response_slave.sv Line: 270 Warning (10230): Verilog HDL assignment warning at altera_merlin_traffic_limiter.sv(721): truncated value with size 7 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_merlin_traffic_limiter.sv Line: 721 Warning (10230): Verilog HDL assignment warning at altera_merlin_traffic_limiter.sv(721): truncated value with size 7 to match size of target (1) File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_merlin_traffic_limiter.sv Line: 721 Warning (10036): Verilog HDL or VHDL warning at altera_merlin_width_adapter.sv(283): object "in_write" assigned a value but never read File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_merlin_width_adapter.sv Line: 283 Warning (12010): Port "ir_out" on the entity instantiation of "node" is connected to a signal of width 1. The formal width of the signal in the module is 3. The extra bits will be driven by GND. File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/altera_avalon_st_jtag_interface.v Line: 101 Warning (14284): Synthesized away the following node(s): Warning (14285): Synthesized away the following RAM node(s): Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[32]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1064 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[33]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1096Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[34]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1128	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[35]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1160 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[36]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1192 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[37]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1224 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[38]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1256 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[39]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1288 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[40]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1320 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[41]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1352 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[42]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1384 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|write_master:write_mstr_internal|scfifo:the_st_to_master_fifo|scfifo_s871:auto_generated|a_dpfifo_f071:dpfifo|altsyncram_3hn1:FIFOram|q_b[43]" File: C:/FPGA_release/Layout/db/altsyncram_3hn1.tdf Line: 1416 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[32]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1064 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[33]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1096 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[34]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1128 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[35]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1160 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[36]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1192 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[37]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1224 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[38]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1256 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[39]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1288	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[40]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1320 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[41]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1352 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[42]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1384 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[43]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1416 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[44]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1448 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[45]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1480 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[46]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1512 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[47]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1544 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[48]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1576 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[49]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1608 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[50]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1640 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|read_master:read_mstr_internal|scfifo:the_master_to_st_fifo|scfifo_r871:auto_generated|a_dpfifo_e071:dpfifo|altsyncram_1hn1:FIFOram|q_b[51]" File: C:/FPGA_release/Layout/db/altsyncram_1hn1.tdf Line: 1672 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[0]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 39 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[1]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 72 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[2]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 105 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[3]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 138 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[4]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 171	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[5]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 204 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[6]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 237 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[7]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 270 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[8]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 303 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[9]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 336 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[10]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 369 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[11]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 402 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[12]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 435 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[13]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 468 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[14]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 501 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[15]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 534 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[16]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 567 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[17]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 600 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[18]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 633 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[19]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 666 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[20]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 699 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[21]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 732	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[22]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 765 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[23]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 798 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[24]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 831 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[25]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 864 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[26]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 897 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[27]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 930 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[28]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 963 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[29]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 996 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[30]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1029 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[31]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1062 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[75]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2514 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[76]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2547 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[77]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2580 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[78]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2613 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[79]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2646 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[80]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2679 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[81]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2712	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[82]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2745 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[83]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2778 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[84]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2811 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[85]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2844 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[86]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2877 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[87]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2910 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[88]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2943 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[89]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2976 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[90]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3009 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[91]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3042 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[92]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3075 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[93]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3108 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[94]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3141 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[95]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3174 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[96]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3207 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[97]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3240 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[98]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3273	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[99]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3306 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[100]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3339 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[101]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3372 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[102]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3405 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[103]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3438 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[104]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3471 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[105]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3504 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[106]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3537 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[109]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3636 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[111]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3702 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[112]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3735 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[113]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3768 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[114]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3801 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[115]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3834 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[116]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3867 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[117]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3900 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[118]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3933	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[119]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3966 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[120]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3999 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[121]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4032 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[122]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4065 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[123]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4098 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[124]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4131 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[125]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4164 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[126]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4197 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[127]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4230 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[32]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1095 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[33]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1128 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[34]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1161 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[35]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1194 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[36]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1227 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[37]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1260 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[38]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1293 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[39]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1326	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[40]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1359 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[41]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1392 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[42]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1425 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[43]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1458 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[44]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1491 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[45]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1524 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[46]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1557 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[47]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1590 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[48]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1623 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[49]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1656 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[50]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1689 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[51]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1722 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[52]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1755 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[53]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1788 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[54]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1821 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[55]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1854 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[56]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1887	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[57]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1920 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[58]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1953 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[59]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1986 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[60]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2019 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[61]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2052 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[62]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2085 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[63]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2118 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[75]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2514 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[76]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2547 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[77]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2580 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[78]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2613 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[79]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2646 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[80]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2679 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[81]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2712 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[82]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2745 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[83]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2778 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[84]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2811	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[85]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2844 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[86]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2877 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[87]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2910 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[88]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2943 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[89]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 2976 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[90]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3009 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[91]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3042 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[92]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3075 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[93]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3108 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[94]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3141 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[95]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3174 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[104]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3471 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[105]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3504 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[107]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3570 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[108]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3603 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[109]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3636 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[110]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3669	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[111]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3702 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[121]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4032 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[122]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4065 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[123]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4098 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[124]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4131 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[125]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4164 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[126]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4197 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[127]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 4230 Warning (14285): Synthesized away the following PLL node(s): Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dc3_top:dc3_top|pt2_top_dc3_top_pll0:pll0|afi_phy_clk" File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_pll0.sv Line: 200 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dc3_top:dc3_top|pt2_top_dc3_top_pll0:pll0|pll_mem_clk" File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_pll0.sv Line: 233 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dc3_top:dc3_top|pt2_top_dc3_top_pll0:pll0|pll_addr_cmd_clk" File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_dc3_top_pll0.sv Line: 329 Warning (14284): Synthesized away the following node(s): Warning (14285): Synthesized away the following RAM node(s): Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[96]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3207 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[97]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3240 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[98]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3273 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[99]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3306 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[100]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3339 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[101]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3372	Warning for IP of the sample circuit. There is no problem.

No.	Target file	Corresponding part	Description
6	*.map.rpt	Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[102]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3405 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[103]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3438 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[112]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3735 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[113]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3768 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[114]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3801 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[115]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3834 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[116]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3867 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[117]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3900 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[118]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3933 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[119]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3966 Warning (14284): Synthesized away the following node(s): Warning (14285): Synthesized away the following RAM node(s): Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[33]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1128 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[32]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 1095 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[1]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 72 Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_read_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[0]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 39 Warning (12241): 43 hierarchies have connectivity warnings - see the Connectivity Checks report folder Warning (14284): Synthesized away the following node(s): Warning (14285): Synthesized away the following RAM node(s): Warning (14320): Synthesized away node "pt2_top:u_pt2_top|pt2_top_dm3_top:dm3_top|dispatcher:dispatcher_internal|descriptor_buffers:the_descriptor_buffers|fifo_with_byteenables:the_write_command_FIFO|altsyncram:the_dp_ram|altsyncram_p2j1:auto_generated|q_b[108]" File: C:/FPGA_release/Layout/db/altsyncram_p2j1.tdf Line: 3603	Warning for IP of the sample circuit. There is no problem.

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No.	Target file	Corresponding part	Description
7	*.map.rpt	Warning (10036): Verilog HDL or VHDL warning at is3_inout_sel.v(793): object "is_iob0_a_on_d1_clk100m_reg" assigned a value but never read File: C:/FPGA_release/RTL/TOP/IS/is3_inout_sel.v Line: 793 Warning (10036): Verilog HDL or VHDL warning at is3_inout_sel.v(796): object "is_iob1_a_on_d1_clk100m_reg" assigned a value but never read File: C:/FPGA_release/RTL/TOP/IS/is3_inout_sel.v Line: 796 Warning (10036): Verilog HDL or VHDL warning at is3_inout_sel.v(799): object "is_iob2_a_on_d1_clk100m_reg" assigned a value but never read File: C:/FPGA_release/RTL/TOP/IS/is3_inout_sel.v Line: 799	Signals for future extension are mounted. It is open on purpose, so there is no problem.
8	*.map.rpt	Warning (21074): Design contains 5 input pin(s) that do not drive logic Warning (15610): No output dependent on input pin "CPU_BUSCLK" File: C:/FPGA_release/RTL/TOP/TOP/top1.v Line: 266 Warning (15610): No output dependent on input pin "CPU_A26" File: C:/FPGA_release/RTL/TOP/TOP/top1.v Line: 295 Warning (15610): No output dependent on input pin "CPU_A27" File: C:/FPGA_release/RTL/TOP/TOP/top1.v Line: 296 Warning (15610): No output dependent on input pin "CPU_WRL0" File: C:/FPGA_release/RTL/TOP/TOP/top1.v Line: 301 Warning (15610): No output dependent on input pin "CPU_WRL1" File: C:/FPGA_release/RTL/TOP/TOP/top1.v Line: 302	Warning about the FPGA terminal. Fixed values of external terminals (1: VCC, 0: GND) are input to the external terminals. There is no problem since it is non-dominant fixed on the circuit board.
9	*.sta.rpt	Warning (332043): Overwriting existing clock: altera_reserved_tck	Clock constraint for the JTAG terminal. There is no problem since the settings are intended in the sample circuit.
10	*.sta.rpt	Warning (332174): Ignored filter at pt2_top_ni2_top_cpu.sdc(48): *pt2_top_ni2_top_cpu:*|pt2_top_ni2_top_cpu_nios2_oci:the_pt2_top_ni2_top_cpu_nios2_oci|pt2_top_ni2_top_cpu_nios2_oci_debug:the_pt2_top_ni2_top_cpu_nios2_oci_debug|monitor_ready could not be matched with a keeper File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 48 Warning (332049): Ignored set_false_path at pt2_top_ni2_top_cpu.sdc(48): Argument <from> is an empty collection File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 48 Warning (332174): Ignored filter at pt2_top_ni2_top_cpu.sdc(49): *pt2_top_ni2_top_cpu:*|pt2_top_ni2_top_cpu_nios2_oci:the_pt2_top_ni2_top_cpu_nios2_oci|pt2_top_ni2_top_cpu_nios2_oci_debug:the_pt2_top_ni2_top_cpu_nios2_oci_debug|monitor_error could not be matched with a keeper File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 49 Warning (332049): Ignored set_false_path at pt2_top_ni2_top_cpu.sdc(49): Argument <from> is an empty collection File: C:/FPGA_release/Layout/db/ip/pt2_top/submodules/pt2_top_ni2_top_cpu.sdc Line: 49	Warning for IP of the sample circuit. There is no problem.
11	*.fit.rpt	Warning (292013): Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.	Warning for logic lock. There is no problem.

*1 The ignored assignments for the sample circuit are shown below.

No.	Name	Ignored Entity	Ignored From	Ignored To	Ignored Value	Ignored Source
1	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[0].oe_reg	ON	Compiler or HDL Assignment
2	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[1].oe_reg	ON	Compiler or HDL Assignment
3	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[2].oe_reg	ON	Compiler or HDL Assignment
4	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[3].oe_reg	ON	Compiler or HDL Assignment
5	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[4].oe_reg	ON	Compiler or HDL Assignment
6	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[5].oe_reg	ON	Compiler or HDL Assignment
7	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[6].oe_reg	ON	Compiler or HDL Assignment
8	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[7].oe_reg	ON	Compiler or HDL Assignment
9	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uio_pads|dq_ddio[0].read_capture_clk_buffer	OFF	QSF Assignment
10	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uio_pads|dq_ddio[1].read_capture_clk_buffer	OFF	QSF Assignment
11	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_wraddress[0]	OFF	QSF Assignment

No.	Name	Ignored Entity	Ignored From	Ignored To	Ignored Value	Ignored Source
12	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_wraddress[1]	OFF	QSF Assignment
13	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_write_side[0]	OFF	QSF Assignment
14	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_write_side[1]	OFF	QSF Assignment
15	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|ureset|phy_reset_mem_stable_n	OFF	QSF Assignment
16	Global Signal	top1	—	u_pt2_top|dc3_top|s0|sequencer_rw_mgr_inst|rw_mgr_inst|rw_mgr_core_inst|rw_soft_reset_n	OFF	QSF Assignment
17	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_N[0]	0	QSF Assignment
18	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_N[1]	0	QSF Assignment
19	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_P[0]	0	QSF Assignment
20	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_P[1]	0	QSF Assignment

Provided pattern warning list

No.	Target file	Corresponding part	Description
1	Common to all provided patterns	# Warning: DONT_CARE value for read_during_write_mode_port_a is not supported in Stratix device family, it might cause incorrect behavioural simulation result	It states that Stratix devices are not supported. Since this FPGA is the cyclone device, there is no problem.
2	Common to all provided patterns	# Warning: # Warning:	Pseudo warning output from the DDR3L SDRAM simulation model. There is no problem.
3	Common to all provided patterns	### Warning ### Need to wait [□□□]us and keep CKE=0 at least 10 ns prior to releasing reset[*1] ### Warning ### Need to wait [□□□]us after reset releasing and prior to CKE=1.[*1]	Pseudo warning output from the DDR3L SDRAM simulation model. There is no problem.
4	FNA_TOP_01010101.log	—	—
5	FNA_TOP_01010102.log	—	—
6	FNA_TOP_01010103.log	—	—
7	FNA_TOP_01010104.log	—	—
8	FNA_TOP_01010105.log	—	—
9	FNA_TOP_01010106.log	—	—
10	FNA_TOP_01010107.log	—	—
11	FNA_TOP_01010108.log	—	—

*1 In □□□, a different numerical value is entered for each pattern. The ignored assignments for the sample circuit are shown below.

No.	Name	Ignored Entity	Ignored From	Ignored To	Ignored Value	Ignored Source
1	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[0].oe_reg	ON	Compiler or HDL Assignment
2	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[1].oe_reg	ON	Compiler or HDL Assignment
3	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[2].oe_reg	ON	Compiler or HDL Assignment
4	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[3].oe_reg	ON	Compiler or HDL Assignment
5	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[4].oe_reg	ON	Compiler or HDL Assignment
6	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[5].oe_reg	ON	Compiler or HDL Assignment
7	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[6].oe_reg	ON	Compiler or HDL Assignment
8	Fast Output Enable Register	altdq_dqs2_acv_connect_to_hard_phy_cyclonev	—	output_path_gen[7].oe_reg	ON	Compiler or HDL Assignment
9	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uio_pads|dq_ddio[0].read_capture_clk_buffer	OFF	QSF Assignment
10	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uio_pads|dq_ddio[1].read_capture_clk_buffer	OFF	QSF Assignment
11	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_wraddress[0]	OFF	QSF Assignment
12	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_wraddress[1]	OFF	QSF Assignment
13	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_write_side[0]	OFF	QSF Assignment
14	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|uread_datapath|reset_n_fifo_write_side[1]	OFF	QSF Assignment
15	Global Signal	top1	—	u_pt2_top|dc3_top|p0|umemphy|ureset|phy_reset_mem_stable_n	OFF	QSF Assignment

No.	Name	Ignored Entity	Ignored From	Ignored To	Ignored Value	Ignored Source
16	Global Signal	top1	—	u_pt2_top|dc3_top|s0|sequencer_rw_mgr_inst|rw_mgr_inst|rw_mgr_core_inst|rw_soft_reset_n	OFF	QSF Assignment
17	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_N[0]	0	QSF Assignment
18	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_N[1]	0	QSF Assignment
19	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_P[0]	0	QSF Assignment
20	D6 Delay (output register to io buffer)	top1	—	DDR_DQS_P[1]	0	QSF Assignment

Appendix 14 Logging Data Bit Assignment

The table below shows the summary of logging target signals.
When the user circuit logging mode is the time division mode, 1024-bit signals are logged.
No.0 to No.431 are output from the user circuit part block for the first time, and No.432 to No.511 are assigned by the logging control part.
No.512 to No.943 are output for the second time, and No.944 to No.1023 are assigned by the logging control part.
When the user circuit logging mode is the non-time division mode, 512-bit signals are logged.
The user circuit part block continues to output No.0 to No.431, and No.432 to No.511 are assigned by the logging control part.
The location — is fixed to 0.

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
0	1	0	Digital input signal ch0 (B0 after filtering)	Digital input signal ch0 (B0 after filtering)
1		1	Digital input signal ch1 (B0 after filtering)	Digital input signal ch1 (B0 after filtering)
2		2	Digital input signal ch2 (B0 after filtering)	Digital input signal ch2 (B0 after filtering)
3		3	Digital input signal ch3 (B0 after filtering)	Digital input signal ch3 (B0 after filtering)
4		4	Digital input signal ch4 (B0 after filtering)	Digital input signal ch4 (B0 after filtering)
5		5	Digital input signal ch5 (B0 after filtering)	Digital input signal ch5 (B0 after filtering)
6		6	Digital input signal ch6 (B0 after filtering)	Digital input signal ch6 (B0 after filtering)
7		7	Digital input signal ch7 (B0 after filtering)	Digital input signal ch7 (B0 after filtering)
8		8	Digital input signal ch8 (B0 after filtering)	Digital input signal ch8 (B0 after filtering)
9		9	Digital input signal ch9 (B0 after filtering)	Digital input signal ch9 (B0 after filtering)
10		10	Digital input signal chA (B0 after filtering)	Digital input signal chA (B0 after filtering)
11		11	Digital input signal chB (B0 after filtering)	Digital input signal chB (B0 after filtering)
12		12	Digital input signal chC (B0 after filtering)	Digital input signal chC (B0 after filtering)
13		13	Digital input signal chD (B0 after filtering)	Digital input signal chD (B0 after filtering)
14		14	Digital input signal chE (B0 after filtering)	Digital input signal chE (B0 after filtering)
15		15	Digital input signal chF (B0 after filtering)	Digital input signal chF (B0 after filtering)
16	2	16	Digital input signal ch0 (B1 after filtering)	Digital input signal ch0 (B1 after filtering)
17		17	Digital input signal ch1 (B1 after filtering)	Digital input signal ch1 (B1 after filtering)
18		18	Digital input signal ch2 (B1 after filtering)	Digital input signal ch2 (B1 after filtering)
19		19	Digital input signal ch3 (B1 after filtering)	Digital input signal ch3 (B1 after filtering)
20		20	Digital input signal ch4 (B1 after filtering)	Digital input signal ch4 (B1 after filtering)
21		21	Digital input signal ch5 (B1 after filtering)	Digital input signal ch5 (B1 after filtering)
22		22	Digital input signal ch6 (B1 after filtering)	Digital input signal ch6 (B1 after filtering)
23		23	Digital input signal ch7 (B1 after filtering)	Digital input signal ch7 (B1 after filtering)
24		24	Digital input signal ch8 (B1 after filtering)	Digital input signal ch8 (B1 after filtering)
25		25	Digital input signal ch9 (B1 after filtering)	Digital input signal ch9 (B1 after filtering)
26		26	Digital input signal chA (B1 after filtering)	Digital input signal chA (B1 after filtering)
27		27	Digital input signal chB (B1 after filtering)	Digital input signal chB (B1 after filtering)
28		28	Digital input signal chC (B1 after filtering)	Digital input signal chC (B1 after filtering)
29		29	Digital input signal chD (B1 after filtering)	Digital input signal chD (B1 after filtering)
30		30	Digital input signal chE (B1 after filtering)	Digital input signal chE (B1 after filtering)
31		31	Digital input signal chF (B1 after filtering)	Digital input signal chF (B1 after filtering)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
32	3	32	Digital input signal ch0 (B2 after filtering)	Digital input signal ch0 (B2 after filtering)
34		34	Digital input signal ch1 (B2 after filtering)	Digital input signal ch1 (B2 after filtering)
34		34	Digital input signal ch2 (B2 after filtering)	Digital input signal ch2 (B2 after filtering)
35		35	Digital input signal ch3 (B2 after filtering)	Digital input signal ch3 (B2 after filtering)
36		36	Digital input signal ch4 (B2 after filtering)	Digital input signal ch4 (B2 after filtering)
37		37	Digital input signal ch5 (B2 after filtering)	Digital input signal ch5 (B2 after filtering)
38		38	Digital input signal ch6 (B2 after filtering)	Digital input signal ch6 (B2 after filtering)
39		39	Digital input signal ch7 (B2 after filtering)	Digital input signal ch7 (B2 after filtering)
40		40	Digital input signal ch8 (B2 after filtering)	Digital input signal ch8 (B2 after filtering)
41		41	Digital input signal ch9 (B2 after filtering)	Digital input signal ch9 (B2 after filtering)
42		42	Digital input signal chA (B2 after filtering)	Digital input signal chA (B2 after filtering)
43		43	Digital input signal chB (B2 after filtering)	Digital input signal chB (B2 after filtering)
44		44	Digital input signal chC (B2 after filtering)	Digital input signal chC (B2 after filtering)
45		45	Digital input signal chD (B2 after filtering)	Digital input signal chD (B2 after filtering)
46		46	Digital input signal chE (B2 after filtering)	Digital input signal chE (B2 after filtering)
47		47	Digital input signal chF (B2 after filtering)	Digital input signal chF (B2 after filtering)
48	4	48	Digital input signal ch0 (E0 after filtering)	Digital input signal ch0 (E0 after filtering)
49		49	Digital input signal ch1 (E0 after filtering)	Digital input signal ch1 (E0 after filtering)
50		50	Digital input signal ch2 (E0 after filtering)	Digital input signal ch2 (E0 after filtering)
51		51	Digital input signal ch3 (E0 after filtering)	Digital input signal ch3 (E0 after filtering)
52		52	Digital input signal ch4 (E0 after filtering)	Digital input signal ch4 (E0 after filtering)
53		53	Digital input signal ch5 (E0 after filtering)	Digital input signal ch5 (E0 after filtering)
54		54	Digital input signal ch6 (E0 after filtering)	Digital input signal ch6 (E0 after filtering)
55		55	Digital input signal ch7 (E0 after filtering)	Digital input signal ch7 (E0 after filtering)
56		56	Digital input signal ch8 (E0 after filtering)	Digital input signal ch8 (E0 after filtering)
57		57	Digital input signal ch9 (E0 after filtering)	Digital input signal ch9 (E0 after filtering)
58		58	Digital input signal chA (E0 after filtering)	Digital input signal chA (E0 after filtering)
59		59	Digital input signal chB (E0 after filtering)	Digital input signal chB (E0 after filtering)
60		60	Digital input signal chC (E0 after filtering)	Digital input signal chC (E0 after filtering)
61		61	Digital input signal chD (E0 after filtering)	Digital input signal chD (E0 after filtering)
62		62	Digital input signal chE (E0 after filtering)	Digital input signal chE (E0 after filtering)
63		63	Digital input signal chF (E0 after filtering)	Digital input signal chF (E0 after filtering)
64	5	64	Digital input signal ch0 (E1 after filtering)	Digital input signal ch0 (E1 after filtering)
65		65	Digital input signal ch1 (E1 after filtering)	Digital input signal ch1 (E1 after filtering)
66		66	Digital input signal ch2 (E1 after filtering)	Digital input signal ch2 (E1 after filtering)
67		67	Digital input signal ch3 (E1 after filtering)	Digital input signal ch3 (E1 after filtering)
68		68	Digital input signal ch4 (E1 after filtering)	Digital input signal ch4 (E1 after filtering)
69		69	Digital input signal ch5 (E1 after filtering)	Digital input signal ch5 (E1 after filtering)
70		70	Digital input signal ch6 (E1 after filtering)	Digital input signal ch6 (E1 after filtering)
71		71	Digital input signal ch7 (E1 after filtering)	Digital input signal ch7 (E1 after filtering)
72		72	Digital input signal ch8 (E1 after filtering)	Digital input signal ch8 (E1 after filtering)
73		73	Digital input signal ch9 (E1 after filtering)	Digital input signal ch9 (E1 after filtering)
74		74	Digital input signal chA (E1 after filtering)	Digital input signal chA (E1 after filtering)
75		75	Digital input signal chB (E1 after filtering)	Digital input signal chB (E1 after filtering)
76		76	Digital input signal chC (E1 after filtering)	Digital input signal chC (E1 after filtering)
77		77	Digital input signal chD (E1 after filtering)	Digital input signal chD (E1 after filtering)
78		78	Digital input signal chE (E1 after filtering)	Digital input signal chE (E1 after filtering)
79		79	Digital input signal chF (E1 after filtering)	Digital input signal chF (E1 after filtering)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
80	6	80	Digital input signal ch0 (E2 after filtering)	Digital input signal ch0 (E2 after filtering)
81		81	Digital input signal ch1 (E2 after filtering)	Digital input signal ch1 (E2 after filtering)
82		82	Digital input signal ch2 (E2 after filtering)	Digital input signal ch2 (E2 after filtering)
83		83	Digital input signal ch3 (E2 after filtering)	Digital input signal ch3 (E2 after filtering)
84		84	Digital input signal ch4 (E2 after filtering)	Digital input signal ch4 (E2 after filtering)
85		85	Digital input signal ch5 (E2 after filtering)	Digital input signal ch5 (E2 after filtering)
86		86	Digital input signal ch6 (E2 after filtering)	Digital input signal ch6 (E2 after filtering)
87		87	Digital input signal ch7 (E2 after filtering)	Digital input signal ch7 (E2 after filtering)
88		88	Digital input signal ch8 (E2 after filtering)	Digital input signal ch8 (E2 after filtering)
89		89	Digital input signal ch9 (E2 after filtering)	Digital input signal ch9 (E2 after filtering)
90		90	Digital input signal chA (E2 after filtering)	Digital input signal chA (E2 after filtering)
91		91	Digital input signal chB (E2 after filtering)	Digital input signal chB (E2 after filtering)
92		92	Digital input signal chC (E2 after filtering)	Digital input signal chC (E2 after filtering)
93		93	Digital input signal chD (E2 after filtering)	Digital input signal chD (E2 after filtering)
94		94	Digital input signal chE (E2 after filtering)	Digital input signal chE (E2 after filtering)
95		95	Digital input signal chF (E2 after filtering)	Digital input signal chF (E2 after filtering)
96	7	96	32-bit ring counter (2-phase multiple of 4) Phase A (B0)	32-bit ring counter (2-phase multiple of 4) Phase A (B0)
97		97	32-bit ring counter (2-phase multiple of 4) Phase B (B0)	32-bit ring counter (2-phase multiple of 4) Phase B (B0)
98		98	—	—
99		99	—	—
100		100	—	—
101		101	—	—
102		102	—	—
103		103	—	—
104		104	—	—
105		105	—	—
106		106	—	—
107		107	—	—
108		108	—	—
109		109	—	—
110		110	—	—
111		111	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
112	8	112	32-bit ring counter (2-phase multiple of 4) bit[0] (B0)	32-bit ring counter (2-phase multiple of 4) bit[0] (B0)
113		113	32-bit ring counter (2-phase multiple of 4) bit[1] (B0)	32-bit ring counter (2-phase multiple of 4) bit[1] (B0)
114		114	32-bit ring counter (2-phase multiple of 4) bit[2] (B0)	32-bit ring counter (2-phase multiple of 4) bit[2] (B0)
115		115	32-bit ring counter (2-phase multiple of 4) bit[3] (B0)	32-bit ring counter (2-phase multiple of 4) bit[3] (B0)
116		116	32-bit ring counter (2-phase multiple of 4) bit[4] (B0)	32-bit ring counter (2-phase multiple of 4) bit[4] (B0)
117		117	32-bit ring counter (2-phase multiple of 4) bit[5] (B0)	32-bit ring counter (2-phase multiple of 4) bit[5] (B0)
118		118	32-bit ring counter (2-phase multiple of 4) bit[6] (B0)	32-bit ring counter (2-phase multiple of 4) bit[6] (B0)
119		119	32-bit ring counter (2-phase multiple of 4) bit[7] (B0)	32-bit ring counter (2-phase multiple of 4) bit[7] (B0)
120		120	32-bit ring counter (2-phase multiple of 4) bit[8] (B0)	32-bit ring counter (2-phase multiple of 4) bit[8] (B0)
121		121	32-bit ring counter (2-phase multiple of 4) bit[9] (B0)	32-bit ring counter (2-phase multiple of 4) bit[9] (B0)
122		122	32-bit ring counter (2-phase multiple of 4) bit[10] (B0)	32-bit ring counter (2-phase multiple of 4) bit[10] (B0)
123		123	32-bit ring counter (2-phase multiple of 4) bit[11] (B0)	32-bit ring counter (2-phase multiple of 4) bit[11] (B0)
124		124	32-bit ring counter (2-phase multiple of 4) bit[12] (B0)	32-bit ring counter (2-phase multiple of 4) bit[12] (B0)
125		125	32-bit ring counter (2-phase multiple of 4) bit[13] (B0)	32-bit ring counter (2-phase multiple of 4) bit[13] (B0)
126		126	32-bit ring counter (2-phase multiple of 4) bit[14] (B0)	32-bit ring counter (2-phase multiple of 4) bit[14] (B0)
127		127	32-bit ring counter (2-phase multiple of 4) bit[15] (B0)	32-bit ring counter (2-phase multiple of 4) bit[15] (B0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
128	9	128	32-bit ring counter (2-phase multiple of 4) bit[16] (B0)	32-bit ring counter (2-phase multiple of 4) bit[16] (B0)
129		129	32-bit ring counter (2-phase multiple of 4) bit[17] (B0)	32-bit ring counter (2-phase multiple of 4) bit[17] (B0)
130		130	32-bit ring counter (2-phase multiple of 4) bit[18] (B0)	32-bit ring counter (2-phase multiple of 4) bit[18] (B0)
131		131	32-bit ring counter (2-phase multiple of 4) bit[19] (B0)	32-bit ring counter (2-phase multiple of 4) bit[19] (B0)
13		13	32-bit ring counter (2-phase multiple of 4) bit[20] (B0)	32-bit ring counter (2-phase multiple of 4) bit[20] (B0)
133		133	32-bit ring counter (2-phase multiple of 4) bit[21] (B0)	32-bit ring counter (2-phase multiple of 4) bit[21] (B0)
134		134	32-bit ring counter (2-phase multiple of 4) bit[22] (B0)	32-bit ring counter (2-phase multiple of 4) bit[22] (B0)
135		135	32-bit ring counter (2-phase multiple of 4) bit[23] (B0)	32-bit ring counter (2-phase multiple of 4) bit[23] (B0)
136		136	32-bit ring counter (2-phase multiple of 4) bit[24] (B0)	32-bit ring counter (2-phase multiple of 4) bit[24] (B0)
137		137	32-bit ring counter (2-phase multiple of 4) bit[25] (B0)	32-bit ring counter (2-phase multiple of 4) bit[25] (B0)
138		138	32-bit ring counter (2-phase multiple of 4) bit[26] (B0)	32-bit ring counter (2-phase multiple of 4) bit[26] (B0)
139		139	32-bit ring counter (2-phase multiple of 4) bit[27] (B0)	32-bit ring counter (2-phase multiple of 4) bit[27] (B0)
140		140	32-bit ring counter (2-phase multiple of 4) bit[28] (B0)	32-bit ring counter (2-phase multiple of 4) bit[28] (B0)
141		141	32-bit ring counter (2-phase multiple of 4) bit[29] (B0)	32-bit ring counter (2-phase multiple of 4) bit[29] (B0)
142		142	32-bit ring counter (2-phase multiple of 4) bit[30] (B0)	32-bit ring counter (2-phase multiple of 4) bit[30] (B0)
143		143	32-bit ring counter (2-phase multiple of 4) bit[31] (B0)	32-bit ring counter (2-phase multiple of 4) bit[31] (B0)
144	10	144	32-bit ring counter (2-phase multiple of 4) Phase A (B1)	32-bit ring counter (2-phase multiple of 4) Phase A (B1)
145		145	32-bit ring counter (2-phase multiple of 4) Phase B (B1)	32-bit ring counter (2-phase multiple of 4) Phase B (B1)
146		146	—	—
147		147	—	—
148		148	—	—
149		149	—	—
150		150	—	—
151		151	—	—
152		152	—	—
153		153	—	—
154		154	—	—
155		155	—	—
156		156	—	—
157		157	—	—
158		158	—	—
159		159	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
160	11	160	32-bit ring counter (2-phase multiple of 4) bit[0] (B1)	A/D conversion value ch0[0] (E0)
161		161	32-bit ring counter (2-phase multiple of 4) bit[1] (B1)	A/D conversion value ch0[1] (E0)
162		162	32-bit ring counter (2-phase multiple of 4) bit[2] (B1)	A/D conversion value ch0[2] (E0)
163		163	32-bit ring counter (2-phase multiple of 4) bit[3] (B1)	A/D conversion value ch0[3] (E0)
164		164	32-bit ring counter (2-phase multiple of 4) bit[4] (B1)	A/D conversion value ch0[4] (E0)
165		165	32-bit ring counter (2-phase multiple of 4) bit[5] (B1)	A/D conversion value ch0[5] (E0)
166		166	32-bit ring counter (2-phase multiple of 4) bit[6] (B1)	A/D conversion value ch0[6] (E0)
167		167	32-bit ring counter (2-phase multiple of 4) bit[7] (B1)	A/D conversion value ch0[7] (E0)
168		168	32-bit ring counter (2-phase multiple of 4) bit[8] (B1)	A/D conversion value ch0[8] (E0)
169		169	32-bit ring counter (2-phase multiple of 4) bit[9] (B1)	A/D conversion value ch0[9] (E0)
170		170	32-bit ring counter (2-phase multiple of 4) bit[10] (B1)	A/D conversion value ch0[10] (E0)
171		171	32-bit ring counter (2-phase multiple of 4) bit[11] (B1)	A/D conversion value ch0[11] (E0)
172		172	32-bit ring counter (2-phase multiple of 4) bit[12] (B1)	A/D conversion value ch0[12] (E0)
173		173	32-bit ring counter (2-phase multiple of 4) bit[13] (B1)	A/D conversion value ch0[13] (E0)
174		174	32-bit ring counter (2-phase multiple of 4) bit[14] (B1)	A/D conversion value ch0[14] (E0)
175		175	32-bit ring counter (2-phase multiple of 4) bit[15] (B1)	A/D conversion value ch0[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
176	12	176	32-bit ring counter (2-phase multiple of 4) bit[16] (B1)	A/D conversion value ch1[0] (E0)
177		177	32-bit ring counter (2-phase multiple of 4) bit[17] (B1)	A/D conversion value ch1[1] (E0)
178		178	32-bit ring counter (2-phase multiple of 4) bit[18] (B1)	A/D conversion value ch1[2] (E0)
179		179	32-bit ring counter (2-phase multiple of 4) bit[19] (B1)	A/D conversion value ch1[3] (E0)
180		180	32-bit ring counter (2-phase multiple of 4) bit[20] (B1)	A/D conversion value ch1[4] (E0)
181		181	32-bit ring counter (2-phase multiple of 4) bit[21] (B1)	A/D conversion value ch1[5] (E0)
182		182	32-bit ring counter (2-phase multiple of 4) bit[22] (B1)	A/D conversion value ch1[6] (E0)
183		183	32-bit ring counter (2-phase multiple of 4) bit[23] (B1)	A/D conversion value ch1[7] (E0)
184		184	32-bit ring counter (2-phase multiple of 4) bit[24] (B1)	A/D conversion value ch1[8] (E0)
185		185	32-bit ring counter (2-phase multiple of 4) bit[25] (B1)	A/D conversion value ch1[9] (E0)
186		186	32-bit ring counter (2-phase multiple of 4) bit[26] (B1)	A/D conversion value ch1[10] (E0)
187		187	32-bit ring counter (2-phase multiple of 4) bit[27] (B1)	A/D conversion value ch1[11] (E0)
188		188	32-bit ring counter (2-phase multiple of 4) bit[28] (B1)	A/D conversion value ch1[12] (E0)
189		189	32-bit ring counter (2-phase multiple of 4) bit[29] (B1)	A/D conversion value ch1[13] (E0)
190		190	32-bit ring counter (2-phase multiple of 4) bit[30] (B1)	A/D conversion value ch1[14] (E0)
191		191	32-bit ring counter (2-phase multiple of 4) bit[31] (B1)	A/D conversion value ch1[15] (E0)
192	13	192	32-bit ring counter (2-phase multiple of 4) Phase A (B2)	A/D conversion value ch2[0] (E0)
193		193	32-bit ring counter (2-phase multiple of 4) Phase B (B2)	A/D conversion value ch2[1] (E0)
194		194	—	A/D conversion value ch2[2] (E0)
195		195	—	A/D conversion value ch2[3] (E0)
196		196	—	A/D conversion value ch2[4] (E0)
197		197	—	A/D conversion value ch2[5] (E0)
198		198	—	A/D conversion value ch2[6] (E0)
199		199	—	A/D conversion value ch2[7] (E0)
200		200	—	A/D conversion value ch2[8] (E0)
201		201	—	A/D conversion value ch2[9] (E0)
202		202	—	A/D conversion value ch2[10] (E0)
203		203	—	A/D conversion value ch2[11] (E0)
204		204	—	A/D conversion value ch2[12] (E0)
205		205	—	A/D conversion value ch2[13] (E0)
206		206	—	A/D conversion value ch2[14] (E0)
207		207	—	A/D conversion value ch2[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
208	14	208	32-bit ring counter (2-phase multiple of 4) bit[0] (B2)	A/D conversion value ch3[0] (E0)
209		209	32-bit ring counter (2-phase multiple of 4) bit[1] (B2)	A/D conversion value ch3[1] (E0)
210		210	32-bit ring counter (2-phase multiple of 4) bit[2] (B2)	A/D conversion value ch3[2] (E0)
211		211	32-bit ring counter (2-phase multiple of 4) bit[3] (B2)	A/D conversion value ch3[3] (E0)
212		212	32-bit ring counter (2-phase multiple of 4) bit[4] (B2)	A/D conversion value ch3[4] (E0)
213		213	32-bit ring counter (2-phase multiple of 4) bit[5] (B2)	A/D conversion value ch3[5] (E0)
214		214	32-bit ring counter (2-phase multiple of 4) bit[6] (B2)	A/D conversion value ch3[6] (E0)
215		215	32-bit ring counter (2-phase multiple of 4) bit[7] (B2)	A/D conversion value ch3[7] (E0)
216		216	32-bit ring counter (2-phase multiple of 4) bit[8] (B2)	A/D conversion value ch3[8] (E0)
217		217	32-bit ring counter (2-phase multiple of 4) bit[9] (B2)	A/D conversion value ch3[9] (E0)
218		218	32-bit ring counter (2-phase multiple of 4) bit[10] (B2)	A/D conversion value ch3[10] (E0)
219		219	32-bit ring counter (2-phase multiple of 4) bit[11] (B2)	A/D conversion value ch3[11] (E0)
220		220	32-bit ring counter (2-phase multiple of 4) bit[12] (B2)	A/D conversion value ch3[12] (E0)
221		221	32-bit ring counter (2-phase multiple of 4) bit[13] (B2)	A/D conversion value ch3[13] (E0)
222		222	32-bit ring counter (2-phase multiple of 4) bit[14] (B2)	A/D conversion value ch3[14] (E0)
223		223	32-bit ring counter (2-phase multiple of 4) bit[15] (B2)	A/D conversion value ch3[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
224	15	224	32-bit ring counter (2-phase multiple of 4) bit[16] (B2)	A/D conversion value ch4[0] (E0)
225		225	32-bit ring counter (2-phase multiple of 4) bit[17] (B2)	A/D conversion value ch4[1] (E0)
226		226	32-bit ring counter (2-phase multiple of 4) bit[18] (B2)	A/D conversion value ch4[2] (E0)
227		227	32-bit ring counter (2-phase multiple of 4) bit[19] (B2)	A/D conversion value ch4[3] (E0)
228		228	32-bit ring counter (2-phase multiple of 4) bit[20] (B2)	A/D conversion value ch4[4] (E0)
229		229	32-bit ring counter (2-phase multiple of 4) bit[21] (B2)	A/D conversion value ch4[5] (E0)
230		230	32-bit ring counter (2-phase multiple of 4) bit[22] (B2)	A/D conversion value ch4[6] (E0)
231		231	32-bit ring counter (2-phase multiple of 4) bit[23] (B2)	A/D conversion value ch4[7] (E0)
232		232	32-bit ring counter (2-phase multiple of 4) bit[24] (B2)	A/D conversion value ch4[8] (E0)
233		233	32-bit ring counter (2-phase multiple of 4) bit[25] (B2)	A/D conversion value ch4[9] (E0)
234		234	32-bit ring counter (2-phase multiple of 4) bit[26] (B2)	A/D conversion value ch4[10] (E0)
235		235	32-bit ring counter (2-phase multiple of 4) bit[27] (B2)	A/D conversion value ch4[11] (E0)
236		236	32-bit ring counter (2-phase multiple of 4) bit[28] (B2)	A/D conversion value ch4[12] (E0)
237		237	32-bit ring counter (2-phase multiple of 4) bit[29] (B2)	A/D conversion value ch4[13] (E0)
238		238	32-bit ring counter (2-phase multiple of 4) bit[30] (B2)	A/D conversion value ch4[14] (E0)
239		239	32-bit ring counter (2-phase multiple of 4) bit[31] (B2)	A/D conversion value ch4[15] (E0)
240	16	240	32-bit ring counter (2-phase multiple of 4) Phase A (E0)	A/D conversion value ch5[0] (E0)
241		241	32-bit ring counter (2-phase multiple of 4) Phase B (E0)	A/D conversion value ch5[1] (E0)
242		242	—	A/D conversion value ch5[2] (E0)
243		243	—	A/D conversion value ch5[3] (E0)
244		244	—	A/D conversion value ch5[4] (E0)
245		245	—	A/D conversion value ch5[5] (E0)
246		246	—	A/D conversion value ch5[6] (E0)
247		247	—	A/D conversion value ch5[7] (E0)
248		248	—	A/D conversion value ch5[8] (E0)
249		249	—	A/D conversion value ch5[9] (E0)
250		250	—	A/D conversion value ch5[10] (E0)
251		251	—	A/D conversion value ch5[11] (E0)
252		252	—	A/D conversion value ch5[12] (E0)
253		253	—	A/D conversion value ch5[13] (E0)
254		254	—	A/D conversion value ch5[14] (E0)
255		255	—	A/D conversion value ch5[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
256	17	256	32-bit ring counter (2-phase multiple of 4) bit[0] (E0)	A/D conversion value ch6[0] (E0)
257		257	32-bit ring counter (2-phase multiple of 4) bit[1] (E0)	A/D conversion value ch6[1] (E0)
258		258	32-bit ring counter (2-phase multiple of 4) bit[2] (E0)	A/D conversion value ch6[2] (E0)
259		259	32-bit ring counter (2-phase multiple of 4) bit[3] (E0)	A/D conversion value ch6[3] (E0)
260		260	32-bit ring counter (2-phase multiple of 4) bit[4] (E0)	A/D conversion value ch6[4] (E0)
261		261	32-bit ring counter (2-phase multiple of 4) bit[5] (E0)	A/D conversion value ch6[5] (E0)
262		262	32-bit ring counter (2-phase multiple of 4) bit[6] (E0)	A/D conversion value ch6[6] (E0)
263		263	32-bit ring counter (2-phase multiple of 4) bit[7] (E0)	A/D conversion value ch6[7] (E0)
246		246	32-bit ring counter (2-phase multiple of 4) bit[8] (E0)	A/D conversion value ch6[8] (E0)
265		265	32-bit ring counter (2-phase multiple of 4) bit[9] (E0)	A/D conversion value ch6[9] (E0)
266		266	32-bit ring counter (2-phase multiple of 4) bit[10] (E0)	A/D conversion value ch6[10] (E0)
267		267	32-bit ring counter (2-phase multiple of 4) bit[11] (E0)	A/D conversion value ch6[11] (E0)
268		268	32-bit ring counter (2-phase multiple of 4) bit[12] (E0)	A/D conversion value ch6[12] (E0)
269		269	32-bit ring counter (2-phase multiple of 4) bit[13] (E0)	A/D conversion value ch6[13] (E0)
270		270	32-bit ring counter (2-phase multiple of 4) bit[14] (E0)	A/D conversion value ch6[14] (E0)
271		271	32-bit ring counter (2-phase multiple of 4) bit[15] (E0)	A/D conversion value ch6[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
272	18	272	32-bit ring counter (2-phase multiple of 4) bit[16] (E0)	A/D conversion value ch7[0] (E0)
273		273	32-bit ring counter (2-phase multiple of 4) bit[17] (E0)	A/D conversion value ch7[1] (E0)
274		274	32-bit ring counter (2-phase multiple of 4) bit[18] (E0)	A/D conversion value ch7[2] (E0)
275		275	32-bit ring counter (2-phase multiple of 4) bit[19] (E0)	A/D conversion value ch7[3] (E0)
276		276	32-bit ring counter (2-phase multiple of 4) bit[20] (E0)	A/D conversion value ch7[4] (E0)
277		277	32-bit ring counter (2-phase multiple of 4) bit[21] (E0)	A/D conversion value ch7[5] (E0)
278		278	32-bit ring counter (2-phase multiple of 4) bit[22] (E0)	A/D conversion value ch7[6] (E0)
279		279	32-bit ring counter (2-phase multiple of 4) bit[23] (E0)	A/D conversion value ch7[7] (E0)
280		280	32-bit ring counter (2-phase multiple of 4) bit[24] (E0)	A/D conversion value ch7[8] (E0)
281		281	32-bit ring counter (2-phase multiple of 4) bit[25] (E0)	A/D conversion value ch7[9] (E0)
282		282	32-bit ring counter (2-phase multiple of 4) bit[26] (E0)	A/D conversion value ch7[10] (E0)
283		283	32-bit ring counter (2-phase multiple of 4) bit[27] (E0)	A/D conversion value ch7[11] (E0)
284		284	32-bit ring counter (2-phase multiple of 4) bit[28] (E0)	A/D conversion value ch7[12] (E0)
285		285	32-bit ring counter (2-phase multiple of 4) bit[29] (E0)	A/D conversion value ch7[13] (E0)
286		286	32-bit ring counter (2-phase multiple of 4) bit[30] (E0)	A/D conversion value ch7[14] (E0)
287		287	32-bit ring counter (2-phase multiple of 4) bit[31] (E0)	A/D conversion value ch7[15] (E0)
288	19	288	32-bit ring counter (2-phase multiple of 4) Phase A (E1)	A/D conversion value ch8[0] (E0)
289		289	32-bit ring counter (2-phase multiple of 4) Phase B (E1)	A/D conversion value ch8[1] (E0)
290		290	—	A/D conversion value ch8[2] (E0)
291		291	—	A/D conversion value ch8[3] (E0)
292		292	—	A/D conversion value ch8[4] (E0)
293		293	—	A/D conversion value ch8[5] (E0)
294		294	—	A/D conversion value ch8[6] (E0)
295		295	—	A/D conversion value ch8[7] (E0)
296		296	—	A/D conversion value ch8[8] (E0)
297		297	—	A/D conversion value ch8[9] (E0)
298		298	—	A/D conversion value ch8[10] (E0)
299		299	—	A/D conversion value ch8[11] (E0)
300		300	—	A/D conversion value ch8[12] (E0)
301		301	—	A/D conversion value ch8[13] (E0)
302		302	—	A/D conversion value ch8[14] (E0)
303		303	—	A/D conversion value ch8[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
304	20	304	32-bit ring counter (2-phase multiple of 4) bit[0] (E1)	A/D conversion value ch9[0] (E0)
305		305	32-bit ring counter (2-phase multiple of 4) bit[1] (E1)	A/D conversion value ch9[1] (E0)
306		306	32-bit ring counter (2-phase multiple of 4) bit[2] (E1)	A/D conversion value ch9[2] (E0)
307		307	32-bit ring counter (2-phase multiple of 4) bit[3] (E1)	A/D conversion value ch9[3] (E0)
308		308	32-bit ring counter (2-phase multiple of 4) bit[4] (E1)	A/D conversion value ch9[4] (E0)
309		309	32-bit ring counter (2-phase multiple of 4) bit[5] (E1)	A/D conversion value ch9[5] (E0)
310		310	32-bit ring counter (2-phase multiple of 4) bit[6] (E1)	A/D conversion value ch9[6] (E0)
311		311	32-bit ring counter (2-phase multiple of 4) bit[7] (E1)	A/D conversion value ch9[7] (E0)
312		312	32-bit ring counter (2-phase multiple of 4) bit[8] (E1)	A/D conversion value ch9[8] (E0)
313		313	32-bit ring counter (2-phase multiple of 4) bit[9] (E1)	A/D conversion value ch9[9] (E0)
314		314	32-bit ring counter (2-phase multiple of 4) bit[10] (E1)	A/D conversion value ch9[10] (E0)
315		315	32-bit ring counter (2-phase multiple of 4) bit[11] (E1)	A/D conversion value ch9[11] (E0)
316		316	32-bit ring counter (2-phase multiple of 4) bit[12] (E1)	A/D conversion value ch9[12] (E0)
317		317	32-bit ring counter (2-phase multiple of 4) bit[13] (E1)	A/D conversion value ch9[13] (E0)
318		318	32-bit ring counter (2-phase multiple of 4) bit[14] (E1)	A/D conversion value ch9[14] (E0)
319		319	32-bit ring counter (2-phase multiple of 4) bit[15] (E1)	A/D conversion value ch9[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
320	21	320	32-bit ring counter (2-phase multiple of 4) bit[16] (E1)	A/D conversion value chA[0] (E0)
321		321	32-bit ring counter (2-phase multiple of 4) bit[17] (E1)	A/D conversion value chA[1] (E0)
322		322	32-bit ring counter (2-phase multiple of 4) bit[18] (E1)	A/D conversion value chA[2] (E0)
323		323	32-bit ring counter (2-phase multiple of 4) bit[19] (E1)	A/D conversion value chA[3] (E0)
324		324	32-bit ring counter (2-phase multiple of 4) bit[20] (E1)	A/D conversion value chA[4] (E0)
325		325	32-bit ring counter (2-phase multiple of 4) bit[21] (E1)	A/D conversion value chA[5] (E0)
326		326	32-bit ring counter (2-phase multiple of 4) bit[22] (E1)	A/D conversion value chA[6] (E0)
327		327	32-bit ring counter (2-phase multiple of 4) bit[23] (E1)	A/D conversion value chA[7] (E0)
328		328	32-bit ring counter (2-phase multiple of 4) bit[24] (E1)	A/D conversion value chA[8] (E0)
329		329	32-bit ring counter (2-phase multiple of 4) bit[25] (E1)	A/D conversion value chA[9] (E0)
330		330	32-bit ring counter (2-phase multiple of 4) bit[26] (E1)	A/D conversion value chA[10] (E0)
331		331	32-bit ring counter (2-phase multiple of 4) bit[27] (E1)	A/D conversion value chA[11] (E0)
332		332	32-bit ring counter (2-phase multiple of 4) bit[28] (E1)	A/D conversion value chA[12] (E0)
333		333	32-bit ring counter (2-phase multiple of 4) bit[29] (E1)	A/D conversion value chA[13] (E0)
334		334	32-bit ring counter (2-phase multiple of 4) bit[30] (E1)	A/D conversion value chA[14] (E0)
335		335	32-bit ring counter (2-phase multiple of 4) bit[31] (E1)	A/D conversion value chA[15] (E0)
336	22	336	32-bit ring counter (2-phase multiple of 4) Phase A (E2)	A/D conversion value chB[0] (E0)
337		337	32-bit ring counter (2-phase multiple of 4) Phase B (E2)	A/D conversion value chB[1] (E0)
338		338	—	A/D conversion value chB[2] (E0)
339		339	—	A/D conversion value chB[3] (E0)
340		340	—	A/D conversion value chB[4] (E0)
341		341	—	A/D conversion value chB[5] (E0)
342		342	—	A/D conversion value chB[6] (E0)
343		343	—	A/D conversion value chB[7] (E0)
344		344	—	A/D conversion value chB[8] (E0)
345		345	—	A/D conversion value chB[9] (E0)
346		346	—	A/D conversion value chB[10] (E0)
347		347	—	A/D conversion value chB[11] (E0)
348		348	—	A/D conversion value chB[12] (E0)
349		349	—	A/D conversion value chB[13] (E0)
350		350	—	A/D conversion value chB[14] (E0)
351		351	—	A/D conversion value chB[15] (E0)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
352	23	352	32-bit ring counter (2-phase multiple of 4) bit[0] (E2)	—
353		353	32-bit ring counter (2-phase multiple of 4) bit[1] (E2)	—
354		354	32-bit ring counter (2-phase multiple of 4) bit[2] (E2)	—
355		355	32-bit ring counter (2-phase multiple of 4) bit[3] (E2)	—
356		356	32-bit ring counter (2-phase multiple of 4) bit[4] (E2)	—
357		357	32-bit ring counter (2-phase multiple of 4) bit[5] (E2)	—
358		358	32-bit ring counter (2-phase multiple of 4) bit[6] (E2)	—
359		359	32-bit ring counter (2-phase multiple of 4) bit[7] (E2)	—
360		360	32-bit ring counter (2-phase multiple of 4) bit[8] (E2)	—
361		361	32-bit ring counter (2-phase multiple of 4) bit[9] (E2)	—
362		362	32-bit ring counter (2-phase multiple of 4) bit[10] (E2)	—
363		363	32-bit ring counter (2-phase multiple of 4) bit[11] (E2)	—
364		364	32-bit ring counter (2-phase multiple of 4) bit[12] (E2)	—
365		365	32-bit ring counter (2-phase multiple of 4) bit[13] (E2)	—
366		366	32-bit ring counter (2-phase multiple of 4) bit[14] (E2)	—
367		367	32-bit ring counter (2-phase multiple of 4) bit[15] (E2)	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
368	24	368	32-bit ring counter (2-phase multiple of 4) bit[16] (E2)	—
369		369	32-bit ring counter (2-phase multiple of 4) bit[17] (E2)	—
370		370	32-bit ring counter (2-phase multiple of 4) bit[18] (E2)	—
371		371	32-bit ring counter (2-phase multiple of 4) bit[19] (E2)	—
372		372	32-bit ring counter (2-phase multiple of 4) bit[20] (E2)	—
373		373	32-bit ring counter (2-phase multiple of 4) bit[21] (E2)	—
374		374	32-bit ring counter (2-phase multiple of 4) bit[22] (E2)	—
375		375	32-bit ring counter (2-phase multiple of 4) bit[23] (E2)	—
376		376	32-bit ring counter (2-phase multiple of 4) bit[24] (E2)	—
377		377	32-bit ring counter (2-phase multiple of 4) bit[25] (E2)	—
378		378	32-bit ring counter (2-phase multiple of 4) bit[26] (E2)	—
379		379	32-bit ring counter (2-phase multiple of 4) bit[27] (E2)	—
380		380	32-bit ring counter (2-phase multiple of 4) bit[28] (E2)	—
381		381	32-bit ring counter (2-phase multiple of 4) bit[29] (E2)	—
382		382	32-bit ring counter (2-phase multiple of 4) bit[30] (E2)	—
383		383	32-bit ring counter (2-phase multiple of 4) bit[31] (E2)	—
384	25	384	—	—
385		385	—	—
386		386	—	—
387		387	—	—
388		388	—	—
389		389	—	—
390		390	—	—
391		391	—	—
392		392	—	—
393		393	—	—
394		394	—	—
395		395	—	—
396		396	—	—
397		397	—	—
398		398	—	—
399		399	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
400	26	400	—	—
401		401	—	—
402		402	—	—
403		403	—	—
404		404	—	—
405		405	—	—
406		406	—	—
407		407	—	—
408		408	—	—
409		409	—	—
410		410	—	—
411		411	—	—
412		412	—	—
413		413	—	—
414		414	—	—
415		415	—	—
416	27	416	—	—
417		417	—	—
418		418	—	—
419		419	—	—
420		420	—	—
421		421	—	—
422		422	—	—
423		423	—	—
424		424	—	—
425		425	—	—
426		426	—	—
427		427	—	—
428		428	—	—
429		429	—	—
430		430	—	—
431		431	—	—
432	28	—	Time information [0] (μs)	Time information [0] (μs)
433		—	Time information [1] (μs)	Time information [1] (μs)
434		—	Time information [2] (μs)	Time information [2] (μs)
435		—	Time information [3] (μs)	Time information [3] (μs)
436		—	Time information [4] (μs)	Time information [4] (μs)
437		—	Time information [5] (μs)	Time information [5] (μs)
438		—	Time information [6] (μs)	Time information [6] (μs)
439		—	Time information [7] (μs)	Time information [7] (μs)
440		—	Time information [8] (μs)	Time information [8] (μs)
441		—	Time information [9] (μs)	Time information [9] (μs)
442		—	—	—
443		—	—	—
444		—	—	—
445		—	—	—
446		—	—	—
447		—	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
448	29	—	Time information [0] (ms)	Time information [0] (ms)
449		—	Time information [1] (ms)	Time information [1] (ms)
450		—	Time information [2] (ms)	Time information [2] (ms)
451		—	Time information [3] (ms)	Time information [3] (ms)
452		—	Time information [4] (ms)	Time information [4] (ms)
453		—	Time information [5] (ms)	Time information [5] (ms)
454		—	Time information [6] (ms)	Time information [6] (ms)
455		—	Time information [7] (ms)	Time information [7] (ms)
456		—	Time information [8] (ms)	Time information [8] (ms)
457		—	Time information [9] (ms)	Time information [9] (ms)
458		—	—	—
459		—	—	—
460		—	—	—
461		—	—	—
462		—	—	—
463		—	—	—
464	30	—	Time information [0] (seconds)	Time information [0] (seconds)
465		—	Time information [1] (seconds)	Time information [1] (seconds)
466		—	Time information [2] (seconds)	Time information [2] (seconds)
467		—	Time information [3] (seconds)	Time information [3] (seconds)
468		—	Time information [4] (seconds)	Time information [4] (seconds)
469		—	Time information [5] (seconds)	Time information [5] (seconds)
470		—	Time information [0] (minutes)	Time information [0] (minutes)
471		—	Time information [1] (minutes)	Time information [1] (minutes)
472		—	Time information [2] (minutes)	Time information [2] (minutes)
473		—	Time information [3] (minutes)	Time information [3] (minutes)
474		—	Time information [4] (minutes)	Time information [4] (minutes)
475		—	Time information [5] (minutes)	Time information [5] (minutes)
476		—	—	—
477		—	—	—
478		—	—	—
479		—	—	—
480	31	—	Time information [0] (hour)	Time information [0] (hour)
481		—	Time information [1] (hour)	Time information [1] (hour)
482		—	Time information [2] (hour)	Time information [2] (hour)
483		—	Time information [3] (hour)	Time information [3] (hour)
484		—	Time information [4] (hour)	Time information [4] (hour)
485		—	Time information [0] (day)	Time information [0] (day)
486		—	Time information [1] (day)	Time information [1] (day)
487		—	Time information [2] (day)	Time information [2] (day)
488		—	Time information [3] (day)	Time information [3] (day)
489		—	Time information [4] (day)	Time information [4] (day)
490		—	Time information [0] (month)	Time information [0] (month)
491		—	Time information [1] (month)	Time information [1] (month)
492		—	Time information [2] (month)	Time information [2] (month)
493		—	Time information [3] (month)	Time information [3] (month)
494		—	—	—
495		—	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
496	32	—	Time information [0] (year)	Time information [0] (year)
497		—	Time information [1] (year)	Time information [1] (year)
498		—	Time information [2] (year)	Time information [2] (year)
499		—	Time information [3] (year)	Time information [3] (year)
500		—	Time information [4] (year)	Time information [4] (year)
501		—	Time information [5] (year)	Time information [5] (year)
502		—	Time information [6] (year)	Time information [6] (year)
503		—	—	—
504		—	—	—
505		—	—	—
506		—	—	—
507		—	—	—
508		—	—	—
509		—	—	—
510		—	—	—
511		—	—	—
512	33	0	—	A/D conversion value ch0[0] (E1)
513		1	—	A/D conversion value ch0[1] (E1)
514		2	—	A/D conversion value ch0[2] (E1)
515		3	—	A/D conversion value ch0[3] (E1)
516		4	—	A/D conversion value ch0[4] (E1)
517		5	—	A/D conversion value ch0[5] (E1)
518		6	—	A/D conversion value ch0[6] (E1)
519		7	—	A/D conversion value ch0[7] (E1)
520		8	—	A/D conversion value ch0[8] (E1)
521		9	—	A/D conversion value ch0[9] (E1)
522		10	—	A/D conversion value ch0[10] (E1)
523		11	—	A/D conversion value ch0[11] (E1)
524		12	—	A/D conversion value ch0[12] (E1)
525		13	—	A/D conversion value ch0[13] (E1)
526		14	—	A/D conversion value ch0[14] (E1)
527		15	—	A/D conversion value ch0[15] (E1)
528	34	16	—	A/D conversion value ch1[0] (E1)
529		17	—	A/D conversion value ch1[1] (E1)
530		18	—	A/D conversion value ch1[2] (E1)
531		19	—	A/D conversion value ch1[3] (E1)
532		20	—	A/D conversion value ch1[4] (E1)
533		21	—	A/D conversion value ch1[5] (E1)
534		22	—	A/D conversion value ch1[6] (E1)
535		23	—	A/D conversion value ch1[7] (E1)
536		24	—	A/D conversion value ch1[8] (E1)
537		25	—	A/D conversion value ch1[9] (E1)
538		26	—	A/D conversion value ch1[10] (E1)
539		27	—	A/D conversion value ch1[11] (E1)
540		28	—	A/D conversion value ch1[12] (E1)
541		29	—	A/D conversion value ch1[13] (E1)
542		30	—	A/D conversion value ch1[14] (E1)
543		31	—	A/D conversion value ch1[15] (E1)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
544	35	32	—	A/D conversion value ch2[0] (E1)
545		33	—	A/D conversion value ch2[1] (E1)
546		34	—	A/D conversion value ch2[2] (E1)
547		35	—	A/D conversion value ch2[3] (E1)
548		36	—	A/D conversion value ch2[4] (E1)
549		37	—	A/D conversion value ch2[5] (E1)
550		38	—	A/D conversion value ch2[6] (E1)
551		39	—	A/D conversion value ch2[7] (E1)
552		40	—	A/D conversion value ch2[8] (E1)
553		41	—	A/D conversion value ch2[9] (E1)
554		42	—	A/D conversion value ch2[10] (E1)
555		43	—	A/D conversion value ch2[11] (E1)
556		44	—	A/D conversion value ch2[12] (E1)
557		45	—	A/D conversion value ch2[13] (E1)
558		46	—	A/D conversion value ch2[14] (E1)
559		47	—	A/D conversion value ch2[15] (E1)
560	36	48	—	A/D conversion value ch3[0] (E1)
561		49	—	A/D conversion value ch3[1] (E1)
562		50	—	A/D conversion value ch3[2] (E1)
563		51	—	A/D conversion value ch3[3] (E1)
564		52	—	A/D conversion value ch3[4] (E1)
565		53	—	A/D conversion value ch3[5] (E1)
566		54	—	A/D conversion value ch3[6] (E1)
567		55	—	A/D conversion value ch3[7] (E1)
568		56	—	A/D conversion value ch3[8] (E1)
569		57	—	A/D conversion value ch3[9] (E1)
570		58	—	A/D conversion value ch3[10] (E1)
571		59	—	A/D conversion value ch3[11] (E1)
572		60	—	A/D conversion value ch3[12] (E1)
573		61	—	A/D conversion value ch3[13] (E1)
574		62	—	A/D conversion value ch3[14] (E1)
575		63	—	A/D conversion value ch3[15] (E1)
576	37	64	—	A/D conversion value ch4[0] (E1)
577		65	—	A/D conversion value ch4[1] (E1)
578		66	—	A/D conversion value ch4[2] (E1)
579		67	—	A/D conversion value ch4[3] (E1)
580		68	—	A/D conversion value ch4[4] (E1)
581		69	—	A/D conversion value ch4[5] (E1)
582		70	—	A/D conversion value ch4[6] (E1)
583		71	—	A/D conversion value ch4[7] (E1)
584		72	—	A/D conversion value ch4[8] (E1)
585		73	—	A/D conversion value ch4[9] (E1)
586		74	—	A/D conversion value ch4[10] (E1)
587		75	—	A/D conversion value ch4[11] (E1)
588		76	—	A/D conversion value ch4[12] (E1)
589		77	—	A/D conversion value ch4[13] (E1)
590		78	—	A/D conversion value ch4[14] (E1)
591		79	—	A/D conversion value ch4[15] (E1)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
592	38	80	—	A/D conversion value ch5[0] (E1)
593		81	—	A/D conversion value ch5[1] (E1)
594		82	—	A/D conversion value ch5[2] (E1)
595		83	—	A/D conversion value ch5[3] (E1)
596		84	—	A/D conversion value ch5[4] (E1)
597		85	—	A/D conversion value ch5[5] (E1)
598		86	—	A/D conversion value ch5[6] (E1)
599		87	—	A/D conversion value ch5[7] (E1)
600		88	—	A/D conversion value ch5[8] (E1)
601		89	—	A/D conversion value ch5[9] (E1)
602		90	—	A/D conversion value ch5[10] (E1)
603		91	—	A/D conversion value ch5[11] (E1)
604		92	—	A/D conversion value ch5[12] (E1)
605		93	—	A/D conversion value ch5[13] (E1)
606		94	—	A/D conversion value ch5[14] (E1)
607		95	—	A/D conversion value ch5[15] (E1)
608	39	96	—	A/D conversion value ch6[0] (E1)
609		97	—	A/D conversion value ch6[1] (E1)
610		98	—	A/D conversion value ch6[2] (E1)
611		99	—	A/D conversion value ch6[3] (E1)
612		100	—	A/D conversion value ch6[4] (E1)
613		101	—	A/D conversion value ch6[5] (E1)
614		102	—	A/D conversion value ch6[6] (E1)
615		103	—	A/D conversion value ch6[7] (E1)
616		104	—	A/D conversion value ch6[8] (E1)
617		105	—	A/D conversion value ch6[9] (E1)
618		106	—	A/D conversion value ch6[10] (E1)
619		107	—	A/D conversion value ch6[11] (E1)
620		108	—	A/D conversion value ch6[12] (E1)
621		109	—	A/D conversion value ch6[13] (E1)
622		110	—	A/D conversion value ch6[14] (E1)
623		111	—	A/D conversion value ch6[15] (E1)
624	40	112	—	A/D conversion value ch7[0] (E1)
625		113	—	A/D conversion value ch7[1] (E1)
626		114	—	A/D conversion value ch7[2] (E1)
627		115	—	A/D conversion value ch7[3] (E1)
628		116	—	A/D conversion value ch7[4] (E1)
629		117	—	A/D conversion value ch7[5] (E1)
630		118	—	A/D conversion value ch7[6] (E1)
631		119	—	A/D conversion value ch7[7] (E1)
632		120	—	A/D conversion value ch7[8] (E1)
633		121	—	A/D conversion value ch7[9] (E1)
634		122	—	A/D conversion value ch7[10] (E1)
635		123	—	A/D conversion value ch7[11] (E1)
636		124	—	A/D conversion value ch7[12] (E1)
637		125	—	A/D conversion value ch7[13] (E1)
638		126	—	A/D conversion value ch7[14] (E1)
639		127	—	A/D conversion value ch7[15] (E1)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
640	41	128	—	A/D conversion value ch8[0] (E1)
641		129	—	A/D conversion value ch8[1] (E1)
642		130	—	A/D conversion value ch8[2] (E1)
643		131	—	A/D conversion value ch8[3] (E1)
644		132	—	A/D conversion value ch8[4] (E1)
645		133	—	A/D conversion value ch8[5] (E1)
646		134	—	A/D conversion value ch8[6] (E1)
647		135	—	A/D conversion value ch8[7] (E1)
648		136	—	A/D conversion value ch8[8] (E1)
649		137	—	A/D conversion value ch8[9] (E1)
650		138	—	A/D conversion value ch8[10] (E1)
651		139	—	A/D conversion value ch8[11] (E1)
652		140	—	A/D conversion value ch8[12] (E1)
653		141	—	A/D conversion value ch8[13] (E1)
654		142	—	A/D conversion value ch8[14] (E1)
655		143	—	A/D conversion value ch8[15] (E1)
656	42	144	—	A/D conversion value ch9[0] (E1)
657		145	—	A/D conversion value ch9[1] (E1)
658		146	—	A/D conversion value ch9[2] (E1)
659		147	—	A/D conversion value ch9[3] (E1)
660		148	—	A/D conversion value ch9[4] (E1)
661		149	—	A/D conversion value ch9[5] (E1)
662		150	—	A/D conversion value ch9[6] (E1)
663		151	—	A/D conversion value ch9[7] (E1)
664		152	—	A/D conversion value ch9[8] (E1)
665		153	—	A/D conversion value ch9[9] (E1)
666		154	—	A/D conversion value ch9[10] (E1)
667		155	—	A/D conversion value ch9[11] (E1)
668		156	—	A/D conversion value ch9[12] (E1)
669		157	—	A/D conversion value ch9[13] (E1)
670		158	—	A/D conversion value ch9[14] (E1)
671		159	—	A/D conversion value ch9[15] (E1)
672	43	160	—	A/D conversion value chA[0] (E1)
673		161	—	A/D conversion value chA[1] (E1)
674		162	—	A/D conversion value chA[2] (E1)
675		163	—	A/D conversion value chA[3] (E1)
676		164	—	A/D conversion value chA[4] (E1)
677		165	—	A/D conversion value chA[5] (E1)
678		166	—	A/D conversion value chA[6] (E1)
679		167	—	A/D conversion value chA[7] (E1)
680		168	—	A/D conversion value chA[8] (E1)
681		169	—	A/D conversion value chA[9] (E1)
682		170	—	A/D conversion value chA[10] (E1)
683		171	—	A/D conversion value chA[11] (E1)
684		172	—	A/D conversion value chA[12] (E1)
685		173	—	A/D conversion value chA[13] (E1)
686		174	—	A/D conversion value chA[14] (E1)
687		175	—	A/D conversion value chA[15] (E1)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
688	44	176	—	A/D conversion value chB[0] (E1)
689		177	—	A/D conversion value chB[1] (E1)
690		178	—	A/D conversion value chB[2] (E1)
691		179	—	A/D conversion value chB[3] (E1)
692		180	—	A/D conversion value chB[4] (E1)
693		181	—	A/D conversion value chB[5] (E1)
694		182	—	A/D conversion value chB[6] (E1)
695		183	—	A/D conversion value chB[7] (E1)
696		184	—	A/D conversion value chB[8] (E1)
697		185	—	A/D conversion value chB[9] (E1)
698		186	—	A/D conversion value chB[10] (E1)
699		187	—	A/D conversion value chB[11] (E1)
700		188	—	A/D conversion value chB[12] (E1)
701		189	—	A/D conversion value chB[13] (E1)
702		190	—	A/D conversion value chB[14] (E1)
703		191	—	A/D conversion value chB[15] (E1)
704	45	192	—	A/D conversion value ch0[0] (E2)
705		193	—	A/D conversion value ch0[1] (E2)
706		194	—	A/D conversion value ch0[2] (E2)
707		195	—	A/D conversion value ch0[3] (E2)
708		196	—	A/D conversion value ch0[4] (E2)
709		197	—	A/D conversion value ch0[5] (E2)
710		198	—	A/D conversion value ch0[6] (E2)
711		199	—	A/D conversion value ch0[7] (E2)
712		200	—	A/D conversion value ch0[8] (E2)
713		201	—	A/D conversion value ch0[9] (E2)
714		202	—	A/D conversion value ch0[10] (E2)
715		203	—	A/D conversion value ch0[11] (E2)
716		204	—	A/D conversion value ch0[12] (E2)
717		205	—	A/D conversion value ch0[13] (E2)
718		206	—	A/D conversion value ch0[14] (E2)
719		207	—	A/D conversion value ch0[15] (E2)
720	46	208	—	A/D conversion value ch1[0] (E2)
721		209	—	A/D conversion value ch1[1] (E2)
722		210	—	A/D conversion value ch1[2] (E2)
723		211	—	A/D conversion value ch1[3] (E2)
724		212	—	A/D conversion value ch1[4] (E2)
725		213	—	A/D conversion value ch1[5] (E2)
726		214	—	A/D conversion value ch1[6] (E2)
727		215	—	A/D conversion value ch1[7] (E2)
728		216	—	A/D conversion value ch1[8] (E2)
729		217	—	A/D conversion value ch1[9] (E2)
730		218	—	A/D conversion value ch1[10] (E2)
731		219	—	A/D conversion value ch1[11] (E2)
732		220	—	A/D conversion value ch1[12] (E2)
733		221	—	A/D conversion value ch1[13] (E2)
734		222	—	A/D conversion value ch1[14] (E2)
735		223	—	A/D conversion value ch1[15] (E2)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
736	47	224	—	A/D conversion value ch2[0] (E2)
737		225	—	A/D conversion value ch2[1] (E2)
738		226	—	A/D conversion value ch2[2] (E2)
739		227	—	A/D conversion value ch2[3] (E2)
740		228	—	A/D conversion value ch2[4] (E2)
741		229	—	A/D conversion value ch2[5] (E2)
742		230	—	A/D conversion value ch2[6] (E2)
743		231	—	A/D conversion value ch2[7] (E2)
744		232	—	A/D conversion value ch2[8] (E2)
745		233	—	A/D conversion value ch2[9] (E2)
746		234	—	A/D conversion value ch2[10] (E2)
747		235	—	A/D conversion value ch2[11] (E2)
748		236	—	A/D conversion value ch2[12] (E2)
749		237	—	A/D conversion value ch2[13] (E2)
750		238	—	A/D conversion value ch2[14] (E2)
751		239	—	A/D conversion value ch2[15] (E2)
752	48	240	—	A/D conversion value ch3[0] (E2)
753		241	—	A/D conversion value ch3[1] (E2)
754		242	—	A/D conversion value ch3[2] (E2)
755		243	—	A/D conversion value ch3[3] (E2)
756		244	—	A/D conversion value ch3[4] (E2)
757		245	—	A/D conversion value ch3[5] (E2)
758		246	—	A/D conversion value ch3[6] (E2)
759		247	—	A/D conversion value ch3[7] (E2)
760		248	—	A/D conversion value ch3[8] (E2)
761		249	—	A/D conversion value ch3[9] (E2)
762		250	—	A/D conversion value ch3[10] (E2)
763		251	—	A/D conversion value ch3[11] (E2)
764		252	—	A/D conversion value ch3[12] (E2)
765		253	—	A/D conversion value ch3[13] (E2)
766		254	—	A/D conversion value ch3[14] (E2)
767		255	—	A/D conversion value ch3[15] (E2)
768	49	256	—	A/D conversion value ch4[0] (E2)
769		257	—	A/D conversion value ch4[1] (E2)
770		258	—	A/D conversion value ch4[2] (E2)
771		259	—	A/D conversion value ch4[3] (E2)
772		260	—	A/D conversion value ch4[4] (E2)
773		261	—	A/D conversion value ch4[5] (E2)
774		262	—	A/D conversion value ch4[6] (E2)
775		263	—	A/D conversion value ch4[7] (E2)
776		264	—	A/D conversion value ch4[8] (E2)
777		265	—	A/D conversion value ch4[9] (E2)
778		266	—	A/D conversion value ch4[10] (E2)
779		267	—	A/D conversion value ch4[11] (E2)
780		268	—	A/D conversion value ch4[12] (E2)
781		269	—	A/D conversion value ch4[13] (E2)
782		270	—	A/D conversion value ch4[14] (E2)
783		271	—	A/D conversion value ch4[15] (E2)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
784	50	272	—	A/D conversion value ch5[0] (E2)
785		273	—	A/D conversion value ch5[1] (E2)
786		274	—	A/D conversion value ch5[2] (E2)
787		275	—	A/D conversion value ch5[3] (E2)
788		276	—	A/D conversion value ch5[4] (E2)
789		277	—	A/D conversion value ch5[5] (E2)
790		278	—	A/D conversion value ch5[6] (E2)
791		279	—	A/D conversion value ch5[7] (E2)
792		280	—	A/D conversion value ch5[8] (E2)
793		281	—	A/D conversion value ch5[9] (E2)
794		282	—	A/D conversion value ch5[10] (E2)
795		283	—	A/D conversion value ch5[11] (E2)
796		284	—	A/D conversion value ch5[12] (E2)
797		285	—	A/D conversion value ch5[13] (E2)
798		286	—	A/D conversion value ch5[14] (E2)
799		287	—	A/D conversion value ch5[15] (E2)
800	51	288	—	A/D conversion value ch6[0] (E2)
801		289	—	A/D conversion value ch6[1] (E2)
802		290	—	A/D conversion value ch6[2] (E2)
803		291	—	A/D conversion value ch6[3] (E2)
804		292	—	A/D conversion value ch6[4] (E2)
805		293	—	A/D conversion value ch6[5] (E2)
806		294	—	A/D conversion value ch6[6] (E2)
807		295	—	A/D conversion value ch6[7] (E2)
808		296	—	A/D conversion value ch6[8] (E2)
809		297	—	A/D conversion value ch6[9] (E2)
810		298	—	A/D conversion value ch6[10] (E2)
811		299	—	A/D conversion value ch6[11] (E2)
812		300	—	A/D conversion value ch6[12] (E2)
813		301	—	A/D conversion value ch6[13] (E2)
814		302	—	A/D conversion value ch6[14] (E2)
815		303	—	A/D conversion value ch6[15] (E2)
816	52	304	—	A/D conversion value ch7[0] (E2)
817		305	—	A/D conversion value ch7[1] (E2)
818		306	—	A/D conversion value ch7[2] (E2)
819		307	—	A/D conversion value ch7[3] (E2)
820		308	—	A/D conversion value ch7[4] (E2)
821		309	—	A/D conversion value ch7[5] (E2)
822		310	—	A/D conversion value ch7[6] (E2)
823		311	—	A/D conversion value ch7[7] (E2)
824		312	—	A/D conversion value ch7[8] (E2)
825		313	—	A/D conversion value ch7[9] (E2)
826		314	—	A/D conversion value ch7[10] (E2)
827		315	—	A/D conversion value ch7[11] (E2)
828		316	—	A/D conversion value ch7[12] (E2)
829		317	—	A/D conversion value ch7[13] (E2)
830		318	—	A/D conversion value ch7[14] (E2)
831		319	—	A/D conversion value ch7[15] (E2)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
832	53	320	—	A/D conversion value ch8[0] (E2)
833		321	—	A/D conversion value ch8[1] (E2)
834		322	—	A/D conversion value ch8[2] (E2)
835		323	—	A/D conversion value ch8[3] (E2)
836		324	—	A/D conversion value ch8[4] (E2)
837		325	—	A/D conversion value ch8[5] (E2)
838		326	—	A/D conversion value ch8[6] (E2)
839		327	—	A/D conversion value ch8[7] (E2)
840		328	—	A/D conversion value ch8[8] (E2)
841		329	—	A/D conversion value ch8[9] (E2)
842		330	—	A/D conversion value ch8[10] (E2)
843		331	—	A/D conversion value ch8[11] (E2)
844		332	—	A/D conversion value ch8[12] (E2)
845		333	—	A/D conversion value ch8[13] (E2)
846		334	—	A/D conversion value ch8[14] (E2)
847		335	—	A/D conversion value ch8[15] (E2)
848	54	336	—	A/D conversion value ch9[0] (E2)
849		337	—	A/D conversion value ch9[1] (E2)
850		338	—	A/D conversion value ch9[2] (E2)
851		339	—	A/D conversion value ch9[3] (E2)
852		340	—	A/D conversion value ch9[4] (E2)
853		341	—	A/D conversion value ch9[5] (E2)
854		342	—	A/D conversion value ch9[6] (E2)
855		343	—	A/D conversion value ch9[7] (E2)
856		344	—	A/D conversion value ch9[8] (E2)
857		345	—	A/D conversion value ch9[9] (E2)
858		346	—	A/D conversion value ch9[10] (E2)
859		347	—	A/D conversion value ch9[11] (E2)
860		348	—	A/D conversion value ch9[12] (E2)
861		349	—	A/D conversion value ch9[13] (E2)
862		350	—	A/D conversion value ch9[14] (E2)
863		351	—	A/D conversion value ch9[15] (E2)
864	55	352	—	A/D conversion value chA[0] (E2)
865		353	—	A/D conversion value chA[1] (E2)
866		354	—	A/D conversion value chA[2] (E2)
867		355	—	A/D conversion value chA[3] (E2)
868		356	—	A/D conversion value chA[4] (E2)
869		357	—	A/D conversion value chA[5] (E2)
870		358	—	A/D conversion value chA[6] (E2)
871		359	—	A/D conversion value chA[7] (E2)
872		360	—	A/D conversion value chA[8] (E2)
873		361	—	A/D conversion value chA[9] (E2)
874		362	—	A/D conversion value chA[10] (E2)
875		363	—	A/D conversion value chA[11] (E2)
876		364	—	A/D conversion value chA[12] (E2)
877		365	—	A/D conversion value chA[13] (E2)
878		366	—	A/D conversion value chA[14] (E2)
879		367	—	A/D conversion value chA[15] (E2)

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
880	56	368	—	A/D conversion value chB[0] (E2)
881		369	—	A/D conversion value chB[1] (E2)
882		370	—	A/D conversion value chB[2] (E2)
883		371	—	A/D conversion value chB[3] (E2)
884		372	—	A/D conversion value chB[4] (E2)
885		373	—	A/D conversion value chB[5] (E2)
886		374	—	A/D conversion value chB[6] (E2)
887		375	—	A/D conversion value chB[7] (E2)
888		376	—	A/D conversion value chB[8] (E2)
889		377	—	A/D conversion value chB[9] (E2)
890		378	—	A/D conversion value chB[10] (E2)
891		379	—	A/D conversion value chB[11] (E2)
892		380	—	A/D conversion value chB[12] (E2)
893		381	—	A/D conversion value chB[13] (E2)
894		382	—	A/D conversion value chB[14] (E2)
895		383	—	A/D conversion value chB[15] (E2)
896	57	384	—	—
897		385	—	—
898		386	—	—
899		387	—	—
900		388	—	—
901		389	—	—
902		390	—	—
903		391	—	—
904		392	—	—
905		393	—	—
906		394	—	—
907		395	—	—
908		396	—	—
909		397	—	—
910		398	—	—
911		399	—	—
912	58	400	—	—
913		401	—	—
914		402	—	—
915		403	—	—
916		404	—	—
917		405	—	—
918		406	—	—
919		407	—	—
920		408	—	—
921		409	—	—
922		410	—	—
923		411	—	—
924		412	—	—
925		413	—	—
926		414	—	—
927		415	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
928	59	416	—	—
929		417	—	—
930		418	—	—
931		419	—	—
932		420	—	—
933		421	—	—
934		422	—	—
935		423	—	—
936		424	—	—
937		425	—	—
938		426	—	—
939		427	—	—
940		428	—	—
941		429	—	—
942		430	—	—
943		431	—	—
944	60	—	Time information [0] (μs)	Time information [0] (μs)
945		—	Time information [1] (μs)	Time information [1] (μs)
946		—	Time information [2] (μs)	Time information [2] (μs)
947		—	Time information [3] (μs)	Time information [3] (μs)
948		—	Time information [4] (μs)	Time information [4] (μs)
949		—	Time information [5] (μs)	Time information [5] (μs)
950		—	Time information [6] (μs)	Time information [6] (μs)
951		—	Time information [7] (μs)	Time information [7] (μs)
952		—	Time information [8] (μs)	Time information [8] (μs)
953		—	Time information [9] (μs)	Time information [9] (μs)
954		—	—	—
955		—	—	—
956		—	—	—
957		—	—	—
958		—	—	—
959		—	—	—
960	61	—	Time information [0] (ms)	Time information [0] (ms)
961		—	Time information [1] (ms)	Time information [1] (ms)
962		—	Time information [2] (ms)	Time information [2] (ms)
963		—	Time information [3] (ms)	Time information [3] (ms)
964		—	Time information [4] (ms)	Time information [4] (ms)
965		—	Time information [5] (ms)	Time information [5] (ms)
966		—	Time information [6] (ms)	Time information [6] (ms)
967		—	Time information [7] (ms)	Time information [7] (ms)
968		—	Time information [8] (ms)	Time information [8] (ms)
969		—	Time information [9] (ms)	Time information [9] (ms)
970		—	—	—
971		—	—	—
972		—	—	—
973		—	—	—
974		—	—	—
975		—	—	—

No.	Word offset	Target bit of logging data (uc_logdat_clk100m_reg)	Logging target list	
			User circuit logging mode is the non-time division mode	User circuit logging mode is the time division mode
976	62	—	Time information [0] (seconds)	Time information [0] (seconds)
977		—	Time information [1] (seconds)	Time information [1] (seconds)
978		—	Time information [2] (seconds)	Time information [2] (seconds)
979		—	Time information [3] (seconds)	Time information [3] (seconds)
980		—	Time information [4] (seconds)	Time information [4] (seconds)
981		—	Time information [5] (seconds)	Time information [5] (seconds)
982		—	Time information [0] (minutes)	Time information [0] (minutes)
983		—	Time information [1] (minutes)	Time information [1] (minutes)
984		—	Time information [2] (minutes)	Time information [2] (minutes)
985		—	Time information [3] (minutes)	Time information [3] (minutes)
986		—	Time information [4] (minutes)	Time information [4] (minutes)
987		—	Time information [5] (minutes)	Time information [5] (minutes)
988		—	—	—
989		—	—	—
990		—	—	—
991		—	—	—
992	63	—	Time information [0] (hour)	Time information [0] (hour)
993		—	Time information [1] (hour)	Time information [1] (hour)
994		—	Time information [2] (hour)	Time information [2] (hour)
995		—	Time information [3] (hour)	Time information [3] (hour)
996		—	Time information [4] (hour)	Time information [4] (hour)
997		—	Time information [0] (day)	Time information [0] (day)
998		—	Time information [1] (day)	Time information [1] (day)
999		—	Time information [2] (day)	Time information [2] (day)
1000		—	Time information [3] (day)	Time information [3] (day)
1001		—	Time information [4] (day)	Time information [4] (day)
1002		—	Time information [0] (month)	Time information [0] (month)
1003		—	Time information [1] (month)	Time information [1] (month)
1004		—	Time information [2] (month)	Time information [2] (month)
1005		—	Time information [3] (month)	Time information [3] (month)
1006		—	—	—
1007		—	—	—
1008	64	—	Time information [0] (year)	Time information [0] (year)
1009		—	Time information [1] (year)	Time information [1] (year)
1010		—	Time information [2] (year)	Time information [2] (year)
1011		—	Time information [3] (year)	Time information [3] (year)
1012		—	Time information [4] (year)	Time information [4] (year)
1013		—	Time information [5] (year)	Time information [5] (year)
1014		—	Time information [6] (year)	Time information [6] (year)
1015		—	—	—
1016		—	—	—
1017		—	—	—
1018		—	—	—
1019		—	—	—
1020		—	—	—
1021		—	—	—
1022		—	—	—
1023		—	—	—

Appendix 15 Open Source Software License

Indicates the license of the open source software used in the FPGA Module Configuration Tool.

DockPanel Suite (DockPanel Suite Theme2019)

■Overview

Library for docking window

Themes for docking window (colors and styles)

■Developer (license)

GitHub: Weifen Luo (MIT license)

■License terms

The MIT License

Copyright (c) 2007 Weifen Luo (email: weifenluo@yahoo.com)

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■Reference URL

http://dockpanelsuite.com

https://github.com/dockpanelsuite/dockpanelsuite

Nlog

■Overview

Logging library

■Developer (license)

NLog Project (BSD 3-Clause license)

■License terms

■Reference URL

https://nlog-project.org
https://github.com/NLog/Nlog

IP address control

■Overview

MFC IP input-like IP address input control

■Developer (license)

Michael Chapman (MIT license)

■License terms

IPAddressControlLib (https://github.com/m66n/ipaddresscontrollib)

Copyright (c) 2016 Michael Chapman

The MIT License (MIT)

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■Reference URL

https://github.com/m66n/ipaddresscontrollib

Appendix 16 Support

Technical support assistance service regarding FPGA module

For the technical support assistance service regarding the FPGA module, refer to the following table. If you are not sure which type the inquiry belongs to, please consult your local Mitsubishi Electric sales office or representative. Please note that Mitsubishi Electric may not be able to answer to inquiries related to FPGA development software.

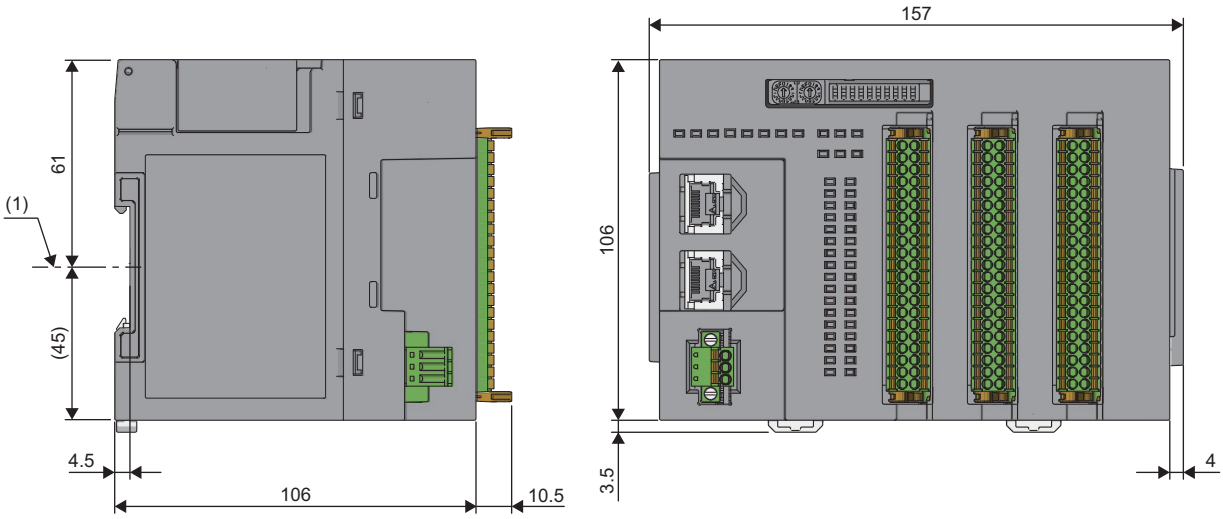
Type	Inquiry	Contact
MELSEC	• Functions and specifications of the FPGA module • Functions and specifications of FPGA Module Configuration Tool and GX Works3 • Functions and specifications of Mitsubishi Electric products (modules and MELSOFT products) to be used with the FPGA module	For further information and services, please contact your local Mitsubishi Electric sales office or representative.
FPGA development environment for the CC-Link IE TSN FPGA module	Specifications and usage of the FPGA development environment for the CC-Link IE TSN FPGA module provided by Mitsubishi Electric	For further information and services, please contact your local Mitsubishi Electric sales office or representative.
FPGA development software	Functions and specifications of Intel® Quartus Prime Design Software and ModelSim-Intel® FPGA Starter Edition	Intel Corporation: www.intel.com

A

Appendix 17 External Dimensions

The figure below shows the external dimensions of the FPGA module.

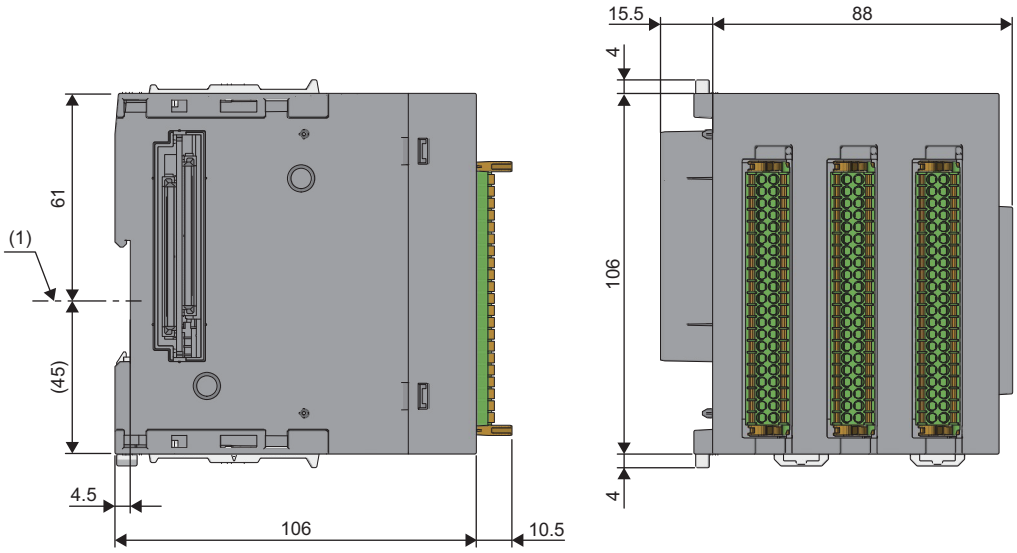
Main module



(1) DIN rail center

(Unit: mm)

Extension module



(1) DIN rail center

(Unit: mm)

MEMO

INDEX

MEMO

REVISIONS

*The manual number is given on the bottom left of the back cover.

Revision date	*Manual number	Revision
October 2023	SH(NA)-082569ENG-A	First edition

Japanese manual number: SH-082568-B

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.

However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place. Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to:

(1) Damages caused by any cause found not to be the responsibility of Mitsubishi.

(2) Loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products.

(3) Special damages and secondary damages whether foreseeable or not, compensation for accidents, and compensation for damages to products other than Mitsubishi products.

(4) Replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

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☞ Page 742 Open Source Software License

SH(NA)-082569ENG-A(2310)MEE
MODEL: CCIETSN-FPGA-U-E
MODEL CODE: 13JX7E

MITSUBISHI ELECTRIC CORPORATION

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